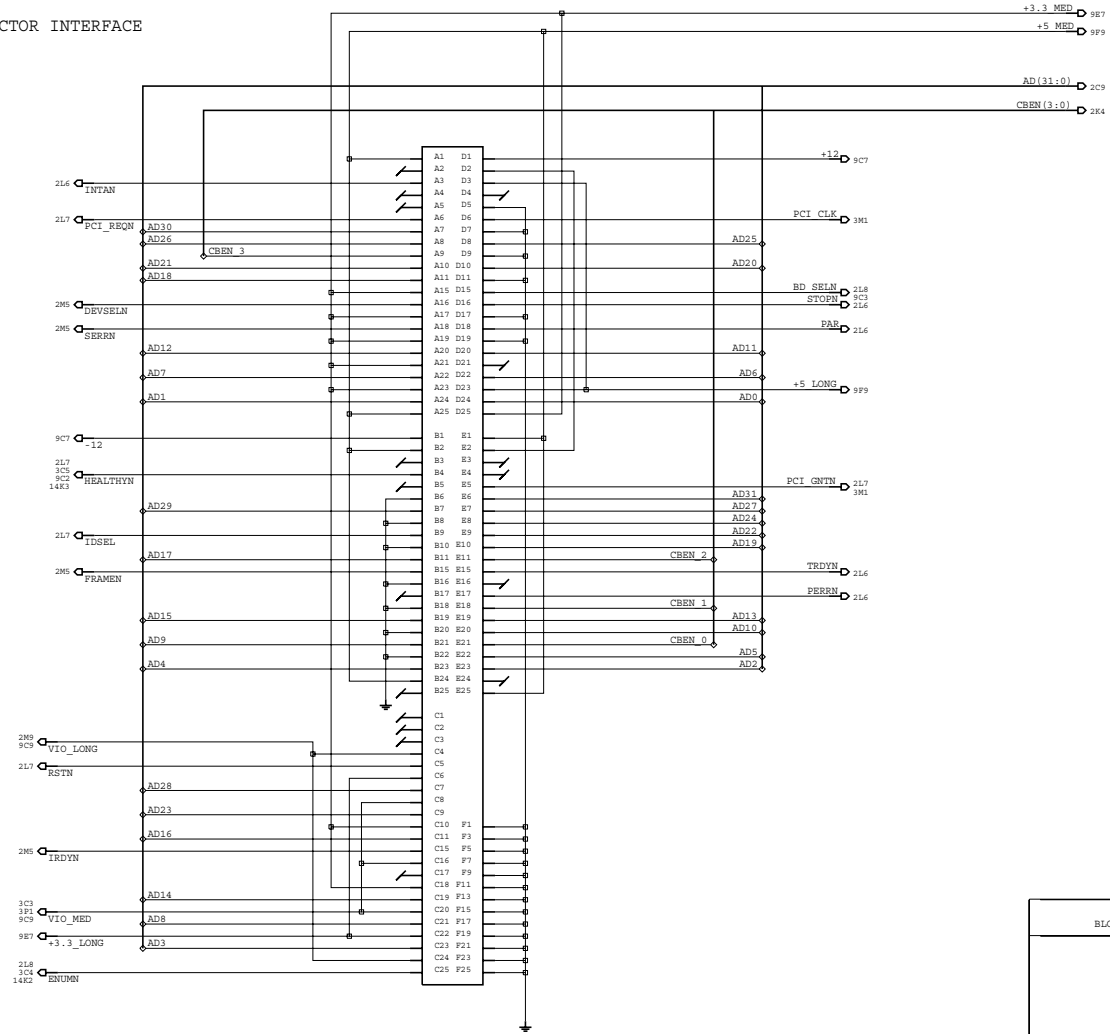


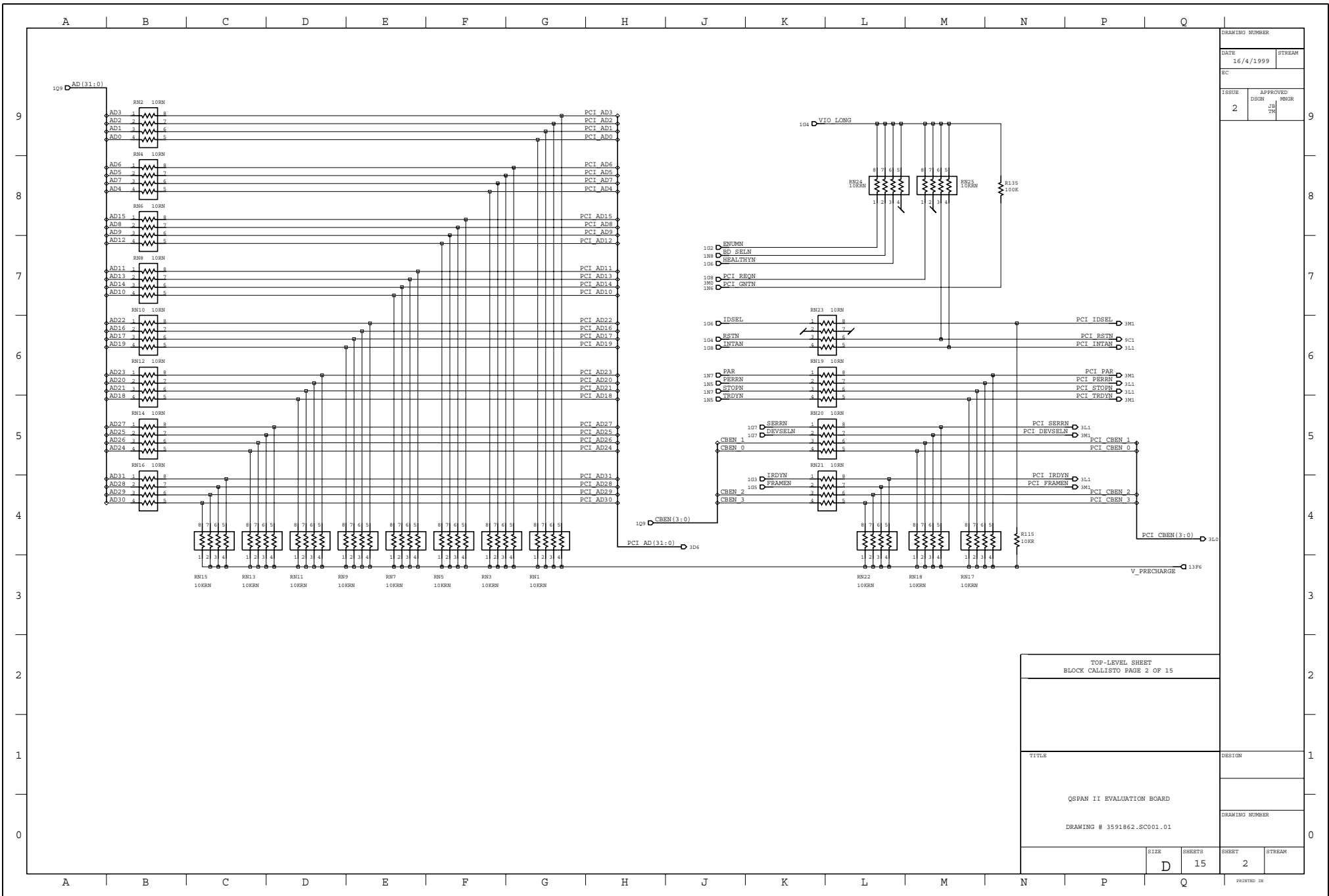
COMPACTPCI CONNECTOR INTERFACE



DRAWING NUMBER	
DATE	STREAM
16/4/1999	
EC	
ISSUE	APPROVED
2	DSGN
	JBI
	TRK

TOP-LEVEL SHEET			
BLOCK CALLISTO PAGE 1 OF 15			
TITLE		DESIGN	
QSPAN II EVALUATION BOARD			
DRAWING # 3591862.SC001.01		DRAWING NUMBER	
SIZE	SHEETS	SHEET	STREAM
D	15	1	

PRINTED IN



DRAWING NUMBER
DATE 16/4/1999
STREAM

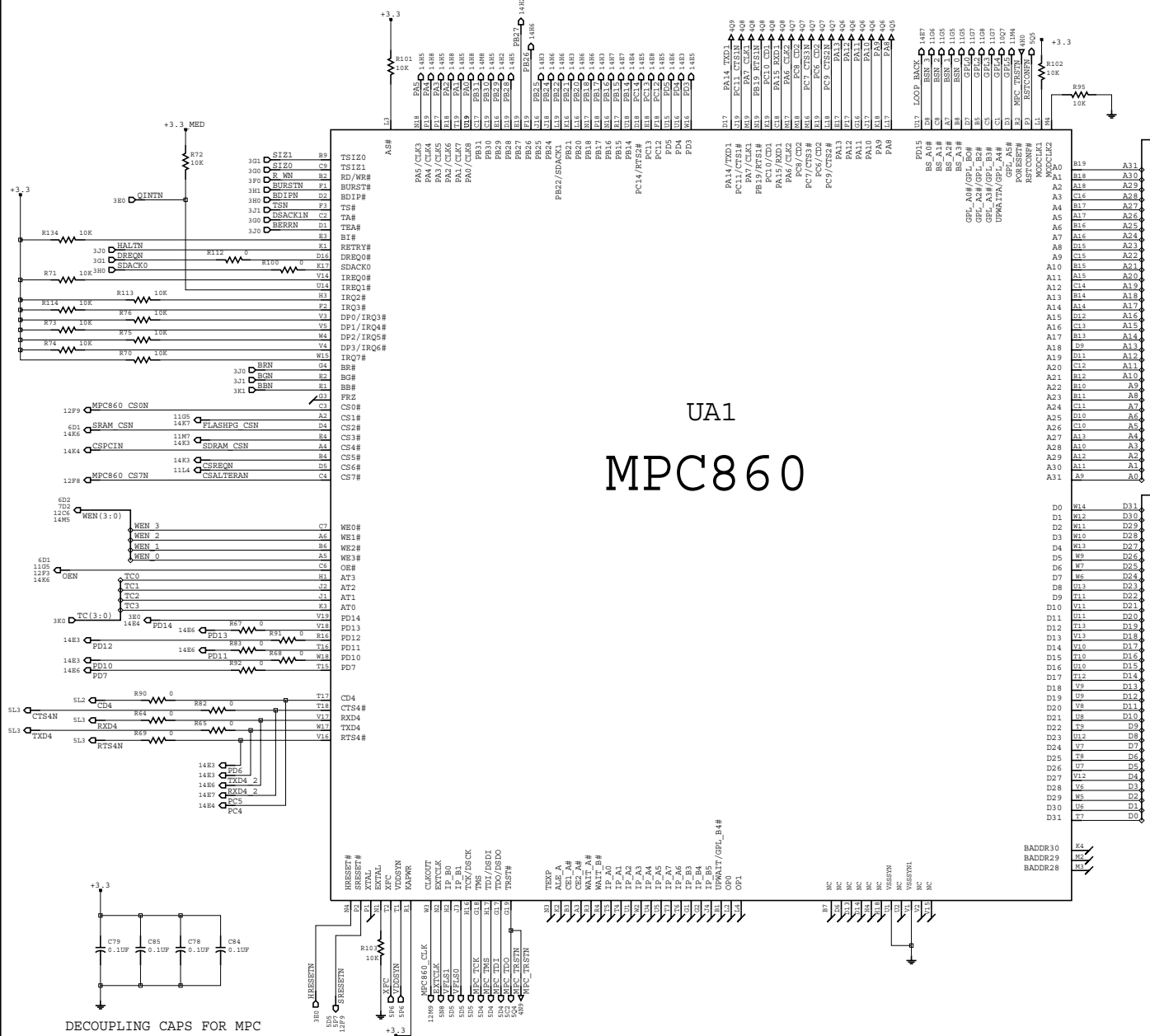
ISSUE 2
DESIGN JBT
REVISION TTK

TOP-LEVEL SHEET BLOCK CALLISTO PAGE 2 OF 15			
TITLE		DESIGN	
QSPAN II EVALUATION BOARD			
DRAWING # 3591862.SC001.01			
SIZE	SHEETS	SHEET	STREAM
D	15	2	

PRINTED IN

DRAWING NUMBER	
DATE	STREAM
16/4/1999	
ISSUE	APPROVED
2	DESIGN
	DATE
	16/4/1999

UA1 MPC860



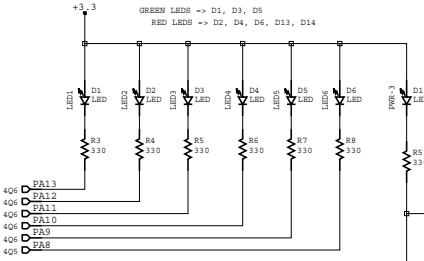
DECOUPLING CAPS FOR MPC

UA1 POWER PINS

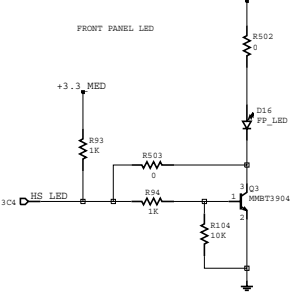
+3.3V - PINS A9, B5, B6, B7, B8, B9, E10, E11, E12, E13, E14, E15, F4, F5, F15, F16, G5, G15, H5, H15, H19, J5, J15, K5, K15, L5, L15, M1, M5, M15, N5, N15, P4, P5, P15, P16, R5, R7, R6, R8, R9, R10, R11, R12, R13, R14, R15, T14, W8.

GND - PINS P6, F7, F8, F9, F10, F11, F12, F13, F14, G6, G7, G8, G9, G10, G11, G12, G13, G14, H6, H7, H8, H9, H10, H11, H12, H13, H14, J6, J7, J8, J9, J10, J11, J12, J13, J14, K6, K7, K8, K9, K10, K11, K12, K13, K14, L6, L7, L8, L9, L10, L11, L12, L13, L14, M6, M7, M8, M9, M10, M11, M12, M13, M14, M6, M7, M8, M9, M10, M11, M12, M13, M14, N6, F7, F8, F9, F10, F11, F12, F13, F14.

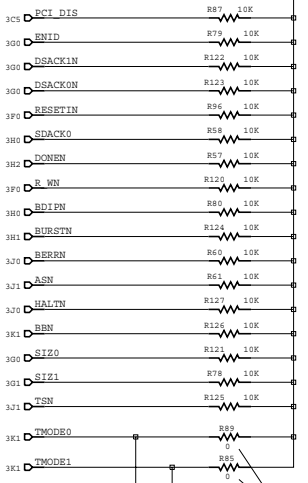
TOP-LEVEL SHEET BLOCK CALLISTO PAGE 4 OF 15			
TITLE	DESIGN		
QSPAN II EVALUATION BOARD			
DRAWING # 3591862.SC001.01			
SIZE	SHEETS	SHEET	STREAM
D	15	4	



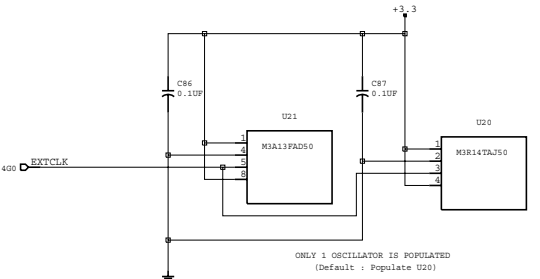
GENERAL PURPOSE LEDs



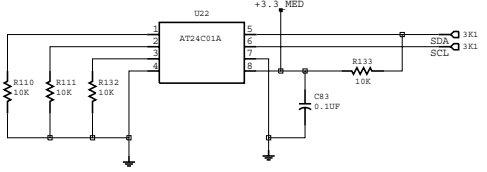
FRONT PANEL LED



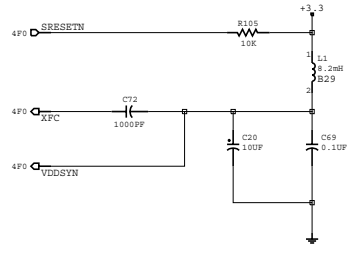
Default : Do not populate R85 and R88



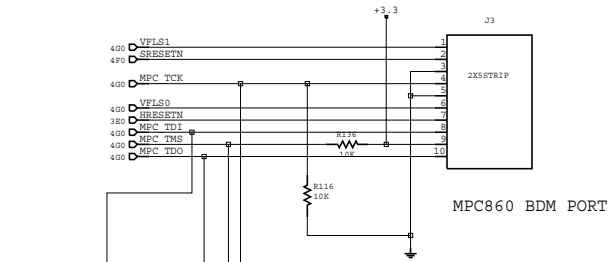
ONLY 1 OSCILLATOR IS POPULATED (Default : Populate U20)



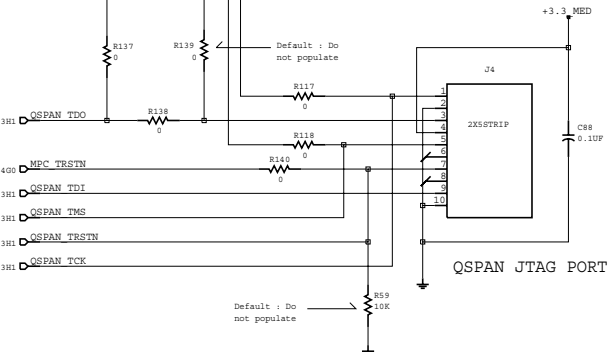
AT24C01A



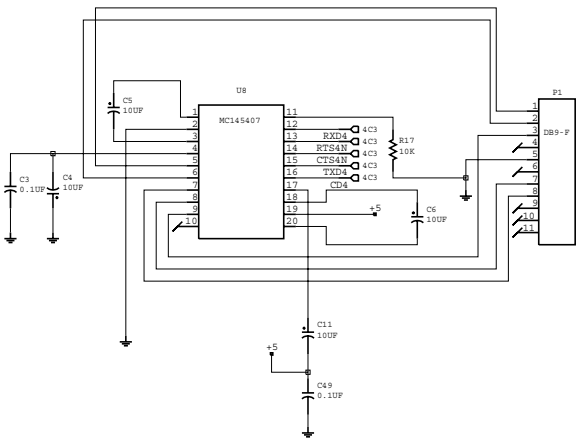
POWER ON RESET CIRCUIT FOR MPC860



MPC860 BDM PORT

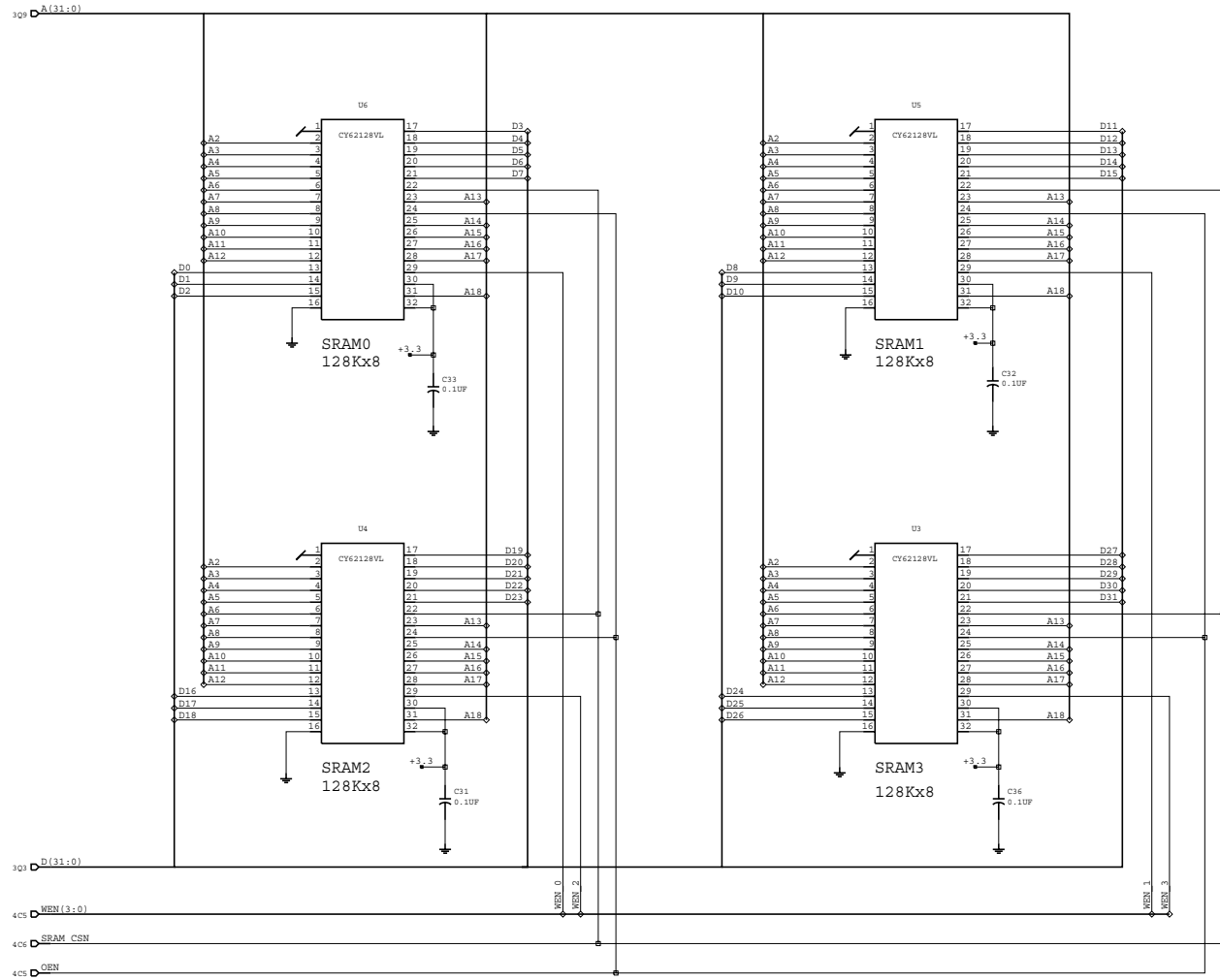


QSPAN JTAG PORT



TOP-LEVEL SHEET			
BLOCK CALLISTO PAGE 5 OF 15			
TITLE		DESIGN	
QSPAN II EVALUATION BOARD			
DRAWING # 3591862.SC001.01		DRAWING NUMBER	
SIZE	SHEETS	SHEET	STREAM
D	15	5	

STATIC RAM



DRAWING NUMBER	
DATE	STREAM
16/4/1999	
EC	
ISSUE	APPROVED
2	DSGN JBT HWER TW

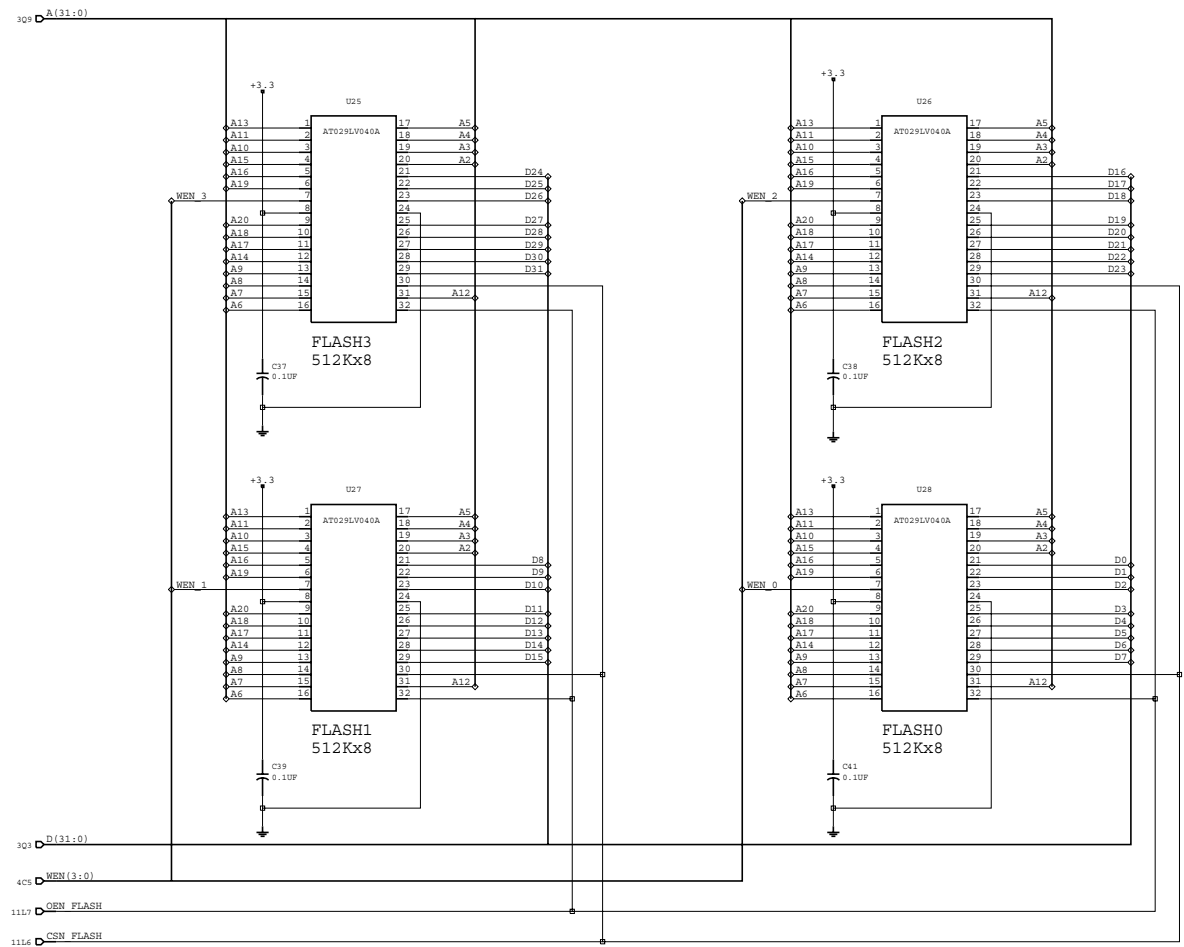
TOP-LEVEL SHEET BLOCK CALLISTO PAGE 6 OF 15			
TITLE		DESIGN	
QSPAN II EVALUATION BOARD			
DRAWING # 3591862.SC001.01		DRAWING NUMBER	
SIZE	SHEETS	SHEET	STREAM
D	15	6	

PRINTED IN

A B C D E F G H J K L M N P Q

DRAWING NUMBER	
DATE	STREAM
16/4/1999	
EC	
ISSUE	APPROVED
2	DSGN JBT HWER TW

FLASH

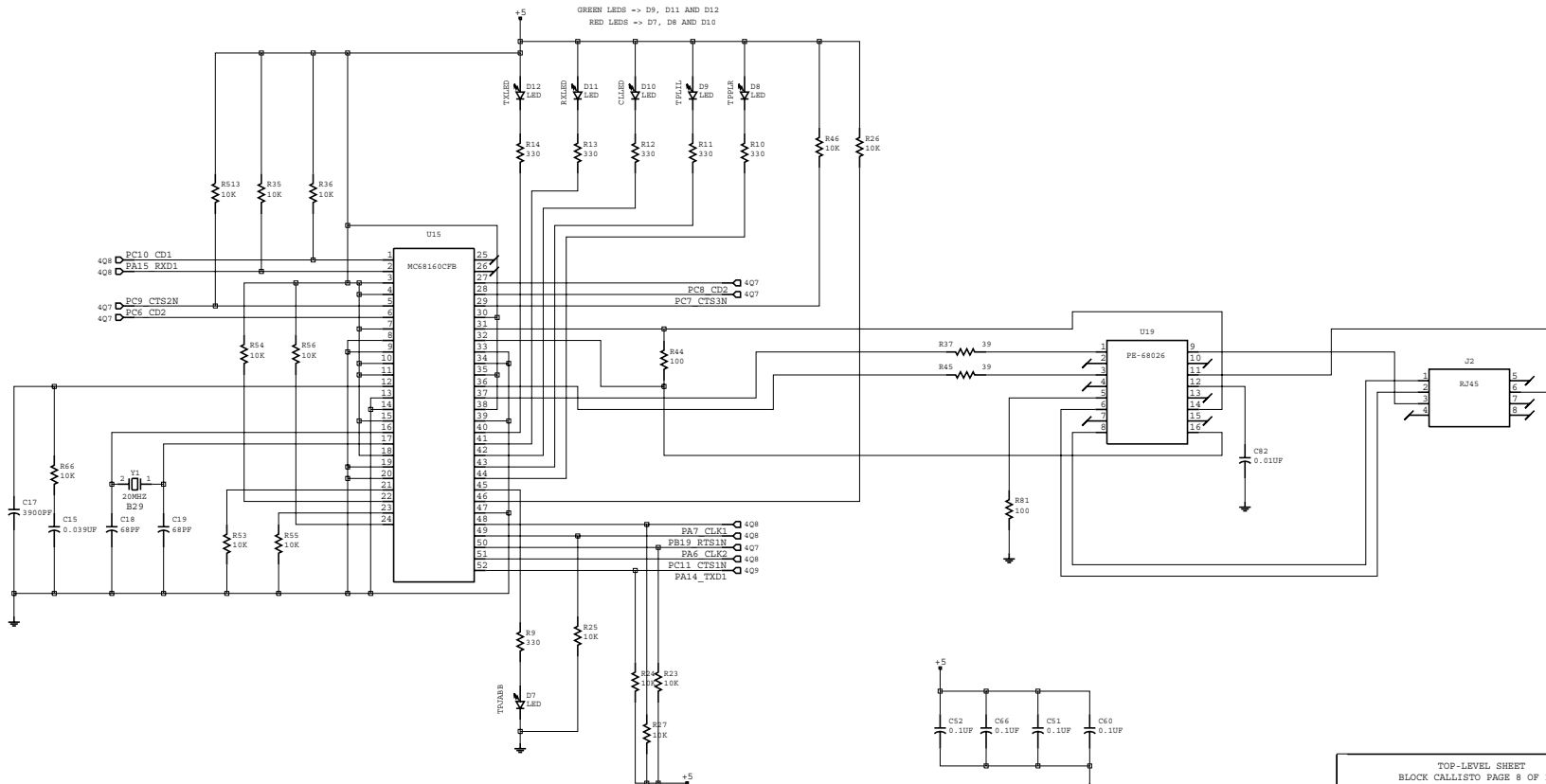


TOP-LEVEL SHEET BLOCK CALLISTO PAGE 7 OF 15			
TITLE			
QSPAN II EVALUATION BOARD			
DRAWING # 3591862.SC001.01			
SIZE	SHEETS	SHEET	STREAM
D	15	7	

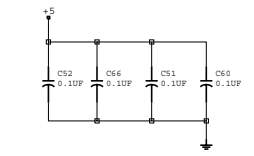
A B C D E F G H J K L M N P Q PRINTED IN

DRAWING NUMBER	
DATE	STREAM
16/4/1999	
DC	
ISSUE	APPROVED
2	DSGN JBT
	HWDR TW

ETHERNET



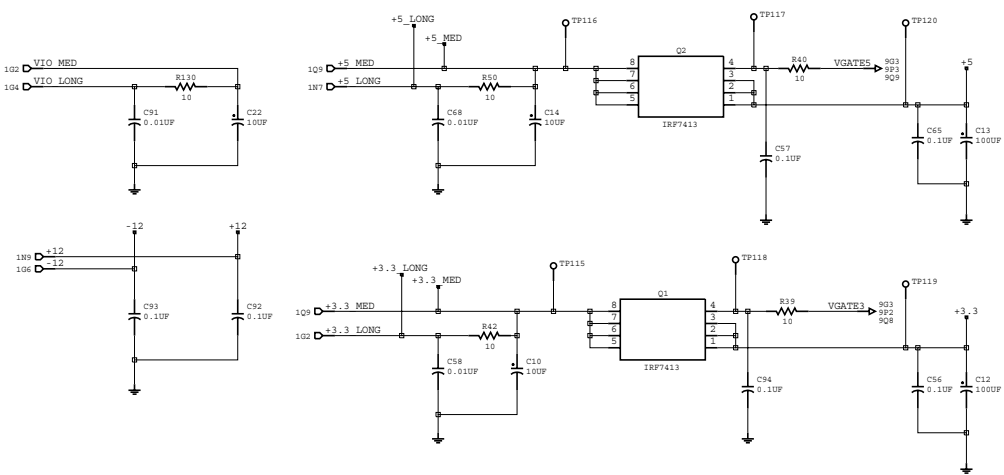
GREEN LEDES -> D9, D11 AND D12
RED LEDES -> D7, D8 AND D10



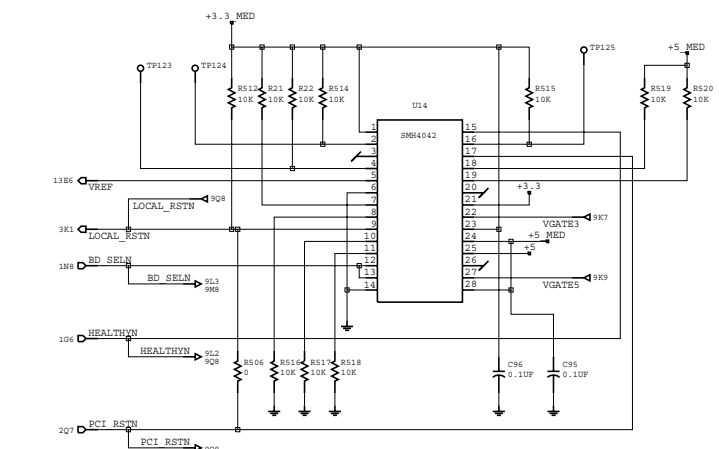
DECOUPLING FOR ETHERNET

TOP-LEVEL SHEET BLOCK CALLISTO PAGE 8 OF 15			
TITLE		DESIGN	
QSPAN II EVALUATION BOARD			
DRAWING # 3591862.SC001.01			
SIZE	SHEETS	SHEET	STREAM
D	15	8	

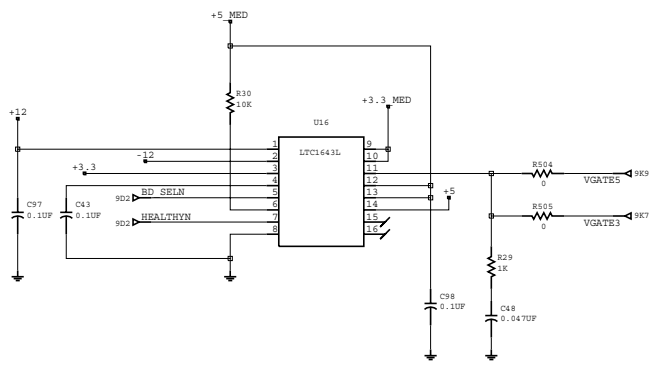
DRAWING NUMBER	
DATE	STREAM
16/4/1999	
EC	
ISSUE	APPROVED
2	DSGN
	JBT
	TM



HOT SWAP CONTROLLER OPTION #3
 When using S39421, do not populate
 U14, U16, R504, R505 and R506.

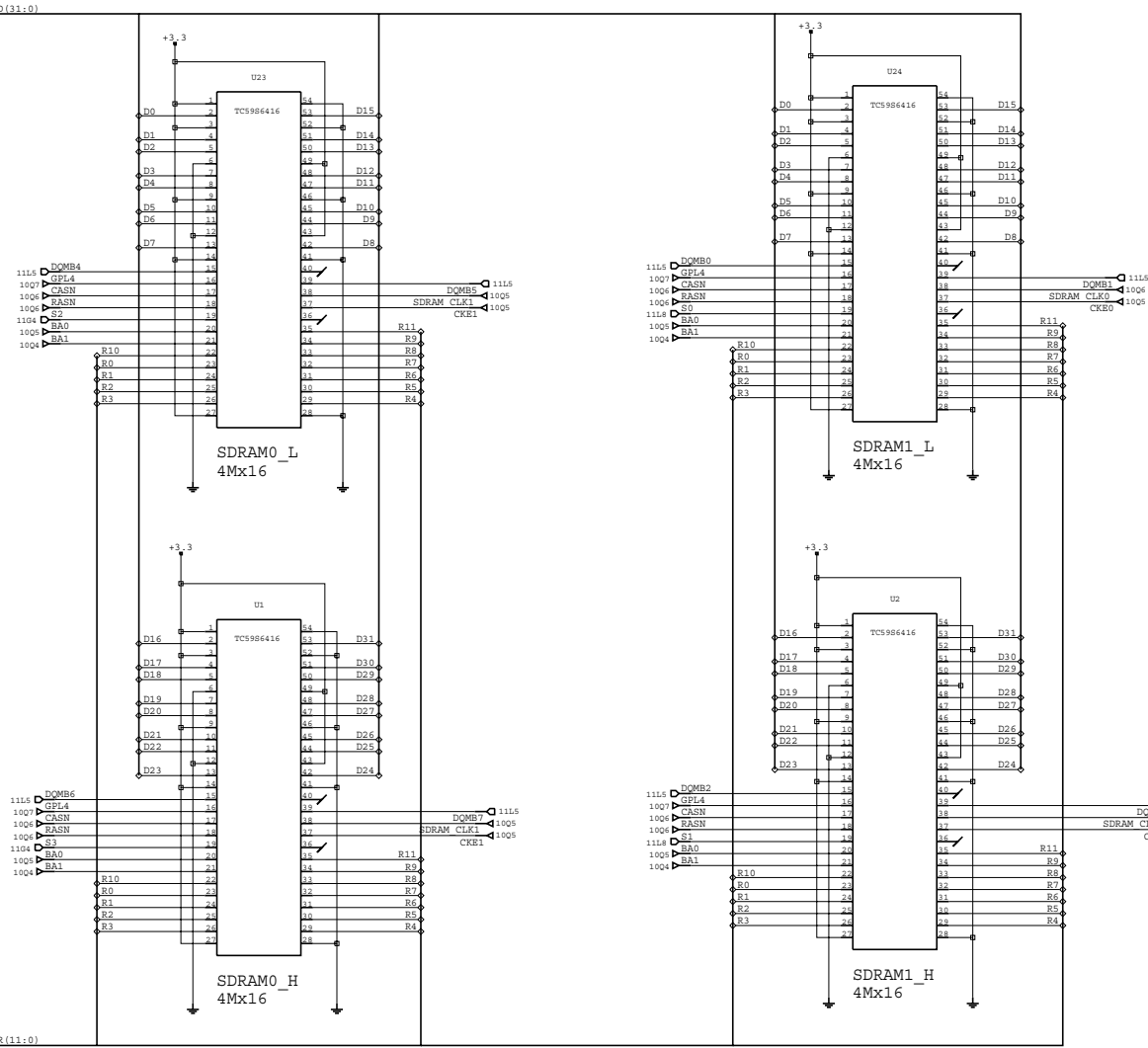
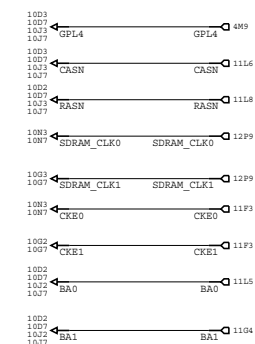
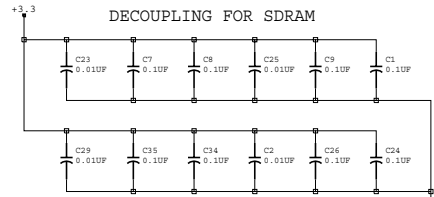


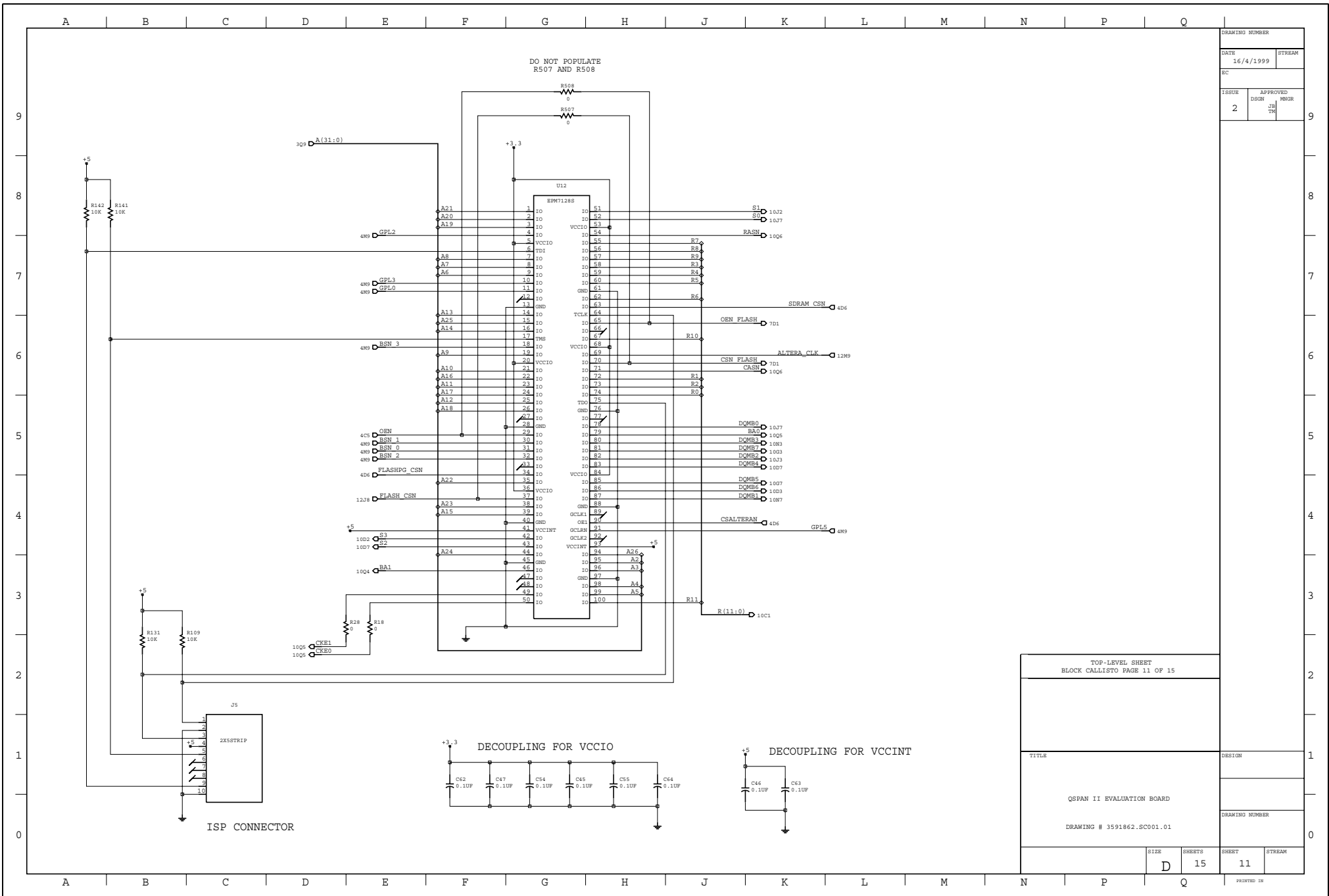
HOT SWAP CONTROLLER OPTION #1
 When using SMH4042, do not populate
 U16, U30, R504, R505 and R506.



HOT SWAP CONTROLLER OPTION #2
 When using LTC1643L, do not populate
 U14 and U30.

TOP-LEVEL SHEET BLOCK CALLISTO PAGE 9 OF 15			
TITLE		DESIGN	
QSPAN II EVALUATION BOARD			
DRAWING # 3591862.SC001.01			
SIZE	SHEETS	SHEET	STREAM
D	15	9	





DRAWING NUMBER

DATE 16/4/1999

STREAM

EC

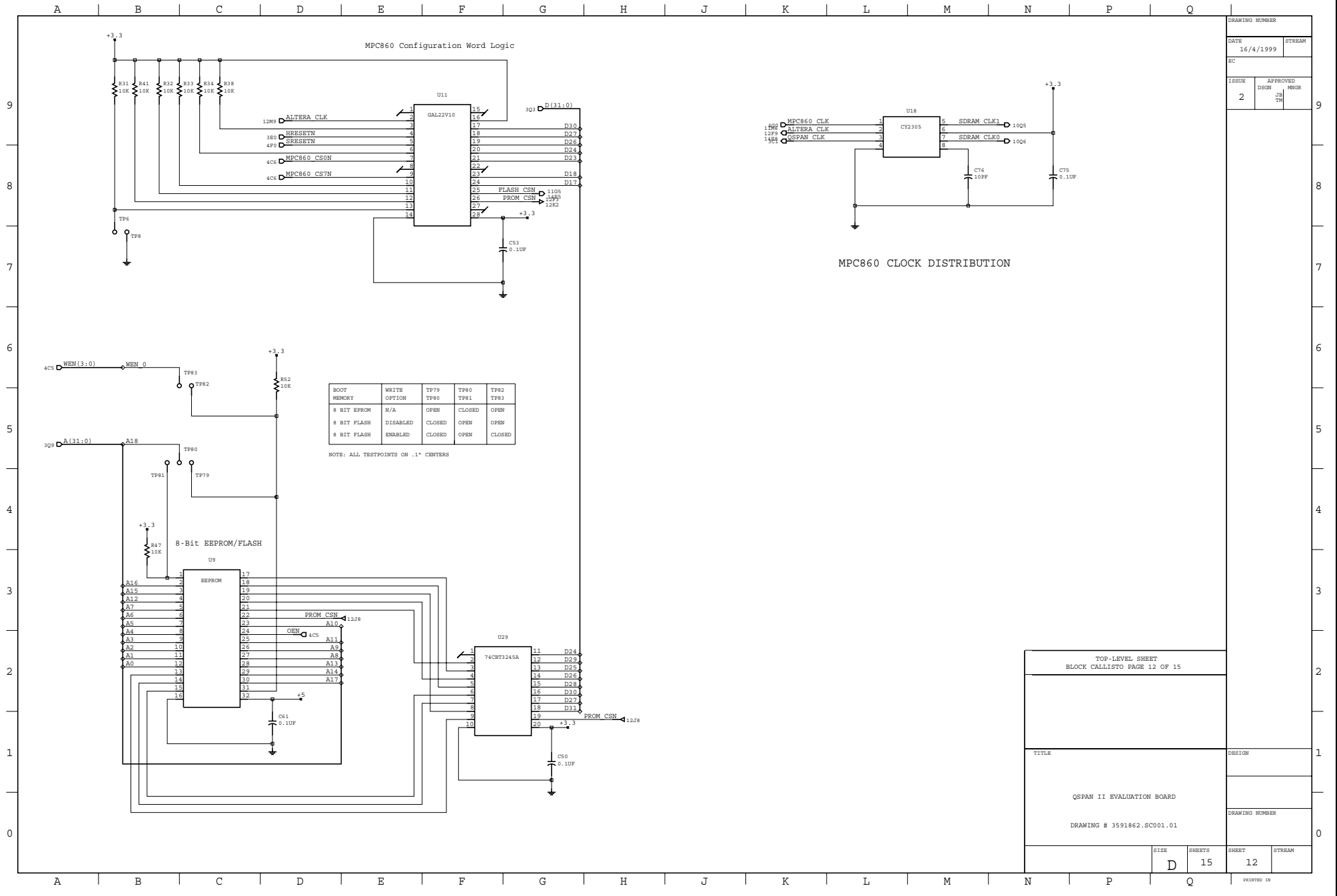
ISSUE 2

APPROVED DSGN JBT

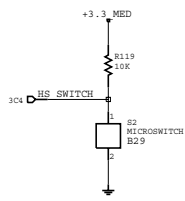
REVISOR TW

TOP-LEVEL SHEET BLOCK CALLISTO PAGE 11 OF 15			
TITLE		DESIGN	
QSPAN II EVALUATION BOARD			
DRAWING # 3591862.SC001.01			
SIZE	SHEETS	SHEET	STREAM
D	15	11	STREAM

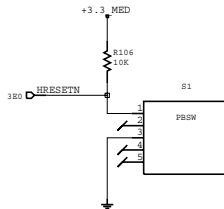
PRINTED IN



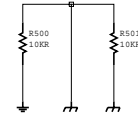
DRAWING NUMBER	
DATE	STREAM
16/4/1999	
ISSUE	APPROVED
2	DESIGN
	DATE
	16/4/1999



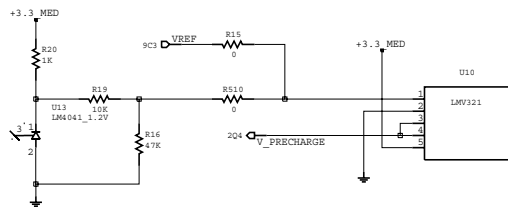
EJECTOR HANDLE SWITCH



PUSHBUTTON RESET



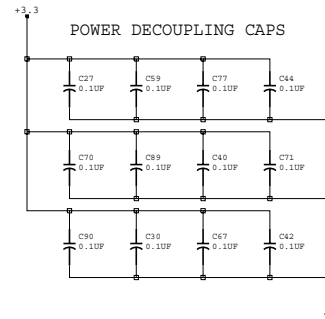
ESD PROTECTION CIRCUIT



PRECHARGE VOLTAGE REFERENCE SUPPLY

For SMH4042 Hot Swap Controller :
Populate R15 and R510 is left open.

For S39421 and LTC1643L Hot Swap Controllers :
Populate R510 and R15 is left open.



POWER DECOUPLING CAPS

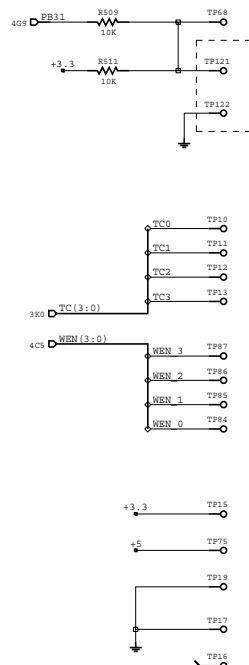
DRAWING NUMBER			
DATE	STREAM		
16/4/1999			
EC			
ISSUE	DESIGN	APPROVED	NUMBER
2		JBTW	
TOP-LEVEL SHEET BLOCK CALLISTO PAGE 13 OF 15			
TITLE		DESIGN	
QSPAN II EVALUATION BOARD			
DRAWING # 3591862.SC001.01		DRAWING NUMBER	
SIZE	SHEETS	SHEET	STREAM
D	15	13	
PRINTED IN			

DRAWING NUMBER	
DATE	STREAM
16/4/1999	
EC	
ISSUE	APPROVED
2	DSGN JBT
	HWER TW

GENERAL PURPOSE TESTPOINTS

NOTE: ALL TESTPOINTS ARE ON .1" CENTERS

12M9	ALTERA CLK	TP9	409	DA0	TP27	301	TSN	TP104
301	BREQN	TP70	409	DA2	TP36	321	SCL	TP100
439	EC13	TP64	409	DA4	TP42	300	HALTN	TP97
408	EC11 CTS1N	TP93	407	DA6 CLK2	TP47	380	QINTN	TP95
407	EC9 CTS2N	TP52	405	DA8	TP48	300	BRN	TP105
407	EC7 CTS3N	TP41	406	EA10	TP57	321	BRN	TP112
482	EC5	TP35	406	EA12	TP42	390	RESETIN	TP103
439	FB15	TP98	409	EA14 TXD1	TP77	380	BDIPN	TP102
489	LOOP_BACK	TP32	489	EB16	TP18	406	FLASHPG_CSN	TP94
404	ED13	TP52	489	EB18	TP44	405	OEN	TP92
404	ED11	TP55	489	EB20	TP55	406	SRAM_CSN	TP107
482	RXD4_2	TP53	489	EB22	TP51	300	SIZ0	TP99
404	ED7	TP51	489	EB24	TP51	309	TEST2	TP90
439	ED5	TP38	489	EB26	TP61	309	TEST1	TP89
439	ED3	TP2	409	EB28	TP7	309	TEST0	TP88
1228	FLASH_CSN	TP7	409	EB30	TP78	304	HS_SWITCH	TP4
439	EC14	TP92	409	EA1	TP9	380	SDACK0	TP113
439	EC12	TP59	409	EA3	TP43	300	BBERN	TP114
408	EC10_CD1	TP9	409	EA5	TP4	301	BREQN	TP111
407	EC8_CD2	TP49	408	DA7 CLK1	TP50	380	CSPCIN	TP106
407	EC6_CD2	TP53	406	EA9	TP5	405	CSN	TP98
482	FC4	TP26	406	EA11	TP60	301	BGN	TP96
439	FB14	TP9	406	EA13	TP4	380	HRESETN	TP96
404	ED14	TP34	408	DA15 RXD1	TP77	380	BURSTN	TP9
404	ED12	TP29	489	EB17	TP4	300	DSACK1N	TP110
404	ED10	TP20	489	EB19 RTS1N	TP46	406	SDRAM_CSN	TP91
483	RXD4_2	TP30	408	EB21	TP7	381	CSBREQN	TP109
483	ED6	TP21	489	EB23	TP7	390	B_MN	TP108
439	ED4	TP33	380	SDACK0	TP58	301	SIZ1	TP101
			489	EB25	TP54	106	HEALTHYIN	TP1
			489	EB27	TP66	305	PCI_DIS	TP2
			409	EB29	TP65	304	PMEN	TP3
						102	ENUNN	TP5



TOP-LEVEL SHEET BLOCK CALLISTO PAGE 14 OF 15			
TITLE		DESIGN	
QSPAN II EVALUATION BOARD			
DRAWING NUMBER		DRAWING # 3591862.SC001.01	
SIZE	SHEETS	SHEET	STREAM
D	15	14	

