NEC

USER'S MANUAL

CB-C7 FAMILY

CELL-BASED IC

(PRELIMINARY)

ANALOG MACRO COMMON

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

INTRODUCTION

This manual describes the functions of analog macros used when integrating analog circuits into the CB-C7 family of 0.8 μm-rule CMOS cell-based IC.

The CB-C7 family allows integration of a large-scale system on a single chip corresponding to your systems that includes analog macros and digital circuits such as CPU macros, peripheral macros, memory macros, and user logic.

A variety of analog macros are available such as high-speed A/D converters for image processing, D/A converters, comparator, 3 V driven general-purpose A/D converters, D/A converters, and analog switches.

For individual information on the above macros, refer to the user's manual – individual part by macro (To be published) in question.

For how to design a circuit with the CB-C7 family, refer to **CB-C7 FAMILY USER'S MANUAL DESIGN PART**. Read the design manual before reading this manual.

Note that the analog macros have features and constraints different from those of digital macros. This manual describes the features and constraints peculiar to the analog macros. Be sure to read through this manual when using the analog macros. Be especially familiar with the constraints on test design and layout.

This manual is a preliminary version and its contents are subject to change without notice. Confirm the latest information on the analog macro when designing your circuits.

CONTENTS

CHAPTER 1 MACRO AREA

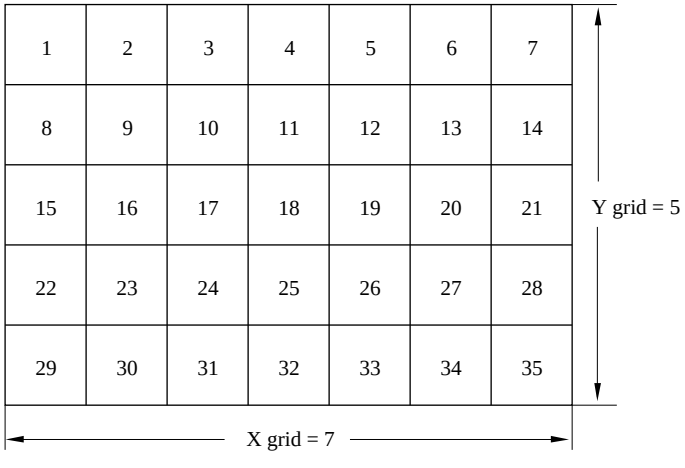
The macro area is expressed using the number of grids as the unit.

Note that this value does not include the wiring area. The actual chip area is the total of the macro area and the wiring area.

For the macro area of each macro, refer to the user's manual-individual part by macro.

Number of grids = X grids (size in X direction) × Y grids (size in Y direction)

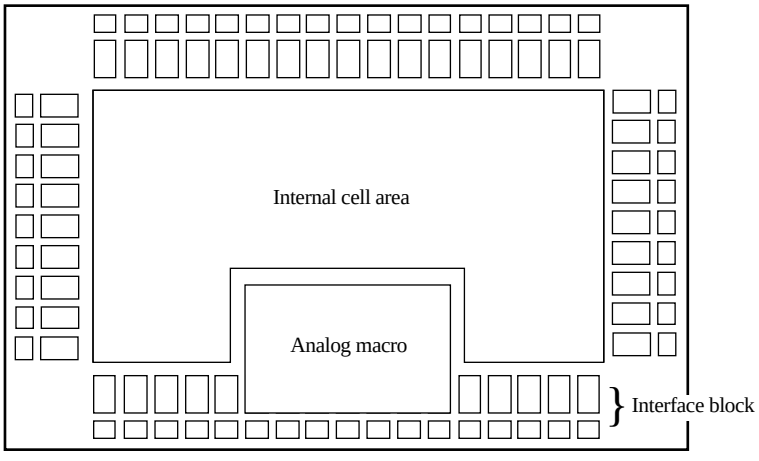
The number of grids is the index which indicates the circuit area for the CB-C7 family.
For example, the circuit shown below is expressed as 35 grids.



1.1 Macro Area of Analog Macro

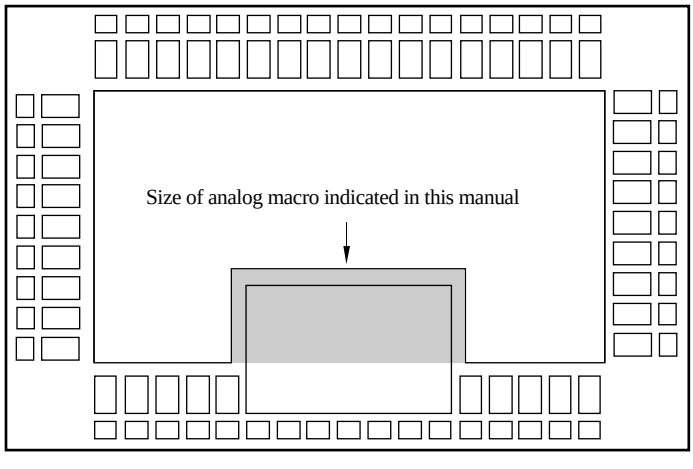
An analog macro actually consists of the internal cell area and interface blocks as shown in Fig. 1-1. As it is, however, it is complicated to estimate the chip size when other circuits are included.

Fig. 1-1 Configuration Including Interface Block



With the analog macros, therefore, only the macro size of internal cells is indicated (see Fig. 1-2), so that the area of the analog macro can be estimated in the same manner as that of other circuits.

Fig. 1-2 Configuration of Internal Cell Area Only



Constraints on the number of pins and layout are not taken into consideration here. In actual use, usable package type and allowable macro location depend on the macro selected, and layout restrictions when incorporating two or more analog macros are specified. For the layout restrictions, refer to **CHAPTER 7 LAYOUT**. For details, consult NEC's sales persons.

Table 1-1 Macro Area

Functions	Area (Number of grids)
8-bit 20 Msps A/D converter	25400
8-bit general purpose A/D converter	10300
8-bit 20 Msps D/A converter	27500
8-bit general purpose D/A converter	7800
Analog switch	1000
comparator	1600

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CHAPTER 2 NOTES ON DESIGNING

An analog macro has features and constraints different from those of other macros. Design your circuit, taking the following points into consideration, when integrating an analog macro.

2.1 Electrical Specifications

Because analog macros handle analog signals, their circuit characteristics vary depending on the operating conditions, and it is difficult to judge, from the electrical characteristic values, whether the analog macro can be used under given conditions. It is therefore recommended that the characteristics be confirmed on a bread board by using a sample of a single analog macro for evaluation. Samples for evaluation are available from NEC upon request.

Each characteristic value shown in the Electrical Specifications is the specification of the macro itself, and may change depending on digital circuits on the same chip, layout of the macros, pin configuration, and package.

2.2 Designing for Testing

Each analog macro is tested as a separate unit to guarantee the characteristics of the macro. The test circuit must therefore be configured so that each macro can be separately tested. For details, refer to **4.2 Test Circuit**.

This section describes important points only.

- **Be sure to connect TBI×× and TBO×× to external pins without changing signal polarities.**
- **Connect analog pins and analog power sources to external pins directly, not via interface blocks.**

2.3 Simulation

Analog macros are treated as digital modules for simulation.

Therefore, analog signals cannot be input from analog pins during the entire circuit simulation.

The total chip simulation for a chip which incorporates analog macros can be carried out in two modes: actual operating mode and total logic circuit test mode.

Input low or high level to the input pins irrelevant to simulation (such as analog macro power supply pins and reference voltage input pins). Do not input X(Don't care) or Z(High-impedance) to those pins during simulation.

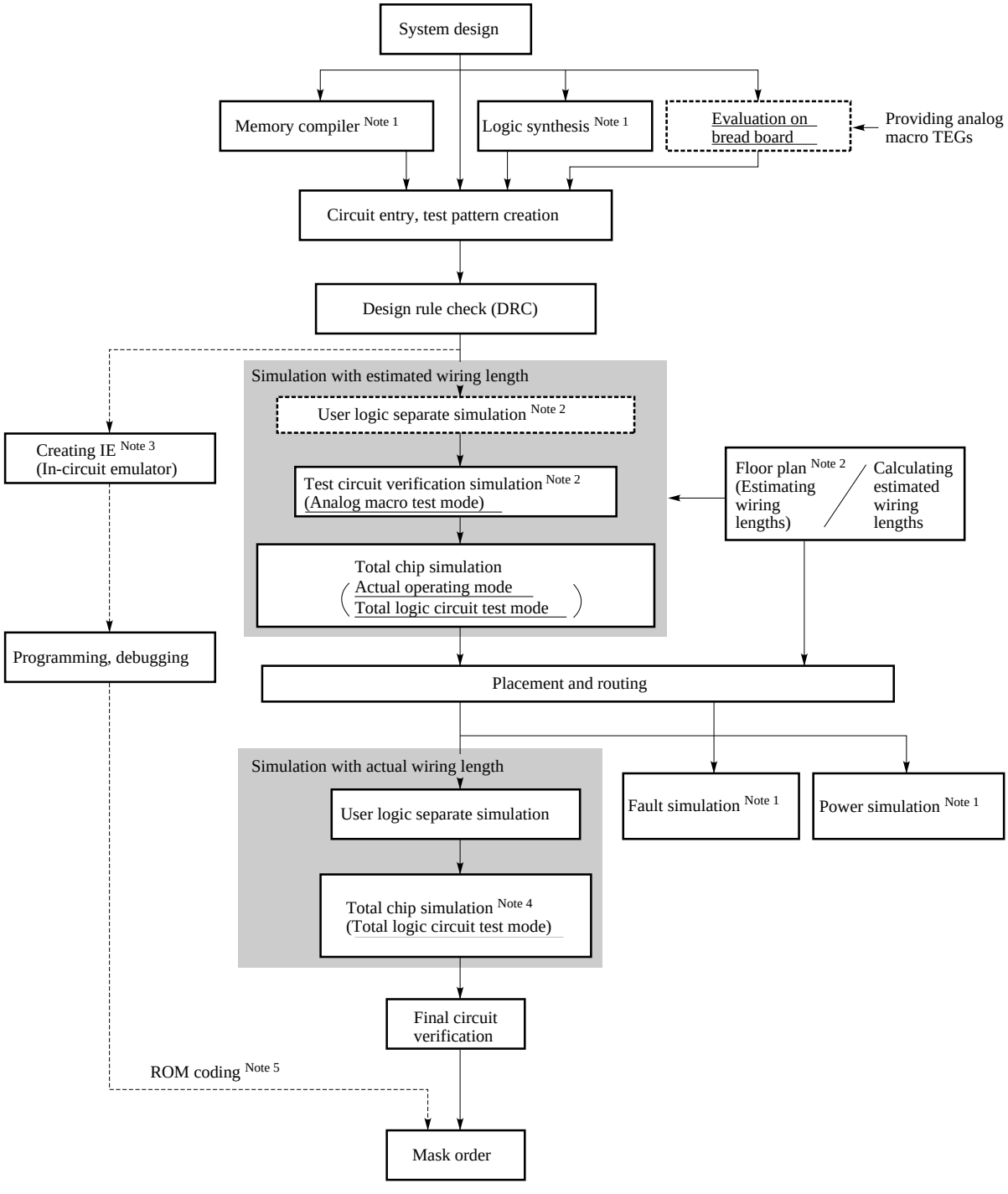
For details, refer to **CHAPTER 5 SIMULATION**.

2.4 Power Consumption Estimation

The power consumed by analog macros is the sum of the AC components which vary with the operating frequency and the DC components independent of the operating frequency.

For details, refer to **CHAPTER 6 POWER CONSUMPTION ESTIMATION**.

The modes underlined in the figure are unique test modes required in incorporating analog macros.



Note 1. Some tools do not support these functions (option function).

2. Required only when a megafunction is incorporated.

3. Required only when the CPU macro is incorporated.

4. When the circuit to be simulated also handles bidirectional signals, the simulation with actual wiring length is not currently available (to be released).

5. Required only when a ROM macro is incorporated.

3.1 Description of Development Flow

Item	Description
System design	Before designing details, specifications are designed to realize necessary functions efficiently and at low cost.
Memory compiler	Necessary RAM/ROM can be easily created by specifying bit width and number of words.
Logic synthesis	Circuit design in gate level can be automatically performed with Verilog-HDL description.
Design rule check (DRC)	Checks whether the circuit is designed in accordance with given rules.
User logic separate simulation	When using an analog macro, it is recommended that the user logic is first simulated as a separate unit to eliminate errors and then the entire circuit is simulated for efficient development.
Test circuit verification simulation (analog macro test mode)	Analog macro test mode is necessary for integrating analog macros. This mode is used to test analog macros only. It is confirmed at shipment through simulation whether analog macros can be tested using a standard test pattern.
Floor plan	Layout of the analog macros and the user logic on chip is determined. Expected value of estimated wiring length is obtained. In addition, chip size is roughly estimated.
Estimated wiring length	Taking block dividing in second hierarchy of the circuit into consideration, estimated wiring length between blocks is calculated from estimated wiring length of each block and the step size used.
Total chip simulation (actual operating mode, total logic circuit test mode)	When an analog macro is integrated, the macro should be checked in the actual operating mode and the total logic circuit test mode. User operates analog macros in this mode. The actual operating mode is used mainly to test the logic portion. In the total logic circuit test mode, the logic circuits excluding analog circuits are tested as a whole.
Power simulation	Power consumption can be obtained in time units. Therefore, inputting a test pattern close to actual operation is recommended.
Fault simulation	Fault detection rate of user-created test pattern to each circuit is calculated. In addition, cell information that cannot be detected with the test pattern is output.
Actual wiring length simulation	User logic simulation and total chip simulation are carried out with actual wiring length.
Preparation for IE creation	When integrating a CPU macro, an in-circuit emulator that helps development of application software should be created.

CHAPTER 4 DESIGNING TEST CIRCUIT

In developing an ASIC, designing a test circuit is of vital importance.

This chapter describes the test functions of analog macros. This test function is necessary for designing CB-C7 integrating analog macros.

4.1 Test Pattern

In development of the CB-C7 family, each internal block is simulated in the following three stages, unlike the case in which a circuit consists of only user logic. When an analog macro is integrated, confirmation must be made in three special test modes (actual operating mode, analog macro test mode, and total logic circuit test mode), unlike the case in which a circuit consists of only digital circuits such as megafunctions.

(1) User logic separate simulation

The detailed functions of each user logic is checked as a separate unit.

(2) Test circuit verification simulation

The test bus that tests the internal functions of analog macros is checked.

The pattern to verify the internal functions of analog macros has been created by NEC.

When an analog macro is integrated, verification is performed in the following mode:

- **Analog macro test mode**

  This mode is used to test the analog macro only.

(3) Total chip simulation

Interconnection between the analog macro, user logic, and interface block is checked.

When the analog macro is integrated, verification is performed in the following two modes:

- **Actual operating mode**

  Mainly tests the logic parts. The analog macros incorporated are actually operated by users in this mode.

- **Total logic circuit test mode**

  Tests the logic circuits as a whole excluding analog circuits.

4.2 Test Circuit

To create a chip in which analog and digital circuits exist, a special circuit that separately checks the following items is necessary:

Characteristics of analog macros
User logic circuit connected to analog macros

Every analog macro is internally provided with a circuit that tests the above items, which is capable of testing each of digital and analog circuit by switching with the test mode select pin.

Configure a control circuit and control signals so that the test circuit can execute each simulation mode. Examples of circuits that test an A/D converter and D/A converter are given below.

For the circuit that tests analog switches and comparators, refer to the user's manual-individual part by macro.

4.2.1 Example of Analog Macro Configuration

The circuits to test A/D converters and D/A converters of analog macros are shown below.

Fig. 4-1 A/D Converter

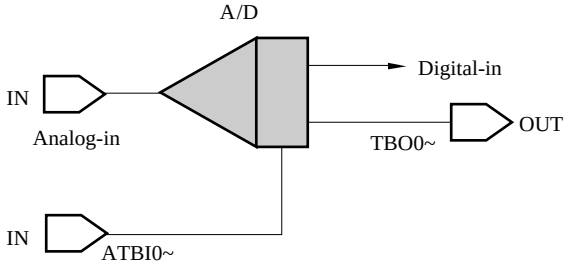
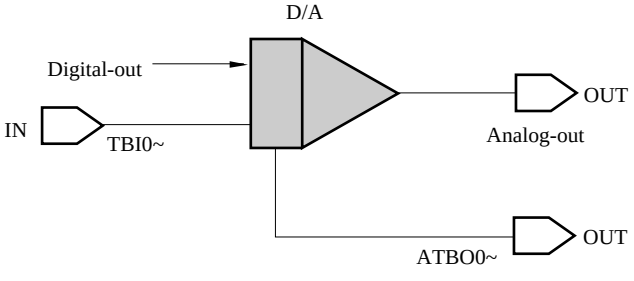


Fig. 4-2 D/A Converter



4.2.2 Test Mode

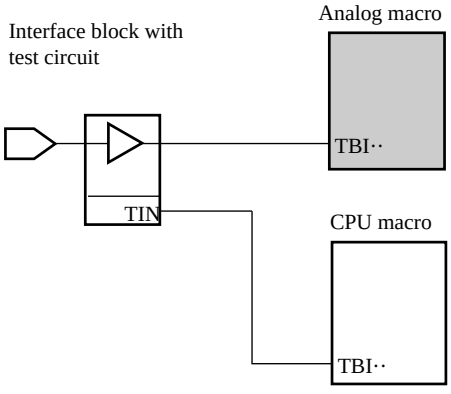
(1) Analog macro test mode

This mode is used to test analog macros only.

By inputting test data from the test input pin with a dedicated tester, operation of the analog macro is verified. Creating a test pattern for this purpose is not necessary.

An interface block can be shared by connecting the normal pin and the test pin of an interface block with test circuit to the TBI×× pin of an analog macro and the TBI×× pin of another macro, respectively, to reduce the number of interface blocks. For the interface block with test circuit, refer to **CB-C7 FAMILY USER'S MANUAL DESIGN PART**.

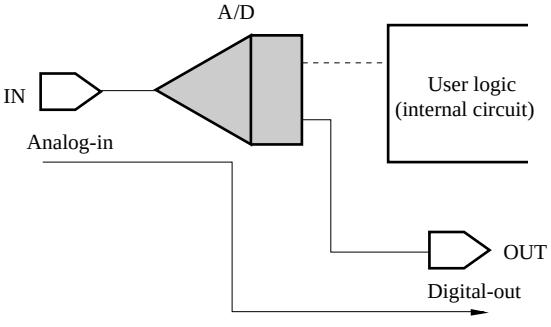
Fig. 4-3 Connection to an Interface Block with Test Circuit



A/D converter

An analog signal is input to the A/D converter, and the converted digital signal is output to an external circuit through the test circuit, to check the A/D converter.

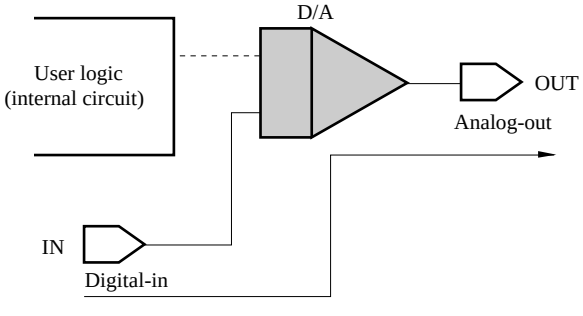
Fig. 4-4 A/D Converter



D/A converter

A digital signal is input to the D/A converter through the test circuit from an external circuit, to check the D/A converter.

Fig. 4-5 D/A Converter



(2) Actual operating mode

In this mode, the user actually uses the analog macro. The logic portion is mainly tested when simulation is executed. Especially in the case of D/A converters, create data (00, FF) input to the D/A converter so that the zero- and full-scale values are output.

Fig. 4-6 A/D Converter

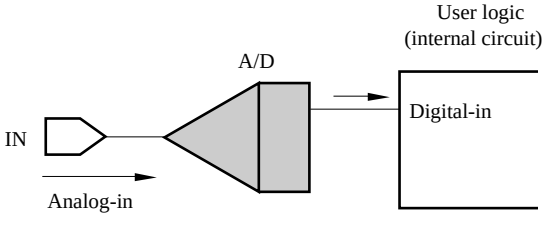
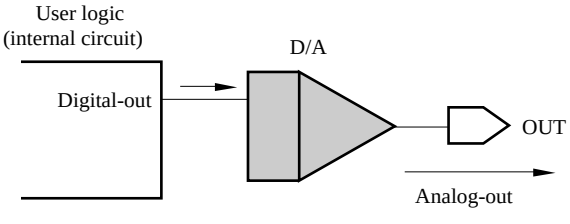


Fig. 4-7 D/A Converter



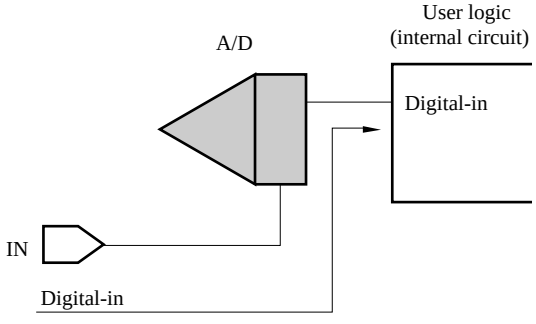
(3) Total logic circuit test mode

This mode is used to test a user logic circuit that interfaces with an analog macro. This mode is provided, because it is difficult, with an analog macro incorporated, to test a circuit that inputs an analog signal and outputs a digital signal or vice versa. This mode is not necessary for conventional digital macros.

A/D converter

The user logic circuit can be checked, by inputting a signal equivalent to the digital signal from the A/D converter, from an external circuit through the test circuit, to use this signal as the simulated output of the A/D converter.

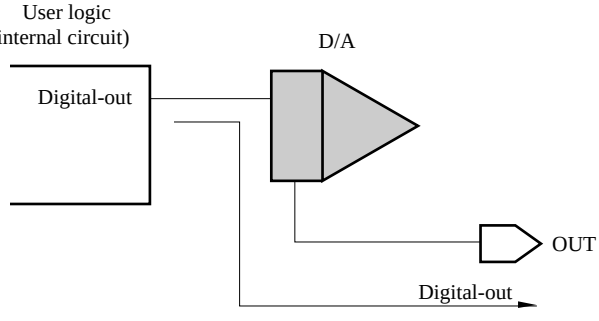
Fig. 4-8 A/D Converter



D/A converter

The user logic circuit can be checked, by extracting the digital signal from the user logic circuit before input to the D/A converter, to an external circuit through the test circuit.

Fig. 4-9 D/A Converter



A clocked macro such as the above A/D converter inputs a digital clock and outputs data in synchronization with the clock under actual operating conditions. In the user logic circuit test mode, however, the macro is not synchronized with the clock, but is configured so that data is directly input (for A/D converter) or output (for D/A converter).

4.3 Pins

An analog macro is provided with unique pins such as test pins necessary for realizing each simulation and mode.

4.3.1 Commonly Necessary Power Supply Pins

When integrating analog macros, the following additional power supply pins are necessary in addition to the standard power supply pins (V_{DD} and GND) specified for each package:

(1) DVDD

Applied to digital circuits in an analog macro (V_{DD}).
If two or more pins are necessary, they are named DVDD1, DVDD2, and so on.

(2) DGND

Applied to digital circuits in an analog macro.
If two or more pins are necessary, they are named DGND1, DGND2, and so on.

(3) AVDD

Applied to analog circuits in an analog macro (V_{DD}).
If two or more pins are necessary, they are named AVDD1, AVDD2, and so on.

(4) AGND

Applied to analog circuits in an analog macro.
If two or more pins are necessary, they are named AGND1, AGND2, and so on.

4.3.2 Test Pins

(1) TBO (n: 0), TBI (m: 0)

The test pins described below are used to simulate the test circuit.
The pins of an analog macro can be broadly classified into test pins and normal pins used to design an ordinary application circuit. The same signals as those from the normal pins with their input and output signals separated are output to the test pins. The number of test pins varies depending on the analog macro used.

(2) ATBO (n: 0), ATBI (m: 0)

The signals of these pins are peculiar to the analog macro, and are test data used in the total logic circuit test mode.

(3) BUNRI, TEST, MODE

These pins select the modes of the test pins and normal pins.

- BUNRI
  Selects the actual operating mode or the test mode (analog macro test and total logic circuit test).
- TEST
  Controls the test pins in combination with the BUNRI pin.
- MODE
  Selects the test mode, and serves as a test mode select pin only when the analog macro is used.
  If two or more pins are used, they are named MODE1, MODE2, and so on.

The analog macro operates as shown in the table in next page according to the combinations of these three inputs.

BUNRI	TEST	MODE	Mode	
0	×	0	Actual operating mode	
		1	Total logic circuit test mode	
1	1	×	Analog macro test mode	Test
	0			Standby

4.3.3 Setting of Pins in Each Mode

The following table shows the setting conditions of the pins to realize each mode, taking 8-bit A/D and D/A converters as examples.

Test mode		Macro name	Pins required for setting of each test mode				Test pins used and their conditions			
			BUNRI	TEST	MODE1	MODE2	TBI	TBO	ATBI	ATBO
Actual operating mode		A/D	0	× Note 1	0	–	Note 2 Invalid	Hi-Z	Invalid	–
		D/A	0	×	0	0		–	–	Hi-Z
Total logic circuit test mode		A/D	0	×	1	–	Invalid	Hi-Z	Valid	–
		D/A (3ch)-Rch	0	×	1	0		–	–	Valid
		D/A (3ch)-Gch	0	×	0	1				
		D/A (3ch)-Bch	0	×	1	1				
Analog macro test mode	Test	A/D	1	1	×	–	Valid	Valid	Invalid	–
		D/A	1	1	×	×		–	–	Hi-Z
	Stand-by	A/D	1	0	×	×	Invalid	Hi-Z	Invalid	–
		D/A						–	–	Hi-Z

Note 1. Input 0 to this pin when it is directly connected to an external pin as an input pin.

2. The input data is ignored.

4.4 Notes on Creating Test Circuits and Test Patterns

The following tables show the points to be noted when creating a test circuit and a test pattern in correspondence with each test mode.

Because the total logic circuit test mode is a mode to check the interface between the user logic and the analog macro, this mode can be omitted if your specifications do not call for checking the interface with the analog macro. This section describes points to be noted when this mode is used.

4.4.1 Notes on Creating Test Circuits

Mode name	Note
Analog macro test mode	Directly connect analog macro test pins TBI×× and TBO×× to interface blocks so that signals are not inverted or do not travel through a sequential circuit. In this case, the test bus can be shared with the test pins of other macros having equivalent functions.
Total logic circuit test mode	Like TBI×× and TBO××, directly connect total logic circuit test pins ATBI×× and ATBO×× to interface blocks so that signals are not inverted or do not travel through a sequential circuit. However, do not configure a data bus by combining these pins with TBI×× and TBO××.
Setting of BUNRI, TEST, and MODE	Set the BUNRI and TEST pins in the same manner as when normal megamacro is integrated. Directly connect the MODE pin to an input buffer. However, if the total logic circuit test mode is not used, fix the MODE pin to low level.

4.4.2 Notes on Creating Test Patterns

Mode name	Note
Actual operating mode	Make sure that logic other than analog macros can be mainly tested. Create a test pattern, because the input and output of analog data equivalent to the zero and full scale values of analog macro can be checked with a digital tester.
Analog macro test mode	Input/output data to/from the TBI××, TBO××, ATBI××, ATBO×× terminals by using a dedicated tester. Creating a test pattern for this purpose is not necessary.
Total logic circuit test mode	For an A/D converter, input the data assumed to be output from the A/D converter and to be input to the user logic circuit, from the ATBI×× pin. For a D/A converter, monitor the data input from the user logic circuit to the D/A converter by using the ATBO×× pin.
Setting of BUNRI, TEST, and MODE	Set the BUNRI and TEST pins in the same manner as when a normal megafunction is integrated. Set the MODE pin as shown in the table in **4.3.3 Setting of pins in each mode**.

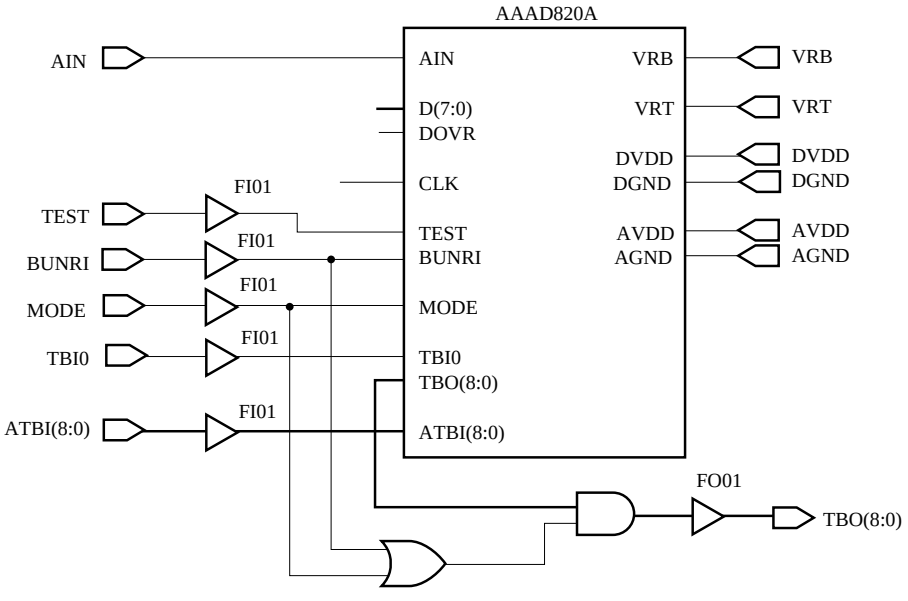
4.5 Example of Test Circuit Configuration with Analog Macro Integrated

This section shows configuration examples of test circuits when an 8-bit, 20 Msps A/D converter and D/A converter (3-ch) are integrated. In this section, description of interface blocks with test circuit necessary for configuring a test circuit is omitted for simplification.

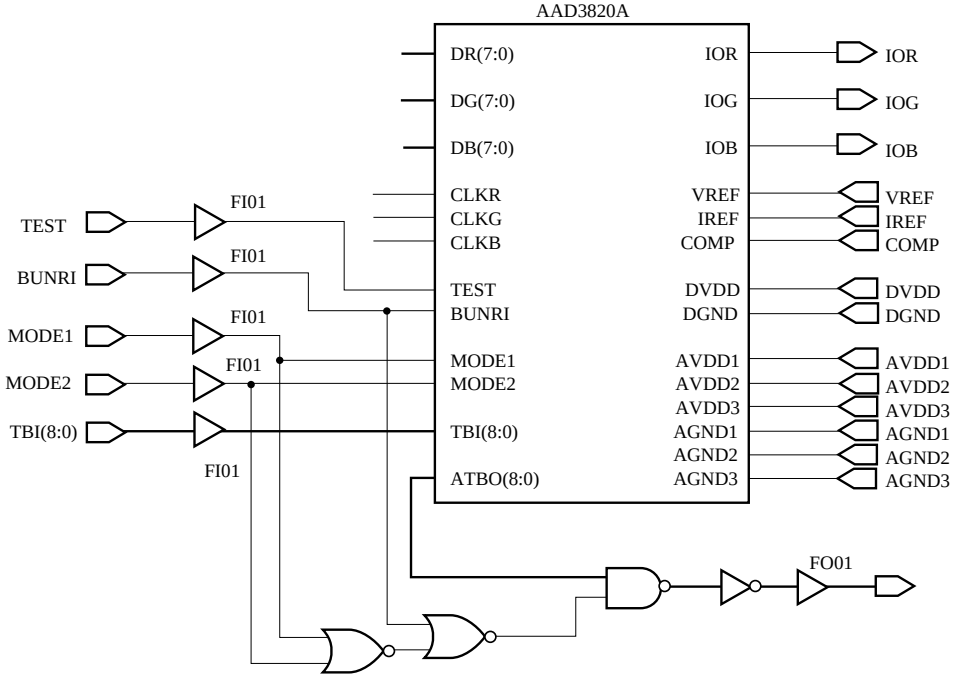
To configure the final test circuit, change the normal interface block to an interface block with test circuit.

4.5.1 When All Test Bus Pins are Dedicated to External Pins

A/D converter: When all TBI0, TBO0 to TBO8, and ATBI0 to ATBI8 are used as independent external pins

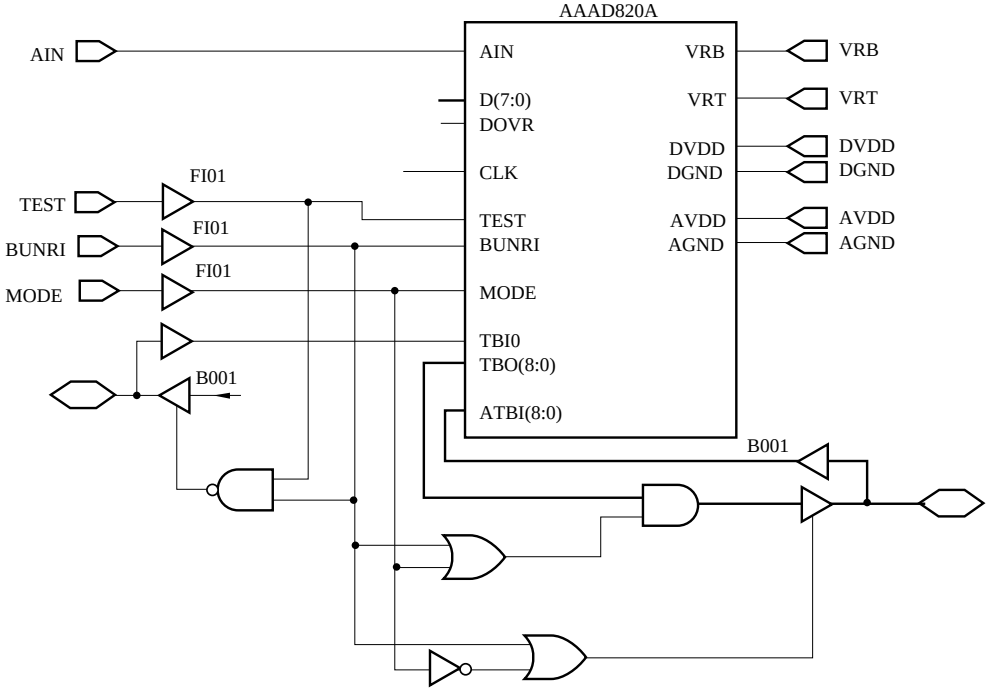


D/A converter: When all TBI0 and ATBO0 to ATBO8 are used as independent external pins

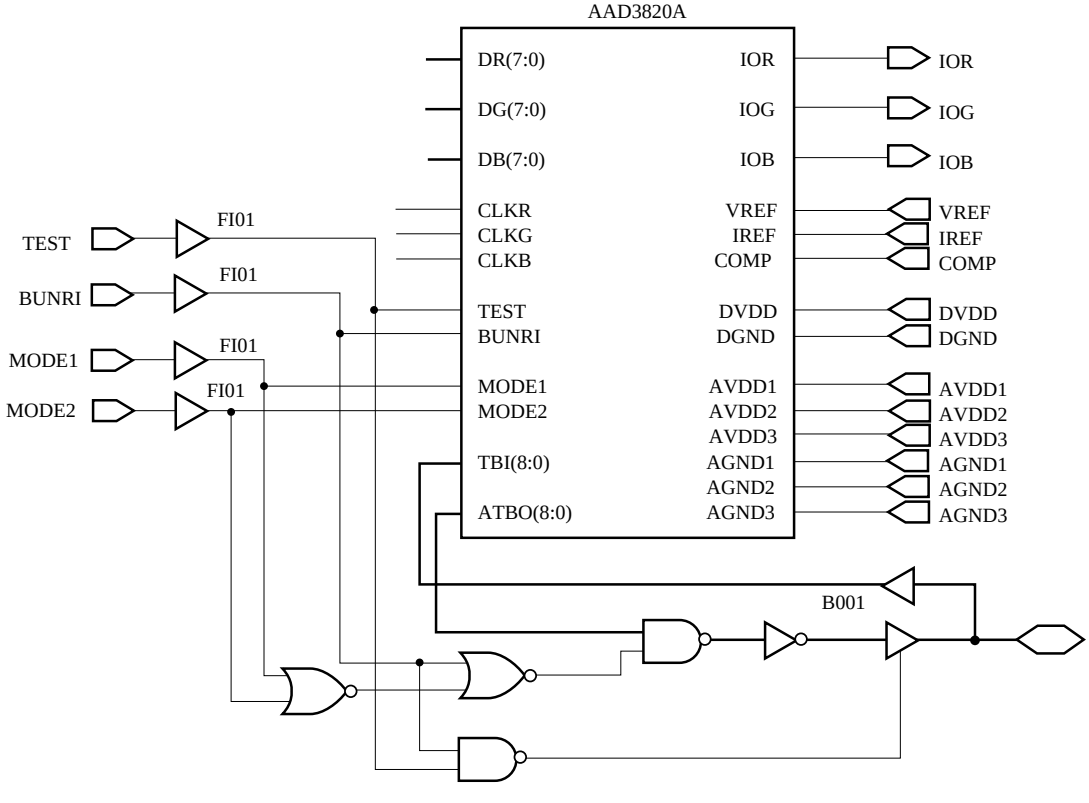


4.5.2 When Test Bus Pins are Shared with External Pins

A/D converter: When TBI0 is shared with an actually used pin and TBO0 to TBO8 are shared with ATBI0 to ATBI8

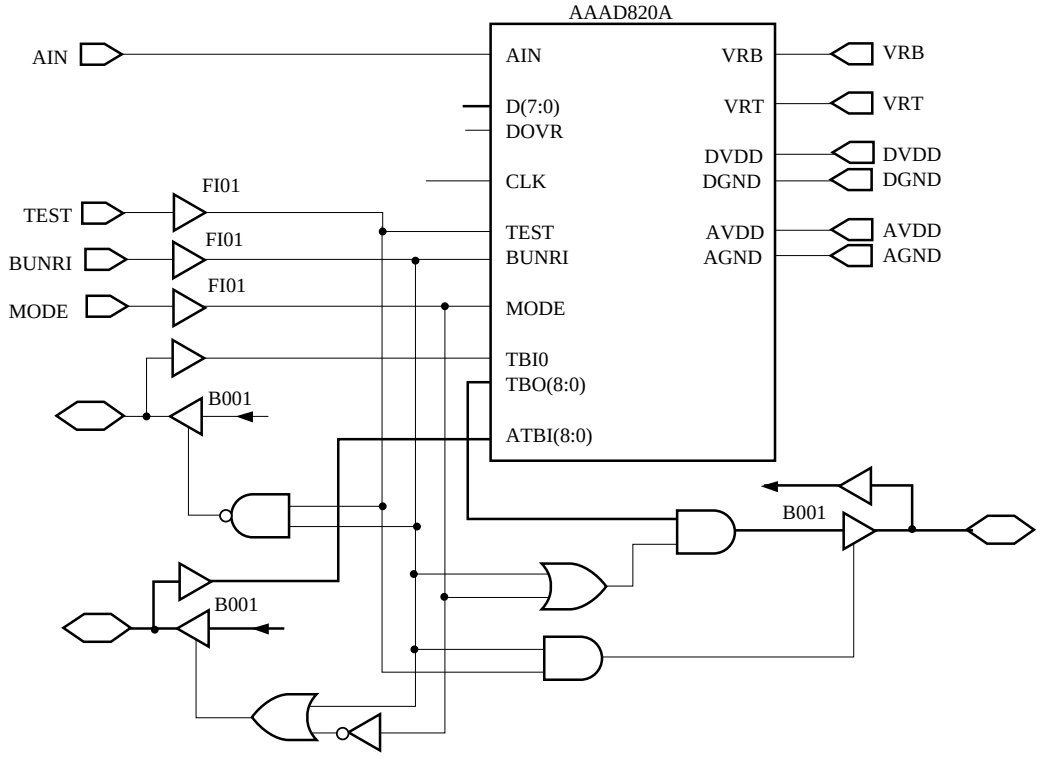


D/A converter: When TBI0 to TBI8 and ATBO0 to ATBO8 are shared

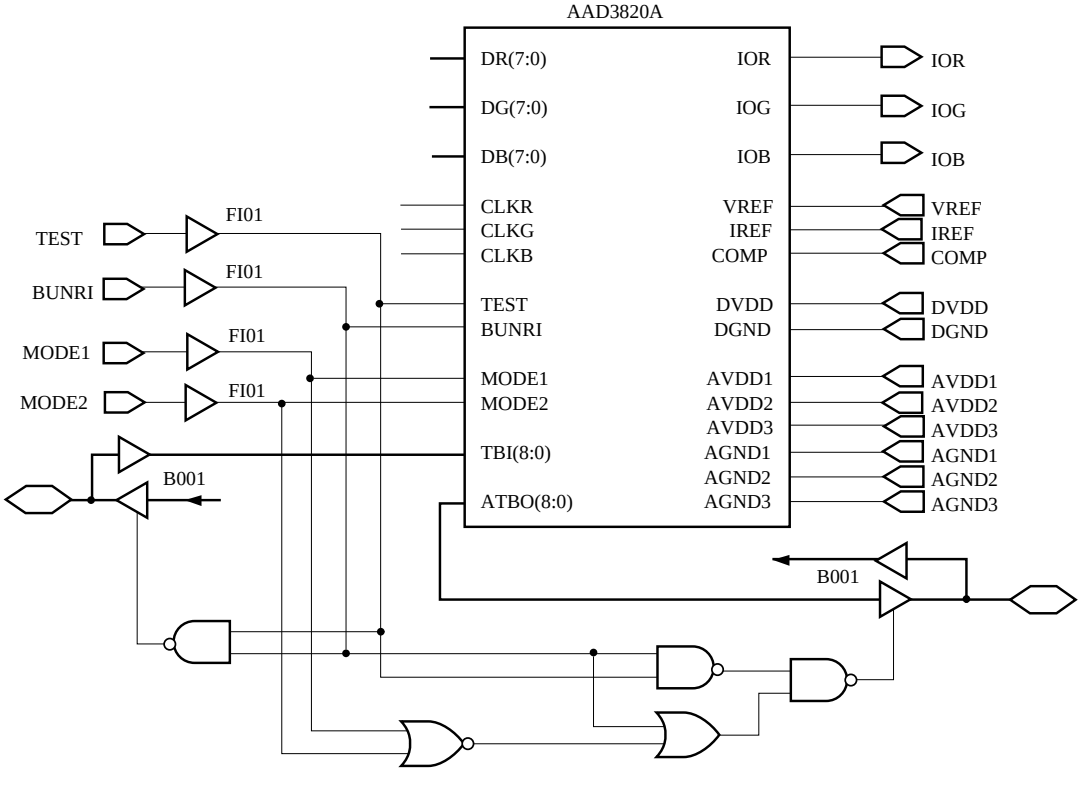


4.5.3 When Test Bus Pins are Shared with External Pins Connected with Normal Pins

A/D converter: When all TBI0, TBO0 to TBO8, and ATBI0 to ATBI8 are shared with actually used pins

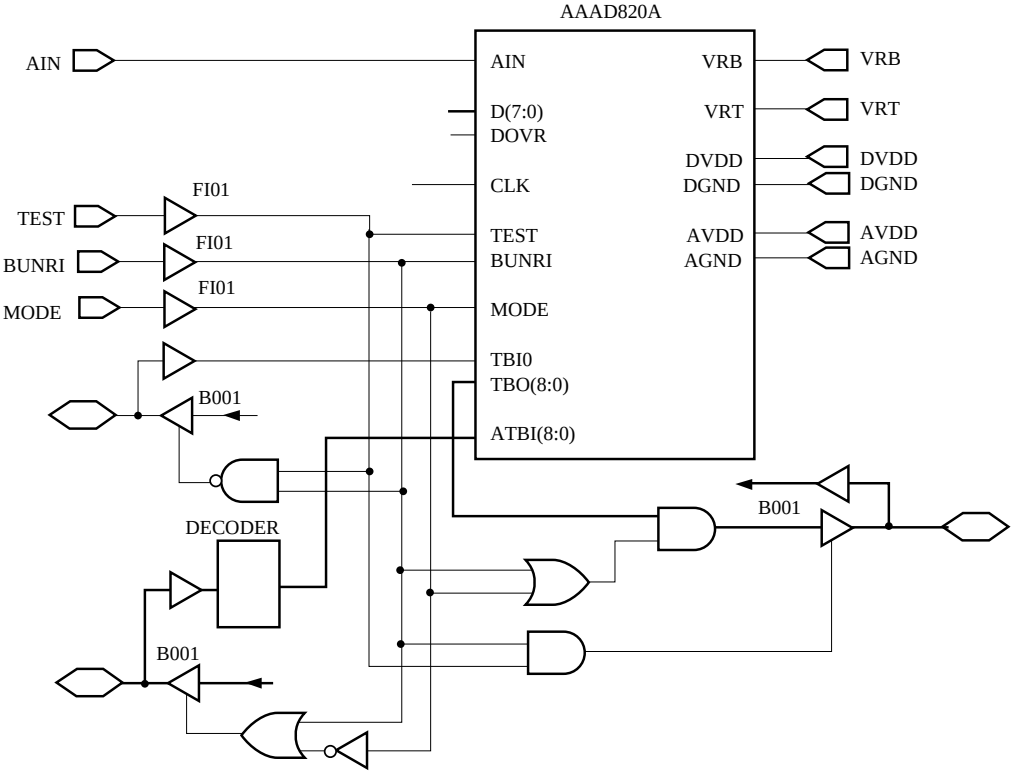


D/A converter: When TBI0 and ATBO0 to ATBO8 are shared with actually used pins

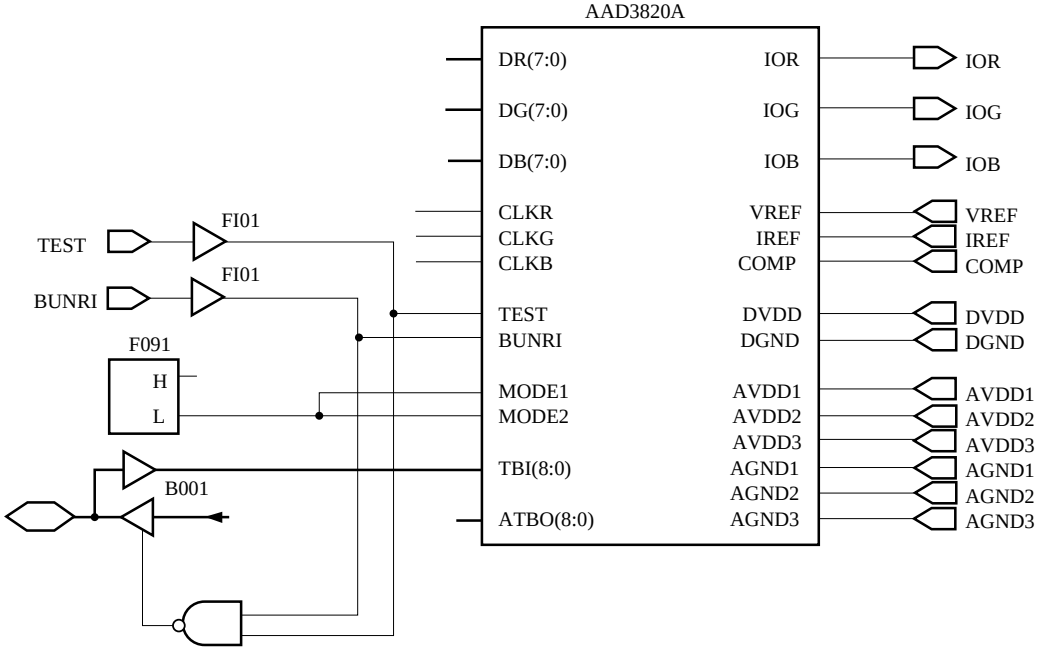


4.5.4 When Omitting Part of Test Bus Pins ATBI×× and ATBO××

A/D converter: When all the ATBI0 to ATBI8 pins are not directly input from external pins but connected to a decoder, connect the other test bus pins to external pins in the same manner as described in **4.5.1 When All Test Pins are Dedicated to External Pins**.

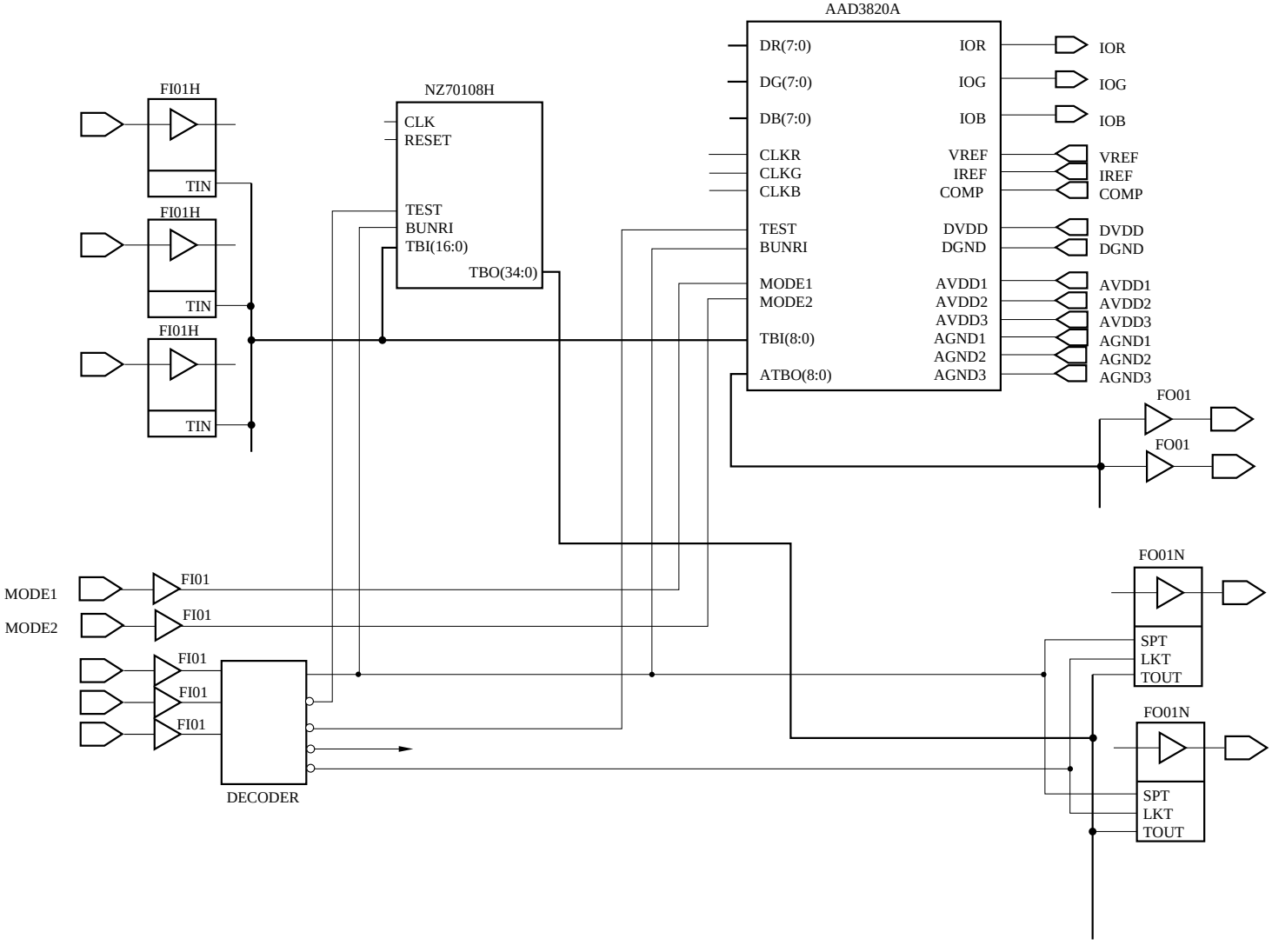


D/A converter: When the ATBO to ATBO8 pins are omitted, share the other test bus pins with external pins as described in **4.5.2 When Test Bus Pins are Shared with External Pins**.



4.5.5 When Both D/A Converter and Other Megafunctions Exist

A configuration example of a test circuit is shown below where a D/A converter is integrated together with other megafunctions. In this figure, the interface block with test circuit necessary for configuring a test bus is also drawn.



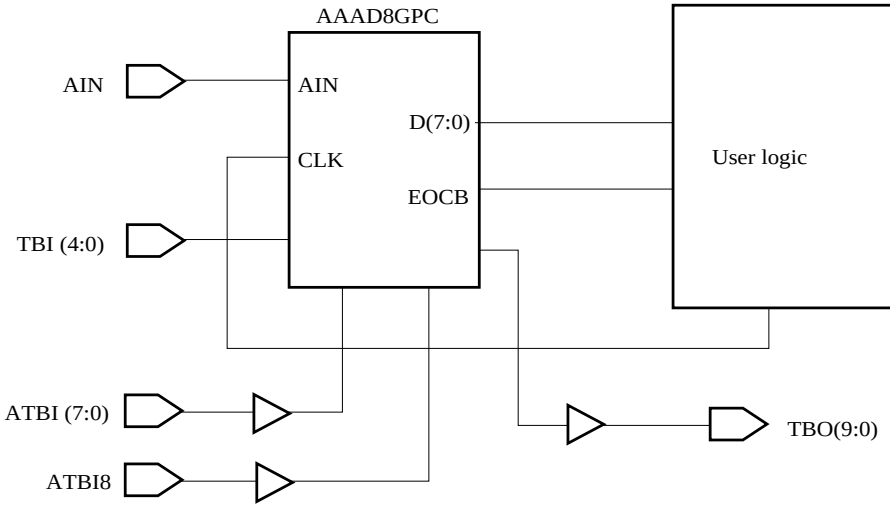
CHAPTER 5 SIMULATION

At present, a digital simulator is used to simulate a circuit that includes analog macros. Consequently, the interface block of the analog macro is simulated with digital signals.

Only limited checks can be carried out during simulation in the actual operating mode.

This chapter describes simulation techniques when an 8-bit general purpose A/D converter AAAD8GPC is used. For details, refer to the user's manual-individual part by macro.

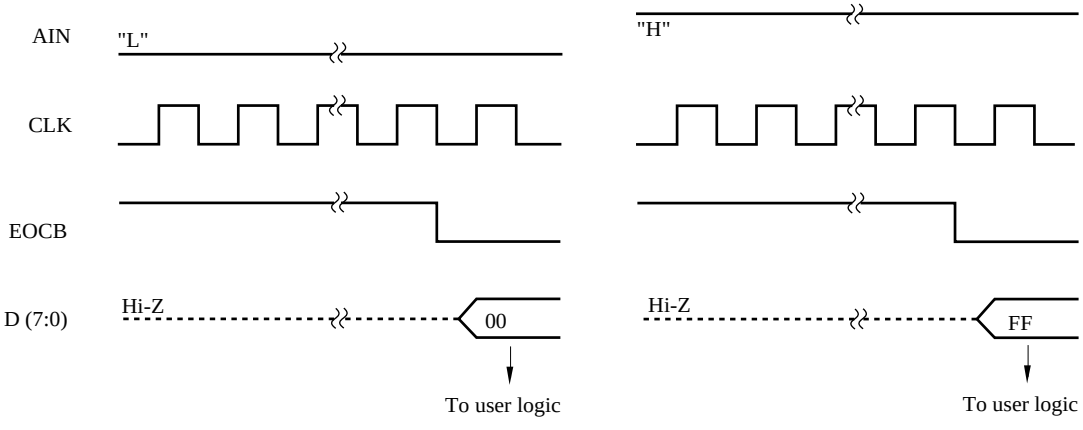
Fig. 5-1 Circuit Diagram for Explanation of Analog Macro Test



Remark This diagram is excerpted from a part of a circuit.

5.1 Actual Operating Mode

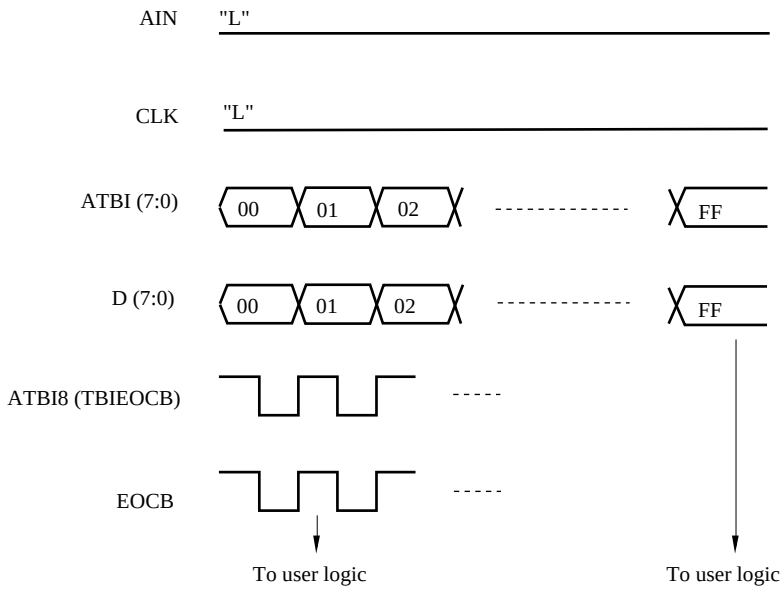
The operation of the analog macro is checked in this mode.



When 0 is input to AIN, 00 is output from D(7:0); when 1 is input to AIN, FF is output from D(7:0). Using these two codes, confirm through the user logic.

5.2 Total Logic Circuit Test Mode

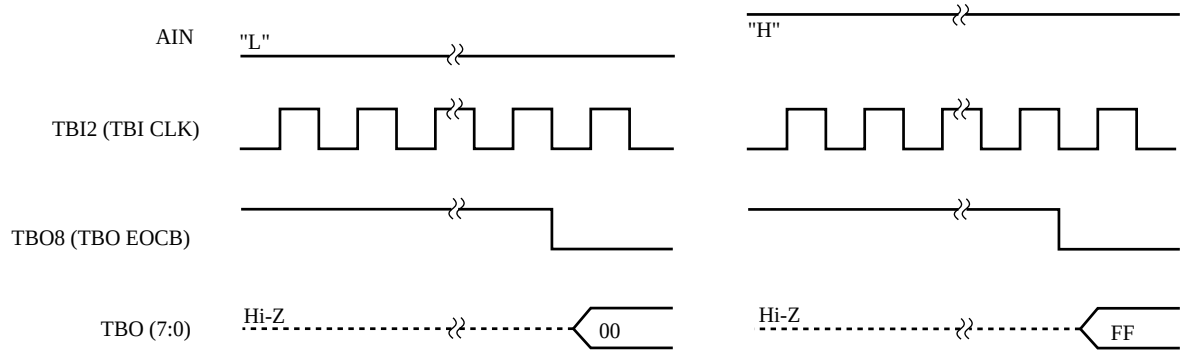
Connection between analog macro and user logic is checked in this mode (operation of the analog macro cannot be checked).



Data input to ATBI(7:0) are output to D(7:0) as is. Confirm through user logic.

5.3 Analog Macro Test Mode

Whether the test circuit of the analog macro is a test circuit that can use the test pattern available from NEC is checked in this mode.



When 0 is input to AIN, 00 is output to TBO(7:0).
When 1 is input to AIN, FF is output to TBO(7:0).
Confirm that these two codes are output to TBO(7:0) by using the output pins.

The items that can be checked in the actual operating mode are limited. Therefore, create a test pattern that can test all items in the actual operating mode, the total logic circuit test mode, or the analog macro test mode.

However, to use the total logic circuit test mode, some pins not usually used are necessary. Adequately consider the necessity of the mode in advance.

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CHAPTER 6 POWER CONSUMPTION ESTIMATION

The power consumed by the analog macro for the CB-C7 family is the sum of the powers consumed by each macro integrated.

Unlike the normal digital circuit, an analog circuit consists of a portion through which a constant current flows independently of the operating frequency, and a portion whose current value changes with the operating frequency.

As for the power consumption, the following equation is used,

$$\mathbf{Pt = (Ps + Pd) \times n}$$

Pt : power consumption of a certain macro
Ps : power consumption of constant-current portion
Pd : power consumption of portion dependent on the operating frequency
n : the number of macros used

For details, refer to the user's manual-individual part by macro.

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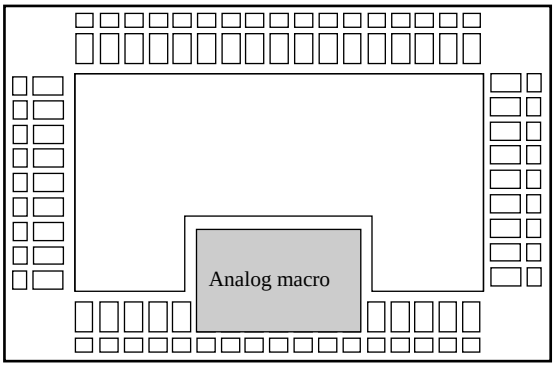
CHAPTER 7 LAYOUT

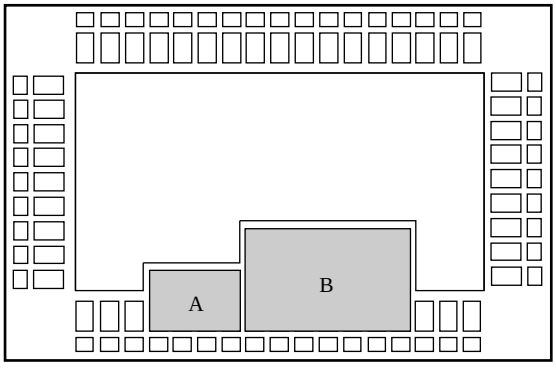
7.1 Note

(1) An analog macro is to be located in the interface block area of a chip, and its size is determined in advance. Therefore, the size of the chip and available package type are limited. In addition, the location of analog pins is also regulated. For details, refer to the user's manual-individual part by macro.



For example, an analog macro cannot be integrated in a PGA because mutual interference between pins is high due to the very complicated connection between bonding wires and package pins.
Packages in which the analog macros can be integrated are listed in **7.2 Package Availability for Analog Macros**. Note, however, that these data are subject to change without notice. For the latest data and details, consult NEC.

(2) The combination of available chip size and package is limited more strictly than the above (1) if two or more types of analog macros are placed. For details, consult NEC.



(3) The digital power supply pin and the GND pin (DVDD and DGND), and the analog power supply pin and the GND pin (AVDD and AGND) are separated inside the macro to improve noise immunity. These pins are also separated from the standard power supply pins used in the package for the CB-C7 family.

(4) To prevent the adverse effect of noise generated when the interface block operates, do not locate an output buffer at a position where the analog macro is to be placed. However, locating an output buffer there that is only used in the test mode does not pose a problem.

7.2 Package Availability for Analog Macro

Package type		Function						
		8-bit general purpose A/D converter	8-bit general purpose D/A converter	8-bit 20 Msps A/D converter	8-bit 20 Msps D/A converter	Analog switch	Comparator	Operational amplifier
S-DIP	64-pin (750mil)	N/A	N/A	N/A	N/A	U/S	N/A	N/A
QFP	44-pin	N/A	N/A	N/A	N/A	A	N/A	N/A
	52-pin	N/A	N/A	N/A	N/A	A	N/A	N/A
	64-pin	A	A	A	A	A	A	A
	80-pin	A	A	A	A	A	A	A
	100-pin	A	A	A	A	A	A	A
	120-pin	A	A	A	A	A	A	A
	136-pin	U/S	U/S	U/S	U/S	A	U/S	U/S
	160-pin	A	A	A	A	A	A	A
	184-pin	U/S	U/S	U/S	U/S	U/S	U/S	U/S
	208-pin	A	A	A	A	A	A	A
QFP (HS)	160-pin	A	A	A	A	A	A	A
TQFP	80-pin	N/A	N/A	N/A	N/A	A	N/A	N/A
QFP (FP)	100-pin	A	A	A	A	A	A	A
	120-pin	U/S	U/S	U/S	U/S	A	U/S	U/S
	144-pin	U/S	U/S	U/S	U/S	A	U/S	U/S
	160-pin	U/S	U/S	U/S	U/S	A	U/S	U/S
	176-pin	U/S	U/S	U/S	U/S	U/S	U/S	U/S
	208-pin	A	A	A	A	A	A	A
	304-pin	U/S	U/S	U/S	U/S	U/S	U/S	U/S
PLCC	68-pin	U/S	U/S	U/S	U/S	A	U/S	U/S
	84-pin	U/S	U/S	U/S	U/S	A	U/S	U/S
PGA	72-pin	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	132-pin	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	176-pin	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	208-pin	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	280-pin	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	364-pin	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Remark Legends in the table above:

A: Available
N/A: Not available
U/S: Under study on availability
(HS): With heat spreader
(FP): Fine pitch type