Design Guide

PCB Design Guidelines for High Speed Signal Interfaces and Others

RZ/G3E FCBGA 15.0/21.0sq

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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

Introduction

This document describes a PCB design guideline for designing a board with the RZ/G3E.

The interfaces which are described in this document are listed below.

- LVDS
- MIPI CSI-2
- MIPI DSI
- USB 2.0
- USB 3.2 Gen2
- PCI Express 3.0
- 12-bit A/D converter (ADC)
- PLL
- OSC

1. LVDS

In this chapter, the design guideline about LVDS is described.

1.1 Signal Trace

Topologies of transmitter and receiver are illustrated in **Figure 1.1**.

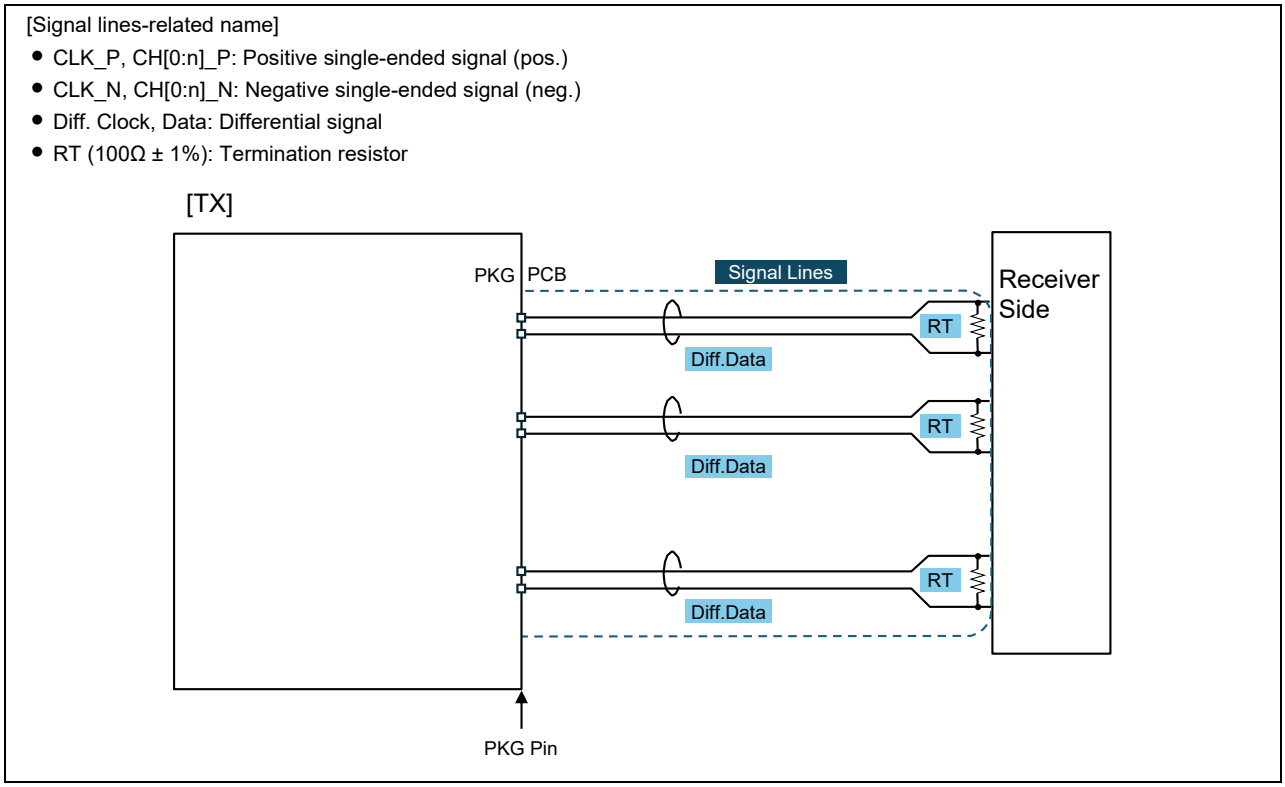

Figure 1.1 Signal Trace Topology

1.1.1 General Guidelines

Give design priority to the high priority items marked with a check mark.

Table 1.1 Guidelines for PCB Signal Lines of LVDS

Items		Guidelines	Fig.	Notes
Line impedance		✓: Differential 100Ω ± 20%	—	1
Line length difference	Between Diff. Clock and Diff. Data	✓: As the same length as possible ✓: Line length is as short as possible	—	2
	Between each pos. and neg.		—	
Line bending		Recommended: External angle 45° (Prohibition: > 45°)	—	3
Line layer Numbers of via	Between Diff. Clock and Diff. Data	Same layer Note: Recommended: Top layer without any vias	—	4
	Between each pos. and neg.	Same via number (number is as few as possible)	—	
Line spacing	Between each pos. and neg.	S (min. of PCB design criterion)	(1) in **Figure 1.2**	5
	Between Diff. and next Diff.	≥ 3S Note: When there is no GND shield	(6) in **Figure 1.3**	
	Between Diff. and GND shields	≥ S Note: Place GND shields on both sides of Diff.	(2) in **Figure 1.2**	
	Between Diff. and other high speed / low speed signal	≥ 3S Note: It is unnecessary when there are GND shields	—	
	Between Diff. and Continuous Ground Plane	≥ S	(3) in **Figure 1.2**	
Line width		≥ S	(4) in **Figure 1.2**	
Return path		✓: Place Continuous Ground Plane under Diff.	(5) in **Figure 1.2**	6
		Place GND through-hole next to signal through-hole Place GND vias symmetrically next to Diff.	—	

Note 1. TDR measurement condition: TRF = 0.5 ns@350 mV

Note 2. This is a guideline to reduce the line skew.

Note 3. Do not bend at an acute angle. Bend as arc.

Note 4. Do not use through hole-via in changing signal line layer (to prevent reflection associated with stub).

Note 5. These sizes are for reference only, and can be changed to the designer-side actual value.

Note 6. Ensure a sufficient Ground Plane width for signal lines width.

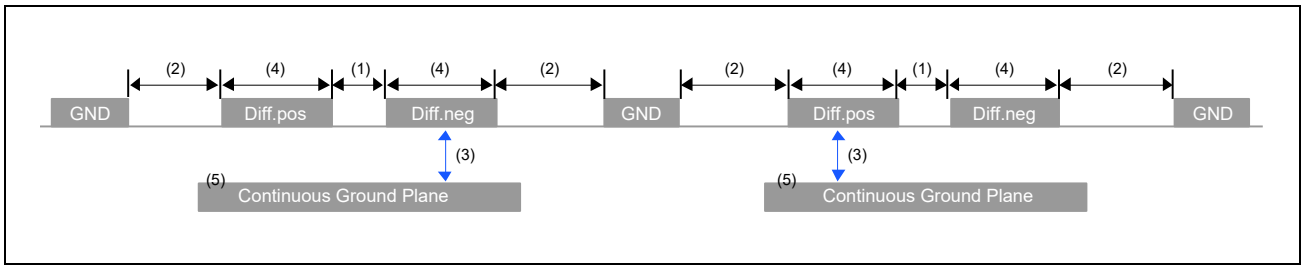

Figure 1.2 Signal Trace Example 1

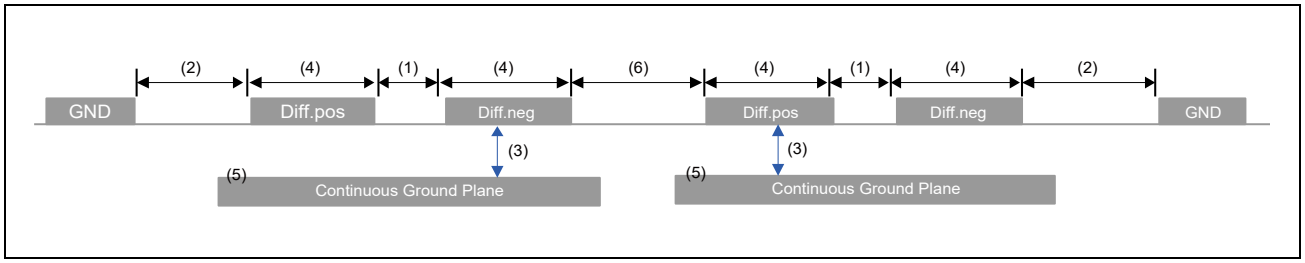

Figure 1.3 Signal Trace Example 2

1.2 Power Supply

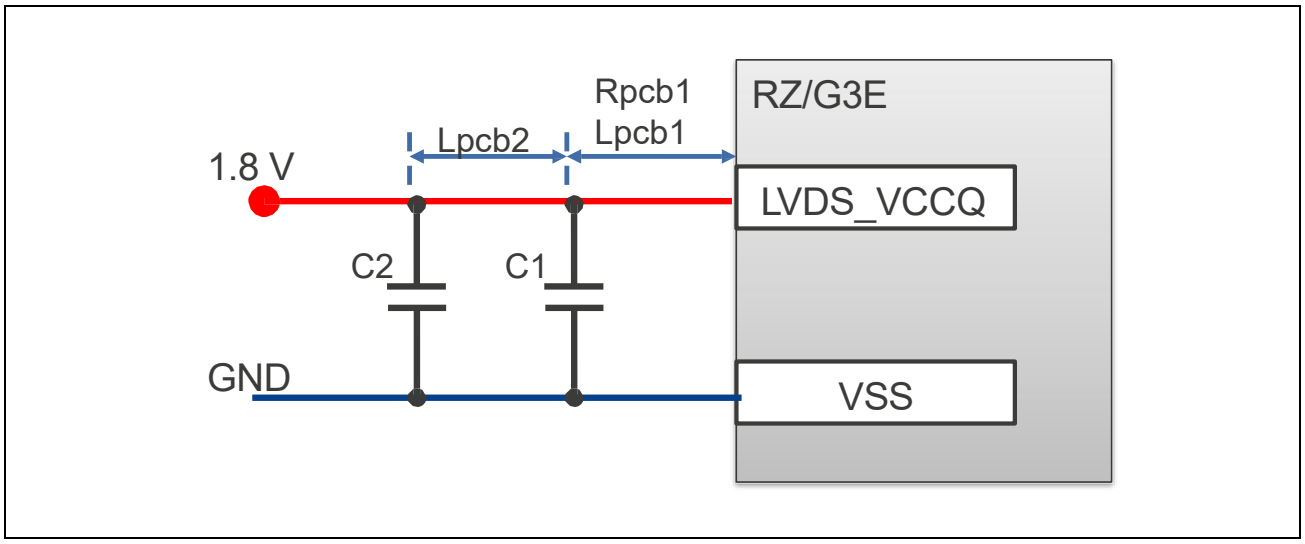

Figure 1.4 External Capacitors for LVDS

Table 1.2 Guidelines for PCB Power Lines of LVDS

Items	TX	Notes
Rpcb1	≤ 30mΩ	—
Lpcb1	≤ 2.8 nH	1
Lpcb2	≤ 3.0 nH	
C1 (nearest the chip)	0.1 µF	2
C2	47 µF	3

Note 1. The power line inductance from the PKG pins to C1 should be as small as possible. Refer to **Appendix A, Concept of Loop Inductance**.

Note 2. Place C1 nearer the PKG pins to prevent the ripple noise by the transient current. Place a bypass capacitor between the respective power supply planes and solder balls.

Note 3. C2 has the effect of preventing noise from the common power plane to IP (If there is no such noise, C2 is unnecessary). Cut-off frequency is about a few kHz. The cut-off frequency should be low enough to prevent noise in the operating frequency/data rate range of this.

2. MIPI CSI-2 and MIPI DSI

In this chapter, design guidelines about MIPI CSI-2 and MIPI DSI are described.

Applicable Standard

For general information on electric and transfer path characteristics, as well as on connector specifications required in designing a PCB, refer to the specification issued by the standards certification bodies listed in **Table 2.1** and **Table 2.2**.

Table 2.1 Standard Applicable to MIPI CSI-2

Standard Certification Body	Title of Specification
MIPI Alliance	MIPI Alliance Specification for D-PHY Version 1.2

Table 2.2 Standard Applicable to MIPI DSI

Standard Certification Body	Title of Specification
MIPI Alliance	MIPI Alliance Specification for D-PHY Version 1.2
	MIPI Alliance Specification for Display Serial Interface Version 1.3.1

2.1 Signal Trace

Topologies of transmitter and receiver are illustrated in **Figure 2.1**.

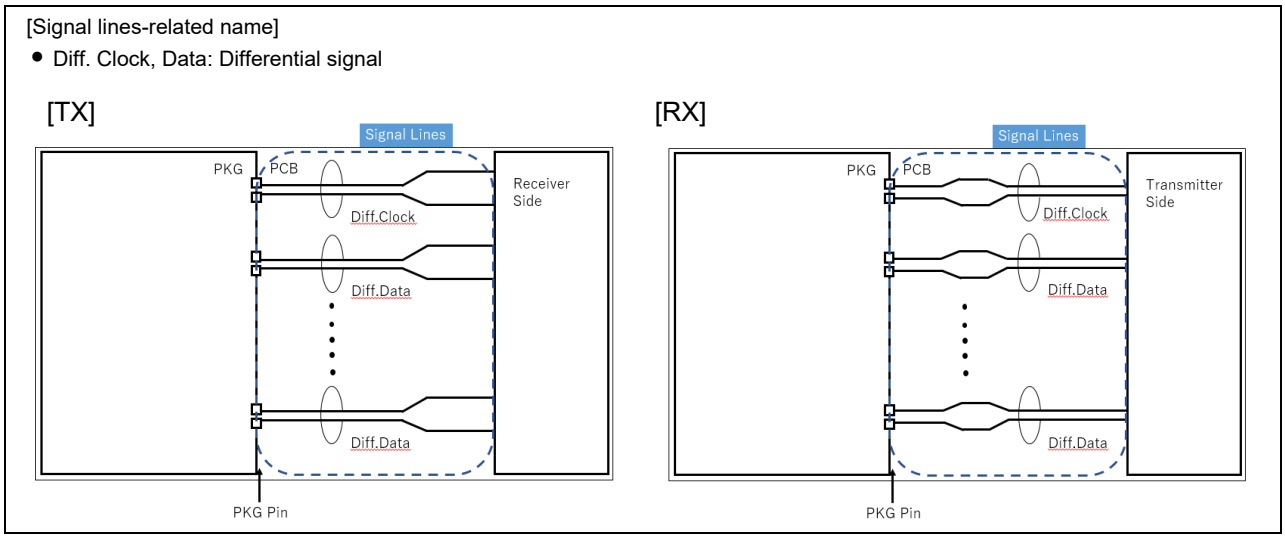

Figure 2.1 Signal Trace Topology

2.1.1 General Guidelines

Give design priority to the high priority items marked with a check mark.

Table 2.3 Guidelines for PCB Signal Lines of MIPI CSI-2 and MIPI DSI

Items		Guidelines	Fig.	Notes
Line impedance		✓: Differential 100Ω ± 5% Single-end 50Ω ± 5% With GND shields: ✓: Differential 90Ω ± 5% Single-end 45Ω ± 5%	—	1
Line length difference	Between Diff. Clock and Diff. Data	✓: As the same length as possible ✓: Line length is as short as possible	—	2, 3
	Between each pos. and neg.		—	
Line bending		Recommended: External angle 45° (Prohibition: > 45°)	—	—
Line layer Numbers of via	Between Diff. Clock and Diff. Data	Same layer Note: Recommended: Top layer without any vias	—	—
	Between each pos. and neg.	Same via number (number is as few as possible)	—	—
Line spacing	Between Diff. and next Diff.	≥ 4S Note: When there is no GND shield	(6) in **Figure 1.3**	2
	Between Diff. and GND shields	≥ 2S Note: Place GND shields on both sides of Diff.	(2) in **Figure 1.2**	
Line width		≥ S	(4) in **Figure 1.2**	
Return path		Place Continuous Ground Plane under Diff.	(5) in **Figure 1.2**	—
		Place GND through-hole next to signal through-hole Place GND vias symmetrically next to Diff.	—	—

Note 1. Priority should be given to differential impedance for characteristics.

Note 2. Target value of wire length difference: within a maximum of 500 µm.

Note 3. The maximum trace length should be less than or equal to 100 mm.

2.1.2 Differential Signals

- DP/DN wiring should be of equal length, parallel, and equal width in the same layer.
- The trace length difference between two differential pair signals should be less than or equal to 2 mm at 1 Gbps, 1.33 mm at 1.5 Gbps, and 1 mm at 2 Gbps.
- Do not allow DP/DN wiring to cross power supply splits or plane voids.
- DP/DN wiring should not be intersected with other signals. When intersecting, sandwich the digital power plane or the GND plane.
- For DP/DN wiring, the number of bends should be kept as low as possible. Also, if you want to bend it, do not bend it at a right angle, but bend it twice to 45 degrees.
- To prevent noise contamination, the DP/DN wiring should be bent and sullen to a minimum, and the layer under the DP/DN wiring should be a GND plane.
- Keep the DP/DN wiring away from other signal wiring. Pay particular attention to rapidly changing signals such as clocks and data buses.
- Place the GND return via adjacent to the DP/DN via. The return path must be continuous at GND.

2.2 Power Supply

2.2.1 MIPI CSI-2

- Place 0.1 µF and 1 µF ceramic capacitors as close to the MPU as possible. At that time, place the small capacity on the MPU side and the large capacity on the regulator side.
- Since the CSI0_MSVDD18 and CSI0_MSVDD0P8 power supplies are IP-only power supplies, consider using ferrite beads when sharing them with other power supplies. When using ferrite beads, do not use the power supply after passing the ferrite beads for anything other than MIPI CSI-2. Also, when using ferrite beads, place them as close to the MPU as possible.
- The inductance of the PCB should be as small as possible.
- The CSI*_MSVDD0P8 requires power to be supplied to all four power terminals, regardless of the number of lanes used, but the CSI*_MSVDD18 requires power supply only to the power supply terminals corresponding to the lane number to be used.

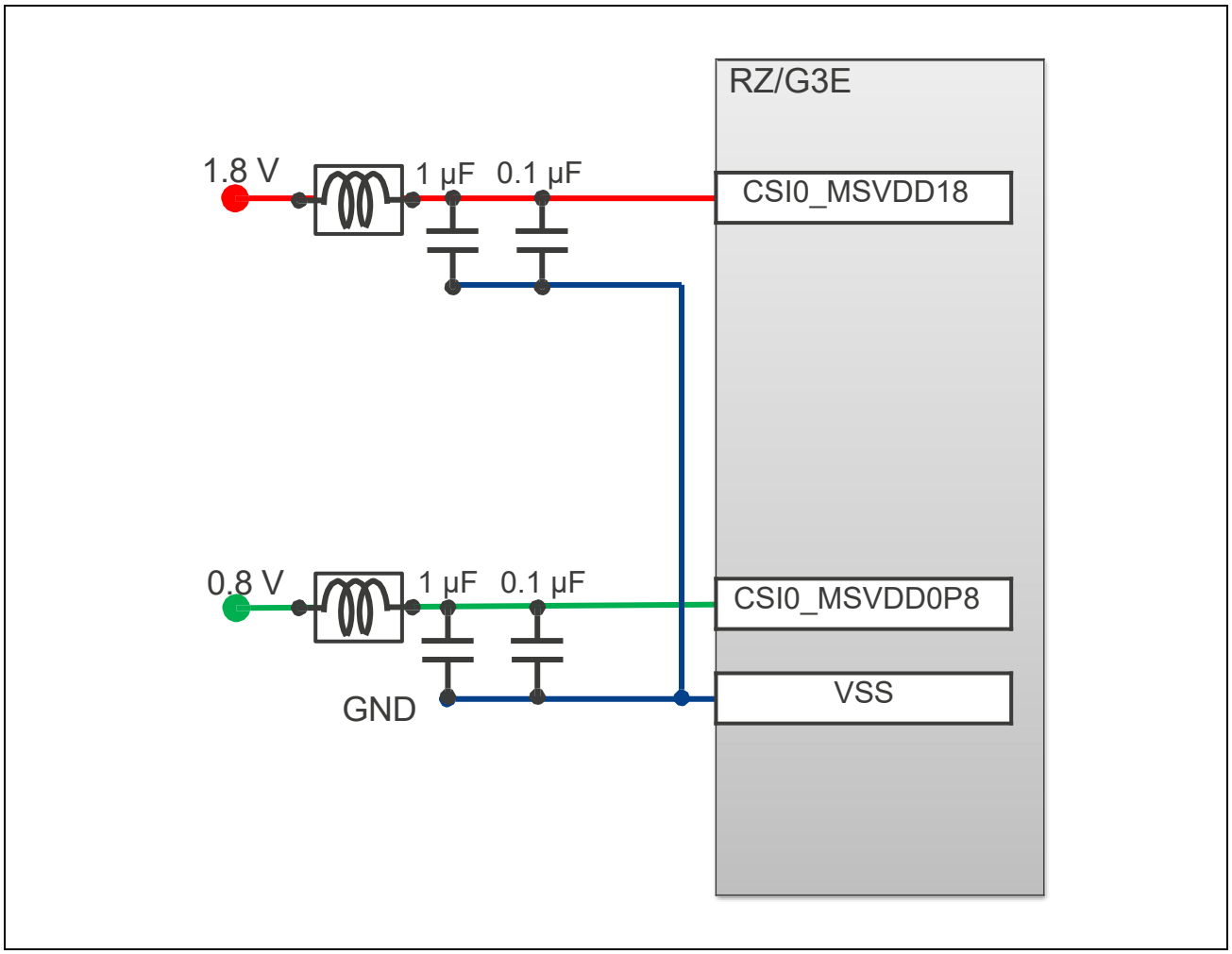

Figure 2.2 External Capacitors for MIPI CSI-2

2.2.2 MIPI DSI

- Place 0.1 µF and 1 µF ceramic capacitors as close to the MPU as possible. At that time, place the small capacity on the MPU side and the large capacity on the regulator side.
- Since each power supply DSI_VDD18, DSI_VDD12, and DSI_VDD0P8 are IP-only power supplies, consider using ferrite beads when sharing them with other power supplies. When using ferrite beads, do not use power through ferrite beads for anything other than MIPI DSI. Also, place the ferrite beads as close to the MPU as possible.
- Place a 2.2 nF capacitor between the DSI_VREG0P4V and VSS near the MPU. Keep the DSI_VREG0P4V away from noisy signal wiring.
- The inductance of the PCB should be as small as possible.

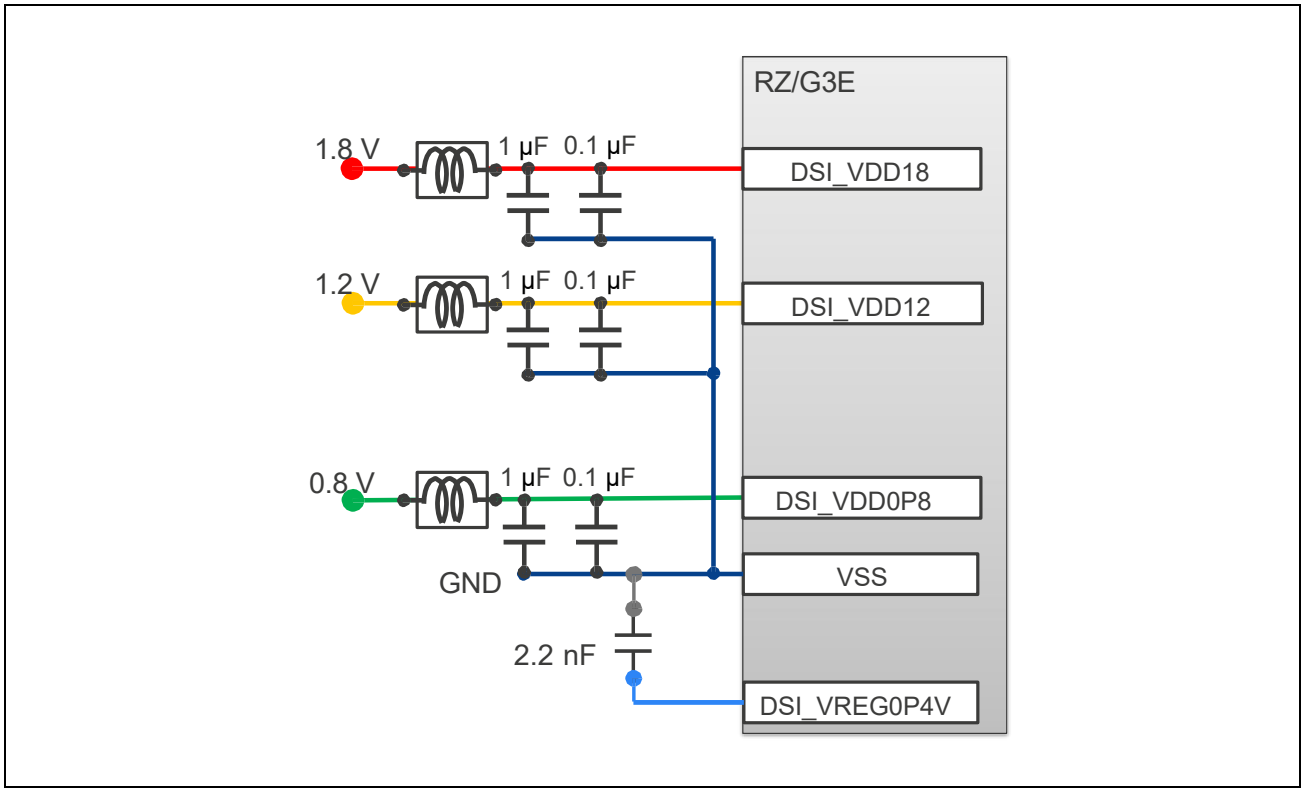

Figure 2.3 External Capacitors for MIPI DSI

3. USB 2.0

In this chapter, the design guideline about USB2.0 is described.

3.1 Signal Trace

3.1.1 General Guidelines

Give design priority to the high priority items marked with a check mark.

Table 3.1 Guidelines for PCB Signal Lines of USB 2.0

Items		Guidelines	Fig.	Notes
Line impedance		✓: Differential 90Ω ± 10% Single-end 45Ω ± 10%	—	1
Line length difference	Between each pos. and neg.	✓: As the same length as possible ✓: Line length is as short as possible	—	2
Line bending		Recommended: External angle 45° (Prohibition: > 45°)	—	—
Line layer Numbers of via	Between each pos. and neg.	Same layer *Note*: Recommended: Top layer without any vias Same via number (number is as few as possible)	—	—
Line spacing	Between each pos, and neg.	At least 0.20 mm	(1) in **Figure 1.2**	—
	Between Diff. and next Diff.	At least 0.51 mm	(6) in **Figure 1.3**	—
	Between Diff. and other high speed clock and periodic signal	At least 1.27 mm *Note:* It is unnecessary when there are GND shields	—	—
	Between Diff. and other low speed / non-periodic signal	At least 0.51 mm *Note:* It is unnecessary when there are GND shields	—	—
Line width	Between each pos. and neg.	✓: As the same width as possible	—	—
Return path		Place Continuous Ground Plane under Diff.	(5) in **Figure 1.2**	—
		Place GND through-hole next to signal through-hole Place GND vias symmetrically next to Diff.	—	—

Note 1. Priority should be given to differential impedance for characteristics.

Note 2. Target value of difference in wiring length: within a maximum of 1 mm.

3.1.2 Differential Signals

- Shorten the DP/DM wiring between the MPU and the connector. According to the USB Specification, the maximum latency from the downstream facing transceiver of the host or hub controller to the external downstream facing connector is 3 ns, and the maximum delay from the upstream facing connector to the upstream facing transceiver is 1 ns. Note that the delay value per length varies depending on the substrate material.
- DP/DM wiring should be of equal length, parallel, and equal width in the same layer.
- Make sure that the DP/DM wiring does not cross the power supply split or plane void. Also, do not intersect DP/DM wiring with other signals. When intersecting, sandwich the digital power plane or the GND plane.
- The number of bends in the DP/DM wiring should be kept as low as possible. When bending, do not bend at a right angle, but bend twice at 45 degrees.
- To prevent noise contamination, the DP/DM wiring should be bent and sullen to a minimum, and the DP/DM wiring should be in the GND plane.
- Shield both sides of the DP/DM wiring. Also, place the GND return via adjacent to the DP/DM via. The return path must be continuous at GND.
- The total value of the L/C/R of the USB20_DP/DM, including the MPU package, board wiring, and USB connector, should be 4 nH or less with an inductance of 4 nH or less, a capacitance of 5 pF or less, and a resistance of 1Ω or less.

3.1.3 Other Signals

The total value of the L/C/R of the USB20_OTG_ID, including the MPU package, board wiring, and USB connector, should be 4 nH or less with an inductance of 4 nH or less, a capacitance of 5 pF or less, and a resistance of 1Ω or less.

3.2 Power Supply

- Separate the digital power plane from the analog power plane.
- A large number of decoupling capacitors are strongly recommended for all power supplies.
- A ceramic capacitor with a low ESR of about 100 nF is recommended.
- The total value of the inductance and resistance values of the power supply wiring (USB2_USVDD33, USB20/21_USVDD18, and USB2_USDVDD), including the MPU package, board writing, and USB connector, should be 4 nH or less and 1Ω or less of resistance.
- Wiring to the DVDD power supply should be as short as possible, and as many vias and contacts should be used.
- In order to minimize the impedance of each power supply wiring, use as wide and short a wiring as possible.
- Place the capacitors in ascending order of capacitance from the MPU to the regulator side. The recommended arrangement of capacitors for the USB2_USVDD33 and USB20_USVDD18 power supplies is 0.1 µF, 2.2 µF, 10 µF, and 47 µF. The recommended arrangement of capacitors for the USB2_USDVDD power supply is 0.01 µF, 0.1 µF, 2.2 µF, 10 µF, and 47 µF.
- The 0.01-µF, 0.1-µF, 2.2-µF, and 10-µF capacitors should be placed as close to the MPU as possible. The 47-µF capacitor can be further away.
- Consider using ferrite beads when supplying from one power supply to each power supply (USB2_USVDD33, USB20/21_USVDD18, and USB2_USDVDD). When using ferrite beads, do not use the power supply through the ferrite beads for anything other than USB 2.0. Also, connect the ferrite beads so that they are as close to the MPU as possible.

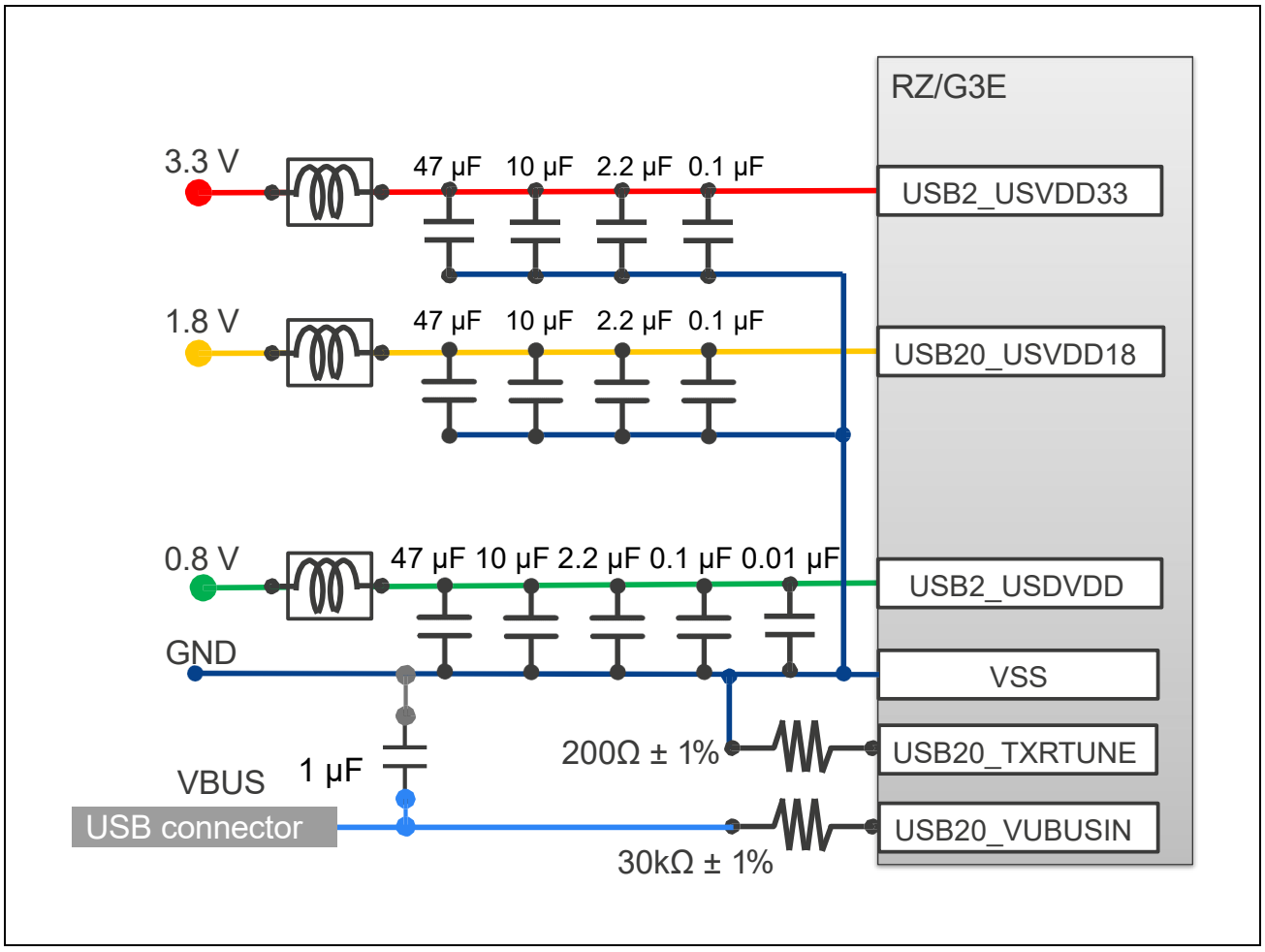

Figure 3.1 External Capacitors for USB 2.0

Note about Reverse Current through USB 2.0 Power Supplies

The reverse current can flow in the following two cases: when the VBUS is powered while the MPU is powered off, and when the USB is in suspend mode. Please take care of them according to your case with the following examples.

A load switch or similar component should be placed between the VBUS and the USB20_VUBUSIN so that 5 V is supplied from the VBUS to the USB20_VUBUSIN after the USB power supplies such as the USB2_USVDD33 and the USB20_USVDD18 are turned on. This prevents the reverse current via the USB20_VUBUSIN from flowing from the power supply terminal of the MPU to the power supply IC during the USB2_USVDD33 and the USB20_USVDD18 are turned off. (**Figure 3.2**)

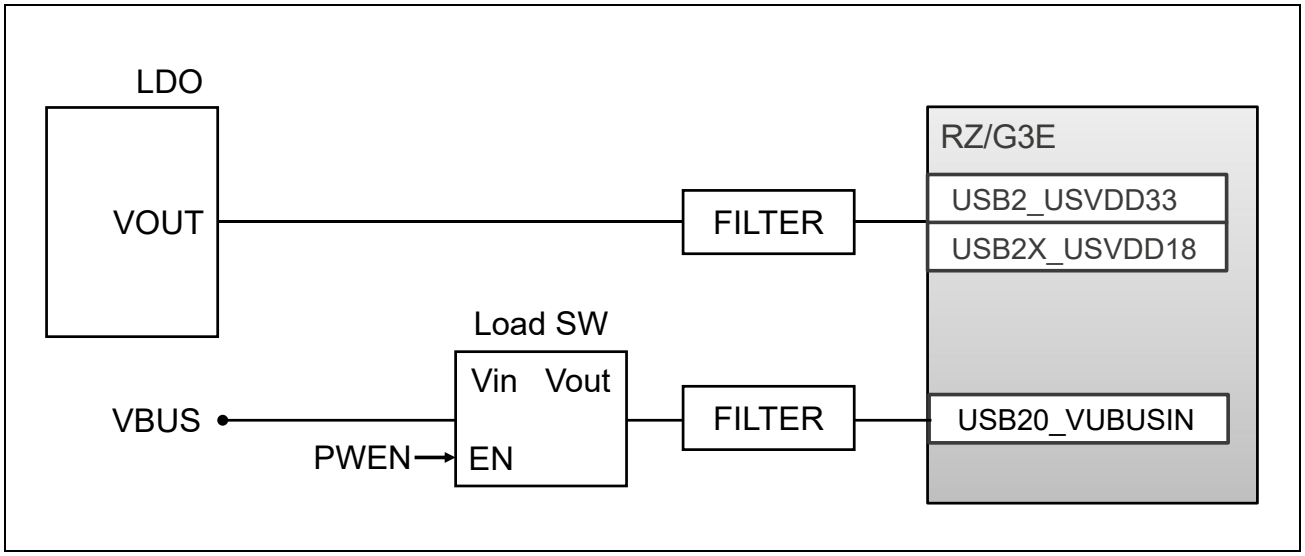

Figure 3.2 Reverse Current from the VBUS

If the USB2_USDVDD 0.8 V power supply is powered by a single power supply and is not shared with other 0.8 V power supplies, a 2.2-kΩ resistor should be placed between USB2_USDVDD and GND. This prevents the reverse current from flowing from the power supply terminal of the MPU to the power supply IC during USB suspend. (**Figure 3.3**) If the USB2_USDVDD is shared with other power supplies, the resistor is not needed because the leakage current flows to other power supply terminals (**Figure 3.4**).

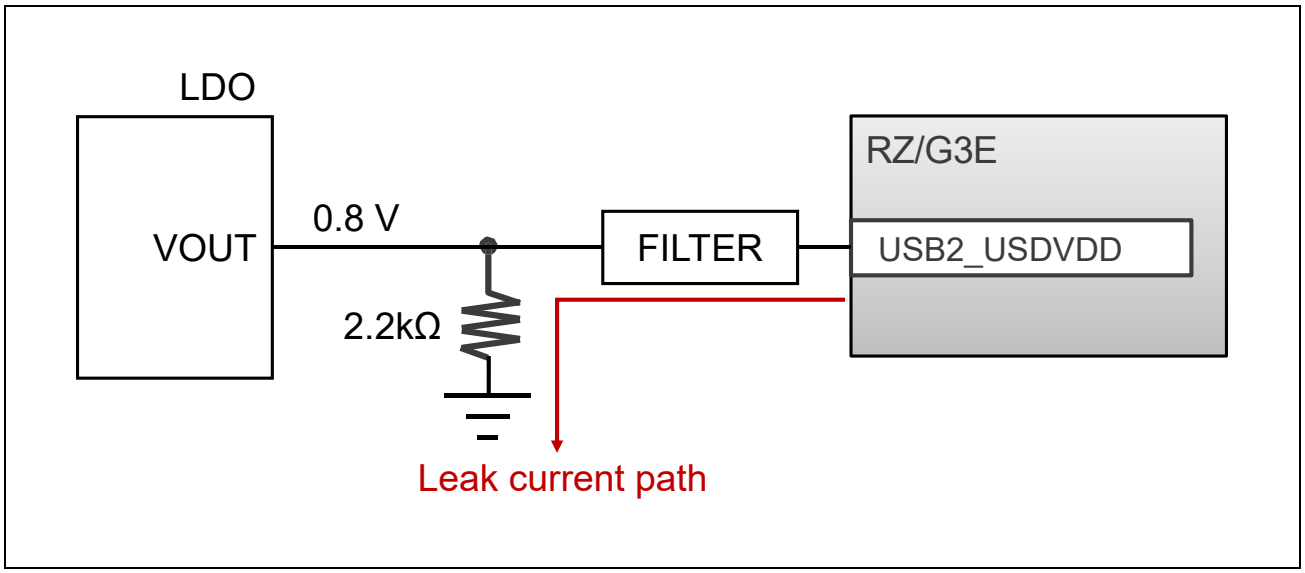

Figure 3.3 Reverse Current from USB2x_USDVDD without Branch

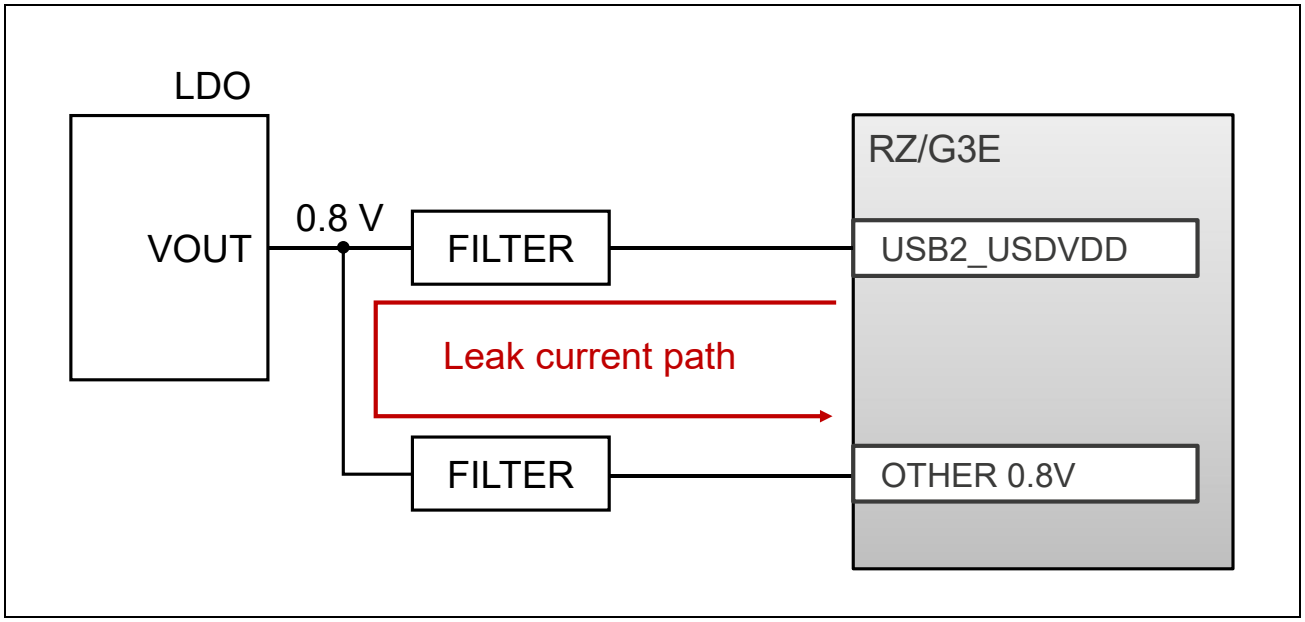

Figure 3.4 Reverse Current from USB2x_USDVDD with Branch

3.3 External Resistors

- A 30kΩ ± 1% resistor should be placed on the USB20_VUBUSIN, and a 200Ω ± 1% resistor on the USB20_TXRTUNE.
- Do not place the capacitance in parallel with an external resistor.
- Connect a 1 µF capacitor to the USB connector to prevent chattering.
- The wire between TXRTUNE and the external resistor should be as thick as possible.
- The total L/C/R values of USB20_VUBUSIN and USB20_TXRTUNE, including the MPU package, board wiring, and USB connector, should be 4 nH or less for inductance, 5 pF or less capacitance, and 1Ω or less for resistance.
- Signals that generate noise, such as clocks, should be kept away from USB20_TXRTUNE or shielded with ground.
  In addition, cross-wiring is prohibited.
- The layer below the external resistor and wiring layer should be the GND plane.

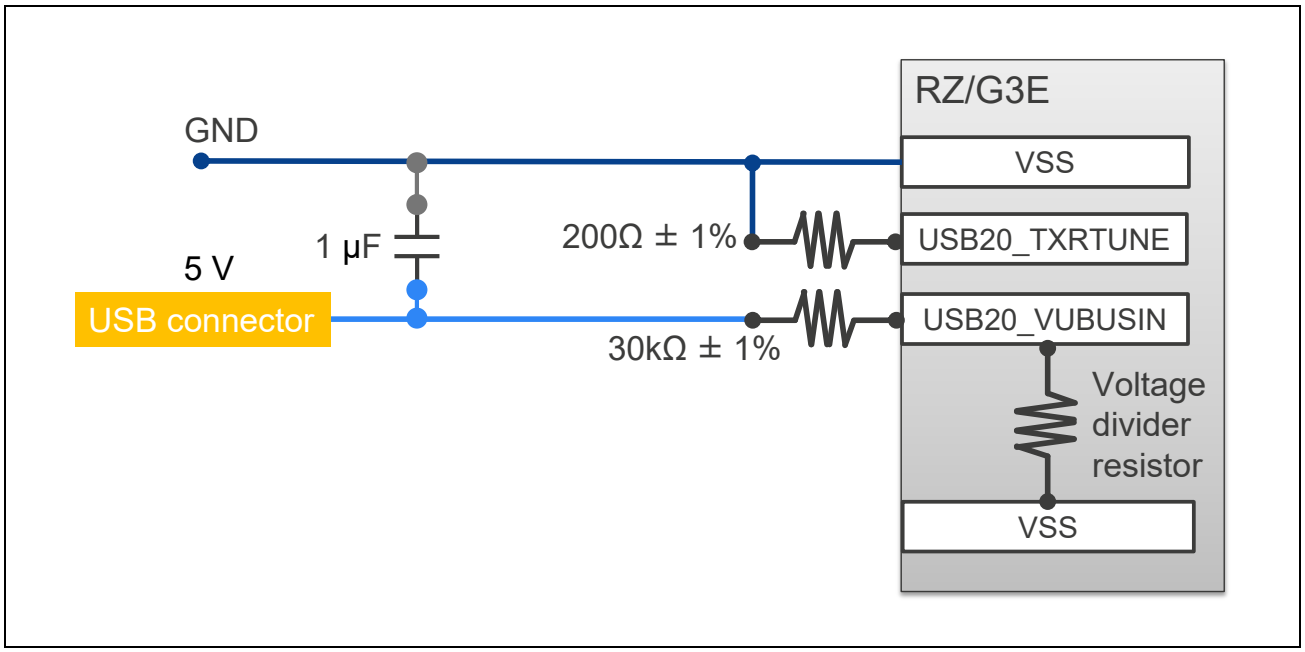

Figure 3.5 External Resistors for USB 2.0 for RZ/G3E

4. USB 3.2 Gen2

In this chapter, the design guideline about USB3.2 Gen2 is described.

4.1 Signal Trace

4.1.1 General Guidelines

Give design priority to the high priority items marked with a check mark.

Table 4.1 Guidelines for PCB Signal Lines of USB 3.2 Gen2

Items		Guidelines	Fig.	Notes
Line impedance		✓: Differential 100Ω ± 10% Single-end 50Ω ± 10%	—	1
Line length difference	Between each pos. and neg.	✓: As the same length as possible ✓: Line length is as short as possible	—	2
Line bending		Recommended: External angle 45° (Prohibition: > 45°)	—	—
Line layer Numbers of via	Between each pos. and neg.	Same layer *Note*: Recommended: Top layer without any vias Same via number (number is as few as possible)	—	—
Line width	Between each pos. and neg.	✓: As the same width as possible	—	—
Return path		✓: Place Continuous Ground Plane under Diff.	(5) in **Figure 1.2**	—
		Place GND through-hole next to signal through-hole Place GND vias symmetrically next to Diff.	—	—

Note 1. Priority should be given to differential impedance for characteristics.

Note 2. Target value of difference in wiring length: within a maximum of 0.25 mm.

4.1.2 Differential Signal

- To avoid crosstalk, route the Tx and Rx pairs in different layers. When routing in the same layer, the distance between the Tx pair and the Rx pair should be at least six times the height of the dielectric on the PCB, and the crosstalk should be less than -30 dB.
- Place an AC-coupling capacitance of 0.1 µF near the TX pin of the MPU and the opposing device.

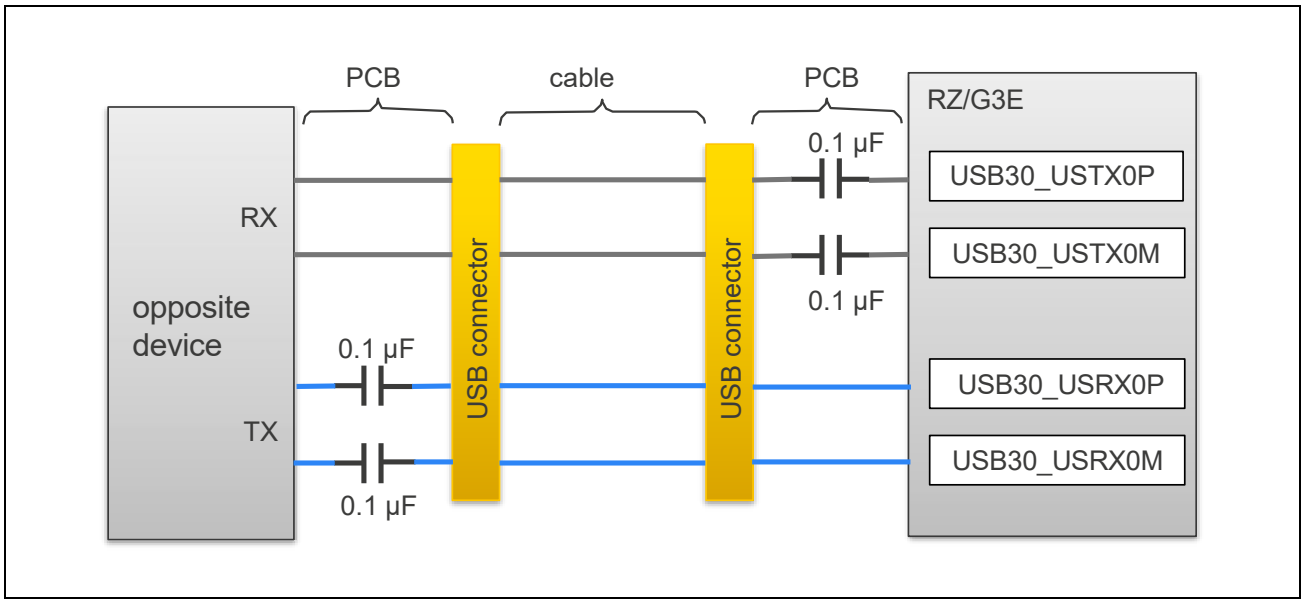

Figure 4.1 Differential Signals of USB 3.2 Gen2 for RZ/G3E

- Consider using thinner core substrates such as 400 µm, if feasible.
- Place GND return vias adjacent to the differential pair vias.
- The return path should be continuous with GND.
- To reduce signal reflections, provide a cutout of the GND plane under the pad of the AC-coupling capacitance.
- Do not allow differential pair wiring to cross power supply splits or plane voids.

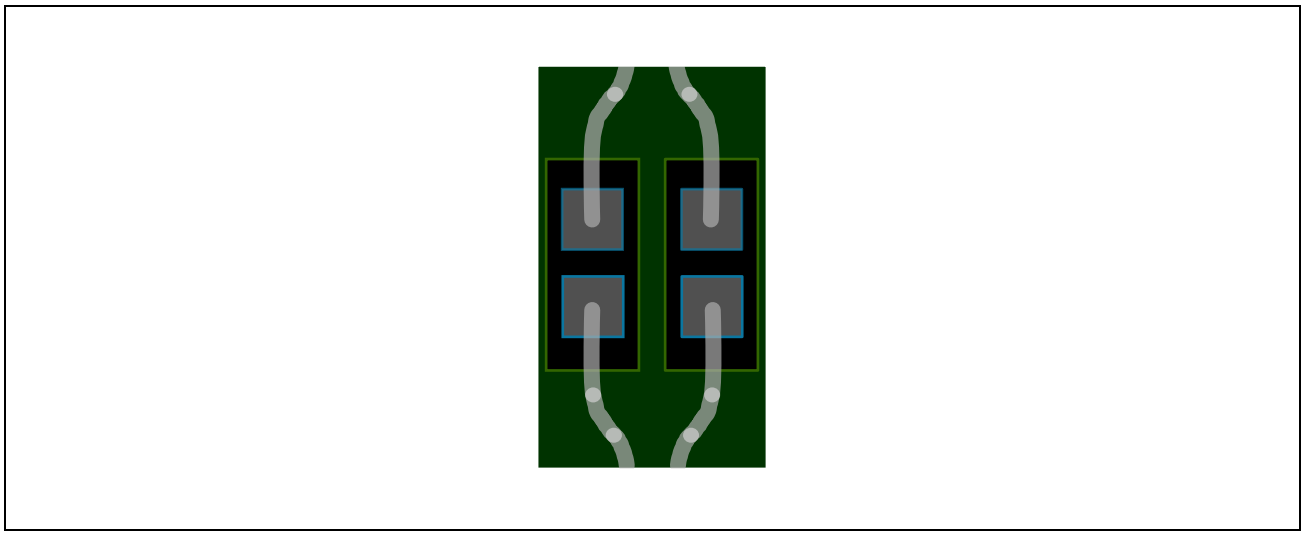

Figure 4.2 Cutout of the GND Plane under the Pads of the AC-Coupling Capacitors

4.2 Power Supply

- Each USB 3.2 power supply (USB30_USVPH and USB20_USVPTX) is an IP-only power supply. If these power supplies are supplied from a single power supply, it is recommended to use ferrite beads. When using ferrite beads, do not use the power supply through the ferrite beads for anything other than USB 3.2. Place ferrite beads as close to the MPU as possible.
- Place the capacitors in ascending order of capacitance from the MPU to the regulator side. The recommended arrangement of capacitors for each power supply is 0.01 µF, 0.1 µF, 4.7 µF, 10 µF, and 47 µF.
- The 0.01-µF and 0.1-µF capacitors should be placed as close to the MPU as possible. The 47-µF capacitor can be further away.
- Do not place noise sources such as memory near GND.
- In order to minimize the impedance of each power supply wiring, make the wiring as wide and short as possible.
- Place the USB30_USVPH/USB30_USVPTX vias and VSS vias next to each other as pairs.
- All power supplies should be designed as plain.
- For information on how to verify ripple noise, refer to the separate document that provides the package S-parameters, CPM, and verification environment.
- It is recommended to add a 100 nF PCB decoupling capacitor to the return pin (VSS) closest to each supply pin.

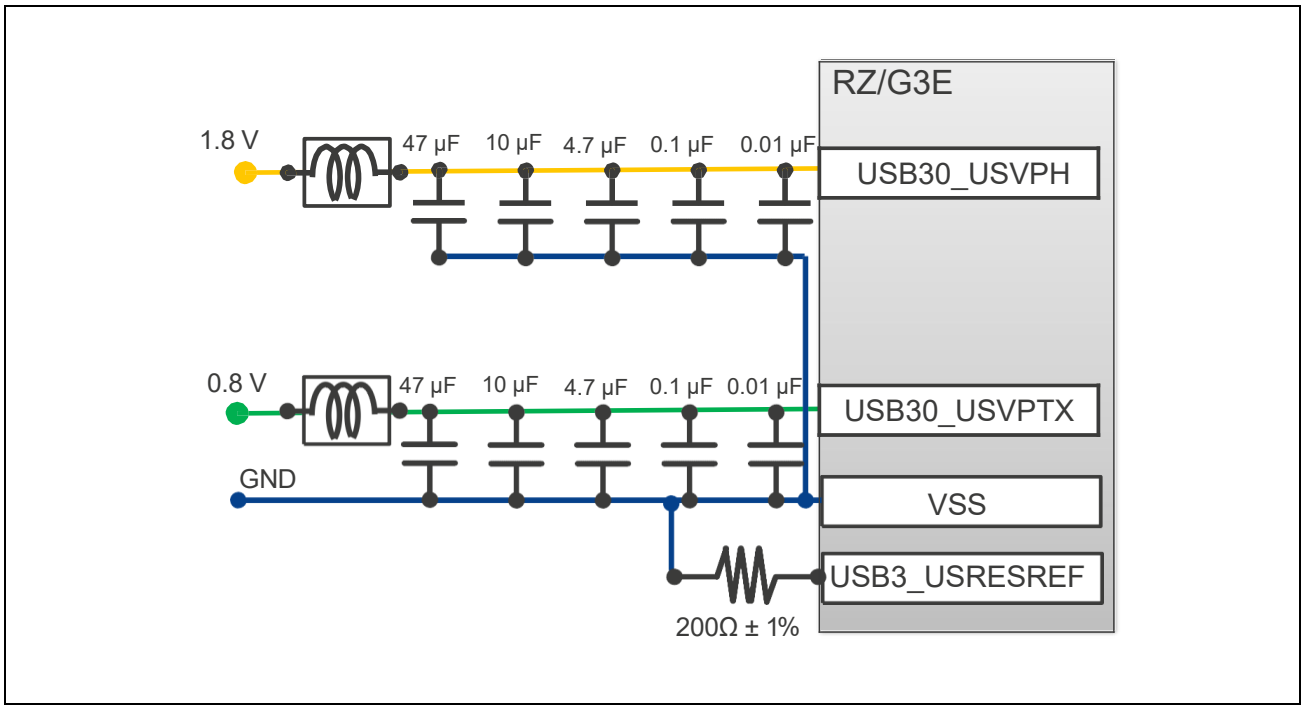

Figure 4.3 External Capacitors for USB 3.2 Gen2

4.3 External Resistors

- Connect 200Ω ± 1% to the RESREF pin. Do not place the capacitance in parallel with an external resistor.
- The board routing from RESREF to the external resistor should be as thick as possible, and the capacitance value of RESREF, including the package and board routing, should be less than 10 pF.
- The GND connected to the external resistor should be as close as possible to the VSS voltage.
- Signals that generate noise, such as clocks, should be kept away from RESREF or shielded with ground. Also, make sure that their wires do not intersect.
- The layer under the external resistors and wiring should be the GND plane.

5. PCI Express 3.0

In this chapter, the design guideline about PCI Express 3.0 is described.

Applicable Standard

For general information on electrical and transfer path characteristics, and on connector specifications required in designing a PCB, refer to the specifications issued by the standards certification bodies listed in the table below.

Table 5.1 Standard Applicable to PCI Express

Standards Certification	Title of Specification
PCI-SIG	PCI Express® Base Specification Revision 4.0
	PCI Express Card Electromechanical Specification Revision 4.0

5.1 Signal Trace

5.1.1 General Guidelines

For the basic design of differential wiring patterns, refer to the guidelines issued by the PCI-SIG at the link given below. The information is relevant regardless of whether the standard being implemented is PCI-Express generation 1, 2, or 3. The relevant descriptions are mainly given in the section, Layout considerations.

Note that the differential impedance value along the transfer path (differential wiring pattern) differs with the module, that is, according to whether it is PCI-Express generation 1, 2, or 3.

- Board Design Guidelines for PCI Express™ Architecture
  (Please download from https://members.pcisig.com/)

5.1.2 Differential Signals

- Place an AC-coupling capacitance of 0.2 µF near the TX pin.
- Match the wire lengths so that there is no skew in the differential signals.
- To minimize losses, keep traces as short as possible.
- For all high-speed signals, use wider traces.
- Do not bend the wiring at 90 degrees, but bend it twice at 45 degrees.
- Keep signal traces and clock signal traces away from noise sources, including other signal traces.
- Avoid layer changes with vias as much as possible. If vias are used to trace differential signals, both wires should have the same number of vias.
- The traces should have the same width, be parallel, and be routed on the same layer. The top or bottom layer is recommended.
- Make sure that the wiring does not cross the power supply split or plane void.
- Make sure you have enough space from the edge of the signal trace to the void area of the edge. Leave at least more than the signal trace width.
- Refer to the PCI Express Architecture Board Design Guidelines published by the PCI-SIG.

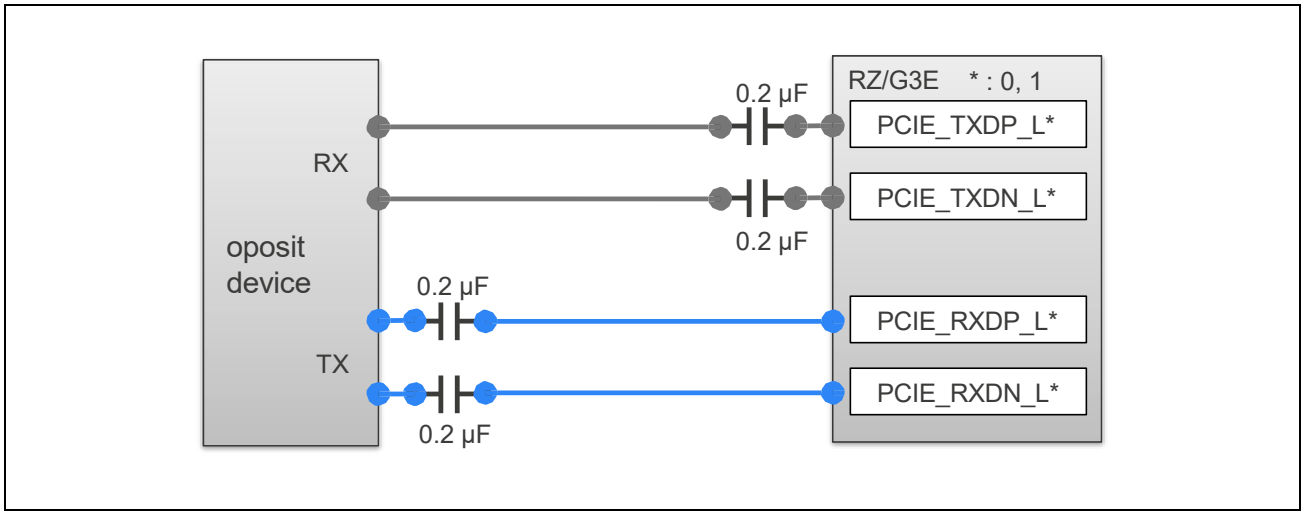

Figure 5.1 Topology of PCIe 3.1

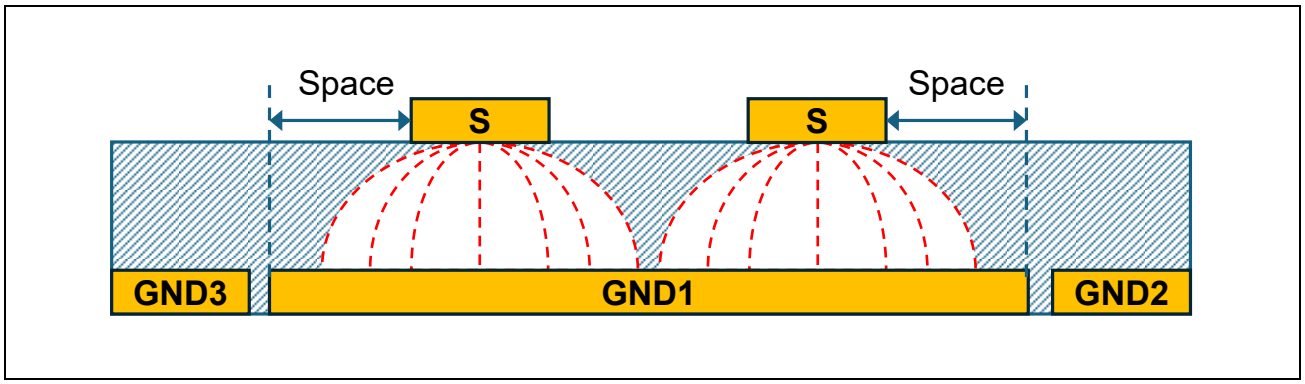

Figure 5.2 Sufficient Space of Reference Ground Plane

- It is recommended that DP/DN wiring be designed with a typical 100Ω ± 5% differential impedance and a typical 50Ω ± 5% single-ended impedance. In addition, priority should be given to differential impedance for characteristics. Alternatively, it can be designed with a typical 85Ω ± 5% differential impedance and a typical 42.5Ω ± 5% single-ended impedance.
- To maximize the signal electrical performance of differential signals, it is recommended to use backdrilled or blind vias instead of through-vias.
- The land of the differential signal should be in the shape of a teardrop.
- Place the GND vias between the TX pair and the RX pair. When the vias of the TX pair and the vias of the RX pair are orthogonal to each other, magnetic coupling can be reduced and near-end crosstalk can be minimized.

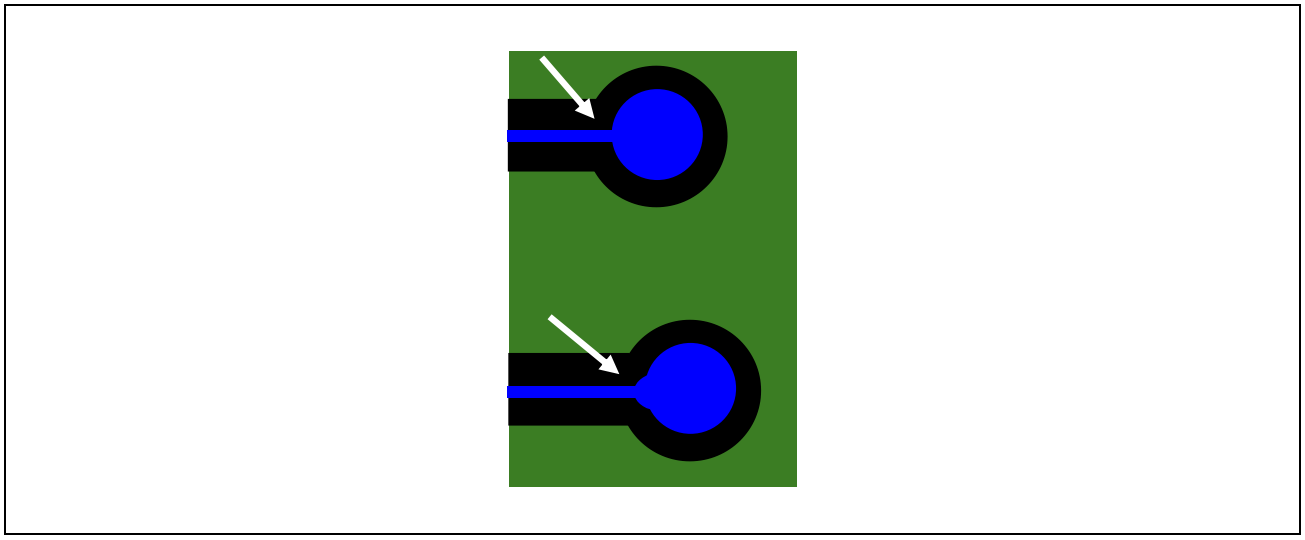

Figure 5.3 Teardrop Shape of Lands and Vias

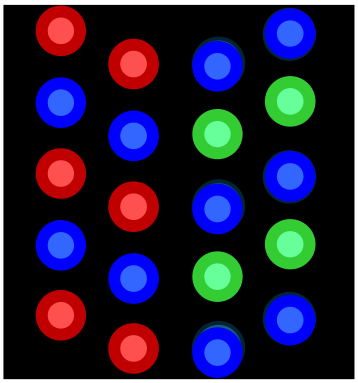

Figure 5.4 Example of Via Pattern

5.2 Power Supply

- Place the low ESR decouple capacitor as close to the power supply as possible.
- Each PCIe power supply (PCIE_VCC18ACMN, PCIE_VCC18AL01 and PCIE_VCC08AL01) is an IP-only power supply. If you want to share the power supply of the source with other power sources, consider using ferrite beads. When using ferrite beads, do not use power supplies through ferrite beads for anything other than PCIe.
- The power supply should be connected to the power plane or ground plane with short, wide wires to ensure low inductance.
- It is recommended to perform inductance calculations to guarantee proper operation of the PCIe interface.
- The inductance on the PCB should be less than 1.2 nH if the compliance test specified to the PCI Express® Base Specification standard is not performed.

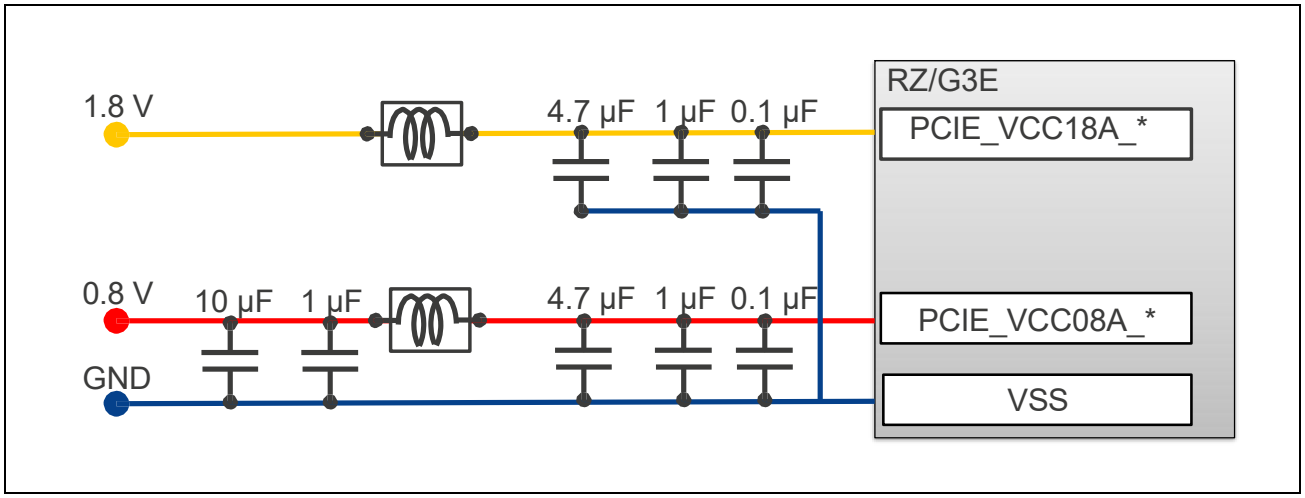

Figure 5.5 External Capacitors for PCIe 3.0

5.2.1 Inductance Extraction Methodology

The inductance of the loop formed by the PCB traces to the closest decoupling capacitor can be modeled directly or indirectly and calculated using the following formula. Refer to each section for details.

$$L_{loop} = L_{pwr} + L_{gnd}$$

5.2.1.1 Direct Modeling

Direct modeling can be done with a parasitic extractor (e.g., Ansys Q3D).

Figure 5.6 illustrates direct modeling.

Designate the BGA ball as the source and the decoupling capacitor pad as the sink.

If there are multiple BGA balls for a specific power or ground net, merge them together in parallel to calculate a single equivalent source-to-sink inductance value.

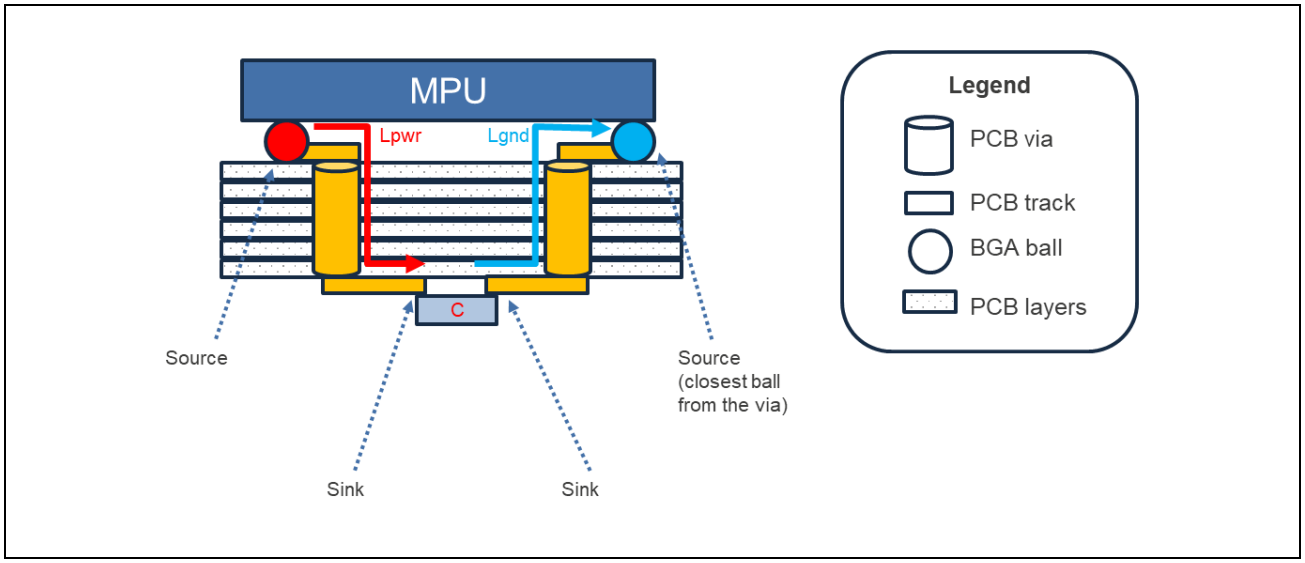

Figure 5.6 Concept for Direct Modeling

5.2.1.2 Indirect Modeling

Indirect modeling can be performed using 2.5D (e.g., Ansys SIwave) or 3D (e.g., Ansys HFSS) tools.
To achieve greater accuracy in modeling, it is recommended to use 3D simulation, as 2.5D simulation only considers the vertical dimension of vias, neglecting other 3D effects.

Figure 5.7 illustrates indirect modeling.

Create a 2-port S-parameter model representing the power and ground net.

Also, create an RL lumped model to approximate the net's impedance.

Excite both models with a current source, perform AC simulations, and compare responses magnitudes.

Run AC simulation and probe the magnitude of the net connected to the current source.

Adjust the inductance and resistance values of the lumped model to align its frequency response with that of the S-parameter model.

Figure 5.8 shows the fitted lumped model response compared to the S-parameter model response.

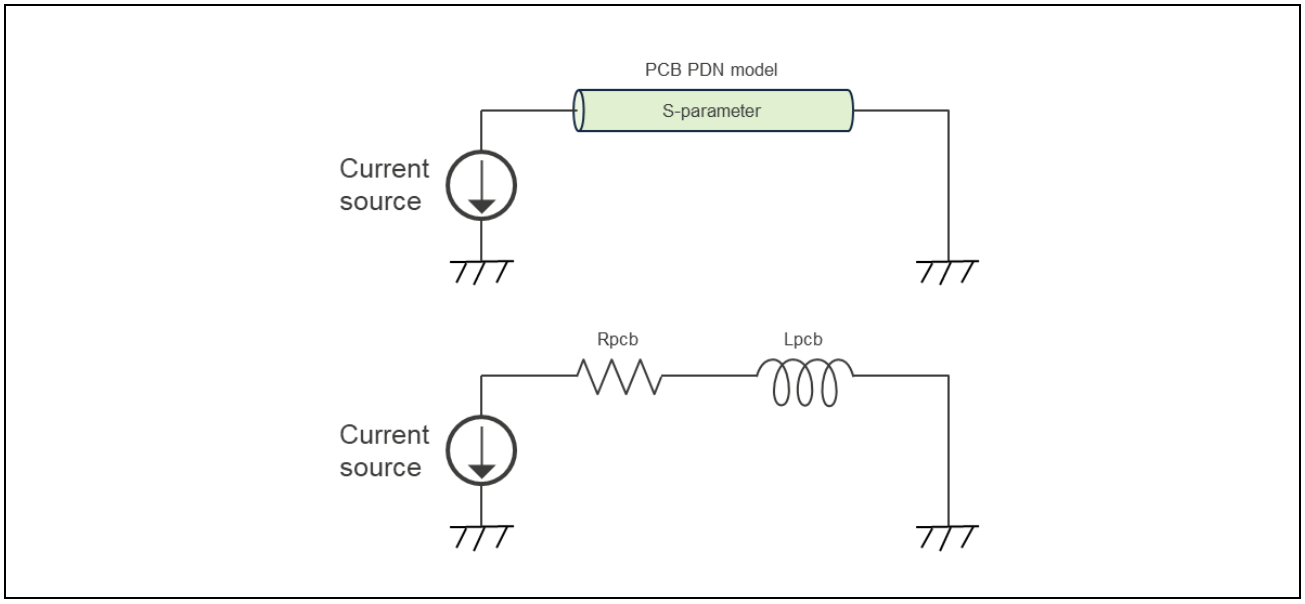

Figure 5.7 Simulator Circuit for Indirect Modeling

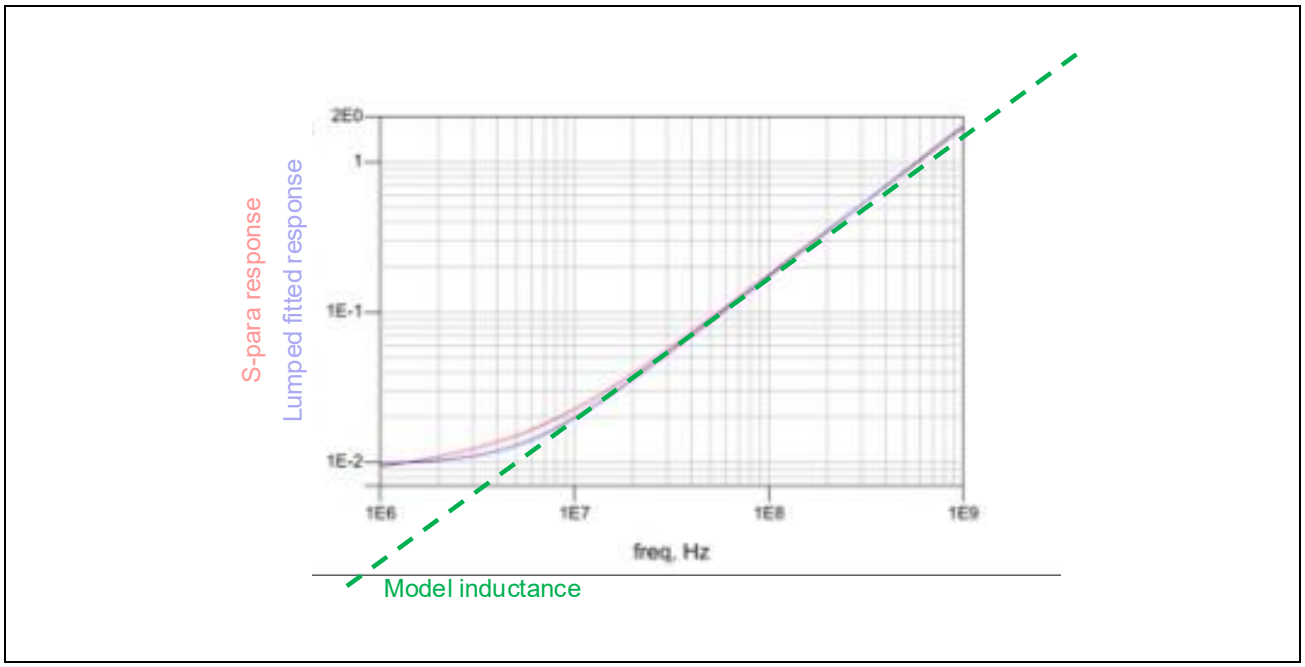

Figure 5.8 Fitted Lumped vs. S-Parameter Model Response

5.3 Clock Input

- The differential clock input should be terminated with 50Ω referenced to VSS.
- Provide a reference clock common to the MPU and the opposing device.

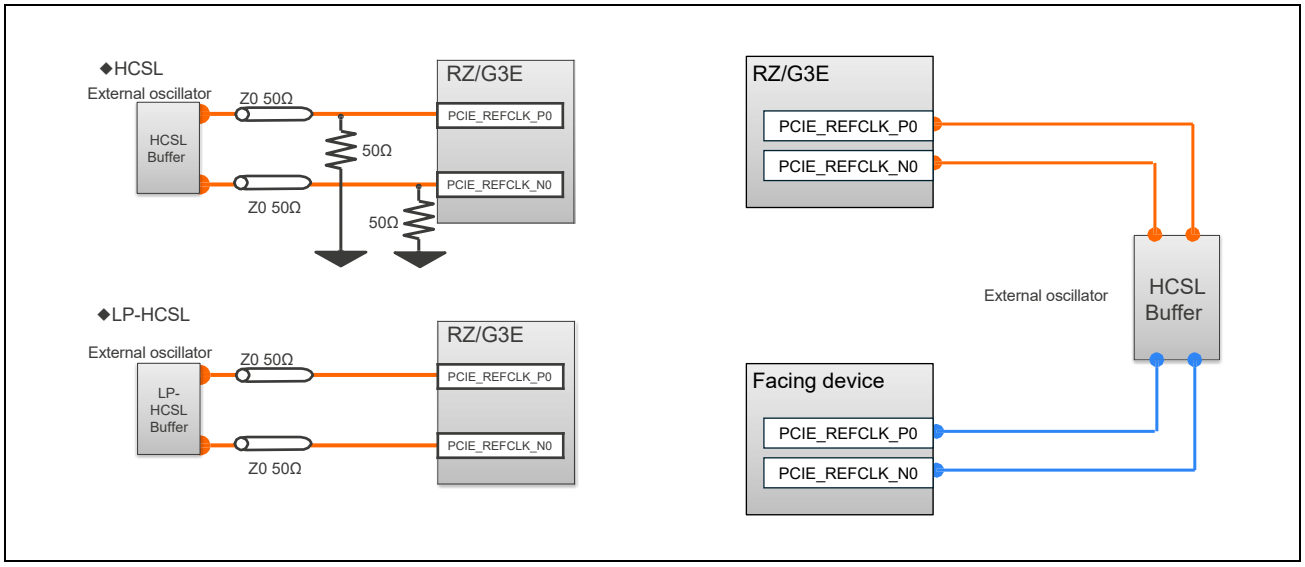

Figure 5.9 Clocking Configurations

6. 12-Bit A/D Converter

In this chapter, the design guideline about A/D Converter is described.

6.1 Power Supply

- ADAVDD18 should have decoupling capacitors with a value of at least 1 µF and 0.1 µF to 10 µF capacitors near the MPU. These capacitors must be placed on the same GND plane of the ADAVSS18.
- Analog inputs (ANI000 to 007) should have traces for equal resistance and capacitance on the PCB level. Shielding of signals is highly recommended with ADAVSS18.
- Analog inputs (ANI000 to 007) should not cross or run parallel to any fasting changing signals like digital ones or the clock input.
- The ferrite beads should be connected as close as possible to the LSI.

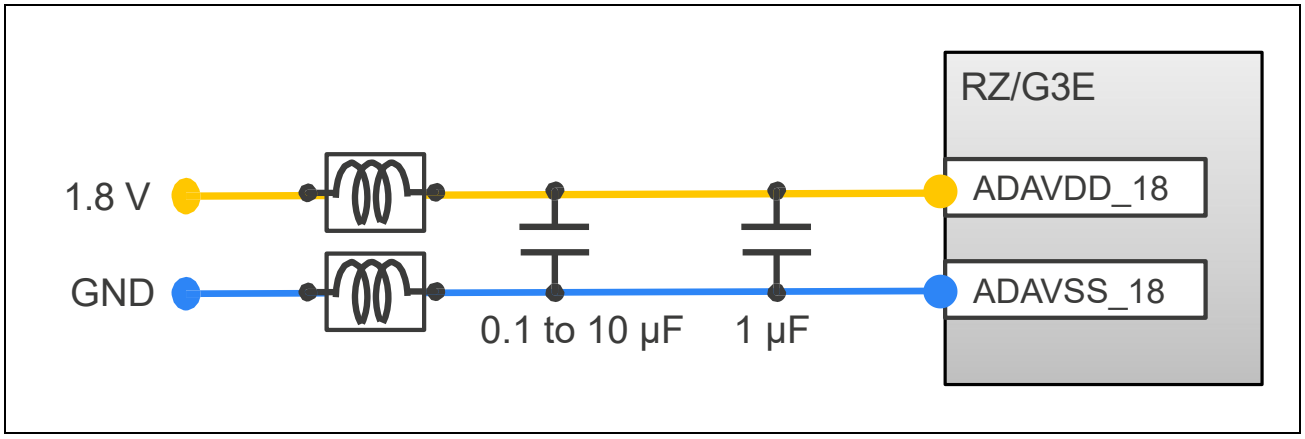

Figure 6.1 External Capacitors for A/D Converter

7. PLL

In this chapter, the design guideline about A/D Converter is described.

7.1 Power Supply

- Ceramic capacitors (0.1 µF) should be placed close to the MPU.
- The traces for the ceramic capacitors (0.1 µF) should be wide and short (less than 2 mm).
- If the power supply is shared with other IP power supplies, consider using the ferrite bead.

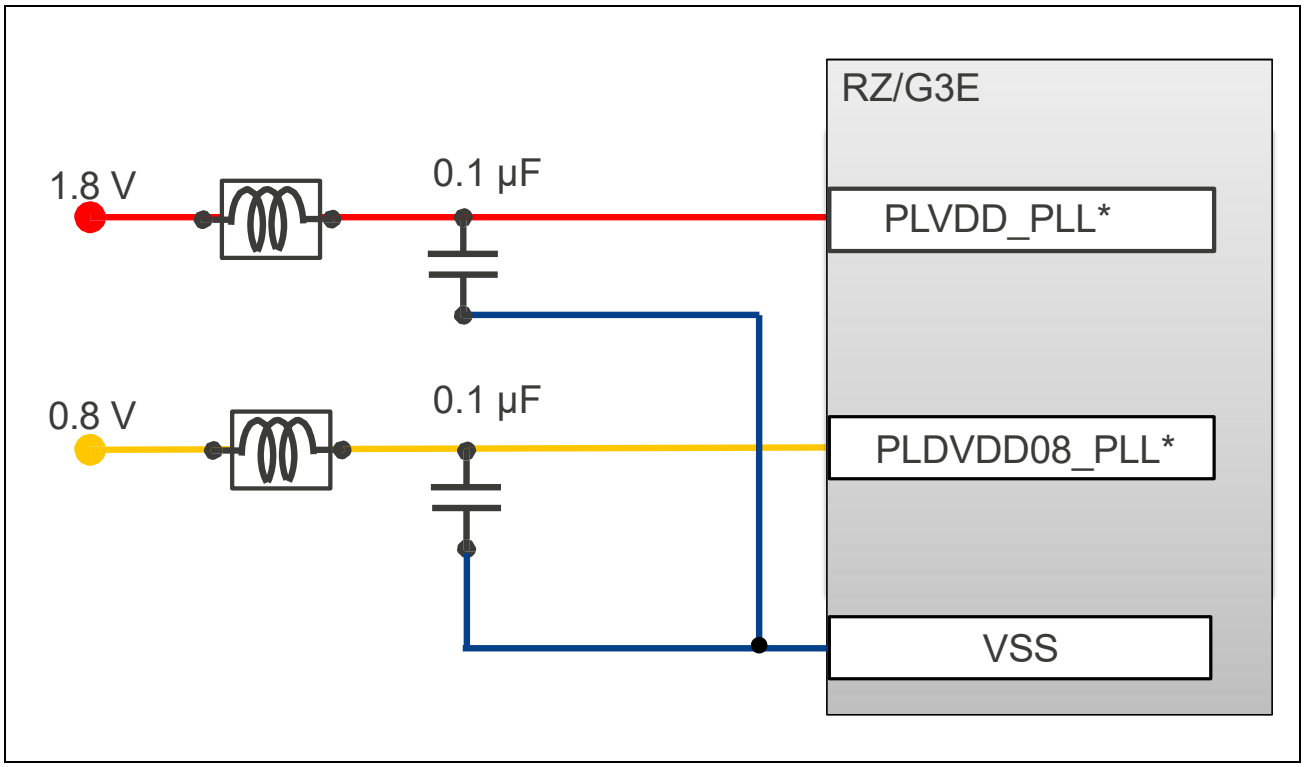

Figure 7.1 External Capacitors for PLL

8. OSC

8.1 Signal Trace

8.1.1 Crystal Frequency at 32.768 kHz

- The trace should be used in the top layer of the board (shielded with GND).
- The GND shields should be placed in the lower layer of the board.
- The trace should not be used in the middle layer of the board.
- The trace length from RTXIN/RTXOUT to crystal should be no greater than 10 mm.
- The trace width of RTXIN/RTXOUT should be 0.1 to 0.3 mm.
- RTXIN/RTXOUT should be more than 0.3 mm away from other signals.
- The space between X1 and X2 should be more than 0.3 mm.

Table 8.1 32.768 kHz

Trace Capacitance CX12	Max. Load Capacitance CL1	Max. Load Capacitance CL2
0 pF	25 pF	25 pF
1 pF	23 pF	23 pF
2 pF	21 pF	21 pF
3 pF	19 pF	19 pF
4 pF	17 pF	17 pF
5 pF	15 pF	15 pF

Note: CL = (CL1 X CL2) / (CL1 + CL2) + CX12
Max. CL: Less than 12.5 pF at 32.768 kHz

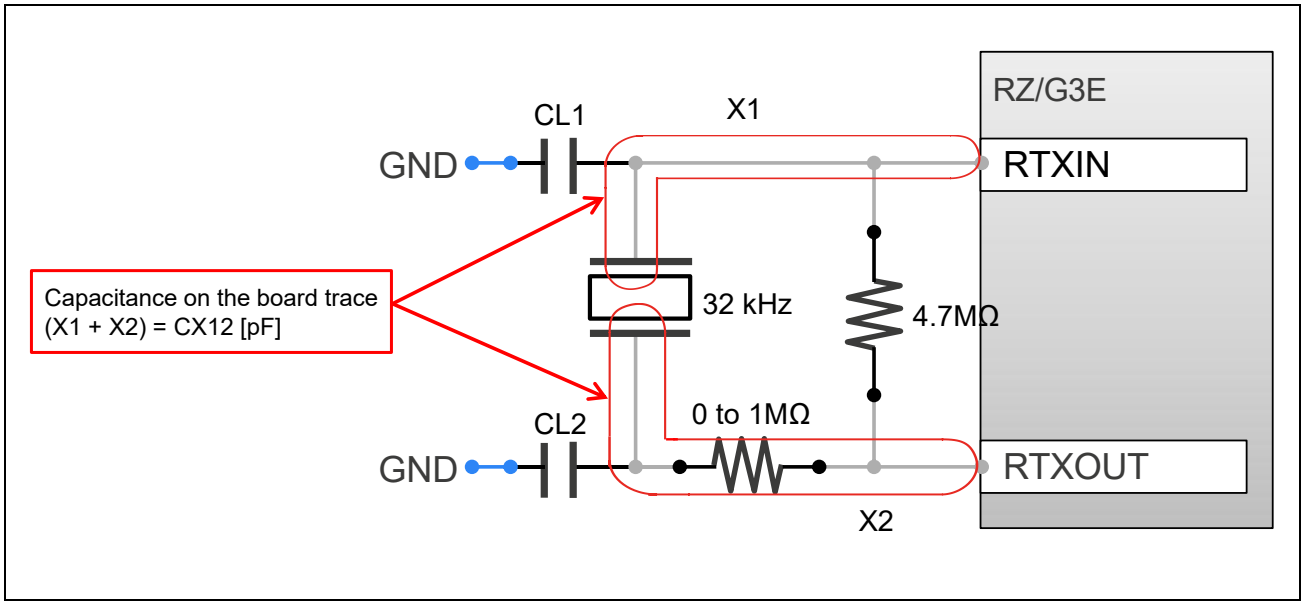

Figure 8.1 RTC Clock OSC Design Guideline

8.1.2 Crystal Frequency at 24 MHz

- Ceramic capacitors (0.1 µF) should be placed close to the MPU.
- The trace should be used in the top layer of the board (shielded with GND).
- The GND shields should be placed in the lower layer of the board.
- The trace should not be used in the middle layer of the board.
- The maximum trace-length from QEXTAL/QXTAL to crystal should be no greater than 10 mm.
- The trace width of QEXTAL/QXTAL should be 0.1 to 0.3 mm.
- QEXTAL/QXTAL should be more than 0.3 mm away from other signals.
- The space between X1 and X2 should be more than 0.3 mm.

Table 8.2 24 MHz

Trace Capacitance CX12	Max. Load Capacitance CL1	Max. Load Capacitance CL2
0 pF	24 pF	24 pF
1 pF	22 pF	22 pF
2 pF	20 pF	20 pF
3 pF	18 pF	18 pF
4 pF	16 pF	16 pF
5 pF	14 pF	14 pF

Note: CL = (CL1 X CL2) / (CL1 + CL2) + CX12
Max. CL: Less than 12.5 pF at 24 MHz

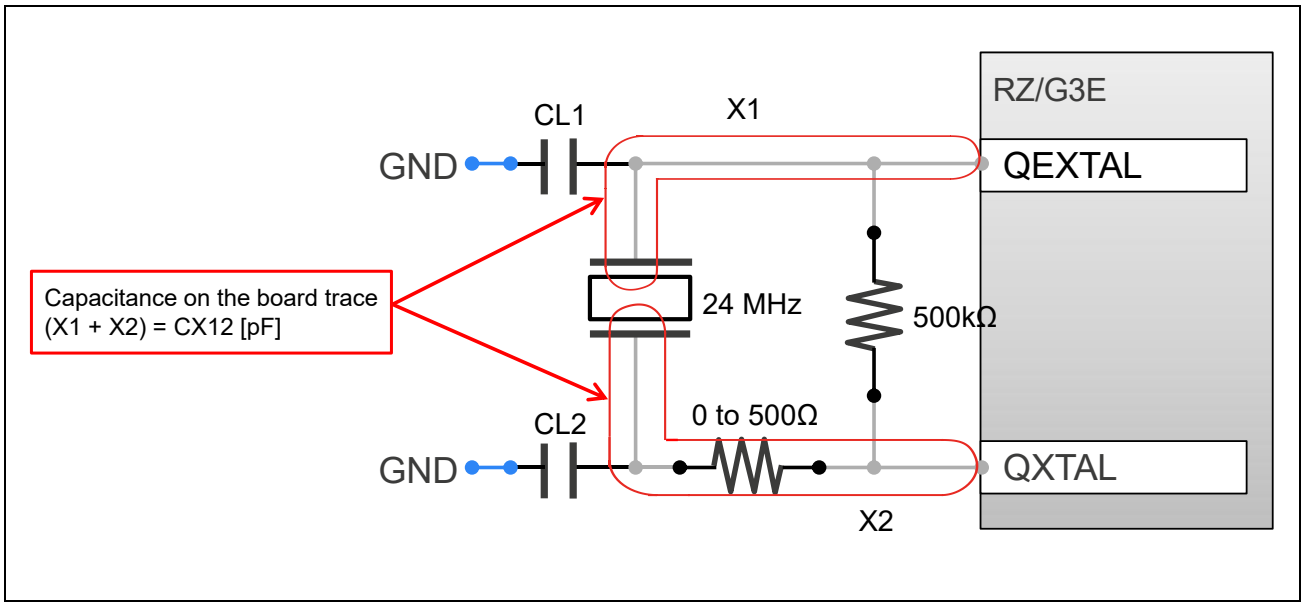

Figure 8.2 System Clock OSC Design Guideline

8.1.3 Crystal Frequency at 48 MHz

- Ceramic capacitors (0.1 µF) should be placed close to the MPU.
- The trace should be used in the top layer of the board (shielded with GND).
- The GND shields should be placed in the lower layer of the board.
- The trace should not be used in the middle layer of the board.
- The maximum trace-length from AUDIO_EXTAL/AUDIO_XTAL to crystal should be no greater than 10 mm.
- The trace width of AUDIO_EXTAL/AUDIO_XTAL should be 0.1 to 0.3 mm.
- AUDIO_EXTAL/AUDIO_XTAL should be more than 0.3 mm away from other signals.
- The space between X1 and X2 should be more than 0.3 mm.

Table 8.3 48 MHz

Trace Capacitance CX12	Max. Load Capacitance CL1	Max. Load Capacitance CL2
0 pF	20 pF	20 pF
1 pF	18 pF	18 pF
2 pF	16 pF	16 pF
3 pF	14 pF	14 pF
4 pF	12 pF	12 pF
5 pF	10 pF	10 pF

Note: CL = (CL1 X CL2) / (CL1 + CL2) + CX12
Max. CL: Less than 10 pF at 48 MHz

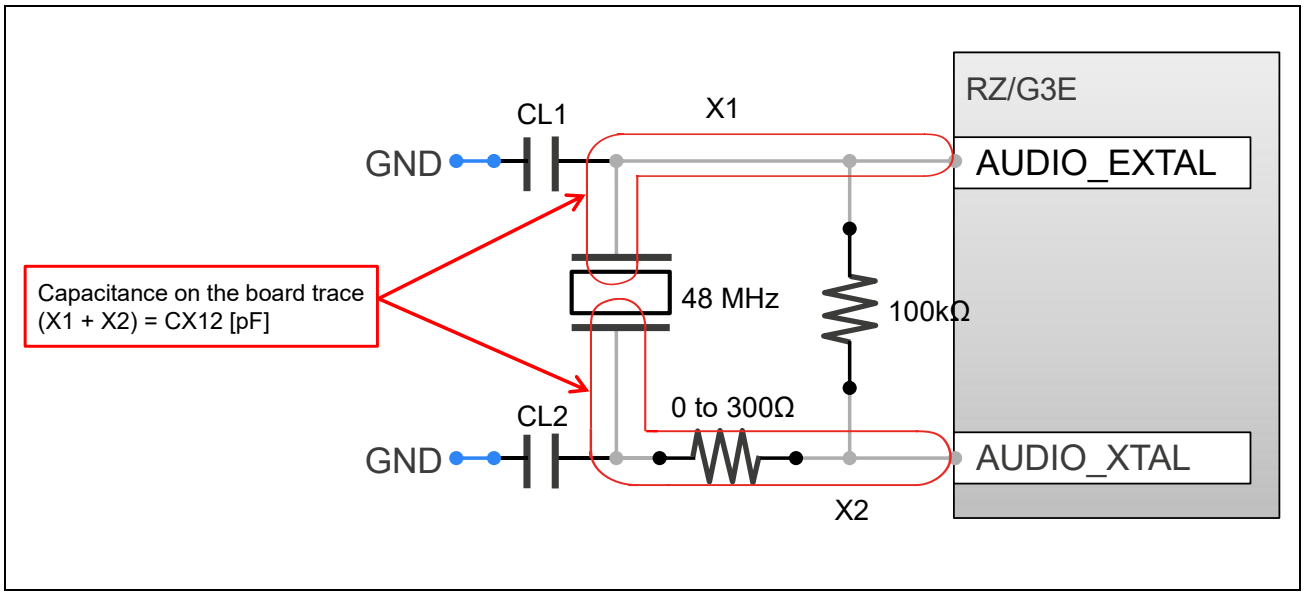

Figure 8.3 Audio Clock OSC Design Guideline

Example of OSC Board Pattern

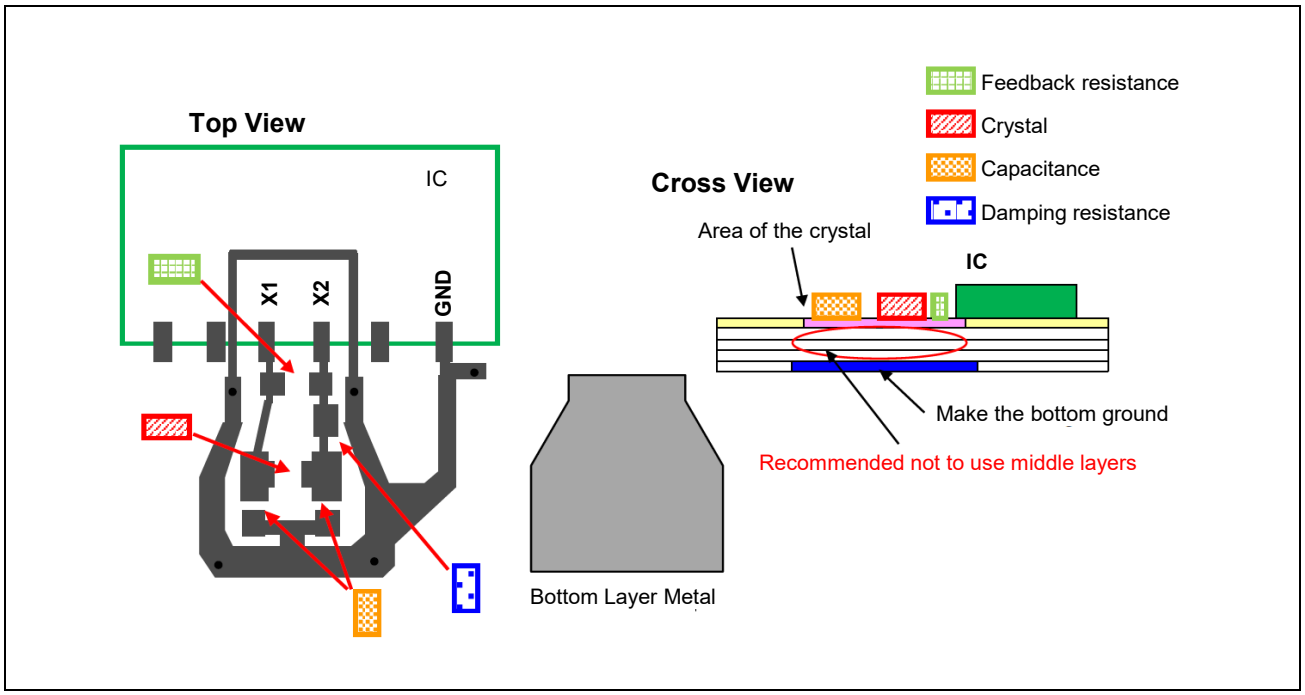

Figure 8.4 Board Pattern Image for Stable Oscillation

9. Modeling

Perform a simulation with a frequency range up to 10 GHz in the case of extracting S parameters.

Appendix A Concept of Loop Inductance

The target inductance can be obtained by calculating the loop inductance from the VDD balls of the package to the VSS balls of the package taken as an ideal GND as shown in the figure below. In this case, include the equivalent series inductance (ESL) component of the bypass capacitor placed close to the LSI chip.

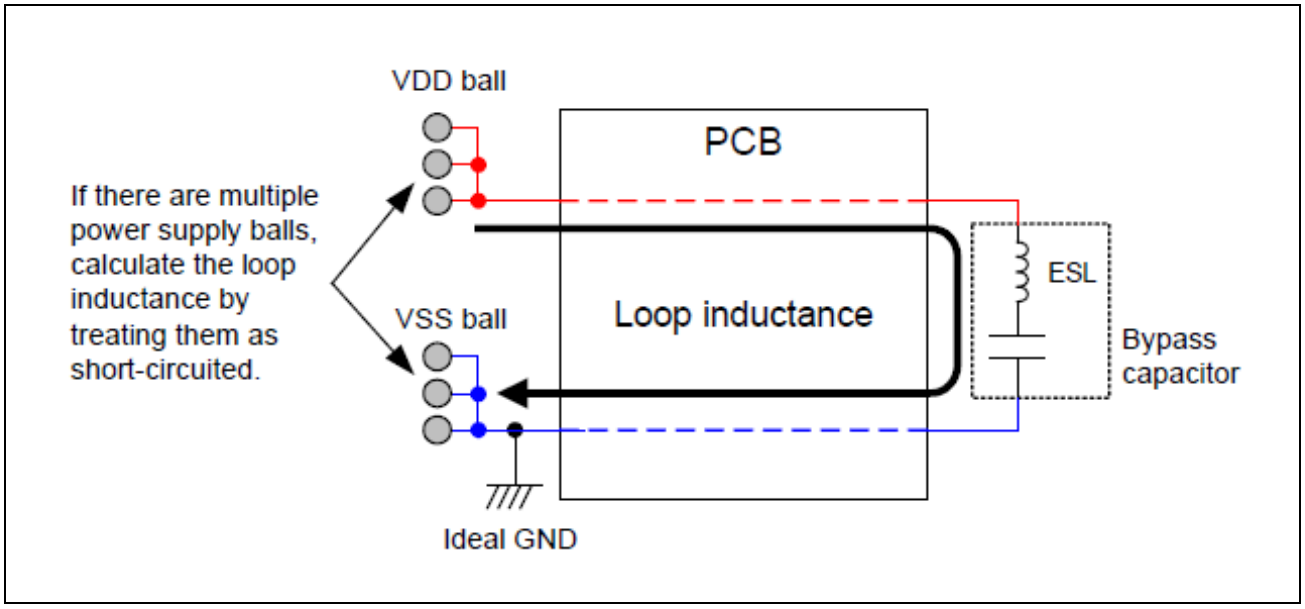

Figure A.1 Concept of Loop Inductance

Appendix B EMI/ESD Protection

Notes on EMI/ESD protection are described below.

When components for EMI/ESD protection such as coils and diodes are mounted on the USB transmission lines, they should be allocated near the USB transmission lines and the wiring should be as short as possible.

The components for EMI/ESD protection must be USB 2.0 High-Speed compliant. By mounting EMI/ESD protection components, an inconsistent impedance may occur on the USB transmission lines, and the waveform may become distorted. Components for use should be selected after thorough evaluation.

Figure B.1 shows an example connection when the components for EMI/ESD protection are used.

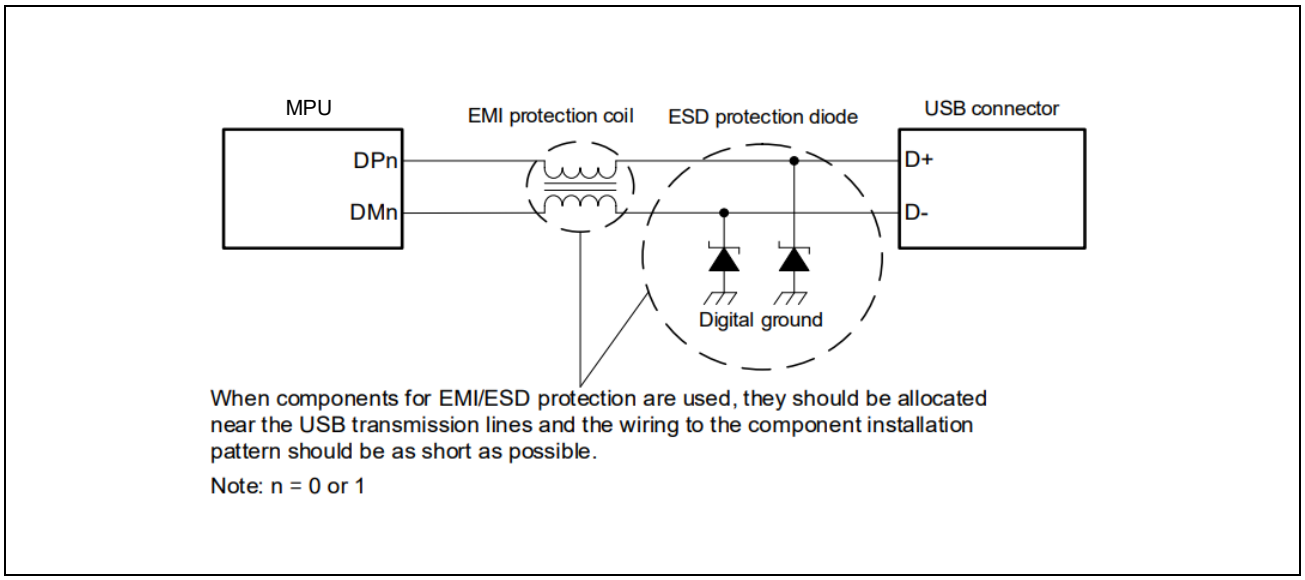

Figure B.1 Connection Example of Components for EMI/ESD Protection

Appendix C Guidelines for Traces

Reference Plane

Signals should be routed on the GND plane and should not cross planes, PLANE VOIDs, or anti-pads as these can cause high frequency currents.

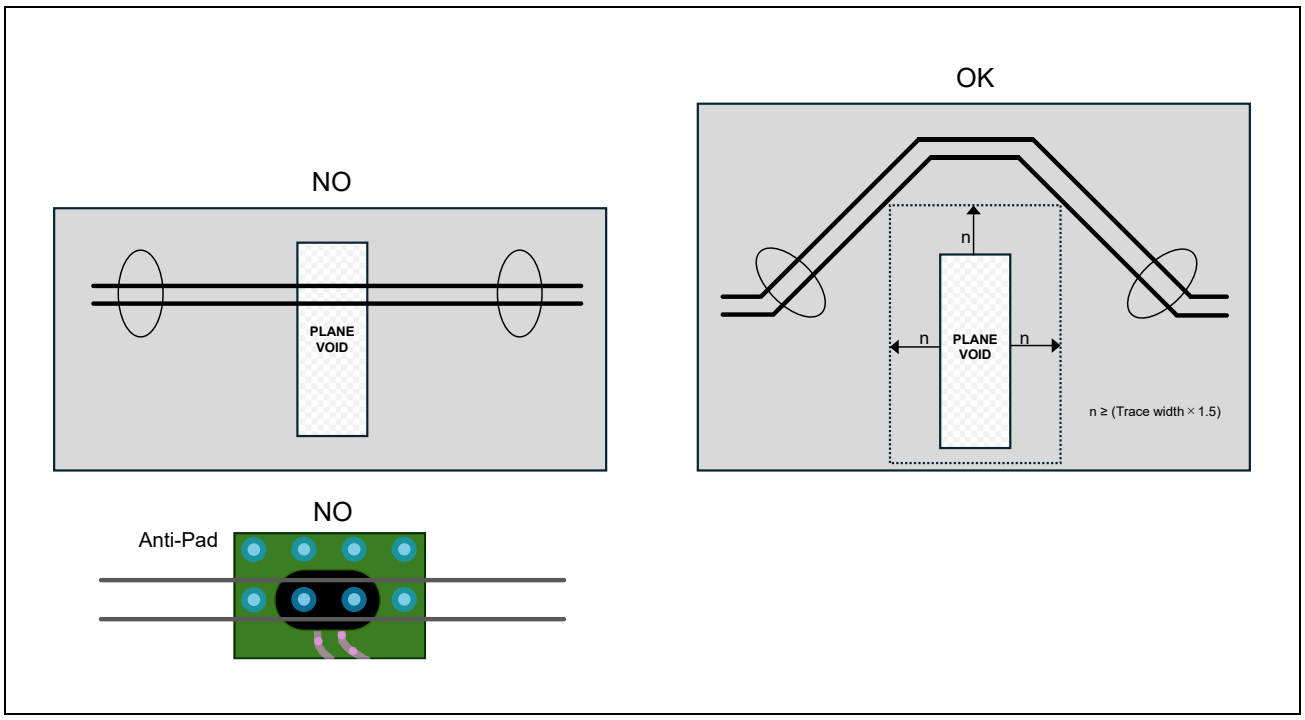

Figure C.1 Plane Void and Anti-Pad

If the signal needs to cross different GND planes, connect them with stitching capacitors. It can prevent high-frequency currents in the return path. The stitching capacitor should have a capacitance of 1 µF or less and should be placed as close as possible to where it crosses the plane.

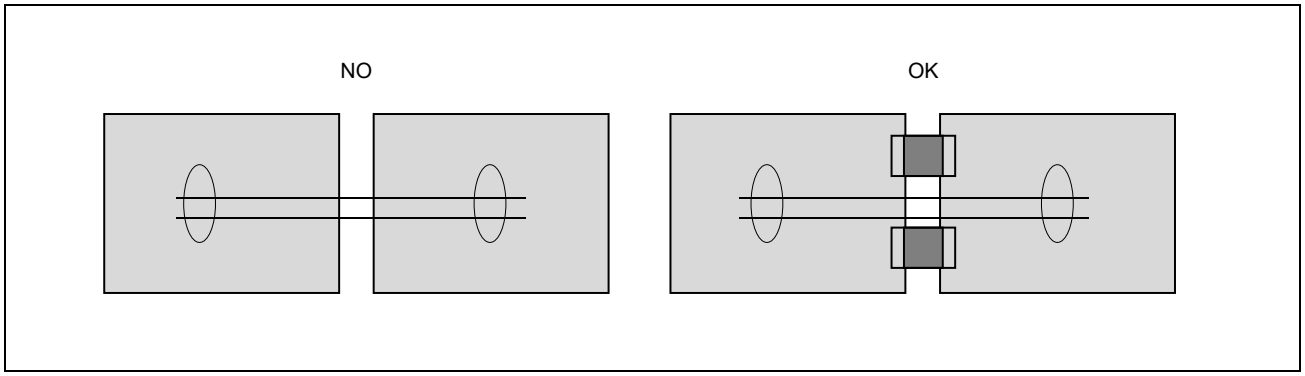

Figure C.2 Crossing Different GNDs

Wire Length Matching

Differential signals should be wired equally. To eliminate differential noise, match at the end of the line, not at the start point. The wire lengths of different differential signals do not need to match.

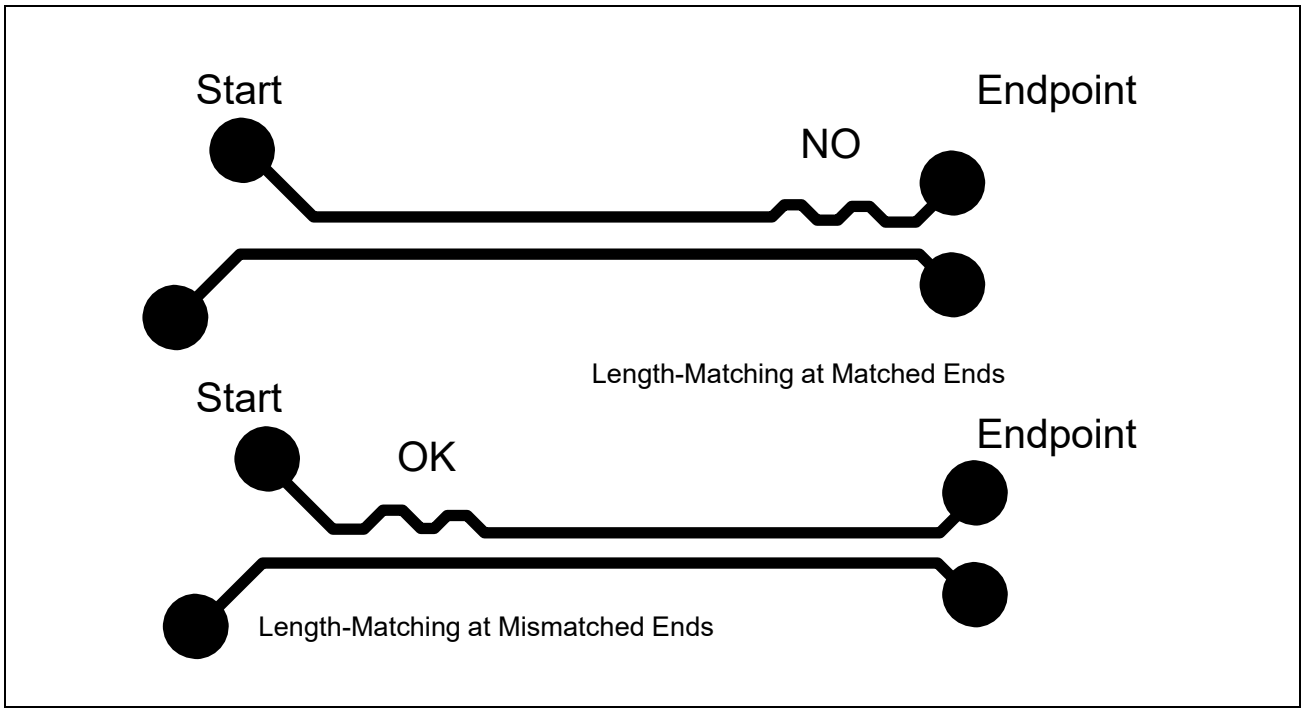

Figure C.3 Wire Length Matching

Differential Signal

Differential signals should be routed parallel and symmetrical.

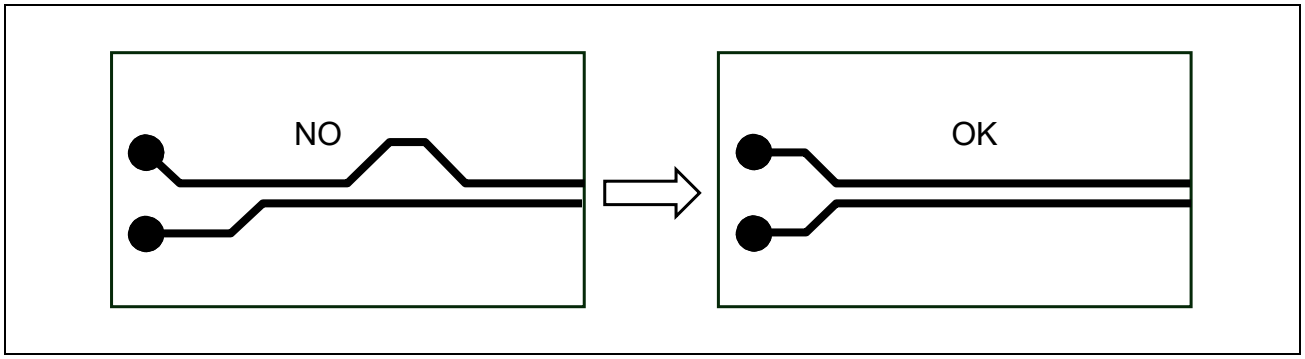

Figure C.4 Parallel and Symmetrical Trace

Do not place any components or vias between differential signals.

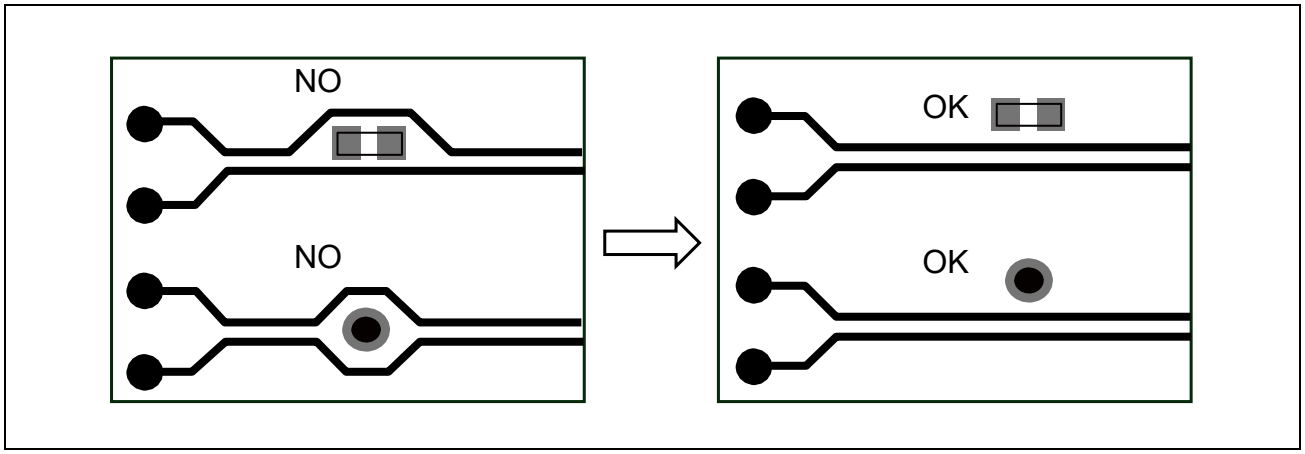

Figure C.5 Components between the Traces

The vias should be symmetrical.

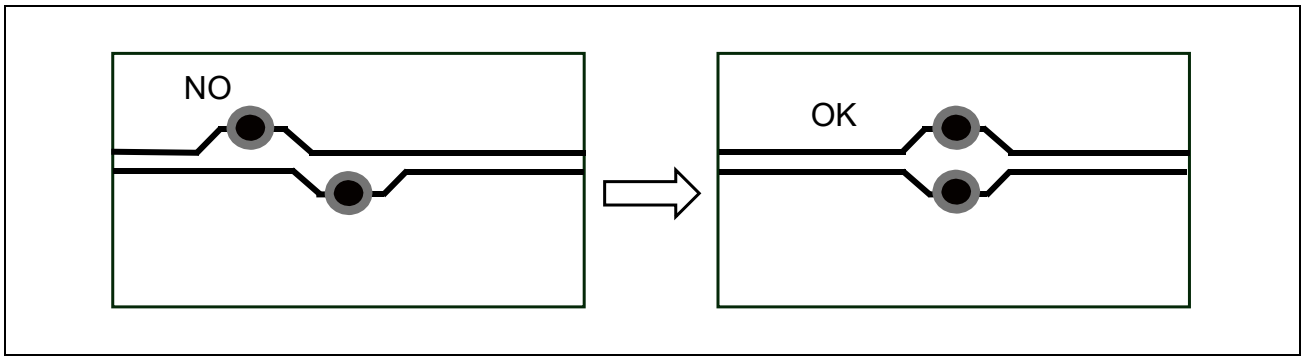

Figure C.6 Symmetrical Vias on the Traces

Differential signals should be routed at the same layer and with the same number of vias.

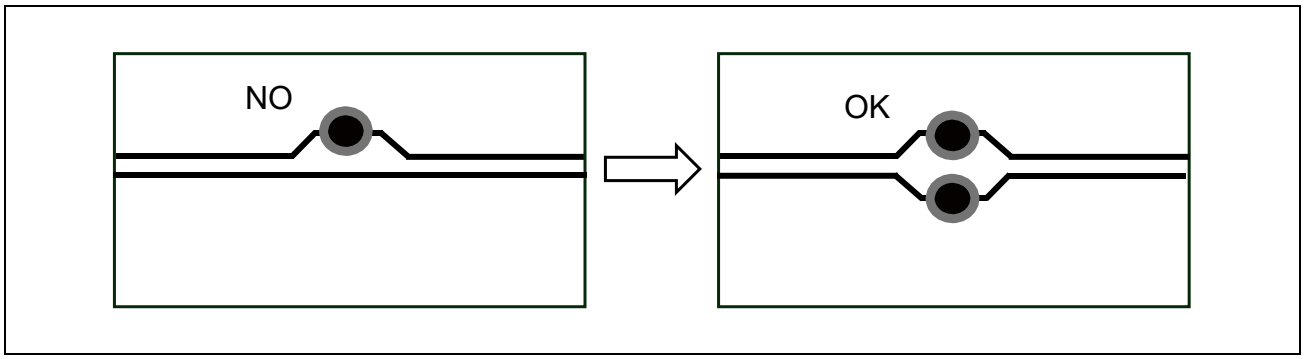

Figure C.7 Same Number of the Vias

The coupling capacitors should be placed symmetrically.

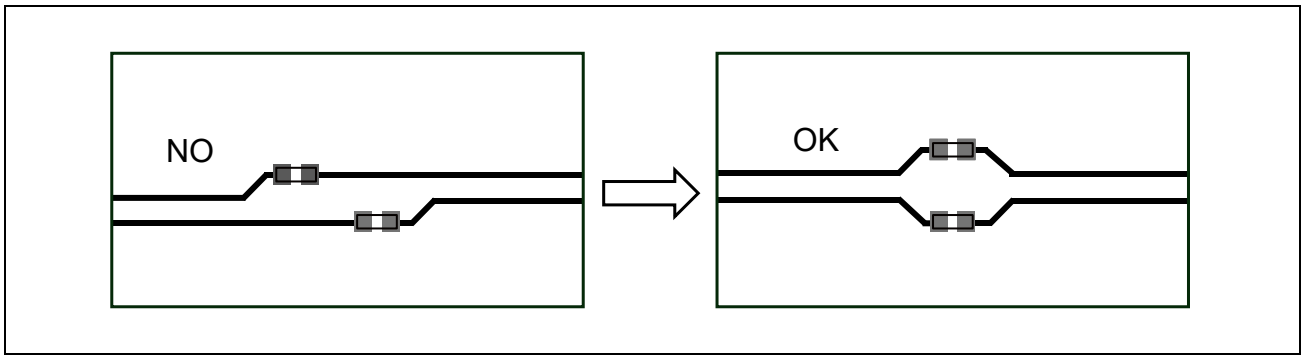

Figure C.8 Symmetrical Placement of Capacitors

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