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RENESAS

User's Manual

Multimedia Processor for Mobile Applications

Terrestrial Digital TV Interface

EMMA Mobile™1

Document No. S19267EJ4V0UM00 (4th edition)
Date Published October 2009

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Printed in Japan

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E0904E

PREFACE

Readers

This manual is intended for hardware/software application system designers who wish to understand and use the terrestrial digital TV interface functions of EMMA Mobile1 (EM1), a multimedia processor for mobile applications.

Purpose

This manual is intended to explain to users the hardware and software functions of the terrestrial digital TV interface of EM1, and be used as a reference material for developing hardware and software for systems that use EM1.

Organization

This manual consists of the following chapters.

- Chapter 1 Overview
- Chapter 2 Pin functions
- Chapter 3 DTV details
- Chapter 4 DTV2 datails

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, and microcontrollers.

To understand the functions of the terrestrial digital TV interface of EM1 in detail
→ Read this manual according to the **CONTENTS**.

To understand the other functions of EM1
→ Refer to the user's manual of the respective module.

To understand the electrical specifications of EM1
→ Refer to the Data Sheet.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Data type:	Word … 32 bits
	Halfword … 16 bits
	Byte … 8 bits

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document No.
MC-10118A Data sheet		S19657E
μ PD77630A Data sheet		S19686E
User's manual	Audio/Voice and PWM Interfaces	S19253E
	DDR SDRAM Interface	S19254E
	DMA Controller	S19255E
	I^2C Interface	S19256E
	ITU-R BT.656 Interface	S19257E
	LCD Controller	S19258E
	MICROWIRE	S19259E
	NAND Flash Interface	S19260E
	SPI	S19261E
	UART Interface	S19262E
	Image Composer	S19263E
	Image Processor Unit	S19264E
	System Control/General-Purpose I/O Interface	S19265E
	Timer	S19266E
	Terrestrial Digital TV Interface	This manual
	Camera Interface	S19285E
	USB Interface	S19359E
	SD Memory Card Interface	S19361E
	PDMA	S19373E
	One Chip (MC-10118A)	S19268E
	One Chip (μ PD77630A)	S19687E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

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CHAPTER 1 OVERVIEW

1.1 General

The terrestrial digital television interface (DTV interface) has a function to transfer stream data sent from an externally connected terrestrial digital TV channel decoder LSI to memory, via DMA. The DTV interface only supports burst output (serial) mode.

1.2 Features

The main features of DTV are as follows.
The DTV interface only supports serial output.

○ DTV interface signals
- DTV_DATA[7] is used in the serial output mode.
- Packet synchronization pulse (DTV_PSYNC)
- Stream data enable signal (DTV_VLD)
- Bus clock (DTV_BCLK)

○ DMA transfer destination buffer
- A ring buffer area can be specified.

○ Reception data selection
- Whether to receive parity fields can be selected.

○ Buffer memory
- A buffer memory of 32 bits × 4 words is incorporated.

1.3 Module Structure (DTV and DTV2)

EM1 has 2 of DTV macro (DTV2 function module (in the following, DTV2) and DTV function module (in the following, DTV)). A circuit and a register of each module are separate perfectly. The register address is common. A mutual function module is sharing OFDM interface and AHB bus interface. The main features of DTV are as follows.

Exclusion moves by setting of DTV/DTV2 change register SWITCH for each module. When 1 is set as DT_SWITCH, DTV2 is chosen, and when 0 is established, DTV is chosen. Defaults are DT_SWITCH=0, and DTV will be in the chosen state.

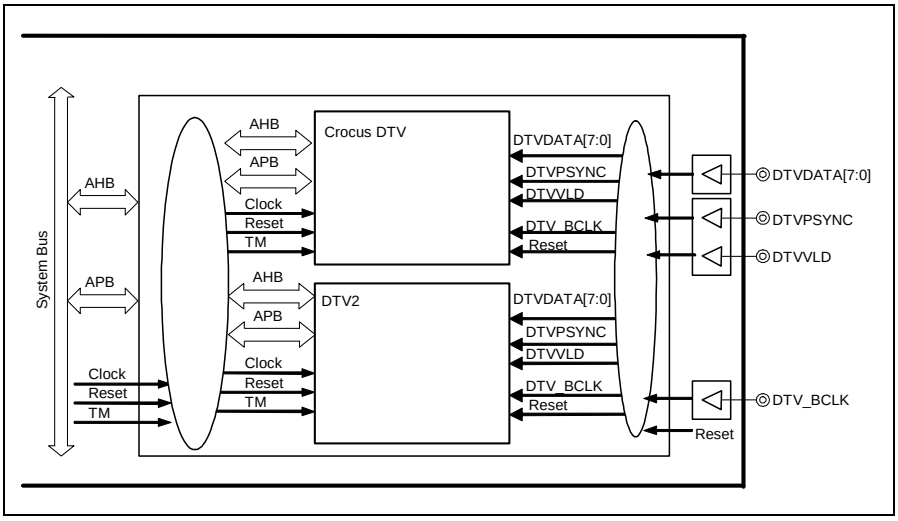


Figure 1-1. Block diagram

1.4 Clock Supply

All clocks are supplied only the function module chosen by DTV / DTV2 change register DT_SWITCH with. It isn't supplied non-selection function module with.

1.5 Reset / Reset release

All resets are reflected by only the function module chosen by DTV / DTV2 change register DT_SWITCH. Non-choice module will be always in the reset state.

Next to DTV / DTV2 change register DT_SWITCH=0 and DTV become effective just after the hardware reset. After reset release, it's necessary to establish DTV / DTV2 change register DT_SWITCH=1 to make DTV2 effective.

1.6 At the timing of DTV / DTV2 change

When changing DTV / DTV2, be sure to change by the following procedure.

1. H/W reset
2. H/W reset release
3. DT_SWITCH setting

CHAPTER 2 PIN FUNCTIONS

2.1 Terrestrial Digital TV Interface Pins

Pin Name	I/O	After Reset	Function	Alternate Pin Function
DTV_BCLK	Input	–	Data clock	SP2_CLK
DTV_DATA	Input	–	YUV data	SP2_SI
DTV_PSYNC	Input	–	Packet synchronization signal	SP2_SO
DTV_VLD	Input	–	Packet data enable	SP2_CS0

1

CHAPTER 3 DTV Details

3.1 Function Block Diagram

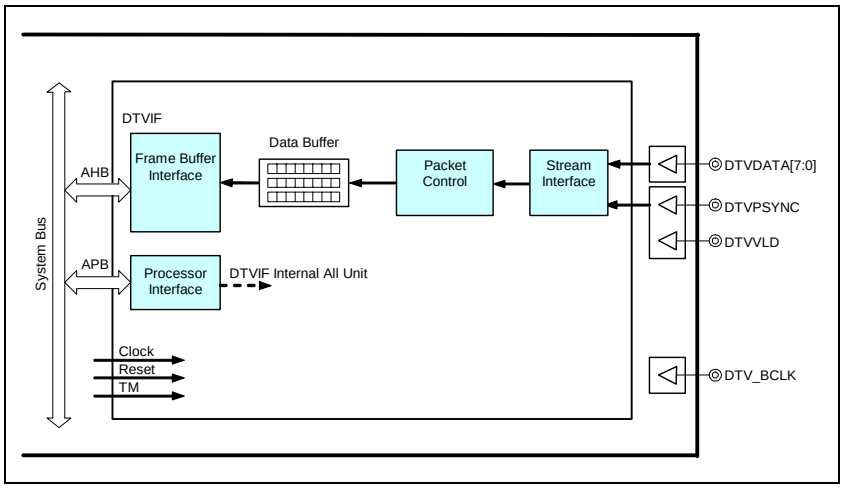


Figure 3-1. DTV Block diagram

3.2 Registers

Do not access reserved registers.

Any value written to reserved bits in each register is ignored.

Base address: 4015_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0020H	DTV / DTV2 change register	DT_SWITCH	R/W	0000_0000H

DTV/DTV2 change register DT_SWITCH=0 can use following register.

4015_0000H to 4015_0040H overlaps DTV2 , but at DT_SWITCH=0, register operation is reflected by only a DTV register.

Base address: 4015_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Interface status register	DT_STATUS	R	0000_0000H
0004H	Interface raw status register	DT_RAWSTATUS	R	0000_0000H
0008H	Interrupt enable set register	DT_ENSET	R/W	0000_0000H
000CH	Interrupt enable clear register	DT_ENCLR	W	0000_0000H
0010H	Interrupt source clear register	DT_FFCLR	W	0000_0000H
0014H	Error address register	DT_ERRORADR	R/W	0000_0000H
0020H	Transfer control register	DT_DMACNT	R/W	0000_0003H
0024H	Transfer request register	DT_DMAREQ	R/W	0000_0000H
0028H	Transfer request cancellation register	DT_DMASTOP	W	0000_0000H
002CH	Start address register	DT_START	R/W	0000_0000H
0030H	Buffer size register	DT_BUFSIZE	R/W	0000_0000H
0034H	Blank size register	DT_BLANK	R/W	0000_0000H
0038H	Current packet register	DT_CURRENT	R	0000_0000H
003CH	DMA completion interrupt setting register	DT_INTCONT	R/W	0000_0000H
0040H	Module control register	DT_MODULECONT	R/W	0000_0000H

3.3 Register Functions

3.3.1 DTV / DTV2 change register

This register (DT_SWITCH:4015_0200H) changes DTV and DTV2 exclusively.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							SWITCH

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
SWITCH	R/W	0	0	DTV / DTV2 change 0 : DTV 1 : DTV2

3.3.2 Interface status register

This read-only register (DT_STATUS: 4015_0000H) can be used to read the status of the interrupt sources enabled by the interrupt enable set register (DT_ENSET).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				DTVSTOP	DTVOR	DTVDMA	DMAERR

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0	Reserved. Don't write in anything but 0. It's prohibited to write in 1.
DTVSTOP	R	3	0	Indicates the status of the DMA stop interrupt. This interrupt is issued when DMA stops.

DTVOR	R	2	0	Indicates the status of the packet overrun error interrupt. This interrupt is issued when the internal buffer overruns.
DTVDMA	R	1	0	Indicates the status of the DMA completion interrupt. This interrupt is issued every time the number of packets specified in the DMA completion interrupt setting register (4015_003CH) have been transferred via DMA.
DMAERR	R	0	0	Indicates the status of the transfer error interrupt. This interrupt is issued when an error response is received during internal bus transfer. This interrupt is issued upon a prohibited operation such as writing to the transfer-prohibited area.

3.3.3 Interface raw status register

This read-only register (DT_RAWSTATUS: 4015_0004H) can be used to read the status of the interrupt sources, regardless of the setting of the interrupt enable set register (DT_ENSET).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				DTVSTOPRAW	DTVORRAW	DTVDMARAW	DMAERRRAW

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0	Reserved. Don't write in anything but 0. It's prohibited to write in 1.
DTVSTOP RAW	R	3	0	Indicates the status of the DMA stop interrupt. This interrupt is issued when DMA stops.
DTVORRAW	R	2	0	Indicates the status of the packet overrun error interrupt. This interrupt is issued when the internal buffer overruns.
DTVDMA RAW	R	1	0	Indicates the status of the DMA completion interrupt. This interrupt is issued every time the number of packets specified in the DMA completion interrupt setting register (4015_003CH) have been transferred via DMA.
DMAERR RAW	R	0	0	Indicates the status of the transfer error interrupt. This interrupt is issued when an error response is received during internal bus transfer. This interrupt is issued upon a prohibited operation such as writing to the transfer-protected area.

3.3.4 Interrupt enable set register

This register (DT_ENSET: 4015_0008H) enables issuance of interrupt requests. When the bit corresponding to an interrupt source is set to 1 in this register, if the interrupt source is set, an interrupt request is issued and the corresponding bit of the interrupt status register (DT_STATUS) is set to 1. Writing 0 to this register does not affect the setting. The interrupt request issuance enable status can be checked by reading this register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				DTVSTOP_EN	DTVOR_EN	DTVDMA_EN	DMAERR_EN

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0	Reserved. Don't write in anything but 0. It's prohibited to write in 1.
DTVSTOP_EN	R	3	0	Indicates whether issuance of DMA stop interrupt requests is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance of DMA stop interrupt requests. 1: Cancels interrupt masking.
DTVOR_EN	R	2	0	Indicates whether issuance of packet overrun error interrupt requests is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance packet overrun error interrupt requests. 1: Cancels interrupt masking.
DTVDMA_EN	R	1	0	Indicates whether issuance of DMA completion interrupt requests is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance of DMA completion interrupt requests. 1: Cancels interrupt masking.
DMAERR_EN	R	0	0	Indicates whether issuance of transfer error interrupt requests is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance of transfer error interrupt requests. 1: Cancels interrupt masking.

3.3.5 Interrupt enable clear register

This register (DT_ENCLR: 4015_000CH) disables issuance of interrupt requests. When the bit corresponding to an interrupt source is set to 1 in this register, an interrupt request is not issued even if an interrupt source occurs. The status of the corresponding bit of the interrupt status register (DT_STATUS) also remains unchanged. Writing 0 to this register does not affect the setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				DTVSTOPMASK	DTVORMASK	DTVDMAMASK	DMAERRMASK

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0	Reserved. Don't write in anything but 0. It's prohibited to write in 1.
DTVSTOP MASK	W	3	0	Disables issuance of DMA stop interrupt requests. 1: Disable
DTVOR MASK	W	2	0	Disables issuance of packet overrun error interrupt requests. 1: Disable
DTVDMA MASK	W	1	0	Disables issuance of DMA completion interrupt requests. 1: Disable
DMAERR MASK	W	0	0	Disables issuance of transfer error requests. 1: Disable

3.3.6 Interrupt source clear register

This write-only register (DT_FFCLR: 4015_0010H) clears the interrupt source by setting the bit corresponding to the interrupt source to 1. Writing 0 to this register does not affect the setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

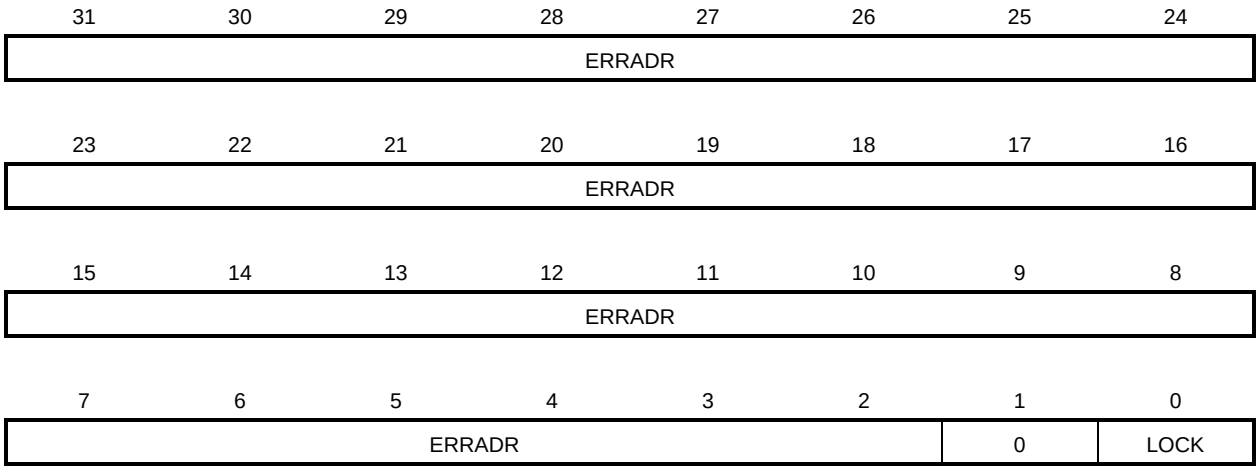
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				DTVSTOPCLR	DTVORCLR	DTVDMACLR	DMAERRCLR

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0	Reserved. Don't write in anything but 0. It's prohibited to write in 1.
DTVSTOPCLR	W	3	0	Clears the DMA stop interrupt source. 1: Clears the source.
DTVORCLR	W	2	0	Clears the packet overrun error interrupt source. 1: Clears the source.
DTVDMACLR	W	1	0	Clears the DMA completion interrupt source. 1: Clears the source.
DMAERRCLR	W	0	0	Clears the transfer error interrupt source. 1: Clears the source.

3.3.7 Error address register

This register (DT_ERRORADR: 4015_0014H) holds the current HADDR status when an internal bus response ERROR, RETRY or SPLIT is received during DMA transfer.



Name	R/W	Bit	After Reset	Function
ERRADR	R	31:2	0	Stores the HADDR status upon occurrence of an error response.
Reserved	R	1	0	Reserved. Don't write in anything but 0. It's prohibited to write in 1.
LOCK	R/W	0	0	Sets error status. 0: Stores the address when an error response occurs. 1: An error response occurred and the address was stored.

Caution If an error response occurs when the LOCK bit is 0, the current HADDR status is stored in the ERRADR bit and the LOCK bit is set to 1.
To acquire the error status again, set the LOCK bit to 0.
Writing 1 to the LOCK bit does not affect the setting.

3.3.8 Transfer control register

This register (DT_DMACNT: 4015_0020H) controls data transfer.

Settings can be changed only when DMA transfer is not being performed (DT_DMAREQ register = 0H).

The DTVSP bit must be set to 1 after activation.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved					DTVSP	DTVMODE	DTVENDIAN

Name	R/W	Bit	After Reset	Function
Reserved	R	31:3	0	Reserved. Don't write in anything but 0. It's prohibited to write in 1.
DTVSP	R/W	2	0	Specifies the data bus type of DTV stream. 0: Burst parallel output **(setting prohibited)** 1: Burst serial output
DTVMODE	R/W	1	1	Specifies the size of a packet. 0: Transfer of synchronization field + data field (188 bytes = 47 words) 1: Transfer of synchronization field + data field + parity field (204 bytes = 51 words)
DTVENDIAN	R/W	0	1	Specifies the DTV stream data format. 0: Big endian 1: Little endian

3.3.9 Transfer request register

This register (DT_DMAREQ: 4015_0024H) specifies the activation of DMA transfer.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							DMAREQ

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. Don't write in anything but 0. It's prohibited to write in 1.
DMAREQ	R	0	0	This bit is set to 1 when DMAREQ is acknowledged. This bit is cleared when the transfer request cancellation register (4015_0028H) is set.
	W		–	Writing 1 to this bit issues a DMA transfer request. DMA is repeated until the transfer request cancellation register (4015_0028H) is set. Writing 0 to this bit does not affect the setting.

Caution) Data transfer is begun from the start address at the time of a DMA transfer request.

3.3.10 Transfer request cancellation register

This register (DT_DMASTOP: 4015_0028H) stops DMA transfer. It'll be the stop reservation state by setting this register, and when not forwarding to the occasion during packet transfer after transfer, DMA is stopped immediately. The DMA transfer request status can be checked by reading the transfer request register (DT_DMAREQ). DMA stop interrupt is issued by the time of a fall of status (the lead value of the transfer request register).

This is a write-only register. If the register is set to 1, DMA transfer is finished. Writing 0 to this register does not affect the setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

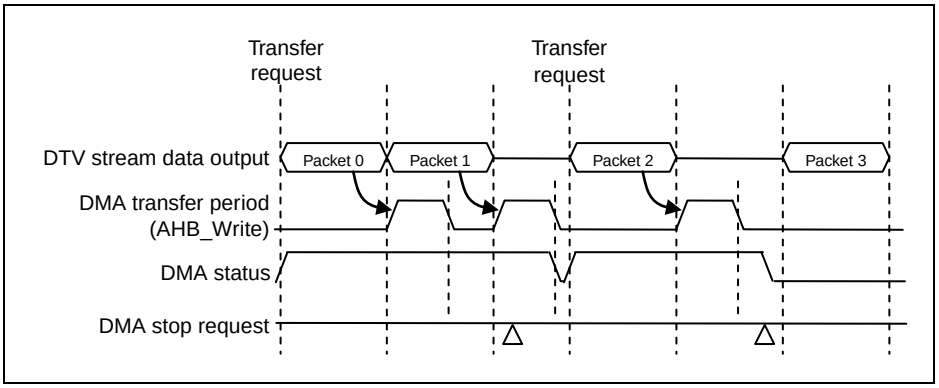
7	6	5	4	3	2	1	0
Reserved							DMASTOP

Name	R/W	Bit	After Reset	Function
Reserved	W	31:1	0	Reserved. Don't write in anything but 0. It's prohibited to write in 1.
DMASTOP	W	0	0	Stops DMA transfer. 1: Transfer stop When DMA transfer is being performed, the transfer stops after sending the current packet. Otherwise, the transfer immediately stops

Caution1) That one for 10 cycles of DTVBCLK leave a space by the (transfer request register set) which resumes DMA after DMA stop interruption.

Caution2) By DMA stop request fixation time, the effective data length, that, even packet data is forwarded to a memory. The data of the buffering way I don't have filled in the effective data length is broken.

Figure 3-2. DMA Stop Timing



3.3.11 Start address register

This register (DT_START: 4015_002CH) specifies the start address of the DMA transfer destination.

Settings can be changed only when DMA transfer is not being performed (DT_DMAREQ register = 0H).

31	30	29	28	27	26	25	24
DTV_START							

23	22	21	20	19	18	17	16
DTV_START							

15	14	13	12	11	10	9	8
DTV_START							

7	6	5	4	3	2	1	0
DTV_START						0	0

Name	R/W	Bit	After Reset	Function
DTV_START	R/W	31:0	0	Specifies the start address of the DMA transfer destination (the lower 2 bits are fixed to 0).

3.3.12 Buffer size register

This register (DT_BUFSIZE: 4015_0030H) specifies the size of the DMA transfer destination area in units of packets.

Settings can be changed only when DMA transfer is not being performed (DT_DMAREQ register = 0H).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved				DTV_BUFSIZE			

15	14	13	12	11	10	9	8
DTV_BUFSIZE							

7	6	5	4	3	2	1	0
DTV_BUFSIZE						0	0

Name	R/W	Bit	After Reset	Function
Reserved	R	31:20	0	Reserved. Don't write in anything but 0. It's prohibited to write in 1.
DTV_ BUFSIZE	R/W	19:0	0	Specifies the size of the DMA transfer destination area in units of packets (the lower 2 bits are fixed to 0).

3.3.13 Blank size register

This register (DT_BLANK: 4015_0034H) specifies the blank size between packets during DMA transfer.

Settings can be changed only when DMA transfer is not being performed (DT_DMAREQ register = 0H).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
DTV_BLANK						0	0

Name	R/W	Bit	After Reset	Function
Reserved	R	31:8	0	Reserved. Don't write in anything but 0. It's prohibited to write in 1.
DTV_BLANK	R/W	7:0	0	Specifies the blank size between packets (the lower 2 bits must be set to 0).

3.3.14 Current packet register

This register (DT_CURRENT: 4015_0038H) indicates the number of packets that have been transferred via DMA.

This register shows the value from 0 to “DT_BUFSIZE register value − 1”.

Settings can be changed only when DMA transfer is not being performed (DT_DMAREQ register = 0H).

31	30	29	28	27	26	25	24
Reserved							

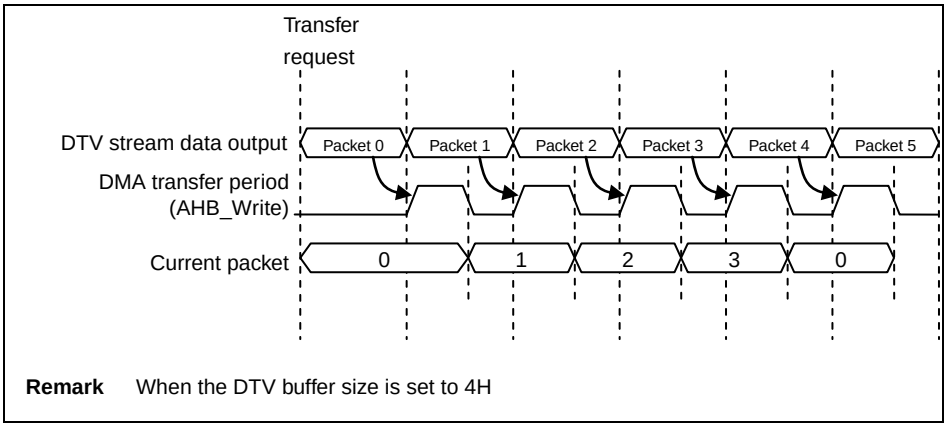
23	22	21	20	19	18	17	16
Reserved				DTV_CURRENT			

15	14	13	12	11	10	9	8
DTV_CURRENT							

7	6	5	4	3	2	1	0
DTV_CURRENT							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:20	0	Reserved. Don't write in anything but 0. It's prohibited to write in 1.
DTV_ CURRENT	R	19:0	0	Stores the number of packets that have been transferred via DMA minus 1.

Figure 3-2. Current Packet Register Values



Remark When the DTV buffer size is set to 4H

Caution) Only while the count value is DT_DMAREQ=1, the count value is effective. While it's DT_DMAREQ=0, it'll be 0.

3.3.15 DMA completion interrupt setting register

This register (DT_INTCONT: 4015_003CH) specifies the interval at which a DMA transfer completion interrupt is issued, in units of packets. A DMA transfer completion interrupt is issued each time DMA transfer of “DT_INTCONT register value + 1” packets is completed.

Settings can be changed only when DMA transfer is not being performed (DT_DMAREQ register = 0H).

31	30	29	28	27	26	25	24
Reserved							

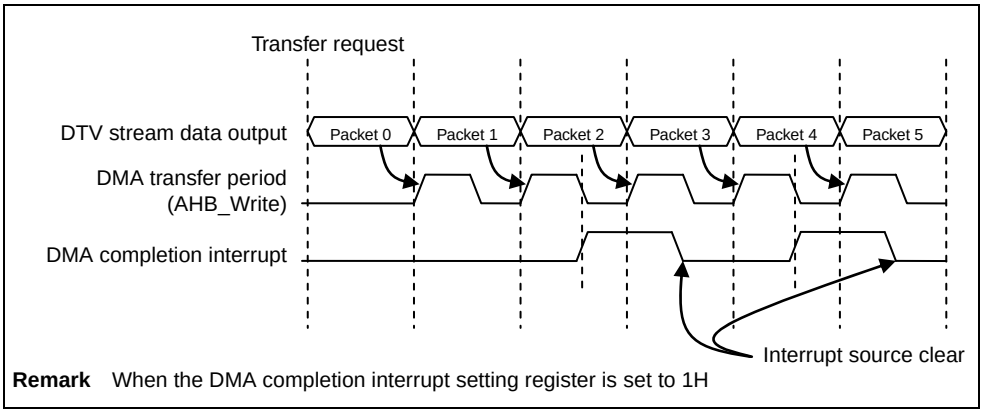
23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
DTV_INTCONT							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:8	0	Reserved. Don't write in anything but 0. It's prohibited to write in 1.
DTV_ INTCONT	R/W	7:0	0	Specifies in units of packets the interval at which a DMA transfer completion interrupt is issued. An interrupt is issued every time the number of packets equal to the set value plus 1 are received.

Figure 3-4. DTV Interface DMA Completion Interrupt Set Timing



Remark When the DMA completion interrupt setting register is set to 1H

3.3.16 Module control register

This register (DT_MODULECONT: 4015_0040H) initializes the operation of the data capturing circuit that synchronizes with DTV_BCLK.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							HW_RSTZ

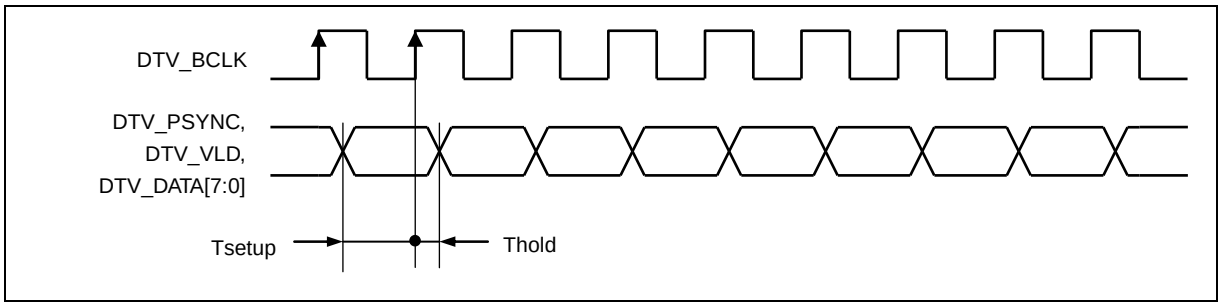
Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. Don't write in anything but 0. It's prohibited to write in 1.
HW_RSTZ	R/W	0	0	Specifies hardware reset. Specifies whether to initialize the operation of the data capturing circuit that synchronizes with DTV_BCLK. 0: Reset 1: Cancels reset

3.4 Function details

3.4.1 Input Signal Timing

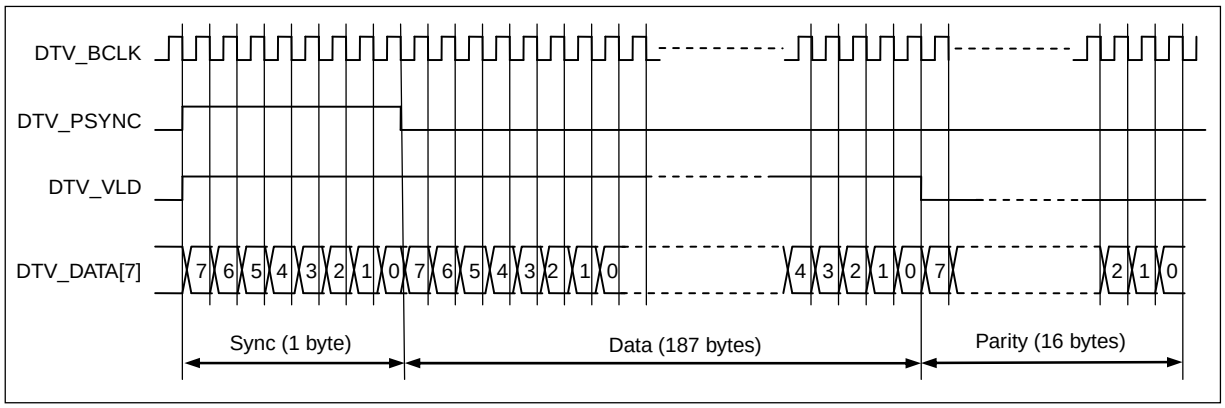
(1) DTV I/F signal timing

Figure 3-5. DTV Interface Signal Timing



(2) Stream timing

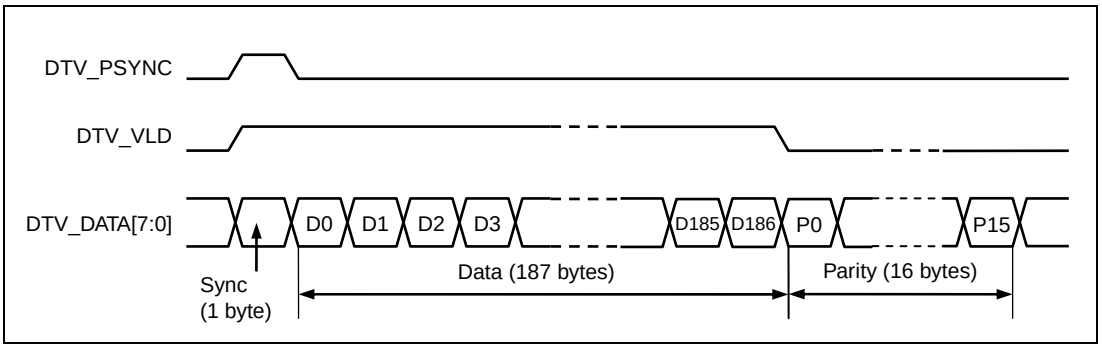
Figure 3-6. Stream Timing (Burst Serial Output)



Caution When reception of the parity field is selected, a blanking interval of at least 2T DTV_BCLK cycles must be inserted between packets.

3.4.2 Data Format

Figure 3-7. Stream Data Storage Format



Data input as shown in Figure 3-7 is stored in the memory in the following format, in accordance with the value set to the DTVENDIAN bit of the transfer control register (DT_DMACNT).

Bit alignment	31 to 24	23 to 16	15 to 8	7 to 0
50 words	P15	P14	P13	P12
49 words	P11	P10	P9	P8
48 words	P7	P6	P5	P4
47 words	P3	P2	P1	P0
46 words	D186	D185	D184	D183
	:	:	:	:
3 words	D14	D13	D12	D11
2 words	D10	D9	D8	D7
1 word	D6	D5	D4	D3
0 words	D2	D1	D0	Sync

Little endian

31 to 24	23 to 16	15 to 8	7 to 0
P14	P15	P12	P13
P10	P11	P8	P9
P6	P7	P4	P5
P2	P3	P0	P1
D185	D186	D183	D184
:	:	:	:
D13	D14	D11	D12
D9	D10	D7	D8
D5	D6	D3	D4
D1	D2	Sync	D0

Big endian

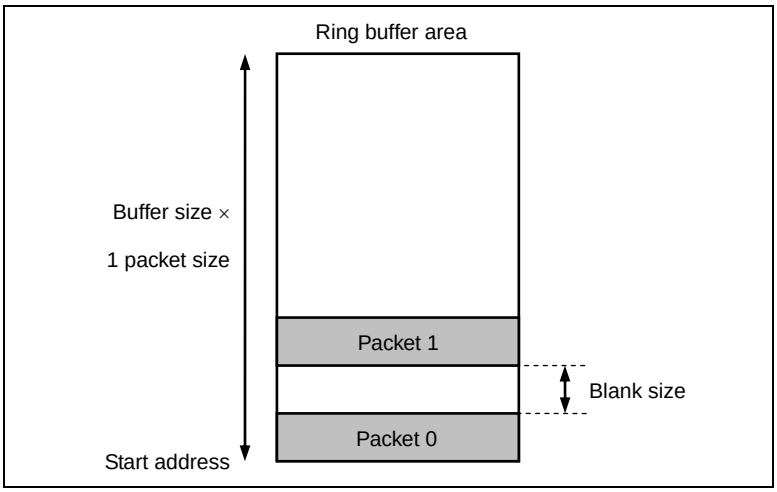
3.4.3 DTV Transfer Processing

Stream data is transferred to the specified buffer area in the memory, in units of packets. The buffer is used as a ring buffer in which the pointer returns to the beginning of the buffer after the specified number of packets are stored.

The following three registers are used to set up the buffer.

- Start address register (32 bits): Specifies the ring buffer start address.
- Buffer size register (20 bits): Specifies the ring buffer area by a packet count.
- Blank size register (8 bits): Specifies the blanking interval between packets.

Figure 3-8. Ring Buffer Mapping



The valid size of a packet can be set to 188 or 204 bytes by using the DTVMODE bit of the transfer control register (DT_DMACNT).

The size of a packet to be mapped to a buffer is the valid size selected by the DTVMODE bit plus the blank size. The total ring buffer size is the above packet size multiplied by the buffer size.

3.4.4 Interrupt Control

The DTV interface uses four interrupts. The bits of the interrupt status register (DT_STATUS) are used to control the interrupts. For details, see Table 3-1.

Table 3-1. Interrupt Sources

Interrupt Type	When to Issue	Bit Assignment
DMA stop interrupt	Issued when the DMA transfer stops.	Bit 3 (DTVSTOP)
Packet overrun	Issued when the internal buffer overruns.	Bit 2 (DTVOR)
DMA completion interrupt	Issued when the specified number of packets have been transferred.	Bit 1 (DTVDMA)
Transfer error interrupt	Issued when the ERROR response is received during internal bus transfer.	Bit 0 (DMAERR)

(1) Transfer error interrupt

When a ERROR reply is received during Internal bus transfer, interrupt is generated.

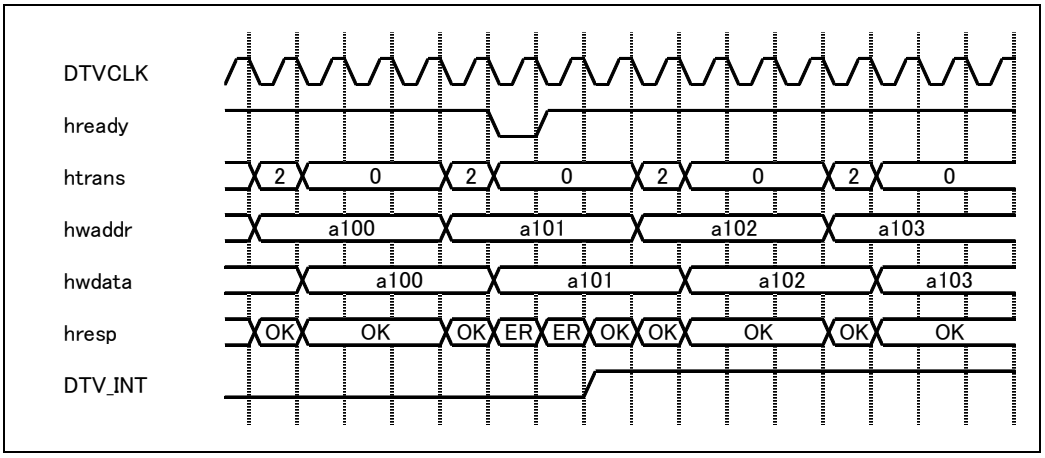


Figure 3-9. Transfer error interrupt timing

(2) DMA completion interrupt

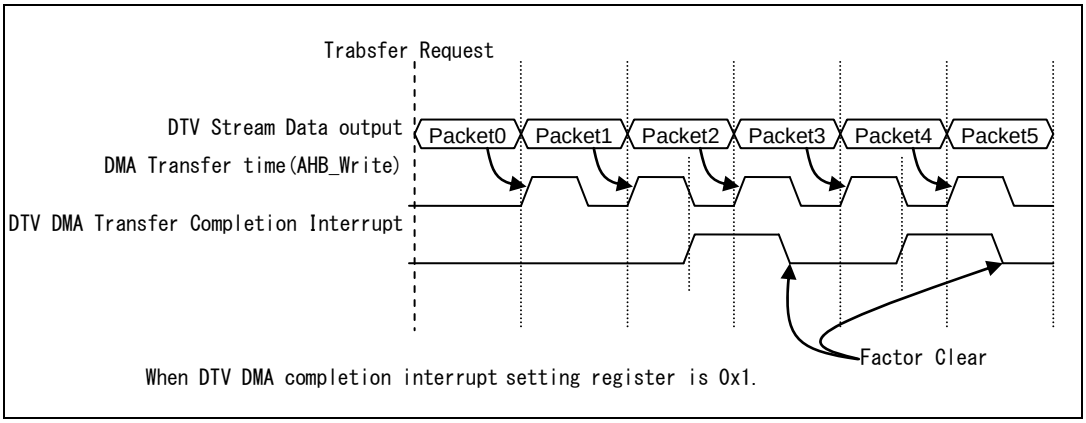


Figure 3-10. DMA completion interrupt Timing

(3) Packet overrun interrupt

The DTV interface uses internal memory (32 bits × 128 words) as a buffer having two banks. Banks are switched for each packet for buffering and the data in the filled bank is transferred to the memory via DMA.

In stream data transfer via the DTV interface, the case where the DMA transfer of the previous packet data is not completed within the period in which a packet is loaded is defined as a packet overrun. If a packet overrun occurs, the corresponding bit of the interrupt source register is immediately set.

If a packet overrun occurs, packet data input via the channel decoder LSI and data stored in the ring buffer becomes inconsistent. In such a case, terminate DMA once, reserve a sufficient band for the internal bus, and then load data again.

(4) DMA stop interrupt

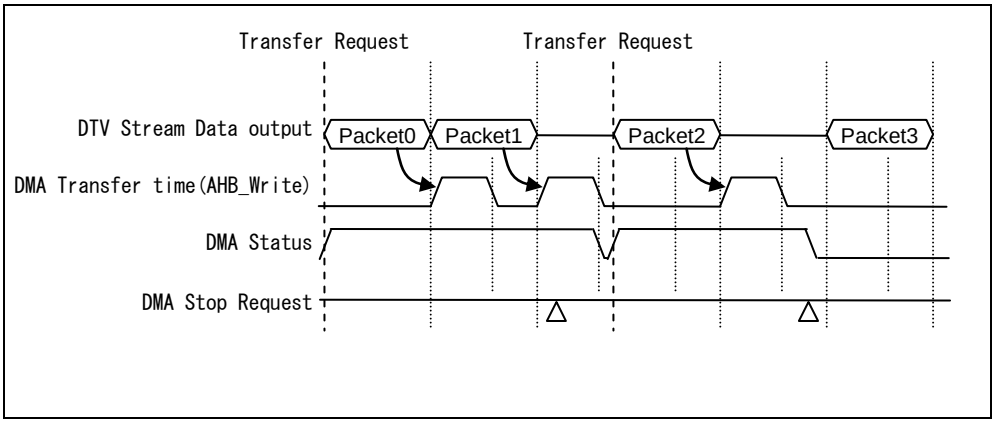


Figure 3-11. DMA stop interrupt Timing

Caution : Leave the space for 10 cycles of DTVBCLK by the (transfer request register set) which resumes DMA after DMA stop interruption.

3.4.5 Clocks Control

In EM1, supply of the internal bus clock is controlled by each module to save power.

The internal bus clock is supplied upon requests from modules and upon register access.

In the DTV interface, a clock supply request is set when a DMA transfer is requested through register access, and the clock supply request is cleared when transfer of the current DMA is completed with no other transfers requested.

(1) Clocks used in DTV interface

(a) DTV_BCLK (external input clock)
Used for capturing the DTV data clock and data.

(b) DTV_CLK (DTV internal clock)
Used for the AHB bus clock and the internal operation of the DTV interface.

(c) DTV_PCLK (APB clock)
Used for the accessing the APB bus (registers).

For details about clock/reset settings, see the **Multimedia Processor for Mobile Applications - System Control/General-Purpose I/O Interface User's Manual (S19265E)**.

(2) DTV_CLKREQ set timing

When the DTV transfer request register is set.

(3) DTV_CLKREQ clear timing

When the DTV transfer request cancellation register is set and DMA transfer of the current packet is completed.

(4) DTV_SWT_CLKREQ output timing

The signal 1CLK preceded to transaction is output as CLKREQ for bus switches.

Signal rising is 1CLK precedence of transaction, and a fall is at the timing of an end of the data phase.

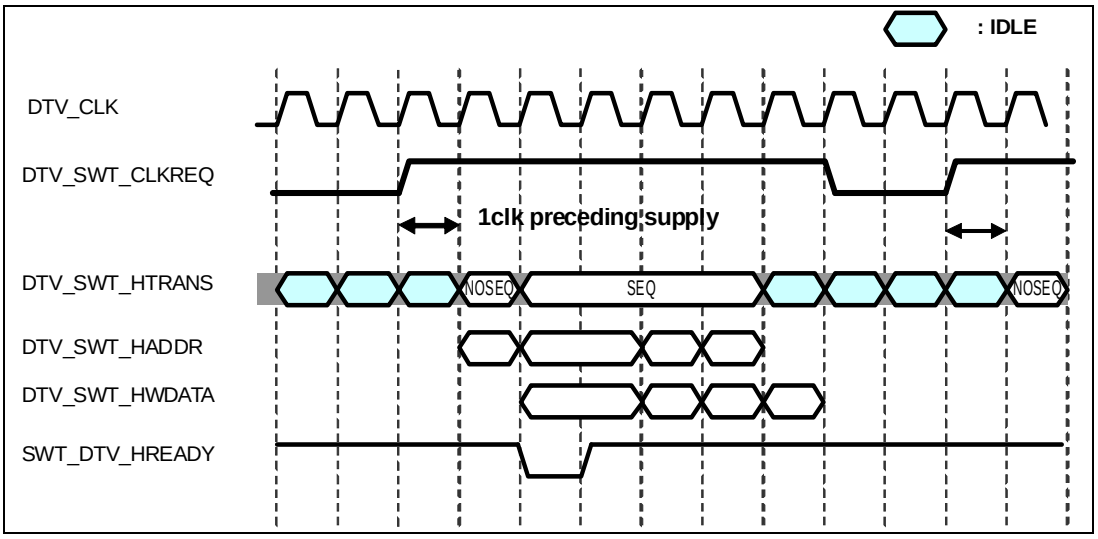


Figure 3-12. DMA_SWT_CLKREQ Timing

(5) Clock restriction

DTV_3 clocks of CLK is need to 32 clocks of DTVBCLK for a data delivery between the external clock and the internal clock.

32 / DTVBCLK ＞ 3 / DTV_CLK

DTV_CLK ＞ 0.093*DTVBCLK

Caution : Even when a clock stop period occurs in clock changes, convert it into a frequency and judge normal movement pros and cons.

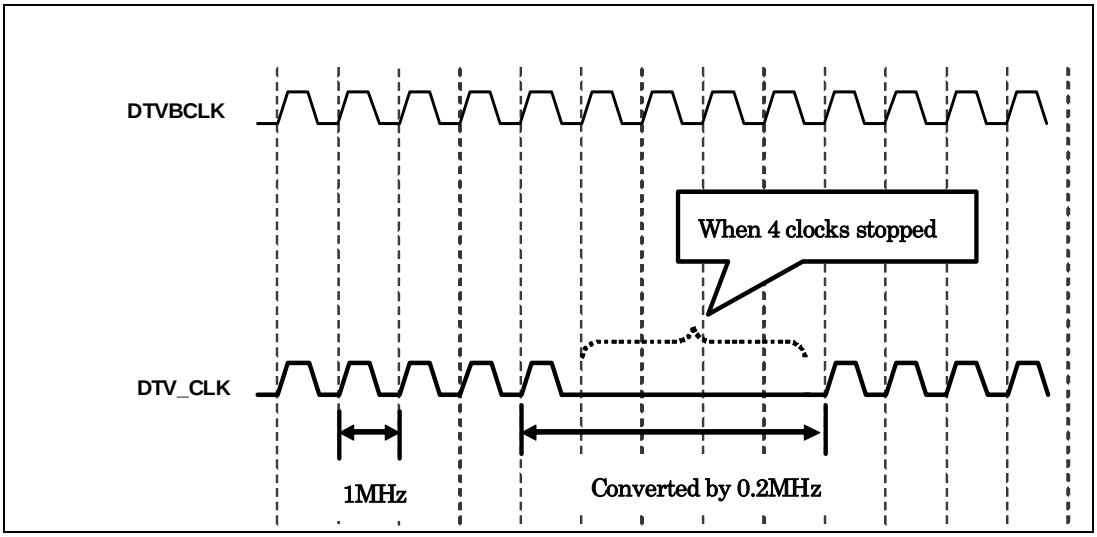


Figure 3-13. Frequency conversion of DTV_CLK and DTVBCLK

(6) Relation between DTVBCLK and input data

Supply is also necessary to DTVBCLK by the following case outside the effective data area.

(1) Before a head packet just after the DMA start (DMAREQ register) is input, it's needed beyond 5 clocks.

(2) It's needed between the packet beyond 10 clocks.

A clock in front of the head packet is for data fetch preparations, and a clock between the packet is necessary to take it in and deliver data to a AHB clock from DTVBCLK.

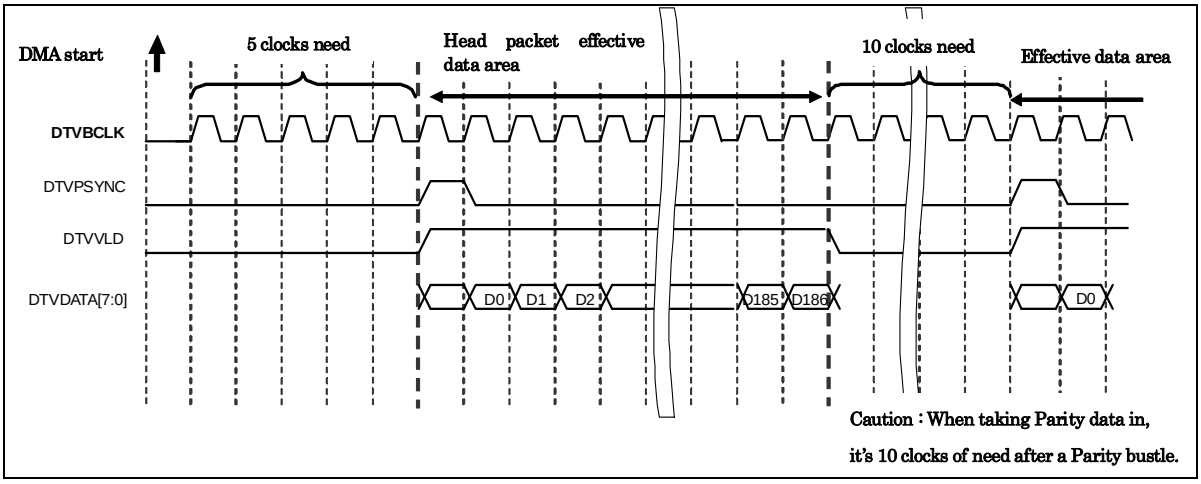


Figure 3-14. Relation between DTVBCLK and input data

3.4.6 Return method from synchronous difference

(1) The bit difference chosen at the timing of a start

When it's piled in a H period of DTVPSYNC input (between 8 clocks) at the timing of a DMA start (DMAREQ), a bit difference occurs to bustle data.

When a bit difference occurs, head packet data after a DMA start is forwarded by the data unit which isn't an original byte boundary. To evade that, head packet data after a DMA start check a Sync code, and please confirm that there are no bit differences. When it isn't a Sync code, a bit difference occurs, so please break packet data.

A bit difference is canceled automatically, and the next packet after a while is forwarded at a normal byte boundary.

(2) Return from a synchronous difference by prescritive outside input

When the case when a clock (DTVBCLK) isn't supplied right and at the timing of prescribed input did, and were different input such as noise occurred to a clock, a same year can't slip and sometimes forward data right.

It's possible to make them return from a synchronous difference by the next processing. Further, the data maintained in the circuit is broken.

(1) Head 1byte data of packet data is checked and a synchronous difference is judged.
(2) DMA transfer stop (DMASTOP register).
(3) The DMA stop interruption is confirmed.
(4) The DTV I/F is reset in HW of a MODULECONT register_RSTZ (note).
(5) The reset release which is the DTV I/F in HW of a MODULECONT register_RSTZ.
(6) Restart of DMA transfer (DMAREQ register).

Note : For HW_RSTZ to initialize only DTV_IF part (the circuit which moves in DTVBCLK), register setting is maintained. Register's readjustment isn't necessary.

CHAPTER 4 DTV2 Details

4.1 Function Block Diagram

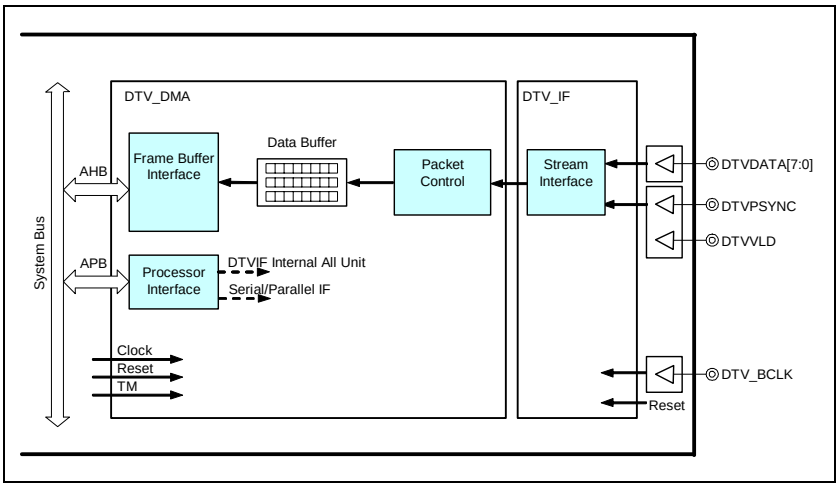


Figure 4-1. DTV Block diagram

4.2 Registers

Do not access reserved registers.

Any value written to reserved bits in each register is ignored.

Base address: 4015_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0020H	DTV / DTV2 change register	DT_SWITCH	R/W	0000_0000H

DTV/DTV2 change register DT_SWITCH=1 can use following register.

4015_0000H to 4015_0040H overlaps DTV2 , but at DT_SWITCH=1, register operation is reflected by only a DTV2 register.

Base address: 4015_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Interface status register	DT2_STATUS	R	0000_0000H
0004H	Interface raw status register	DT2_RAWSTATUS	R	0000_0000H
0008H	Interrupt enable set register	DT2_ENSET	R/W	0000_0000H
000CH	Interrupt enable clear register	DT2_ENCLR	W	0000_0000H
0010H	Interrupt source clear register	DT2_FFCLR	W	0000_0000H
0014H	Error address register	DT2_ERRORADR	R/W	0000_0000H
0020H	Transfer control register	DT2_DMACNT	R/W	0000_0003H
0024H	Transfer request register	DT2_DMAREQ	R/W	0000_0000H
0028H	Transfer request cancellation register	DT2_DMASTOP	W	0000_0000H
002CH	Start address register	DT2_START	R/W	0000_0000H
0030H	Buffer size register	DT2_BUFSIZE	R/W	0000_0000H
0034H	Blank size register	DT2_BLANK	R/W	0000_0000H
0038H	Current packet register	DT2_CURRENT	R	0000_0000H
003CH	DMA completion interrupt setting register	DT2_INTCONT	R/W	0000_0000H
0040H	Module control register	DT2_MODULECONT	R/W	0000_0000H
0044H	DTVPSYNC / DTVVLD Polarity designation register	DT2_SIGNALINVERT	R/W	0000_0000H
0048H	Input pin status monitor register	DT2_MONITOR	R	0000_0000H

4.3 Register Functions

4.3.1 DTV / DTV2 change register

This register (DT_SWITCH:4015_0200H) changes DTV and DTV2 exclusively.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							SWITCH

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
SWITCH	R/W	0	0	DTV / DTV2 change 0 : DTV 1 : DTV2

4.3.2 Interface status register

This read-only register (DT2_STATUS: 4015_0000H) can be used to read the status of the interrupt sources enabled by the interrupt enable set register (DT_ENSET).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	DTVLP	DTVSP	DTVSYNC	DTVSTOP	DTVOR	DTVDMA	DMAERR

Name	R/W	Bit	After Reset	Function
Reserved	R	31:7	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVLP	R	6	0	Indicates the status of the packet length excess. This interrupt is issued when 1 packet exceeded 188byte or 204byte, interrupt is generated.
DTVSP	R	5	0	Indicates the status of the packet length short. This interrupt is issued transfer data includes SyncByte and the transfer amount of the just before packet data generates interrupt in case of less than 187 bytes or less than 203 bytes.
DTVSYNC	R	4	0	Indicates the status of the illegal SyncByte. This interrupt is issued the value of SyncByte generates interrupt in case of 47H or anything but B8H.
DTVSTOP	R	3	0	Indicates the status of the DMA stop interrupt. This interrupt is issued when DMA stops.
DTVOR	R	2	0	Indicates the status of the packet overrun error interrupt. This interrupt is issued when the internal buffer overruns.
DTVDMA	R	1	0	Indicates the status of the DMA completion interrupt. This interrupt is issued every time the number of packets specified in the DMA completion interrupt setting register (4015_003CH) have been transferred via DMA.
DMAERR	R	0	0	Indicates the status of the transfer error interrupt. This interrupt is issued when an error response is received during internal bus transfer. This interrupt is issued upon a prohibited operation such as writing to the transfer-prohibited area.

4.3.3 Interface raw status register

This read-only register (DT2_RAWSTATUS: 4015_0004H) can be used to read the status of the interrupt sources, regardless of the setting of the interrupt enable set register (DT2_ENSET).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	DTVLPRAW	DTVSPRAW	DTVSYNCRAW	DTVSTOPRAW	DTVORRAW	DTVDMARAW	DMAERRRAW

Name	R/W	Bit	After Reset	Function
Reserved	R	31:7	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVLPRAW	R	6	0	Indicates the status of the packet length excess. This interrupt is issued when 1 packet exceeded 188byte or 204byte, interrupt is generated.
DTVSPRAW	R	5	0	Indicates the status of the packet length short. This interrupt is issued transfer data includes SyncByte and the transfer amount of the just before packet data generates interrupt in case of less than 187 bytes or less than 203 bytes.
DTVSYNCRAW	R	4	0	Indicates the status of the illegal SyncByte. This interrupt is issued the value of SyncByte generates interrupt in case of 47H or anything but B8H.
DTVSTOPRAW	R	3	0	Indicates the status of the DMA stop interrupt. This interrupt is issued when DMA stops.
DTVORRAW	R	2	0	Indicates the status of the packet overrun error interrupt. This interrupt is issued when the internal buffer overruns.
DTVDMARAW	R	1	0	Indicates the status of the DMA completion interrupt. This interrupt is issued every time the number of packets specified in the DMA completion interrupt setting register (4015_003CH) have been transferred via DMA.
DMAERRRAW	R	0	0	Indicates the status of the transfer error interrupt. This interrupt is issued when an error response is received during internal bus transfer. This interrupt is issued upon a prohibited operation such as writing to the transfer-protected area.

4.3.4 Interrupt enable set register

This register (DT2_ENSET: 4015_0008H) enables issuance of interrupt requests. When the bit corresponding to an interrupt source is set to 1 in this register, if the interrupt source is set, an interrupt request is issued and the corresponding bit of the interrupt status register (DT2_STATUS) is set to 1. Writing 0 to this register does not affect the setting. The interrupt request issuance enable status can be checked by reading this register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	DTVLP_EN	DTVSP_EN	DTVSYNC_EN	DTVSTOP_EN	DTVOR_EN	DTVDMA_EN	DMAERR_EN

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31:7	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVLP_EN	R	6	0	Indicates whether issuance of packet length excess interrupt request is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance of packet length excess interrupt requests. 1: Cancels interrupt masking.
DTVSP_EN	R	5	0	Indicates whether issuance of packet length short interrupt request is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance of packet length short interrupt requests. 1: Cancels interrupt masking.
DTVSYNC_EN	R	4	0	Indicates whether issuance of illegal SyncByte interrupt request is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance of illegal SyncByte interrupt requests. 1: Cancels interrupt masking.
DTVSTOP_EN	R	3	0	Indicates whether issuance of DMA stop interrupt requests is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance of DMA stop interrupt requests. 1: Cancels interrupt masking.
DTVOR_EN	R	2	0	Indicates whether issuance of packet overrun error interrupt requests is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance packet overrun error interrupt requests. 1: Cancels interrupt masking.

(2/2)

Name	R/W	Bit	After Reset	Function
DTVDMA_EN	R	1	0	Indicates whether issuance of DMA completion interrupt requests is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance of DMA completion interrupt requests. 1: Cancels interrupt masking.
DMAERR_EN	R	0	0	Indicates whether issuance of transfer error interrupt requests is enabled. 0: Not enabled. 1: Enabled.
	W			Specifies whether to enable issuance of transfer error interrupt requests. 1: Cancels interrupt masking.

4.3.5 Interrupt enable clear register

This register (DT2_ENCLR: 4015_000CH) disables issuance of interrupt requests. When the bit corresponding to an interrupt source is set to 1 in this register, an interrupt request is not issued even if an interrupt source occurs. The status of the corresponding bit of the interrupt status register (DT2_STATUS) also remains unchanged. Writing 0 to this register does not affect the setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	DTVLPMASK	DTVSPMASK	DTVSYNCMASK	DTVSTOPMASK	DTVORMASK	DTVDMAMASK	DMAERRMASK

Name	R/W	Bit	After Reset	Function
Reserved	R	31:7	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVLPMASK	W	6	0	Disables issuance of packet length excess interrupt requests. 1: Disable
DTVSPMASK	W	5	0	Disables issuance of packet length short interrupt requests. 1: Disable
DTVSYNCMASK	W	4	0	Disables issuance of illegal SyncByte interrupt requests. 1: Disable
DTVSTOPMASK	W	3	0	Disables issuance of DMA stop interrupt requests. 1: Disable
DTVORMASK	W	2	0	Disables issuance of packet overrun error interrupt requests. 1: Disable
DTVDMAMASK	W	1	0	Disables issuance of DMA completion interrupt requests. 1: Disable
DMAERRMASK	W	0	0	Disables issuance of transfer error requests. 1: Disable

4.3.6 Interrupt source clear register

This write-only register (DT2_FFCLR: 4015_0010H) clears the interrupt source by setting the bit corresponding to the interrupt source to 1. Writing 0 to this register does not affect the setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

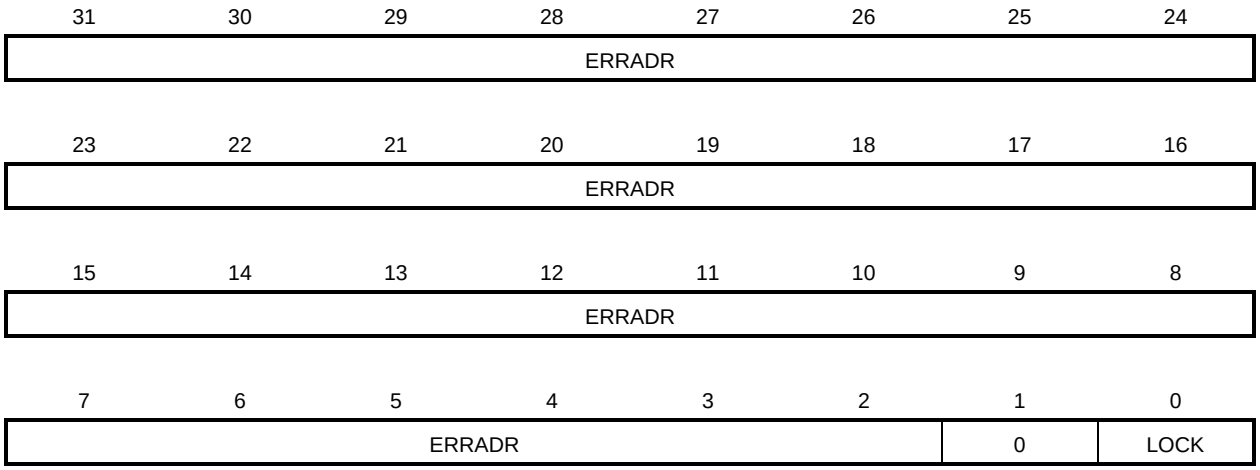
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	DTVLPCLR	DTVSPCLR	DTVSYNCCLR	DTVSTOPCLR	DTVORCLR	DTVDMACLR	DMAERRCLR

Name	R/W	Bit	After Reset	Function
Reserved	R	31:7	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVLPCLR	W	6	0	Clears the packet length excess interrupt source. 1: Clears the source.
DTVSPCLR	W	5	0	Clears the packet length short interrupt source. 1: Clears the source.
DTVSYNCCLR	W	4	0	Clears the illegal SyncByte interrupt source. 1: Clears the source.
DTVSTOPCLR	W	3	0	Clears the DMA stop interrupt source. 1: Clears the source.
DTVORCLR	W	2	0	Clears the packet overrun error interrupt source. 1: Clears the source.
DTVDMACLR	W	1	0	Clears the DMA completion interrupt source. 1: Clears the source.
DMAERRCLR	W	0	0	Clears the transfer error interrupt source. 1: Clears the source.

4.3.7 Error address register

This register (DT2_ERRORADR: 4015_0014H) holds the current HADDR status when an internal bus response ERROR, RETRY or SPLIT is received during DMA transfer.



Name	R/W	Bit	After Reset	Function
ERRADR	R	31:2	0	Stores the HADDR status upon occurrence of an error response.
Reserved	R	1	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
LOCK	R/	0	0	Sets error status. 0: Stores the address when an error response occurs. 1: An error response occurred and the address was stored.
	W			Clear error status. 0: Stores the address when an next error response occurs. 1: Nothing action.

Caution If an error response occurs when the LOCK bit is 0, the current HADDR status is stored in the ERRADR bit and the LOCK bit is set to 1.
To acquire the error status again, set the LOCK bit to 0.
Writing 1 to the LOCK bit does not affect the setting.

4.3.8 Transfer control register

This register (DT2_DMACNT: 4015_0020H) controls data transfer.

Settings can be changed only when DMA transfer is not being performed (DT2_DMAREQ register = 0H).

The DTVSP bit must be set to 1 after activation.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved					DTVSP	DTVMODE	DTVENDIAN

Name	R/W	Bit	After Reset	Function
Reserved	R	31:3	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVSP	R/W	2	0	Specifies the data bus type of DTV stream. 0: Burst parallel output **(setting prohibited)** 1: Burst serial output
DTVMODE	R/W	1	1	Specifies the size of a packet. 0: Transfer of synchronization field + data field (188 bytes = 47 words) 1: Transfer of synchronization field + data field + parity field (204 bytes = 51 words)
DTVENDIAN	R/W	0	1	Specifies the DTV stream data format. 0: Big endian 1: Little endian

4.3.9 Transfer request register

This register (DT2_DMAREQ: 4015_0024H) specifies the activation of DMA transfer.

After setting 1 in this register, the lead value of this register is 0 until DMA transfer begins it. When DMA transfer begins it, the lead value changes into 1. 1 is set by a transfer release request cashier, and when DMA transfer stops, the lead value of this register changes into 0.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							DMAREQ

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
DMAREQ	R	0	0	This bit is set to 1 when DMAREQ is acknowledged. This bit is cleared when the transfer request cancellation register (4015_0028H) is set.
	W		–	Writing 1 to this bit issues a DMA transfer request. DMA is repeated until the transfer request cancellation register (4015_0028H) is set. Writing 0 to this bit does not affect the setting.

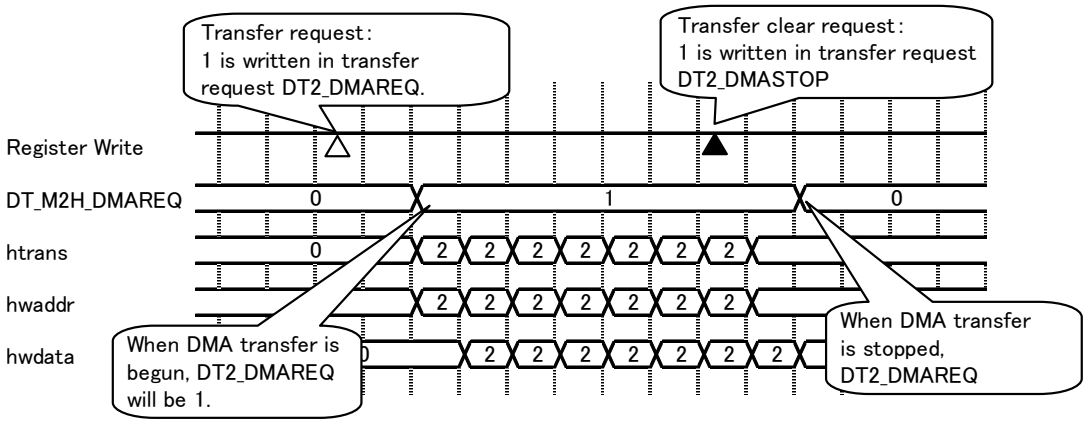


Figure 4-2. Change of transfer request register value

Caution) At the time of a DMA transfer request, a data transfer, just before, DMASTOP, it begins from the address location. When beginning DMA transfer from the start address, do a DMA transfer request after H/W is reset.

4.3.10 Transfer request cancellation register

This register (DT2_DMASTOP: 4015_0028H) stops DMA transfer. It'll be the stop reservation state by setting this register, and when not forwarding to the occasion during packet transfer after transfer, DMA is stopped immediately. The DMA transfer request status can be checked by reading the transfer request register (DT2_DMAREQ). DMA stop interrupt is issued by the time of a fall of status (the lead value of the transfer request register).

This is a write-only register. If the register is set to 1, DMA transfer is finished. Writing 0 to this register does not affect the setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							DMASTOP

Name	R/W	Bit	After Reset	Function
Reserved	W	31:1	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
DMASTOP	W	0	0	Stops DMA transfer. 1: Transfer stop When DMA transfer is being performed, the transfer stops after sending the current packet. Otherwise, the transfer immediately stops

Caution1) The restriction matter in DTV "One for 10 cycles of DTVBCLK leave a space by the (transfer request register set) which resumes DMA after DMA stop interruption, please." is unnecessary in DTV2.

Caution2) Word data until DMA stop request fixation time is forwarded to a memory. Transfer data was filled in the effective data length of 1 packet (188byte or 204byte), when not having that, even a packet next to the stop request fixation after a while will be unsettled data..

4.3.11 Start address register

This register (DT2_START: 4015_002CH) specifies the start address of the DMA transfer destination.

Settings can be changed only when DMA transfer is not being performed (DT2_DMAREQ register = 0H).

31	30	29	28	27	26	25	24
DTV_START							

23	22	21	20	19	18	17	16
DTV_START							

15	14	13	12	11	10	9	8
DTV_START							

7	6	5	4	3	2	1	0
DTV_START						0	0

Name	R/W	Bit	After Reset	Function
DTV_START	R/W	31:0	0	Specifies the start address of the DMA transfer destination (the lower 2 bits are fixed to 0).

4.3.12 Buffer size register

This register (DT2_BUFSIZE: 4015_0030H) specifies the size of the DMA transfer destination area in units of packets.

Settings can be changed only when DMA transfer is not being performed (DT2_DMAREQ register = 0H).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved				DTV_BUFSIZE			

15	14	13	12	11	10	9	8
DTV_BUFSIZE							

7	6	5	4	3	2	1	0
DTV_BUFSIZE						0	0

Name	R/W	Bit	After Reset	Function
Reserved	R	31:20	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTV_ BUFSIZE	R/W	19:0	0	Specifies the size of the DMA transfer destination area in units of packets (the lower 2 bits are fixed to 0).

4.3.13 Blank size register

This register (DT2_BLANK: 4015_0034H) specifies the blank size between packets during DMA transfer.

Settings can be changed only when DMA transfer is not being performed (DT2_DMAREQ register = 0H).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
DTV_BLANK						0	0

Name	R/W	Bit	After Reset	Function
Reserved	R	31:8	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTV_BLANK	R/W	7:0	0	Specifies the blank size between packets (the lower 2 bits must be set to 0).

4.3.14 Current packet register

This register (DT2_CURRENT: 4015_0038H) indicates the number of packets that have been transferred via DMA.

This register shows the value from 0 to “DT2_BUFSIZE register value − 1”.

Settings can be changed only when DMA transfer is not being performed (DT2_DMAREQ register = 0H).

31	30	29	28	27	26	25	24
Reserved							

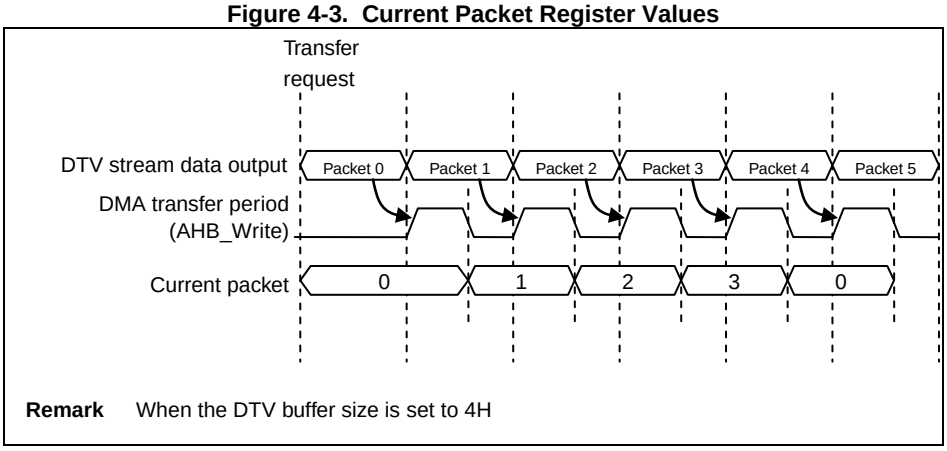
23	22	21	20	19	18	17	16
Reserved				DTV_CURRENT			

15	14	13	12	11	10	9	8
DTV_CURRENT							

7	6	5	4	3	2	1	0
DTV_CURRENT							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:20	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTV_ CURRENT	R	19:0	0	Stores the number of packets that have been transferred via DMA minus 1.

Figure 4-3. Current Packet Register Values



Remark When the DTV buffer size is set to 4H

Caution) The count value is maintained until H/W resets.

4.3.15 DMA completion interrupt setting register

This register (DT2_INTCONT: 4015_003CH) specifies the interval at which a DMA transfer completion interrupt is issued, in units of packets. A DMA transfer completion interrupt is issued each time DMA transfer of "DT2_INTCONT register value + 1" packets is completed.

Settings can be changed only when DMA transfer is not being performed (DT2_DMAREQ register = 0H).

31	30	29	28	27	26	25	24
Reserved							

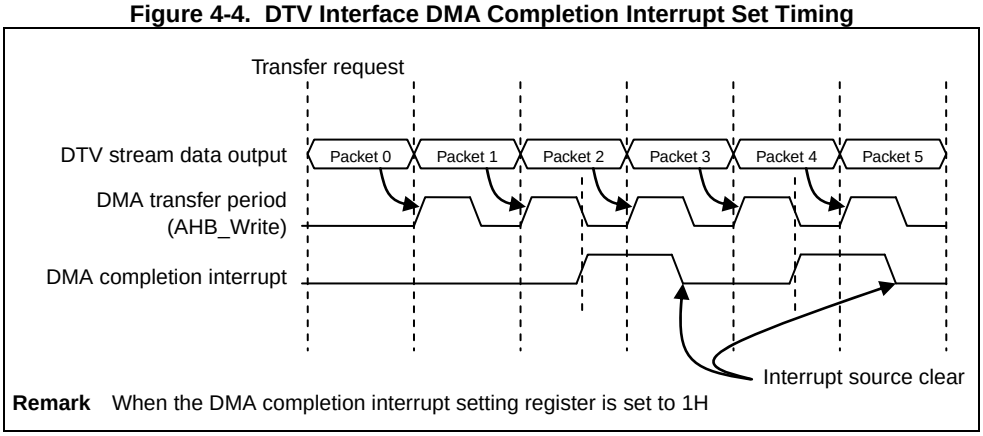
23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
DTV_INTCONT							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:8	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTV_ INTCONT	R/W	7:0	0	Specifies in units of packets the interval at which a DMA transfer completion interrupt is issued. An interrupt is issued every time the number of packets equal to the set value plus 1 are received.

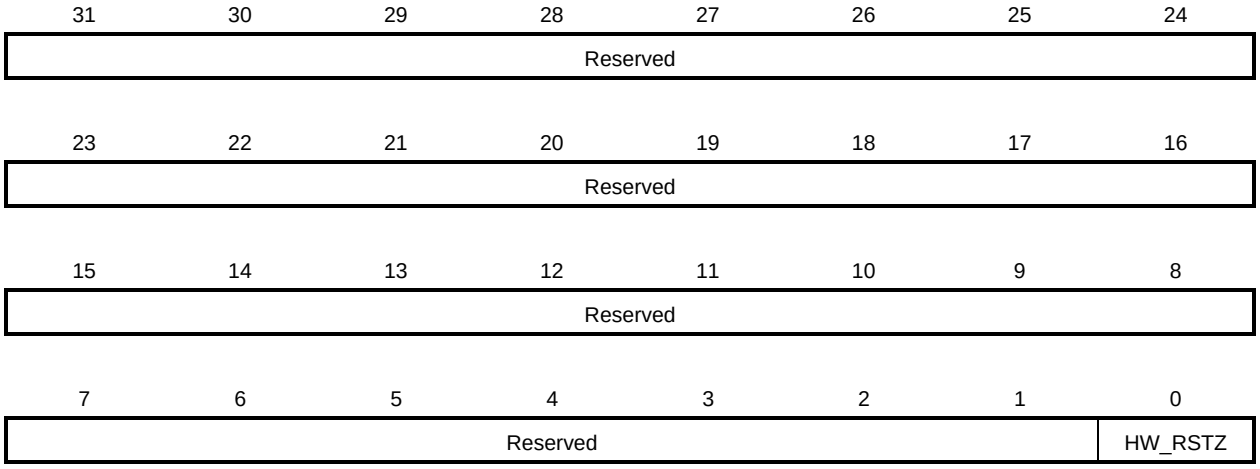
Figure 4-4. DTV Interface DMA Completion Interrupt Set Timing



Remark When the DMA completion interrupt setting register is set to 1H

4.3.16 Module control register

This register (DT2_MODULECONT: 4015_0040H) initializes the operation of the data capturing circuit that synchronizes with DTV_BCLK.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
HW_RSTZ	R/W	0	0	Specifies hardware reset. Specifies whether to initialize the operation of the data capturing circuit that synchronizes with DTV_BCLK. 0: Reset 1: Cancels reset

4.3.17 DTVPSYNC / DTVVLD Polarity designation register

This register (DT2_SIGNALINVERT: 4015_0044H) assign polarity of used DTVPSYNC and DTVVLD respectively..

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						DTVPSYNC	DTVVLD

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVPSYNC	R/W	1	0	Polarity of DTVPSYNC is assigned. 0: Normal 1: Reverse
DTVVLD	R/W	0	0	Polarity of DTVVLD is assigned. 0: Normal 1: Reverse

4.3.18 Input pin status monitor register

This register (DT2_MONITOR: 4015_0048H) indicates terminal input status of DTVPSYNC, DTVVLD, DTVDATA, BCLK..

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
DTVDATA							

7	6	5	4	3	2	1	0
Reserved					DTVBCLK	DTVPSYNC	DTVVLD

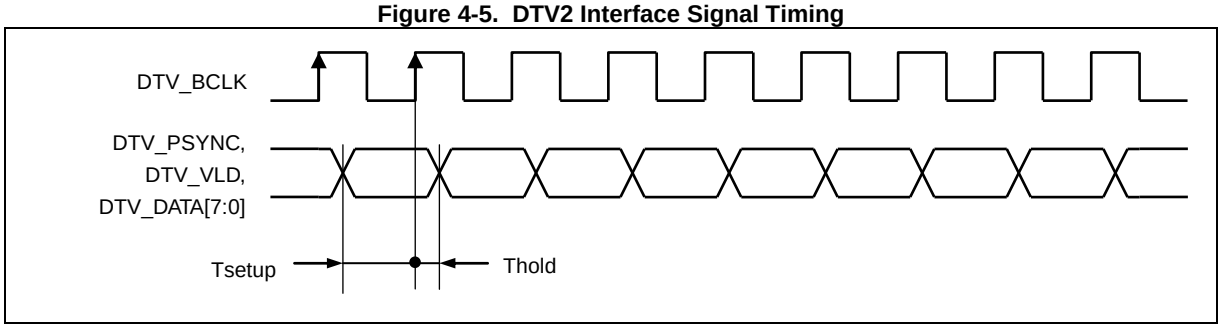
Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVDATA	R	15:8	0	DTVDATA is indicated.
Reserved	R	7:3	0	Reserved. Reading returns the unsettled value. Writing in is ignored.
DTVBCLK	R	2	0	DTVBCLK is indicated.
DTVPSYNC	R/	1	0	DTVPSYNC is indicated.
DTVVLD	R/	0	0	DTVVLD is indicated.

4.4 Function details

4.4.1 Input Signal Timing

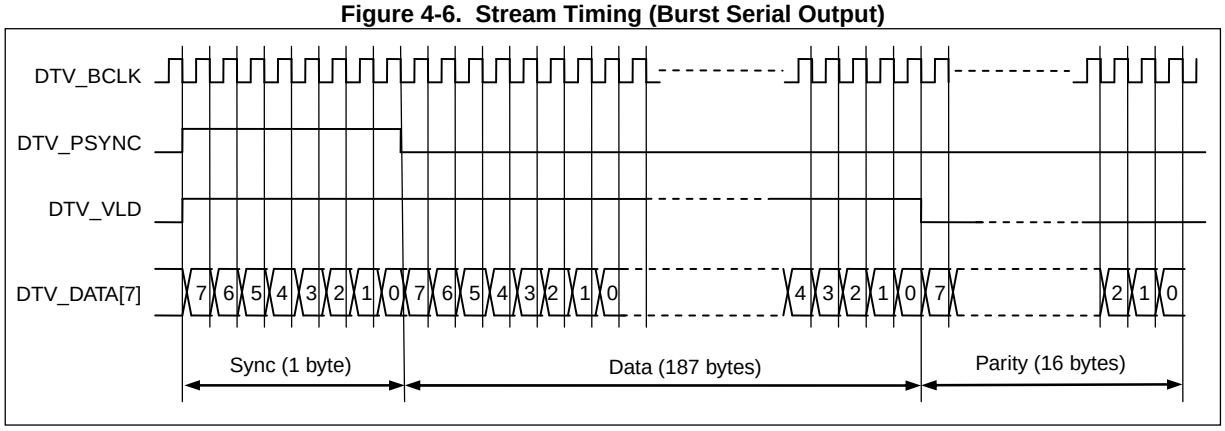
(1) DTV2 I/F signal timing

Figure 4-5. DTV2 Interface Signal Timing



(2) Stream timing

Figure 4-6. Stream Timing (Burst Serial Output)

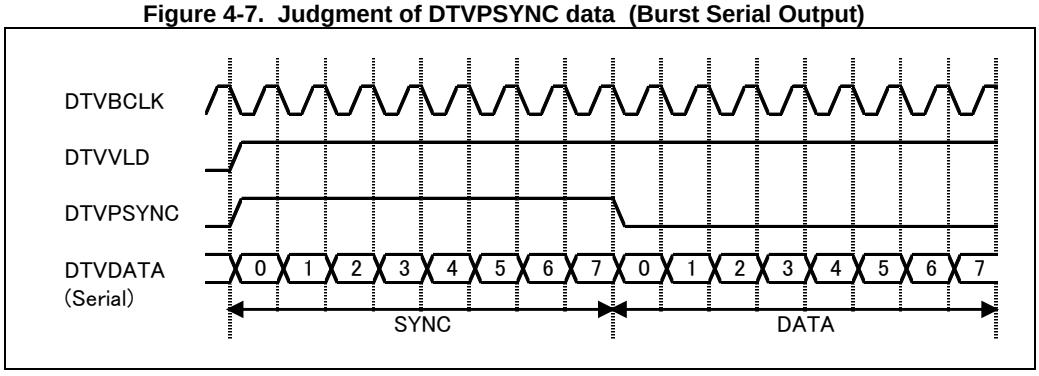


Caution Polarity assignation is possible by register setting in DTVSYNC,DTVVLD.

(3) At the timing of a receipt of DTV2 I/F signal (Burst Serial Output)Stream timing

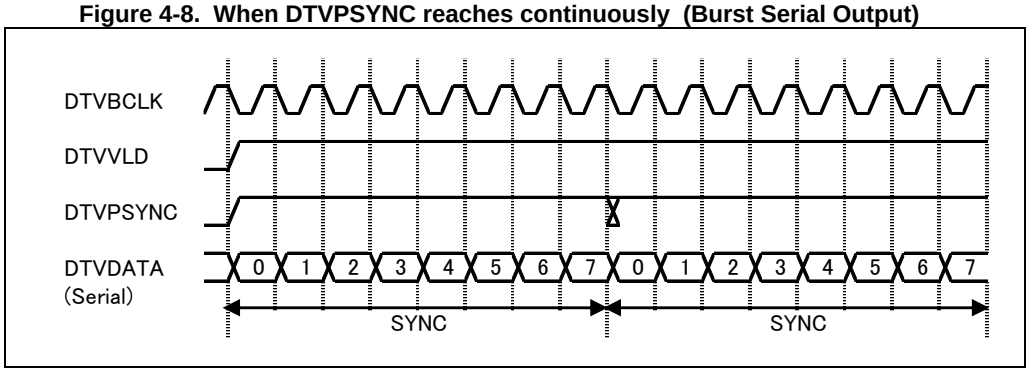
When DTVVLD=1 and DTVPSYNC=1 reached for 8 cycles continuously, the 8bits data received at that time is made SYNC. It's made DATA from 8bits following that.

Figure 4-7. Judgment of DTVPSYNC data (Burst Serial Output)



It's made SYNC continued by the 8bits unit as it indicates on figure 4-8 when DTVVLD=1 and DTVPSYNC=1 reached more than 16 cycles continuously.

Figure 4-8. When DTVPSYNC reaches continuously (Burst Serial Output)



When it was DTVVLD=0 during reception, the effective Data bit is made data using 8bits except for DTVVLD=0 period (figure 4-9). In case of DTVPSYNC=1, like, it's made SYNC using 8bits except for DTVVLD=0 period (figure 4-10). But, when changing into DTVPSYNC=0 during DTVVLD=0 period, it's made DATA, not SYNC (figure 4-11).

Figure 4-9. When DTVVLD intermits (Burst Serial Output)

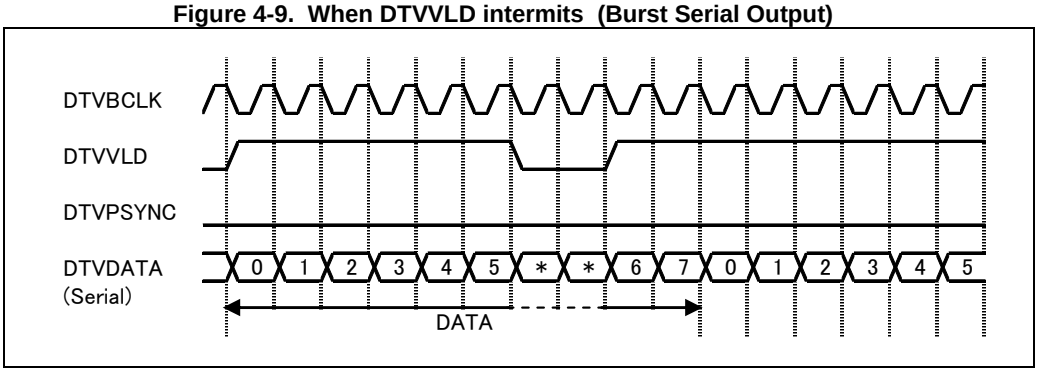


Figure 4-10. When DTVVLD intermits while DTVPSYNC is HIGH (Burst Serial Output)

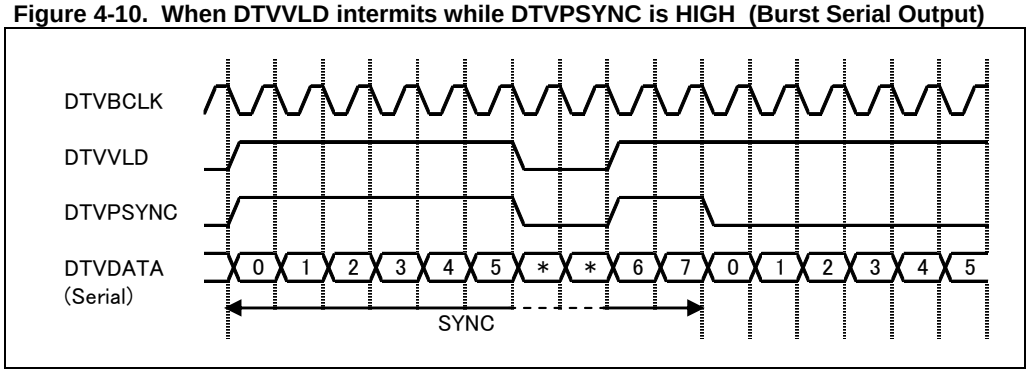
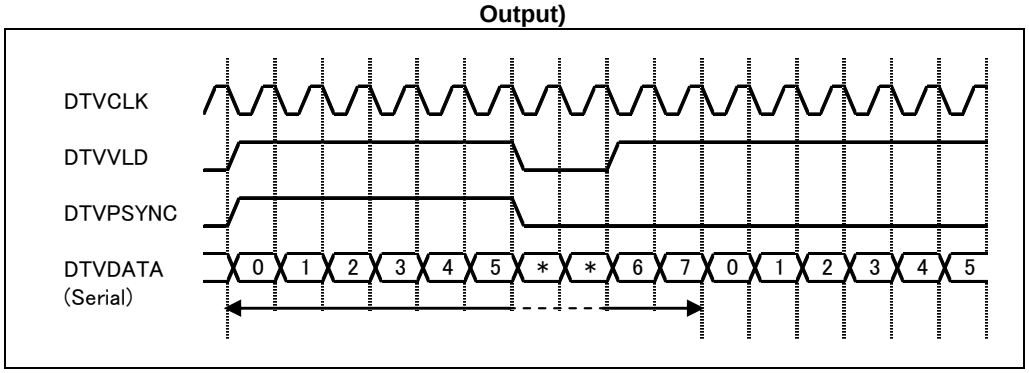


Figure 4-11. When DTVPSYNC stands up and goes down during a DTVVLD intermission period (Burst Serial Output)



Even DTVVLD=1 doesn't receive data in the period when DTVBCLK doesn't enter (figure 4-12, 4-13).

Figure 4-12. When BCLK intermits (Burst Serial Output)

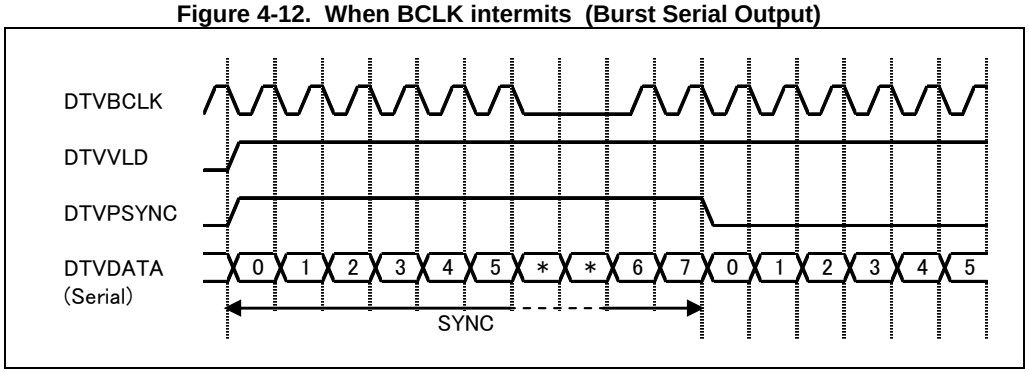
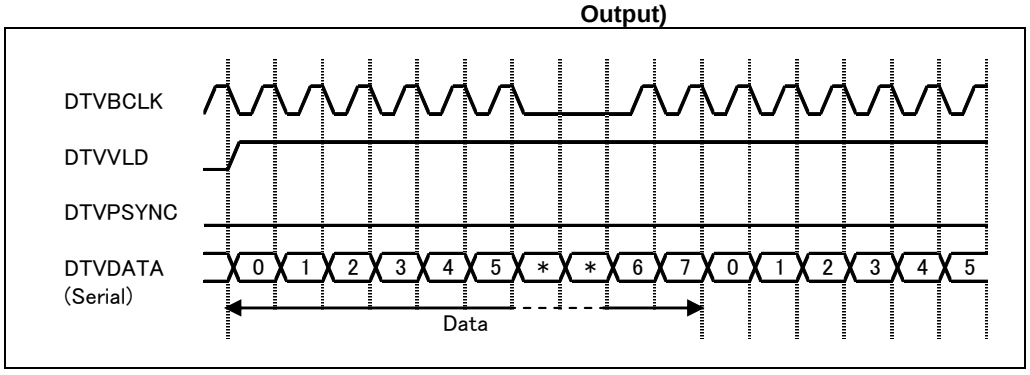


Figure 4-13. When DTVPSYNC stands up and goes down during a BCLK intermission period (Burst Serial Output)



The bit line was filled in 8bits, when it was DTVPSYNC=1 in the state I don't have, it's made Data after that 8 bits in even time. When DTVPSYNC continues it 8 cycles, just after making the rising of DTVPSYNC a cardinal point, it's made SYNC with 8bits (figure 4-14). DTVPSYNC=1 was filled in 8 cycles, when not having that, it's made effective data just before from the bit line 8bits later (figure 4-15).

Figure 4-14. The bit just before the DTVPSYNC arrival was filled in 8bits, when I don't have that (Burst Serial Output)

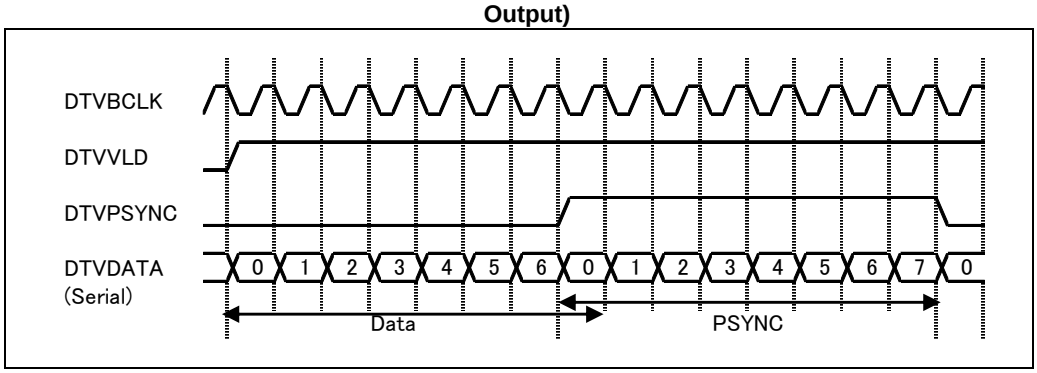
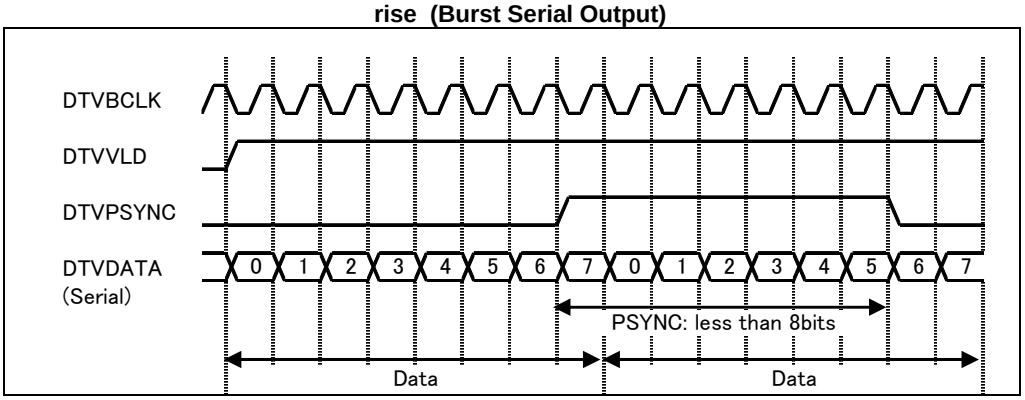


Figure 4-15. The bit line just before the DTVPSYNC arrival, when 8bits non-rise and DTVPSYNC are 8bits non-rise (Burst Serial Output)



The bit line received just after just after the start and the reset will be an invalid bit, and it's made the effective bit from first DTVPSYNC (figure 4-16). It was filled in 8bits which has been received at the end in a case with a reset when receiving an effective bit, the data I don't have is made invalid data (figure 4-17).

Figure 4-16. Until DTVPSYNC comes to the data just after the reset, invalid data (Burst Serial Output)

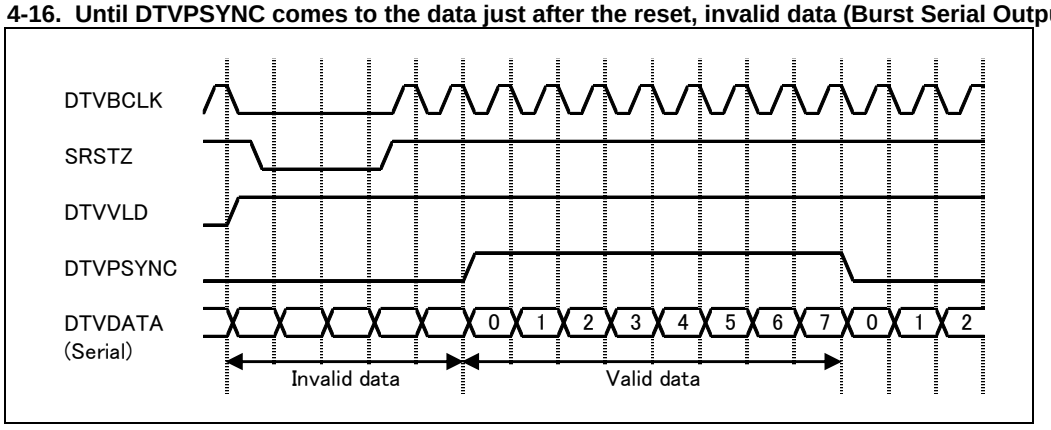
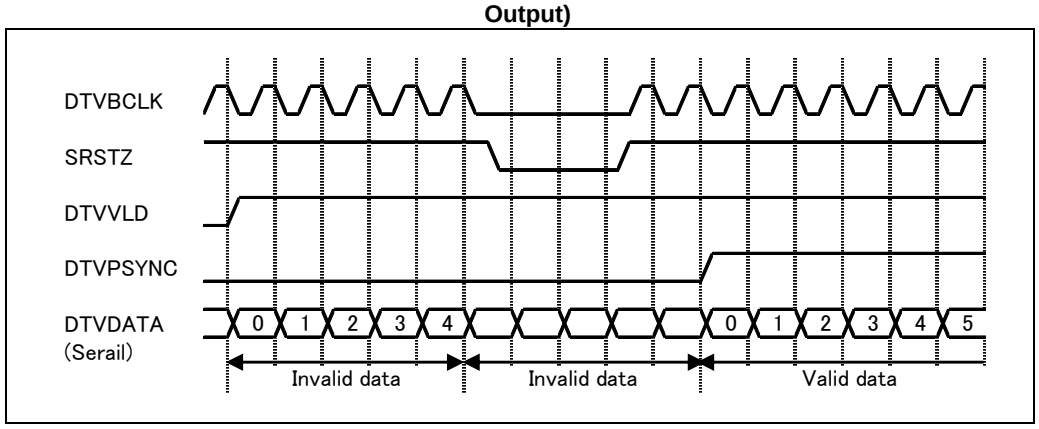
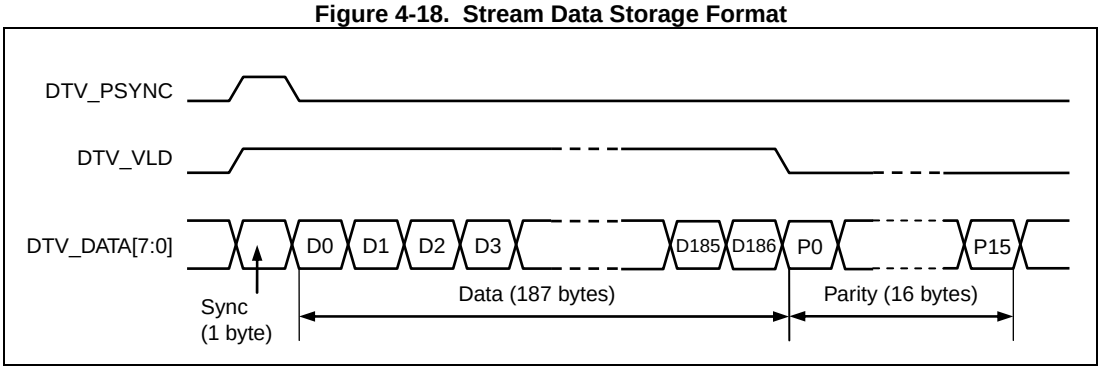


Figure 4-17. It was filled in 8bits just before the reset, the data I don't have is invalid data (Burst Serial Output)



4.4.2 Data Format

Figure 4-18. Stream Data Storage Format



Data input as shown in Figure 4-18 is stored in the memory in the following format, in accordance with the value set to the DTVENDIAN bit of the transfer control register (DT2_DMACNT).

Bit alignment	31 to 24	23 to 16	15 to 8	7 to 0
50 words	P15	P14	P13	P12
49 words	P11	P10	P9	P8
48 words	P7	P6	P5	P4
47 words	P3	P2	P1	P0
46 words	D186	D185	D184	D183
	:	:	:	:
3 words	D14	D13	D12	D11
2 words	D10	D9	D8	D7
1 word	D6	D5	D4	D3
0 words	D2	D1	D0	Sync

Little endian

31 to 24	23 to 16	15 to 8	7 to 0
P14	P15	P12	P13
P10	P11	P8	P9
P6	P7	P4	P5
P2	P3	P0	P1
D185	D186	D183	D184
:	:	:	:
D13	D14	D11	D12
D9	D10	D7	D8
D5	D6	D3	D4
D1	D2	Sync	D0

Big endian

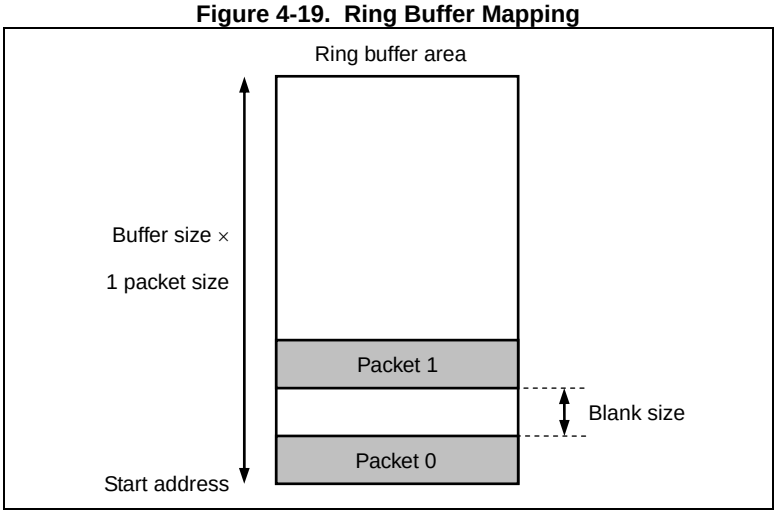
4.4.3 DTV Transfer Processing

Stream data is transferred to the specified buffer area in the memory, in units of packets. The buffer is used as a ring buffer in which the pointer returns to the beginning of the buffer after the specified number of packets are stored.

The following three registers are used to set up the buffer.

- Start address register (32 bits): Specifies the ring buffer start address.
- Buffer size register (20 bits): Specifies the ring buffer area by a packet count.
- Blank size register (8 bits): Specifies the blanking interval between packets.

Figure 4-19. Ring Buffer Mapping



Effective size of 1 packet and data is established by the DTVMODE bit of the transfer control register (DT2_DMACNT) by 188 bytes or 204 bytes.

The capacity of 1 packet unit by which the mapping is made a buffer will be the effective size chosen by the DTVMODE bit+ blank size. The total capacity of the ring buffer will be a packet of above-mentioned volume x buffer size.

The DTV flow received from OFDM is the part-time work unit, and buffering is done by FIFO inside DTV2, and every time it gathers 4 bytes, DMA is forwarded to a memory (figure 4-20).

Data is stocked by new address aligning which made SyncByte the head as I come and show in figure 4-21 at the time of the following exception occurrence at the time of SyncByte reception at the time of normal operation.

a) When next SyncByte has come after restoration from a FIFO overflow by a packet overrun.

b) When next SyncByte has come (An excess is repealed.) after the transfer amount of the data exceeded a packet of effective size.

c) When the transfer amount of the data is a packet of effective size sheep rise, and next SyncByte has come (The shortage will be unsettled data.)

d) When it's different from the expectation value (47H or B8H is established by the DTVMODE bit of the DMA control register.) in the price of received SyncByte.

Figure 4-20. Stock method of a packet (at DTVMODE=0)

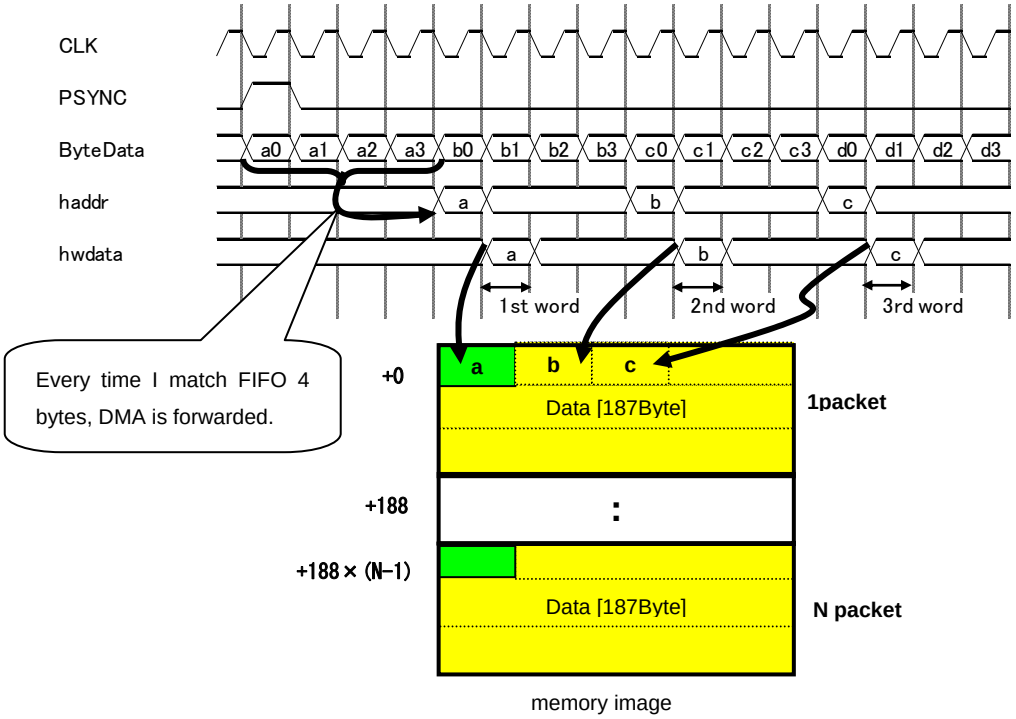
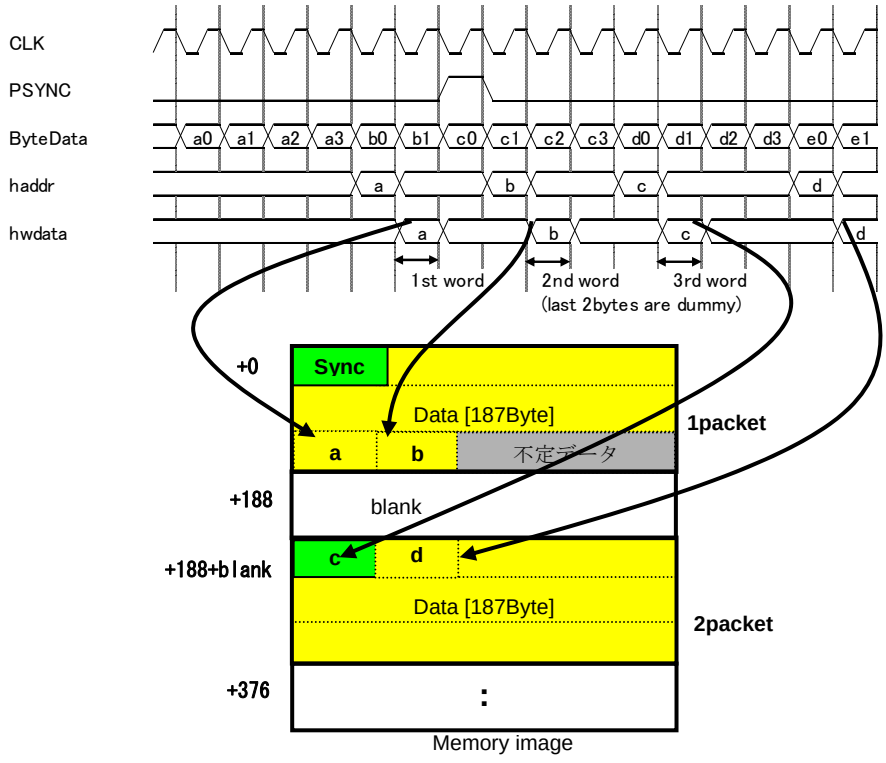


Figure 4-21. Packet stock method when next SyncByte has come, (at DTVMODE=0)



4.4.4 Interrupt Control

DTV2 I/F issues 7 kinds of interrupt.

Control of each interrupt interrupts, and it's assigned to each bit of the status register. Please refer to table 4-1 for details.

Table 4-1. Interrupt Sources

Interrupt Type	When to Issue	Bit Assignment
Packet length excess interrupt	Issued when 1 packet exceeded 188byte or 204byte.	DT2_STATUS[6] : DTVLP
Packet length short interrupt	Issued when DTVPSYNC=1 and reception data are less than 187 bytes or less than 203 bytes.	DT2_STATUS[5] : DTVSP
Illegal SyncByte onyerrupt	Issued when the price of DTVPSYNC=1 and SyncByte is 47H or anything but B8H.	DT2_STATUS[4] : DTVSYNC
DMA stop interrupt	Issued when the DMA transfer stops.	DT2_STATUS[3] : DTVSTOP
Packet overrun	Issued when the internal buffer overruns.	DT2_STATUS[2] : DTVOR
DMA completion interrupt	Issued when the specified number of packets have been transferred.	DT2_STATUS[1] : DTVDMA
Transfer error interrupt	Issued when the ERROR response is received during internal bus transfer.	DT2_STATUS[0] : DMAERR

(1) Transfer error interrupt

When a ERROR reply is received during Internal bus transfer, interrupt is generated.

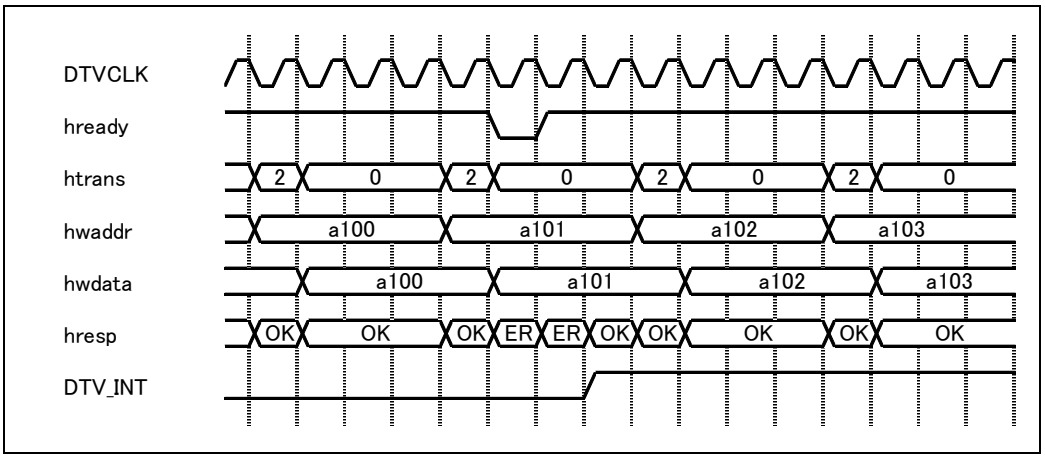


Figure 4-21. Transfer error interrupt timing

(2) DMA completion interrupt

Every time DMA of the number of packets set as register DT2_INTCONT is completed, interrupt is generated.

(3) Packet overrun interrupt

DTV2 I/F uses the inner memory (32 bits x 128 words) as a buffer. A bustle of a word does DMA transfer of completed data. When the interior buffer overflows, overrun interrupt is generated. When a packet overrun occurred, the adjustment-lessness occurs to the packet data input from DTV and the range stocked in a ring buffer, but after return, a normal packet bustle is resumed from next Psync from a packet overrun.

(4) DMA stop interrupt

When doing DMA transfer of DMA immediately when not forwarding, when DMA transfer stop reservation was formed out of register DT2_DMASTOP, when the transfer has been completed, interrupt is generated.

Figure 4-23. At the timing of the interruption when DMA transfer is being done, and transfer has been reserved to cry

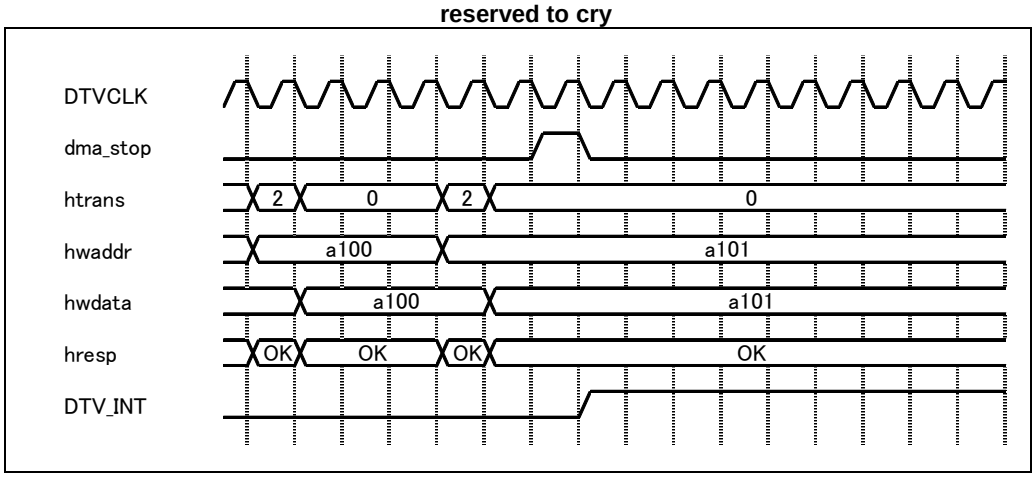
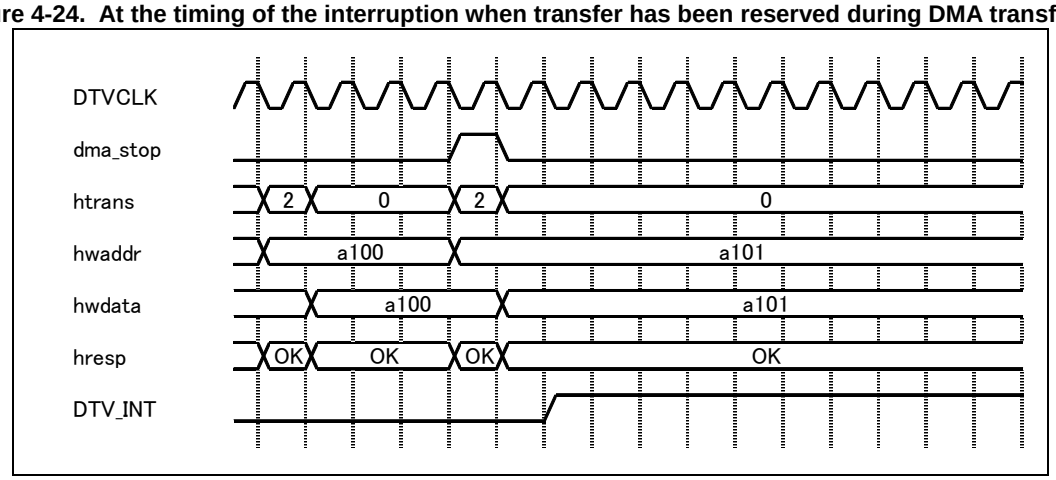


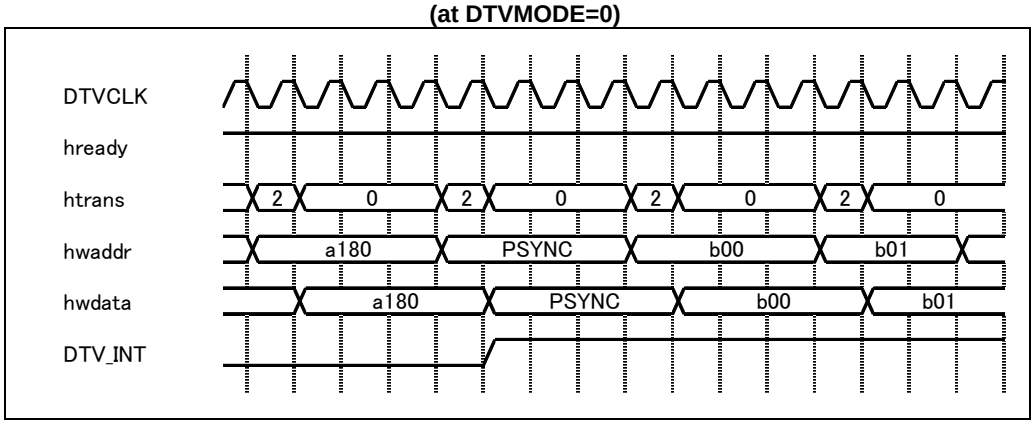
Figure 4-24. At the timing of the interruption when transfer has been reserved during DMA transfer



(5) Packet length short interrupt

When next SyncByte has arrived in less than 203 bytes of state at less than 187 bytes and packet chief effective size 204byte at packet chief effective size 188byte, the forwarded data length generates interrupt. Effective size is established by the DTVMODE bit of the transfer control register.

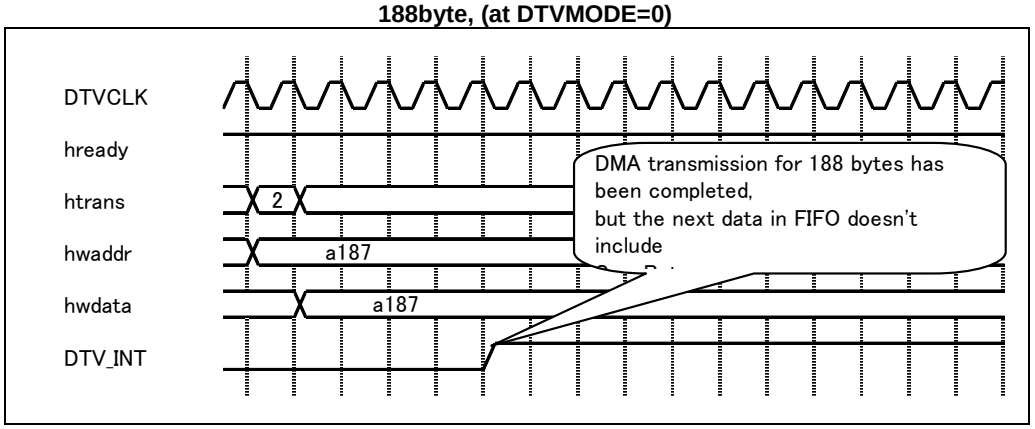
Figure 4-25. Interrupt timing of the word transfer which includes PSYNC part-time work by less than 187 bytes (at DTVMODE=0)



(6) Packet length excess interrupt

When a packet chief closes beyond effective size (188byte or 204byte), interrupt is generated. Effective size is designated by the DTVMODE bit of the transfer control register.

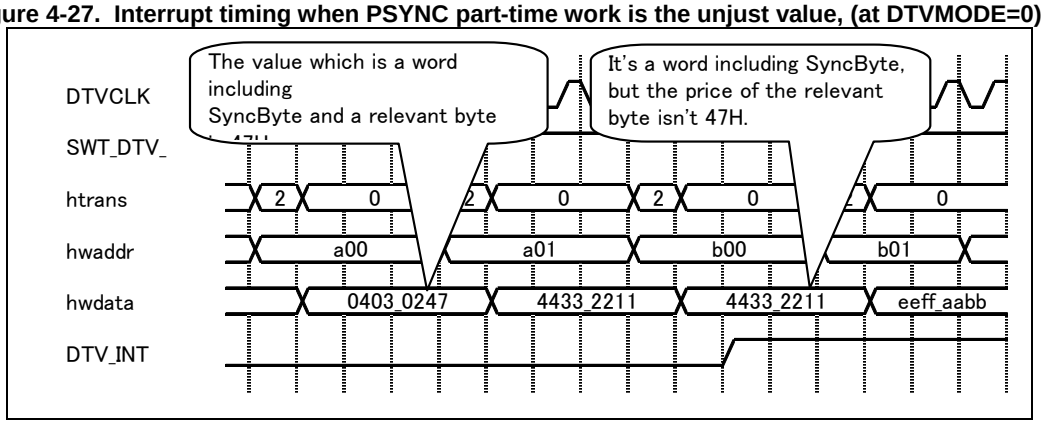
Figure 4-26. Interrupt timing when also not having complete set of word data including SyncByte beyond 188byte, (at DTVMODE=0)



(6) Illegal SyncByte interrupt

SyncByte shows 47H or B8H. The time 47H the price is decided about by DTVMODE of a transfer control register, and which is DTVMODE=0, the B8H is made the expectation value at DTVMODE=1. In case of all except for the expectation value, SyncByte of DMA transfer word data including SyncByte brings about unjust SyncByte interrupt.

Figure 4-27. Interrupt timing when PSYNC part-time work is the unjust value, (at DTVMODE=0)



4.4.5 Clocks Control

In EM1, supply of the internal bus clock is controlled by each module to save power.

The internal bus clock is supplied upon requests from modules and upon register access.

In the DTV interface, a clock supply request is set when a DMA transfer is requested through register access, and the clock supply request is cleared when transfer of the current DMA is completed with no other transfers requested.

(1) Clocks used in DTV interface

(a) DTV_BCLK (external input clock)
Used for capturing the DTV data clock and data.

(b) DTV_CLK (DTV internal clock)
Used for the AHB bus clock and the internal operation of the DTV interface.

(c) DTV_PCLK (APB clock)
Used for the accessing the APB bus (registers).

For details about clock/reset settings, see the **Multimedia Processor for Mobile Applications - System Control/General-Purpose I/O Interface User's Manual (S19265E)**.

(2) DTV_CLKREQ set timing

When the DTV transfer request register is set.

(3) DTV_CLKREQ clear timing

When the DTV transfer request cancellation register is set and DMA transfer of the current packet is completed.

(4) DTV_SWT_CLKREQ output timing

The signal 1CLK preceded to transaction is output as CLKREQ for bus switches.

Signal rising is 1CLK precedence of transaction, and a fall is at the timing of an end of the data phase.

Revision History

Date	Revision	Comments
February 10, 2009	1.0	–
April 27, 2009	2.0	Incremental update from comments to the 1.0.
September 30, 2009	3.0	Incremental update from comments to the 2.0. 4.5 chapters and 4.6 chapters are added.
October 13, 2009	4.0	The item of DTV2 is added. (chapter 4)

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