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RENESAS

User's Manual

Multimedia Processor for Mobile Applications

MICROWIRE

EMMA Mobile1

Document No. S19259EJ2V0UM00 (2nd edition)
Date Published April 2009

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E 02. 11-1

PREFACE

Readers

This manual is intended for hardware/software application system designers who wish to understand and use the MICROWIRE™ interface functions of EMMA Mobile1 (EM1), a multimedia processor for mobile applications.

Purpose

This manual is intended to explain to users the hardware and software functions of the MICROWIRE interface of EM1, and be used as a reference material for developing hardware and software for systems that use EM1.

Organization

This manual consists of the following chapters.

- Chapter 1 Overview
- Chapter 2 Pin functions
- Chapter 3 Registers
- Chapter 4 Description of functions
- Chapter 5 Usage

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, and microcontrollers.

To understand the functions of the MICROWIRE interface of EM1 in detail

→ Read this manual according to the **CONTENTS**.

To understand the other functions of EM1

→ Refer to the user's manual of the respective module.

To understand the electrical specifications of EM1

→ Refer to the Data Sheet.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Data type:	Word … 32 bits
	Halfword … 16 bits
	Byte … 8 bits

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document No.
MC-10118A Data sheet		S19657E
μPD77630A Data sheet		S19686E
User's manual	Audio/Voice and PWM Interfaces	S19253E
	DDR SDRAM Interface	S19254E
	DMA Controller	S19255E
	I^2C Interface	S19256E
	ITU-R BT.656 Interface	S19257E
	LCD Controller	S19258E
	MICROWIRE	This manual
	NAND Flash Interface	S19260E
	SPI	S19261E
	UART Interface	S19262E
	Image Composer	S19263E
	Image Processor Unit	S19264E
	System Control/General-Purpose I/O Interface	S19265E
	Timer	S19266E
	Terrestrial Digital TV Interface	S19267E
	Camera Interface	S19285E
	USB Interface	S19359E
	SD Memory Card Interface	S19361E
	PDMA	S19373E
	One Chip (MC-10118A)	S19598E
	One Chip (μPD77630A)	S19687E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

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CHAPTER 1 OVERVIEW

The MICROWIRE interface is a 4-wire serial I/O interface for EM1.

Caution The MWI_CS1 signal has been removed from the EM1 specifications, but the descriptions of the signal remain in this document.

1.1 Features

The main features of the MICROWIRE interface are as follows:

- Conversion from serial to parallel or from parallel to serial
- The transmission data unit is 64 bits maximum and the received data unit is 32 bits maximum.
- Synchronous trigger
- Serial transmission clock control
- Single transfer (data transmission, reception, concurrent transmission/reception)
- Burst transfer (data transmission, reception, concurrent transmission/reception)

Remark During data transmission using a burst transfer, only data transmission is contiguous.
During data transmission, the mode cannot be changed to data reception or concurrent data transmission/reception.

○ Clock output
- Transmission clock (MWI_SK)

○ Data format
- Transmission: 32-bit variable address, 32-bit (up to 64-bit) variable data
- Reception: 32-bit variable data

CHAPTER 2 PIN FUNCTIONS

2.1 MICROWIRE Interface Pins

Pin Name	I/O	After Reset	Function	Alternate Pin Function
MWI_SK	Output	0	Transmission clock	SP0_CLK
MWI_SI	Input	–	Serial input data	SP0_SI
MWI_SO	Output	0	Serial output data	SP0_SO
MWI_CS	Output	0	Slave chip select	SP0_CS0

CHAPTER 3 REGISTERS

3.1 Registers

The MICROWIRE interface registers allow word access only.

Do not access reserved registers. An undefined value is returned for a read access.

Do not write any value other than 0 to reserved bits in each register.

Base address: C016_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	System control register	MWI_CONT	R/W	0000_0000H
0004H	CS0 setting register	MWI_CS0	R/W	0000_0001H
0008H	CS1 setting register	MWI_CS1	R/W	0000_0001H
000CH	Communication start register	MWI_START	R/W	0000_0000H
0020H	Interrupt status register	MWI_INTSTATUS	R	0000_0000H
0024H	Interrupt raw status register	MWI_INTRAW	R	0000_0000H
0028H	Interrupt source clear register	MWI_INTFFCLR	W	0000_0000H
002CH	Interrupt enable set register	MWI_INTENSET	R/W	0000_0000H
0030H	Interrupt enable clear register	MWI_INTENCLR	W	0000_0000H
0040H	Transmission address register	MWI_TXQA	R/W	0000_0000H
0050H	Transmission data register	MWI_TXQ	R/W	0000_0000H
0060H	Reception data register	MWI_RXQ	R	0000_0000H

3.2 Register Functions

The MICROWIRE interface has three communication modes: data transmission mode, data reception mode, and concurrent data transmission/reception mode.

The communication mode cannot be changed during communication, regardless of which mode is used. If the settings of the MWI_CONT, MWI_CS1, and MWI_CS0 registers are changed during communication, the operation is not guaranteed. Therefore, set up these registers before starting communication.

3.2.1 System control register

This register (MWI_CONT: C016_0000H) specifies the MICROWIRE interface operation.

If the settings of this register are changed during communication (while the START bit of the MWI_START register is 1), the operation is not guaranteed.

31	30	29	28	27	26	25	24
Reserved		BITRX_EN	BIT_RX4	BIT_RX3	BIT_RX2	BIT_RX1	BIT_RX0

23	22	21	20	19	18	17	16
Reserved		BITATX_EN	BIT_ATX4	BIT_ATX3	BIT_ATX2	BIT_ATX1	BIT_ATX0

15	14	13	12	11	10	9	8
Reserved		BITDTX_EN	BIT_DTX4	BIT_DTX3	BIT_DTX2	BIT_DTX1	BIT_DTX0

7	6	5	4	3	2	1	0
Reserved		CS1_EN	CS0_EN	CS1	CS0	RX_ EN	TX_EN

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31:30	0	Reserved. When these bits are read, 0 is returned for each bit.
BITRX_EN	R/W	29	0	Specifies whether to enable the received data bit width specified by the BIT_RX bit. 0: Disable (default) 1: Enable When this bit is set to 0, the received data bit length is set to 0. The BIT_RX setting does not change.
BIT_RX	R/W	28:24	00H	Specifies the received data bit width. Any value from 00H to 1FH (1 to 32 bits) can be set. 00H: 1 bit, 01H: 2 bits, …, 1EH: 31 bits, 1FH: 32 bits
Reserved	R	23:22	0	Reserved. When these bits are read, 0 is returned for each bit.
BITATX_EN	R/W	21	0	Specifies whether to enable the transmission address bit width specified by the BIT_ATX bit. 0: Disable (default) 1: Enable When this bit is set to 0, the transmission address bit length is set to 0. The BIT_ATX setting does not change.

(2/2)

Name	R/W	Bit	After Reset	Function
BIT_ATX	R/W	20:16	00H	Specifies the transmission address bit width. Any value from 00H to 1FH (1 to 32 bits) can be set. 00H: 1 bit, 01H: 2 bits, …, 1EH: 31 bits, 1FH: 32 bits
Reserved	R	15:14	0	Reserved. When these bits are read, 0 is returned for each bit.
BITDTX_EN	R/W	13	0	Specifies whether to enable the transmission data bit width specified by the BIT_DTX bit. 0: Disable (default) 1: Enable When this bit is set to 0, the transmission data bit length is set to 0. The BIT_DTX setting does not change.
BIT_DTX	R/W	12:8	00H	Specifies the transmission data bit width. Any value from 00H to 1FH (1 to 32 bits) can be set. 00H: 1 bit, 01H: 2 bits, …, 1EH: 31 bits, 1FH: 32 bits
Reserved	R	7:6	0	Reserved. When these bits are read, 0 is returned for each bit.
CS1_EN	W	5	0	Specifies whether to enable writing to the CS1 bit. (When the CS1_EN bit is read, 0 is returned.) Set up this bit and the CS1 bit simultaneously. 0: Disable (default) 1: Enable
CS0_EN	W	4	0	Specifies whether to enable writing to the CS0 bit. (When the CS0_EN bit is read, 0 is returned.) Set up this bit and the CS0 bit simultaneously. 0: Disable (default) 1: Enable
CS1	R/W	3	0	The value written to this bit is valid when the CS1_EN bit is 1.
CS0	R/W	2	0	The value written to this bit is valid when the CS0_EN bit is 1.
RX_EN	R/W	1	0	Specifies whether to enable reception. 0: Disable (default) 1: Enable
TX_EN	R/W	0	0	Specifies whether to enable transmission. 0: Disable (default) 1: Enable

(1) Specifying a communication mode

Use the BITRX_EN, BITATX_EN, and BITDTX_EN bits to select a communication mode.

Communication Mode	BITRX_EN	BITATX_EN	BITDTX_EN	RX_EN	TX_EN
Data transmission mode	0	1	1	0	1
Data reception mode	1	1	0	1	1
Concurrent data transmission/reception mode	1	0	1	1	1

Caution If settings other than above are specified, communication does not start even if the START bit of the communication start register is enabled.

(2) Controlling the MWI_CS1 and MWI_CS0 signals

When concurrently setting the CS1_EN and CS0_EN bits to 1, do not specify settings that assert both the MWI_CS1 and MWI_CS0 signals. After communication ends, set the CS1 or CS0 bit corresponding to the asserted signal to a value that deasserts the signal (1, if the active level is 0).

There are four setting patterns.

(a) When the active level of the MWI_CS1 and MWI_CS0 signals is 0

Set the CS1 and CS0 bits to 1 before starting communication.

CS1	CS0	Description
0	0	Setting prohibited.
0	1	Asserts the MWI_CS1 signal.
1	0	Asserts the MWI_CS0 signal.
1	1	Initial setting (Both signals are inactive.)

(b) When the active level of the MWI_CS1 signal is 0 and the active level of the MWI_CS0 signal is 1

Set the CS1 bit to 1 and the CS0 bit to 0 before starting communication.

CS1	CS0	Description
0	0	Asserts the MWI_CS1 signal.
0	1	Setting prohibited.
1	0	Initial setting (Both signals are inactive.)
1	1	Asserts the MWI_CS0 signal.

(c) When the active level of the MWI_CS1 signal is 1 and the active level of the MWI_CS0 signal is 0

Set the CS1 bit to 0 and the CS0 bit to 1 before starting communication.

CS1	CS0	Description
0	0	Asserts the MWI_CS0 signal.
0	1	Initial setting (Both signals are inactive.)
1	0	Setting prohibited.
1	1	Asserts the MWI_CS1 signal.

(d) When the active level of the MWI_CS1 and MWI_CS0 signals is 1

Set the CS1 and CS0 bits to 0 before starting communication.

CS1	CS0	Description
0	0	Initial setting (Both signals are inactive.)
0	1	Asserts the MWI_CS0 signal.
1	0	Asserts the MWI_CS1 signal.
1	1	Setting prohibited.

Caution If communication starts while both the MWI_CS1 and MWI_CS0 signals are active, the operation is not guaranteed.

Example An operation example when the active level of the MWI_CS1 signal is 1 and the active level of the MWI_CS0 signal is 0 is shown below (see **Figure 3-1**). For the setting for the CS1_EN, CS0_EN, CS1, and CS0 bits of the MWI_CONT register, see **Table 3-1**.

<1> Initial setting: The MWI_CS1 and MWI_CS0 signals are inactive.
Register settings: CS1_EN = 1, CS1 = 0
CS0_EN = 1, CS0 = 1

<2> Preparation for CS1 communication: Assert the MWI_CS1 signal.
Register settings: CS1_EN = 1, CS1 = 1
CS0_EN = 0, CS0 = any value

<3> Completion of CS1 communication: Deassert the MWI_CS1 signal.
Register settings: CS1_EN = 1, CS1 = 0
CS0_EN = 0, CS0 = any value

<4> Preparation for CS0 communication: Assert the CS0 signal.
Register settings: CS1_EN = 0, CS1 = any value
CS0_EN = 1, CS0 = 0

<5> Completion of CS0 communication: Deassert the CS0 signal.
Register settings: CS1_EN = 0, CS1 = any value
CS0_EN = 1, CS0 = 1

Figure 3-1. CS Control Example

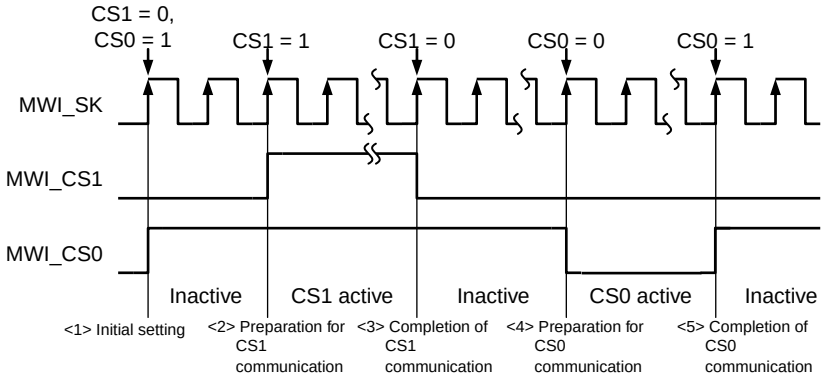
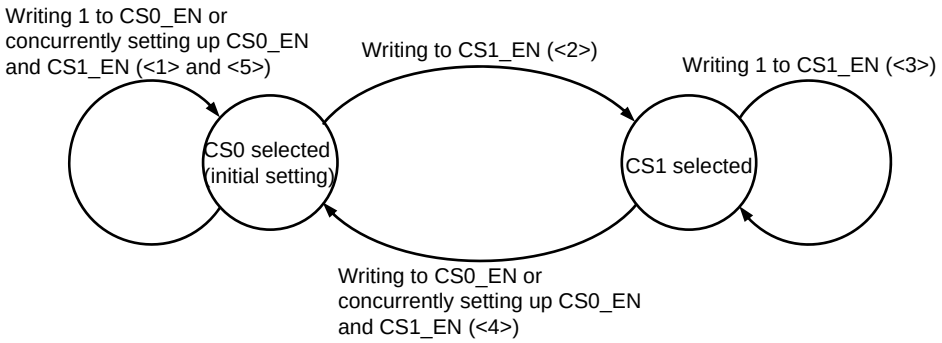


Table 3-1. Settings of CSn_EN and CSn Bits

CSn_EN	CSn	Description (n = 1, 0)
0	0	The previous CSn value is retained.
0	1	The previous CSn value is retained.
1	0	The active level of the MWI_CSn signal is set to 0.
1	1	The active level of the MWI_CSn signal is set to 1.

Which of the MWI_CS0 and MWI_CS1 signals is asserted is specified by using the CS0_EN and CS1_EN bits of the MWI_CONT register. Figure 3-2 shows the transition of the selection status.

Figure 3-2. Transition of CS Selection Status



Remark Statuses <1> to <5> in Figure 3-2 correspond to the step numbers of the operation example shown in Figure 3-1.

3.2.2 CS0 setting register

This register (MWI_CS0: C016_0004H) selects the clock edge (the rising or falling edge) of the MWI_CS0 signal at which data is transmitted or received, when the use of CS0 is selected. If the settings of this register are changed during communication, the operation is not guaranteed.

For details about how to select the register, see **3.2.1 (2) Controlling MWI_CS1 and MWI_CS0.**

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						RX_EDGE0	TX_EDGE0

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0	Reserved. When these bits are read, 0 is returned for each bit.
RX_EDGE0	R/W	1	0	Selects the sampling edge for reception. 0: Rising edge (default) 1: Falling edge
TX_EDGE0	R/W	0	1	Selects the edge of the output trigger for transmission. 0: Rising edge 1: Falling edge (default)

3.2.3 CS1 setting register

This register (MWI_CS1: C016_0008H) selects the clock edge (the rising or falling edge) of the MWI_CS1 signal at which data is transmitted or received, when the use of CS1 is selected. If the settings of this register are changed during communication, the operation is not guaranteed.

For details about how to select the register, see **3.2.1 (2) Controlling MWI_CS1 and MWI_CS0.**

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						RX_EDGE1	TX_EDGE1

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0	Reserved. When these bits are read, 0 is returned for each bit.
RX_EDGE1	R/W	1	0	Selects the sampling edge for reception. 0: Rising edge (default) 1: Falling edge
TX_EDGE1	R/W	0	1	Selects the edge of the output trigger for transmission. 0: Rising edge 1: Falling edge (default)

3.2.4 Communication start register

This register (MWI_START: C016_000CH) starts MICROWIRE interface communication. This register can be used to check the current communication status.

If the START bit is set to 0 during communication, the communication is stopped forcibly, but this setting is prohibited because the operation after that is not guaranteed.

To execute the same communication (burst transfer) after the previous communication is completed, write 1 to the START bit again.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							START

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
START	R/W	0	0	Starts serial communication. When read: 0: Communication is stopped (default). 1: Communication is in progress. When written: 0: Stops communication. This setting is prohibited during communication. 1: Starts communication. This bit is cleared to 0 after the completion of communication.

Cautions 1. Before setting the START bit to 1, read the START bit to confirm that no communication is in progress (confirm that START = 0) and read the MWI_STATUS bit of the MWI_INTSTATUS register to confirm that no interrupt is being issued (confirm that MWI_STATUS = 0). If the settings of the MWI_CONT, MWI_CS0, MWI_CS1, or MWI_START register is changed during communication, the operation is not guaranteed.

2. When setting the START bit to 1 following communication completion and interrupt issuance, clear the interrupt for the previous communication before starting the next communication.

3. Before starting communication again, be sure to specify the transfer data for the corresponding registers.

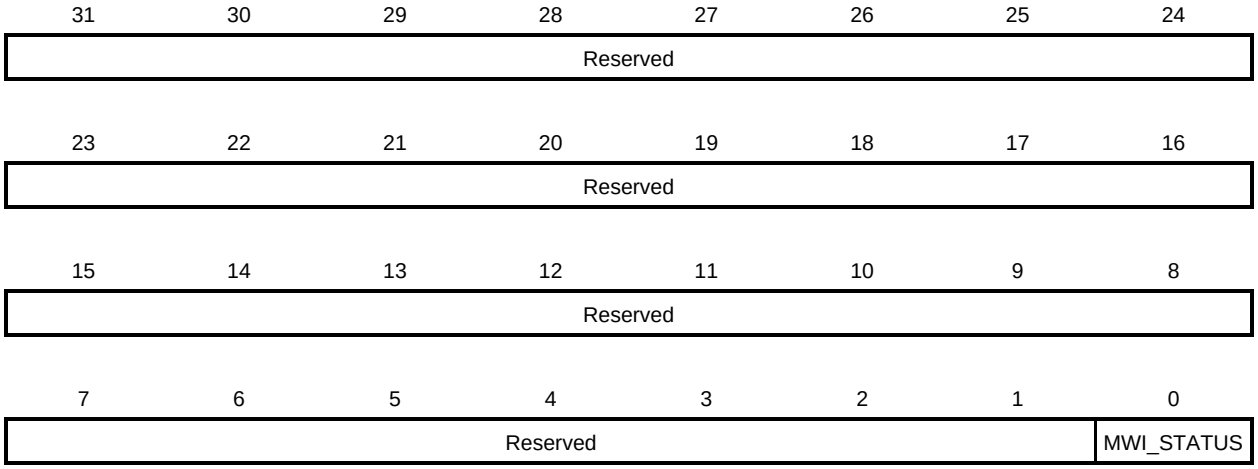
Example In data transmission mode: Specify data for the MWI_TXQA and MWI_TXQ registers.
In data reception mode: Specify data for the MWI_RXQ register.

4. If the communication mode is not set correctly or if the START bit is set to 1 while an interrupt is occurring, the START bit is not automatically cleared. In this case, manually write 0 to this bit.

3.2.5 Interrupt status register

This register (MWI_INTSTATUS: C016_0020H) indicates whether an interrupt has occurred after the completion of communication.

The register is enabled only if the issuance of interrupts is enabled by setting the MWI_ENSET bit of the MWI_INTENSET register to 1. Otherwise, the value of the MWI_STATUS bit is fixed to 0.

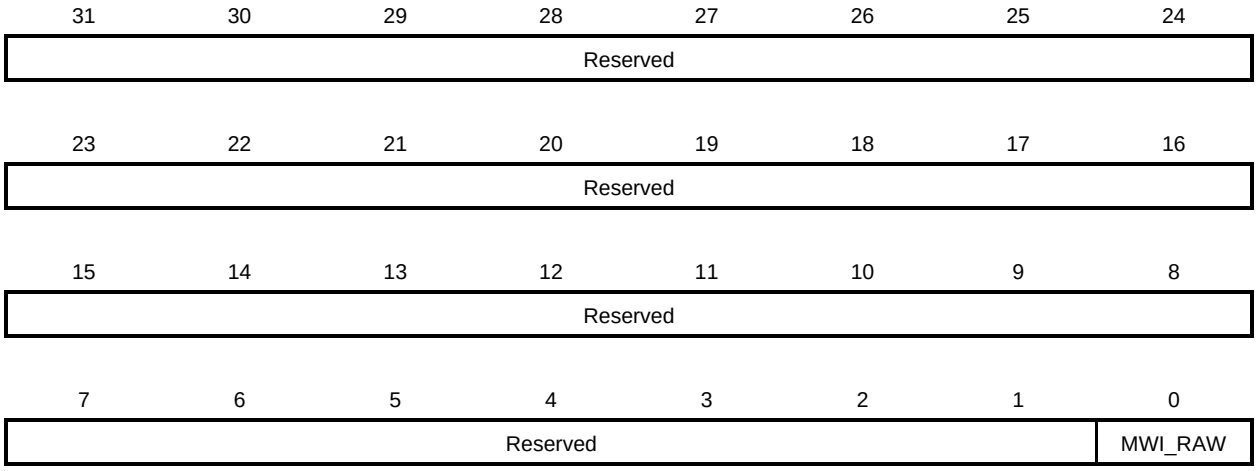


Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
MWI_STATUS	R	0	0	Indicates whether an interrupt has occurred. 0: No interrupt (default) 1: An interrupt has occurred.

3.2.6 Interrupt raw status register

This register (MWI_INTRAW: C016_0024H) indicates whether an interrupt has occurred, regardless of whether the issuance of interrupts is enabled in the MWI_INTENSET register.

This register is used mainly to confirm that no interrupt has occurred before starting communication.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
MWI_RAW	R	0	0	Indicates whether an interrupt has occurred. 0: No interrupt (default) 1: An interrupt has occurred.

3.2.7 Interrupt source clear register

This register (MWI_INTFFCLR: C016_0028H) clears the MWI_INTSTATUS and MWI_INTRAW registers.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							MWI_FFCLR

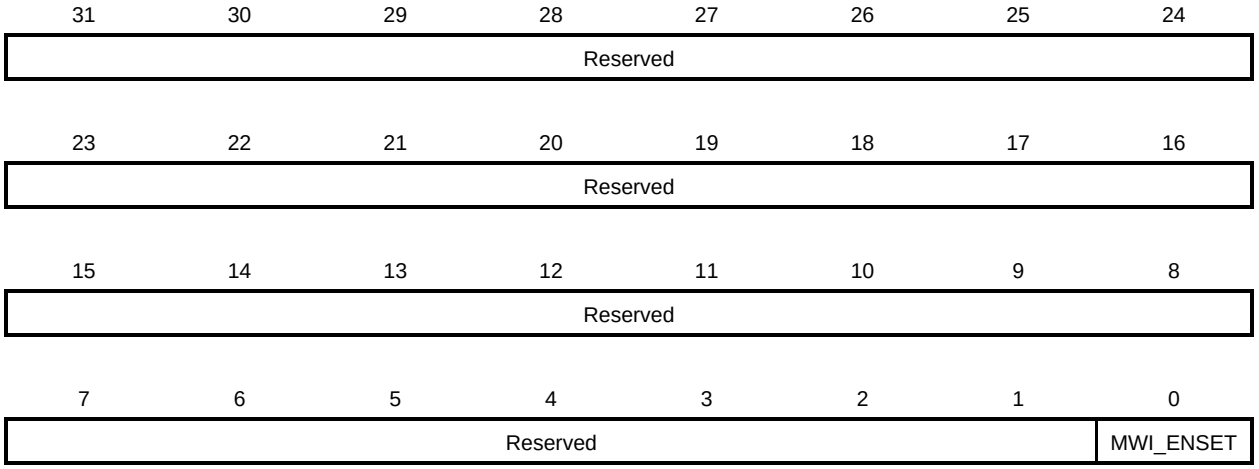
Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
MWI_FFCLR	W	0	0	Clears an interrupt. 0: Uses NOP to wait 1 clock cycle. (Default) 1: Clears an interrupt. This bit is cleared 1 clock cycle after being set to 1.

3.2.8 Interrupt enable set register

This register (MWI_INTENSET: C016_002CH) specifies whether to enable the issuance of interrupts after the completion of communication.

Write 1 to the MWI_ENSET bit to enable interrupts before starting communication.

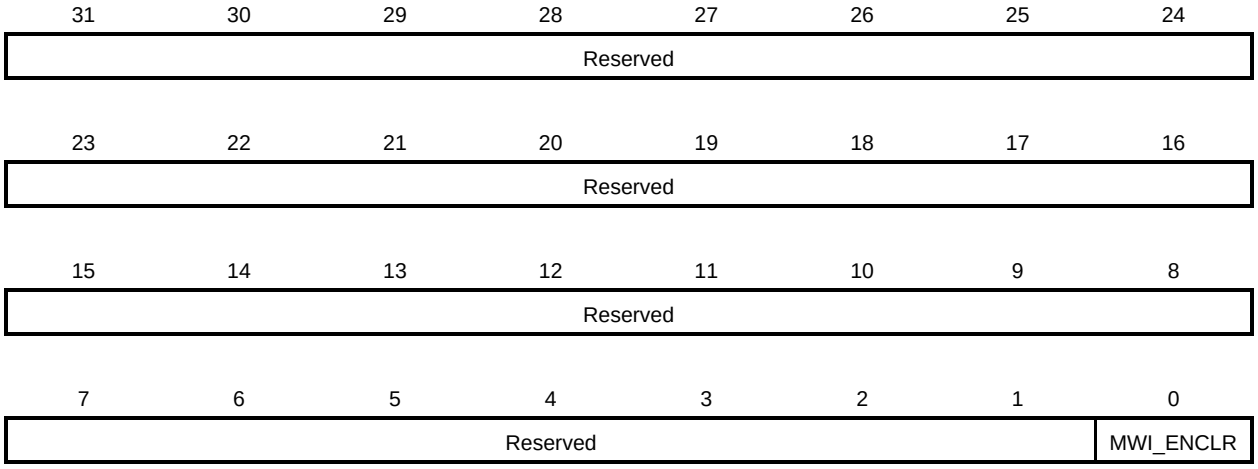
This register can be used to check whether the issuance of interrupts is enabled.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
MWI_ENSET	R/W	0	0	Specifies whether to enable the issuance of interrupts. 0: Disables the issuance of interrupts. (Default) 1: Enables the issuance of interrupts.

3.2.9 Interrupt enable clear register

This write-only register (MWI_INTENCLR: C016_0030H) disables the issuance of interrupts, which are enabled using the MWI_INTENSET register. When this register is read, 0 is returned.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
MWI_ENCLR	W	0	0	Specifies whether to disable the issuance of interrupts. 0: Keeps the current state. (Default) 1: Disables

3.2.10 Transmission address register

This register (MWI_TXQA: C016_0040H) stores the transmission address.

The bit width of this address can be specified using the BIT_ATX bit of the MWI_CONT register.

Written data whose bit width is greater than that specified by the BIT_ATX bit is ignored.

31	30	29	28	27	26	25	24
TXQA_31	TXQA_30	TXQA_29	TXQA_28	TXQA_27	TXQA_26	TXQA_25	TXQA_24

23	22	21	20	19	18	17	16
TXQA_23	TXQA_22	TXQA_21	TXQA_20	TXQA_19	TXQA_18	TXQA_17	TXQA_16

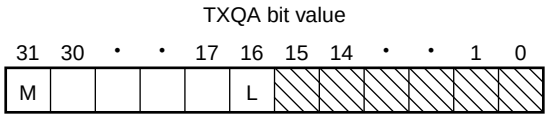
15	14	13	12	11	10	9	8
TXQA_15	TXQA_14	TXQA_13	TXQA_12	TXQA_11	TXQA_10	TXQA_9	TXQA_8

7	6	5	4	3	2	1	0
TXQA_7	TXQA_6	TXQA_5	TXQA_4	TXQA_3	TXQA_2	TXQA_1	TXQA_0

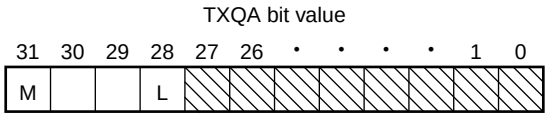
Name	R/W	Bit	After Reset	Function
TXQA_[31:0]	R/W	31:0	0000_0000H	Stores the transmission address.

Data is stored left-aligned in the MWI_TXQA register and output starting with the MSB (bit 31) when communication starts. Shift valid data towards the MSB before writing it.

Example BIT_ATX = 15 (16-bit data is output)



BIT_ATX = 3 (4-bit data is output)



Remarks 1. M = MSB, L = LSB

2. Because the previously-written transmission address and transmission data are retained, 0 is output from the bits that are not specified as valid by the BIT_ATX bit (transmission address width) and the BIT_DTX bit (transmission data width) of the MWI_CONT register.

3.2.11 Transmission data register

This register (MWI_TXQ: C016_0050H) stores the transmission data.

The bit width of this data can be specified using the BIT_DTX bit of the MWI_CONT register.

Written data whose bit width is greater than that specified by the BIT_DTX bit is ignored.

31	30	29	28	27	26	25	24
TXQD_31	TXQD_30	TXQD_29	TXQD_28	TXQD_27	TXQD_26	TXQD_25	TXQD_24

23	22	21	20	19	18	17	16
TXQD_23	TXQD_22	TXQD_21	TXQD_20	TXQD_19	TXQD_18	TXQD_17	TXQD_16

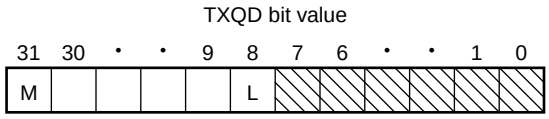
15	14	13	12	11	10	9	8
TXQD_15	TXQD_14	TXQD_13	TXQD_12	TXQD_11	TXQD_10	TXQD_9	TXQD_8

7	6	5	4	3	2	1	0
TXQD_7	TXQD_6	TXQD_5	TXQD_4	TXQD_3	TXQD_2	TXQD_1	TXQD_0

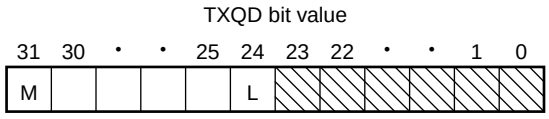
Name	R/W	Bit	After Reset	Function
TXQD_[31:0]	R/W	31:0	0000_0000H	stores transmission data.

Data is stored left-aligned in the MWI_TXQ register and output starting with the MSB (bit 31) when communication starts.

Example BIT_DTX = 23 (24-bit data is output)



BIT_DTX = 7 (8-bit data is output)



Remarks 1. M = MSB, L = LSB

2. Because the previously-written transmission address and transmission data are retained, 0 is output from the bits that are not specified as valid by the BIT_ATX bit (transmission address width) and the BIT_DTX bit (transmission data width) of the MWI_CONT register.

3.2.12 Reception data register

This register (MWI_RXQ: C016_0060H) stores the data received through serial communication.

The bit width of the received data can be specified using the BIT_RX bit of the MWI_CONT register. Zeros are input to bits that are not specified as valid by the BIT_RX bit.

31	30	29	28	27	26	25	24
RXQ_31	RXQ_30	RXQ_29	RXQ_28	RXQ_27	RXQ_26	RXQ_25	RXQ_24

23	22	21	20	19	18	17	16
RXQ_23	RXQ_22	RXQ_21	RXQ_20	RXQ_19	RXQ_18	RXQ_17	RXQ_16

15	14	13	12	11	10	9	8
RXQ_15	RXQ_14	RXQ_13	RXQ_12	RXQ_11	RXQ_10	RXQ_9	RXQ_8

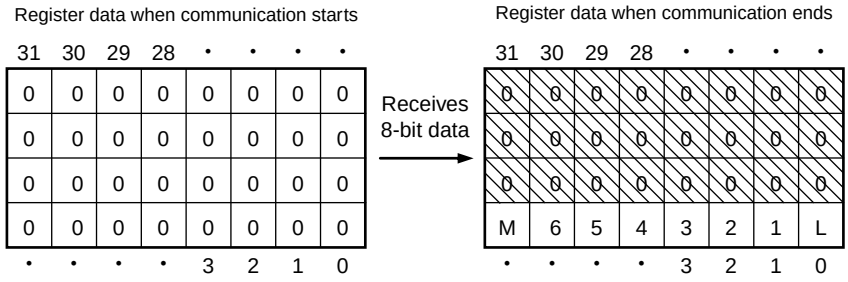
7	6	5	4	3	2	1	0
RXQ_7	RXQ_6	RXQ_5	RXQ_4	RXQ_3	RXQ_2	RXQ_1	RXQ_0

Name	R/W	Bit	After Reset	Function
RXQ_[31:0]	R	31:0	0000_0000H	Stores received data.

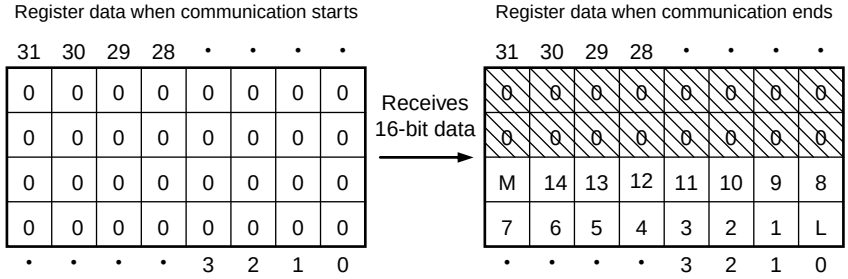
Received data that has a bit width specified by the BIT_RX bit of the MWI_CONT register is stored in the MWI_RXQ register. Any bit width from 1(00H) to 32 bits (1FH) can be selected. Data is stored right-aligned.

When the START bit of the MWI_START register is set to 1, 0 is temporarily assigned to all bits of the MWI_RXQ register. After reception is complete, any received data can be read, if any.

Example BIT_RX = 7 (reception of 8-bit data)



BIT_RX = 15 (reception of 16-bit data)



CHAPTER 4 DESCRIPTION OF FUNCTIONS

4.1 Operation Timing

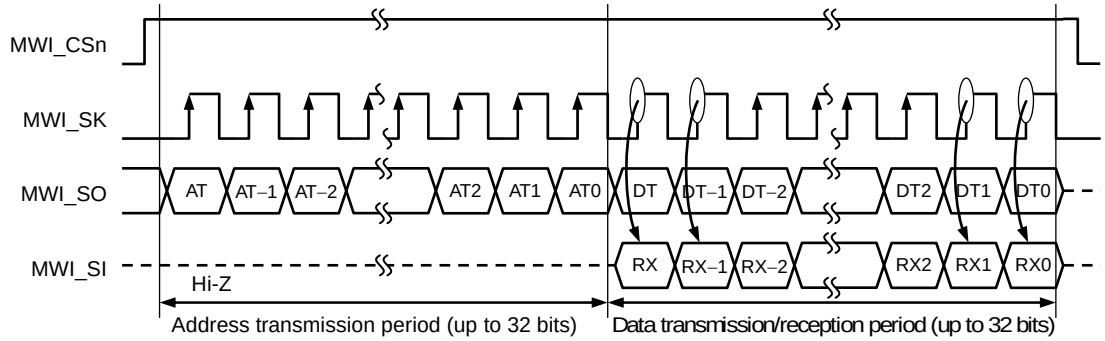
4.1.1 Transmission at the falling edge and reception at the rising edge

Figure 4-1 shows an example of operation when the RX_EDGEn bit is set to 0 and the TX_EDGEn bit is set to 1 in the MWI_CSn register (default settings).

The transmission device starts outputting data from the MWI_SO pin, triggered by a falling clock edge.

The reception device samples and captures the data from the MWI_SI pin at the rising edge of the clock.

Figure 4-1. MWI Serial Transfer Timing (Transmission at the Falling Edge and Reception at the Rising Edge)



Remarks 1. It is assumed that the slave device on the transmission side samples and captures data at the rising edge.

2. It is assumed that the slave device on the reception side starts data transmission triggered by a falling edge.

3. The symbols in the above figure refer to the following parameters:

AT: BIT_ATX (transmission address data width)

DT: BIT_DTX (transmission data width)

RX: BIT_RX (received data width)

$0 \leq AT < 32$, $0 \leq DT < 32$, $0 \leq RX < 32$

4. n = 0, 1

(1) Data transmission mode (single/burst transfer)

In the case shown in Figure 4-1, up to 31 bits can be specified for AT and DT.

During this operation, data is not input to the MWI_SI pin. The address (AT) and data (DT) are transmitted.

(2) Data reception mode (single/burst transfer)

In the case shown in Figure 4-1, up to 31 bits can be specified for AT and RX.

During this operation, data (DT) is not output from the MWI_SO pin. The address (AT) is transmitted and the corresponding data (RX) is received.

(3) Concurrent data transmission/reception mode (single/burst transfer)

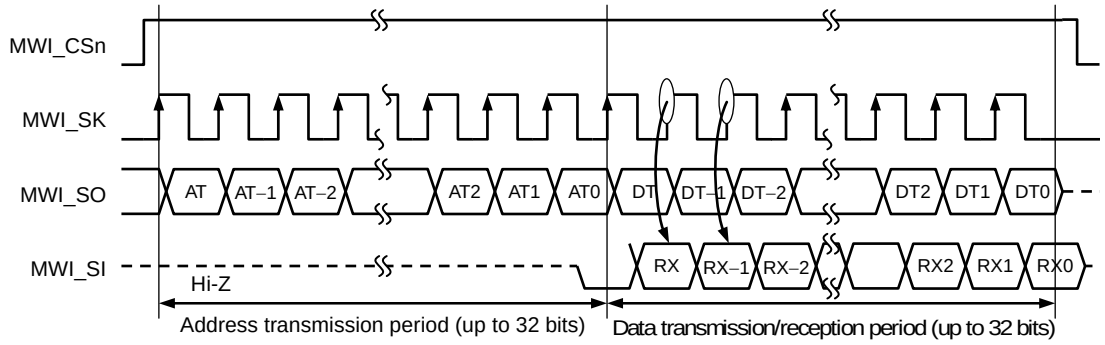
In the case shown in Figure 4-1, up to 31 bits can be specified for RX and DT.

During this operation, no address is transmitted and only the data of the bit width equivalent to that of the address is concurrently transmitted and received.

4.1.2 Transmission and reception at the rising edge

Figure 4-2 shows an example of operation when the RX_EDGEn and TX_EDGEn bits are set to 0 in the MWI_CSn register.

Figure 4-2. MWI Serial Transfer Timing (Transmission and Reception at the Rising Edge)

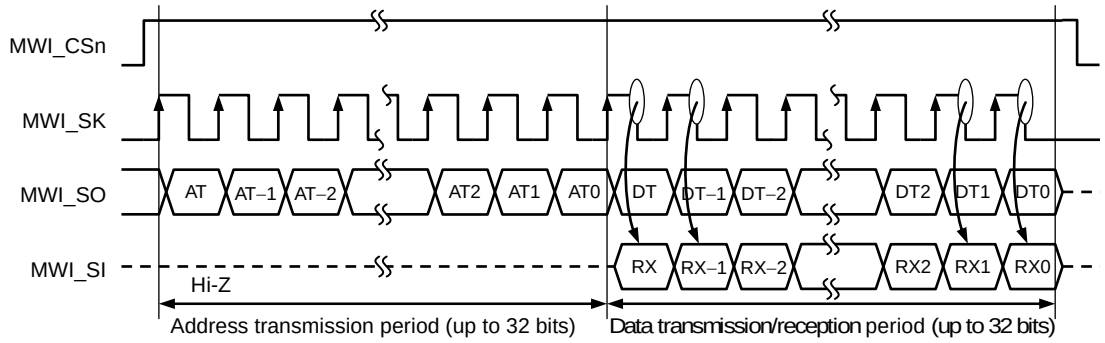


Remark n = 0, 1

4.1.3 Transmission at the rising edge and reception at the falling edge

Figure 4-3 shows an example of operation when the RX_EDGEn bit is set to 1 and the TX_EDGEn bit is set to 0 in the MWI_CSn register.

Figure 4-3. MWI Serial Transfer Timing (Transmission at the Rising Edge and Reception at the Falling Edge)

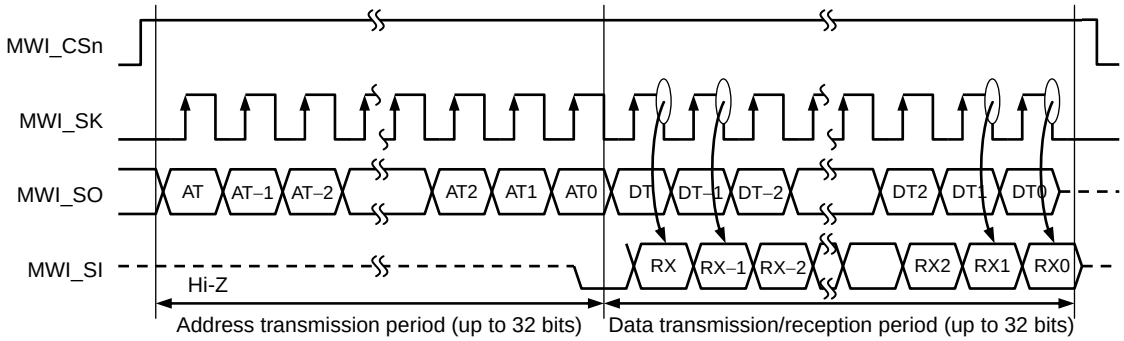


Remark n = 0, 1

4.1.4 Transmission and reception at the falling edge

Figure 4-4 shows an example of operation when the RX_EDGEn and TX_EDGEn bits are set to 1 in the MWI_CSn register.

Figure 4-4. MWI Serial Transfer Timing (Transmission and Reception at the Falling Edge)



Remark n = 0, 1

4.2 Clocks and Reset

The following clocks are used for the MICROWIRE interface.

(1) MIW_SCLK (serial clock)

Used for the internal operation of the MICROWIRE interface.

(2) MIW_PCLK (APB clock)

Used for accessing the registers on the APB bus.

For details about clock and reset settings, see the **Multimedia Processor for Mobile Applications - System Control/General-Purpose I/O Interface User's Manual (S19265E)**.

4.3 Interrupt Source

The MICROWIRE interface uses the following interrupt.

Table 4-1. Interrupt Source

Interrupt Type	When to Issue	Bit Assignment
Transfer completion interrupt	This interrupt is Issued when a transfer is completed.	Bit 0 (MWI_STATUS) of the MWI_INTSTATUS register

CHAPTER 5 USAGE

5.1 Initial Status (After a Reset)

The MICROWIRE registers are initialized to the following settings after a reset.

- MWI_CONT register (Initial value: 0000_0000H)
  - CS0 = 0 The MWI_CS0 signal is inactive.
  - CS1 = 0 The MWI_CS1 signal is inactive.
  - RX_EN = 0 Reception is disabled.
  - TX_EN = 0 Transmission is disabled.
  - BITRX_EN = 0 The bit width specified for received data is disabled.
  - BIT_RX = 0 The bit width of received data is 0.
  - BITATX_EN = 0 The bit width specified for the transmission address is disabled.
  - BIT_ATX = 0 The bit width of the transmission address is 0.
  - BITDTX_EN = 0 The bit width specified for transmission data is disabled.
  - BIT_DTX = 0 The bit width of transmission data is 0.

- MWI_CS0 register (Initial value: 0000_0001H)
  - RX_EDGE0 = 0 Rising edge of reception clock
  - TX_EDGE0 = 1 Falling edge of transmission clock

- MWI_CS1 register (Initial value: 0000_0001H)
  - RX_EDGE1 = 0 Rising edge of reception clock
  - TX_EDGE1 = 1 Falling edge of transmission clock

- MWI_START register (Initial value: 0000_0000H)
  - START = 0 No communication has started.

- MWI_INTENSET register (Initial value: 0000_0000H)
  - MWI_ENSET = 0 The interrupts are disabled.

- MWI_TXQA register (Initial value: 0000_0000H)
  - TXQA = 0 There is no transmission address.

- MWI_TXQ register (Initial value: 0000_0000H)
  - TXQD = 0 There is no transmission data.

Caution Set up the CS1 and CS0 bits of the MWI_CONT register so that both the MWI_CS1 and MWI_CS0 signals become inactive after a reset.

5.2 Data Transmission Mode

The examples below assume the MICROWIRE interface is used under the following conditions:

- The active level of the MWI_CS0 signal is 1.
- The active level of the MWI_CS1 signal is 0.
- CS0 is used.
- Transmission address width = 8
- Transmission data width = 8
- Transmission clock output trigger edge = Falling edge
- Reception clock sampling edge = Rising edge

5.2.1 Settings common to single and burst transfer

The common procedure for single and burst transfer is shown below.

(1) Communication setup

Caution Make sure that no interrupt is being issued before specifying these settings.

<1> Specify the settings for CS0 and CS1 are as follows:

MWI_CONT register (Written data value: 0000_0038H)

- CS0_EN = 1 Writing to the CS0 bit is enabled.
- CS1_EN = 1 Writing to the CS1 bit is enabled.
- CS0 = 0 The MWI_CS0 signal is inactive.
- CS1 = 1 The MWI_CS1 signal is inactive.
- RX_EN = 0 Reception is disabled.
- TX_EN = 0 Transmission is disabled.
- BITRX_EN = 0 The bit width specified for received data is disabled.
- BIT_RX = 0 The bit width of received data is 0.
- BITATX_EN = 0 The bit width specified for the transmission address is disabled.
- BIT_ATX = 0 The bit width of the transmission address is 0.
- BITDTX_EN = 0 The bit width specified for transmission data is disabled.
- BIT_DTX = 0 The bit width of transmission data is 0.

<2> Select the rising or falling edge of the transmission and reception clocks.

MWI_CS0 register (Written data value: 0000_0001H)

- RX_EDGE0 = 0 Rising edge of reception clock
- TX_EDGE0 = 1 Falling edge of transmission clock

Caution Be sure to perform steps <1> and <2> first after a reset. For the second and subsequent transmission or reception, specify the setting in <3> and the following.

<3> Prepare for transmission.

MWI_CONT register (Written data value: 0027_2715H)

- CS0_EN = 1 Writing to the CS0 bit is enabled.
- CS1_EN = 0 Writing to the CS1 bit is disabled.
- CS0 = 1 The MWI_CS0 signal is asserted.
- CS1 = 1 The MWI_CS1 signal is inactive.
- RX_EN = 0 Reception is disabled.
- TX_EN = 1 Transmission is enabled.
- BITRX_EN = 0 The bit width specified for received data is disabled.
- BIT_RX = 0 The bit width of received data is 0.
- BITATX_EN = 1 The bit width specified for the transmission address is enabled.
- BIT_ATX = 7 The bit width of the transmission address is set to 8.
- BITDTX_EN = 1 The width specified for transmission data is enabled.
- BIT_DTX = 7 The bit width of transmission data is set to 8.

<4> Write the transmission address.

MWI_TXQA register (Written data value: any 8-bit value)

- TXQA = any 8-bit value 8-bit transmission address

<5> Write transmission data.

MWI_TXQ register (Written data value: any 8-bit value)

- TXQD = any 8-bit value 8-bit transmission data

<6> Enable issuance of the communication completion interrupt.

MWI_INTENSET register (Written data value: 0000_0001H)

- MWI_ENSET = 1 The interrupt is enabled.

<7> Start communication.

MWI_START register (Written data value: 0000_0001H)

- START = 1 Communication starts.

(2) Communication end

A transmission completion interrupt occurs.

<8> Clear the interrupt.

MWI_INTFFCLR register (Written data value: 0000_0001H)

- MWI_FFCLR = 1 The interrupt source is cleared.

<9> Make sure that no interrupt is being issued.

MWI_INTSTATUS register (read data value: 0000_0000H)

- Make sure that the MWI_STATUS bit is set to 0.

5.2.2 Single transfer setup

Steps <1> to <9> are the same as those described in **5.2.1 Settings common to single and burst transfer**.

(1) Communication end

<10> Disable the interrupt.

MWI_INTENCLR register (Written data value: 0000_0000H)

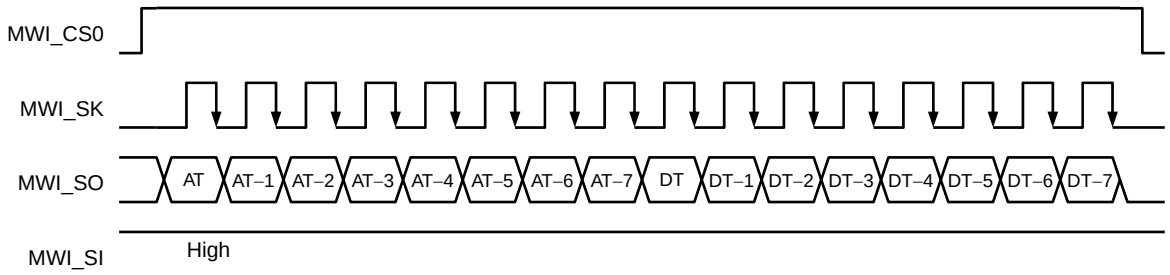
- MWI_ENCLR = 0 The interrupt is disabled.

<11> Reset the MWI_CONT register (deassert NWI_CS0).

MWI_CONT register (Written data value: 0000_0010H)

- CS0_EN = 1 Writing to the CS0 bit is enabled.
- CS1_EN = 0 Writing to the CS1 bit is disabled.
- CS0 = 0 The MWI_CS0 signal is deasserted.
- CS1 = 1 The MWI_CS1 signal is inactive.
- RX_EN = 0 Reception is disabled.
- TX_EN = 0 Transmission is disabled.
- BITRX_EN = 0 The bit width specified for received data is disabled.
- BIT_RX = 0 The bit width of received data is 0.
- BITATX_EN = 0 The bit width specified for the transmission address is disabled.
- BIT_ATX = 0 The bit width of the transmission address is set to 0.
- BITDTX_EN = 0 The bit width specified for the transmission data is disabled.
- BIT_DTX = 0 The bit width of transmission data is set to 0.

Figure 5-1. Data Transmission Timing (During a Single Transfer)



5.2.3 Burst transfer setup

Steps <1> to <9> are the same as those described in **5.2.1 Settings common to single and burst transfer**.

(1) Communication setup

<10> Write the transmission address.

MWI_TXQA register (Written data value: any 8-bit value)

- TXQA = any 8-bit value 8-bit transmission address

<11> Write transmission data.

MWI_TXQ register (Written data value: any 8-bit value)

- TXQD = any 8-bit value 8-bit transmission data

<12> Start communication.

MWI_START register (Written data value: 0000_0001H)

- START = 1 Communication starts.

(2) Communication end

A transmission completion interrupt occurs.

<13> Clear the interrupt.

MWI_INTFFCLR register (Written data value: 0000_0001H)

- MWI_FFCLR = 1 The interrupt source is cleared.

<14> Make sure that no interrupt is being issued.

MWI_INTSTATUS register (read data value: 0000_0000H)

- Make sure that the MWI_STATUS bit is set to 0.

Remark If communication is executed three or more times, repeat <10> to <14>.

<15> Disable the interrupt.

MWI_INTENCLR register (Written data value: 0000_0000H)

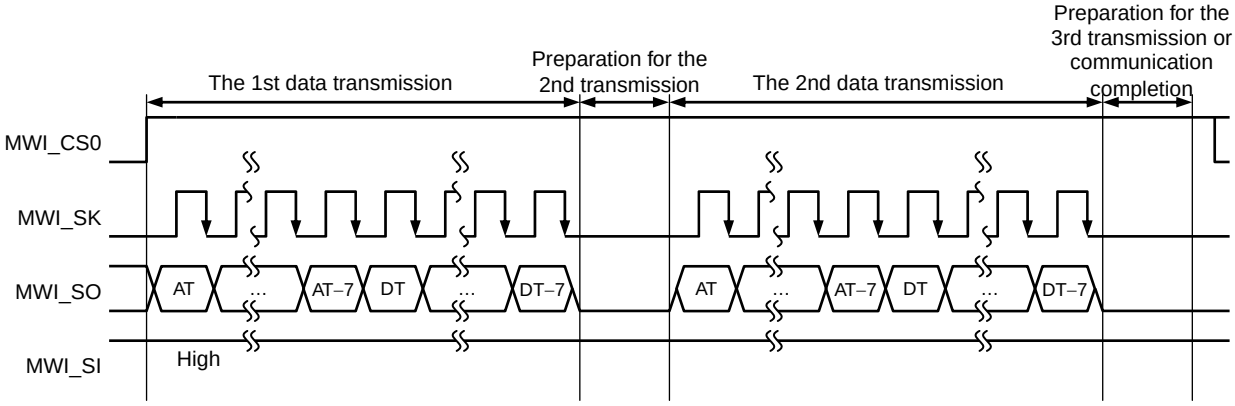
- MWI_ENCLR = 0 The interrupt is disabled.

<16> Reset the MWI_CONT register (deassert NWI_CS0).

MWI_CONT register (Written data value: 0000_0010H)

- CS0_EN = 1 Writing to the CS0 bit is enabled.
- CS1_EN = 0 Writing to the CS1 bit is disabled.
- CS0 = 0 The MWI_CS0 signal is deasserted.
- CS1 = 1 The MWI_CS1 signal is inactive.
- RX_EN = 0 Reception is disabled.
- TX_EN = 0 Transmission is disabled.
- BITRX_EN = 0 The bit width specified for received data is disabled.
- BIT_RX = 0 The bit width of received data is 0.
- BITATX_EN = 0 The bit width specified for the transmission address is disabled.
- BIT_ATX = 0 The bit width of the transmission address is set to 0.
- BITDTX_EN = 0 The bit width specified for the transmission data is disabled.
- BIT_DTX = 0 The bit width of transmission data is set to 0.

Figure 5-2. Data Transmission Timing (During a Burst Transfer)



5.3 Data Reception Mode

The examples below assume the MICROWIRE interface is used under the following conditions:

- The active level of the MWI_CS0 signal is 0.
- The active level of the MWI_CS1 signal is 1.
- CS1 is used.
- Transmission address width = 8
- Transmission data width = 8
- Transmission clock output trigger edge = Falling edge
- Reception clock sampling edge = Falling edge

5.3.1 Settings common to single and burst transfer

The common procedure for single and burst transfer is shown below.

(1) Communication setup

Caution Make sure that no interrupt is being issued before specifying these settings.

<1> Specify the settings for CS0 and CS1 are as follows:

MWI_CONT register (Written data value: 0000_0034H)

- CS0_EN = 1 Writing to the CS0 bit is enabled.
- CS1_EN = 1 Writing to the CS1 bit is enabled.
- CS0 = 1 The MWI_CS0 signal is inactive.
- CS1 = 0 The MWI_CS1 signal is inactive.
- RX_EN = 0 Reception is disabled.
- TX_EN = 0 Transmission is disabled.
- BITRX_EN = 0 The bit width specified for received data is disabled.
- BIT_RX = 0 The bit width of received data is 0.
- BITATX_EN = 0 The bit width specified for the transmission address is disabled.
- BIT_ATX = 0 The bit width of the transmission address is 0.
- BITDTX_EN = 0 The bit width specified for transmission data is disabled.
- BIT_DTX = 0 The bit width of transmission data is 0.

<2> Select the rising or falling edge of the transmission and reception clocks.

MWI_CS1 register (Written data value: 0000_0003H)

- RX_EDGE1 = 1 Falling edge of reception clock
- TX_EDGE1 = 1 Falling edge of transmission clock

Caution Be sure to perform steps <1> and <2> first after a reset. For the second and subsequent transmission or reception, specify the setting in <3> and the following.

<3> Prepare for transmission.

MWI_CONT register (Written data value: 2727_002BH)

- CS0_EN = 0 Writing to the CS0 bit is disabled.
- CS1_EN = 1 Writing to the CS1 bit is enabled.
- CS0 = 1 The MWI_CS0 signal is inactive.
- CS1 = 1 The MWI_CS1 signal is asserted.
- RX_EN = 1 Reception is enabled.
- TX_EN = 1 Transmission is enabled.
- BITRX_EN = 1 The bit width specified for received data is enabled.
- BIT_RX = 7 The bit width of received data is set to 8.
- BITATX_EN = 1 The bit width specified for the transmission address is enabled.
- BIT_ATX = 7 The bit width of the transmission address is set to 8.
- BITDTX_EN = 0 The bit width specified for transmission data is disabled.
- BIT_DTX = 0 The bit width of transmission data is 0.

<4> Write the transmission address.

MWI_TXQA register (Written data value: any 8-bit value)

- TXQA = any 8-bit value 8-bit transmission address

<5> Enable issuance of the communication completion interrupt.

MWI_INTENSET register (Written data value: 0000_0001H)

- MWI_ENSET = 1 The interrupt is enabled.

<6> Start communication.

MWI_START register (Written data value: 0000_0001H)

- START = 1 Communication starts.

(2) Communication end

A transmission completion interrupt occurs.

<7> Read the received data.

MWI_RXQ register (read data value)

- RXQ = Read data 8-bit data

<8> Clear the interrupt.

MWI_INTFFCLR register (Written data value: 0000_0001H)

- MWI_FFCLR = 1 The interrupt source is cleared.

<9> Make sure that no interrupt is being issued.

MWI_INTSTATUS register (read data value: 0000_0000H)

- Make sure that the MWI_STATUS bit is set to 0.

5.3.2 Single transfer setup

Steps <1> to <9> are the same as those described in **5.3.1 Settings common to single and burst transfer**.

(1) Communication end

<10> Disable the interrupt.

MWI_INTENCLR register (Written data value: 0000_0000H)

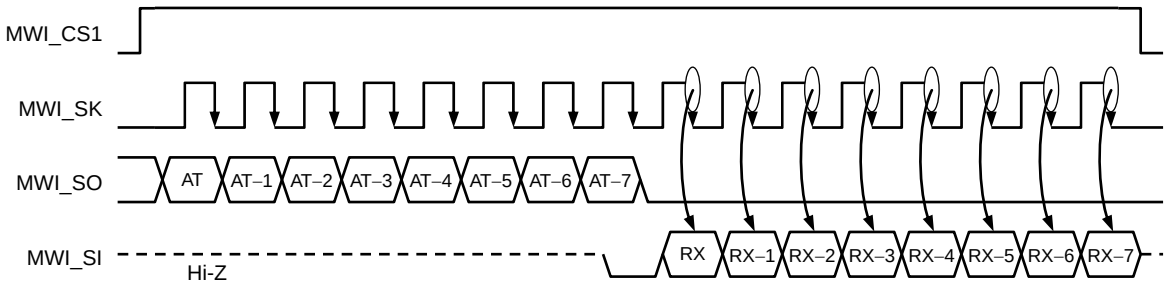
- MWI_ENCLR = 0 The interrupt is disabled.

<11> Reset the MWI_CONT register (deassert NWI_CS1).

MWI_CONT register (Written data value: 0000_0020H)

- CS0_EN = 0 Writing to the CS0 bit is disabled.
- CS1_EN = 1 Writing to the CS1 bit is enabled.
- CS0 = 1 The MWI_CS0 signal is inactive.
- CS1 = 0 The MWI_CS1 signal is deasserted.
- RX_EN = 0 Reception is disabled.
- TX_EN = 0 Transmission is disabled.
- BITRX_EN = 0 The bit width specified for received data is disabled.
- BIT_RX = 0 The bit width of received data is set to 0.
- BITATX_EN = 0 The bit width specified for the transmission address is disabled.
- BIT_ATX = 0 The bit width of the transmission address is set to 0.
- BITDTX_EN = 0 The bit width specified for transmission data is disabled.
- BIT_DTX = 0 The bit width of transmission data is 0.

Figure 5-3. Data Reception Timing (During a Single Transfer)



5.3.3 Burst transfer setup

Steps <1> to <9> are the same as those described in **5.3.1 Settings common to single and burst transfer**.

(1) Communication setup

<10> Write the transmission address.

MWI_TXQA register (Written data value: any 8-bit value)

- TXQA = any 8-bit value 8-bit transmission address

<11> Start communication.

MWI_START register (Written data value: 0000_0001H)

- START = 1 Communication starts.

(2) Communication end

A transmission completion interrupt occurs.

<12> Read the received data.

MWI_RXQ register (read data value)

- RXQ = Read data 8-bit data

<13> Clear the interrupt.

MWI_INTFFCLR register (Written data value: 0000_0001H)

- MWI_FFCLR = 1 The interrupt source is cleared.

<14> Make sure that no interrupt is being issued.

MWI_INTSTATUS register (read data value: 0000_0000H)

- Make sure that the MWI_STATUS bit is set to 0.

Remark If communication is executed three or more times, repeat <10> to <14>.

<15> Disable the interrupt.

MWI_INTENCLR register (Written data value: 0000_0000H)

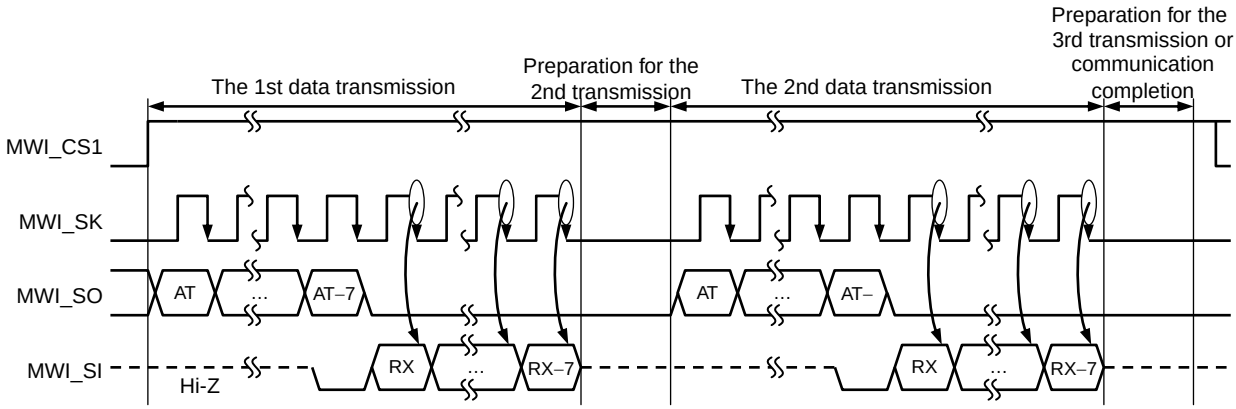
- MWI_ENCLR = 0 The interrupt is disabled.

<16> Reset the MWI_CONT register (deassert NWI_CS1).

MWI_CONT register (Written data value: 0000_0020H)

- CS0_EN = 0 Writing to the CS0 bit is disabled.
- CS1_EN = 1 Writing to the CS1 bit is enabled.
- CS0 = 1 The MWI_CS0 signal is inactive.
- CS1 = 0 The MWI_CS1 signal is deasserted.
- RX_EN = 0 Reception is disabled.
- TX_EN = 0 Transmission is disabled.
- BITRX_EN = 0 The bit width specified for received data is disabled.
- BIT_RX = 0 The bit width of received data is set to 0.
- BITATX_EN = 0 The bit width specified for the transmission address is disabled.
- BIT_ATX = 0 The bit width of the transmission address is set to 0.
- BITDTX_EN = 0 The bit width specified for transmission data is disabled.
- BIT_DTX = 0 The bit width of transmission data is 0.

Figure 5-4. Data Reception Timing (During a Burst Transfer)



5.4 Concurrent Data Transmission/Reception Mode

The examples below assume the MICROWIRE interface is used under the following conditions:

- The active level of the MWI_CS0 signal is 1.
- The active level of the MWI_CS1 signal is 1.
- CS0 is used.
- Transmission address width = 8
- Transmission data width = 8
- Transmission clock output trigger edge = Falling edge
- Reception clock sampling edge = Rising edge

5.4.1 Settings common to single and burst transfer

The common procedure for single and burst transfer is shown below.

(1) Communication setup

Caution Make sure that no interrupt is being issued before specifying these settings.

<1> Specify the settings for CS0 and CS1 are as follows:

MWI_CONT register (Written data value: 0000_0030H)

- CS0_EN = 1 Writing to the CS0 bit is enabled.
- CS1_EN = 1 Writing to the CS1 bit is enabled.
- CS0 = 0 The MWI_CS0 signal is inactive.
- CS1 = 0 The MWI_CS1 signal is inactive.
- RX_EN = 0 Reception is disabled.
- TX_EN = 0 Transmission is disabled.
- BITRX_EN = 0 The bit width specified for received data is disabled.
- BIT_RX = 0 The bit width of received data is 0.
- BITATX_EN = 0 The bit width specified for the transmission address is disabled.
- BIT_ATX = 0 The bit width of the transmission address is 0.
- BITDTX_EN = 0 The bit width specified for transmission data is disabled.
- BIT_DTX = 0 The bit width of transmission data is 0.

<2> Select the rising or falling edge of the transmission and reception clocks.

MWI_CS0 register (Written data value: 0000_0001H)

- RX_EDGE0 = 0 Rising edge of reception clock
- TX_EDGE0 = 1 Falling edge of transmission clock

Caution Be sure to perform steps <1> and <2> first after a reset. For the second and subsequent transmission or reception, specify the setting in <3> and the following.

<3> Prepare for transmission.

MWI_CONT register (Written data value: 2700_2717H)

- CS0_EN = 1 Writing to the CS0 bit is enabled.
- CS1_EN = 0 Writing to the CS1 bit is disabled.
- CS0 = 1 The MWI_CS0 signal is asserted.
- CS1 = 0 The MWI_CS1 signal is inactive.
- RX_EN = 1 Reception is enabled.
- TX_EN = 1 Transmission is enabled.
- BITRX_EN = 1 The bit width specified for received data is enabled.
- BIT_RX = 7 The bit width of received data is set to 8.
- BITATX_EN = 0 The bit width specified for the transmission address is disabled.
- BIT_ATX = 0 The bit width of the transmission address is 0.
- BITDTX_EN = 1 The bit width specified for transmission data is enabled.
- BIT_DTX = 7 The bit width of transmission data is set to 8.

<4> Write transmission data.

MWI_TXQ register (Written data value: any 8-bit value)

- TXQ = any 8-bit value 8-bit transmission data

<5> Enable issuance of the communication completion interrupt.

MWI_INTENSET register (Written data value: 0000_0001H)

- MWI_ENSET = 1 The interrupt is enabled.

<6> Start communication.

MWI_START register (Written data value: 0000_0001H)

- START = 1 Communication starts.

(2) Communication end

A transmission completion interrupt occurs.

<7> Read the received data.

MWI_RXQ register (read data value)

- RXQ = Read data 8-bit data

<8> Clear the interrupt.

MWI_INTFFCLR register (Written data value: 0000_0001H)

- MWI_FFCLR = 1 The interrupt source is cleared.

<9> Make sure that no interrupt is being issued.

MWI_INTSTATUS register (read data value: 0000_0000H)

- Make sure that the MWI_STATUS bit is set to 0.

5.4.2 Single transfer setup

Steps <1> to <9> are the same as those described in **5.4.1 Settings common to single and burst transfer**.

(1) Communication end

<10> Disable the interrupt.

MWI_INTENCLR register (Written data value: 0000_0000H)

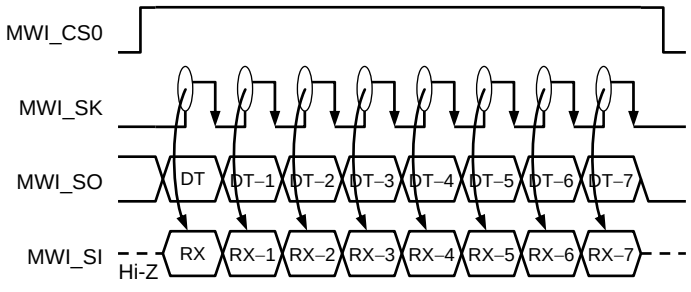
- MWI_ENCLR = 0 The interrupt is disabled.

<11> Reset the MWI_CONT register (deassert NWI_CS0).

MWI_CONT register (Written data value: 0000_0010H)

- CS0_EN = 1 Writing to the CS0 bit is enabled.
- CS1_EN = 0 Writing to the CS1 bit is disabled.
- CS0 = 0 The MWI_CS0 signal is deasserted.
- CS1 = 0 The MWI_CS1 signal is inactive.
- RX_EN = 0 Reception is disabled.
- TX_EN = 0 Transmission is disabled.
- BITRX_EN = 0 The bit width specified for received data is disabled.
- BIT_RX = 0 The bit width of received data is set to 0.
- BITATX_EN = 0 The bit width specified for the transmission address is disabled.
- BIT_ATX = 0 The bit width of the transmission address is 0.
- BITDTX_EN = 0 The bit width specified for the transmission data is disabled.
- BIT_DTX = 0 The bit width of transmission data is set to 0.

Figure 5-5. Concurrent Data Transmission/Reception Timing (During a Single Transfer)



5.4.3 Burst transfer setup

Steps <1> to <9> are the same as those described in **5.4.1 Settings common to single and burst transfer**.

(1) Communication setup

<10> Write transmission data.

MWI_TXQ register (Written data value: any 8-bit value)

- TXQD = any 8-bit value 8-bit transmission data

<11> Start communication.

MWI_START register (Written data value: 0000_0001H)

- START = 1 Communication starts.

(2) Communication end

A transmission completion interrupt occurs.

<12> Read the received data.

MWI_RXQ register (read data value)

- RXQ = Read data 8-bit data

<13> Clear the interrupt.

MWI_INTFFCLR register (Written data value: 0000_0001H)

- MWI_FFCLR = 1 The interrupt source is cleared.

<14> Make sure that no interrupt is being issued.

MWI_INTSTATUS register (read data value: 0000_0000H)

- Make sure that the MWI_STATUS bit is set to 0.

Remark If communication is executed three or more times, repeat <10> to <14>.

<15> Disable the interrupt.

MWI_INTENCLR register (Written data value: 0000_0000H)

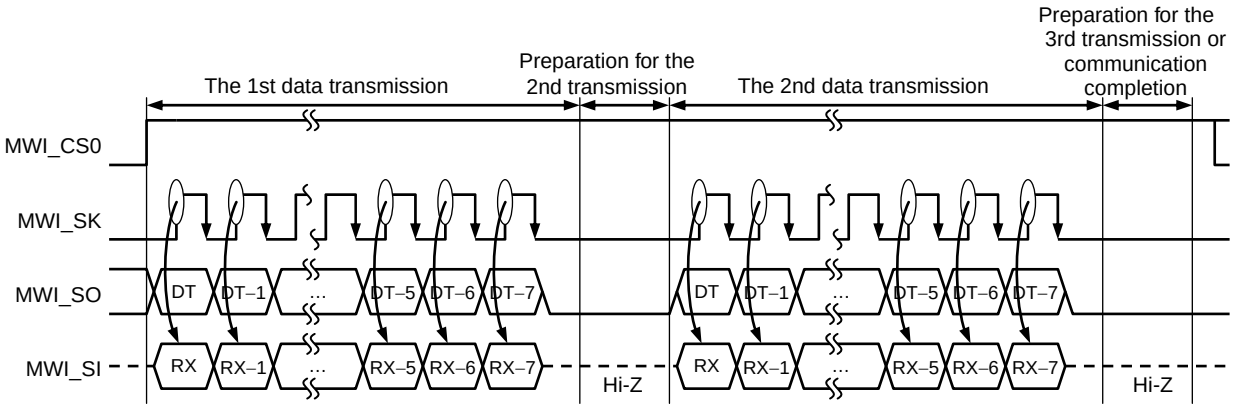
- MWI_ENCLR = 0 The interrupt is disabled.

<16> Reset the MWI_CONT register (deassert NWI_CS0).

MWI_CONT register (Written data value: 0000_0010H)

- CS0_EN = 1 Writing to the CS0 bit is enabled.
- CS1_EN = 0 Writing to the CS1 bit is disabled.
- CS0 = 0 The MWI_CS0 signal is deasserted.
- CS1 = 0 The MWI_CS1 signal is inactive.
- RX_EN = 0 Reception is disabled.
- TX_EN = 0 Transmission is disabled.
- BITRX_EN = 0 The bit width specified for received data is disabled.
- BIT_RX = 0 The bit width of received data is set to 0.
- BITATX_EN = 0 The bit width specified for the transmission address is disabled.
- BIT_ATX = 0 The bit width of the transmission address is 0.
- BITDTX_EN = 0 The bit width specified for the transmission data is disabled.
- BIT_DTX = 0 The bit width of transmission data is set to 0.

Figure 5-6. Concurrent Data Transmission/Reception Timing (During a Burst Transfer)



Revision History

Date	Revision	Comments
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April 27, 2009	2.0	Incremental update from comments to the 1.0..

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