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RENESAS

User's Manual

Multimedia Processor for Mobile Applications

ITU-R BT.656 Interface

EMMA Mobile1

Document No. S19257EJ2V0UM00 (2nd edition)
Date Published April 2009

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E 02. 11-1

PREFACE

Readers

This manual is intended for hardware/software application system designers who wish to understand and use the ITU-R BT.656 interface functions of EMMA Mobile1 (EM1), a multimedia processor for mobile applications.

Purpose

This manual is intended to explain to users the hardware and software functions of the ITU-R BT.656 interface of EM1, and be used as a reference material for developing hardware and software for systems that use EM1.

Organization

This manual consists of the following chapters.

- Chapter 1 Overview
- Chapter 2 Pin functions
- Chapter 3 Registers
- Chapter 4 Description of functions

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, and microcontrollers.

To understand the functions of the ITU-R BT.656 interface of EM1 in detail
→ Read this manual according to the **CONTENTS**.

To understand the other functions of EM1
→ Refer to the user's manual of the respective module.

To understand the electrical specifications of EM1
→ Refer to the Data Sheet.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Data type:	Word … 32 bits
	Halfword … 16 bits
	Byte … 8 bits

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document No.
MC-10118A Data sheet		S19657E
μ PD77630A Data sheet		S19686E
User's manual	Audio/Voice and PWM Interfaces	S19253E
	DDR SDRAM Interface	S19254E
	DMA Controller	S19255E
	I^2C Interface	S19256E
	ITU-R BT.656 Interface	This manual
	LCD Controller	S19258E
	MICROWIRE	S19259E
	NAND Flash Interface	S19260E
	SPI	S19261E
	UART Interface	S19262E
	Image Composer	S19263E
	Image Processor Unit	S19264E
	System Control/General-Purpose I/O Interface	S19265E
	Timer	S19266E
	Terrestrial Digital TV Interface	S19267E
	Camera Interface	S19285E
	USB Interface	S19359E
	SD Memory Card Interface	S19361E
	PDMA	S19373E
	One Chip (MC-10118A)	S19598E
	One Chip (μ PD77630A)	S19687E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

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LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 OVERVIEW

1.1 General

This document describes the ITU-R BT.656 interface (NTS) of EM1.

1.2 Features

NTS fetches YUV422-format image data from a frame buffer memory, converts it to the image to be output to the ITU-R BT.656-compliant parallel interface in synchronization with the internal timing signals, and outputs it to an external NTSC/PAL encoder IC.

(1) Supported standards
NTSC (525/60): Effective pixels: 720 × 486
PAL (625/50): Effective pixels: 720 × 576

(2) Output data format
ITU-R BT.656-compliant parallel data interface for data output

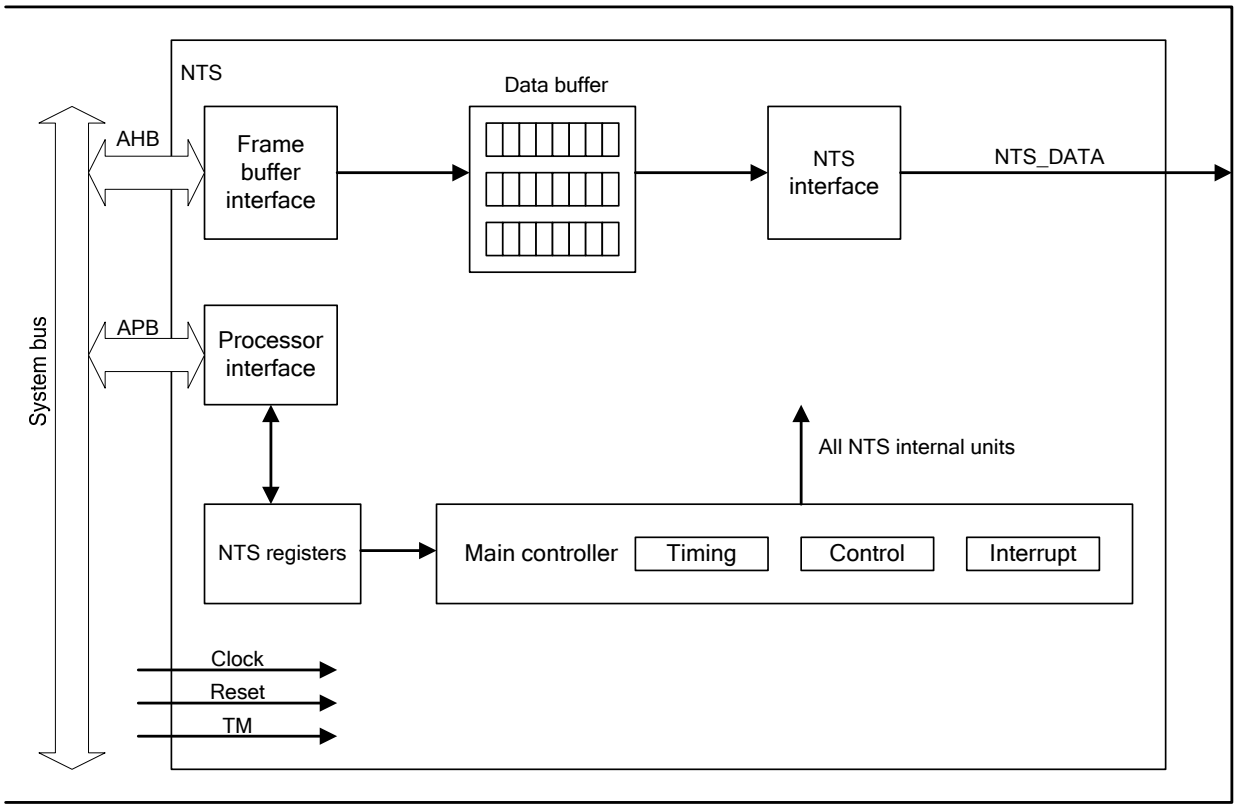
(3) Input image data format
YUV422 image data

(4) Gain adjustment
Internally adjusts the gain of the input YUV data to support ITU-R BT.601.

(5) Upscaling
Can double an image vertically and horizontally.
If images need not be expanded to NTSC/PAL size, such as when playing MPEG videos, a small image is generated in the memory and is quadrupled when transferred to the encoder IC. This function reduces internal processing during image generation and memory traffic.

1.3 Function Block Diagram

Figure 1-1. NTS Block Diagram



CHAPTER 2 PIN FUNCTIONS

2.1 NTS Pins

Pin Name	I/O	After Reset	Function	Alternate Pin Function
NTS_DATA0	Output	–	ITU-R BT.656-compliant parallel data Bit 0	AB0_A17/GIO_P28/GIO_P75/SPI_SO CAM_YUV0
NTS_DATA1	Output	–	ITU-R BT.656-compliant parallel data Bit 1	AB0_A18/GIO_P29/GIO_P76/SP1_CS0 CAM_YUV1
NTS_DATA2	Output	–	ITU-R BT.656-compliant parallel data Bit 2	AB0_A19/GIO_P30/GIO_P77/SP1_CS1 CAM_YUV2
NTS_DATA3	Output	–	ITU-R BT.656-compliant parallel data Bit 3	AB0_RDB/GIO_P39/GIO_P78/SP1_CS2 CAM_YUV3
NTS_DATA4	Output	–	ITU-R BT.656-compliant parallel data Bit 4	AB0_WRB/GIO_P40/GIO_P79/SP1_CS3
NTS_DATA5	Output	–	ITU-R BT.656-compliant parallel data Bit 5	AB0_WAIT/GIO_P41/GIO_P80/ SP1_CS4/PM1_SEN
NTS_DATA6	Output	–	ITU-R BT.656-compliant parallel data Bit 6	AB0_CSB0/GIO_P42/GIO_P81/ SP1_CS5/PM1_SI
NTS_DATA7	Output	–	ITU-R BT.656-compliant parallel data Bit 7	AB0_CSB1/GIO_P43/GIO_P82/PM1_SO
NTS_VS	Output	–	Vertical synchronization signal (for debugging)	AB0_CSB2/GIO_P44/GIO_P73/ SP1_CLK
NTS_HS	Output	–	Horizontal synchronization signal (for debugging)	AB0_CSB3/GIO_P45/GIO_P74/SP1_SI
NTS_CLK	Input	–	ITU-R BT.656 interface control clock (27 MHz)	AB0_CLK/GIO_P11/GIO_P72/PM1_CLK

CHAPTER 3 REGISTERS

The NTS registers allow word access only.

Do not access reserved registers.

Any value written to reserved bits in each register is ignored.

3.1 Registers

Base address: 4021_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Control register	NTS_CONTROL	R/W	0000_0000H
0004H	Display register	NTS_OUT	R/W	0000_0000H
0008H	Status register	NTS_STATUS	R	0000_0000H
000CH	Display area address register YA	NTS_YAREAAD_A	R/W	0000_0000H
0010H	Display area address register YB	NTS_YAREAAD_B	R/W	0000_0000H
0014H	Display area address register YC	NTS_YAREAAD_C	R/W	0000_0000H
0018H	Display area address register UVA	NTS_UVAREAAD_A	R/W	0000_0000H
001CH	Display area address register UVB	NTS_UVAREAAD_B	R/W	0000_0000H
0020H	Display area address register UVC	NTS_UVAREAAD_C	R/W	0000_0000H
0024H	Address addition value register	NTS_HOFFSET	R/W	0000_0000H
0028H	Frame select register	NTS_FRAMESEL	R/W	0000_0001H
002CH-005CH	Reserved	–	–	–
0060H	Interrupt status register	NTS_INTSTATUS	R	0000_0000H
0064H	Interrupt raw status register	NTS_INTRAWSTATUS	R	0000_0000H
0068H	Interrupt enable set register	NTS_INTENSET	R/W	0000_0000H
006CH	Interrupt enable clear register	NTS_INTENCLR	W	0000_0000H
0070H	Interrupt source clear register	NTS_INTFFCLR	W	0000_0000H
0074H	Error address register	NTS_ERRORADR	R/W	0000_0000H
0078H	Software reset register	NTS_SWRESET	R/W	0000_0000H
007CH-00FCH	Reserved	–	–	–

3.2 Register Functions

3.2.1 Control register

This register (NTS_CONTROL: 4021_0000H) control NTS.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

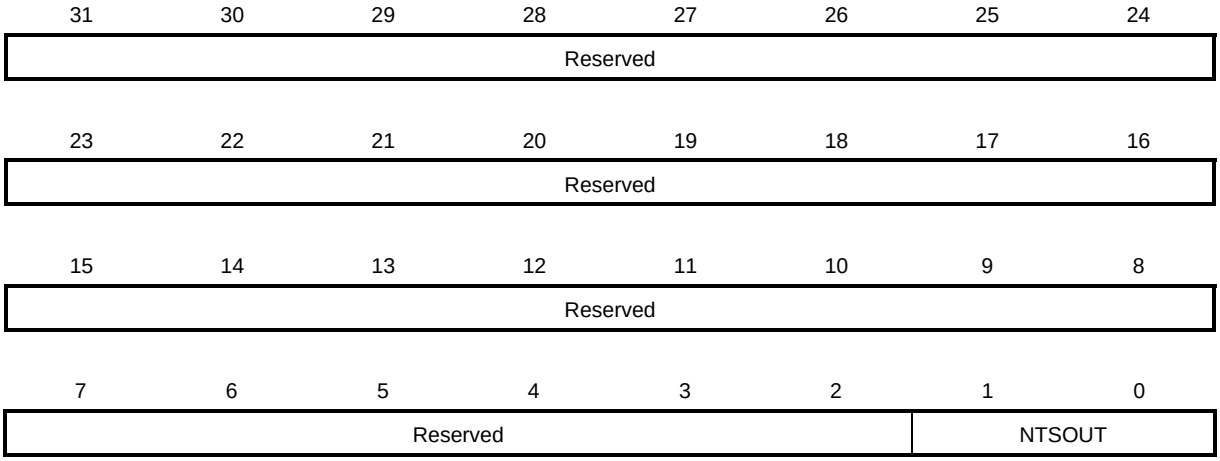
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				UPSCALE	OUTMODE	CLKPOL	ENDIAN

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0	Reserved. When these bits are read, 0 is returned for each bit.
UPSCALE	R/W	3	0	Specifies whether to enable the upscale (zoom) function. 0: Disable 1: Enable
OUTMODE	R/W	2	0	Selects the NTSC encoder interface output system. 0: NTSC (525/60) 1: PAL (625/60)
CLKPOL	R/W	1	0	Selects the phase of the NTS_CLKI (27 MHz). 0: Rising edge of NTS_CLKI 1: Falling edge of NTS_CLKI
ENDIAN	R/W	0	0	Specifies the endian of the image data being stored in the frame buffer memory. 0: Little endian 1: Big endian

3.2.2 Display register

This register (NTS_OUT: 4021_0004H) controls the data output to the NTS encoder interface.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0	Reserved. When these bits are read, 0 is returned for each bit.
NTSOUT	R/W	1:0	0	Controls the data output to the NTS encoder interface. 00: OFF (all-0 data is output), without synchronization signal output 01: ON (BlackBack output), with synchronization signal output 10: ON (BlueBack output), with synchronization signal output 11: ON (Normal output), with synchronization signal output

3.2.3 Status register

This register (NTS_STATUS: 4021_0008H) indicates the status of NTS. The status of the NTS output can be acquired by polling this register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

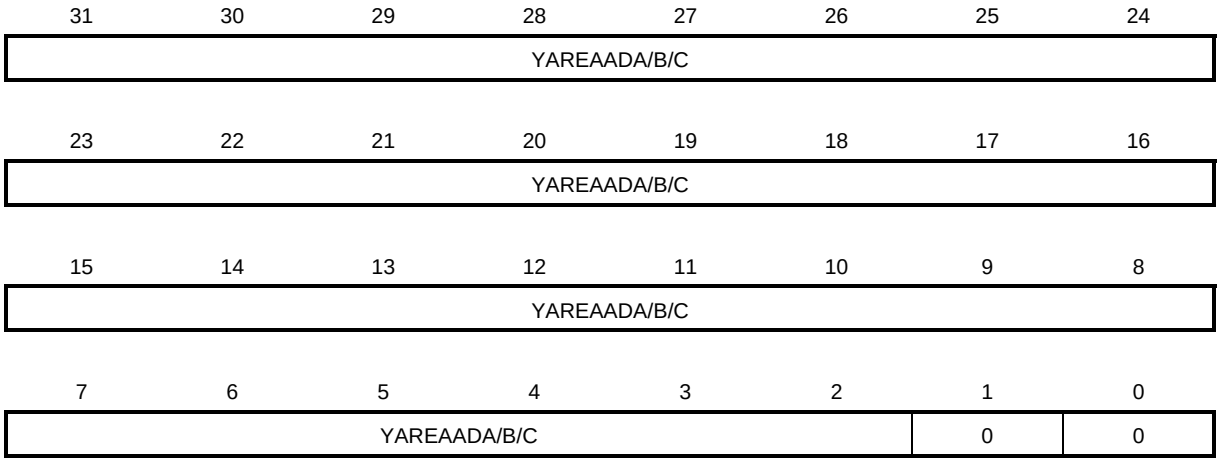
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						STATUS	

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0	Reserved. When these bits are read, 0 is returned for each bit.
STATUS	R	1:0	0	Indicates the NTS output status. 00: OFF (all-0 data is output), without synchronization signal output 01: ON (BlackBack output), with synchronization signal output 10: ON (BlueBack output), with synchronization signal output 11: ON (Normal output), with synchronization signal output

3.2.4 Display area address register

These registers (NTS_YAREAAD_A: 4021_000CH, NTS_YAREAAD_B: 4021_0010H, NTS_YAREAAD_C: 4021_0014H) specify the head address of the Y-layer area in the frame buffer memory to which the YUV422-format image data is stored. A UV layer has three planes (A, B, and C), which have common specifications.



Name	R/W	Bit	After Reset	Function
YAREAADA/ B/C	R/W	31:2	0	Specifies the head address of the frame buffer memory(Y layer). Specify the address by byte address on a 32-bit boundary.
–	R	1:0	0	Fixed to 0. When these bits are read, 0 is returned for each bit.

3.2.5 Display area address register UV

These registers (NTS_UVAREAAD_A: 4021_0018H, NTS_UVAREAAD_B: 4021_001CH, NTS_UVAREAAD_C: 4021_0020H) specify the head address of the UV-layer area in the frame buffer memory to which the YUV422-format image data is stored. A UV layer has three planes (A, B, and C), which have common specifications.

31	30	29	28	27	26	25	24
UVAREAADA/B/C							

23	22	21	20	19	18	17	16
UVAREAADA/B/C							

15	14	13	12	11	10	9	8
UVAREAADA/B/C							

7	6	5	4	3	2	1	0
UVAREAADA/B/C						0	0

Name	R/W	Bit	After Reset	Function
UVAREAADA/B/C	R/W	31:2	0	Specifies the head address of the frame buffer memory (UV layer). Specify the address by byte address on a 32-bit boundary.
–	R	1:0	0	Fixed to 0. When these bits are read, 0 is returned for each bit.

3.2.6 Address addition value register

This register (NTS_HOFFSET: 4021_0024H) specifies the total number of bytes in the horizontal direction of frame buffer areas. The setting is commonly applied to frame buffers A, B and C.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved			HOFFSET				

7	6	5	4	3	2	1	0
HOFFSET						0	0

Name	R/W	Bit	After Reset	Function
Reserved	R	31:13	0	Reserved. When these bits are read, 0 is returned for each bit.
HOFFSET	R/W	12:0	0	Specifies the total number of bytes in the horizontal direction of the frame buffer areas. (The lower 2 bits are fixed to 0.)

3.2.7 Frame select register

This register (NTS_FRAMESEL: 4021_0028H) selects display frame A, B, or C.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				AREASTATUS		AREASEL	

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0	Reserved. When these bits are read, 0 is returned for each bit.
AREASTATUS	R	3:2	00	Indicates the frame currently being displayed. 00: Initial state 01: Frame buffer A 10: Frame buffer B 11: Frame buffer C
AREASEL	R/W	1:0	01	Selects the frame buffer whose image is to be displayed. 00: Setting prohibited 01: Frame buffer A 10: Frame buffer B 11: Frame buffer C

3.2.8 Interrupt setting registers

These registers are used to specify various interrupt parameters. NTS uses four interrupts.

(1) Interrupt status register

This read-only register (NTS_INTSTATUS: 4021_0060H) indicates the status of the interrupt sources. The status of the interrupt sources enabled by the interrupt enable set register can be read.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				UNDERRUN	DMASTOP	DMAERR	NTSVS

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0	Reserved. When these bits are read, 0 is returned for each bit.
UNDERRUN	R	3	0	Indicates the status of the underrun interrupt. 0: No interrupt source 1: Interrupt source occurred
DMASTOP	R	2	0	Indicates the status of the transfer stop interrupt. 0: No interrupt source 1: Interrupt source occurred
DMAERR	R	1	0	Indicates the status of the transfer error interrupt. 0: No interrupt source 1: Interrupt source occurred
NTSVS	R	0	0	Indicates the status of the NTS frame interrupt. 0: No interrupt source 1: Interrupt source occurred

(2) Interrupt raw status register

This read-only register (NTS_INTRAWSTATUS: 4021_0064H) indicates the status of the interrupt sources. The bits corresponding to the interrupt sources are set regardless of the settings of the interrupt enable set register and the interrupt enable clear register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				UNDERRUN RAW	DMASTOP RAW	DMAERRRAW	NTSVSRAW

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0	Reserved. When these bits are read, 0 is returned for each bit.
UNDERRUN RAW	R	3	0	Indicates the status of the underrun interrupt. 0: No interrupt source 1: Interrupt source occurred
DMASTOPR AW	R	2	0	Indicates the status of the transfer stop interrupt. 0: No interrupt source 1: Interrupt source occurred
DMAERRRA W	R	1	0	Indicates the status of the transfer error interrupt. 0: No interrupt source 1: Interrupt source occurred
NTSVSRAW	R	0	0	Indicates the status of the NTS frame interrupt. 0: No interrupt source 1: Interrupt source occurred

(3) Interrupt enable set register

This register (NTS_INTENSET: 4021_0068H) enables issuance of interrupt requests. Only data of bits to which 1 is written is updated. When the bit corresponding to an interrupt source in this register is set to 1, the interrupt source is set, request for the interrupt is issued, and the corresponding bit of the interrupt status register is set to 1. If no bits are set to 1 in this register, no interrupt requests are issued even if an interrupt source is set, but the corresponding bit of the interrupt raw status register is set to 1.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				UNDERRUNEN	DMASTOPEN	DMAERREN	NTSVSEN

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0	Reserved. When these bits are read, 0 is returned for each bit.
UNDERRUNEN	R	3	0	Indicates whether issuance of the underrun interrupt request is enabled. 0: Not enabled, 1: Enabled
	W	3	–	Enables issuance of the underrun interrupt request. 0: Ignored, 1: Cancels masking of the interrupt.
DMASTOPEN	R	2	0	Indicates whether issuance of the transfer stop interrupt request is enabled. 0: Not enabled, 1: Enabled
	W	2	–	Enables issuance of the transfer stop interrupt request. 0: Ignored, 1: Cancels masking of the interrupt.
DMAERREN	R	1	0	Indicates whether issuance of the transfer stop interrupt request is enabled. 0: Not enabled, 1: Enabled
	W	1	–	Enables issuance of the transfer stop interrupt request. 0: Ignored, 1: Cancels masking of the interrupt.
NTSVSEN	R	0	0	Indicates whether issuance of the NTS frame interrupt request is enabled. 0: Not enabled, 1: Enabled
	W	0	–	Enables issuance of the NTS frame interrupt request. 0: Ignored, 1: Cancels masking of the interrupt.

(4) Interrupt enable clear register

This write-only register (NTS_INTENCLR:4021_006CH) disables (masks) issuance of interrupt requests. If the bit corresponding to an interrupt source in this register is set to 1, no interrupt requests are issued even if the interrupt source is generated. The status of the corresponding bit in the interrupt status register also remains unchanged. If no bits are set to 1 in this register, an interrupt request is issued when an interrupt source is set, and the corresponding bit of the interrupt status register is set to 1. Writing 0 to this register does not affect the setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				UNDERRUN MASK	DMASTOP MASK	DMAERR MASK	NTSVSMASK

Name	R/W	Bit	After Reset	Function
Reserved	–	31:4	0	Reserved.
UNDERRUN MASK	W	3	0	Disables issuance of the underrun interrupt request. 1: Disables (masks) the interrupt.
DMASTOPMASK	W	2	0	Disables issuance of the transfer stop interrupt request. 1: Disables (masks) the interrupt.
DMAERRMASK	W	1	0	Disables issuance of the transfer stop interrupt request. 1: Disables (masks) the interrupt.
NTSVSMASK	W	0	0	Disables issuance of the NTS frame interrupt request. 1: Disables (masks) the interrupt.

(5) Interrupt source clear register

This write-only register (NTS_INTFFCLR: 4021_0070H) requests clearing of interrupt sources. Setting the bit corresponding to an interrupt source to 1 clears the interrupt source. Writing 0 to this register does not affect the setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

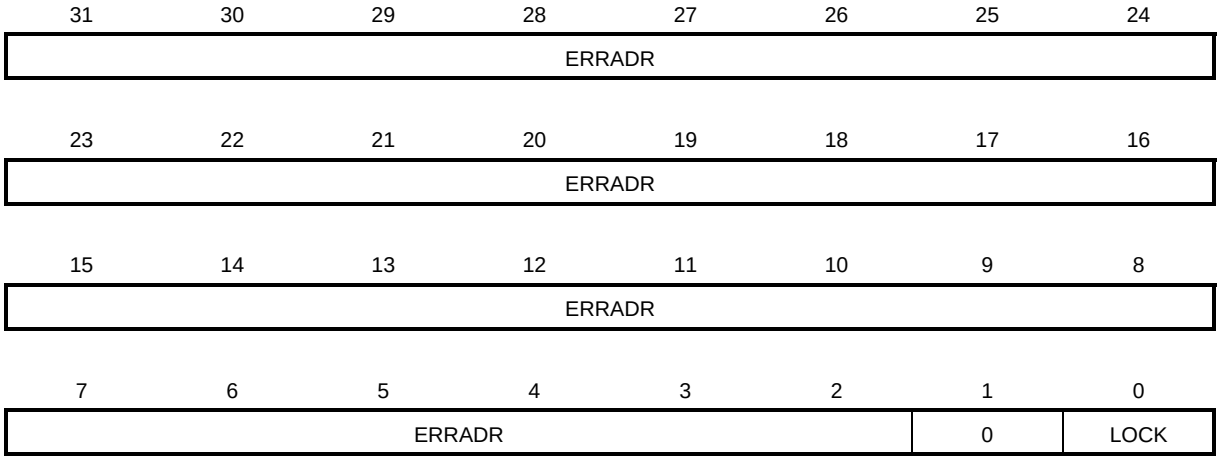
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				UNDERRUNCLR	DMASTOPCLR	DMAERR CLR	NTSVS CLR

Name	R/W	Bit	After Reset	Function
Reserved	–	31:4	0	Reserved.
UNDERRUN CLR	W	3	0	Requests clearing of the source of the underrun interrupt. 1: Clears the interrupt source.
DMASTOPC LR	W	2	0	Requests clearing of the source of the transfer stop interrupt. 1: Clears the interrupt source.
DMAERRCLR	W	1	0	Requests clearing of the source of the transfer error interrupt. 1: Clears the interrupt source.
NTSVSCLR	W	0	0	Requests clearing of the source of the NTS frame interrupt. 1: Clears the interrupt source.

(6) Error address register

This register (NTS_ERRORADR: 4021_0074H) retains the current HADDR status when an internal bus response ERROR, RETRY, or SPLIT is received during DMA transfer.



Name	R/W	Bit	After Reset	Function
ERRADR	R	31:2	0	Stores HADDR upon occurrence of an error response.
Reserved	R	1	0	Reserved. When this bit is read, 0 is returned.
LOCK	R/W	0	0	Error status 0: Stores the address when an error response occurs. 1: An error response occurred and the address was stored.

Caution If an error response occurs when the LOCK bit is 0, the current HADDR status is stored in the ERRADR bit and the LOCK bit is set to 1. To acquire the error status again, set the LOCK bit to 0. Writing 1 to the LOCK bit does not affect the setting.

(7) Software reset register

This register (NTS_SWRESET: 4021_0078H) is used for switching the phase of the NTS_CLKI (27 MHz) clock. This register resets the circuit operating at 27 MHz before the NTS_CLK phase is switched by using the CLKPOL bit of the control register (NTS_CONTROL). Cancel this setting after changing the phase.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							SWRESET

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
SWRESET	R/W	0	0	Specifies whether to enable software reset. 0: Disables reset. 1: Enables reset.

CHAPTER 4 DESCRIPTION OF FUNCTIONS

4.1 NTS Encoder Interface

The ITU-R BT.656-compliant format uses the interlace system where a single screen (frame) consists of two fields. This system does not use the vertical synchronizing (VD) and horizontal synchronizing (HD) signals for synchronizing the image, but recognizes the effective pixel area by using the two timing reference signals SAV (start of active video) and EAV (end of active video), included in the data stream, for the synchronization.

SAV and EAV each consist of 3-byte preamble data (FF/00/00) and 1-byte timing reference data.

The following table lists the timing for the NTSC system and PAL system.

Table 4-1. Video Timing Reference Codes

Data[7:0] Bit Number	1st Word (FF)	2nd Word (00)	3rd Word (00)	4th Word (XY)
7 (MSB)	1	0	0	1
6	1	0	0	F
5	1	0	0	V
4	1	0	0	H
3	1	0	0	P3
2	1	0	0	P2
1	1	0	0	P1
0	1	0	0	P0

F = 0: Field 1 is being accessed F = 1: Field 2 is being accessed

V = 0: Not in a field blanking interval V = 1: In a field blanking interval

H = 0: SAV, H = 1: EAV

P3 to P0: Protection bits

P3 = V EXOR H

P2 = F EXOR H

P1 = F EXOR V

P0 = F EXOR V EXOR H

(1) NTSC system

Figure 4-1. Data Format in NTSC System

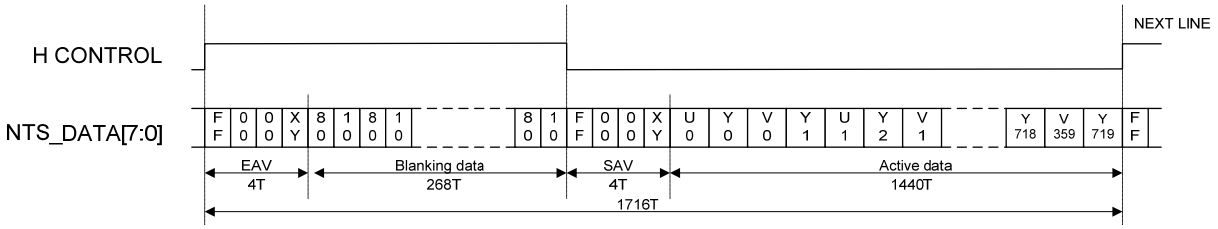
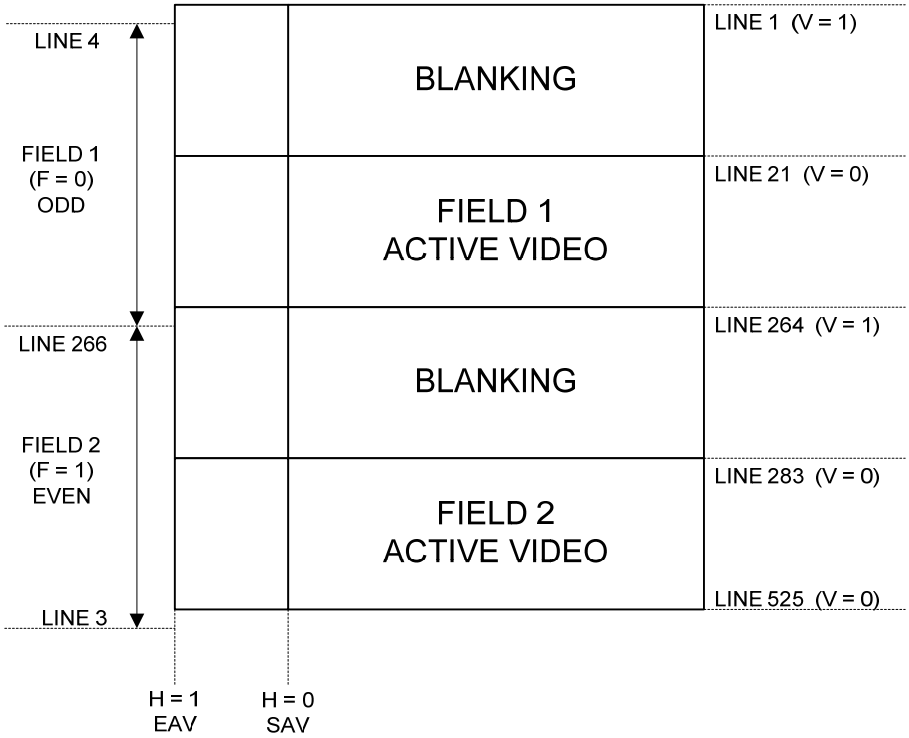


Table 4-2. SAV and EAV Setting Values in NTSC System

Line No.	SAV: XY Value								EAV: XY Value							
NTSC	1	F	V	H	P3	P2	P1	P0	1	F	V	H	P3	P2	P1	P0
1 to 3	1	1	1	0	1	1	0	0	1	1	1	1	0	0	0	1
4 to 20	1	0	1	0	1	0	1	1	1	0	1	1	0	1	1	0
21 to 263	1	0	0	0	0	0	0	0	1	0	0	1	1	1	0	1
264 to 265	1	0	1	0	1	0	1	1	1	0	1	1	0	1	1	0
266 to 282	1	1	1	0	1	1	0	0	1	1	1	1	0	0	0	1
283 to 525	1	1	0	0	0	1	1	1	1	1	0	1	1	0	1	0

Figure 4-2. Vertical Blanking Interval in NTSC System



(2) PAL system

Figure 4-3. Data Format in PAL System

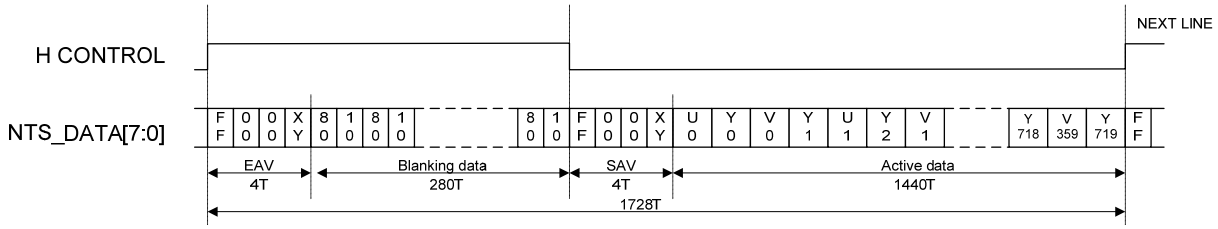
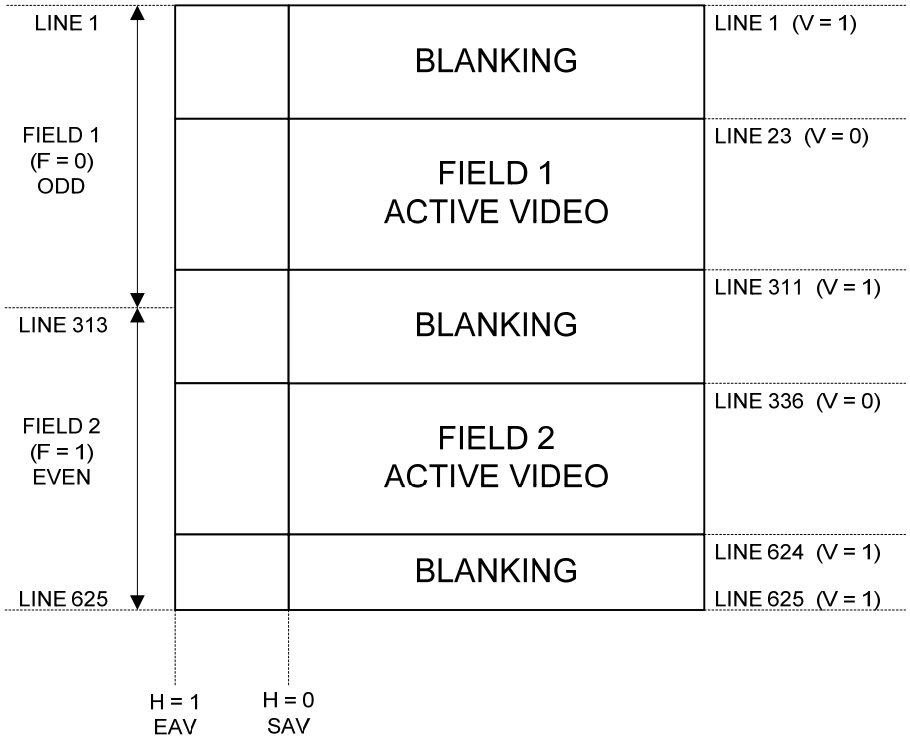


Table 4-3. SAV and EAV Setting Values in PAL System

Line No.	SAV: XY Value								EAV: XY Value							
PAL	1	F	V	H	P3	P2	P1	P0	1	F	V	H	P3	P2	P1	P0
1 to 22	1	0	1	0	1	0	1	1	1	0	1	1	0	1	1	0
23 to 310	1	0	0	0	0	0	0	0	1	0	0	1	1	1	0	1
311 to 312	1	0	1	0	1	0	1	1	1	0	0	1	1	1	1	0
313 to 335	1	1	1	0	1	1	0	0	1	1	1	1	0	0	0	1
336 to 623	1	1	0	0	0	1	1	1	1	1	0	1	1	0	1	0
624 to 625	1	1	1	0	1	1	0	0	1	1	1	1	0	0	0	1

Figure 4-4. Vertical Blanking Interval in PAL System



4.1.1 Generating synchronization signals

The horizontal-direction timing control signal is generated by using an 11-bit counter that operates with the NTS_CLKI clock.

The vertical-direction timing control signal is generated by using a 10-bit counter that operates with the generated horizontal-direction timing control signal.

Figure 4-5. Relationship Between Horizontal- and Vertical-Direction Timing Control Signals in NTSC System

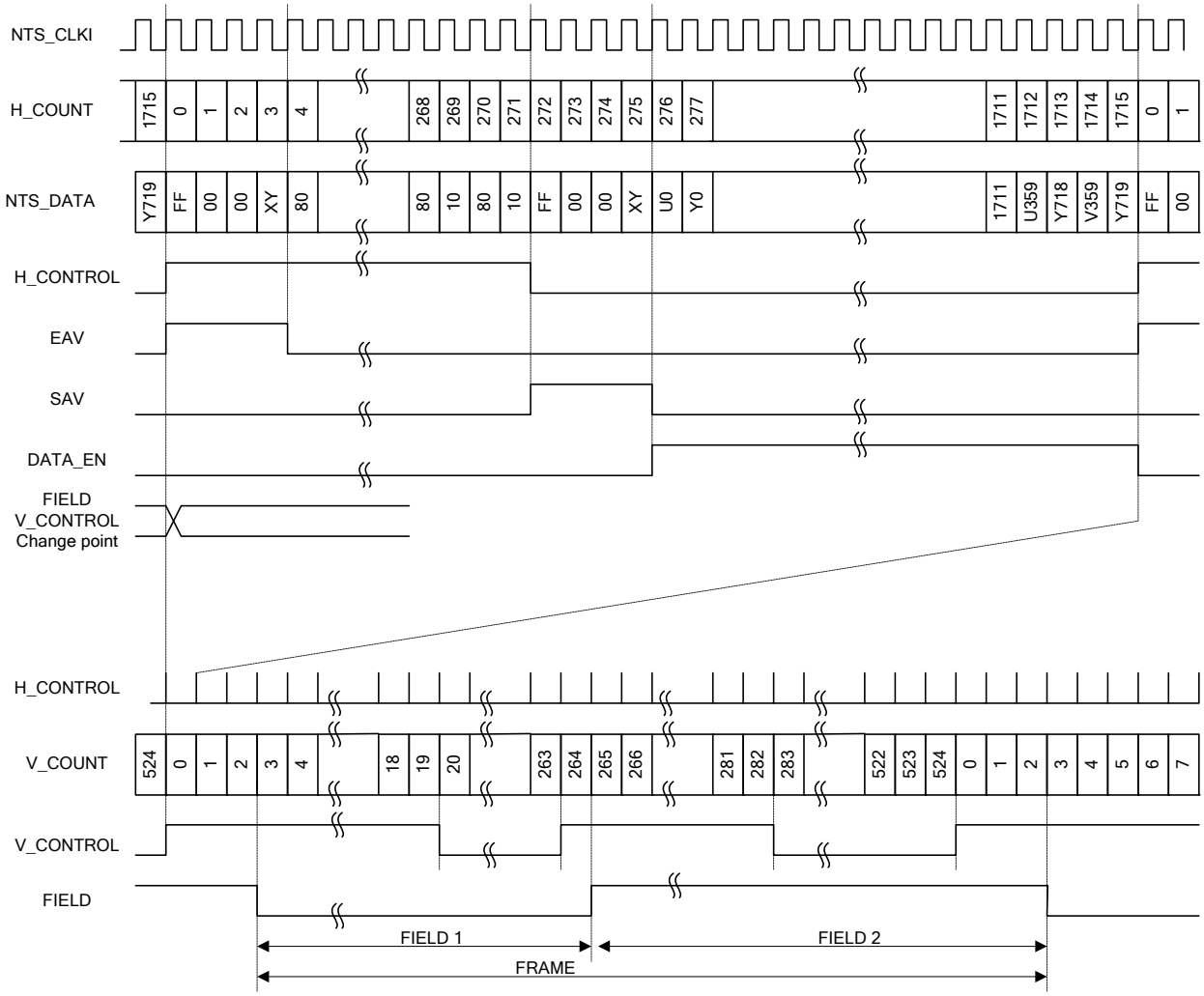
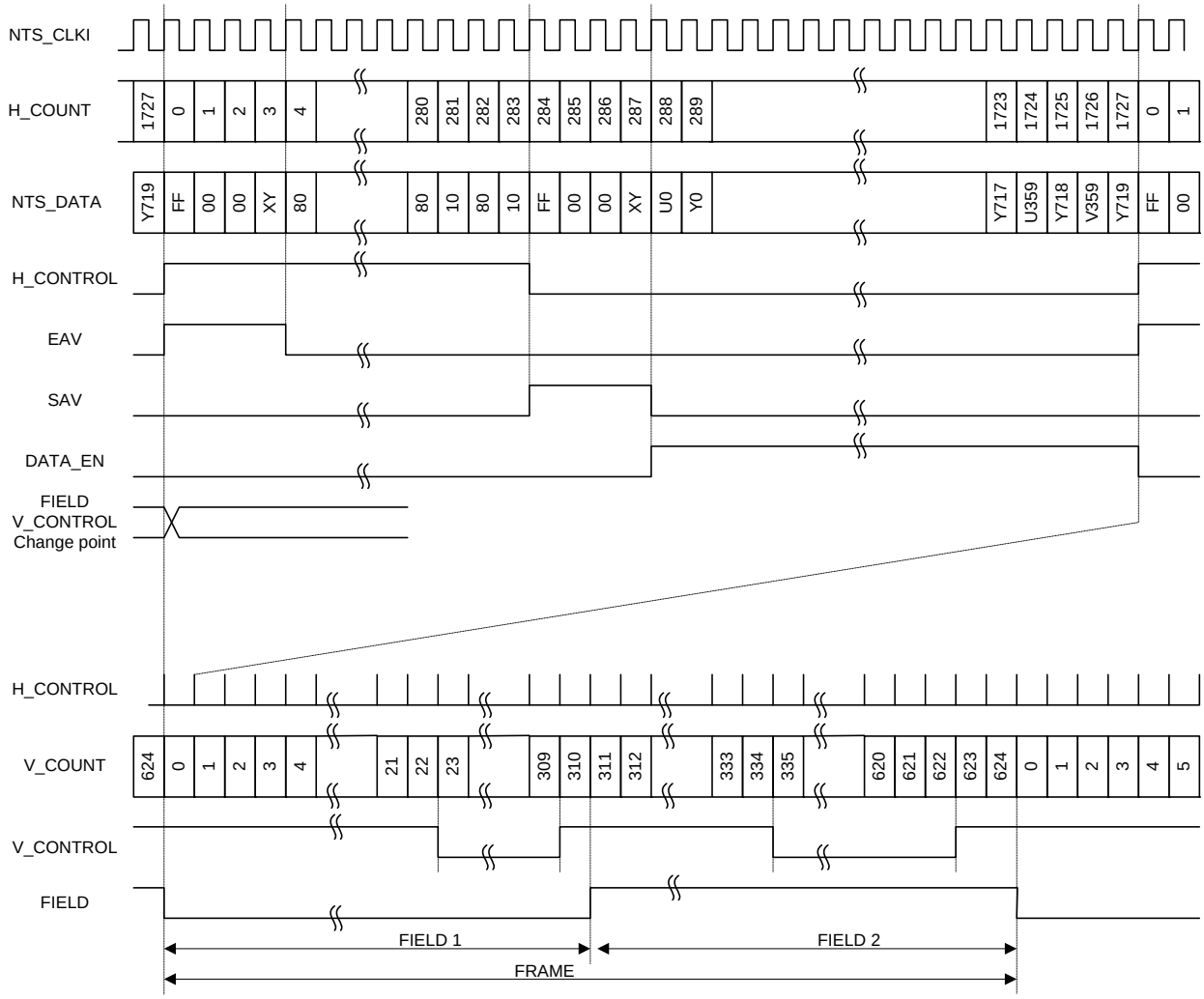


Figure 4-6. Relationship Between Horizontal- and Vertical-Direction Timing Control Signals in PAL System



4.1.2 Adjusting the phase of control clock (NTS_CLKI)

The timing of outputting NTS_DATA can be selected from the rising or falling edge of the NTS_CLKI clock by setting the CLKPOL bit of the NTS_CONTROL register. The NTS_DATA signal is output in synchronization with the rising edge of the NTS_CLKI clock when CLKPOL is set to 0, and with the falling edge when CLKPOL is set to 1.

As a result of this adjustment, the phase of circuits operating at 27 MHz is changed. To prevent the internal circuits from malfunctioning, reset the circuits operating at 27 MHz by using the software reset register (NTS_SWRESET) before phase adjustment, and cancel the reset after adjustment.

Figure 4-7. Synchronization with Rising Edge of NTS_CLKI

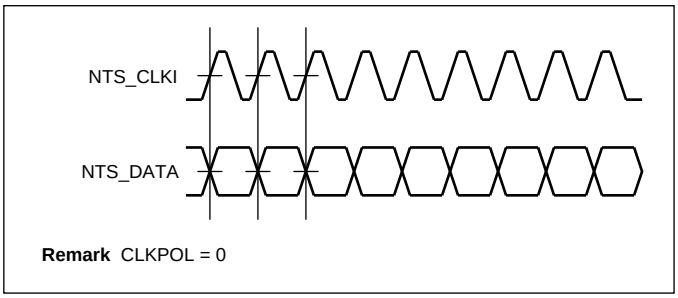
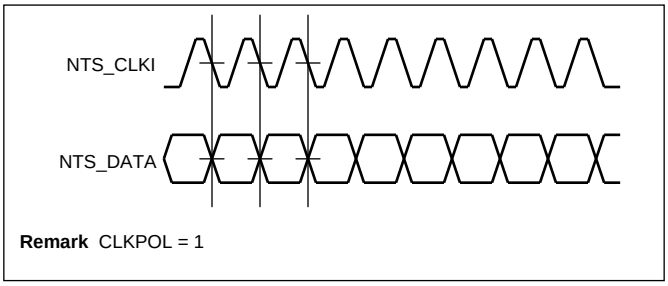


Figure 4-8. Synchronization with Falling Edge of NTS_CLKI



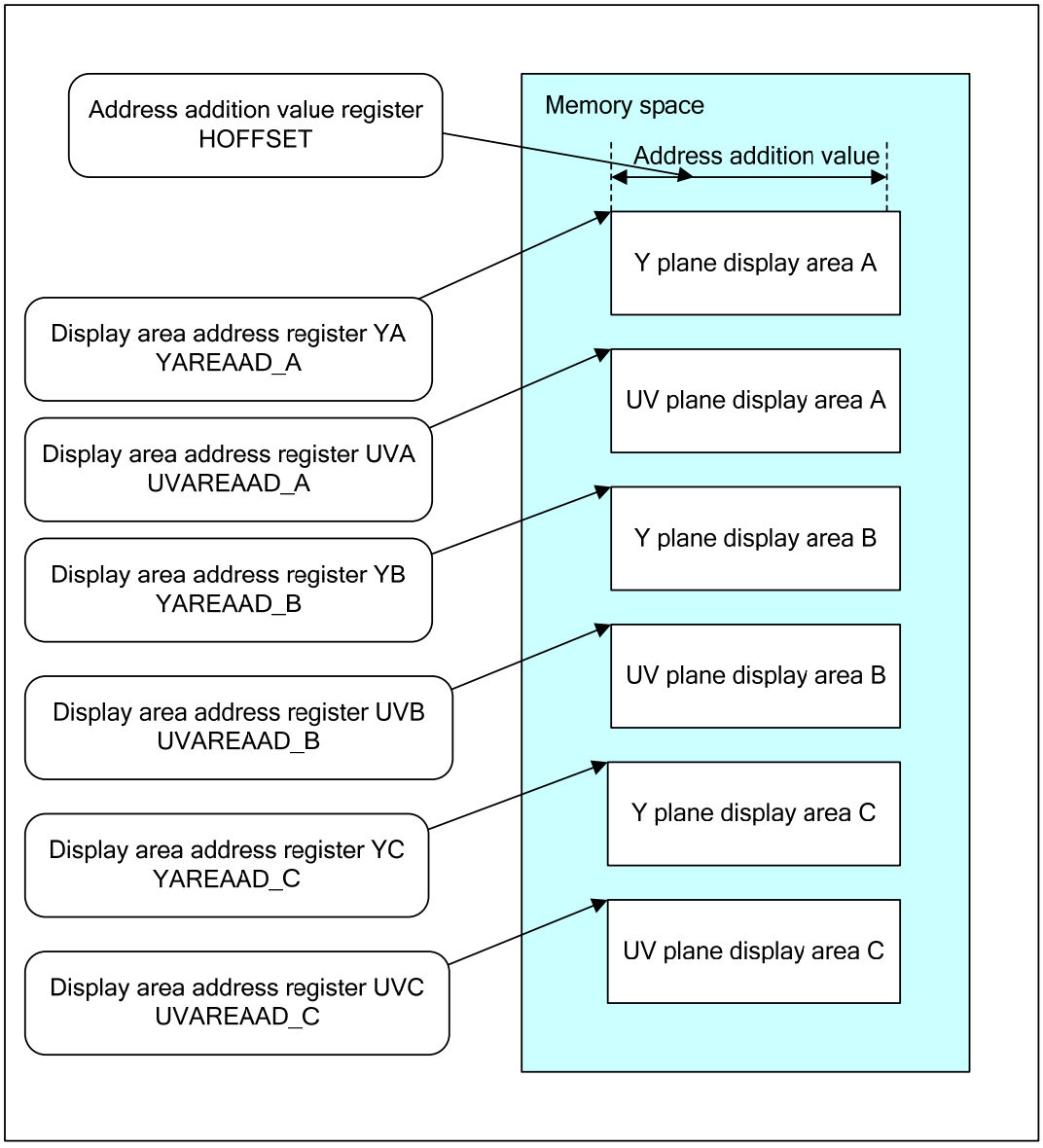
4.2 Frame Buffer and Data Buffer

4.2.1 Frame buffer

Frame buffer is generic term used to refer to a buffer storing a single screen of image data. There are three frame buffers, defined as frame buffers A, B, and C. The display area address registers Y (NTS_YAREAAD_A/B/C) and the display area address registers UV (NTS_UVAREAAD_A/B/C) correspond to frame buffers A, B, and C, respectively, and any address can be set by using these registers. The address addition value register (NTS_HOFFSET) can be used to specify the horizontal size of the frame buffer area in word (2 bytes) units. By this means, a rectangle area clipped from the frame buffer, which has been mapped in a size larger than the display image size, can be output to NTS. (The parameter of address addition value is common to frame buffers A, B, and C.)

Frame buffers A, B, and C are never accessed at the same time. One frame buffer is selected by an order of the processor.

Figure 4-9. Image of Frame Buffer



4.2.2 Frame buffer storage format

Frame buffers store YUV422-format image data. The storage data format is shown below. The endian type for the bus can be specified by using the ENDIAN bit of the NTS_CONTROL register.

Data size: The same size for Y and UV planes.

Y Plane: Data size is X size × Y size bytes for the data at 1 pixel per byte.

UV Plane: Data size is X size × Y size bytes for the data at 2 pixels per byte for UV individually.

The following shows the file images when X size = n, Y size = m, and the number of images is 1.

(1) Little endian

- Y plane

Y[0]	Y[1]	Y[2]	Y[3]	Y[4]	Y[5]	.	.	.		Y[14]	Y[15]
Y[16]	Y[17]										
.											
.											
.											
											Y[nxm-1]

- UV plane

U[0]	V[0]	U[1]	V[1]	U[2]	V[2]	.	.	.		U[7]	V[7]
U[8]	V[8]										
.											
.											
.											
										U[nxm/2-1]	V[nxm/2-1]

(2) Big endian

• Y plane

Y[1]	Y[0]	Y[3]	Y[2]	Y[5]	Y[4]	.	.	.		Y[15]	Y[14]
Y[17]	Y[16]										
.											
.											
.											
										Y[nxm-1]	Y[nxm-2]

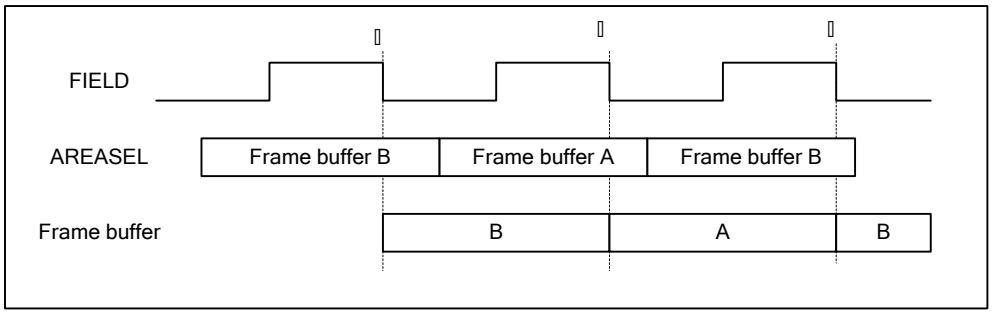
• UV plane

V[0]	U[0]	V[1]	U[1]	V[2]	U[2]	.	.	.		V[7]	U[7]
V[8]	U[8]										
.											
.											
.											
										V[nxm/2-1]	U[nxm/2-1]

4.2.3 Switching frame buffers

The AREASEL bit of the frame select register (NTS_FRAMESEL) can be used to switch the frame buffers. The frame buffers are switched at the start of a frame (frame display start signal).

Figure 4-10. Frame Buffer Switching Timing



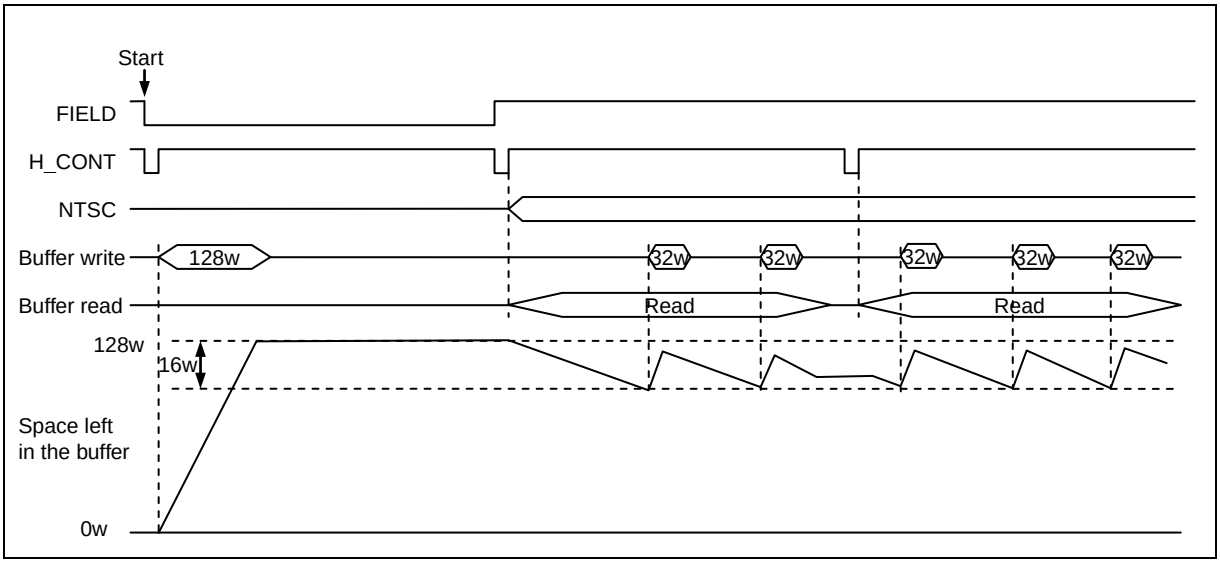
4.2.4 Data buffer

Data buffer is an NTS internal buffer that fetches the image data sent from the frame buffer by burst transfer.

The data buffer is a 32-bit × 128- word FIFO buffer with two ports (1R and 1W). If there is an available space of 64 bytes in the data buffer, data is written to the data buffer from the write port via the frame buffer interface. The read port is used to read (display) data from NTS.

The data buffer is accessed as shown in Figure 4-11. First, image data is written to the data buffer via the frame buffer interface. NTS reads the image data from the area where it was written, and displays the image. The image data is written to the frame buffer if the data buffer has an available space of 64 bytes. If the speed of reading the data buffer by NTS is faster than the buffer write speed, an underrun interrupt occurs.

Figure 4-11. Data Buffer Access



Caution If the burst transfer rate is not fast enough in comparison with the NTS image refresh rate, the image data amount is insufficient, which results in a fatal image deterioration.
To avoid this, determine the clock cycle so that the following expression is sufficiently met.
NTS_CLKI clock << AHB clock

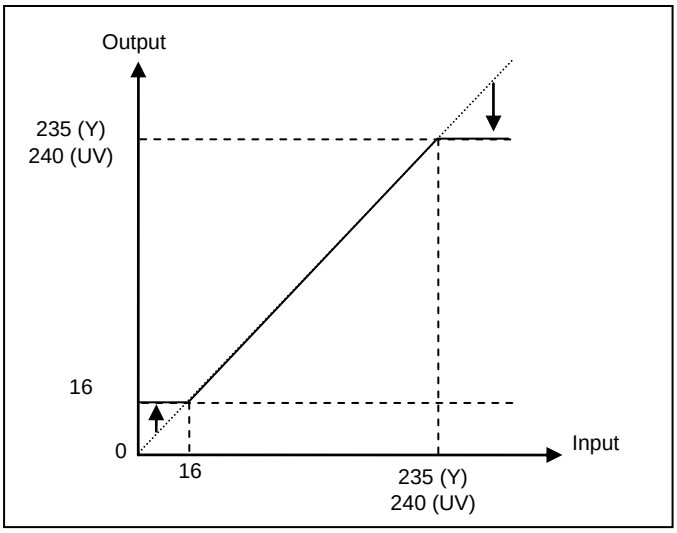
4.2.5 Gain adjustment

To comply with ITU-R BT.601, a gain is internally adjusted for the input YUV data. The following shows the method.

Restrict the image data, which is input with values 0 to 255, to the range of 16 to 240.

Restrict Y data to the range of 16 to 235, and UV data to the range of 16 to 240. The values out of the range are fixed to 0.

Figure 4-12. YUV Data Gain Adjustment



4.3 Interrupt Sources

Control of each interrupt is assigned to each bit of the interrupt setting registers.

Table 4-4. Interrupt Sources

Interrupt Name	Source	Bit Assignment
Underrun interrupt	Generated when an underrun occurs in the NTS internal data buffer.	3
Transfer stop interrupt	Generated when a RETRY or SPLIT response is received during AHB transfer.	2
Transfer error interrupt	Generated when an ERROR response is received during AHB transfer, after a single NTSC image of display data has been output.	1
NTS frame interrupt	Generated when the frame display is started.	0

Generation of an NTS frame interrupt is triggered by the frame display start signal. If register settings are changed immediately after an NTS frame interrupt occurs, the change is enabled from the next and subsequent frames.

4.4 Clock Control

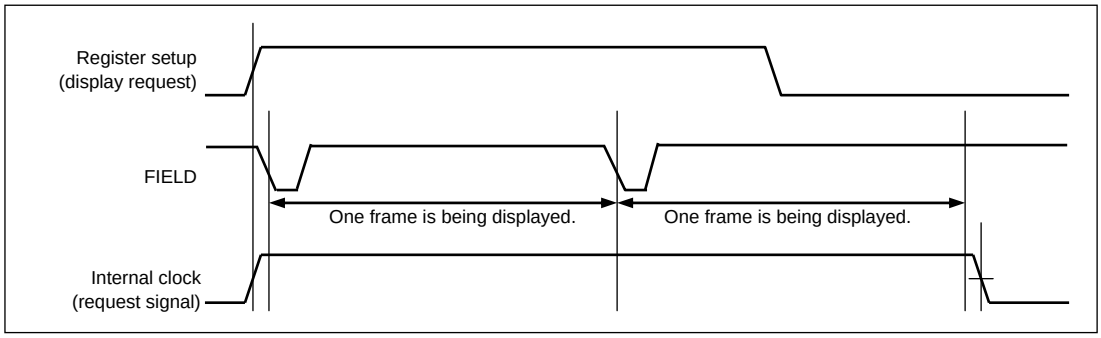
EM1 is designed for low power consumption, so it controls the clock supply on a module basis.

A clock is supplied when a module requests a clock or a register is accessed to request a clock.

For the NTSC system, a clock supply request is issued if the display register (NTS_OUT) is set to 1.

When a display frame ends with no display requests (the NTS_OUT register is 0), the clock supply request is canceled. The following shows the timing of requesting clock supply.

Figure 4-13. Clock Supply Timing



Revision History

Date	Revision	Comments
February 10,2009	1.0	–
April 27, 2009	2.0	Incremental update from comments to the 1.0.

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