User's Manual

Multimedia Processor for Mobile Applications

One Chip

EMMA Mobile™1-D512
MC-10118B (Logic Chip + DDR SDRAM)

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[MEMO]

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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

PREFACE

Readers

This manual is intended for hardware/software application system designers who wish to understand and use the functions of EMMA Mobile1-D512 (EM1-D512), a multimedia processor for mobile applications.

Purpose

This manual is intended to explain to users the hardware and software functions of EM1-D512, and be used as a reference material for developing hardware and software for systems that use EM1-D512.

Organization

This manual consists of the following chapters.

- Chapter 1 Overview
- Chapter 2 Pin functions
- Chapter 3 Description of functions
- Chapter 4 System control
- Chapter 5 Power control
- Chapter 6 Bus
- Chapter 7 Interrupt control
- Chapter 8 Alternate pin function switching
- Appendix A Registers
- Appendix B Clock (preliminary)
- Appendix C Boot loader in ROM
- Appendix D Signal pins
- Appendix E External bus interface
- Appendix F Interrupt (AINT)
- Appendix G SRC/internal SRAM
- Appendix H ADSP address converter (DCV)
- Appendix I PMU
- Appendix J DDR connection setting

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, and microcontrollers.

To gain an overview of the functions of EM1-D512

→ Read this manual according to the **CONTENTS**.

To understand the functions of EM1-D512 in detail

→ Refer to the user's manual of the respective module.

To understand the electrical specifications of EM1-D512

→ Refer to the Data Sheet.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxb
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Data type:	Word … 32 bits
	Halfword … 16 bits
	Byte … 8 bits

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document No.
EMMA Mobile1-D512 Data sheet		R19DS0008EJ (S19657E)
EMMA Mobile1-D512 user's manual	One Chip	This manual
EMMA Mobile1 user's manual	Audio/Voice and PWM Interfaces	R19UH0027EJ (S19253E)
	DDR SDRAM Interface	R19UH0028EJ (S19254E)
	DMA Controller	S19255E
	I^2C Interface	S19256E
	ITU-R BT.656 Interface	S19257E
	LCD Controller	S19258E
	MICROWIRE	S19259E
	NAND Flash Interface	S19260E
	SPI	S19261E
	UART Interface	S19262E
	Image Composer	S19263E
	Image Processor Unit	S19264E
	System Control/General-Purpose I/O Interface	R19UH0029EJ (S19265E)
	Timer	S19266E
	Terrestrial Digital TV Interface	S19267E
	Camera Interface	S19285E
	USB Interface	S19359E
	SD Memory Card Interface	S19361E
	PDMA	S19373E

( ) : old number

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

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CHAPTER 1 OVERVIEW

EMMA Mobile1-D512 (EM1-D512) (SIP: MC-10118B) is a multimedia processor for mobile applications that integrates a logic chip incorporating a CPU and DSP, and a Mobile DDR SDRAM chip, in one package.

As multimedia processor functions, EM1-D512 incorporates one CPU (ARM1176JZF-S™) and one DSP (DSPK701), achieving high-speed, power-efficient application processing. EM1-D512 also incorporates image processors with various functions to accelerate image processing.

Various power save modes enable the power to be controlled according to application processing. Moreover, power consumption can be reduced during standby by using sequences independent from the system.

1.1 Features

○ CPU: ARM1176JZF-S (Max. 500 MHz, I-cache: 32 KB, D-cache: 32 KB)
○ DSP: DSPK701 (Max. 500 MHz, I-cache: 32 KB, D-cache: 32 KB)
○ DMA controller: Memory ↔ memory and memory ↔ peripheral interface
○ Mobile DDR SDRAM (512 Mb)
○ Timers: General-purpose timers, watchdog timer (WDT)
○ Image processing
- Image processor (resizing, filtering, etc.)
- Image rotator (0°, 90°, 180°, 270°)
- Graphics DMA (ROP and FILL)
- Image composer (LCD output image synthesis)

○ H.264/MPEG-4 AVC accelerator application performance
- H.264/MPEG-4 AVC Encode/Decode: D1 30 fps

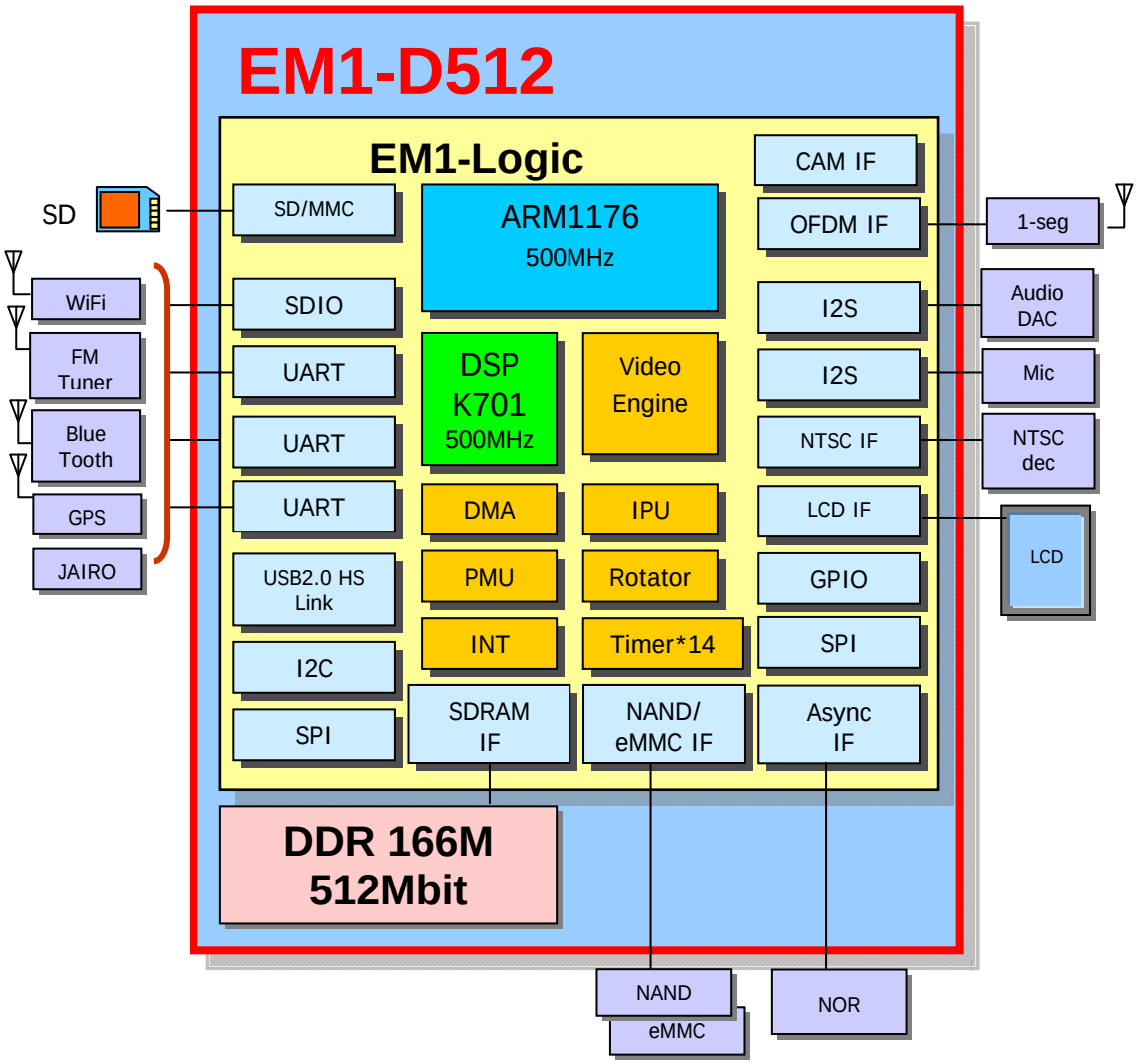
○ Peripheral interfaces
- Memory interface: External bus interface (16 bits: Flash memory, etc.), NAND interface
- Serial interfaces: UART, I^2C, audio/voice, SPI, IrDA
- SD card interface
- Image-related interfaces: LCD interface, terrestrial digital TV interface (OFDM), ITU-R.BT656 interface (NTS), camera interface
- General-purpose I/O interface: GIO
- USB interface

○ Power supply voltage
- Core power supply: V (1.2 V system : 1.1V – 1.3V)
- IO power supply: VIO18 (1.8 V system : 1.7V – 1.9V), VIO3 (3 V system : 2.7V – 3.6V)

○ Package
- 481-pin fine-pitch BGA package (12.7 × 12.7 mm)

1.2 System Configuration

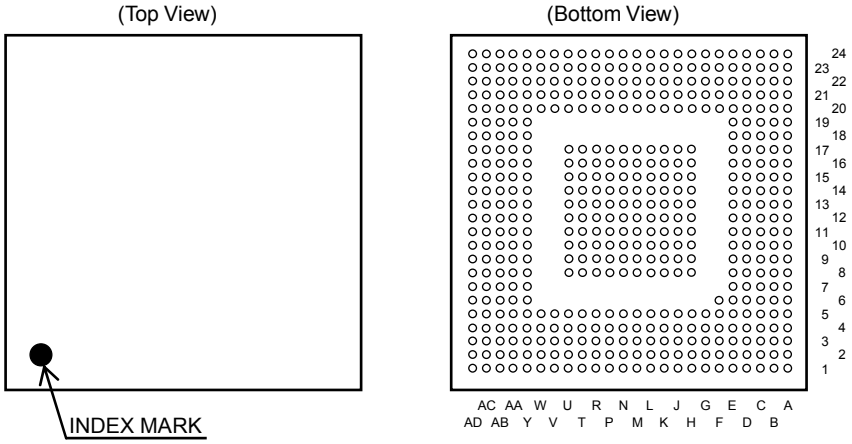
Figure 1-1. EM1-D512 System Configuration



1.3 Pin Layout

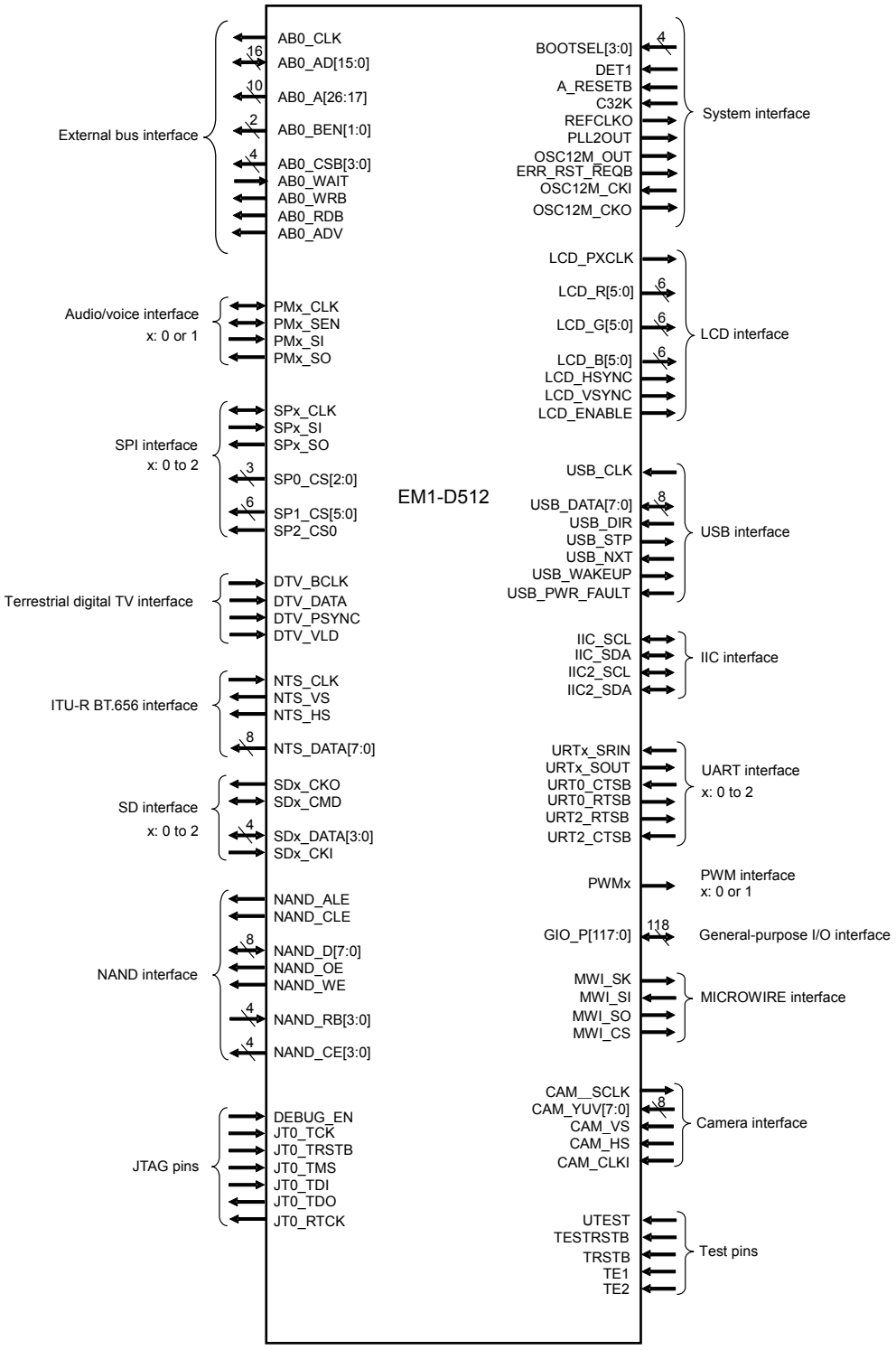
481-pin fine-pitch BGA package (12.7 × 12.7 mm, 0.5 mm pitch)

Figure 1-2. EM1-D512 Pin Layout



2.1 Pin Configuration

2.1.1 EM1-D512 pin layout



2.1.2 EM1-D512 pins

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Pin No.	Type	Pin Name
A1	–	G
A2	–	G
A3	–	G
A4	D	PWM0
A5	D	URT0_SRIN
A6	–	G
A7	–	V
A8	C	PM0_CLK
A9	B	C32K
A10	–	VA2
A11	–	G
A12	–	VA3
A13	–	V
A14	–	VIO3
A15	–	G
A16	D	REFCLKO
A17	Z	OSC12M_CKO
A18	Z	OSC12M_CKI
A19	–	G
A20	–	V
A21	–	VIO18
A22	–	G
A23	–	G
A24	–	G
B1	–	G
B2	–	G
B3	D	URT2_SOUT
B4	D	PWM1
B5	D	URT0_SOUT
B6	–	G
B7	–	V
B8	D	SP0_CLK
B9	C	IIC2_SDA
B10	–	VA2
B11	–	G
B12	–	VA3
B13	–	V
B14	–	VIO3
B15	–	G
B16	D	JT0_TMS
B17	A	DET1
B18	J	LCD_HSYNC
B19	–	G
B20	–	V
B21	–	VIO18
B22	J	LCD_G1
B23	–	G
B24	–	G
C1	–	G
C2	D	DTV_DATA
C3	D	URT2_SRIN
C4	D	URT2_RTSB
C5	D	URT0_RTSB
C6	–	G
C7	–	VIO3
C8	D	SP0_SI
C9	C	IIC2_SCL
C10	C	IIC_SDA
C11	–	VA1
C12	E	BOOTSEL1
C13	D	GIO_P2
C14	–	VIO3
C15	–	G
C16	D	JT0_TDI
C17	D	JT0_RTCK
C18	J	LCD_VSYNC
C19	J	LCD_B3
C20	J	LCD_B0
C21	J	LCD_G3
C22	J	LCD_G2
C23	J	LCD_G0
C24	–	G
D1	C	DTV_BCLK
D2	D	DTV_PSYNC
D3	D	DTV_VLD
D4	D	URT2_CTSB
D5	D	URT0_CTSB
D6	–	G
D7	–	VIO3
D8	D	SP0_SO
D9	D	PM0_SEN
D10	C	IIC_SCL
D11	–	VA1
D12	E	BOOTSEL2
D13	D	GIO_P3
D14	–	VIO3
D15	–	G
D16	D	JT0_TDO
D17	C	JT0_TRSTB
D18	J	LCD_ENABLE
D19	J	LCD_B4
D20	J	LCD_B1
D21	J	LCD_G4
D22	J	LCD_R5
D23	J	LCD_R4
D24	J	LCD_PXCLK
E1	–	V
E2	–	V
E3	–	VIO18
E4	–	VIO18
E5	D	GIO_P6
E6	D	GIO_P5
E7	D	GIO_P4
E8	D	SP0_CS2
E9	D	SP0_CS0
E10	D	PM0_SI
E11	R	TE2
E12	E	BOOTSEL3
E13	E	BOOTSEL0
E14	D	GIO_P0
E15	–	G
E16	C	JT0_TCK
E17	N	TESTRSTB
E18	M	TRSTB
E19	J	LCD_B5
E20	J	LCD_B2
E21	J	LCD_G5
E22	J	LCD_R3
E23	J	LCD_R2
E24	J	LCD_R1
F1	–	G
F2	–	G
F3	–	G
F4	–	G
F5	D	GIO_P7
F6	–	G
F20	J	LCD_R0
F21	M	AB0_CSB3
F22	M	AB0_CSB2

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Pin No.	Type	Pin Name
F23	–	V
F24	–	V
G1	–	VDDQ_DDR
G2	–	VDDQ_DDR
G3	–	VDD_DDR
G4	–	VDD_DDR
G5	D	GIO_P8
G20	M	AB0_CSB1
G21	–	G
G22	–	G
G23	–	G
G24	–	G
H1	C	NTS_CLK
H2	D	NTS_VS
H3	D	NTS_HS
H4	D	NTS_DATA0
H5	D	NTS_DATA5
H8	D	SP0_CS1
H9	D	PM0_SO
H10	D	ERR_RST_REQB
H11	–	G
H12	Q	TE1
H13	C	A_RESETB
H14	D	GIO_P1
H15	–	G
H16	J	DEBUG_EN
H17	E	UTEST
H20	M	AB0_CSB0
H21	–	VDD_DDR
H22	–	VDD_DDR
H23	–	VDD_DDR
H24	–	VDD_DDR
J1	D	NTS_DATA1
J2	D	NTS_DATA2
J3	D	NTS_DATA3
J4	D	NTS_DATA4
J5	D	NTS_DATA6
J8	–	G
J9	–	G
J10	–	G
J11	–	G
J12	–	G
J13	–	G

Pin No.	Type	Pin Name
J14	–	G
J15	–	G
J16	–	G
J17	–	G
J20	M	AB0_WAIT
J21	M	AB0_BEN1
J22	M	AB0_BEN0
J23	M	AB0_A26
J24	M	AB0_A25
K1	C	SD1_CKI
K2	D	SD1_CMD
K3	D	SD1_CKO
K4	D	SD1_DATA0
K5	D	NTS_DATA7
K8	–	G
K9	–	G
K10	–	G
K11	–	G
K12	–	G
K13	–	G
K14	–	G
K15	–	G
K16	–	G
K17	–	IC
K20	M	AB0_A24
K21	M	AB0_A23
K22	M	AB0_A22
K23	M	AB0_A21
K24	M	AB0_A20
L1	D	SD1_DATA1
L2	D	SD1_DATA2
L3	D	SD1_DATA3
L4	D	SD0_CMD
L5	D	SD0_DATA0
L8	–	G
L9	–	G
L10	–	G
L11	–	G
L12	–	G
L13	–	G
L14	–	G
L15	–	G
L16	–	G

Pin No.	Type	Pin Name
L17	–	G
L20	M	AB0_A19
L21	–	V
L22	–	V
L23	–	VIO18
L24	–	VIO18
M1	–	VIO3
M2	–	VIO3
M3	–	VIO3
M4	–	VIO3
M5	D	SD0_DATA1
M8	–	G
M9	–	G
M10	–	G
M11	–	G
M12	–	G
M13	–	G
M14	–	G
M15	–	G
M16	–	G
M17	–	G
M20	M	AB0_A18
M21	–	G
M22	–	G
M23	–	G
M24	–	G
N1	–	G
N2	–	G
N3	–	G
N4	–	G
N5	–	G
N8	–	G
N9	–	G
N10	–	G
N11	–	G
N12	–	G
N13	–	G
N14	–	G
N15	–	G
N16	–	G
N17	–	G
N20	M	AB0_A17
N21	–	VDD_DDR

Remark IC: Internally-connected pins (Leave open.)

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Pin No.	Type	Pin Name
N22	–	VDD_DDR
N23	–	VDD_DDR
N24	–	VDD_DDR
P1	–	VDD_DDR
P2	–	VDD_DDR
P3	–	VDDQ_DDR
P4	–	VDDQ_DDR
P5	–	VDDQ_DDR
P8	–	G
P9	–	G
P10	–	G
P11	–	G
P12	–	G
P13	–	G
P14	–	G
P15	–	G
P16	–	G
P17	–	G
P20	M	AB0_WRB
P21	M	AB0_RDB
P22	P	AB0_AD15
P23	P	AB0_AD14
P24	P	AB0_AD13
R1	C	SD0_CKI
R2	D	SD0_DATA2
R3	D	SD0_DATA3
R4	D	SD2_CMD
R5	D	GIO_P9
R8	–	G
R9	–	G
R10	–	G
R11	–	G
R12	–	G
R13	–	G
R14	–	G
R15	–	G
R16	–	G
R17	–	G
R20	P	AB0_AD12
R21	P	AB0_AD11
R22	P	AB0_AD10
R23	P	AB0_AD9
R24	J	AB0_CLK

Pin No.	Type	Pin Name
T1	D	SD0_CKO
T2	D	SD2_DATA0
T3	D	SD2_DATA1
T4	D	SD2_DATA2
T5	D	GIO_P10
T8	–	G
T9	–	G
T10	–	G
T11	–	G
T12	–	IC
T13	–	IC
T14	–	G
T15	–	G
T16	–	G
T17	–	G
T20	P	AB0_AD8
T21	P	AB0_AD7
T22	P	AB0_AD6
T23	P	AB0_AD5
T24	P	AB0_AD4
U1	–	V
U2	–	V
U3	–	V
U4	–	V
U5	–	V
U8	–	G
U9	–	G
U10	–	G
U11	–	G
U12	–	IC
U13	–	IC
U14	–	IC
U15	–	IC
U16	–	IC
U17	–	G
U20	P	AB0_AD3
U21	–	V
U22	–	V
U23	–	VIO18
U24	–	VIO18
V1	–	G
V2	–	G
V3	–	G

Pin No.	Type	Pin Name
V4	–	G
V5	–	G
V20	P	AB0_AD2
V21	–	G
V22	–	G
V23	–	G
V24	–	G
W1	–	VDDQ_DDR
W2	–	VDDQ_DDR
W3	–	VDD_DDR
W4	–	VDD_DDR
W5	–	IC
W20	P	AB0_AD1
W21	–	VDD_DDR
W22	–	VDD_DDR
W23	–	VDD_DDR
W24	–	VDD_DDR
Y1	–	VIO3
Y2	–	VIO3
Y3	–	VIO3
Y4	–	VIO3
Y5	–	IC
Y6	–	IC
Y7	–	IC
Y8	–	IC
Y9	–	IC
Y10	–	IC
Y11	–	V
Y12	–	IC
Y13	–	IC
Y14	–	IC
Y15	–	IC
Y16	–	IC
Y17	–	IC
Y18	–	IC
Y19	–	IC
Y20	–	IC
Y21	P	AB0_AD0
Y22	G	AB0_ADV
Y23	G	USB_STP
Y24	G	USB_CLK
AA1	C	SD2_CKI
AA2	D	SD2_DATA3

Remark IC: Internally-connected pins (Leave open.)

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Pin No.	Type	Pin Name
AA3	–	IC
AA4	–	IC
AA5	–	IC
AA6	–	G
AA7	–	IC
AA8	–	IC
AA9	–	IC
AA10	–	G
AA11	–	V
AA12	–	IC
AA13	–	IC
AA14	–	IC
AA15	–	G
AA16	–	IC
AA17	–	IC
AA18	–	VIO18
AA19	–	G
AA20	–	IC
AA21	G	USB_DATA7
AA22	G	USB_DATA6
AA23	G	USB_DATA5
AA24	G	USB_NXT
AB1	–	G
AB2	D	SD2_CKO
AB3	–	IC
AB4	–	IC
AB5	–	IC
AB6	–	G
AB7	–	VIO18
AB8	–	IC
AB9	–	IC
AB10	–	G
AB11	–	VIO18
AB12	–	IC
AB13	–	IC
AB14	–	IC
AB15	–	G
AB16	–	IC
AB17	–	IC
AB18	–	VIO18
AB19	–	G
AB20	–	IC
AB21	G	USB_DATA4

Pin No.	Type	Pin Name
AB22	G	USB_DIR
AB23	G	USB_DATA3
AB24	–	G
AC1	–	G
AC2	–	G
AC3	–	IC
AC4	–	IC
AC5	–	V
AC6	–	G
AC7	–	VIO18
AC8	–	IC
AC9	–	IC
AC10	–	G
AC11	–	VIO18
AC12	–	IC
AC13	–	IC
AC14	–	IC
AC15	–	G
AC16	–	IC
AC17	–	IC
AC18	–	V
AC19	–	G
AC20	–	IC
AC21	G	USB_DATA1
AC22	G	USB_DATA2
AC23	–	G
AC24	–	G
AD1	–	G
AD2	–	G
AD3	–	G
AD4	–	IC
AD5	–	V
AD6	–	G
AD7	–	VIO18
AD8	–	IC
AD9	–	IC
AD10	–	G
AD11	–	VIO18
AD12	–	IC
AD13	–	IC
AD14	–	IC
AD15	–	G
AD16	–	IC

Pin No.	Type	Pin Name
AD17	–	IC
AD18	–	V
AD19	–	G
AD20	–	IC
AD21	G	USB_DATA0
AD22	–	G
AD23	–	G
AD24	–	G

2.2 Pin Functions

(1) Boot select signals (VIO18)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
BOOTSEL3	E12	Input	Boot mode selection 3	–	E	–
BOOTSEL2	D12	Input	Boot mode selection 2	–	E	–
BOOTSEL1	C12	Input	Boot mode selection 1	–	E	–
BOOTSEL0	E13	Input	Boot mode selection 0	–	E	–

(2) System control signals (VIO3 / VIO18)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
DET1	B17	Input	Power-on reset	–	A	.–
A_RESETB	H13	Input	System reset	–	C	.–
C32K	A9	Input	Reference clock (32.768 kHz)	–	B	–.
REFCLKO	A16	Output	Reference clock	PLL2OUT OSC12M_OUT	D	Leave open.
PLL2OUT	A16	Output	Internal PLL2 output	REFCLKO OSC12M_OUT	D	Leave open.
OSC12M_OUT	A16	Output	Internal OSC output	REFCLKO PLL2OUT	D	Leave open.
ERR_RST_REQB	H10	Output	Error reset request	–	D	Leave open.
OSC12M_CKI Note	A18	Input	OSC XT1	–	Z	Leave open.
OSC12M_CKO Note	A17	Output	OSC XT2	–	Z	Leave open.

Note VIO18

(3) External bus interface signals (VIO18)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
AB0_CLK	R24	Output	Clock	GIO_P11 NTS_CLK	J	Leave open.
AB0_AD[15:0]	P22, P23, P24, R20, R21, R22, R23, T20, T21, T22, T23, T24, U20, V20, W20, Y21	I/O	Data	GIO_P[27:12]	P	Leave open.
AB0_A[26:20]	J23, J24, K20, K21, K22, K23, K24	Output	Address	GIO_P[37:31] AB0_A[10:4]	M	Leave open.
AB0_A[19:17]	L20, M20, N20	Output	Address	GIO_P[30:28] NTS_DATA[2:0] AB0_A[3:1]	M	Leave open.
AB0_A[10:4]	J23, J24, K20, K21, K22, K23, K24	Output	Address	GIO_P[37:31] AB0_A[26:20]	M	Leave open.
AB0_A[3:1]	L20, M20, N20	Output	Address	GIO_P[30:28] NTS_DATA[2:0] AB0_A[19:17]	M	Leave open.
AB0_BEN[1:0]	J21, J22	Output	Byte enable	GIO_P[47:46]	M	Leave open.
AB0_CSB3	F21	Output	Chip select	GIO_P45 NTS_HS	M	Leave open.
AB0_CSB2	F22	Output	Chip select	GIO_P44 NTS_VS	M	Leave open.
AB0_CSB1	G20	Output	Chip select	GIO_P43 NTS_DATA7	M	Leave open.
AB0_CSB0	H20	Output	Chip select	GIO_P42 NTS_DATA6	M	Leave open.
AB0_WAIT	J20	Input	Wait	GIO_P41 NTS_DATA5	M	Leave open.
AB0_WRB	P20	Output	Write strobe	GIO_P40 NTS_DATA4	M	Leave open.
AB0_RDB	P21	Output	Read strobe	GIO_P39 NTS_DATA3	M	Leave open.
AB0_ADV	Y22	Output	Address enable	GIO_P38	G	Leave open.

(4) Audio interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
PM0_CLK	A8	I/O	PCM0 clock (default input)	–	C	Leave open.
PM0_SEN	D9	I/O	PCM0 frame synchronization (default input)	–	D	Leave open.
PM0_SI	E10	Input	PCM0 data	GIO_P87	D	Leave open.
PM0_SO	H9	Output	PCM0 data	–	D	Leave open.
PM1_CLK	H1	I/O	PCM1 clock (default input)	GIO_P72 NTS_CLK	C	Leave open.
PM1_SEN	H5	I/O	PCM1 frame synchronization (default input)	GIO_P80 NTS_DATA5 SP1_CS4	D	Leave open.
PM1_SI	J5	Input	PCM1 data	GIO_P81 NTS_DATA6 SP1_CS5	D	Leave open.
PM1_SO	K5	Output	PCM1 data	GIO_P82 NTS_DATA7	D	Leave open.

(5) Camera interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
CAM_SCLK	E6	Output	Camera clock	GIO_P5, NAND_RB2	D	Leave open.
CAM_CLKI	K1	Input	Camera interface	GIO_P92, SD1_CKI	C	Leave open.
CAM_YUV7	L1	Input	Camera interface	SD1_DATA1	D	Leave open.
CAM_YUV6	K4	Input	Camera interface	SD1_DATA0	D	Leave open.
CAM_YUV5	K2	Input	Camera interface	SD1_CMD	D	Leave open.
CAM_YUV4	J4	Input	Camera interface	NTS_DATA4, SP1_CS3, GIO_P79	D	Leave open.
CAM_YUV3	J3	Input	Camera interface	NTS_DATA3, SP1_CS2, GIO_P78	D	Leave open.
CAM_YUV2	J2	Input	Camera interface	NTS_DATA2, SP1_CS1, GIO_P77	D	Leave open.
CAM_YUV1	J1	Input	Camera interface	NTS_DATA1, SP1_CS0, GIO_P76	D	Leave open.
CAM_YUV0	H4	Input	Camera interface	NTS_DATA0, SP1_SO, GIO_P75	D	Leave open.
CAM_HS	L3	Input	Camera interface	SD1_DATA3	D	Leave open.
CAM_VS	L2	Input	Camera interface	SD1_DATA2	D	Leave open.

(6) SPI interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
SP0_CLK	B8	I/O	SPI0 clock output	MWI_SK	D	Leave open.
SP0_SI	C8	Input	SPI0 data	MWI_SI	D	Leave open.
SP0_SO	D8	Output	SPI0 data	MWI_SO	D	Leave open.
SP0_CS0	E9	I/O	SPI0 chip select	MWI_CS	D	Leave open.
SP0_CS[2:1]	E8, H8	Output	SPI0 chip select	GIO_P[49:48]	D	Leave open.
SP1_CLK	H2	I/O	SPI1 clock input	GIO_P73 NTS_VS	D	Leave open.
SP1_SI	H3	Input	SPI1 data	GIO_P74 NTS_HS	D	Leave open.
SP1_SO	H4	Output	SPI1 data	GIO_P75 NTS_DATA0 CAM_YUV0	D	Leave open.
SP1_CS5	J5	Output	SPI1 chip select	GIO_P81 NTS_DATA6 PM1_SI	D	Leave open.
SP1_CS4	H5	Output	SPI1 chip select	GIO_P80 NTS_DATA5 PM1_SEN	D	Leave open.
SP1_CS[3:1]	J4, J3, J2	Output	SPI1 chip select	GIO_P[79:77] NTS_DATA[4:2] CAM_YUV[4:2]	D	Leave open.
SP1_CS0	J1	I/O	SPI1 chip select	GIO_P76 NTS_DATA1 CAM_YUV1	D	Leave open.
SP2_CLK	D1	I/O	SPI2 clock input	DTV_BCLK	C	Leave open.
SP2_SI	C2	Input	SPI2 data	DTV_DATA	D	Leave open.
SP2_SO	D2	Output	SPI2 data	DTV_PSYNC	D	Leave open.
SP2_CS0	D3	I/O	SPI2 chip select	DTV_VLD	D	Leave open.

(7) Terrestrial digital TV interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
DTV_BCLK	D1	Input	Clock	SP2_CLK	C	Leave open.
DTV_DATA	C2	Input	YUV data	SP2_SI	D	Leave open.
DTV_PSYNC	D2	Input	Vertical synchronization	SP2_SO	D	Leave open.
DTV_VLD	D3	Input	Horizontal synchronization	SP2_CS0	D	Leave open.

(8) LCD interface signals (VIO18)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
LCD_PXCLK	D24	Output	Pixel clock	GIO_P50	J	Leave open.
LCD_R[5:0]	D22, D23, E22, E23, E24, F20	Output	Red data	GIO_P[56:51]	J	Leave open.
LCD_G[5:0]	E21, D21, C21, C22, B22, C23	Output	Green data	GIO_P[62:57]	J	Leave open.
LCD_B[5:0]	E19, D19, C19, E20, D20, C20	Output	Blue data	GIO_P[68:63]	J	Leave open.
LCD_HSYNC	B18	Output	Horizontal synchronization	GIO_P69	J	Leave open.
LCD_VSYNC	C18	Output	Vertical synchronization	GIO_P70	J	Leave open.
LCD_ENABLE	D18	Output	Data enable	GIO_P71	J	Leave open.

(9) USB interface signals (VIO18 / VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
USB_CLK	Y24	Input	Clock	GIO_P96	G	Leave open.
USB_DATA[7:0]	AA21, AA22, AA23, AB21, AB23, AC22, AC21, AD21	I/O	USB data	GIO_P[104:97]	G	Leave open.
USB_DIR	AB22	Input	USB DIR input	GIO_P105	G	Leave open.
USB_STP	Y23	Output	USB STOP output	GIO_P106	G	Leave open.
USB_NXT	AA24	Input	USB NXT input	GIO_P107	G	Leave open.
USB_WAKEUP[Note]	H14	Output	Suspend wakeup	GIO_P1 USB_PWR_FAULT	D	Leave open.
USB_PWR_FAULT[Note]	H14	Input	Power fault	GIO_P1 USB_WAKEUP	D	Leave open.

Note VIO3

(10) ITU-R BT.656 interface signals (VIO3 / VIO18)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
NTS_CLK	H1	Input	Clock	GIO_P72, PM1_CLK	C	Leave open.
	R24 Note			AB0_CLK, GIO_P11	J	Leave open.
NTS_VS	H2	Output	Vertical synchronization	GIO_P73, SP1_CLK	D	Leave open.
	F22 Note			AB0_CSB2, GIO_P44	M	Leave ope
NTS_HS	H3	Output	Horizontal synchronization	GIO_P74, SP1_SI	D	Leave open.
	F21 Note			AB0_CSB3, GIO_P45	M	Leave open.
NTS_DATA7	K5	Output	NTSC data	GIO_P82, PM1_SO	D	Leave open.
	G20 Note			AB0_CSB1, GIO_P43	M	Leave open
NTS_DATA6	J5	Output	NTSC data	GIO_P81, SP1_CS5 PM1_SI	D	Leave open.
	H20 Note			AB0_CSB0, GIO_P42	M	Leave open
NTS_DATA5	H5	Output	NTSC data	GIO_P80, SP1_CS4 PM1_SEN	D	Leave open.
	J20 Note			AB0_WAIT, GIO_P41	M	Leave open
NTS_DATA4	J4	Output	NTSC data	GIO_P79, SP1_CS3 CAM_YUV4	D	Leave open.
	P20 Note			AB0_WRB, GIO_P40	M	Leave open
NTS_DATA3	J3	Output	NTSC data	GIO_P78, SP1_CS2 CAM_YUV3	D	Leave open.
	P21 Note			AB0_RDB, GIO_P39	M	Leave open.
NTS_DATA2	J2	Output	NTSC data	GIO_P77, SP1_CS1 CAM_YUV2	D	Leave open.
	L20 Note			AB0_A3, AB0_A19 GIO_P30	M	Leave open.
NTS_DATA1	J1	Output	NTSC data	GIO_P76, SP1_CS0 CAM_YUV1	D	Leave open.
	M20 Note			AB0_A2, AB0_A18 GIO_P29	M	Leave open.
NTS_DATA0	H4	Output	NTSC data	GIO_P75, SP1_SO CAM_YUV0	D	Leave open.
	N20 Note			AB0_A1, AB0_A17 GIO_P28	M	Leave ope

Note VIO18

(11) IIC interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
IIC_SCL	D10	Output	Serial clock output	GIO_P83	C	Leave open.
IIC_SDA	C10	I/O	Serial data output	GIO_P84	C	Leave open.
IIC2_SCL	C9	Output	Serial clock output	NAND_WE	C	Leave open.
IIC2_SDA	B9	I/O	Serial data output	NAND_RB0	C	Leave open.

(12) UART interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
URT0_SRIN	A5	Input	Serial data	–	D	Leave open.
URT0_SOUT	B5	Output	Serial data	–	D	Leave open.
URT0_CTSB	D5	Input	Data transmission/reception ready in destination device	GIO_P85 URT1_SRIN	D	Leave open.
URT1_SOUT	C5	Output	Data transmission/reception ready	GIO_P86 URT1_SOUT	D	Leave open.
URT1_SRIN	D5	Input	Serial data	GIO_P85 URT0_CTSB	D	Leave open.
URT1_SOUT	C5	Output	Serial data	GIO_P86 URT0_RTSB	D	Leave open.
URT2_SRIN	C3	Input	Serial data	GIO_P108 NAND_ALE	D	Leave open.
URT2_SOUT	B3	Output	Serial data	GIO_P109 NAND_CLE	D	Leave open.
URT2_CTSB	D4	Input	Data transmission/reception ready in destination device	GIO_P110 NAND_D0	D	Leave open.
URT2_RTSB	C4	Output	Data transmission/reception ready	GIO_P111 NAND_D1	D	Leave open.

(13) Memory card interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
SD0_CKO	T1	Output	Clock	–	D	Leave open.
SD0_CMD	L4	I/O	Command response	–	D	Leave open.
SD0_DATA[3:1]	R3, R2, M5	I/O	Data	GIO_P[90:88]	D	Leave open.
SD0_DATA0	L5	I/O	Data	–	D	Leave open.
SD0_CKI	R1	Input	Loop back	GIO_P91	C	Leave open.
SD1_CKO	K3	Output	Clock	–	D	Leave open.
SD1_CMD	K2	I/O	Command response	CAM_YUV5	D	Leave open.
SD1_DATA3	L3	I/O	Data	CAM_HS	D	Leave open.
SD1_DATA2	L2	I/O	Data	CAM_VS	D	Leave open.
SD1_DATA1	L1	I/O	Data	CAM_YUV7	D	Leave open.
SD1_DATA0	K4	I/O	Data	CAM_YUV6	D	Leave open.
SD1_CKI	K1	Input	Loop back	GIO_P92 CAM_CLKI	C	Leave open.
SD2_CKO	AB2	Output	Clock	GIO_P112 NAND_D2	D	Leave open.
SD2_CMD	R4	I/O	Command response	GIO_P113 NAND_D#	D	Leave open
SD2_DATA[3:0]	AA2, T4 T3, T2	I/O	Data	GIO_P[117:114] NAND_D[7:4]	D	Leave open
SD2_CKI	AA1	Input	Loop back	GIO_P93 NAND_OE	C	Leave open

(14) PWM interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
PWM0	A4	Output	PWM output	GIO_P94	D	Leave open.
PWM1	B4	Output	PWM output	GIO_P95	D	Leave open.

(15) General-purpose I/O interface signals (VIO18 / VIO3)

(1/3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
GIO_P[117:114]	AA2, T4, T3, T2	I/O	General-purpose IO	SD2_DATA[3:0] NAND_D[7:4]	D	Leave open.
GIO_P113	R4	I/O	General-purpose IO	SD2_CMD NAND_D3	D	Leave open.
GIO_P112	AB2	I/O	General-purpose IO	SD2_CKO NAND_D2	D	Leave open.
GIO_P111	C4	I/O	General-purpose IO	URT2_RTSB NAND_D1	D	Leave open.
GIO_P110	D4	I/O	General-purpose IO	URT2_CTSB NAND_D0	D	Leave open.
GIO_P109	B3	I/O	General-purpose IO	URT2_SOUT NAND_CLE	D	Leave open.
GIO_P108	C3	I/O	General-purpose IO	URT2_SRIN NAND_ALE	D	Leave open.
GIO_P107 Note	AA24	I/O	General-purpose IO	USB_NXT	G	Leave open.
GIO_P106 Note	Y23	I/O	General-purpose IO	USB_STP	G	Leave open.
GIO_P105 Note	AB22	I/O	General-purpose IO	USB_DIR	G	Leave open.
GIO_P[104:97] Note	AA21, AA22, AA23, AB21, AB23, AC22, AC21, AD21	I/O	General-purpose IO	USB_DATA[7:0]	G	Leave open.
GIO_P96 Note	Y24	I/O	General-purpose IO	USB_CLK	G	Leave open.
GIO_P[95:94]	B4, A4	I/O	General-purpose IO	PWM[1:0]	D	Leave open.
GIO_P93	AA1	I/O	General-purpose IO	SD2_CKI NAND_OE	C	Leave open.
GIO_P92	K1	I/O	General-purpose IO	SD1_CKI CAM_CLKI	C	Leave open.
GIO_P91	R1	I/O	General-purpose IO	SD0_CKI	C	Leave open.
GIO_P[90:88]	R3, R2, M5	I/O	General-purpose IO	SD0_DATA[3:1]	D	Leave open.
GIO_P87	E10	I/O	General-purpose IO	PM0_SI	D	Leave open.
GIO_P86	C5	I/O	General-purpose IO	URT0_RTSB URT1_SOUT	D	Leave open.
GIO_P85	D5	I/O	General-purpose IO	URT0_CTSB URT1_SRIN	D	Leave open.
GIO_P84	C10	I/O	General-purpose IO	IIC_SDA	C	Leave open.
GIO_P83	D10	I/O	General-purpose IO	IIC_SCL	C	Leave open.
GIO_P82	K5	I/O	General-purpose IO	NTS_DATA7 PM1_SO	D	Leave open.

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Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
GIO_P81	J5	I/O	General-purpose IO	NTS_DATA6 SP1_CS5 PM1_SI	D	Leave open.
GIO_P80	H5	I/O	General-purpose IO	NTS_DATA5 SP1_CS4 PM1_SEN	D	Leave open.
GIO_P[79:76]	J4, J3, J2, J1	I/O	General-purpose IO	NTS_DATA[4:1] SP1_CS[3:0] CAM_YUV[4:1]	D	Leave open.
GIO_P75	H4	I/O	General-purpose IO	NTS_DATA0 SP1_SO CAM_YUV0	D	Leave open.
GIO_P74	H3	I/O	General-purpose IO	NTS_HS SP1_SI	D	Leave open.
GIO_P73	H2	I/O	General-purpose IO	NTS_VS SP1_CLK	D	Leave open.
GIO_P72	H1	I/O	General-purpose IO	NTS_CLK PM1_CLK	C	Leave open.
GIO_P71 Note	D18	I/O	General-purpose IO	LCD_ENABLE	J	Leave open.
GIO_P70 Note	C18	I/O	General-purpose IO	LCD_VSYNC	J	Leave open.
GIO_P69 Note	B18	I/O	General-purpose IO	LCD_HSYNC	J	Leave open.
GIO_P[68:63] Note	E19, D19, C19, E20, D20, C20	I/O	General-purpose IO	LCD_B[5:0]	J	Leave open.
GIO_P[62:57] Note	E21, D21, C21, C22, B22, C23	I/O	General-purpose IO	LCD_G[5:0]	J	Leave open.
GIO_P[56:51] Note	D22, D23, E22, E23, E24, F20	I/O	General-purpose IO	LCD_R[5:0]	J	Leave open.
GIO_P50 Note	D24	I/O	General-purpose IO	LCD_PXCLK	J	Leave open.
GIO_P[49:48] Note	E8, H8	I/O	General-purpose IO	SP0_CS[2:1]	D	Leave open.
GIO_P[47:46] Note	J21, J22	I/O	General-purpose IO	AB0_BEN[1:0]	M	Leave open.
GIO_P45 Note	F21	I/O	General-purpose IO	AB0_CSB3 NTS_HS	M	Leave open.
GIO_P44 Note	F22	I/O	General-purpose IO	AB0_CSB2 NTS_VS	M	Leave open.
GIO_P43 Note	G20	I/O	General-purpose IO	AB0_CSB1 NTS_DATA7	M	Leave open.
GIO_P42 Note	H20	I/O	General-purpose IO	AB0_CSB0 NTS_DATA6	M	Leave open.
GIO_P41 Note	J20	I/O	General-purpose IO	AB0_WAIT NTS_DATA5	M	Leave open.
GIO_P40 Note	P20	I/O	General-purpose IO	AB0_WRB NTS_DATA4	M	Leave open.

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Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
GIO_P39 Note	P21	I/O	General-purpose IO	AB0_RDB NTS_DATA3	M	Leave open.
GIO_P38 Note	Y22	I/O	General-purpose IO	AB0_ADV	G	Leave open.
GIO_P[37:31] Note	J23, J24, K20, K21, K22, K23, K24	I/O	General-purpose IO	AB0_A[26:20] AB0_A[10:4]	M	Leave open.
GIO_P[30:28] Note	L20, M20, N20	I/O	General-purpose IO	AB0_A[19:17] NTS_DATA[2:0] AB0_A[3:1]	M	Leave open.
GIO_P[27:12] Note	P22, P23, P24, R20, R21, R22, R23, T20, T21, T22, T23, T24, U20, V20, W20, Y21	I/O	General-purpose IO	AB0_AD[15:0]	P	Leave open.
GIO_P11 Note	R24	I/O	General-purpose IO	AB0_CLK NTS_CLK	J	Leave open.
GIO_P[10:7]	T5, R5, G5, F5	I/O	General-purpose IO	NAND_CE[3:0]	D	Leave open.
GIO_P6	E5	I/O	General-purpose IO	NAND_RB3	D	Leave open.
GIO_P5	E6	I/O	General-purpose IO	NAND_RB2 CAM_SCLK	D	Leave open.
GIO_P4	E7	I/O	General-purpose IO	NAND_RB1	D	Leave open.
GIO_P[3:2]	D13, C13	I/O	General-purpose IO	–	D	Leave open.
GIO_P1	H14	I/O	General-purpose IO	USB_WAKEUP USB_PWR_FAULT	D	Leave open.
GIO_P0	E14	I/O	General-purpose IO	–	D	Leave open.

Note VIO18

(16) MICROWIRE interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
MWI_SK	B8	Output	Clock	SP0_CLK	D	Leave open.
MWI_SI	C8	Input	Data	SP0_SI	D	Leave open.
MWI_SO	D8	Output	Data	SP0_SO	D	Leave open.
MWI_CS	E9	Output	Chip select	SP0_CS0	D	Leave open.

(17) NAND Flash interface signals (VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
NAND_ALE	C3	Output	Address latch enable	URT2_SRIN GIO_P108	D	Leave open.
NAND_CLE	B3	Output	Command latch enable	URT2_SOUT GIO_P109	D	Leave open.
NAND_D[7:4]	AA2, T4, T3, T2	I/O	Data	SD2_DATA[3:0] GIO_P[117:114]	D	Leave open.
NAND_D3	R4	I/O	Data	SD2_CMD GIO_P113	D	Leave open.
NAND_D2	AB2	I/O	Data	SD2_CKO GIO_P112	D	Leave open.
NAND_D1	C4	I/O	Data	URT2_RTSB GIO_P111	D	Leave open.
NAND_D0	D4	I/O	Data	URT2_CTSB GIO_P110	D	Leave open.
NAND_OE	AA1	Output	Output enable	SD2_CKI GIO_P93	C	Leave open.
NAND_WE	C9	Output	Write enable	IIC2_SCL	C	Leave open.
NAND_RB0	B9	Input	Ready busy	IIC2_SDA	C	Leave open.
NAND_RB3	E5	Input	Ready busy	GIO_P6	D	Leave open.
NAND_RB2	E6	Input	Ready busy	GIO_P5 CAM_SCLK	D	Leave open.
NAND_RB1	E7	Input	Ready busy	GIO_P4	D	Leave open.
NAND_CE[3:0]	T5, R5, G5, F5	Output	Chip enable	GIO_P[10:7]	D	Leave open.

(18) JTAG signals (VIO18 / VIO3)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
DEBUG_EN Note	H16	Input	JTAG	–	J	Leave open.
JT0_TCK	E16	Input	JTAG	–	C	Leave open.
JT0_TRSTB	D17	Input	JTAG	–	C	Leave open.
JT0_TMS	B16	Input	JTAG	–	D	Leave open.
JT0_TDI	C16	Input	JTAG	–	D	Leave open.
JT0_TDO	D16	Output	JTAG	–	D	Leave open.
JT0_RTCK	C17	Output	JTAG	–	D	Leave open.

Note VIO18

(19) Test signals (VIO18)

Pin Name	Pin No.	I/O	Function	Alternate Pin Function	Type	Handling When Not Used
UTEST	H17	Input	Test pin (usually fixed to 0)	–	E	“L” level hold.
TESTRSTB	E17	Input	Asynchronous reset for testing	–	N	Leave open.
TRSTB	E18	Input	Test pin	–	M	Leave open.
TE1	H12	Input	Test pin	–	Q	Leave open.
TE2	E11	Input	Test pin	–	R	Leave open.

(20) Power supply

Pin Name	Pin No.	I/O	Function	Type	Handling When Not Used
V	A7, A13, A20, B7, B13, B20, E1, E2, F23, F24, L21, L22, U1, U2, U3, U4, U5, U21, U22, Y11, AA11, AC5, AC18, AD5, AD18	–	Core power supply (1.2 V)	–	–
VIO18	A21, B21, E3, E4, L23, L24, U23, U24, AA18, AB7, AB11, AB18, AC7, AC11, AD7, AD11	–	IO power supply (1.8 V system)	–	–
VIO3	A14, B14, C7, C14, D7, D14, M1, M2, M3, M4, Y1, Y2, Y3, Y4	–	IO power supply (3 V system)	–	–
VA1	C11, D11	–	PLL power supply (1.2V)	–	–
VA2	A10, B10	–	PLL power supply (1.2V)	–	–
VA3	A12, B12	–	PLL power supply (1.2V)	–	–
VDDQ_DDR	G1, G2, P3, P4, P5, W1, W2	–	DDR power supply (1.8V)	–	–
VDD_DDR	G3, G4, H21, H22, H23, H24, N21, N22, N23, N24, P1, P2, W3, W4, W21, W22, W23, W24	–	DDR power supply (1.8V)	–	–

(21) GND

Pin Name	Pin No.	I/O	Function	Type	Handling When Not Used
G	A1, A2, A3, A6, A11, A15, A19, A22, A23, A24, B1, B2, B6, B11, B15, B19, B23, B24, C1, C6, C15, C24, D6, D15, E15, F1, F2, F3, F4, F6, G21, G22, G23, G24, H11, H15, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17,K8, K9, K10, K11, K12, K13, K14, K15, K16, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, M21, M22, M23, M24, N1, N2, N3, N4, N5, N8, N9, N10, N11, N12, N13, N14, N15, N16, N17, P8, P9, P10, P11, P12, P13, P14, P15, P16, P17, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, T8, T9, T10, T11, T14, T15, T16, T17, U8, U9, U10, U11, U17, V1, V2, V3, V4, V5, V21, V22, V23, V24, AA6, AA10, AA15, AA19, AB1, AB6, AB10, AB15, AB19, AB24, AC1, AC2, AC6, AC10, AC15, AC19, AC23, AC24, AD1, AD2, AD3, AD6, AD10, AD15, AD19, AD22, AD23, AD24	–	GND	–	–

(22) Other

Pin Name	Pin No.	I/O	Function	Type	Handling When Not Used
IC	K17, T12, T13, U12, U13, U14, U15, U16, W5, Y5, Y6, Y7, Y8, Y9, Y10, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, AA3, AA4, AA5, AA7, AA8, AA9, AA12, AA13, AA14, AA16, AA17, AA20, AB3, AB4, AB5, AB8, AB9, AB12, AB13, AB14, AB16, AB17, AB20, AC3, AC4, AC8, AC9, AC12, AC13, AC14, AC16, AC17, AC20, AD4, AD8, AD9, AD12, AD13, AD14, AD16, AD17, AD20	–	Internally-connected pins	–	–

2.2.1 Pin I/O circuits

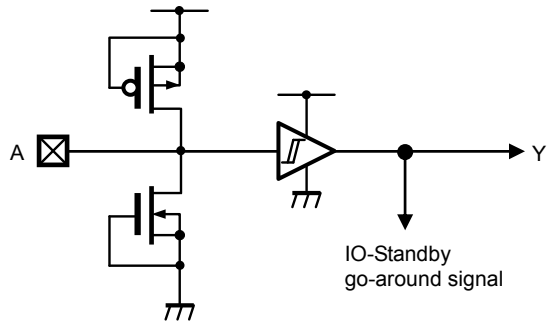
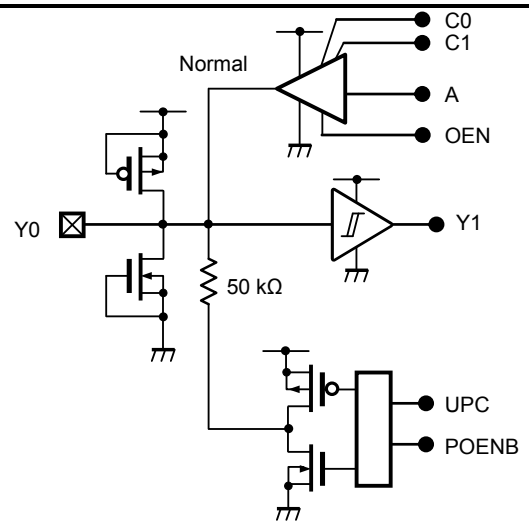
This section shows the types of I/O circuits used in EM1-D512. The correspondence between circuits and pins is shown in the table below.

Type	VDD	IO	Schmitt	AND	Low Noise	Pull Down	Pull Up	Bus Hold	Drive Current	Remark
A	3 3V	IN	√	×	×	×	×	×	–	For DET1
B	3.3 V	IO	√	×	×	√	√	×	2/4/8/12	
C	3.3 V	IO	√	×	×	√	√	×	2/4/6/8	
D	3.3 V	IO	×	√	×	√	√	×	2/4/6/8	
E	1.8 V	IO	√	×	×	√	√	×	2/4/8/12	
F	1.8 V	IO	×	√	×	√	√	×	2/4/8/12	
G	1.8 V	IO	×	√	×	√	√	×	2/4/8/12	
J	1.8 V	IO	√	√	×	√	√	×	2/4/8/12	
M	1.8 V	IO	√	×	√	√	√	×	2/4/6/8	
N	1.8 V	IO	√	×	√	√	√	×	2/4/6/8	
P	1.8 V	IO	×	×	×	×	×	√	2/4/8/12	
Q	1.8 V	IN	×	×	×	√	×	×	–	For testing
R	1.8 V	IN	×	×	×	√	×	×	–	For testing
Z	3.3 V	IO	–	–	–	–	–	–	–	

Remark √: Supported, ×: Not supported, –: Don't care

2.2.2 I/O circuits

(1/4)

Type A	Description
	Input buffer Schmitt (VIO3) w / IO-Standby Control Other IO buffers are fixed on the time of Power OFF mode in POW OFF state of appendix D by inputting the Low level to this buffer. **Remark** In the Power-off mode, pins remain in a Hi-Z state (input) and the signals are passed through this buffer.
Types B, E	**Description**
	Bidirectional buffer Schmitt (type B = VIO3, type E = VIO18) w / IOLH CONTROL Normal / Pull-up 50 kΩ / Pull-down 50 kΩ • During power-off: Pins remain in a Hi-Z state • Resistance = 50 kΩ (typ.)

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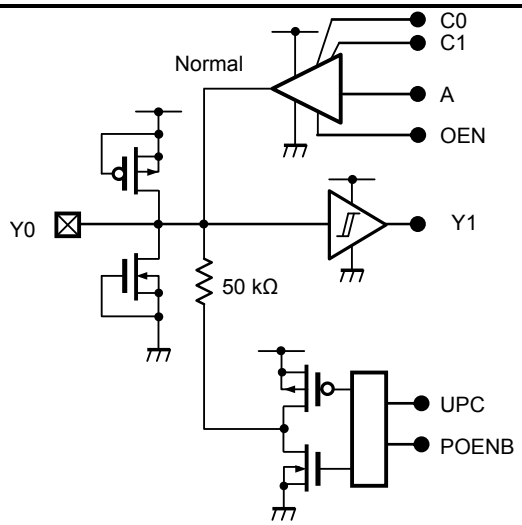
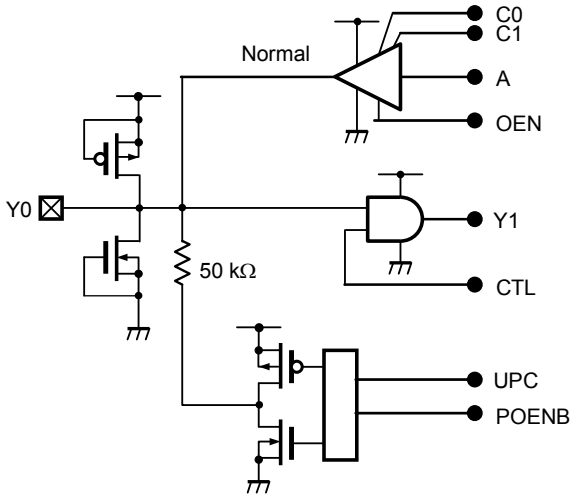
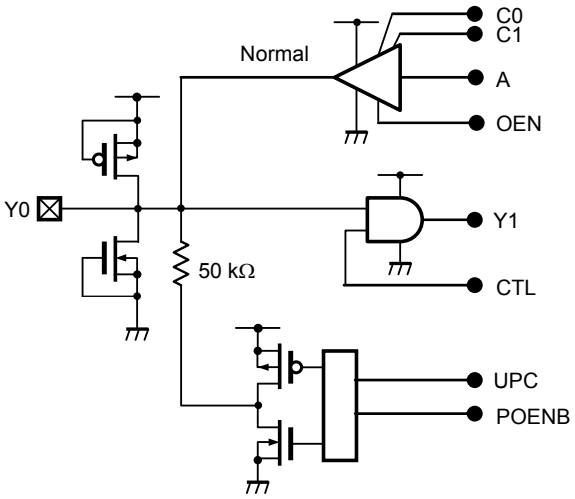
Type C	Description
	Bidirectional buffer Schmitt (VIO3) w / IOLH CONTROL Normal / Pull-up 50 kΩ / Pull-down 50 kΩ • During power-off: Pins remain in a Hi-Z state (masked by 0 internally) • Resistance = 50 kΩ (typ.)

Type D	Description
	Bidirectional buffer AND (VIO3) w / IOLH CONTROL Normal / Pull-up 50 kΩ / Pull-down 50 kΩ • During power-off: Pins remain in a Hi-Z state (masked by 0 internally) • Resistance = 50 kΩ (typ.)

Types G	Description
	Bidirectional buffer AND (VIO18) w / IOLH CONTROL Normal / Pull-up 50 kΩ Pull-down 50 kΩ • During power-off: Type G: Pins are pulled down (masked by 0 internally) • Resistance = 50 kΩ (typ.)

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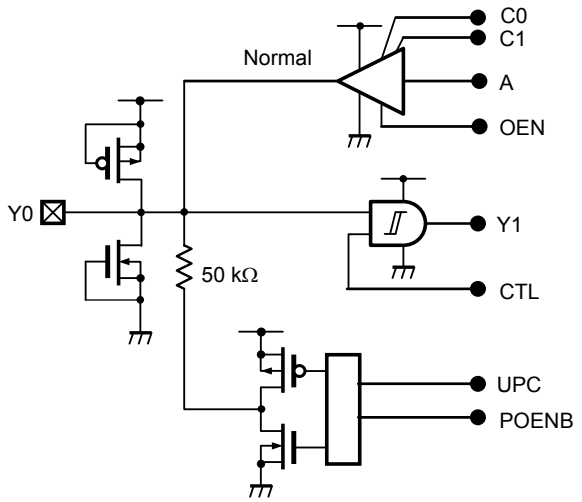
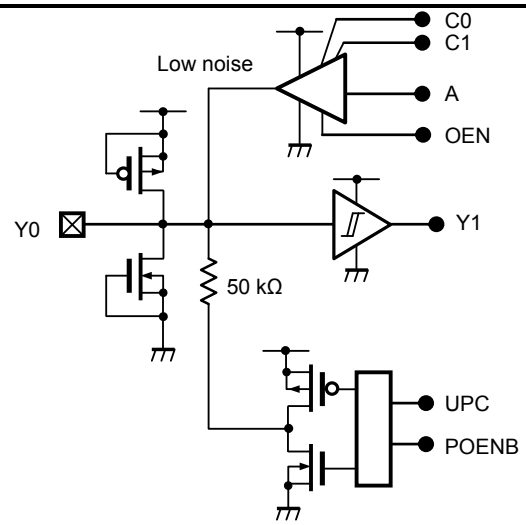
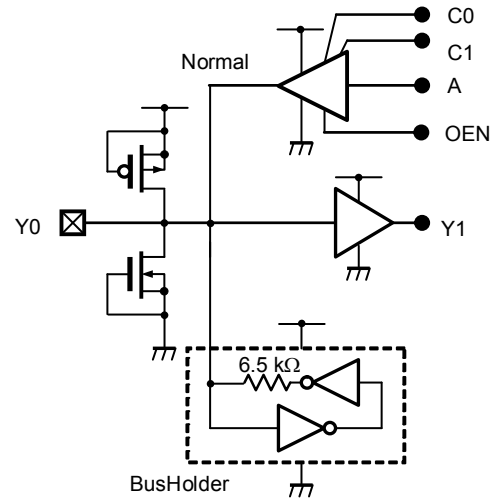
Type J	Description
	Bidirectional buffer AND, Schmitt (VIO18) w / IOLH CONTROL Normal / Pull-up 50 kΩ / Pull-down 50 kΩ • During power-off: Pins are pulled down (masked by 0 internally) • Resistance = 50 kΩ (typ.)

Types M, N	Description
	Bidirectional buffer Schmitt / LowNoise (VIO18) w / IOLH CONTROL Normal / Pull-up 50 kΩ / Pull-down 50 kΩ • During power-off Type M: Pins are pulled down (masked by 0 internally) Type N: Pins are pulled up (masked by 0 internally) • Resistance = 50 kΩ (typ.)

Type P	Description
	Bidirectional buffer (VIO18) w / IOLH control busholder • During power-off: Pins output a low level (masked by 0 internally) • Resistance = 6.5 kΩ (typ.)

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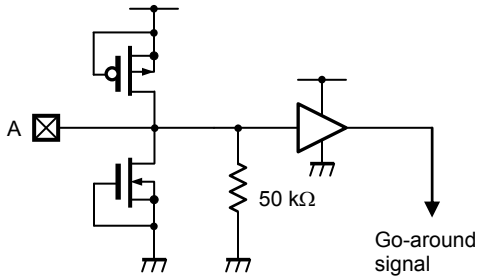
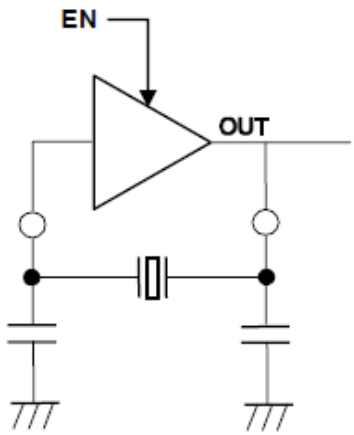
Types Q, R	Description
	Test buffer (VIO18) Types Q and R are buffers used exclusively for testing. Leave open when used in the actual device. (Always pull down the pins (typ. 50 kΩ)
Type Z	**Description**
	oscillator

CHAPTER 3 DESCRIPTION OF FUNCTIONS

3.1 System Functions

3.1.1 System management unit (ASMU)

The ASMU resets the EM1-D512 clocks and controls the power supply switching. The ASMU has the following functions.

- ○ Generation of clock and control
- ○ Generation of reset and control
- ○ Control of PLL
- ○ Control of power supply switching and barrier gates
- ○ Automatic sequencer for power supply state transition

3.1.2 Power management unit (PMU)

PMU is power supply on/off control and the module to do a clock change. But, power control of ADSP isn't performed in PMU (ACPU controls.) The part is controlled by HW sequence in ASMU. Power control method of PMU gets command executable format. (It's to assume that that is applicable to the various situations of the peripheral equipment and the power management flexibly.). SP1 isn't controlled from PMU.

- ○ QuickRecovery processing of ACPU is performed.
- ○ It's possible to change the number of on/off control cycle of the clock of PCLK.
- ○ The capacity of the command buffer is RAM 4KB (32bitx, 1024word) +FF 64 B (32bitx, 16word), and the bit width of the command buffer is 32bit.
- ○ Register in PMU (including command buffer) answers to only word access completely.
  - ・The command which is at the time of master movement reads the command from a command buffer in PMU, and carries out.
  - ・Read/ Write to a register is performed variously as APB master. The macro by which control is possible is below.
    ATIM, AINT, PM0, GIO, MWI, MEMC, PDMA, DCV, AXL0, PMU, ASMU, SP0, SP1, CHG
  - ・All kinds' Power ON/OFF sequence to power supply IC is carried out from SP0. The direct control of power supply IC is also possible from a register of ASMU. The control of a power supply is possible by the range of L1 power supply.
  - ・Power supply SW is controlled. Power supply SW where control is possible is the following territory.
    ACPU territory and L1 territory.
    Power supply SW control in ADSP territory by ACPU and don't do by PMU.
- ○ Interrupt signal to ACPU (INT_FIQ0Z, INT_IRQ0Z) is watched and state transition processing is performed by these signal detection.
- ○ Incorporates a watchdog timer (WDT) (32.768 kHz, 18 bits), and outputs a system reset request signal to the external power supply LSI upon occurrence of a timeout.

3.1.3 Interrupt controller (AINT)

AINT has a function that controls output of interrupts for multiple processors and a function for interprocessor communication.

○ Interrupt output signals

AINT outputs interrupt signals for processors.

- IRQ/FIQ interrupt output for ACPU (PMU_IQU0Z, PMU_FIQ0Z)
  The PMU hooks the interrupts when the power of the ACPU is off.
- Interrupt output for ADSP (ADSP_INTP)

○ Interrupt sources

AINT can handle 72 interrupt sources.

- Interprocessor communication interrupts (INT0 to INT4)
- External peripheral interrupt input (INT5 to INT95)
  INT88 to INT95 can be input independently for each processor.

○ Interprocessor communication function

AINT has individual buffers for communication paths and can transmit 6-bit messages to the destination processor.

AINT supports the following combinations of interprocessor communication.

- ACPU → ADSP
- ADSP → ACPU

3.1.4 Timer (ATIM)

ATIM is a group of general-purpose timers that can be used as an interval timer or watchdog timer.

○ 32-bit counter length

○ Timer clock

- Clock generated by dividing PLL3
- 32.768 kHz

Remark The timer clock can be set by using an ASMU register.

○ ATIM includes 14 timers (TI0 to TI3, TW0 to TW3, and TG0 to TG5), all of which has the same function.

3.2 Processor Functions

3.2.1 ACPU TOP module (ACPU)

The ACPU is the main processor. ARM1176JZF-S is incorporated as the processor core.

○ ARM architecture
ARM v6
○ L1 cache
- Instruction cache: 32 KB, data cache: 32 KB
VIPT cache (PIPT when the cache size is 16 KB)

○ Floating point operation
VFP11 supported
○ Main bus
- AMBA3 64-bit AXI bus × 1

○ Interrupts
nIRQ, nFIQ, nPMU
○ Leakage current control
Controlled by power switch (Quick Recovery)
○ Debug function
- JTAG

3.2.2 Digital signal processor (ADSP) (DSPK701)

The ADSP is a DSP core that processes voice and image codecs such as MPEG4/H264, and various applications that require a high processing capability with low power consumption.

○ Functions
- Improved pipeline of SPXK6. Operation speed increased by using a 4-stage pipeline for cache access
- 11-stage pipeline (12 stages for only multiply-accumulate operations)
- Instruction-compatible with SPKX5/SPXK6 at source level
- Executes up to four instructions at the same time
- Two multiply-accumulate operation units, ALUs, and load/store units each
- Special instructions for signal processing applications
- Byte data load/store instructions
- JTAG function

○ Programming
- Multiply-accumulate operation unit of 16 bits × 16 bits + 40 bits → 40 bits
- Eight 40-bit general-purpose registers (also usable as sixteen 16-bit registers)
- Eight 32-bit data pointer registers
- Interrupt expansion by interrupt controller
- Non-maskable interrupt (NMI)
- Mixed 16-bit and 32-bit instruction set
- Can issue up to four instructions at the same time by using a 64-bit fetch packet.
- Execution stage operating with 2 clocks for multiply-accumulate operations only and with 1 clock for other operations
- Parallel loading/storing of 8-, 16-, or 32-bit data

○ Memory space
- 4 GB (32-bit byte address) single memory space

3.2.3 ADSP address converter (DCV)

DCV is an address converter that translates the ADSP address map. DCV is used to map physical addresses to the ADSP's cacheable area, bufferable area, and unbufferable area.

○ Address translation function

Addresses can be translated for each bank (256 MB) in 64 KB units.

Do not change the parameters dynamically because this may affect debugging of the ADSP.

3.3 Memory Interface Functions

3.3.1 Asynchronous bus interface (AB0)

AB0 is an external asynchronous interface that can connect asynchronous devices such as NOR-Flash and SRAM.

- ○ 16-bit bus
- ○ Number of connectable slave devices: 4 (CS × 4)
- ○ Address ranges can be set for individual slaves
  The specifiable address ranges are 0000_0000H to 0FFF_FFFFH, 1000_0000H to 1FFF_FFFFH, and 2000_0000H to 2FFF_FFFFH, up to 256 MB. Addresses that extend over these ranges cannot be set.
  Addresses 2FFF_0000H to 2FFF_FFFFH are assigned to the AB0 local registers, so cannot be used by the user.
- ○ AB0 supports Intel Strata Flash Memory / Intel Strata Flash with A/D Muxed I/O.
- ○ Operations is possible with the ratio of the AB0 clock and flash memory clock of 1:1 or 2:1.
- ○ The supported patterns to access the external modules are as follows.
  - Single read/write
  - Page read
- ○ The local registers in AB0 support can be accessed only in word (32-bit) units, and cannot be accessed in byte, halfword, and double-word units.

3.3.2 Internal SRAM (SRC)

SRC is an internal 128 KB general-purpose SRAM.

- ○ SRC protects the security areas from access. If a master attempts to access an access-prohibited area, SRC executes interrupt servicing and retains the accessed address and the ID of the master that attempted the access. Register accessing for holding this information is also performed from an AHB address space.

3.4 Bus Functions

3.4.1 AXI buses (AXL0, AXL1)

○ Has 3-layer AXI (DRAM, internal SRAM, AB0) and 1-layer AHB (PB0, PB1, AB1, AHB slave) functions.
○ Operates with 166 MHz max.
○ Has an on-chip 32 KB boot ROM (used for purposes such as NAND boot).
○ Since these buses are connected to two power domains, they are separated into two modules AXL0 and AXL1.
○ Has a 32-bit address bus and a 64-bit data bus.
○ Has a memory-to-memory transfer DMA function.

3.4.2 DMA controller (DMAC)

○ Three physical channels (PCH0, PCH2, PCH3) and 26 logical channels (LCH) are incorporated. (PCH1 is a reserved channel).
  - PCH0 (LCH0 to LCH3): Memory-to-memory transfer
  - PCH2 (LCH0 to LCH14): Memory-to-peripheral transfer. (LCH6 to LCH8 and LCH11 are reserved.)
  - PCH3 (LCH0 to LCH14): Peripheral-to-memory transfer. (LCH6 to LCH8 and LCH11 are reserved.)

○ Each physical channel (PCH) has one AHB bus master for reading and another AHB bus master for writing.
○ Connected as an AHB master, to a total of six locations of internal bus slave interface (three locations for reading and another three locations for writing).
○ The six AHB bus masters can operate concurrently.
○ The DMAC internal registers are accessed via an APB. The APB can be accessed only in word units.
○ PCH0 and PCH2 feature ring buffers in SRAM. PCH3 has a 16-entry FIFO (configured with FF).
The size of the internal buffer of each physical channel is as follows.
  - PCH0: 256 words (256 bytes per LCH)
  - PCH2: 416 words (128 bytes per LCH)
  - PCH3: 16 words (4 bytes × 16 entries)

○ Transfer operation
The DMAC reads data from a source address (transfer source address), stores the data in the DMAC internal buffer, and writes that data to a destination address (transfer destination address).
○ An interrupt signal is generated for each processor when transfer ends.
(Four types of interrupt sources are available: length, block, error, and timeout.)
○ Each AHB master has an arbitration circuit, which arbitrates among requests from the logical channels, using a round-robin algorithm.
○ Both memory-to-memory AHB transfer and memory-to-peripheral AHB transfer support 8-, 16- and 32-bit bus width.
○ Endian conversion function
  - The read control block and write control block each have an endian conversion function.
  - Byte lane of data loaded to a data buffer (FIFO) can be selected for each byte on the read side.
  - Byte lane of data to be output to the AHB write bus can be selected for each byte on the write side.

○ PCH0 supports reverse transfer in block units (implemented by setting the offset to the lower address direction).

3.5 I/O Control Functions

3.5.1 CHG, CHGL1, CHGREG, and IO

These units control the external pins, switch the alternate pin functions, and monitor the internal signals.

○ External pin control

Can control the following functions for some external pins by using the CHGREG register.

- Switching of pull-up and pull-down for pins
- Masking input to pins
- Switching of pin drive capability (drive strength)

○ Alternate pin function control

Can switch the alternate pin functions.

○ Boot mode decoder

Decodes the status of several external pins (UTEST, BOOTSEL, etc.) and generates a boot mode signal.

The boot mode signal is connected to the ACPU, and the ACPU selects the boot address from an external flash (AB0) or internal SRAM (SRC).

○ L1_HOLD function

Holds the state of external pins controlled from the L1 domain when the power of L1 power domain is off.

3.6 Image Processing Functions

3.6.1 LCD controller (LCD)

The LCD controller has a function to output image data on the memory to an external parallel LCD panel.

○ Supported LCD panel specifications
- ～WVGA (800×480)
- TFT colors: 16 bpp and 18 bpp

○ Input image data formats
- RGB565, RGB666
- YUV422, YUV420 (when operating together with the IMC)

○ Output format
- RGB565, RGB666

3.6.2 Image composer (IMC)

The IMC has a function to convert image data on the memory and output it to the LCD controller.

○ Supported image size
- Horizontal direction: Up to 2,046 pixels
- Vertical direction: Up to 2,046 lines

○ Data format
- Input: RGB565, RGB666, YUV422, YUV420
- Output: RGB565, RGB666

○ YUV-to-RGB conversion,Dithering, Gain offset
- Gain and offset can be adjusted for YUV components, from 0 to x2
- When the input data format is YUV, RGB conversion can be performed with two types of coefficients
- Dithering by using 2 × 2 matrix upon subtracting colors for converting images into RGB666

○ Overlay function
- Up to four layers can be synthesized.
- Position and size of synthesized planes can be set flexibly.
- Each layer can be defined independently in two dimensions, and formatting, mirror flipping, resizing, double buffering, and gain/offset adjustment can be set separately. (Whether this function is supported varies in each layer.)
- Transparent color and alpha blending can be used for the two front layers.

○ Gamma adjustment by table referencing

○ Image data after conversion can be written back to memory (WB function), as well as supplying to the LCD controller.

○ Support of ARGB4444 format
- The ARGB4444 format can be set for four layers: layers 0, 1A, 1B, and 1C.

3.6.3 Terrestrial digital TV interface (DTV)

DTV has a function to transfer stream data sent from an externally connected DTV decoder IC to memory. DTV supports the burst serial output transfer.

- ○ Supports OFDM encode LSI μPD61531.
- ○ Supports serial transfer mode.
- ○ Supports DMA transfer of input stream to memory.

3.6.4 Camera interface (CAM)

CAM captures YUV422 image data from an external camera module, reduces the image to any size (down to 1/16), and transfers it to an external memory.

- ○ Camera interface signal
  - Data bus (CAM_YUV[7:0])
  - Vertical synchronization (CAM_VS)
  - Horizontal synchronization (CAM_HS)
  - Pixel clock (CAM_CLKI)
- ○ Synchronization signal encoding
  - Vertical/horizontal synchronization signal sampling
  - Enable signal sampling
  - ITU-R BT.656 encoding
- ○ ITU-R BT.656 input

  The following three modes are available.
  - Store the first field to buffer A, and the second field to buffer B.
  - Store only the first field to buffer A.
  - Store only the second field to buffer A.
- ○ Data format
  - Input: YUV422
  - Output: Selected from YUV422 or YUV420 format

    (YUV Semi-Planar, YUV Interleave and YUV Planar modes are selectable in YUV422 mode.
    YUV Semi-Planar and YUV Planar modes are selectable in YUV420 mode.)
- ○ Maximum image size
  - 4,088 pixels (horizontal) × 4,092 pixels (vertical)
- ○ Data sampling

  Data can be sampled at the following timing for the pixel clock:
  - Rising edge
  - Falling edge
  - Both edges
- ○ Level adjustment

  The gain and offset of the captured external camera images can be adjusted. Values can be specified separately for Y, U and V.
- ○ Reduction
  - Nearest-neighbor sampling
  - Reduction range of 1 to 1/16 (can be set to any size)

○ Frame-skipped transfer
- No skipping: Every frame is transferred.
- 1/2 skipping: One out of two frames is transferred.
- 1/3 skipping: One out of three frames is transferred.
- 1/4 skipping: One out of four frames is transferred.

○ Horizontal and vertical flipping

Data can be individually flipped horizontally and/or vertically and transferred to memory.

○ Double buffer transfer

The transfer destination frame is switched automatically for each transfer frame.

○ Buffer memory

Two 32-bit × 256-word buffer memories

○ Compliant with AMBA™ system bus architecture (Rev. 2.0)

○ Simple QoS
- Controls the priority of the AXI (AHB) bus modules based on the vacant space in the data buffer.
- The threshold of the vacant space in the data buffer can be specified by using a register.
- CAM outputs a priority signal to the control side.

○ Outputting of amount of valid data in FIFO (data buffer)
- The amount of valid data in the data buffer is output.

○ Safe reset
- A reset is asserted only when the AHB bus is in the idle state.

3.7 Image Processing Modules

3.7.1 Image processing unit (IPU)

The IPU has an image processor function that supports acceleration of various image processing, an image rotator function that rotates YUV images, and a Graphics DMA function.

Processing by the image processor, image rotator and Graphics DMA can be linked to the queue at the same time. In addition, the image processor and image rotator execute one-pass processing.

○ Image processor function
- Image enlargement/reduction function (resizer)
- Image space conversion function (converter)
- Color dithering function (dithering)
- Pixel packing function
- Two-image overlay function
- Vertical/horizontal flip function
- Endian switch function
- Byte lane switch function
- One-pass processing by image processor and image rotator

○ Image rotator function
- Image rotate processing function (rotator)
- Endian switch function
- Byte lane switch function

○ Graphics DMA function and other functions
- Functions that accelerates image synthesis
- Memory-to-memory copy function and rectangle fill function
- Raster operation
- Color key (mask) function
- Byte lane switch function
- Register update reserve function

3.7.2 H.264 HW encoder/decoder (AVC)

AVC is an encoder/decoder for H.264 images, which converts data on the memory and writes back the result to the memory.

○ Supports H.264/MPEG-4 AVC Baseline Profile Level3 or lower.
○ Encoding and decoding of images with a size of 128 × 96 (Sub QCIF) to 720 × 480 (D1).
○ Supports CBR (Max. 10 Mbps) and VBR.
○ Supports Byte Stream Format (Annex B).
○ Supports YUV420 Planar and Semi-Planar formats.

3.8 External Interface Functions

3.8.1 Serial peripheral interface (SP0, SP1, SP2)

EM1-D512 incorporates three channels of the SPI interface that is one of the 4-wire serial interfaces.

○ Transfer modes
- Master and slave modes
- CPU control mode and DMA control mode
  - CPU control mode: Mode in which transfer ends when transmission, reception, or transmission/reception of 1 frame ends.
  - DMA control mode: Mode in which transfer is executed continuously by using an individual 32-word FIFO for transmission and reception. This mode is classified into two modes: normal mode, in which transfer is executed until it is stopped by the CPU, and fixed-length mode, in which transfer automatically stops according to the FIFO status.

○ SCLK polarity (normal/inverted) and delay (half of SCLK) can be set for individual CS.
○ Transfer bit length setting (8 to 32 bits)
○ Clock request signal (SPx_PCLKREQ, SPx_SCLKREQ) generation
○ Automatic transfer stop function (fixed-length DMA mode)
- Stops SPI transmission when the transmit buffer becomes empty during DMA master transmission.
- Stops SPI reception when the data amount stored in the receive buffer reaches the threshold specified with a register, during DMA master reception.

○ CS-fixed control via register setting
○ SI/SO I/O phase switching

3.8.2 USB interface

This is a USB controller conforming to USB 2.0. PHY devices are connected externally.

○ PHY interface
Supports the UTMI + Low Pin Interface (ULPI).
○ 16 USB pipes supported with ETD data structure management.
○ Actual transfer level such as transaction scheduling and handling is supported by hardware.
○ USB function controller
Has 16 endpoints.
○ Uses a dual-port RAM buffer to exclude system bus latency from the USB timing requirements.

3.8.3 I^2C interface (IIC)

EM1-D512 incorporates two channels for IIC bus format interfaces.

○ It's based upon I2C bus and the format (Philips company 1995 Update edition).
Data length: 8 bits (but, after ,8 bit data, by a ACK signal, 1 bit).
It corresponds to a standard mode (transfer rate: At most 70 Kbps)/a fast mode (transfer rate: At most 341 Kbps).

○ The automatic distinction function of the serial data.
The start condition on the serial data bus, the slave address, data and the stop condition are detected automatically.

○ Chip selection by the address.
It's possible to choose the specific slave device connected to I2C bus and communicate by sending the slave address or extension code at the time of master movement.

○ The wake-up function.
Only when the received address received the case parallel with the price of SVA0 register and extension code at the time of slave movement, interrupt is generated. Therefore a device besides the chosen slave on the I2C bus can move irrespective of a serial communication.

○ Acknowledging (ACK) control function.
It's possible to control the acknowledging signal to confirm that a serial communication was normally carried out at the time of master/slave movement.

○ Weight (WAIT) control function.
The weight ringing control to tell the weight state can be performed.

○ Arbitration control function.

3.8.4 General-purpose I/O (GIO)

EM1-D512 incorporates 118 general-purpose I/O ports.

○ I/O can be switched in port units.

○ Interrupt settings can be set in port units

○ The following types interrupt detection can be set.

- Detection of 32.768 kHz clock synchronization/asynchronization
- Detection of positive or negative logic level
- Detection of rising edge, falling edge, or both edges

3.8.5 SDIO interface (SDI)

○ Supports SDIO interface.

○ Supports 1-bit/4-bit data

○ Supports SD Binding function.

○ Supports HSMMC function.

3.8.6 UART interface (U70, U71, U72)

EM1-D512 incorporates three channels for UART serial interface.

- ○ Three channels of UART compatible with TL16C750 made by TI Inc.
- ○ Maximum baud rate: 3,680,000 bps
- ○ It has FIFO built-in 64 bytes in sending/each receiving. It's possible to choose the next operation mode by setting.
  - ・Non-FIFO mode (16450 modes)
  - ・16 byte FIFO mode (16550 modes)
  - ・ 64 byte FIFO mode
- ○ Programmable auto-RTS,auto-CTS is being supported.
- ○ The start which is the average asynchronous communications control bit, a stop and addition of the parity bit/elimination are possible to a send and receive serial data. The next programmable control is possible.
  - ・Character length control: 5, 6, 7 or 8 bits.
  - ・Parity bit control: Without even numbered parity, odd parity or a parity bit.
  - ・Stop bit length control: 1 or 2 bits.
  - ・Baud rate control: Reference clock division setting of 1-216- (1) is possible..
- ○ Modem control interface is being supported (CTS,RTS,DSR,DTR,RI,DCD).
- ○ Loop-back function is being supported.
- ○ It has an encoder for IrDA SIR (2.4 kbps-115.2 kbps)/a decoder built-in.

3.9 Sound Functions

3.9.1 PCM interface (PM0, PM1)

EM1-D512 incorporates two channels for the audio system codec.

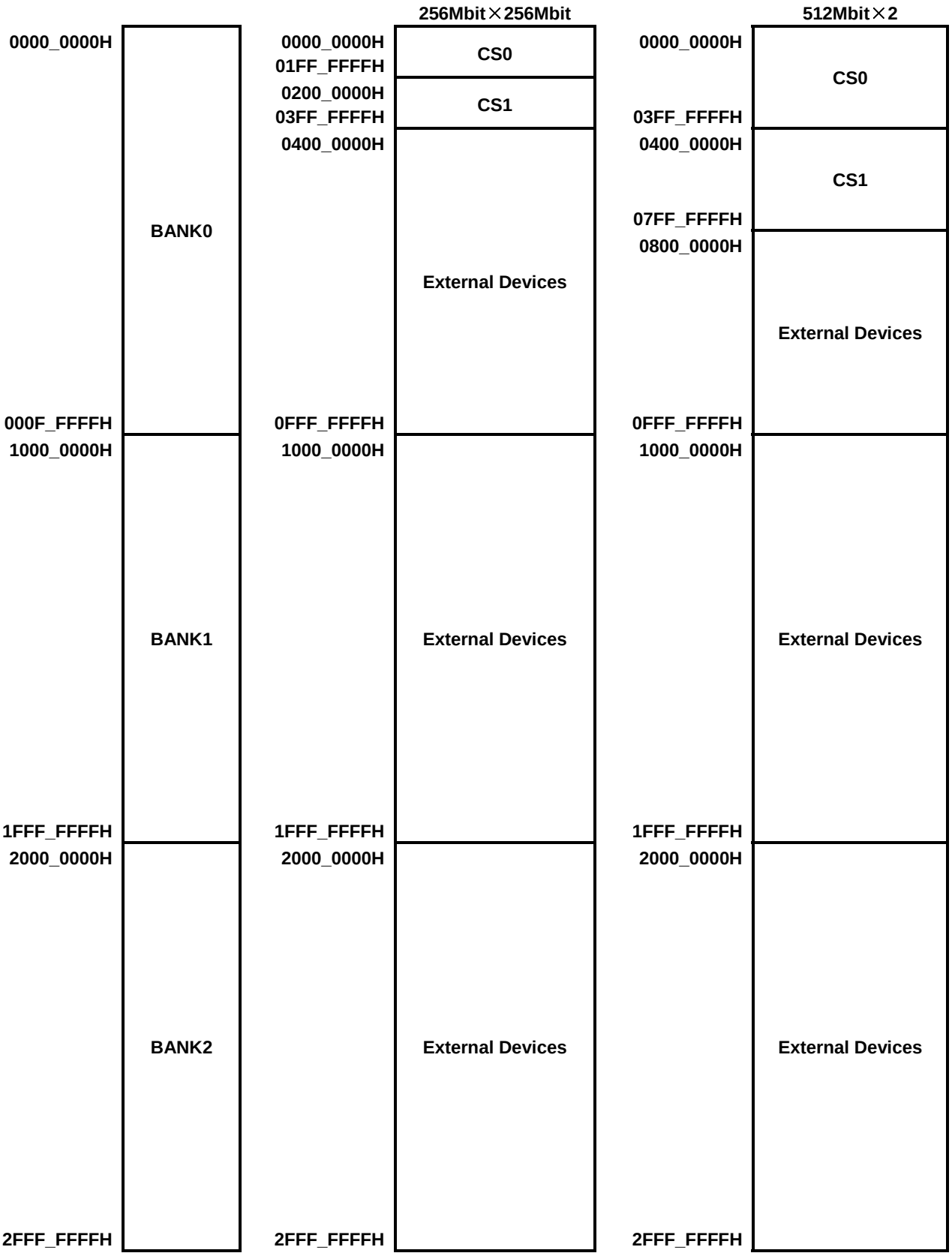
- ○ Seven types of operating modes
- ○ Can use DMA transfer.
- ○ Incorporates 32-bit × 32-word FIFO for transmission and reception.
- ○ Supports transfer via dedicated DMA (PM0).

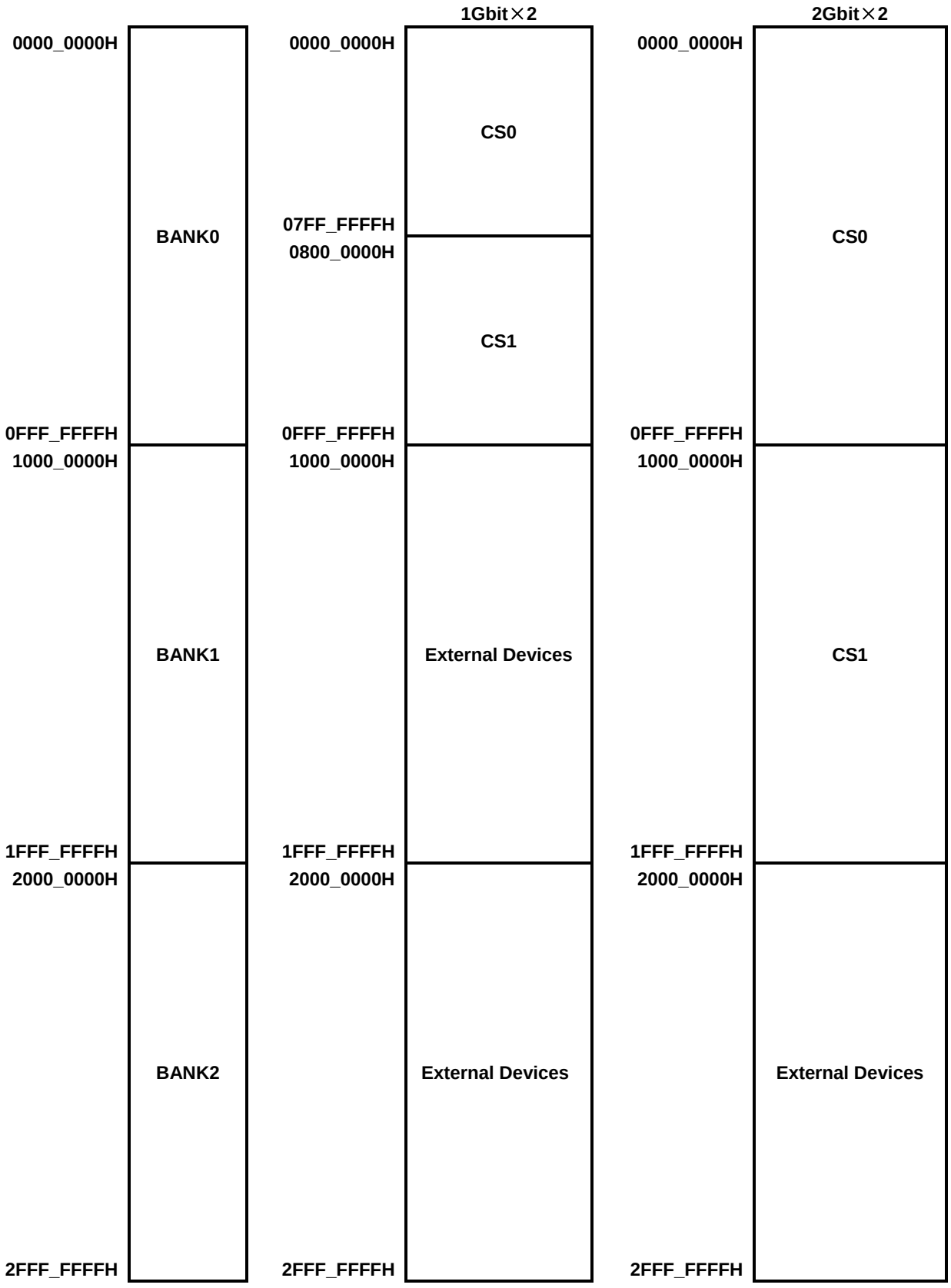
4.1 Memory Map

	BANK	Description	Target Module
0000_0000H 0FFF_FFFFH	BANK0	NOR FLASH	AB0
1000_0000H 1FFF_FFFFH	BANK1	NOR FLASH External Device	
2000_0000H 2FFF_FFFFH	BANK2	External Device	
3000_0000H 3FFF_FFFFH	BANK3	DRAM	MEMC
4000_0000H 4FFF_FFFFH	BANK4	APB Bus #0	PB0
5000_0000H 5FFF_FFFFH	BANK5	Async Bus #1	AB1
6000_0000H 6FFF_FFFFH	BANK6	AHB Slave	SWL1
7000_0000H 7FFF_FFFFH	BANK7	Reserved	
8000_0000H 8FFF_FFFFH	BANK8	Reserved	
9000_0000H 9FFF_FFFFH	BANK9	Reserved	
A000_0000H AFFF_FFFFH	BANK10	Internal SRAM	SRC
B000_0000H BFFF_FFFFH	BANK11	Reserved	
C000_0000H CFFF_FFFFH	BANK12	APB1	PB1 (PMU)
D000_0000H DFFF_FFFFH	BANK13	Reserved	
E000_0000H EFFF_FFFFH	BANK14	Reserved	
F000_0000H FFFF_FFFFH	BANK15	Boot ROM	AXL1

4.1.1 BANK0 to BANK2

BANK0/1/2：AB0 (NOR FLASH/ External Device)
0000_0000H－2FFF_FFFFH

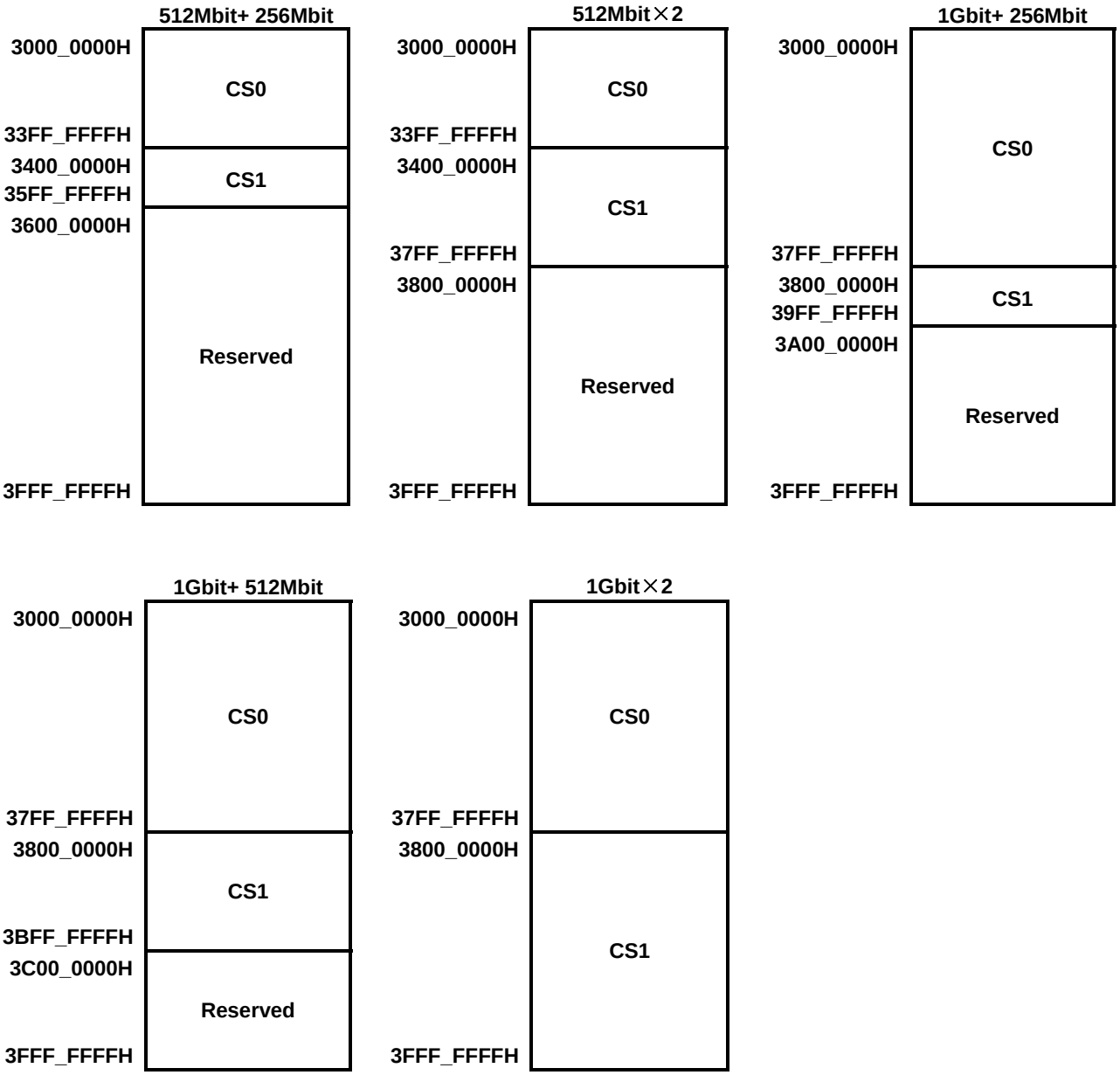



1Gbit×2
2Gbit×2
0000_0000H
0000_0000H
0000_0000H
BANK0
CS0
07FF_FFFFH
0800_0000H
CS0
CS1
0FFF_FFFFH
0FFF_FFFFH
0FFF_FFFFH
1000_0000H
1000_0000H
1000_0000H
BANK1
External Devices
CS1
1FFF_FFFFH
1FFF_FFFFH
1FFF_FFFFH
2000_0000H
2000_0000H
2000_0000H
BANK2
External Devices
External Devices
2FFF_FFFFH
2FFF_FFFFH
2FFF_FFFFH

4.1.2 BANK3

BANK3 : MEMC (DRAM)

3000_0000H－3FFF_FFFFH

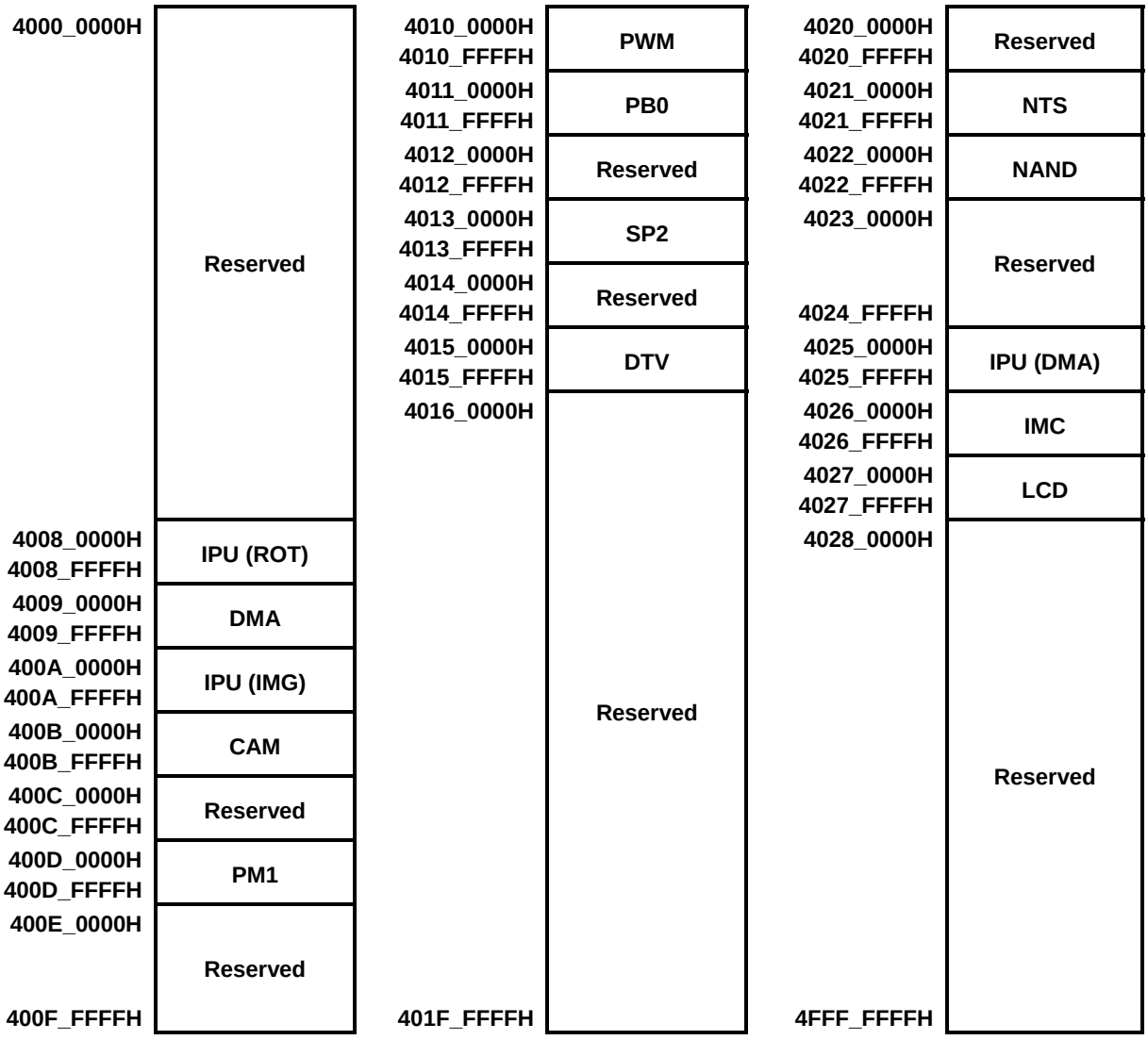


4.1.3 BANK4

BANK4：PB0 (APB-Bus #0)

4000_0000H－4FFF_FFFFH

* A 64KB space is allocated to each module.

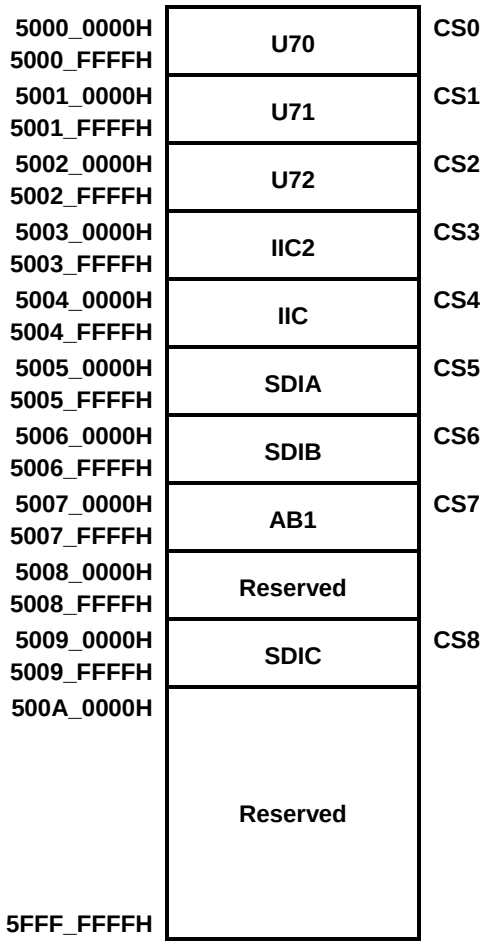


4.1.4 BANK5

BANK5：AB1 (Async-Bus #1)

5000_0000H－5FFF_FFFFH

* A 64KB space is allocated to each module.

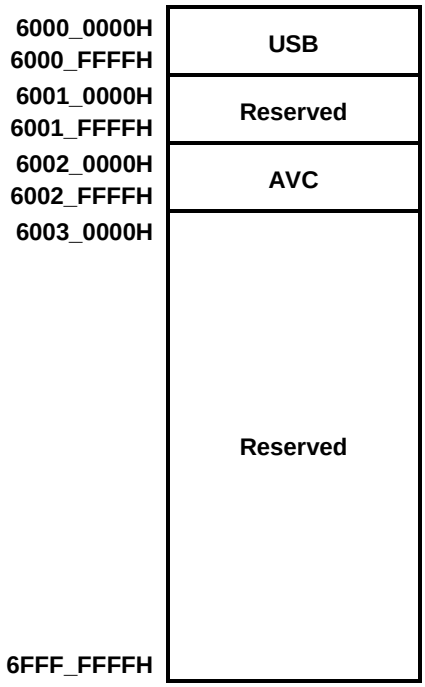


4.1.5 BANK6

BANK6：AHB Slave

6000_0000H－6FFF_FFFFH

* A 64KB space is allocated to each module.

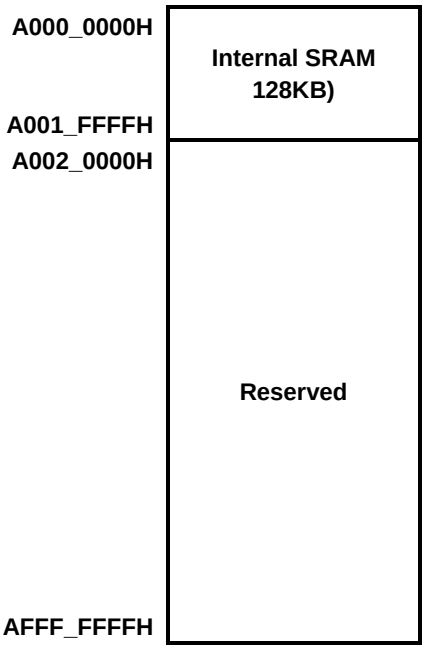


4.1.6 BANK10

BANK10：SRC (Internal SRAM)

A000_0000H－AFFF_FFFFH

* A 64KB space is allocated to each module.

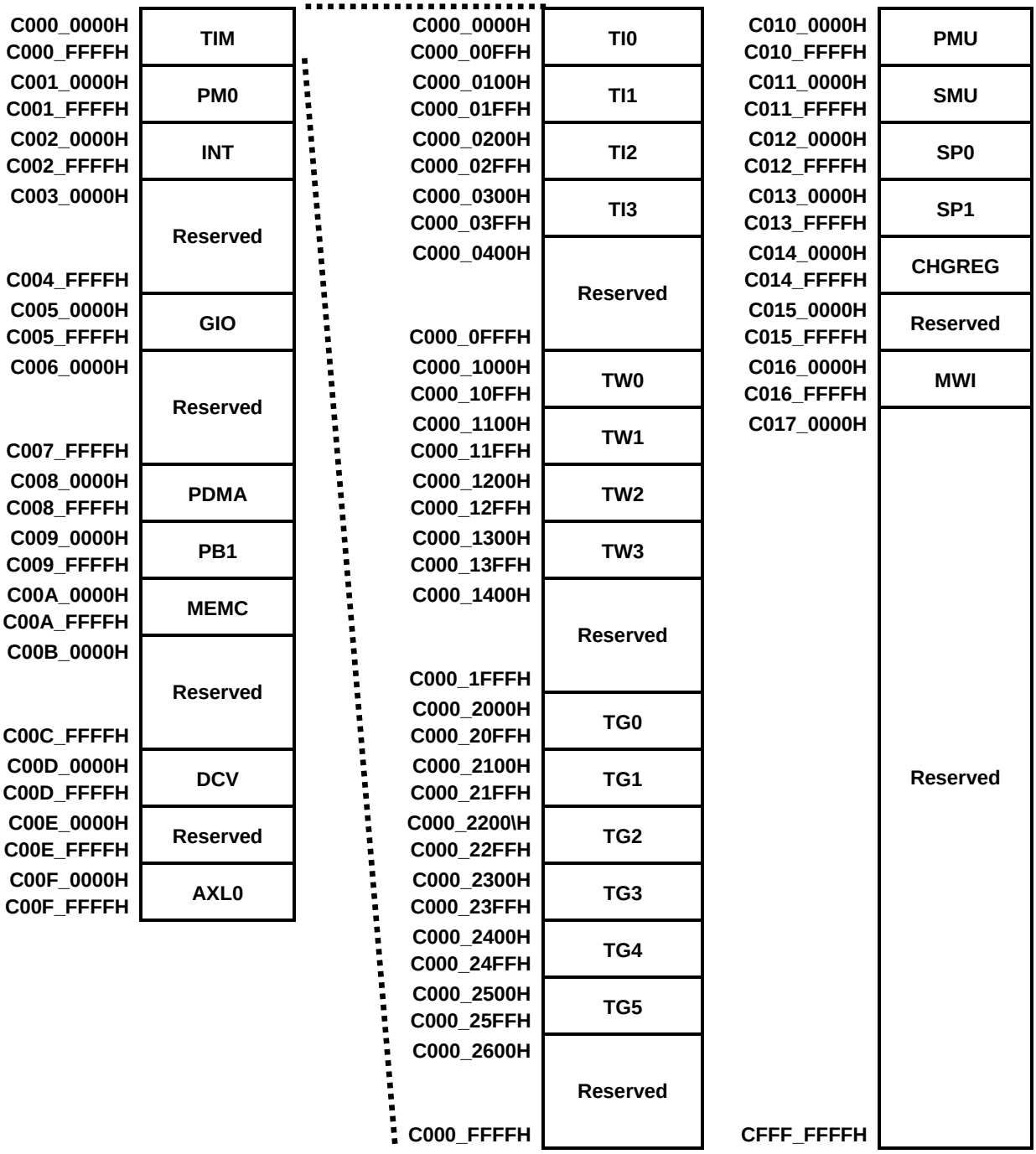


4.1.7 BANK12

BANK12 : PB1 (APB-Bus #1)

C000_0000H－CFFF_FFFFH

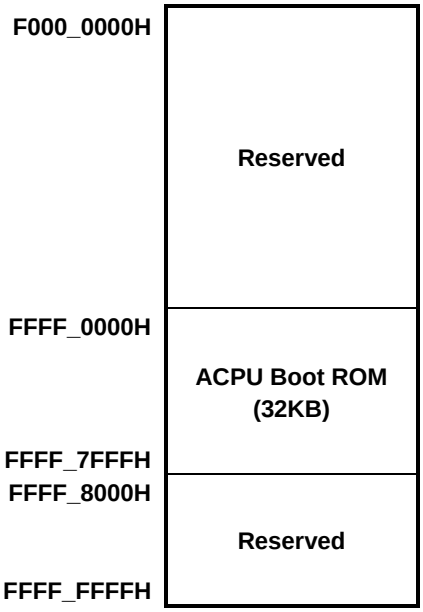
* A 64KB space is allocated to each module.



4.1.8 BANK15

BANK15：BootROM

F000_0000H－FFFF_FFFFH



4.2 Clock

- ○ The system clock is selectable from 32.768 kHz input, PLL3 (229.376 MHz max.), and PLL1 (500 MHz max.).
- ○ The clock to be supplied to peripheral functions is generated from PLL3.
- ○ Turning on or off the clock supply to each macro can be controlled via registers.
- ○ Turning on or off the clock supply to the ACPU can be controlled independently.
- ○ An automatic clock switch function is provided which stops clock supply to a module that no longer sends a clock request signal.
- ○ When a clock request from each master module has disappeared, I have the frequency automatic switch system to make the clock which divided output of PLL1 by the frequency dividing rate established in SMU beforehand a system clock (If a clock request from master occurs, it'll be changed to 500 MHz immediately.)

4.2.1 PLL used

(1) PLL1

PLL for main clock
Clock frequency: 320 MHz to 500 MHz
PLL1 is used as the main clock during normal operation.
The multiplication ratio of PLL1 is variable. (Before changing the multiplication ratio, change the clock source to PLL3.)

(2) PLL2

PLL for audio DAC
Clock frequency: 320 MHz to 500 MHz
PLL2 is used as the clock for the audio DAC.

(3) PLL3

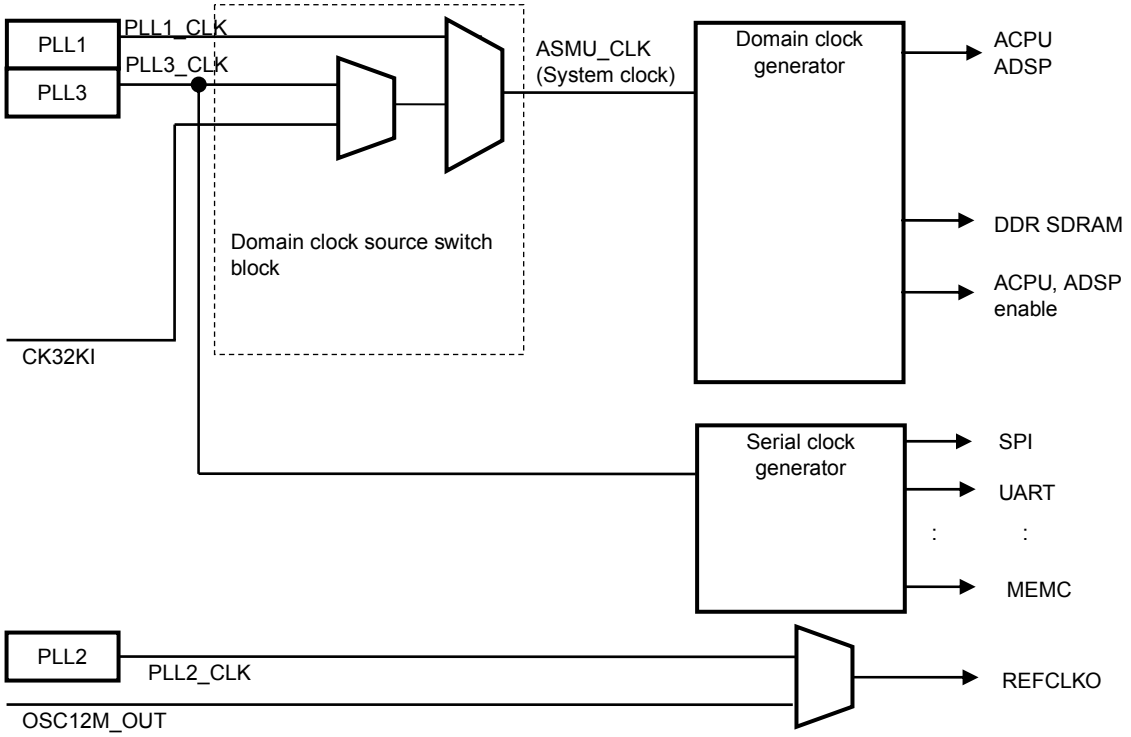
PLL for peripheral
Clock frequency: 229.376 MHz (fixed)
PLL3 constantly operates to be used as the system clock. It is also used for each peripheral.
(Standby only when operating at 32 kHz in Sleep mode).

The names PLL1, PLL2, and PLL3 are used for explanation in this chapter.

4.2.2 Outline of clock system

The following is a schematic diagram of the clock system.

Figure 4-1. Schematic Diagram of Clock System



Refer to appendix B for details.

4.2.3 Automatic frequency control

When the master for which automatic frequency control is enabled becomes inactive, the overall clock frequency is decreased to the frequency ratio of each domain clock remaining unchanged.

Unlike switching of the clock source and division ratio, the frequency is changed by changing the division factor without stopping the clock.

4.2.4 Automatic clock control

This function is used to supply a clock automatically when each function macro requires a clock. When a clock request signal (CLKREQ) is received from each macro, the ASMU supplies the relevant clock to the requested macro.

The automatic control function ON/OFF register and forced clock supply stop register are used to implement this function.

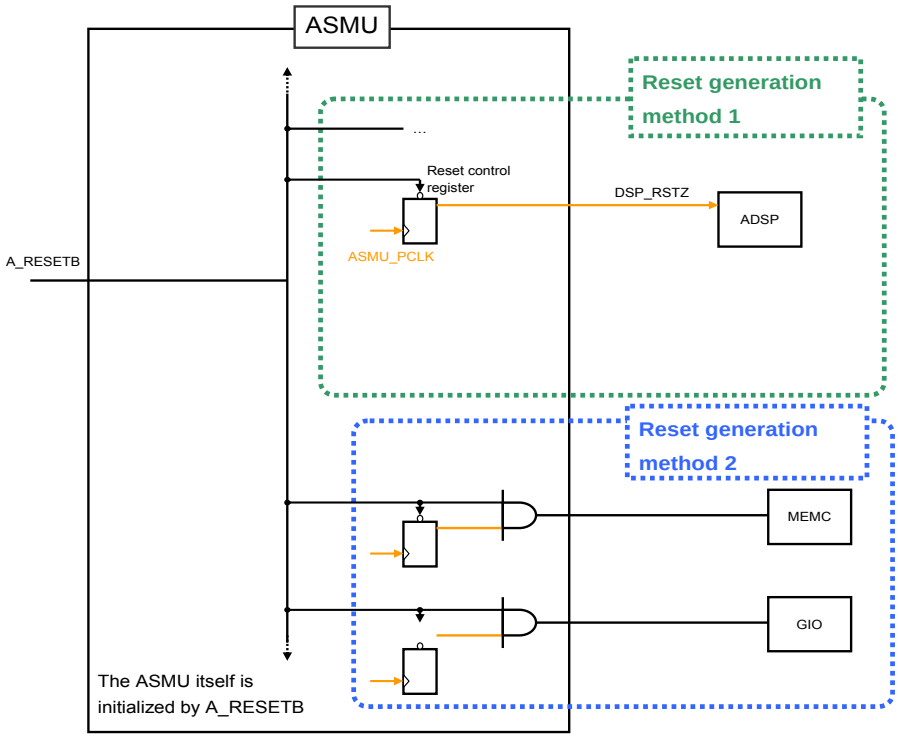
4.3 Reset

- ○ Macros other than the ASMU use synchronous reset. Be sure to turn on clock supply to a macro before it is reset by software.
- ○ The output reset signal is synchronized in the relevant macro.

The ASMU supplies the reset signal for each EM1-D512 macro. The reset structure of EM1-D512 is shown in the following figure.

The reset signal for macros is generated via hard reset input and the register values in the ASMU. The two types of methods are available.

Figure 4-2. Reset Structure Diagram



4.3.1 Reset generation method 1

The reset for each macro is controlled via the reset control registers. These registers can be read or written from the ACPU via APB. This method uses a synchronous reset.

The reset control registers are initialized by a system reset (A_RESETB), but these registers hold the reset state until the ACPU issues a reset cancel command, because their initial values are low level. Macros that do not need to start at boot are reset by this method.

4.3.2 Reset generation method 2

Like reset generation method 1, the reset for each macro is controlled via the reset control registers and these registers can be read or written from the ACPU via APB. This method uses a synchronous reset.

The reset control registers are initialized by a system reset (A_RESETB), but this reset state is cancelled at the same time as a hardware reset is applied. Macros that must start at boot (CHG, AXL0, MEMC, SWL0, SRC, PB1, PMU, AINT, TW0, TW3, GIO, AXL1, ACPU, AB0, SWL1, and PB3) are reset by this method.

4.4 Status Transition

4.4.1 Power domain

EM1-D512 is separated into several power supply domains. The features of each domain are as follows.

○ L0 domain

The current flows in this domain even if EM1-D512 enters Low Power mode. This domain includes macros that should retain the register settings after returning from Low Power mode.

○ L1 domain

Power to this domain is turned off in Low Power mode.

○ L2 domain

Power to this domain is turned off in Low Power mode. This domain only includes the USB, which can be controlled independently from L0.

○ L3 domain

Power to this domain is turned off in Low Power mode. This domain only includes AVC (H.264 accelerator), which can be controlled independently from L1.

○ ACPU domain

Power to this domain is turned off in Low Power mode. This domain only includes the ACPU, which can be controlled independently from L1.

○ ADSP domain

Power to this domain is turned off in Low Power mode. This domain only includes the ADSP, which can be controlled independently from L1.

4.5 Control of DMA Controller

DMA transfers are classified into the types shown in the following table. A separate physical channel is provided for each transfer type.

Physical channel 1 (PCH1) does not exist.

Table 4-1. Transfer Types and Number of Channels

Transfer Type	Memory-to-Memory	Memory-to-Peripheral	Peripheral-to-Memory
Physical channel name	PCH0	PCH2	PCH3
Number of logical channels	4	11	11
Two-dimensional transfer function	○	△ Note 1	△ Note 1
Timer function	×	△ Note 2	△ Note 2
Reverse transfer function	○	×	×

Notes 1. The two-dimensional transfer function is supported only on the memory side.

2. The timer function is supported only for UART channels (LCH0, LCH1, and LCH2).

Remark ○: Supported, △: Supported with certain conditions, ×: Not supported

4.5.1 Memory-to-memory transfer

Memory-to-memory transfer sends data from a source address to a destination address, according to the ACPU register settings. The areas AB0, MEMC and SRC are subject to memory-to-memory transfer, in any combinations, except for transfer that involves overwriting (such as right-scrolling of an image). The minimum unit of transfer is one byte.

Table 4-2. Memory-to-Memory Transfer Combinations

Memory-to-Memory Transfer	AB0 Area	SRC	MEMC Area
AB0 area	○	○	○
SRC area	○	○	○
MEMC area	○	○	○

Remark ○: Combination available

4.5.2 Memory-to-peripheral transfer

Memory-to-peripheral transfer sends data from a source address to a destination address, in response to request signals sent from each macro, in addition to transfer according to the ACPU register settings.

The following table lists blocks subject to memory-to-peripheral transfer.

Table 4-3. Memory-to-Peripheral Transfer Combinations

LCH No.	Memory-to-Peripheral Transfer	AB0 Area	MEMC Area
0	UART0	○	○
1	UART1	○	○
2	UART2	○	○
3	SDIA	○	○
4	SDIB	○	○
5	SDIC	○	○
6	Reserved (unused)	–	–
7	Reserved (unused)	–	–
8	Reserved (unused)	–	–
9	PCM0 (audio serial)	○	○
10	PCM1 (audio serial)	○	○
11	Reserved (unused)	–	–
12	SPI0	○	○
13	SPI1	○	○
14	SPI2 (GD)	○	○

Physical channel 2 (PCH2) is a channel dedicated to memory-to-peripheral transfer. PCH2 has 13 logical channels (LCH0 to LCH14). These logical channels are arbitrated on a burst transfer size basis in a round-robin fashion. LCH6 to LCH8 and LCH11 are the reserved channels and therefore cannot be used.

4.5.3 Peripheral-to-memory transfer

Peripheral-to-memory transfer sends data from a source address to a destination address, in response to request signals sent from each macro, in addition to transfer according to the ACPU register settings. The following table lists blocks subject to peripheral-to-memory transfer.

Table 4-4. Peripheral-to-Memory Transfer Combinations

LCH No.	Peripheral-to-Memory Transfer	AB0 Area	MEMC Area
0	UART0	○	○
1	UART1	○	○
2	UART2	○	○
3	SDIA	○	○
4	SDIB	○	○
5	SDIC	○	○
6	Reserved (unused)	–	–
7	Reserved (unused)	–	–
8	Reserved (unused)	–	–
9	PCM0 (audio serial)	○	○
10	PCM1 (audio serial)	○	○
11	Reserved (unused)	–	–
12	SPI0	○	○
13	SPI1	○	○
14	SPI2 (GD)	○	○

Physical channel 3 (PCH3) is a channel dedicated to peripheral-to-memory transfer. PCH3 has 13 logical channels. These logical channels are arbitrated on a single transfer size basis in a round-robin fashion. LCH6 to LCH8 and LCH11 are reserved channels and therefore cannot be used.

CHAPTER 5 POWER CONTROL

5.1 Power Supply Control

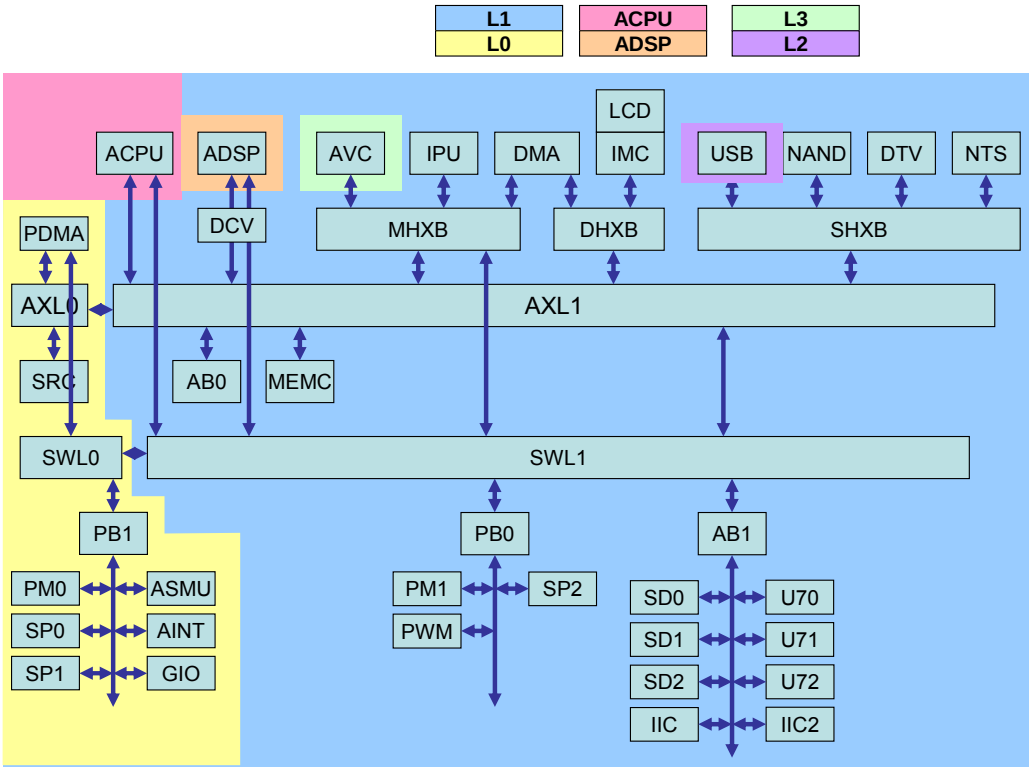
EM1-D512 (logic) divides the core into three power domains to reduce the leakage current. The power of each power domain is turned on and off by controlling the power supply switch in the LSI. The ACPU cannot operate when the power of the L1 domain is turned off, so in this case, the PMU in the L0 domain serves as the master and executes control operations such as register write, power supply control, and wait insertion.

5.1.1 Power supply separation diagram

Figure 5-1 shows the EM1-D512 (logic) power supply separation structure.

In EM1-D512 (logic), the digital parts of the internal core are divided into six power domains: L0, L1, ACPU, ADSP, L3, and L2. The L0 domain includes the ASMU, PMU, AINT, TI0, TW0, SPI0, GIO, PWM, LCD and internal SRAM (128 KB). Power to this domain is always on. Power for other blocks can be switched on and off according to the status transition.

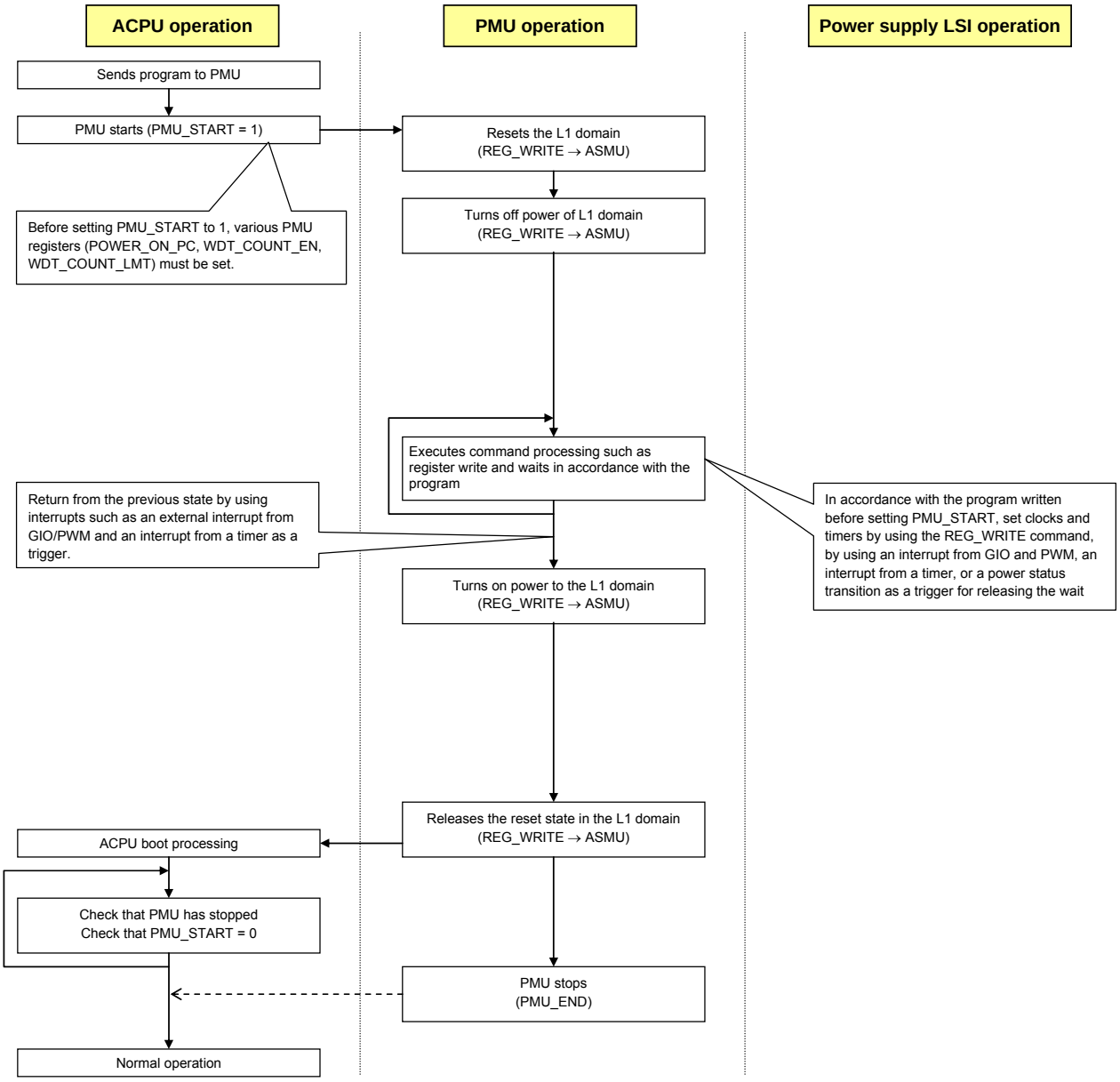
Figure 5-1. EM1-D512 (Logic) Power Supply Separation Diagram



5.1.2 Example of PMU operation when ACPU is stopped

The ACPU cannot operate when the power of the L1 domain is turned off (power save mode), so the PMU in L0 domain serves as the master and executes control operations such as register write, power supply control, and wait insertion. Figure 5-2 shows an example where the PMU turns on the power of the L1 domain after performing various processing and starts the ACPU.

Figure 5-2. Example of PMU Operation When ACPU Is Stopped

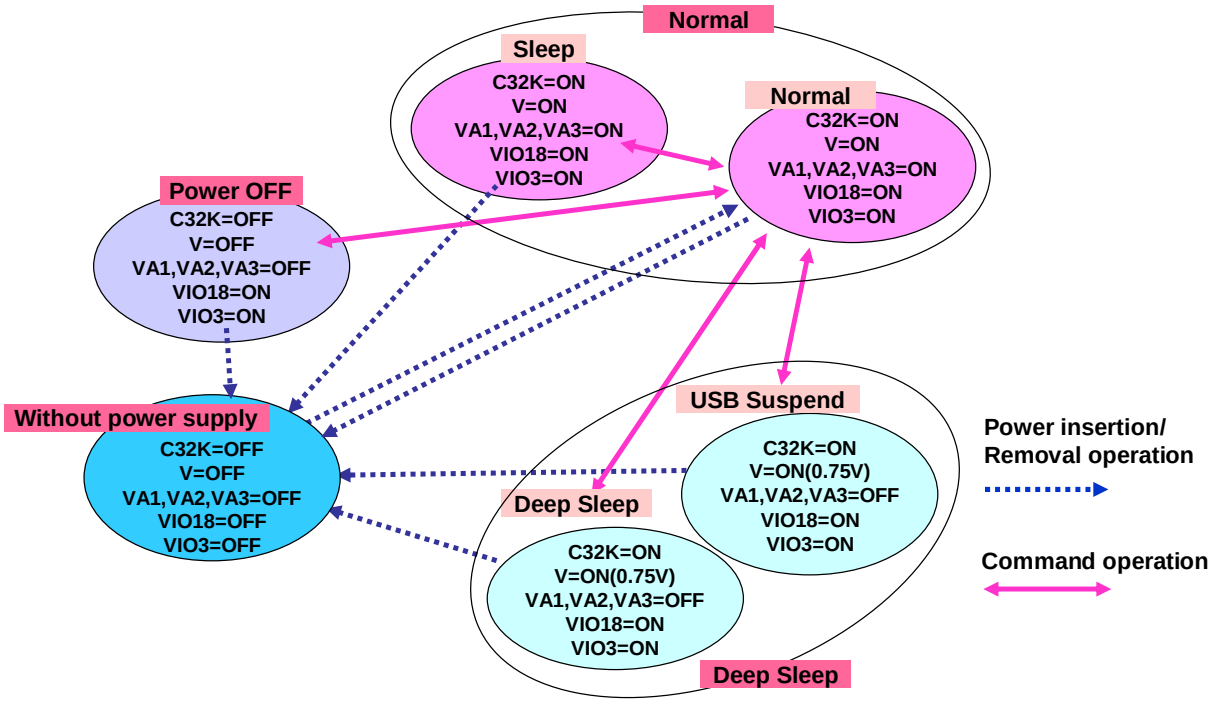


5.2 System State Transition

EM1-D512 can make the system state transfer by combining with Power Management IC.

The following figure showed state transition every system.

Figure 5-3. System State Transition



Pin Name	Function
C32K	Reference clock (32.768 KHz)
V	Core power supply (1.2 V)
VA1, VA2, VA3,	PLL power supply (1.2 V)
VIO18	IO power supply (1.8 V system)
VIO3	IO power supply (3 V system)

Normal (Sleep, Normal)

It's in the state of the normal operation of audio and video playback. Sleep and Normal are the mode to move by the inside PLL frequency. The transfer to Sleep is performed by EM1-D512 control, and it's only the difference in the consumption current as Power Management IC. Power Management IC supplies Core power supply (V) to 1.2V and always supply C32K pin with a clock of 32.768kHz.

DeepSleep (DeepSleep, USB suspend)

Core power supply (V) is set to 0.75V. 0.75V is the internal SRAM retention voltage.

EM1-D512 moves by a clock of 32.768kHz. This mode is in the state of the low current more than the Sleep mode. The transfer to DeepSleep is performed by the command to the Power Management IC from EM1-D512. All release of DeepSleep will be Power Management IC factor. The Power Management IC which received a return factor supplies Core power supply (V) to 1.2V. And Power Management IC hands interrupt signal (GIO_P0) down to EM1-D512.

EM1-D512 begins to carry out return sequence to Normal from DeepSleep by interrupt signal (GIO_P0), and a Warm boot is begun.

PowerOff

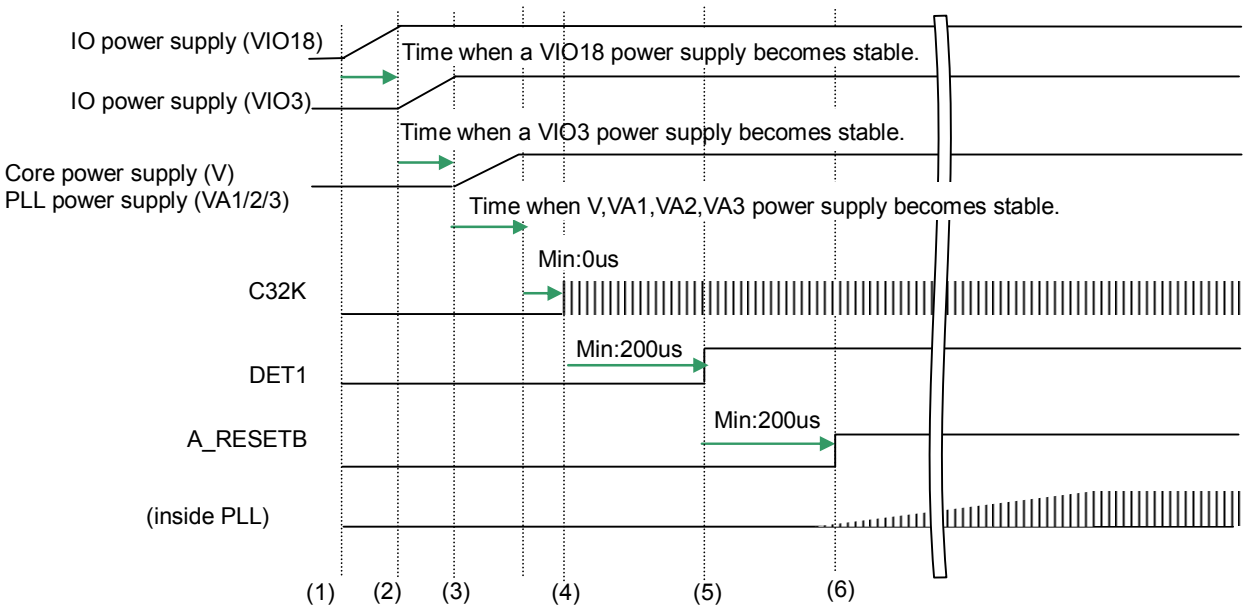
Core power supply (V) and PLL power supply (VA1, VA2, VA3) are stopped. Only IO power supplies (VIO18, VIO3) are in the state turned on. The transfer to PowerOff is performed by the command to the Power Management IC from EM1-D512.The Power Management IC which received a return factor supplies Core power supply (V) of EM1-D512. And the Power Management IC releases a reset signal of EM1-D512 for return from PowerOff. A Cold boot is begun by reset signal release.

Without Power Supply

There are no power supplies on the system. There are no power supplies in EM1-D512 at all. After Power Management IC detects a power supply on the system, a power supply to EM1-D512 and a control signal are started in turn by decided timing.

5.2.1 Power supply start-up Timing (without power supply -> Normal)

Figure 5-4. Power supply start-up timing



Remarks "Stable" means that each power supply becomes the specification minimum voltage.

The timing figure which starts from the "Without power supply".

(1) IO power supply (VIO18) is supplied, and stands by until a power supply becomes stable.

(2) IO power supply (VIO3) is supplied, and stands by until a power supply becomes stable.

(3) Corepower supply (V) and PLL power supply (VA1/2/3) are supplied, and stands by until a power supply becomes stable.

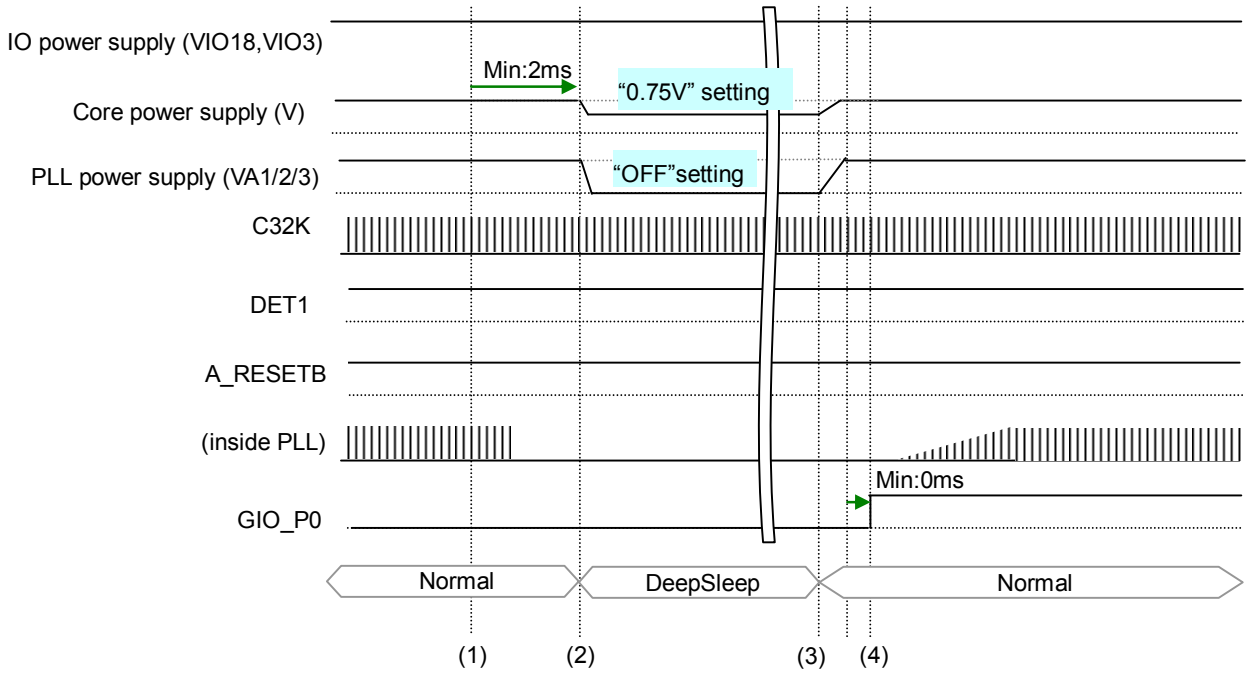
(4) RTC clock 32.768kHz (C32K) is input.

(5) DET1 is signal is started.

(6) A_RESETB signal rising (reset release), and PLL begins to oscillate.

5.2.2 Power supply start-up Timing (DeepSleep<- -> Normal)

Figure 5-5. DeepSleep Normal timing



(1) EM1-D512 sends the command to Power Management IC by SPI Interface. The contents of the command are as follows. Core power supply (V) voltage is changed to 0.75 from 1.2V. PLL power supply (VA1/2/3) is stopped.

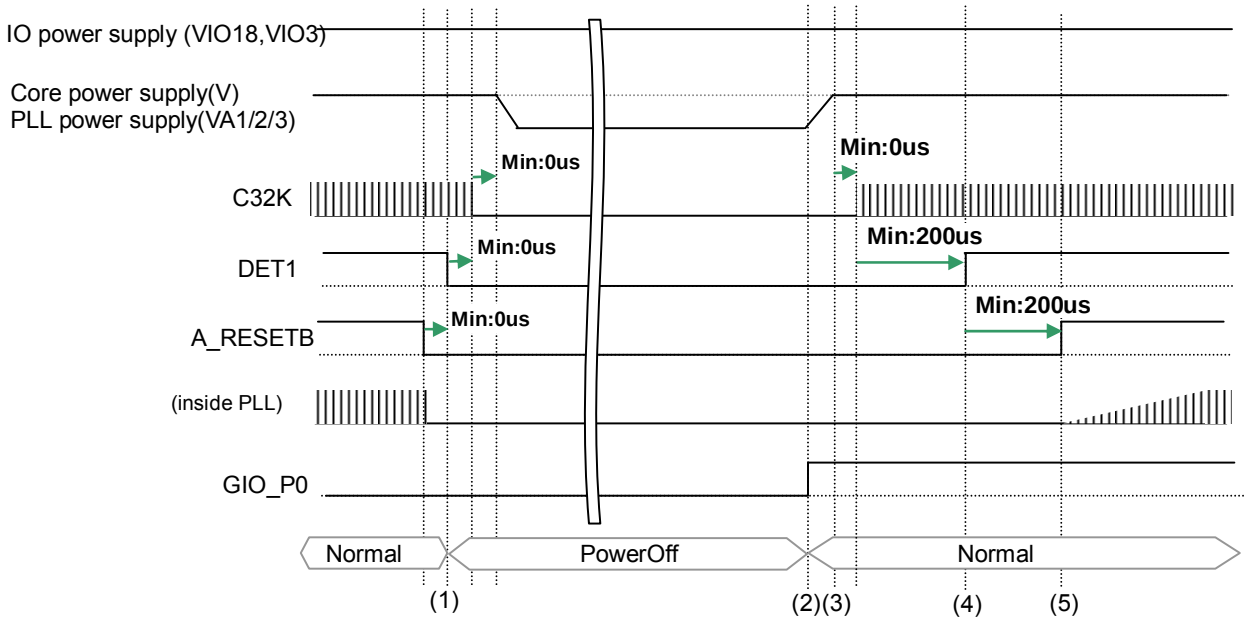
(2) Power Management IC changes the Core power supply (V) to 0.75V from 1.2V in at least 2 ms later and stops PLL power supply (VA1/2/3). EM1-D512 does the preparations to transfer to the DeepSleep state between (1) and (2).

(3) Core power supply (V) voltage is changed to 1.2V from 0.75V. VPLL power supply (VA1/2/3) is supplied.

(4) GIO_P0 signal rising and inside PLL begins to oscillate. EM1-D512 is transit of state from DeepSleep to Normal after inside PLL stable.

5.2.3 Power supply start-up Timing (PowerOff<- -> Normal)

Figure 5-6. PowerOff Normal timing



(1) A_RESETB signal and DET1 signal are falling, and RTC clock (C32K) is stop. Next Core power supply and PLL power supply are stopped at the same time.

(2) Core power supply (V) and PLL power supply (VA1/2/3) are supplied same time, and stand by until a power supplies become stable.

(3) RTC clock 32.768kHz (C32K) is input.

GIO_P0 signal rising. It's to make EM1-D512 recognizes that it's different from "Without power supply".

(4) DET1 is signal is started.

(5) A_RESETB signal rising (reset release), and inside PLL begins to oscillate.

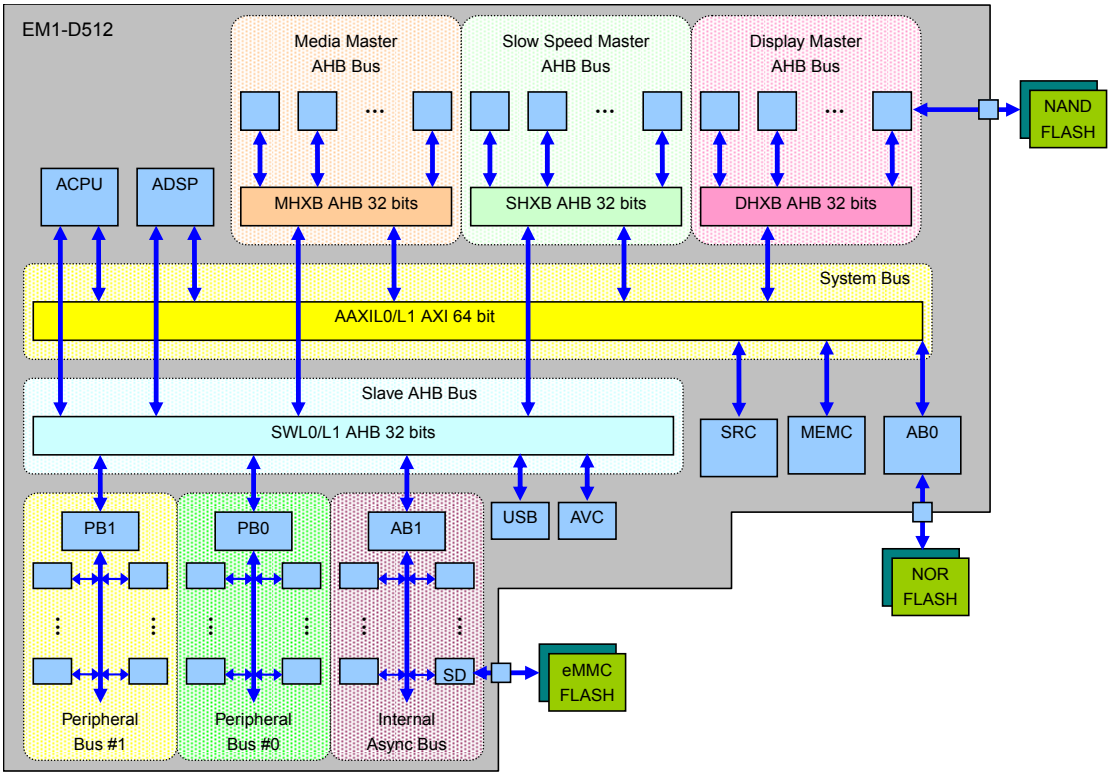
CHAPTER 6 BUS

6.1 General

6.1.1 Bus configuration

Figure 6-1 shows the EM1-D512 bus architecture.

Figure 6-1. EM1-D512 Bus Configuration



EM1-D512 employs the ARM AXI (64 bits, 166 MHz, 3 layers) as the system bus.

The system bus employs a 3-layer AXI bus switch that consists of one AXI bus switch for the memory controller (MEMC), and external memory interface (AB0) and internal SRAM (SRC), respectively.

○ Media master AHB bus (MHXB)

AHB bus to which multimedia-related AHB master devices are mainly connected

○ Display master AHB bus (DHXB)

AHB bus to which image processing-related AHB master devices are mainly connected

○ Slow speed master AHB bus (SHXB)

AHB bus to which AHB master devices that access memory comparatively less frequently are connected

○ Slave AHB bus (SWL0 and SWL1)

AHB bus to which AHB slave devices are connected

○ Peripheral buses 0 and 2

APB bus to which APB slave devices mounted in the domain where power can be turned on or off are connected

○ Peripheral buses 1 and 3

APB bus to which APB slave devices mounted in the domain where power is constantly on are connected

6.1.2 Master-slave connection

The bus slave devices that can be accessed from bus master devices are restricted.

Table 6-1 lists the accessible connections between master and slave devices.

Table 6-1. Master-Slave Connection

		AB0	MEMC	SRC	AB1	PB0	PB1	AHB Slave	ACPU ROM
ACPU		○	○	○	○	○	○	○	○
ADSP_I		○	○	○	–	–	–	–	–
ADSP_D		○	○	○	○	○	○	○	–
PDMA		–	–	○	–	–	○	–	–
DHXB	IMC	○	○	○	–	–	–	–	–
	DMA#0R	○	○	○	–	–	–	–	–
	DMA#3W	○	○	○	–	–	–	–	–
MHXB	IPU (R/W)	○	○	○	–	–	–	–	–
	AVC	○	○	○	–	–	–	–	–
	DMA#0W	○	○	○	–	–	–	–	–
	DMA#2R	○	○	○	–	–	–	–	–
	DMA#2W	–	–	–	○	○	○	○	–
MHHB	DMA#3R	–	–	–	○	○	○	○	–
SHXB	NAND	–	○	○	–	–	–	–	–
	NTS	–	○	○	–	–	–	–	–
	DTV	–	○	○	–	–	–	–	–
	USB	–	○	○	–	–	–	–	–

Remark ○: Accessible, –: Not accessible

CHAPTER 7 INTERRUPT CONTROL

7.1 Interrupt Sources

The interrupt sources that are assigned to INT[0:95] are listed in Table 7-1.

Table 7-1. Interrupt Sources (1/3)

INT No.	Source	Description	Polarity	Type	Interrupt Signal
0	ACPU	Inter-PE communication (ACPU → ADSP)	Positive	Level	(Internal signal)
1	–	Reserved	Positive	Level	Reserved
2	–	Reserved	Positive	Level	Reserved
3	ADSP	Inter-PE communication (ADSP → ACPU)	Positive	Level	(Internal signal)
4	–	Reserved	Positive	Level	Reserved
5	SDIA	SD card interface A	Positive[Note]	Level	SDIA_SD_INT
6	SDIA	SD card interface A	Positive[Note]	Level	SDIA_CC_INT
7	SDIB	SD card interface B	Positive[Note]	Level	SDIB_SD_INT
8	SDIB	SD card interface B	Positive[Note]	Level	SDIB_CC_INT
9	U70	UART0	Positive[Note]	Level	U70_INT
10	U71	UART1	Positive[Note]	Level	U71_INT
11	U72	UART2	Positive[Note]	Level	U72_INT
12	–	Reserved	Positive[Note]	Level	Reserved
13	PCM0	Multi mode serial	Positive[Note]	Level	PM0_INT
14	PCM1	Multi mode serial	Positive[Note]	Level	PM1_INT
15	–	Reserved	Positive[Note]	Level	Reserved
16	–	Reserved	Positive[Note]	Level	Reserved
17	ASMU	ASMU interrupt	Positive[Note]	Level	ASMU_INT
18	MWI	MICROWIRE module interrupt	Positive[Note]	Level	MWI_INT
19	PDMA	miniDMA for PCM0	Positive[Note]	Level	PDMA_INT
20	LCD	LCD control	Positive[Note]	Level	LCD_INT
21	CAM	Camera interface	Positive[Note]	Level	CAM_INT
22	IMG	Image processor	Positive[Note]	Level	IMG_INT
23	ROT	Rotator	Positive[Note]	Level	ROT_INT
24	SP0	SP0 interrupt	Positive[Note]	Level	SP0_INT
25	SP1	SP1 interrupt	Positive[Note]	Level	SP1_INT
26	GIO	GIO6 interrupt	Positive[Note]	Level	GIO6_INT
27	GIO	GIO7 interrupt	Positive[Note]	Level	GIO7_INT
28	NTS	NTSC Enc interface	Positive[Note]	Level	NTS

Note Polarity when polarity inversion is disabled (default) by the corresponding bit in the interrupt input polarity inversion enable set register (IT_PINV_SET[0:2])

Table 7-1. Interrupt Sources (2/3)

INT No.	Source	Description	Polarity	Type	Interrupt Signal
29	SDIC_SD	SD card interface C	Positive[Note]	Level	SDIC_SD
30	SDIC_CC	SD card interface C	Positive[Note]	Level	SDIC_CC
31	–	Reserved	Positive[Note]	Level	Reserved
32	–	Reserved	Positive[Note]	Level	Reserved
33	IIC	IIC	Positive[Note]	Edge	IIC_INT
34	TG0	General-purpose timer 0 interrupt	Positive[Note]	Edge	TG0_TOUT
35	TG1	General-purpose timer 1 interrupt	Positive[Note]	Edge	TG1_TOUT
36	TG2	General-purpose timer 2 interrupt	Positive[Note]	Edge	TG2_TOUT
37	DMA	INT for ACPU	Positive[Note]	Level	DMA_ACPU_INT
38	–	Reserved	Positive[Note]	Level	Reserved
39	IIC2	IIC2 module interrupt	Positive[Note]	Edge	IIC2_INT
40	DMA	INT for ADSP	Positive[Note]	Level	DMA_ADSP_INT
41	USB	USB interrupt	Positive[Note]	Level	USB_ INT
42	SP2	SP2 interrupt	Positive[Note]	Level	SP2_INT
43	USB_WAK	USB_SUSPEND_WAKEUP	Positive[Note]	Edge	USB_SUSPEND_WAKEUP
44	TG3	General timer 3 interrupt	Positive[Note]	Edge	TG3_TOUT
45	TG4	General timer 4 interrupt	Positive[Note]	Edge	TG4_TOUT
46	TG5	General timer 5 interrupt	Positive[Note]	Edge	TG5_TOUT
47	NAND	NAND interrupt	Positive[Note]	Level	NAND_INT
48	DTV	DTV interrupt	Positive[Note]	Level	DTV_INT
49	–	Reserved	Positive[Note]	Level	Reserved
50	GIO	GIO0 interrupt	Positive[Note]	Level	GIO0_INT
51	GIO	GIO1 interrupt	Positive[Note]	Level	GIO1_INT
52	GIO	GIO2 interrupt	Positive[Note]	Level	GIO2_INT
53	GIO	GIO3 interrupt	Positive[Note]	Level	GIO3_INT
54	TI0	Timer 0	Positive[Note]	Edge	TI0_TOUT
55	TI1	Timer 1	Positive[Note]	Edge	TI1_TOUT
56	TI2	Timer 2	Positive[Note]	Edge	TI2_TOUT
57	TI3	Timer 3	Positive[Note]	Edge	TI3_TOUT
58	TW0	Watchdog timer 0	Positive[Note]	Edge	TW0_TOUT
59	TW1	Watchdog timer 1	Positive[Note]	Edge	TW1_TOUT
60	TW2	Watchdog timer 2	Positive[Note]	Edge	TW2_TOUT
61	TW3	Watchdog timer 3	Positive[Note]	Edge	TW3_TOUT
62	–	Reserved	Positive[Note]	Level	Reserved
63	–	Reserved	Positive[Note]	Level	Reserved

Note Polarity when polarity inversion is disabled (default) by the corresponding bit in the interrupt input polarity inversion enable set register (IT_PINV_SET[0:2])

Table 7-1. Interrupt Sources (3/3)

INT No.	Source	Description	Polarity	Type	Interrupt Signal
64	–	Reserved	Positive[Note]	Level	Reserved
65	PMU_ACPU	PMU ACPU interrupt	Positive[Note]	Level	PMU_ACPU_INT
66	AVC_A	AVC bus error	Positive[Note]	Level	AVC_INTA
67	AVC_C	AVC core error	Positive[Note]	Level	AVC_INTC
68	–	Reserved	Positive[Note]	Level	Reserved
69	PWM	PWM module interrupt	Positive[Note]	Level	PWM_INT
70	IMC	IMC module interrupt	Positive[Note]	Level	IMC_INT
71	–	Reserved	Positive[Note]	Level	Reserved
72	IPU_DMA	IPU DMA interrupt	Positive[Note]	Level	IPU_DMA_INT
73	–	Reserved	Positive[Note]	Level	Reserved
74	ACPU_PMU	ACPU PMU interrupt	Positive[Note]	Level	ACPU_PMUIRQ
75	–	Reserved	Positive[Note]	Level	Reserved
76	DCV	DCV bus error	Positive[Note]	Level	DCV_INT
77	–	Reserved	Positive[Note]	Level	Reserved
78	–	Reserved	Positive[Note]	Level	Reserved
79	GIO	GIO4 interrupt	Positive[Note]	Level	GIO4_INT
80	GIO	GIO5 interrupt	Positive[Note]	Level	GIO5_INT
81	IIS0	Internal interrupt status 0	Positive[Note]	Level	IIS0
82	IIS1	Internal interrupt status 1	Positive[Note]	Level	IIS1
83	IIS2	Internal interrupt status 2	Positive[Note]	Level	IIS2
84	IIS3	Internal interrupt status 3	Positive[Note]	Level	IIS3
85	Reserved	Reserved	Positive[Note]	Level	Reserved
86	Reserved	Reserved	Positive[Note]	Level	Reserved
87	Reserved	Reserved	Positive[Note]	Level	Reserved

Note Polarity when polarity inversion is disabled (default) by the corresponding bit in the interrupt input polarity inversion enable set register (IT_PINV_SET[0:2])

Table 7-2 lists the interrupts input to the ACPU only.

Table 7-2. Interrupt Sources (for ACPU Only)

INT No.	Source	Description	Polarity	Type	Interrupt Signal
INT_A88	AAXI_INT_A	AXL1 DMA interrupt	Positive[Note]	Level	AAXI_INT_A
INT_A89	MEMC_ERR	MEMC protect error	Positive[Note]	Level	MEMC_INT_A
INT_A90	AB0_ERR	AB0 protect error	Positive[Note]	Level	AB0_INT_A
INT_A91	PB1_ERR	PB1 protect error	Positive[Note]	Level	PB1_INT_A
INT_A92	SRC_ERR	SRC protect error	Positive[Note]	Level	SRC_INT_A
INT_A93	AXL0_ERR	AXL0 decode error	Positive[Note]	Level	AXL0_INT_A
INT_A94	–	Reserved	Positive[Note]	Level	Reserved
INT_A95	–	Reserved	Positive[Note]	Level	Reserved

Note Polarity when polarity inversion is disabled (default) by the corresponding bit in the interrupt input polarity inversion enable set register (IT_PINV_SET[0:2])

7.1.1 Interrupt output

The following types of interrupt outputs (internal signals) are available.

- ACPU IRQ interrupt (PMU_IQU0Z)
- ACPU FIQ interrupt (PMU_FIQ0Z)
- ADSP interrupt (ADSP_INTP)

(1) IRQ interrupt output (PMU_IRQ0Z)

This signal is used to report the occurrence of an interrupt to the ACPU.

INT_IRQ0Z is available for the ACPU.

- Assert condition

  When an interrupt request is issued due to an unmasked interrupt source.

- Deassert condition

  When the following conditions <1> to <3> are satisfied, or the interrupts are masked (IT0_IDS[0:2]).

  <1> Interprocessor communication interrupt

  All messages from the reception side are cleared (IT[1:4]_IPI0_CLR)

  <2> External interrupts (level)

  Interrupt signal level changed to inactive

  <3> External interrupts (edge)

  All the sources transit to the reset state by setting the ACPU interrupt status reset register (IT0_IIR).

(2) FIQ interrupt output (PMU_FIQ0Z)

- Assert condition

  When the interrupt request signal (GIO_INT_FIQ) is asserted (high) (GIO_INT_FIQ is not masked)

- Deassert condition

  When the interrupt request signal (GIO_INT_FIQ) is asserted (low), or GIO_INT_FIQ is masked

(3) ADSP interrupt output (ADSP_INTP)

- Assert condition

  When an interrupt request is issued due to an unmasked interrupt source

- Deassert condition

  When the following conditions <1> to <3> are satisfied, or the interrupts are masked (IT3_IDS[0:2]) and then the interrupt output signal clear register (ID_CLR) is set

Remark The ID_CLR register (C002_C094) must be set to clear an interrupt once it is issued. The interrupt is not cancelled only by masking it (IT3_IDS[0:2]).

<1> Interprocessor communication interrupt

All messages from the reception side are cleared (IT0_IPI2_CLR).

<2> External interrupts (level)

Interrupt signal level changed to inactive.

<3> External interrupts (edge)

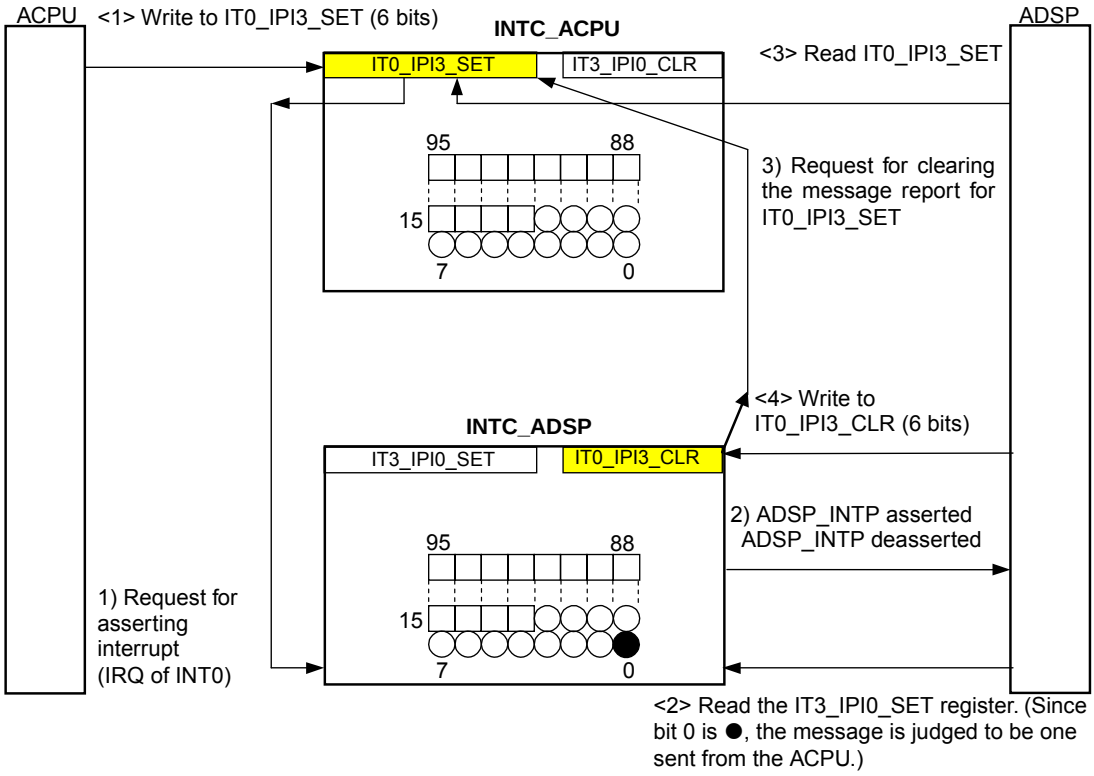
All the sources transit to the reset state by setting the ADSP interrupt status reset register (IT3_IIR).

7.2 Interrupt Control

7.2.1 Interprocessor communication interrupt

Interprocessor communication refers to the operation that reports messages between the ACPU and any of the other processors. (Sending of messages causes interrupt for the receiver processor.)

The following shows an example of interprocessor communication from the ACPU to ADSP.



Remark The filled circle (●) in the above figure shows bit 0 of the interrupt raw status register (IT3_RAW0), which indicates that a message has been sent from the ACPU.

<1> The ACPU writes 00_1010 to the IT0_IPI3_SET register.

1) INTC_ADSP sets bit 0 of the IT0_IPI3_SET register to “1”.

2) INTC_ADSP asserts the ADSP_INTP signal.

<2> The ADSP reads the IT0_IPI3_SET register.

(Since bit 0 holds “1”, the ACPU is judged to be the communication source.)

<3> The ADSP reads the IT0_IPI3_SET register; value 00_1010 is then read out.

<4> The ADSP writes data to the IT0_IPI3_CLR register[Note].

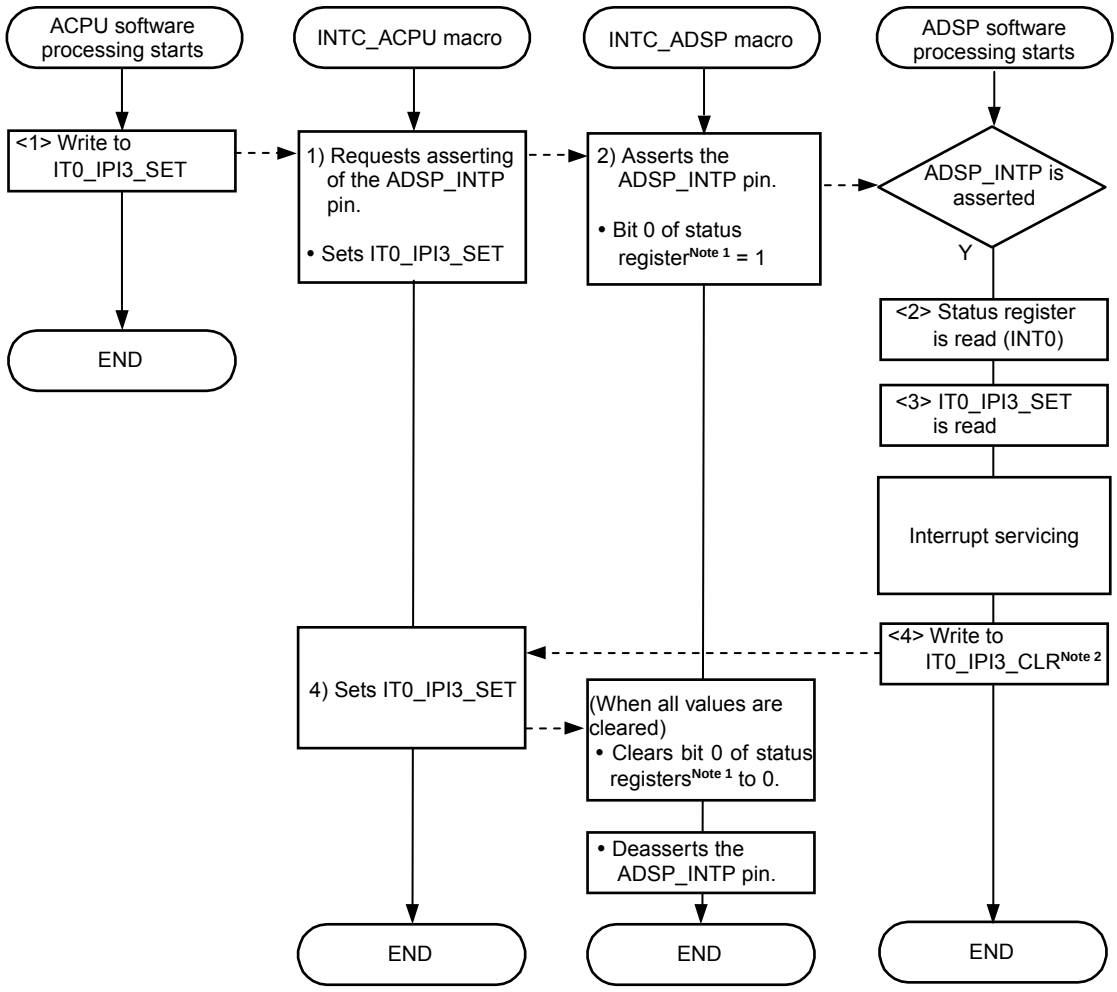
Note The values of bit 0 of the IT0_IPI3_SET register and IT3_RAW0 register vary depending on data written to the IT0_IPI3_CLR register by the ADSP, as follows.

	Value Read from IT0_IPI3_SET	Bit 0 of IT3_RAW0
<1> ITO_IPI3_SET (ACPU write): 00_1010	00_1010	1 is read out. <2>
<4> IT0_IPI3_CLR (ADSP write): 00_1000	00_0010 (* First read)	Retains 1.
<4> IT0_IPI3_CLR (ADSP write): 00_0010	00_0000 (* Second read)	Cleared to 0.

(* First read) When not all of the IT0_IPI3_SET values are cleared, bit 0 of the IT3_RAW0 register retains 1 and the ADSP_INTP signal is kept asserted.

(* Second read) When all the IT0_IPI3_SET values are cleared, bit 0 of the IT3_RAW0 register is cleared to 0 and the ADSP_INTP signal is deasserted if no more interrupt source occurs.

[Flowchart]



Notes 1. The status registers in the above flow refers to the following two registers. At this step, turn on or off these registers at the same time. (The timing may vary depending on the AINT register setting or occurrence of multiple interrupt sources.)

IT*_RAW0: Interrupt raw status register 0

IT*_MST0: Interrupt maskable status register 0

2. The values of bit 0 of the IT0_IPI3_SET register and corresponding status register vary depending on data written to the IT0_IPI3_CLR register by the ADSP, as follows.

	Value Read from IT0_IPI3_SET	Bit 0 of Status Register
<1> ITO_IPI3_SET (ACPU write): 00_1010	00_1010	1 is read out. <2>
<4> IT0_IPI3_CLR (ADSP write): 00_1000	00_0010 (* First read)	Retains 1.
<4> IT0_IPI3_CLR (ADSP write): 00_0010	00_0000 (* Second read)	Cleared to 0.

(* First read) When not all of the IT0_IPI3_SET values are cleared, bit 0 of the corresponding status register retains 1 and the ADSP_INTP signal is kept asserted.

(* Second read) When all the IT0_IPI3_SET values are cleared, bit 0 of the corresponding status register is cleared to 0 and the ADSP_INTP signal is deasserted if no more interrupt source occurs.

CHAPTER 8 ALTERNATE PIN FUNCTION SWITCHING

8.1 Alternate Pin Function Switch Registers

Alternate pin functions are switched using the following registers.

Base address: C014_0000H

(1/2)

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Boot mode register	CHG_BOOT_MODE	R	–
0004H	L1 OFF data hold control register	CHG_L1_HOLD	R/W	0000_0000H
0010H	LSI revision register	CHG_LSI_REVISION	R	0000_0010H
0014H-0100H	Reserved	–	–	–
0104H	SDI (A, B, C) interrupt mask register	CHG_CTRL_SDINT	R/W	0000_0007H
0108H	AB0 (ASYNC) boot switch register	CHG_CTRL_AB0_BOOT	R/W	0000_0000H
0110H	OSC control register	CHG_CTRL_OSC	R/W	0000_0000H
0114H-01FCH	Reserved	–	–	–
0200H	GIO_P[15:0] pin alternate function switch register	CHG_PINSEL_G00	R/W	0000_0000H
0204H	GIO_P[31:16] pin alternate function switch register	CHG_PINSEL_G16	R/W	0000_0000H
0208H	GIO_P[47:32] pin alternate function switch register	CHG_PINSEL_G32	R/W	0000_0000H
020CH	GIO_P[63:48] pin alternate function switch register	CHG_PINSEL_G48	R/W	0000_0000H
0210H	GIO_P[79:64] pin alternate function switch register	CHG_PINSEL_G64	R/W	0000_0000H
0214H	GIO_P[95:80] pin alternate function switch register	CHG_PINSEL_G80	R/W	0000_0000H
0218H	GIO_P[111:96] pin alternate function switch register	CHG_PINSEL_G96	R/W	0000_0000H
021CH	GIO_P[117:112] pin alternate function switch register	CHG_PINSEL_G112	R/W	0000_0000H
0220H-027CH	Reserved	–	–	–
0280H	SP0 pin alternate function switch register	CHG_PINSEL_SP0	R/W	0000_0000H
0284H	DTV pin alternate function switch register	CHG_PINSEL_DTV	R/W	0000_0000H
0288H	SD0 pin alternate function switch register	CHG_PINSEL_SD0	R/W	0000_0000H
028CH	SD1 pin alternate function switch register	CHG_PINSEL_SD1	R/W	0000_0000H
0290H	IIC2 pin alternate function switch register	CHG_PINSEL_IIC2	R/W	0000_0000H
0294H	REFCLKO clock pin switch register	CHG_PINSEL_REFCLKO	R/W	0000_0000H
0298H-029CH	Reserved	–	–	–
0300H	GIO_P[7:0] pin pull-up/pull-down/input enable control register	CHG_PULL_G00	R/W	0000_0000H
0304H	GIO_P[15:8] pin pull-up/pull-down/input enable control register	CHG_PULL_G08	R/W	0000_0000H

(2/2)

Address	Register Name	Register Symbol	R/W	After Reset
0308H	GIO_P[23:16] pin pull-up/pull-down/input enable control register	CHG_PULL_G16	R/W	0000_0000H
030CH	GIO_P[31:24] pin pull-up/pull-down/input enable control register	CHG_PULL_G24	R/W	0000_0000H
0310H	GIO_P[39:32] pin pull-up/pull-down/input enable control register	CHG_PULL_G32	R/W	0000_0000H
0314H	GIO_P[47:40] pin pull-up/pull-down/input enable control register	CHG_PULL_G40	R/W	0000_2200H
0318H	GIO_P[55:48] pin pull-up/pull-down/input enable control register	CHG_PULL_G48	R/W	1111_1111H
031CH	GIO_P[63:56] pin pull-up/pull-down/input enable control register	CHG_PULL_G56	R/W	1111_1111H
0320H	GIO_P[71:64] pin pull-up/pull-down/input enable control register	CHG_PULL_G64	R/W	1111_1111H
0324H	GIO_P[79:72] pin pull-up/pull-down/input enable control register	CHG_PULL_G72	R/W	0000_0000H
0328H	GIO_P[87:80] pin pull-up/pull-down/input enable control register	CHG_PULL_G80	R/W	0000_0000H
032CH	GIO_P[95:88] pin pull-up/pull-down/input enable control register	CHG_PULL_G88	R/W	0000_0000H
0330H	GIO_P[103:96] pin pull-up/pull-down/input enable control register	CHG_PULL_G96	R/W	0000_0000H
0334H	GIO_P[111:104] pin pull-up/pull-down/input enable control register	CHG_PULL_G104	R/W	0000_0000H
0338H	GIO_P[119:112] pin pull-up/pull-down/input enable control register	CHG_PULL_G112	R/W	0000_0000H
033CH	GIO_P[127:120] pin pull-up/pull-down/input enable control register	CHG_PULL_G120	R/W	0000_0000H
0340H-037CH	Reserved	–	–	–
0380H	Pull-up/pull-down/input enable control register 0	CHG_PULL0	R/W	0000_0004H
0384H	Pull-up/pull-down/input enable control register 1	CHG_PULL1	R/W	0000_0600H
0388H	Pull-up/pull-down/input enable control register 2	CHG_PULL2	R/W	0000_1001H
038CH	Pull-up/pull-down/input enable control register 3	CHG_PULL3	R/W	0000_0000H
0390H-039CH	Reserved	–	–	–
0400H	Drive capability switch register 0	CHG_DRIVE0	R/W	5550_0155H
0404H	Drive capability switch register 1	CHG_DRIVE1	R/W	5555_5555H
0408H	Drive capability switch register 2	CHG_DRIVE2	R/W	0001_1555H

8.1.1 Register details

(1) Resetting CHG registers

CHG registers are reset when the DET1 pin is low level.

They are not reset by the system reset pin (A_RESETB).

(2) Boot mode register

CHG_BOOT_MODE: C014_0000H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						TE2	TE1
7	6	5	4	3	2	1	0
Reserved			BOOT_SEL3	BOOT_SEL2	BOOT_SEL1	BOOT_SEL0	UTEST

Name	R/W	Bit	After Reset	Function
Reserved	R	31:10	–	Reserved. When these bits are read, 0 is returned for each bit.
TE2	R	9	–	Indicates the TE2 pin status. This bit is valid only during testing. It is set to “0” in normal mode.
TE1	R	8	–	Indicates the TE1 pin status. This bit is valid only during testing. It is set to “0” in normal mode.
Reserved	R	7:5	–	Reserved. When these bits are read, 0 is returned for each bit.
BOOT_SEL3	R	4	–	Switching to L_SPEED mode (low-speed clock mode)
BOOT_SEL[2:0]	R	3:1	–	Indicates the BOOTSEL pin status. “000” or “101”: Boot AB0 (ASYNC). Other than above: Boot from ROM. BOOT_SEL[2:0] 000: AB0 boot 001: eMMC boot 010: SD boot 011: Reserved 100: Reserved 101: AB0 boot (ADSP JTAG) 110: eMMC boot (ADSP JTAG) 111: SD boot (ADSP JTAG)
UTEST	R	0	–	Indicates the UTEST pin status. 0: Normal 1: Test UTEST is used for testing of the LSI.

(3) L1 OFF data hold control register

CHG_L1_HOLD: C014_0004H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
L1_HOLD_RSV						L1_HOLD	LATCH_TRIG

Name	R/W	Bit	After Reset	Function
Reserved	R	31:8	–	Reserved. When these bits are read, 0 is returned for each bit.
L1_HOLD_RSV	R/W	7:2	0	Spare bits for HOLD.
L1_HOLD	R/W	1	0	0: Through output 1: Outputs latched data
LATCH_TRIG	W	0	0	When this bit is set to 1, the signals from the L1 domain are latched in CHG. When this bit is read, 0 is returned.

(4) LSI revision register

CHG_LSI_REVISION: C014_0010H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
LSI_REV							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:8	–	Reserved. When these bits are read, 0 is returned for each bit.
LSI_REV	R	7:0	0001_0000b	Indicates the LSI revision number.

(5) SDI interrupt mask register

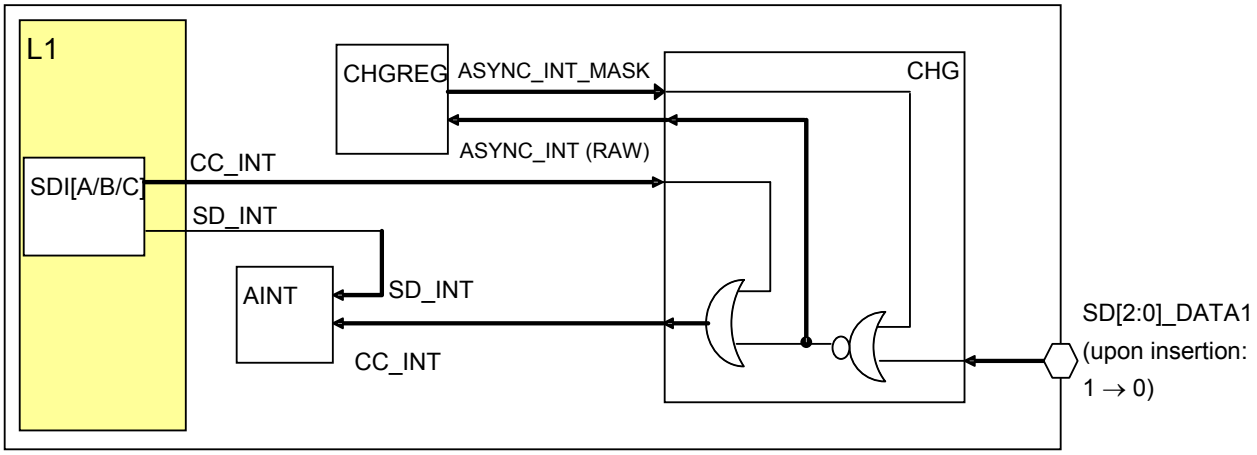
This register (CHG_CTRL_SDINT: C014_0104H) sets masking of the interrupt signals (SYNC_INT) for SDIA, SDIB, and SDIC.

The occurrence of an interrupt from the SD pin (DATA1) is reported to AINT when the SD macro is not operating.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	SDI2(C)_ ASYNC_INT	SDI1(B)_ ASYNC_INT	SDI0(A)_ ASYNC_INT	Reserved	SDI2(C)_ASYNC_INT_MASK	SDI1(B)_ASYNC_INT_MASK	SDI0(A)_ASYNC_INT_MASK

Name	R/W	Bit	After Reset	Function
Reserved	R	31:7	–	Reserved. When these bits are read, 0 is returned for each bit.
SDI2(C)_ASYNC_INT	R	6	0	Indicates the status of the SDI2(C)_ASYNC_INT signal after it is masked. 0: No interrupt source 1: No interrupt source (when masking is canceled)
SDI1(B)_ASYNC_INT	R	5	0	Indicates the status of the SDI1(B)_ASYNC_INT signal after it is masked. 0: No interrupt source 1: No interrupt source (when masking is canceled)
SDI0(A)_ASYNC_INT	R	4	0	Indicates the status of the SDI0(A)_ASYNC_INT signal after it is masked. 0: No interrupt source 1: No interrupt source (when masking is canceled)
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
SDI2(C)_ASYNC_INT_MASK	R/W	2	1	Sets masking of the SDI2(C)_ASYNC_INT signal. 0: Cancels masking 1: Sets masking (default)
SDI1(B)_ASYNC_INT_MASK	R/W	1	1	Sets masking of the SDI1(B)_ASYNC_INT signal. 0: Cancels masking 1: Sets masking (default)
SDI0(A)_ASYNC_INT_MASK	R/W	0	1	Sets masking of the SDI0(A)_ASYNC_INT signal. 0: Cancels masking 1: Sets masking (default)



An interrupt from the external DATA1 pin is detected when the SDI[A/B/C] macro is in the reset state (or the power is off).

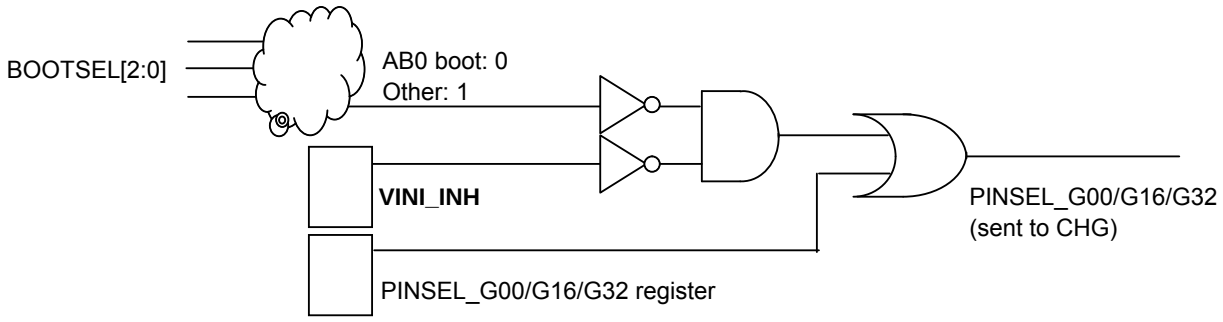
This mechanism is provided individually or SDIA, SDIB and SDIC.

(6) AB0 (ASYNC) boot switch register

This register (CHG_CTRL_AB0_BOOT: C014_0108H) enables selection of the function of the target pin (from AB0-fixed to GPIO-selectable), when a macro is boot from the memory connected to AB0 (ASYNC). Before enabling the setting of the relevant bit, the setting specified by PINSEL must be fixed in advance.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						MODE_VINI	VINI_INH

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	–	Reserved. When these bits are read, 0 is returned for each bit.
MODE_VINI	R	1	–	Indicates the selection mode through external setting by using the GPIO/AB0 pins. 0: AB0 selection mode 1: Ordinary selection
VINI_INH	R/W	0	0	1: Cancels selection of AB0 and enables selection via PINSEL. GPIO11 to GPIO47 are selectable.



Set VINI_INH to 1 so that the value 1, which is sent to CHG for pin selection, is logically masked and the register logic is genuinely enabled.

When the power is turned on, GIO_P11 to GIO_P47 are usually selected as the AB0 pins. The AB0 functions are selected via software, but this does not enable booting from AB0 (asynchronous memory). Therefore, forcibly select the boot from AB0 by using the BOOTSEL[2:0] pins (= “000”).

At this time, the MODE_VINI bit shows “0”. If the VINI_INH bit is set to “1”, the default selection is restored. Note, at this time, that the settings of the PINSEL_G00, PINSEL_G16, and PINSEL_G32 registers are reflected as is and therefore these registers should be set in advance.

The above diagram shows a circuit that forcibly selects AB0 and releases the selection by software (returns to the default selection).

(7) OSC control register

This register (CHG_CTRL_OSC: C014_0110H) controls an oscillator.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						OSC_THRU	OSC_EN

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	–	Reserved. When these bits are read, 0 is returned for each bit.
OSC_THRU	R/W	1	0	Sets whether to pass the output from the oscillator in the EM1-D512 logic through as is. When this bit is set to 1, CKO is latched the internal circuits. 0: Does not pass the output through (normal state when a resonator is connected) 1: Passes the output through (CKO is input)
OSC_EN	R/W	0	0	Sets whether to enable the oscillator in the EM1-D512 logic. 0: Disables the oscillator. 1: Enables the oscillator.

(8) GIO_P[15:0] pin alternate function switch register

This register (CHG_PINSEL_G00: C014_0200H) switches the GIO_P[15:0] pin functions.

To change the setting of CHG_PINSEL_xx that alternately functions as GIO, change the setting basically by using GIO_Pxx.

When switching pins according to the function, note that some pins may also be used as GIO pins.

31 30	29 28	27 26	25 24
GIO_P15[1:0]	GIO_P14[1:0]	GIO_P13[1:0]	GIO_P12[1:0]

23 22	21 20	19 18	17 16
GIO_P11[1:0]	GIO_P10[1:0]	GIO_P09[1:0]	GIO_P08[1:0]

15 14	13 12	11 10	9 8
GIO_P07[1:0]	GIO_P06[1:0]	GIO_P05[1:0]	GIO_P04[1:0]

7 6	5 4	3 2	1 0
GIO_P03[1:0]	GIO_P02[1:0]	GIO_P01[1:0]	GIO_P00[1:0]

Name	R/W	Bit	After Reset	Function
GIO_P15[1:0]	R/W	31:30	0	Switches the GIO_P15 pin functions.
GIO_P14[1:0]	R/W	29:28	0	Switches the GIO_P14 pin functions.
GIO_P13[1:0]	R/W	27:26	0	Switches the GIO_P13 pin functions.
GIO_P12[1:0]	R/W	25:24	0	Switches the GIO_P12 pin functions.
GIO_P11[1:0]	R/W	23:22	0	Switches the GIO_P11 pin functions.
GIO_P10[1:0]	R/W	21:20	0	Switches the GIO_P10 pin functions.
GIO_P09[1:0]	R/W	19:18	0	Switches the GIO_P09 pin functions.
GIO_P08[1:0]	R/W	17:16	0	Switches the GIO_P08 pin functions.
GIO_P07[1:0]	R/W	15:14	0	Switches the GIO_P07 pin functions.
GIO_P06[1:0]	R/W	13:12	0	Switches the GIO_P06 pin functions.
GIO_P05[1:0]	R/W	11:10	0	Switches the GIO_P05 pin functions.
GIO_P04[1:0]	R/W	9:8	0	Switches the GIO_P04 pin functions.
GIO_P03[1:0]	R/W	7:6	0	Switches the spare GIO_P03 pin functions.
GIO_P02[1:0]	R/W	5:4	0	Switches the spare GIO_P02 pin functions.
GIO_P01[1:0]	R/W	3:2	0	Switches the GIO_P01 pin functions.
GIO_P00[1:0]	R/W	1:0	0	Switches the spare GIO_P00 pin functions.

PINSEL_GIO_Pxx	2'b00	2'b01	2'b10	2'b11	Description
Pin Name	Default				
GIO_P0	GIO_P0				
GIO_P1	GIO_P1	USB_WAKEUP	USB_ PWR_FAULT		
GIO_P2	GIO_P2				
GIO_P3	GIO_P3				
GIO_P4	GIO_P4		NAND_RB1	CAM_SCLK	
GIO_P5	GIO_P5		NAND_RB2		
GIO_P6	GIO_P6		NAND_RB3		
GIO_P7	GIO_P7		NAND_CE0		
GIO_P8	GIO_P8		NAND_CE1		
GIO_P9	GIO_P9		NAND_CE2		
GIO_P10	GIO_P10		NAND_CE3		
AB0_CLK	GIO_P11	AB0_CLK	NTS_CLK		
AB0_AD0	GIO_P12	AB0_AD0			
AB0_AD1	GIO_P13	AB0_AD1			
AB0_AD2	GIO_P14	AB0_AD2			
AB0_AD3	GIO_P15	AB0_AD3			

(9) GIO_P[31:16] pin alternate function switch register

This register (CHG_PINSEL_G16: C014_0204H) switches the GIO_P[31:16] pin functions.

To change the setting of CHG_PINSEL_xx that alternately functions as GIO, change the setting basically by using GIO_Pxx.

When switching pins according to the function, note that some pins may also be used as GIO pins.

31	30	29	28	27	26	25	24
GIO_P31[1:0]		GIO_P30[1:0]		GIO_P29[1:0]		GIO_P28[1:0]	
23	22	21	20	19	18	17	16
GIO_P27[1:0]		GIO_P26[1:0]		GIO_P25[1:0]		GIO_P24[1:0]	
15	14	13	12	11	10	9	8
GIO_P23[1:0]		GIO_P22[1:0]		GIO_P21[1:0]		GIO_P20[1:0]	
7	6	5	4	3	2	1	0
GIO_P19[1:0]		GIO_P18[1:0]		GIO_P17[1:0]		GIO_P16[1:0]	

Name	R/W	Bit	After Reset	Function
GIO_P31[1:0]	R/W	31:30	0	Switches the GIO_P31 pin functions.
GIO_P30[1:0]	R/W	29:28	0	Switches the GIO_P30 pin functions.
GIO_P29[1:0]	R/W	27:26	0	Switches the GIO_P29 pin functions.
GIO_P28[1:0]	R/W	25:24	0	Switches the GIO_P28 pin functions.
GIO_P27[1:0]	R/W	23:22	0	Switches the GIO_P27 pin functions.
GIO_P26[1:0]	R/W	21:20	0	Switches the GIO_P26 pin functions.
GIO_P25[1:0]	R/W	19:18	0	Switches the GIO_P25 pin functions.
GIO_P24[1:0]	R/W	17:16	0	Switches the GIO_P24 pin functions.
GIO_P23[1:0]	R/W	15:14	0	Switches the GIO_P23 pin functions.
GIO_P22[1:0]	R/W	13:12	0	Switches the GIO_P22 pin functions.
GIO_P21[1:0]	R/W	11:10	0	Switches the GIO_P21 pin functions.
GIO_P20[1:0]	R/W	9:8	0	Switches the GIO_P20 pin functions.
GIO_P19[1:0]	R/W	7:6	0	Switches the GIO_P19 pin functions.
GIO_P18[1:0]	R/W	5:4	0	Switches the GIO_P18 pin functions.
GIO_P17[1:0]	R/W	3:2	0	Switches the GIO_P17 pin functions.
GIO_P16[1:0]	R/W	1:0	0	Switches the GIO_P16 pin functions.

PINSEL_GIO_Pxx	2'b00	2'b01	2'b10	2'b11	Description
Pin Name	Default				
AB0_AD4	GIO_P16	AB0_AD4			
AB0_AD5	GIO_P17	AB0_AD5			
AB0_AD6	GIO_P18	AB0_AD6			
AB0_AD7	GIO_P19	AB0_AD7			
AB0_AD8	GIO_P20	AB0_AD8			
AB0_AD9	GIO_P21	AB0_AD9			
AB0_AD10	GIO_P22	AB0_AD10			
AB0_AD11	GIO_P23	AB0_AD11			
AB0_AD12	GIO_P24	AB0_AD12			
AB0_AD13	GIO_P25	AB0_AD13			
AB0_AD14	GIO_P26	AB0_AD14			
AB0_AD15	GIO_P27	AB0_AD15			
AB0_A17	GIO_P28	AB0_A17	NTS_DATA0		
AB0_A18	GIO_P29	AB0_A18	NTS_DATA1		
AB0_A19	GIO_P30	AB0_A19	NTS_DATA2		
AB0_A20	GIO_P31	AB0_A20			

(10) GIO_P[47:32] pin alternate function switch register

This register (CHG_PINSEL_G32: C014_0208) switches the GIO_P[47:32] pin functions.

To change the setting of CHG_PINSEL_xx that alternately functions as GIO, change the setting basically by using GIO_Pxx.

When switching pins according to the function, note that some pins may also be used as GIO pins.

31 30	29 28	27 26	25 24
GIO_P47[1:0]	GIO_P46[1:0]	GIO_P45[1:0]	GIO_P44[1:0]

23 22	21 20	19 18	17 16
GIO_P43[1:0]	GIO_P42[1:0]	GIO_P41[1:0]	GIO_P40[1:0]

15 14	13 12	11 10	9 8
GIO_P39[1:0]	GIO_P38[1:0]	GIO_P37[1:0]	GIO_P36[1:0]

7 6	5 4	3 2	1 0
GIO_P35[1:0]	GIO_P34[1:0]	GIO_P33[1:0]	GIO_P32[1:0]

Name	R/W	Bit	After Reset	Function
GIO_P47[1:0]	R/W	31:30	0	Switches the GIO_P47 pin functions.
GIO_P46[1:0]	R/W	29:28	0	Switches the GIO_P46 pin functions.
GIO_P45[1:0]	R/W	27:26	0	Switches the GIO_P45 pin functions.
GIO_P44[1:0]	R/W	25:24	0	Switches the GIO_P44 pin functions.
GIO_P43[1:0]	R/W	23:22	0	Switches the GIO_P43 pin functions.
GIO_P42[1:0]	R/W	21:20	0	Switches the GIO_P42 pin functions.
GIO_P41[1:0]	R/W	19:18	0	Switches the GIO_P41 pin functions.
GIO_P40[1:0]	R/W	17:16	0	Switches the GIO_P40 pin functions.
GIO_P39[1:0]	R/W	15:14	0	Switches the GIO_P39 pin functions.
GIO_P38[1:0]	R/W	13:12	0	Switches the GIO_P38 pin functions.
GIO_P37[1:0]	R/W	11:10	0	Switches the GIO_P37 pin functions.
GIO_P36[1:0]	R/W	9:8	0	Switches the GIO_P36 pin functions.
GIO_P35[1:0]	R/W	7:6	0	Switches the GIO_P35 pin functions.
GIO_P34[1:0]	R/W	5:4	0	Switches the GIO_P34 pin functions.
GIO_P33[1:0]	R/W	3:2	0	Switches the GIO_P33 pin functions.
GIO_P32[1:0]	R/W	1:0	0	Switches the GIO_P32 pin functions.

PINSEL_GIO_Pxx	2'b00	2'b01	2'b10	2'b11	Description
Pin Name	Default				
AB0_A21	GIO_P32	AB0_A21			
AB0_A22	GIO_P33	AB0_A22			
AB0_A23	GIO_P34	AB0_A23			
AB0_A24	GIO_P35	AB0_A24			
AB0_A25	GIO_P36	AB0_A25			
AB0_A26	GIO_P37	AB0_A26			
AB0_ADV	GIO_P38	AB0_ADV			
AB0_RDB	GIO_P39	AB0_RDB	NTS_DATA3		
AB0_WRB	GIO_P40	AB0_WRB	NTS_DATA4		
AB0_WAIT	GIO_P41	AB0_WAIT	NTS_DATA5		
AB0_CSB0	GIO_P42	AB0_CSB0	NTS_DATA6		
AB0_CSB1	GIO_P43	AB0_CSB1	NTS_DATA7		
AB0_CSB2	GIO_P44	AB0_CSB2	NTS_VS		
AB0_CSB3	GIO_P45	AB0_CSB3	NTS_HS		
AB0_BEN0	GIO_P46	AB0_BEN0			
AB0_BEN1	GIO_P47	AB0_BEN1			

(11) GIO_P[63:48] pin alternate function switch register

This register (CHG_PINSEL_G48: C014_020CH) switches the GIO_P[63:48] pin functions.

To change the setting of CHG_PINSEL_xx that alternately functions as GIO, change the setting basically by using GIO_Pxx.

When switching pins according to the function, note that some pins may also be used as GIO pins.

31 30	29 28	27 26	25 24
GIO_P63[1:0]	GIO_P62[1:0]	GIO_P61[1:0]	GIO_P60[1:0]

23 22	21 20	19 18	17 16
GIO_P59[1:0]	GIO_P58[1:0]	GIO_P57[1:0]	GIO_P56[1:0]

15 14	13 12	11 10	9 8
GIO_P55[1:0]	GIO_P54[1:0]	GIO_P53[1:0]	GIO_P52[1:0]

7 6	5 4	3 2	1 0
GIO_P51[1:0]	GIO_P50[1:0]	GIO_P49[1:0]	GIO_P48[1:0]

Name	R/W	Bit	After Reset	Function
GIO_P63[1:0]	R/W	31:30	0	Switches the GIO_P63 pin functions.
GIO_P62[1:0]	R/W	29:28	0	Switches the GIO_P62 pin functions.
GIO_P61[1:0]	R/W	27:26	0	Switches the GIO_P61 pin functions.
GIO_P60[1:0]	R/W	25:24	0	Switches the GIO_P60 pin functions.
GIO_P59[1:0]	R/W	23:22	0	Switches the GIO_P59 pin functions.
GIO_P58[1:0]	R/W	21:20	0	Switches the GIO_P58 pin functions.
GIO_P57[1:0]	R/W	19:18	0	Switches the GIO_P57 pin functions.
GIO_P56[1:0]	R/W	17:16	0	Switches the GIO_P56 pin functions.
GIO_P55[1:0]	R/W	15:14	0	Switches the GIO_P55 pin functions.
GIO_P54[1:0]	R/W	13:12	0	Switches the GIO_P54 pin functions.
GIO_P53[1:0]	R/W	11:10	0	Switches the GIO_P53 pin functions.
GIO_P52[1:0]	R/W	9:8	0	Switches the GIO_P52 pin functions.
GIO_P51[1:0]	R/W	7:6	0	Switches the GIO_P51 pin functions.
GIO_P50[1:0]	R/W	5:4	0	Switches the GIO_P50 pin functions.
GIO_P49[1:0]	R/W	3:2	0	Switches the GIO_P49 pin functions.
GIO_P48[1:0]	R/W	1:0	0	Switches the GIO_P48 pin functions.

PINSEL_GIO_Pxx	2'b00	2'b01	2'b10	2'b11	Description
Pin Name	Default				
SP0_CS1	GIO_P48	SP0_CS1			
SP0_CS2	GIO_P49	SP0_CS2			
LCD_PXCLK	GIO_P50	LCD_PXCLK			Switched when using LCD
LCD_R0	GIO_P51	LCD_R0			Switched when using LCD
LCD_R1	GIO_P52	LCD_R1			Switched when using LCD
LCD_R2	GIO_P53	LCD_R2			Switched when using LCD
LCD_R3	GIO_P54	LCD_R3			Switched when using LCD
LCD_R4	GIO_P55	LCD_R4			Switched when using LCD
LCD_R5	GIO_P56	LCD_R5			Switched when using LCD
LCD_G0	GIO_P57	LCD_G0			Switched when using LCD
LCD_G1	GIO_P58	LCD_G1			Switched when using LCD
LCD_G2	GIO_P59	LCD_G2			Switched when using LCD
LCD_G3	GIO_P60	LCD_G3			Switched when using LCD
LCD_G4	GIO_P61	LCD_G4			Switched when using LCD
LCD_G5	GIO_P62	LCD_G5			Switched when using LCD
LCD_B0	GIO_P63	LCD_B0			Switched when using LCD

(12) GIO_P[79:64] pin alternate function switch register

This register (CHG_PINSEL_G64: C014_0210H) switches the GIO_P[79:64] pin functions.

To change the setting of CHG_PINSEL_xx that alternately functions as GIO, change the setting basically by using GIO_Pxx.

When switching pins according to the function, note that some pins may also be used as GIO pins.

31 30	29 28	27 26	25 24
GIO_P79[1:0]	GIO_P78[1:0]	GIO_P77[1:0]	GIO_P76[1:0]

23 22	21 20	19 18	17 16
GIO_P75[1:0]	GIO_P74[1:0]	GIO_P73[1:0]	GIO_P72[1:0]

15 14	13 12	11 10	9 8
GIO_P71[1:0]	GIO_P70[1:0]	GIO_P69[1:0]	GIO_P68[1:0]

7 6	5 4	3 2	1 0
GIO_P67[1:0]	GIO_P66[1:0]	GIO_P65[1:0]	GIO_P64[1:0]

Name	R/W	Bit	After Reset	Function
GIO_P79[1:0]	R/W	31:30	0	Switches the GIO_P79 pin functions.
GIO_P78[1:0]	R/W	29:28	0	Switches the GIO_P78 pin functions.
GIO_P77[1:0]	R/W	27:26	0	Switches the GIO_P77 pin functions.
GIO_P76[1:0]	R/W	25:24	0	Switches the GIO_P76 pin functions.
GIO_P75[1:0]	R/W	23:22	0	Switches the GIO_P75 pin functions.
GIO_P74[1:0]	R/W	21:20	0	Switches the GIO_P74 pin functions.
GIO_P73[1:0]	R/W	19:18	0	Switches the GIO_P73 pin functions.
GIO_P72[1:0]	R/W	17:16	0	Switches the GIO_P72 pin functions.
GIO_P71[1:0]	R/W	15:14	0	Switches the GIO_P71 pin functions.
GIO_P70[1:0]	R/W	13:12	0	Switches the GIO_P70 pin functions.
GIO_P69[1:0]	R/W	11:10	0	Switches the GIO_P69 pin functions.
GIO_P68[1:0]	R/W	9:8	0	Switches the GIO_P68 pin functions.
GIO_P67[1:0]	R/W	7:6	0	Switches the GIO_P67 pin functions.
GIO_P66[1:0]	R/W	5:4	0	Switches the GIO_P66 pin functions.
GIO_P65[1:0]	R/W	3:2	0	Switches the GIO_P65 pin functions.
GIO_P64[1:0]	R/W	1:0	0	Switches the GIO_P64 pin functions.

PINSEL_GIO_Pxx	2'b00	2'b01	2'b10	2'b11	Description
Pin Name	Default				
LCD_B1	GIO_P64	LCD_B1			Switched when using LCD
LCD_B2	GIO_P65	LCD_B2			Switched when using LCD
LCD_B3	GIO_P66	LCD_B3			Switched when using LCD
LCD_B4	GIO_P67	LCD_B4			Switched when using LCD
LCD_B5	GIO_P68	LCD_B5			Switched when using LCD
LCD_HSYNC	GIO_P69	LCD_HSYNC			Switched when using LCD
LCD_VSYNC	GIO_P70	LCD_VSYNC			Switched when using LCD
LCD_ENABLE	GIO_P71	LCD_ENABLE			Switched when using LCD
NTS_CLK	GIO_P72	NTS_CLK		PM1_CLK	
NTS_VS	GIO_P73	NTS_VS	SP1_CLK		
NTS_HS	GIO_P74	NTS_HS	SP1_SI		
NTS_DATA0	GIO_P75	NTS_DATA0	SP1_SO	CAM_YUV0	
NTS_DATA1	GIO_P76	NTS_DATA1	SP1_CS0	CAM_YUV1	
NTS_DATA2	GIO_P77	NTS_DATA2	SP1_CS1	CAM_YUV2	
NTS_DATA3	GIO_P78	NTS_DATA3	SP1_CS2	CAM_YUV3	
NTS_DATA4	GIO_P79	NTS_DATA4	SP1_CS3	CAM_YUV4	

(13) GIO_P[95:80] pin alternate function switch register

This register (CHG_PINSEL_G80: C014_0214H) switches the GIO_P[95:80] pin functions.

To change the setting of CHG_PINSEL_xx that alternately functions as GIO, change the setting basically by using GIO_Pxx.

When switching pins according to the function, note that some pins may also be used as GIO pins.

31 30	29 28	27 26	25 24
GIO_P95[1:0]	GIO_P94[1:0]	GIO_P93[1:0]	GIO_P92[1:0]

23 22	21 20	19 18	17 16
GIO_P91[1:0]	GIO_P90[1:0]	GIO_P89[1:0]	GIO_P88[1:0]

15 14	13 12	11 10	9 8
GIO_P87[1:0]	GIO_P86[1:0]	GIO_P85[1:0]	GIO_P84[1:0]

7 6	5 4	3 2	1 0
GIO_P83[1:0]	GIO_P82[1:0]	GIO_P81[1:0]	GIO_P80[1:0]

Name	R/W	Bit	After Reset	Function
GIO_P95[1:0]	R/W	31:30	0	Switches the GIO_P95 pin functions.
GIO_P94[1:0]	R/W	29:28	0	Switches the GIO_P94 pin functions.
GIO_P93[1:0]	R/W	27:26	0	Switches the GIO_P93 pin functions.
GIO_P92[1:0]	R/W	25:24	0	Switches the GIO_P92 pin functions.
GIO_P91[1:0]	R/W	23:22	0	Switches the GIO_P91 pin functions.
GIO_P90[1:0]	R/W	21:20	0	Switches the GIO_P90 pin functions.
GIO_P89[1:0]	R/W	19:18	0	Switches the GIO_P89 pin functions.
GIO_P88[1:0]	R/W	17:16	0	Switches the GIO_P88 pin functions.
GIO_P87[1:0]	R/W	15:14	0	Switches the GIO_P87 pin functions.
GIO_P86[1:0]	R/W	13:12	0	Switches the GIO_P86 pin functions.
GIO_P85[1:0]	R/W	11:10	0	Switches the GIO_P85 pin functions.
GIO_P84[1:0]	R/W	9:8	0	Switches the GIO_P84 pin functions.
GIO_P83[1:0]	R/W	7:6	0	Switches the GIO_P83 pin functions.
GIO_P82[1:0]	R/W	5:4	0	Switches the GIO_P82 pin functions.
GIO_P81[1:0]	R/W	3:2	0	Switches the GIO_P81 pin functions.
GIO_P80[1:0]	R/W	1:0	0	Switches the GIO_P80 pin functions.

PINSEL_GIO_Pxx	2'b00	2'b01	2'b10	2'b11	Description
Pin Name	Default				
NTS_DATA5	GIO_P80	NTS_DATA5	SP1_CS4	PM1_SEN	
NTS_DATA6	GIO_P81	NTS_DATA6	SP1_CS5	PM1_SI	
NTS_DATA7	GIO_P82	NTS_DATA7		PM1_SO	
IIC_SCL	GIO_P83	IIC_SCL			
IIC_SDA	GIO_P84	IIC_SDA			
URT0_CTSB	GIO_P85	URT0_CTSB	URT1_SRIN		
URT0_RTSB	GIO_P86	URT0_RTSB	URT1_SOUT		
PM0_SI	GIO_P87	PM0_SI			Switched when using PM0
SD0_DATA1	GIO_P88	SD0_DATA1			
SD0_DATA2	GIO_P89	SD0_DATA2			
SD0_DATA3	GIO_P90	SD0_DATA3			
SD0_CKI	GIO_P91	SD0_CKI			
SD1_CKI	GIO_P92	SD1_CKI	CAM_CLKI		
SD2_CKI	GIO_P93	SD2_CKI	NAND_OE		
PWM0	GIO_P94	PWM0			
PWM1	GIO_P95	PWM1			

(14) GIO_P[111:96] pin alternate function switch register

This register (CHG_PINSEL_G96: C014_0218H) switches the GIO_P[111:96] pin functions.

To change the setting of CHG_PINSEL_xx that alternately functions as GIO, change the setting basically by using GIO_Pxx.

When switching pins according to the function, note that some pins may also be used as GIO pins.

31 30	29 28	27 26	25 24
GIO_P111[1:0]	GIO_P110[1:0]	GIO_P109[1:0]	GIO_P108[1:0]

23 22	21 20	19 18	17 16
GIO_P107[1:0]	GIO_P106[1:0]	GIO_P105[1:0]	GIO_P104[1:0]

15 14	13 12	11 10	9 8
GIO_P103[1:0]	GIO_P102[1:0]	GIO_P101[1:0]	GIO_P100[1:0]

7 6	5 4	3 2	1 0
GIO_P99[1:0]	GIO_P98[1:0]	GIO_P97[1:0]	GIO_P96[1:0]

Name	R/W	Bit	After Reset	Function
GIO_P111[1:0]	R/W	31:30	0	Switches the GIO_P111 pin functions.
GIO_P110[1:0]	R/W	29:28	0	Switches the GIO_P110 pin functions.
GIO_P109[1:0]	R/W	27:26	0	Switches the GIO_P109 pin functions.
GIO_P108[1:0]	R/W	25:24	0	Switches the GIO_P108 pin functions.
GIO_P107[1:0]	R/W	23:22	0	Switches the GIO_P107 pin functions.
GIO_P106[1:0]	R/W	21:20	0	Switches the GIO_P106 pin functions.
GIO_P105[1:0]	R/W	19:18	0	Switches the GIO_P105 pin functions.
GIO_P104[1:0]	R/W	17:16	0	Switches the GIO_P104 pin functions.
GIO_P103[1:0]	R/W	15:14	0	Switches the GIO_P103 pin functions.
GIO_P102[1:0]	R/W	13:12	0	Switches the GIO_P102 pin functions.
GIO_P101[1:0]	R/W	11:10	0	Switches the GIO_P101 pin functions.
GIO_P100[1:0]	R/W	9:8	0	Switches the GIO_P100 pin functions.
GIO_P99[1:0]	R/W	7:6	0	Switches the GIO_P99 pin functions.
GIO_P98[1:0]	R/W	5:4	0	Switches the GIO_P98 pin functions.
GIO_P97[1:0]	R/W	3:2	0	Switches the GIO_P97 pin functions.
GIO_P96[1:0]	R/W	1:0	0	Switches the GIO_P96 pin functions.

PINSEL_GIO_Pxx	2'b00	2'b01	2'b10	2'b11	Description
Pin Name	Default				
USB_CLK	GIO_P96	USB_CLK			
USB_DATA0	GIO_P97	USB_DATA0			
USB_DATA1	GIO_P98	USB_DATA1			
USB_DATA2	GIO_P99	USB_DATA2			
USB_DATA3	GIO_P100	USB_DATA3			
USB_DATA4	GIO_P101	USB_DATA4			
USB_DATA5	GIO_P102	USB_DATA5			
USB_DATA6	GIO_P103	USB_DATA6			
USB_DATA7	GIO_P104	USB_DATA7			
USB_DIR	GIO_P105	USB_DIR			
USB_STP	GIO_P106	USB_STP			
USB_NXT	GIO_P107	USB_NXT			
URT2_SRIN	GIO_P108	URT2_SRIN	NAND_ALE		
URT2_SOUT	GIO_P109	URT2_SOUT	NAND_CLE		
URT2_CTSB	GIO_P110	URT2_CTSB	NAND_D0		
URT2_RTSB	GIO_P111	URT2_RTSB	NAND_D1		

(15) GIO_P[117:112] pin alternate function switch register

This register (CHG_PINSEL_G112: C014_021C) switches the GIO_P[117:112] pin functions.

To change the setting of CHG_PINSEL_xx that alternately functions as GIO, change the setting basically by using GIO_Pxx.

When switching pins according to the function, note that some pins may also be used as GIO pins.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
GIO_P119[1:0]		GIO_P118[1:0]		GIO_P117[1:0]		GIO_P116[1:0]	

7	6	5	4	3	2	1	0
GIO_P115[1:0]		GIO_P114[1:0]		GIO_P113[1:0]		GIO_P112[1:0]	

Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	–	Reserved. When these bits are read, 0 is returned for each bit.
GIO_P119[1:0]	R/W	15:14	0	Switches the spare GIO_P119 pin functions.
GIO_P118[1:0]	R/W	13:12	0	Switches the spare GIO_P118 pin functions.
GIO_P117[1:0]	R/W	11:10	0	Switches the GIO_P117 pin functions.
GIO_P116[1:0]	R/W	9:8	0	Switches the GIO_P116 pin functions.
GIO_P115[1:0]	R/W	7:6	0	Switches the GIO_P115 pin functions.
GIO_P114[1:0]	R/W	5:4	0	Switches the GIO_P114 pin functions.
GIO_P113[1:0]	R/W	3:2	0	Switches the GIO_P113 pin functions.
GIO_P112[1:0]	R/W	1:0	0	Switches the GIO_P112 pin functions.

PINSEL_GIO_Pxx	2'b00	2'b01	2'b10	2'b11	Description
Pin Name	Default				
SD2_CKO	GIO_P112	SD2_CKO	NAND_D2		
SD2_CMD	GIO_P113	SD2_CMD	NAND_D3		
SD2_DATA0	GIO_P114	SD2_DATA0	NAND_D4		
SD2_DATA1	GIO_P115	SD2_DATA1	NAND_D5		
SD2_DATA2	GIO_P116	SD2_DATA2	NAND_D6		
SD2_DATA3	GIO_P117	SD2_DATA3	NAND_D7		

(16) SP0 pin alternate function switch register

This register (CHG_PINSEL_SP0: C014_0280) switches the SP0 pin functions.

Switch the SP0_CS1 and SP0_CS2 pins by using GIO_P48 and GIO_P49.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						PINSEL_SP0[1:0]	

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	–	Reserved. When these bits are read, 0 is returned for each bit.
PINSEL_SP0[1:0]	R/W	1:0	0	Switches the SP0 pin functions.

PINSEL_SP0	2'b00	2'b01	2'b10	2'b11	Description
Pin Name	Default	MWI			
SP0_CLK	SP0_CLK	MWI_SK			
SP0_SI	SP0_SI	MWI_SI			
SP0_SO	SP0_SO	MWI_SO			
SP0_CS0	SP0_CS0	MWI_CS			
SP0_CS1	GIO_P48	SP0_CS1			Switched by using GIO_P48
SP0_CS2	GIO_P49	SP0_CS2			Switched by using GIO_P49

(17) DTV pin alternate function switch register

This register (CHG_PINSEL_DTV: C014_0284H) switches the DTV pin functions.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						PINSEL_DTV[1:0]	

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	–	Reserved. When these bits are read, 0 is returned for each bit.
PINSEL_DTV[1:0]	R/W	1:0	0	Switches the DTV pin functions.

PINSEL_DTV	2'b00	2'b01	2'b10	2'b11	Description
Pin Name	Default	SP2			
DTV_BCLK	DTV_BCLK	SP2_CLK			
DTV_DATA	DTV_DATA	SP2_SI			
DTV_PSYNC	DTV_PSYNC	SP2_SO			
DTV_VLD	DTV_VLD	SP2_CS0			

(18) SD0 pin alternate function switch register

This register (CHG_PINSEL_SD0: C014_0288H) switches the SD0 pin functions.

Switch the SD0_DATA[3:1] and SD0_CKI pins by using GIO_P[91:88].

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						PINSEL_SD0[1:0]	

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	–	Reserved. When these bits are read, 0 is returned for each bit.
PINSEL_SD0[1:0]	R/W	1:0	0	Switches the SD0 pin functions.

PINSEL_SD0	2'b00	2'b01	2'b10	2'b11	Description
Pin Name	Default				
SD0_CKO	SD0_CKO				
SD0_CMD	SD0_CMD				
SD0_DATA0	SD0_DATA0				
SD0_DATA1	GIO_P88	SD0_DATA1			Switched by using GIO_P88
SD0_DATA2	GIO_P89	SD0_DATA2			Switched by using GIO_P89
SD0_DATA3	GIO_P90	SD0_DATA3			Switched by using GIO_P90
SD0_CKI	GIO_P91	SD0_CKI			Switched by using GIO_P91

(19) SD1 pin alternate function switch register

This register (CHG_PINSEL_SD1: C014_028CH) switches the SD1 pin functions.

Switch the SD1_CKI pin by using GIO_P92.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						PINSEL_SD1[1:0]	

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	–	Reserved. When these bits are read, 0 is returned for each bit.
PINSEL_SD1[1:0]	R/W	1:0	0	Switches the SD1 pin functions.

PINSEL_SD1	2'b00	2'b01	2'b10	2'b11	Description
Pin Name	Default		CAM		
SD1_CKO	SD1_CKO				
SD1_CMD	SD1_CMD		CAM_YUV5		
SD1_DATA0	SD1_DATA0		CAM_YUV6		
SD1_DATA1	SD1_DATA1		CAM_YUV7		
SD1_DATA2	SD1_DATA2		CAM_VS		
SD1_DATA3	SD1_DATA3		CAM_HS		
SD1_CKI	GIO_P92	SD1_CKI	CAM_CLKI		Switched by using GIO_P92

(20) IIC2 pin alternate function switch register

This register (CHG_PINSEL_IIC2: C014_0290H) switches the IIC2 pin functions.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						PINSEL_IIC2[1:0]	

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	–	Reserved. When these bits are read, 0 is returned for each bit.
PINSEL_IIC2[1:0]	R/W	1:0	0	Switches the IIC2 pin functions.

PINSEL_IIC2	2'b00	2'b01	2'b10	2'b11	Description
Pin Name	Default		NAND		
IIC2_SCL	IIC2_SCL		NAND_WE		
IIC2_SDA	IIC2_SDA		NAND_RB0		

(21) REFCLKO clock pin switch register

This register (CHG_PINSEL_REFCLKO: C014_0294H) switches the REFCLKO pin functions.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						PINSEL_REFCLKO[1:0]	

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	–	Reserved. When these bits are read, 0 is returned for each bit.
PINSEL_REFCLKO [1:0]	R/W	1:0	0	Switches the REFCLKO pin functions.

PINSEL_REFCLKO	2'b00	2'b01	2'b10	2'b11	Description
Pin Name	Default				
REFCLKO	OSC12M_OUT	PLL2OUT			Internal OSC and internal PLL2 are switched

(22) GIO_P[7:0] pin pull-up/pull-down/input enable control register

This register (CHG_PULL_G00: C014_0300H) selects pull-up or pull-down and enable inputs for the GIO_P[7:0] pins.

31	30	29	28	27	26	25	24
Reserved	GIO07_IE	GIO07_UPC	GIO07_POENB	Reserved	GIO06_IE	GIO06_UPC	GIO06_POENB
23	22	21	20	19	18	17	16
Reserved	GIO05_IE	GIO05_UPC	GIO05_POENB	Reserved	GIO04_IE	GIO04_UPC	GIO04_POENB
15	14	13	12	11	10	9	8
Reserved	GIO03_IE	GIO03_UPC	GIO03_POENB	Reserved	GIO02_IE	GIO02_UPC	GIO02_POENB
7	6	5	4	3	2	1	0
Reserved	GIO01_IE	GIO01_UPC	GIO01_POENB	Reserved	GIO00_IE	GIO00_UPC	GIO00_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
GIO07_IE	R/W	30	0	Specifies whether to enable inputting to the GIO_P7 pin. 0: Masks inputs. 1: Enables inputs.
GIO07_UPC	R/W	29	0	Specifies pull-up or pull-down of the GIO_P7 pin. 0: Pull down, 1: Pull up
GIO07_POENB	R/W	28	0	Specifies whether to enable pull-up or pull-down of the GIO_P7 pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
GIO06_IE	R/W	26	0	Specifies whether to enable inputting to the GIO_P6 pin. 0: Masks inputs. 1: Enables inputs.
GIO06_UPC	R/W	25	0	Specifies pull-up or pull-down of the GIO_P6 pin. 0: Pull down, 1: Pull up
GIO06_POENB	R/W	24	0	Specifies whether to enable pull-up or pull-down of the GIO_P6 pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
GIO05_IE	R/W	22	0	Specifies whether to enable inputting to the GIO_P5 pin. 0: Masks inputs. 1: Enables inputs.
GIO05_UPC	R/W	21	0	Specifies pull-up or pull-down of the GIO_P5 pin. 0: Pull down, 1: Pull up
GIO05_POENB	R/W	20	0	Specifies whether to enable pull-up or pull-down of the GIO_P5 pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
GIO04_IE	R/W	18	0	Specifies whether to enable inputting to the GIO_P4 pin. 0: Masks inputs. 1: Enables inputs.
GIO04_UPC	R/W	17	0	Specifies pull-up or pull-down of the GIO_P4 pin. 0: Pull down, 1: Pull up
GIO04_POENB	R/W	16	0	Specifies whether to enable pull-up or pull-down of the GIO_P4 pin. 0: Enable, 1: Disable

(2/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
GIO03_IE	R/W	14	0	Specifies whether to enable inputting to the GIO_P3 pin. 0: Masks inputs. 1: Enables inputs.
GIO03_UPC	R/W	13	0	Specifies pull-up or pull-down of the GIO_P3 pin. 0: Pull down, 1: Pull up
GIO03_POENB	R/W	12	0	Specifies whether to enable pull-up or pull-down of the GIO_P3 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
GIO02_IE	R/W	10	0	Specifies whether to enable inputting to the GIO_P2 pin. 0: Masks inputs. 1: Enables inputs.
GIO02_UPC	R/W	9	0	Specifies pull-up or pull-down of the GIO_P2 pin. 0: Pull down, 1: Pull up
GIO02_POENB	R/W	8	0	Specifies whether to enable pull-up or pull-down of the GIO_P2 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
GIO01_IE	R/W	6	0	Specifies whether to enable inputting to the GIO_P1 pin. 0: Masks inputs. 1: Enables inputs.
GIO01_UPC	R/W	5	0	Specifies pull-up or pull-down of the GIO_P1 pin. 0: Pull down, 1: Pull up
GIO01_POENB	R/W	4	0	Specifies whether to enable pull-up or pull-down of the GIO_P1 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
GIO00_IE	R/W	2	0	Specifies whether to enable inputting to the GIO_P0 pin. 0: Masks inputs. 1: Enables inputs.
GIO00_UPC	R/W	1	0	Specifies pull-up or pull-down of the GIO_P0 pin. 0: Pull down, 1: Pull up
GIO00_POENB	R/W	0	0	Specifies whether to enable pull-up or pull-down of the GIO_P0 pin. 0: Enable, 1: Disable

(23) GIO_P[15:8] pin pull-up/pull-down/input enable control register

This register (CHG_PULL_G08: C014_0304H) selects pull-up or pull-down and enable inputs for the GIO_P[15:8] pins.

31	30	29	28	27	26	25	24
Reserved	GIO15_IE	GIO15_UPC	GIO15_POENB	Reserved	GIO14_IE	GIO14_UPC	GIO14_POENB
23	22	21	20	19	18	17	16
Reserved	GIO13_IE	GIO13_UPC	GIO13_POENB	Reserved	GIO12_IE	GIO12_UPC	GIO12_POENB
15	14	13	12	11	10	9	8
Reserved	GIO11_IE	GIO11_UPC	GIO11_POENB	Reserved	GIO10_IE	GIO10_UPC	GIO10_POENB
7	6	5	4	3	2	1	0
Reserved	GIO09_IE	GIO09_UPC	GIO09_POENB	Reserved	GIO08_IE	GIO08_UPC	GIO08_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
GIO15_IE	R/W	30	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P15 pin. 0: Masks inputs. 1: Enables inputs.
GIO15_UPC	R/W	29	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P15 pin. 0: Pull down, 1: Pull up
GIO15_POENB	R/W	28	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P15 pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
GIO14_IE	R/W	26	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P14 pin. 0: Masks inputs. 1: Enables inputs.
GIO14_UPC	R/W	25	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P14 pin. 0: Pull down, 1: Pull up
GIO14_POENB	R/W	24	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P14 pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
GIO13_IE	R/W	22	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P13 pin. 0: Masks inputs. 1: Enables inputs.
GIO13_UPC	R/W	21	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P13 pin. 0: Pull down, 1: Pull up
GIO13_POENB	R/W	20	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P13 pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
GIO12_IE	R/W	18	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P12 pin. 0: Masks inputs. 1: Enables inputs.

Note The spare bits are provided in the register, but they do not indicate any hardware status.

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Name	R/W	Bit	After Reset	Function
GIO12_UPC	R/W	17	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P12 pin. 0: Pull down, 1: Pull up
GIO12_POENB	R/W	16	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P12 pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
GIO11_IE	R/W	14	0	Specifies whether to enable inputting to the GIO_P11 pin. 0: Masks inputs. 1: Enables inputs.
GIO11_UPC	R/W	13	0	Specifies pull-up or pull-down of the GIO_P11 pin. 0: Pull down, 1: Pull up
GIO11_POENB	R/W	12	0	Specifies whether to enable pull-up or pull-down of the GIO_P11 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
GIO10_IE	R/W	10	0	Specifies whether to enable inputting to the GIO_P10 pin. 0: Masks inputs. 1: Enables inputs.
GIO10_UPC	R/W	9	0	Specifies pull-up or pull-down of the GIO_P10 pin. 0: Pull down, 1: Pull up
GIO10_POENB	R/W	8	0	Specifies whether to enable pull-up or pull-down of the GIO_P10 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
GIO9_IE	R/W	6	0	Specifies whether to enable inputting to the GIO_P9 pin. 0: Masks inputs. 1: Enables inputs.
GIO9_UPC	R/W	5	0	Specifies pull-up or pull-down of the GIO_P9 pin. 0: Pull down, 1: Pull up
GIO9_POENB	R/W	4	0	Specifies whether to enable pull-up or pull-down of the GIO_P9 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
GIO8_IE	R/W	2	0	Specifies whether to enable inputting to the GIO_P8 pin. 0: Masks inputs. 1: Enables inputs.
GIO8_UPC	R/W	1	0	Specifies pull-up or pull-down of the GIO_P8 pin. 0: Pull down, 1: Pull up
GIO8_POENB	R/W	0	0	Specifies whether to enable pull-up or pull-down of the GIO_P8 pin. 0: Enable, 1: Disable

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(24) GIO_P[23:16] pin pull-up/pull-down/input enable control register

This register (CHG_PULL_G16: C014_0308H) selects pull-up or pull-down and enable inputs for the GIO_P[23:16] pins.

31	30	29	28	27	26	25	24
Reserved	GIO23_IE	GIO23_UPC	GIO23_POENB	Reserved	GIO22_IE	GIO22_UPC	GIO22_POENB
23	22	21	20	19	18	17	16
Reserved	GIO21_IE	GIO21_UPC	GIO21_POENB	Reserved	GIO20_IE	GIO20_UPC	GIO20_POENB
15	14	13	12	11	10	9	8
Reserved	GIO19_IE	GIO19_UPC	GIO19_POENB	Reserved	GIO18_IE	GIO18_UPC	GIO18_POENB
7	6	5	4	3	2	1	0
Reserved	GIO17_IE	GIO17_UPC	GIO17_POENB	Reserved	GIO16_IE	GIO16_UPC	GIO16_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
GIO23_IE	R/W	30	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P23 pin. 0: Masks inputs. 1: Enables inputs.
GIO23_UPC	R/W	29	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P23 pin. 0: Pull down, 1: Pull up
GIO23_POENB	R/W	28	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P23 pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
GIO22_IE	R/W	26	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P22 pin. 0: Masks inputs. 1: Enables inputs.
GIO22_UPC	R/W	25	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P22 pin. 0: Pull down, 1: Pull up
GIO22_POENB	R/W	24	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P22 pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
GIO21_IE	R/W	22	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P21 pin. 0: Masks inputs. 1: Enables inputs.
GIO21_UPC	R/W	21	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P21 pin. 0: Pull down, 1: Pull up
GIO21_POENB	R/W	20	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P21 pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.

Note The spare bits are provided in the register, but they do not indicate any hardware status.

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Name	R/W	Bit	After Reset	Function
GIO20_IE	R/W	18	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P20 pin. 0: Masks inputs. 1: Enables inputs.
GIO20_UPC	R/W	17	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P20 pin. 0: Pull down, 1: Pull up
GIO20_POENB	R/W	16	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P20 pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
GIO19_IE	R/W	14	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P19 pin. 0: Masks inputs. 1: Enables inputs.
GIO19_UPC	R/W	13	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P19 pin. 0: Pull down, 1: Pull up
GIO19_POENB	R/W	12	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P19 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
GIO18_IE	R/W	10	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P18 pin. 0: Masks inputs. 1: Enables inputs.
GIO18_UPC	R/W	9	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P18 pin. 0: Pull down, 1: Pull up
GIO18_POENB	R/W	8	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P18 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
GIO17_IE	R/W	6	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P17 pin. 0: Masks inputs. 1: Enables inputs.
GIO17_UPC	R/W	5	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P17 pin. 0: Pull down, 1: Pull up
GIO17_POENB	R/W	4	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P17 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
GIO16_IE	R/W	2	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P16 pin. 0: Masks inputs. 1: Enables inputs.
GIO16_UPC	R/W	1	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P16 pin. 0: Pull down, 1: Pull up
GIO16_POENB	R/W	0	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P16 pin. 0: Enable, 1: Disable

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(25) GIO_P[31:24] pin pull-up/pull-down/input enable control register

This register (CHG_PULL_G24: C014_030CH) selects pull-up or pull-down and enable inputs for the GIO_P[31:24] pins.

31	30	29	28	27	26	25	24
Reserved	GIO31_IE	GIO31_UPC	GIO31_POENB	Reserved	GIO30_IE	GIO30_UPC	GIO30_POENB
23	22	21	20	19	18	17	16
Reserved	GIO29_IE	GIO29_UPC	GIO29_POENB	Reserved	GIO28_IE	GIO28_UPC	GIO28_POENB
15	14	13	12	11	10	9	8
Reserved	GIO27_IE	GIO27_UPC	GIO27_POENB	Reserved	GIO26_IE	GIO26_UPC	GIO26_POENB
7	6	5	4	3	2	1	0
Reserved	GIO25_IE	GIO25_UPC	GIO25_POENB	Reserved	GIO24_IE	GIO24_UPC	GIO24_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
GIO31_IE	R/W	30	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO31 pin. 0: Masks inputs. 1: Enables inputs.
GIO31_UPC	R/W	29	0	Specifies pull-up or pull-down of the GIO_P31 pin. 0: Pull down, 1: Pull up
GIO31_POENB	R/W	28	0	Specifies whether to enable pull-up or pull-down of the GIO_P31 pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
GIO30_IE	R/W	26	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P30 pin. 0: Masks inputs. 1: Enables inputs.
GIO30_UPC	R/W	25	0	Specifies pull-up or pull-down of the GIO_P30 pin. 0: Pull down, 1: Pull up
GIO30_POENB	R/W	24	0	Specifies whether to enable pull-up or pull-down of the GIO_P30 pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
GIO29_IE	R/W	22	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P29 pin. 0: Masks inputs. 1: Enables inputs.
GIO29_UPC	R/W	21	0	Specifies pull-up or pull-down of the GIO_P29 pin. 0: Pull down, 1: Pull up
GIO29_POENB	R/W	20	0	Specifies whether to enable pull-up or pull-down of the GIO_P29 pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
GIO28_IE	R/W	18	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P28 pin. 0: Masks inputs. 1: Enables inputs.
GIO28_UPC	R/W	17	0	Specifies pull-up or pull-down of the GIO_P28 pin. 0: Pull down, 1: Pull up

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(2/2)

Name	R/W	Bit	After Reset	Function
GIO28_POENB	R/W	16	0	Specifies whether to enable pull-up or pull-down of the GIO_P28 pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
GIO27_IE	R/W	14	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P27 pin. 0: Masks inputs. 1: Enables inputs.
GIO27_UPC	R/W	13	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P27 pin. 0: Pull down, 1: Pull up
GIO27_POENB	R/W	12	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P27 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
GIO26_IE	R/W	10	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P26 pin. 0: Masks inputs. 1: Enables inputs.
GIO26_UPC	R/W	9	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P26 pin. 0: Pull down, 1: Pull up
GIO26_POENB	R/W	8	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P26 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
GIO25_IE	R/W	6	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P25 pin. 0: Masks inputs. 1: Enables inputs.
GIO25_UPC	R/W	5	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P25 pin. 0: Pull down, 1: Pull up
GIO25_POENB	R/W	4	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P25 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
GIO24_IE	R/W	2	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P24 pin. 0: Masks inputs. 1: Enables inputs.
GIO24_UPC	R/W	1	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P24 pin. 0: Pull down, 1: Pull up
GIO24_POENB	R/W	0	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P24 pin. 0: Enable, 1: Disable

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(26) GIO_P[39:32] pin pull-up/pull-down/input enable control register

This register (CHG_PULL_G32: C014_0310H) selects pull-up or pull-down and enable inputs for the GIO_P[39:32] pins.

31	30	29	28	27	26	25	24
Reserved	GIO39_IE	GIO39_UPC	GIO39_POENB	Reserved	GIO38_IE	GIO38_UPC	GIO38_POENB
23	22	21	20	19	18	17	16
Reserved	GIO37_IE	GIO37_UPC	GIO37_POENB	Reserved	GIO36_IE	GIO36_UPC	GIO36_POENB
15	14	13	12	11	10	9	8
Reserved	GIO35_IE	GIO35_UPC	GIO35_POENB	Reserved	GIO34_IE	GIO34_UPC	GIO34_POENB
7	6	5	4	3	2	1	0
Reserved	GIO33_IE	GIO33_UPC	GIO33_POENB	Reserved	GIO32_IE	GIO32_UPC	GIO32_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
GIO39_IE	R/W	30	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P39 pin. 0: Masks inputs. 1: Enables inputs.
GIO39_UPC	R/W	29	0	Specifies pull-up or pull-down of the GIO_P39 pin. 0: Pull down, 1: Pull up
GIO39_POENB	R/W	28	0	Specifies whether to enable pull-up or pull-down of the GIO_P39 pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
GIO38_IE	R/W	26	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P38 pin. 0: Masks inputs. 1: Enables inputs.
GIO38_UPC	R/W	25	0	Specifies pull-up or pull-down of the GIO_P38 pin. 0: Pull down, 1: Pull up
GIO38_POENB	R/W	24	0	Specifies whether to enable pull-up or pull-down of the GIO_P38 pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
GIO37_IE	R/W	22	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P37 pin. 0: Masks inputs. 1: Enables inputs.
GIO37_UPC	R/W	21	0	Specifies pull-up or pull-down of the GIO_P37 pin. 0: Pull down, 1: Pull up
GIO37_POENB	R/W	20	0	Specifies whether to enable pull-up or pull-down of the GIO_P37 pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
GIO36_IE	R/W	18	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P36 pin. 0: Masks inputs. 1: Enables inputs.
GIO36_UPC	R/W	17	0	Specifies pull-up or pull-down of the GIO_P36 pin. 0: Pull down, 1: Pull up

Note The spare bits are provided in the register, but they do not indicate any hardware status.

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Name	R/W	Bit	After Reset	Function
GIO36_POENB	R/W	16	0	Specifies whether to enable pull-up or pull-down of the GIO_P36 pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
GIO35_IE	R/W	14	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P35 pin. 0: Masks inputs. 1: Enables inputs.
GIO35_UPC	R/W	13	0	Specifies pull-up or pull-down of the GIO_P35 pin. 0: Pull down, 1: Pull up
GIO35_POENB	R/W	12	0	Specifies whether to enable pull-up or pull-down of the GIO_P35 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
GIO34_IE	R/W	10	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P34 pin. 0: Masks inputs. 1: Enables inputs.
GIO34_UPC	R/W	9	0	Specifies pull-up or pull-down of the GIO_P34 pin. 0: Pull down, 1: Pull up
GIO34_POENB	R/W	8	0	Specifies whether to enable pull-up or pull-down of the GIO_P34 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
GIO33_IE	R/W	6	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P33 pin. 0: Masks inputs. 1: Enables inputs.
GIO33_UPC	R/W	5	0	Specifies pull-up or pull-down of the GIO_P33 pin. 0: Pull down, 1: Pull up
GIO33_POENB	R/W	4	0	Specifies whether to enable pull-up or pull-down of the GIO_P33 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
GIO32_IE	R/W	2	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P32 pin. 0: Masks inputs. 1: Enables inputs.
GIO32_UPC	R/W	1	0	Specifies pull-up or pull-down of the GIO_P32 pin. 0: Pull down, 1: Pull up
GIO32_POENB	R/W	0	0	Specifies whether to enable pull-up or pull-down of the GIO_P32 pin. 0: Enable, 1: Disable

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(27) GIO_P[47:40] pin pull-up/pull-down/input enable control register

This register (CHG_PULL_G40: C014_0314H) selects pull-up or pull-down and enable inputs for the GIO_P[47:40] pins.

31	30	29	28	27	26	25	24
Reserved	GIO47_IE	GIO47_UPC	GIO47_POENB	Reserved	GIO46_IE	GIO46_UPC	GIO46_POENB
23	22	21	20	19	18	17	16
Reserved	GIO45_IE	GIO45_UPC	GIO45_POENB	Reserved	GIO44_IE	GIO44_UPC	GIO44_POENB
15	14	13	12	11	10	9	8
Reserved	GIO43_IE	GIO43_UPC	GIO43_POENB	Reserved	GIO42_IE	GIO42_UPC	GIO42_POENB
7	6	5	4	3	2	1	0
Reserved	GIO41_IE	GIO41_UPC	GIO41_POENB	Reserved	GIO40_IE	GIO40_UPC	GIO40_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
GIO47_IE	R/W	30	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P47 pin. 0: Masks inputs. 1: Enables inputs.
GIO47_UPC	R/W	29	0	Specifies pull-up or pull-down of the GIO_P47 pin. 0: Pull down, 1: Pull up
GIO47_POENB	R/W	28	0	Specifies whether to enable pull-up or pull-down of the GIO_P47 pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
GIO46_IE	R/W	26	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P46 pin. 0: Masks inputs. 1: Enables inputs.
GIO46_UPC	R/W	25	0	Specifies pull-up or pull-down of the GIO_P46 pin. 0: Pull down, 1: Pull up
GIO46_POENB	R/W	24	0	Specifies whether to enable pull-up or pull-down of the GIO_P46 pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
GIO45_IE	R/W	22	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P45 pin. 0: Masks inputs. 1: Enables inputs.
GIO45_UPC	R/W	21	0	Specifies pull-up or pull-down of the GIO_P45 pin. 0: Pull down, 1: Pull up
GIO45_POENB	R/W	20	0	Specifies whether to enable pull-up or pull-down of the GIO_P45 pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
GIO44_IE	R/W	18	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P44 pin. 0: Masks inputs. 1: Enables inputs.
GIO44_UPC	R/W	17	0	Specifies pull-up or pull-down of the GIO_P44 pin. 0: Pull down, 1: Pull up

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(2/2)

Name	R/W	Bit	After Reset	Function
GIO44_POENB	R/W	16	0	Specifies whether to enable pull-up or pull-down of the GIO_P44 pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
GIO43_IE	R/W	14	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P43 pin. 0: Masks inputs. 1: Enables inputs.
GIO43_UPC	R/W	13	1	Specifies pull-up or pull-down of the GIO_P43 pin. 0: Pull down, 1: Pull up
GIO43_POENB	R/W	12	0	Specifies whether to enable pull-up or pull-down of the GIO_P43 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
GIO42_IE	R/W	10	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P42 pin. 0: Masks inputs. 1: Enables inputs.
GIO42_UPC	R/W	9	1	Specifies pull-up or pull-down of the GIO_P42 pin. 0: Pull down, 1: Pull up
GIO42_POENB	R/W	8	0	Specifies whether to enable pull-up or pull-down of the GIO_P42 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
GIO41_IE	R/W	6	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P41 pin. 0: Masks inputs. 1: Enables inputs.
GIO41_UPC	R/W	5	0	Specifies pull-up or pull-down of the GIO_P41 pin. 0: Pull down, 1: Pull up
GIO41_POENB	R/W	4	0	Specifies whether to enable pull-up or pull-down of the GIO_P41 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
GIO40_IE	R/W	2	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P40 pin. 0: Masks inputs. 1: Enables inputs.
GIO40_UPC	R/W	1	0	Specifies pull-up or pull-down of the GIO_P40 pin. 0: Pull down, 1: Pull up
GIO40_POENB	R/W	0	0	Specifies whether to enable pull-up or pull-down of the GIO_P40 pin. 0: Enable, 1: Disable

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(28) GIO_P[55:48] pin pull-up/pull-down/input enable control register

This register (CHG_PULL_G48: C014_0318H) selects pull-up or pull-down and enable inputs for the GIO_P[55:48] pins.

31	30	29	28	27	26	25	24
Reserved	GIO55_IE	GIO55_UPC	GIO55_POENB	Reserved	GIO54_IE	GIO54_UPC	GIO54_POENB
23	22	21	20	19	18	17	16
Reserved	GIO53_IE	GIO53_UPC	GIO53_POENB	Reserved	GIO52_IE	GIO52_UPC	GIO52_POENB
15	14	13	12	11	10	9	8
Reserved	GIO51_IE	GIO51_UPC	GIO51_POENB	Reserved	GIO50_IE	GIO50_UPC	GIO50_POENB
7	6	5	4	3	2	1	0
Reserved	GIO49_IE	GIO49_UPC	GIO49_POENB	Reserved	GIO48_IE	GIO48_UPC	GIO48_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
GIO55_IE	R/W	30	0	Specifies whether to enable inputting to the GIO_P55 pin. 0: Masks inputs. 1: Enables inputs.
GIO55_UPC	R/W	29	0	Specifies pull-up or pull-down of the GIO_P55 pin. 0: Pull down, 1: Pull up
GIO55_POENB	R/W	28	1	Specifies whether to enable pull-up or pull-down of the GIO_P55 pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
GIO54_IE	R/W	26	0	Specifies whether to enable inputting to the GIO_P54 pin. 0: Masks inputs. 1: Enables inputs.
GIO54_UPC	R/W	25	0	Specifies pull-up or pull-down of the GIO_P54 pin. 0: Pull down, 1: Pull up
GIO54_POENB	R/W	24	1	Specifies whether to enable pull-up or pull-down of the GIO_P54 pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
GIO53_IE	R/W	22	0	Specifies whether to enable inputting to the GIO_P53 pin. 0: Masks inputs. 1: Enables inputs.
GIO53_UPC	R/W	21	0	Specifies pull-up or pull-down of the GIO_P53 pin. 0: Pull down, 1: Pull up
GIO53_POENB	R/W	20	1	Specifies whether to enable pull-up or pull-down of the GIO_P53 pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
GIO52_IE	R/W	18	0	Specifies whether to enable inputting to the GIO_P52 pin. 0: Masks inputs. 1: Enables inputs.
GIO52_UPC	R/W	17	0	Specifies pull-up or pull-down of the GIO_P52 pin. 0: Pull down, 1: Pull up

(2/2)

Name	R/W	Bit	After Reset	Function
GIO52_POENB	R/W	16	1	Specifies whether to enable pull-up or pull-down of the GIO_P52 pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
GIO51_IE	R/W	14	0	Specifies whether to enable inputting to the GIO_P51 pin. 0: Masks inputs. 1: Enables inputs.
GIO51_UPC	R/W	13	0	Specifies pull-up or pull-down of the GIO_P51 pin. 0: Pull down, 1: Pull up
GIO51_POENB	R/W	12	1	Specifies whether to enable pull-up or pull-down of the GIO_P51 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
GIO50_IE	R/W	10	0	Specifies whether to enable inputting to the GIO_P50 pin. 0: Masks inputs. 1: Enables inputs.
GIO50_UPC	R/W	9	0	Specifies pull-up or pull-down of the GIO_P50 pin. 0: Pull down, 1: Pull up
GIO50_POENB	R/W	8	1	Specifies whether to enable pull-up or pull-down of the GIO_P50 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
GIO49_IE	R/W	6	0	Specifies whether to enable inputting to the GIO_P49 pin. 0: Masks inputs. 1: Enables inputs.
GIO49_UPC	R/W	5	0	Specifies pull-up or pull-down of the GIO_P49 pin. 0: Pull down, 1: Pull up
GIO49_POENB	R/W	4	1	Specifies whether to enable pull-up or pull-down of the GIO_P49 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
GIO48_IE	R/W	2	0	Specifies whether to enable inputting to the GIO_P48 pin. 0: Masks inputs. 1: Enables inputs.
GIO48_UPC	R/W	1	0	Specifies pull-up or pull-down of the GIO_P48 pin. 0: Pull down, 1: Pull up
GIO48_POENB	R/W	0	1	Specifies whether to enable pull-up or pull-down of the GIO_P48 pin. 0: Enable, 1: Disable

(29) GIO_P[63:56] pin pull-up/pull-down/input enable control register

This register (CHG_PULL_G56: C014_031CH) selects pull-up or pull-down and enable inputs for the GIO_P[63:56] pins.

31	30	29	28	27	26	25	24
Reserved	GIO63_IE	GIO63_UPC	GIO63_POENB	Reserved	GIO62_IE	GIO62_UPC	GIO62_POENB
23	22	21	20	19	18	17	16
Reserved	GIO61_IE	GIO61_UPC	GIO61_POENB	Reserved	GIO60_IE	GIO60_UPC	GIO60_POENB
15	14	13	12	11	10	9	8
Reserved	GIO59_IE	GIO59_UPC	GIO59_POENB	Reserved	GIO58_IE	GIO58_UPC	GIO58_POENB
7	6	5	4	3	2	1	0
Reserved	GIO57_IE	GIO57_UPC	GIO57_POENB	Reserved	GIO56_IE	GIO56_UPC	GIO56_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
GIO63_IE	R/W	30	0	Specifies whether to enable inputting to the GIO_P63 pin. 0: Masks inputs. 1: Enables inputs.
GIO63_UPC	R/W	29	0	Specifies pull-up or pull-down of the GIO_P63 pin. 0: Pull down, 1: Pull up
GIO63_POENB	R/W	28	1	Specifies whether to enable pull-up or pull-down of the GIO_P63 pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
GIO62_IE	R/W	26	0	Specifies whether to enable inputting to the GIO_P62 pin. 0: Masks inputs. 1: Enables inputs.
GIO62_UPC	R/W	25	0	Specifies pull-up or pull-down of the GIO_P62 pin. 0: Pull down, 1: Pull up
GIO62_POENB	R/W	24	1	Specifies whether to enable pull-up or pull-down of the GIO_P62 pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
GIO61_IE	R/W	22	0	Specifies whether to enable inputting to the GIO_P61 pin. 0: Masks inputs. 1: Enables inputs.
GIO61_UPC	R/W	21	0	Specifies pull-up or pull-down of the GIO_P61 pin. 0: Pull down, 1: Pull up
GIO61_POENB	R/W	20	1	Specifies whether to enable pull-up or pull-down of the GIO_P61 pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
GIO60_IE	R/W	18	0	Specifies whether to enable inputting to the GIO_P60 pin. 0: Masks inputs. 1: Enables inputs.
GIO60_UPC	R/W	17	0	Specifies pull-up or pull-down of the GIO_P60 pin. 0: Pull down, 1: Pull up

(2/2)

Name	R/W	Bit	After Reset	Function
GIO60_POENB	R/W	16	1	Specifies whether to enable pull-up or pull-down of the GIO_P60 pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
GIO59_IE	R/W	14	0	Specifies whether to enable inputting to the GIO_P59 pin. 0: Masks inputs. 1: Enables inputs.
GIO59_UPC	R/W	13	0	Specifies pull-up or pull-down of the GIO_P59 pin. 0: Pull down, 1: Pull up
GIO59_POENB	R/W	12	1	Specifies whether to enable pull-up or pull-down of the GIO_P59 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
GIO58_IE	R/W	10	0	Specifies whether to enable inputting to the GIO_P58 pin. 0: Masks inputs. 1: Enables inputs.
GIO58_UPC	R/W	9	0	Specifies pull-up or pull-down of the GIO_P58 pin. 0: Pull down, 1: Pull up
GIO58_POENB	R/W	8	1	Specifies whether to enable pull-up or pull-down of the GIO_P58 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
GIO57_IE	R/W	6	0	Specifies whether to enable inputting to the GIO_P57 pin. 0: Masks inputs. 1: Enables inputs.
GIO57_UPC	R/W	5	0	Specifies pull-up or pull-down of the GIO_P57 pin. 0: Pull down, 1: Pull up
GIO57_POENB	R/W	4	1	Specifies whether to enable pull-up or pull-down of the GIO_P57 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
GIO56_IE	R/W	2	0	Specifies whether to enable inputting to the GIO_P56 pin. 0: Masks inputs. 1: Enables inputs.
GIO56_UPC	R/W	1	0	Specifies pull-up or pull-down of the GIO_P56 pin. 0: Pull down, 1: Pull up
GIO56_POENB	R/W	0	1	Specifies whether to enable pull-up or pull-down of the GIO_P56 pin. 0: Enable, 1: Disable

(30) GIO_P[71:64] pin pull-up/pull-down/input enable control register

This register (CHG_PULL_G64: C014_0320H) selects pull-up or pull-down and enable inputs for the GIO_P[71:64] pins.

31	30	29	28	27	26	25	24
Reserved	GIO71_IE	GIO71_UPC	GIO71_POENB	Reserved	GIO70_IE	GIO70_UPC	GIO70_POENB
23	22	21	20	19	18	17	16
Reserved	GIO69_IE	GIO69_UPC	GIO69_POENB	Reserved	GIO68_IE	GIO68_UPC	GIO68_POENB
15	14	13	12	11	10	9	8
Reserved	GIO67_IE	GIO67_UPC	GIO67_POENB	Reserved	GIO66_IE	GIO66_UPC	GIO66_POENB
7	6	5	4	3	2	1	0
Reserved	GIO65_IE	GIO65_UPC	GIO65_POENB	Reserved	GIO64_IE	GIO64_UPC	GIO64_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
GIO71_IE	R/W	30	0	Specifies whether to enable inputting to the GIO_P71 pin. 0: Masks inputs. 1: Enables inputs.
GIO71_UPC	R/W	29	0	Specifies pull-up or pull-down of the GIO_P71 pin. 0: Pull down, 1: Pull up
GIO71_POENB	R/W	28	1	Specifies whether to enable pull-up or pull-down of the GIO_P71 pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
GIO70_IE	R/W	26	0	Specifies whether to enable inputting to the GIO_P70 pin. 0: Masks inputs. 1: Enables inputs.
GIO70_UPC	R/W	25	0	Specifies pull-up or pull-down of the GIO_P70 pin. 0: Pull down, 1: Pull up
GIO70_POENB	R/W	24	1	Specifies whether to enable pull-up or pull-down of the GIO_P70 pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
GIO69_IE	R/W	22	0	Specifies whether to enable inputting to the GIO_P69 pin. 0: Masks inputs. 1: Enables inputs.
GIO69_UPC	R/W	21	0	Specifies pull-up or pull-down of the GIO_P69 pin. 0: Pull down, 1: Pull up
GIO69_POENB	R/W	20	1	Specifies whether to enable pull-up or pull-down of the GIO_P69 pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
GIO68_IE	R/W	18	0	Specifies whether to enable inputting to the GIO_P68 pin. 0: Masks inputs. 1: Enables inputs.
GIO68_UPC	R/W	17	0	Specifies pull-up or pull-down of the GIO_P68 pin. 0: Pull down, 1: Pull up

(2/2)

Name	R/W	Bit	After Reset	Function
GIO68_POENB	R/W	16	1	Specifies whether to enable pull-up or pull-down of the GIO_P68 pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
GIO67_IE	R/W	14	0	Specifies whether to enable inputting to the GIO_P67 pin. 0: Masks inputs. 1: Enables inputs.
GIO67_UPC	R/W	13	0	Specifies pull-up or pull-down of the GIO_P67 pin. 0: Pull down, 1: Pull up
GIO67_POENB	R/W	12	1	Specifies whether to enable pull-up or pull-down of the GIO_P67 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
GIO66_IE	R/W	10	0	Specifies whether to enable inputting to the GIO_P66 pin. 0: Masks inputs. 1: Enables inputs.
GIO66_UPC	R/W	9	0	Specifies pull-up or pull-down of the GIO_P66 pin. 0: Pull down, 1: Pull up
GIO66_POENB	R/W	8	1	Specifies whether to enable pull-up or pull-down of the GIO_P66 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
GIO65_IE	R/W	6	0	Specifies whether to enable inputting to the GIO_P65 pin. 0: Masks inputs. 1: Enables inputs.
GIO65_UPC	R/W	5	0	Specifies pull-up or pull-down of the GIO_P65 pin. 0: Pull down, 1: Pull up
GIO65_POENB	R/W	4	1	Specifies whether to enable pull-up or pull-down of the GIO_P65 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
GIO64_IE	R/W	2	0	Specifies whether to enable inputting to the GIO_P64 pin. 0: Masks inputs. 1: Enables inputs.
GIO64_UPC	R/W	1	0	Specifies pull-up or pull-down of the GIO_P64 pin. 0: Pull down, 1: Pull up
GIO64_POENB	R/W	0	1	Specifies whether to enable pull-up or pull-down of the GIO_P64 pin. 0: Enable, 1: Disable

(31) GIO_P[79:72] pin pull-up/pull-down/input enable control register

This register (CHG_PULL_G72: C014_0324H) selects pull-up or pull-down and enable inputs for the GIO_P[79:72] pins.

31	30	29	28	27	26	25	24
Reserved	GIO79_IE	GIO79_UPC	GIO79_POENB	Reserved	GIO78_IE	GIO78_UPC	GIO78_POENB
23	22	21	20	19	18	17	16
Reserved	GIO77_IE	GIO77_UPC	GIO77_POENB	Reserved	GIO76_IE	GIO76_UPC	GIO76_POENB
15	14	13	12	11	10	9	8
Reserved	GIO75_IE	GIO75_UPC	GIO75_POENB	Reserved	GIO74_IE	GIO74_UPC	GIO74_POENB
7	6	5	4	3	2	1	0
Reserved	GIO73_IE	GIO73_UPC	GIO73_POENB	Reserved	GIO72_IE	GIO72_UPC	GIO72_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
GIO79_IE	R/W	30	0	Specifies whether to enable inputting to the GIO_P79 pin. 0: Masks inputs. 1: Enables inputs.
GIO79_UPC	R/W	29	0	Specifies pull-up or pull-down of the GIO_P79 pin. 0: Pull down, 1: Pull up
GIO79_POENB	R/W	28	0	Specifies whether to enable pull-up or pull-down of the GIO_P79 pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
GIO78_IE	R/W	26	0	Specifies whether to enable inputting to the GIO_P78 pin. 0: Masks inputs. 1: Enables inputs.
GIO78_UPC	R/W	25	0	Specifies pull-up or pull-down of the GIO_P78 pin. 0: Pull down, 1: Pull up
GIO78_POENB	R/W	24	0	Specifies whether to enable pull-up or pull-down of the GIO_P78 pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
GIO77_IE	R/W	22	0	Specifies whether to enable inputting to the GIO_P77 pin. 0: Masks inputs. 1: Enables inputs.
GIO77_UPC	R/W	21	0	Specifies pull-up or pull-down of the GIO_P77 pin. 0: Pull down, 1: Pull up
GIO77_POENB	R/W	20	0	Specifies whether to enable pull-up or pull-down of the GIO_P77 pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
GIO76_IE	R/W	18	0	Specifies whether to enable inputting to the GIO_P76 pin. 0: Masks inputs. 1: Enables inputs.
GIO76_UPC	R/W	17	0	Specifies pull-up or pull-down of the GIO_P76 pin. 0: Pull down, 1: Pull up

(2/2)

Name	R/W	Bit	After Reset	Function
GIO76_POENB	R/W	16	0	Specifies whether to enable pull-up or pull-down of the GIO_P76 pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
GIO75_IE	R/W	14	0	Specifies whether to enable inputting to the GIO_P75 pin. 0: Masks inputs. 1: Enables inputs.
GIO75_UPC	R/W	13	0	Specifies pull-up or pull-down of the GIO_P75 pin. 0: Pull down, 1: Pull up
GIO75_POENB	R/W	12	0	Specifies whether to enable pull-up or pull-down of the GIO_P75 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
GIO74_IE	R/W	10	0	Specifies whether to enable inputting to the GIO_P74 pin. 0: Masks inputs. 1: Enables inputs.
GIO74_UPC	R/W	9	0	Specifies pull-up or pull-down of the GIO_P74 pin. 0: Pull down, 1: Pull up
GIO74_POENB	R/W	8	0	Specifies whether to enable pull-up or pull-down of the GIO_P74 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
GIO73_IE	R/W	6	0	Specifies whether to enable inputting to the GIO_P73 pin. 0: Masks inputs. 1: Enables inputs.
GIO73_UPC	R/W	5	0	Specifies pull-up or pull-down of the GIO_P73 pin. 0: Pull down, 1: Pull up
GIO73_POENB	R/W	4	0	Specifies whether to enable pull-up or pull-down of the GIO_P73 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
GIO72_IE	R/W	2	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P72 pin. 0: Masks inputs. 1: Enables inputs.
GIO72_UPC	R/W	1	0	Specifies pull-up or pull-down of the GIO_P72 pin. 0: Pull down, 1: Pull up
GIO72_POENB	R/W	0	0	Specifies whether to enable pull-up or pull-down of the GIO_P72 pin. 0: Enable, 1: Disable

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(32) GIO_P[87:80] pin pull-up/pull-down/input enable control register

This register (CHG_PULL_G80: C014_0328H) selects pull-up or pull-down and enable inputs for the GIO_P[87:80] pins.

31	30	29	28	27	26	25	24
Reserved	GIO87_IE	GIO87_UPC	GIO87_POENB	Reserved	GIO86_IE	GIO86_UPC	GIO86_POENB
23	22	21	20	19	18	17	16
Reserved	GIO85_IE	GIO85_UPC	GIO85_POENB	Reserved	GIO84_IE	GIO84_UPC	GIO84_POENB
15	14	13	12	11	10	9	8
Reserved	GIO83_IE	GIO83_UPC	GIO83_POENB	Reserved	GIO82_IE	GIO82_UPC	GIO82_POENB
7	6	5	4	3	2	1	0
Reserved	GIO81_IE	GIO81_UPC	GIO81_POENB	Reserved	GIO80_IE	GIO80_UPC	GIO80_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
GIO87_IE	R/W	30	0	Specifies whether to enable inputting to the GIO_P87 pin. 0: Masks inputs. 1: Enables inputs.
GIO87_UPC	R/W	29	0	Specifies pull-up or pull-down of the GIO_P87 pin. 0: Pull down, 1: Pull up
GIO87_POENB	R/W	28	0	Specifies whether to enable pull-up or pull-down of the GIO_P87 pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
GIO86_IE	R/W	26	0	Specifies whether to enable inputting to the GIO_P86 pin. 0: Masks inputs. 1: Enables inputs.
GIO86_UPC	R/W	25	0	Specifies pull-up or pull-down of the GIO_P86 pin. 0: Pull down, 1: Pull up
GIO86_POENB	R/W	24	0	Specifies whether to enable pull-up or pull-down of the GIO_P86 pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
GIO85_IE	R/W	22	0	Specifies whether to enable inputting to the GIO_P85 pin. 0: Masks inputs. 1: Enables inputs.
GIO85_UPC	R/W	21	0	Specifies pull-up or pull-down of the GIO_P85 pin. 0: Pull down, 1: Pull up
GIO85_POENB	R/W	20	0	Specifies whether to enable pull-up or pull-down of the GIO_P85 pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
GIO84_IE	R/W	18	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P84 pin. 0: Masks inputs. 1: Enables inputs.
GIO84_UPC	R/W	17	0	Specifies pull-up or pull-down of the GIO_P84 pin. 0: Pull down, 1: Pull up

Note The spare bits are provided in the register, but they do not indicate any hardware status.

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Name	R/W	Bit	After Reset	Function
GIO84_POENB	R/W	16	0	Specifies whether to enable pull-up or pull-down of the GIO_P84 pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
GIO83_IE	R/W	14	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P83 pin. 0: Masks inputs. 1: Enables inputs.
GIO83_UPC	R/W	13	0	Specifies pull-up or pull-down of the GIO_P83 pin. 0: Pull down, 1: Pull up
GIO83_POENB	R/W	12	0	Specifies whether to enable pull-up or pull-down of the GIO_P83 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
GIO82_IE	R/W	10	0	Specifies whether to enable inputting to the GIO_P82 pin. 0: Masks inputs. 1: Enables inputs.
GIO82_UPC	R/W	9	0	Specifies pull-up or pull-down of the GIO_P82 pin. 0: Pull down, 1: Pull up
GIO82_POENB	R/W	8	0	Specifies whether to enable pull-up or pull-down of the GIO_P82 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
GIO81_IE	R/W	6	0	Specifies whether to enable inputting to the GIO_P81 pin. 0: Masks inputs. 1: Enables inputs.
GIO81_UPC	R/W	5	0	Specifies pull-up or pull-down of the GIO_P81 pin. 0: Pull down, 1: Pull up
GIO81_POENB	R/W	4	0	Specifies whether to enable pull-up or pull-down of the GIO_P81 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
GIO80_IE	R/W	2	0	Specifies whether to enable inputting to the GIO_P80 pin. 0: Masks inputs. 1: Enables inputs.
GIO80_UPC	R/W	1	0	Specifies pull-up or pull-down of the GIO_P80 pin. 0: Pull down, 1: Pull up
GIO80_POENB	R/W	0	0	Specifies whether to enable pull-up or pull-down of the GIO_P80 pin. 0: Enable, 1: Disable

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(33) GIO_P[95:88] pin pull-up/pull-down/input enable control register

This register (CHG_PULL_G88: C014_032CH) selects pull-up or pull-down and enable inputs for the GIO_P[95:88] pins.

31	30	29	28	27	26	25	24
Reserved	GIO95_IE	GIO95_UPC	GIO95_POENB	Reserved	GIO94_IE	GIO94_UPC	GIO94_POENB
23	22	21	20	19	18	17	16
Reserved	GIO93_IE	GIO93_UPC	GIO93_POENB	Reserved	GIO92_IE	GIO92_UPC	GIO92_POENB
15	14	13	12	11	10	9	8
Reserved	GIO91_IE	GIO91_UPC	GIO91_POENB	Reserved	GIO90_IE	GIO90_UPC	GIO90_POENB
7	6	5	4	3	2	1	0
Reserved	GIO89_IE	GIO89_UPC	GIO89_POENB	Reserved	GIO88_IE	GIO88_UPC	GIO88_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
GIO95_IE	R/W	30	0	Specifies whether to enable inputting to the GIO_P95 pin. 0: Masks inputs. 1: Enables inputs.
GIO95_UPC	R/W	29	0	Specifies pull-up or pull-down of the GIO_P95 pin. 0: Pull down, 1: Pull up
GIO95_POENB	R/W	28	0	Specifies whether to enable pull-up or pull-down of the GIO_P95 pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
GIO94_IE	R/W	26	0	Specifies whether to enable inputting to the GIO_P94 pin. 0: Masks inputs. 1: Enables inputs.
GIO94_UPC	R/W	25	0	Specifies pull-up or pull-down of the GIO_P94 pin. 0: Pull down, 1: Pull up
GIO94_POENB	R/W	24	0	Specifies whether to enable pull-up or pull-down of the GIO_P94 pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
GIO93_IE	R/W	22	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P93 pin. 0: Masks inputs. 1: Enables inputs.
GIO93_UPC	R/W	21	0	Specifies pull-up or pull-down of the GIO_P93 pin. 0: Pull down, 1: Pull up
GIO93_POENB	R/W	20	0	Specifies whether to enable pull-up or pull-down of the GIO_P93 pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
GIO92_IE	R/W	18	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P92 pin. 0: Masks inputs. 1: Enables inputs.
GIO92_UPC	R/W	17	0	Specifies pull-up or pull-down of the GIO_P92 pin. 0: Pull down, 1: Pull up

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(2/2)

Name	R/W	Bit	After Reset	Function
GIO92_POENB	R/W	16	0	Specifies whether to enable pull-up or pull-down of the GIO_P92 pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
GIO91_IE	R/W	14	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P91 pin. 0: Masks inputs. 1: Enables inputs.
GIO91_UPC	R/W	13	0	Specifies pull-up or pull-down of the GIO_P91 pin. 0: Pull down, 1: Pull up
GIO91_POENB	R/W	12	0	Specifies whether to enable pull-up or pull-down of the GIO_P91 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
GIO90_IE	R/W	10	0	Specifies whether to enable inputting to the GIO_P90 pin. 0: Masks inputs. 1: Enables inputs.
GIO90_UPC	R/W	9	0	Specifies pull-up or pull-down of the GIO_P90 pin. 0: Pull down, 1: Pull up
GIO90_POENB	R/W	8	0	Specifies whether to enable pull-up or pull-down of the GIO_P90 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
GIO89_IE	R/W	6	0	Specifies whether to enable inputting to the GIO_P89 pin. 0: Masks inputs. 1: Enables inputs.
GIO89_UPC	R/W	5	0	Specifies pull-up or pull-down of the GIO_P89 pin. 0: Pull down, 1: Pull up
GIO89_POENB	R/W	4	0	Specifies whether to enable pull-up or pull-down of the GIO_P89 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
GIO88_IE	R/W	2	0	Specifies whether to enable inputting to the GIO_P88 pin. 0: Masks inputs. 1: Enables inputs.
GIO88_UPC	R/W	1	0	Specifies pull-up or pull-down of the GIO_P88 pin. 0: Pull down, 1: Pull up
GIO88_POENB	R/W	0	0	Specifies whether to enable pull-up or pull-down of the GIO_P88 pin. 0: Enable, 1: Disable

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(34) GIO_P[103:96] pin pull-up/pull-down/input enable control register

This register (CHG_PULL_G96: C014_0330H) selects pull-up or pull-down and enable inputs for the GIO_P[103:96] pins.

31	30	29	28	27	26	25	24
Reserved	GIO103_IE	GIO103_UPC	GIO103_POENB	Reserved	GIO102_IE	GIO102_UPC	GIO102_POENB
23	22	21	20	19	18	17	16
Reserved	GIO101_IE	GIO101_UPC	GIO101_POENB	Reserved	GIO100_IE	GIO100_UPC	GIO100_POENB
15	14	13	12	11	10	9	8
Reserved	GIO99_IE	GIO99_UPC	GIO99_POENB	Reserved	GIO98_IE	GIO98_UPC	GIO98_POENB
7	6	5	4	3	2	1	0
Reserved	GIO97_IE	GIO97_UPC	GIO97_POENB	Reserved	GIO96_IE	GIO96_UPC	GIO96_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
GIO103_IE	R/W	30	0	Specifies whether to enable inputting to the GIO_P103 pin. 0: Masks inputs. 1: Enables inputs.
GIO103_UPC	R/W	29	0	Specifies pull-up or pull-down of the GIO_P103 pin. 0: Pull down, 1: Pull up
GIO103_POENB	R/W	28	0	Specifies whether to enable pull-up or pull-down of the GIO_P103 pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
GIO102_IE	R/W	26	0	Specifies whether to enable inputting to the GIO_P102 pin. 0: Masks inputs. 1: Enables inputs.
GIO102_UPC	R/W	25	0	Specifies pull-up or pull-down of the GIO_P102 pin. 0: Pull down, 1: Pull up
GIO102_POENB	R/W	24	0	Specifies whether to enable pull-up or pull-down of the GIO_P102 pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
GIO101_IE	R/W	22	0	Specifies whether to enable inputting to the GIO_P101 pin. 0: Masks inputs. 1: Enables inputs.
GIO101_UPC	R/W	21	0	Specifies pull-up or pull-down of the GIO_P101 pin. 0: Pull down, 1: Pull up
GIO101_POENB	R/W	20	0	Specifies whether to enable pull-up or pull-down of the GIO_P101 pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
GIO100_IE	R/W	18	0	Specifies whether to enable inputting to the GIO_P100 pin. 0: Masks inputs. 1: Enables inputs.
GIO100_UPC	R/W	17	0	Specifies pull-up or pull-down of the GIO_P100 pin. 0: Pull down, 1: Pull up

(2/2)

Name	R/W	Bit	After Reset	Function
GIO100_POENB	R/W	16	0	Specifies whether to enable pull-up or pull-down of the GIO_P100 pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
GIO99_IE	R/W	14	0	Specifies whether to enable inputting to the GIO_P99 pin. 0: Masks inputs. 1: Enables inputs.
GIO99_UPC	R/W	13	0	Specifies pull-up or pull-down of the GIO_P99 pin. 0: Pull down, 1: Pull up
GIO99_POENB	R/W	12	0	Specifies whether to enable pull-up or pull-down of the GIO_P99 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
GIO98_IE	R/W	10	0	Specifies whether to enable inputting to the GIO_P98 pin. 0: Masks inputs. 1: Enables inputs.
GIO98_UPC	R/W	9	0	Specifies pull-up or pull-down of the GIO_P98 pin. 0: Pull down, 1: Pull up
GIO98_POENB	R/W	8	0	Specifies whether to enable pull-up or pull-down of the GIO_P98 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
GIO97_IE	R/W	6	0	Specifies whether to enable inputting to the GIO_P97 pin. 0: Masks inputs. 1: Enables inputs.
GIO97_UPC	R/W	5	0	Specifies pull-up or pull-down of the GIO_P97 pin. 0: Pull down, 1: Pull up
GIO97_POENB	R/W	4	0	Specifies whether to enable pull-up or pull-down of the GIO_P97 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
GIO96_IE	R/W	2	0	Specifies whether to enable inputting to the GIO_P96 pin. 0: Masks inputs. 1: Enables inputs.
GIO96_UPC	R/W	1	0	Specifies pull-up or pull-down of the GIO_P96 pin. 0: Pull down, 1: Pull up
GIO96_POENB	R/W	0	0	Specifies whether to enable pull-up or pull-down of the GIO_P96 pin. 0: Enable, 1: Disable

(35) GIO_P[111:104] pin pull-up/pull-down/input enable control register

This register (CHG_PULL_G104: C014_0334H) selects pull-up or pull-down and enable inputs for the GIO_P[111:104] pins.

31	30	29	28	27	26	25	24
Reserved	GIO111_IE	GIO111_UPC	GIO111_POENB	Reserved	GIO110_IE	GIO110_UPC	GIO110_POENB
23	22	21	20	19	18	17	16
Reserved	GIO109_IE	GIO109_UPC	GIO109_POENB	Reserved	GIO108_IE	GIO108_UPC	GIO108_POENB
15	14	13	12	11	10	9	8
Reserved	GIO107_IE	GIO107_UPC	GIO107_POENB	Reserved	GIO106_IE	GIO106_UPC	GIO106_POENB
7	6	5	4	3	2	1	0
Reserved	GIO105_IE	GIO105_UPC	GIO105_POENB	Reserved	GIO104_IE	GIO104_UPC	GIO104_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
GIO111_IE	R/W	30	0	Specifies whether to enable inputting to the GIO_P111 pin. 0: Masks inputs. 1: Enables inputs.
GIO111_UPC	R/W	29	0	Specifies pull-up or pull-down of the GIO_P111 pin. 0: Pull down, 1: Pull up
GIO111_POENB	R/W	28	0	Specifies whether to enable pull-up or pull-down of the GIO_P111 pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
GIO110_IE	R/W	26	0	Specifies whether to enable inputting to the GIO_P110 pin. 0: Masks inputs. 1: Enables inputs.
GIO110_UPC	R/W	25	0	Specifies pull-up or pull-down of the GIO_P110 pin. 0: Pull down, 1: Pull up
GIO110_POENB	R/W	24	0	Specifies whether to enable pull-up or pull-down of the GIO_P110 pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
GIO109_IE	R/W	22	0	Specifies whether to enable inputting to the GIO_P109 pin. 0: Masks inputs. 1: Enables inputs.
GIO109_UPC	R/W	21	0	Specifies pull-up or pull-down of the GIO_P109 pin. 0: Pull down, 1: Pull up
GIO109_POENB	R/W	20	0	Specifies whether to enable pull-up or pull-down of the GIO_P109 pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
GIO108_IE	R/W	18	0	Specifies whether to enable inputting to the GIO_P108 pin. 0: Masks inputs. 1: Enables inputs.
GIO108_UPC	R/W	17	0	Specifies pull-up or pull-down of the GIO_P108 pin. 0: Pull down, 1: Pull up

(2/2)

Name	R/W	Bit	After Reset	Function
GIO108_POENB	R/W	16	0	Specifies whether to enable pull-up or pull-down of the GIO_P108 pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
GIO107_IE	R/W	14	0	Specifies whether to enable inputting to the GIO_P107 pin. 0: Masks inputs. 1: Enables inputs.
GIO107_UPC	R/W	13	0	Specifies pull-up or pull-down of the GIO_P107 pin. 0: Pull down, 1: Pull up
GIO107_POENB	R/W	12	0	Specifies whether to enable pull-up or pull-down of the GIO_P107 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
GIO106_IE	R/W	10	0	Specifies whether to enable inputting to the GIO_P106 pin. 0: Masks inputs. 1: Enables inputs.
GIO106_UPC	R/W	9	0	Specifies pull-up or pull-down of the GIO_P106 pin. 0: Pull down, 1: Pull up
GIO106_POENB	R/W	8	0	Specifies whether to enable pull-up or pull-down of the GIO_P106 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
GIO105_IE	R/W	6	0	Specifies whether to enable inputting to the GIO_P105 pin. 0: Masks inputs. 1: Enables inputs.
GIO105_UPC	R/W	5	0	Specifies pull-up or pull-down of the GIO_P105 pin. 0: Pull down, 1: Pull up
GIO105_POENB	R/W	4	0	Specifies whether to enable pull-up or pull-down of the GIO_P105 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
GIO104_IE	R/W	2	0	Specifies whether to enable inputting to the GIO_P104 pin. 0: Masks inputs. 1: Enables inputs.
GIO104_UPC	R/W	1	0	Specifies pull-up or pull-down of the GIO_P104 pin. 0: Pull down, 1: Pull up
GIO104_POENB	R/W	0	0	Specifies whether to enable pull-up or pull-down of the GIO_P104 pin. 0: Enable, 1: Disable

(36) GIO_P[119:112] pin pull-up/pull-down/input enable control register

This register (CHG_PULL_G112: C014_0338H) selects pull-up or pull-down and enable inputs for the GIO_P[119:112] pins.

31	30	29	28	27	26	25	24
Reserved	GIO119_IE	GIO119_UPC	GIO119_POENB	Reserved	GIO118_IE	GIO118_UPC	GIO118_POENB
23	22	21	20	19	18	17	16
Reserved	GIO117_IE	GIO117_UPC	GIO117_POENB	Reserved	GIO116_IE	GIO116_UPC	GIO116_POENB
15	14	13	12	11	10	9	8
Reserved	GIO115_IE	GIO115_UPC	GIO115_POENB	Reserved	GIO114_IE	GIO114_UPC	GIO114_POENB
7	6	5	4	3	2	1	0
Reserved	GIO113_IE	GIO113_UPC	GIO113_POENB	Reserved	GIO112_IE	GIO112_UPC	GIO112_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
GIO119_IE	R/W	30	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P119 pin. 0: Masks inputs. 1: Enables inputs.
GIO119_UPC	R/W	29	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P119 pin. 0: Pull down, 1: Pull up
GIO119_POENB	R/W	28	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P119 pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
GIO118_IE	R/W	26	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P118 pin. 0: Masks inputs. 1: Enables inputs.
GIO118_UPC	R/W	25	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P118 pin. 0: Pull down, 1: Pull up
GIO118_POENB	R/W	24	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P118 pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
GIO117_IE	R/W	22	0	Specifies whether to enable inputting to the GIO_P117 pin. 0: Masks inputs. 1: Enables inputs.
GIO117_UPC	R/W	21	0	Specifies pull-up or pull-down of the GIO_P117 pin. 0: Pull down, 1: Pull up
GIO117_POENB	R/W	20	0	Specifies whether to enable pull-up or pull-down of the GIO_P117 pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
GIO116_IE	R/W	18	0	Specifies whether to enable inputting to the GIO_P116 pin. 0: Masks inputs. 1: Enables inputs.

Note The spare bits are provided in the register, but they do not indicate any hardware status.

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Name	R/W	Bit	After Reset	Function
GIO116_UPC	R/W	17	0	Specifies pull-up or pull-down of the GIO_P116 pin. 0: Pull down, 1: Pull up
GIO116_POENB	R/W	16	0	Specifies whether to enable pull-up or pull-down of the GIO_P116 pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
GIO115_IE	R/W	14	0	Specifies whether to enable inputting to the GIO_P115 pin. 0: Masks inputs. 1: Enables inputs.
GIO115_UPC	R/W	13	0	Specifies pull-up or pull-down of the GIO_P115 pin. 0: Pull down, 1: Pull up
GIO115_POENB	R/W	12	0	Specifies whether to enable pull-up or pull-down of the GIO_P115 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
GIO114_IE	R/W	10	0	Specifies whether to enable inputting to the GIO_P114 pin. 0: Masks inputs. 1: Enables inputs.
GIO114_UPC	R/W	9	0	Specifies pull-up or pull-down of the GIO_P114 pin. 0: Pull down, 1: Pull up
GIO114_POENB	R/W	8	0	Specifies whether to enable pull-up or pull-down of the GIO_P114 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
GIO113_IE	R/W	6	0	Specifies whether to enable inputting to the GIO_P113 pin. 0: Masks inputs. 1: Enables inputs.
GIO113_UPC	R/W	5	0	Specifies pull-up or pull-down of the GIO_P113 pin. 0: Pull down, 1: Pull up
GIO113_POENB	R/W	4	0	Specifies whether to enable pull-up or pull-down of the GIO_P113 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
GIO112_IE	R/W	2	0	Specifies whether to enable inputting to the GIO_P112 pin. 0: Masks inputs. 1: Enables inputs.
GIO112_UPC	R/W	1	0	Specifies pull-up or pull-down of the GIO_P112 pin. 0: Pull down, 1: Pull up
GIO112_POENB	R/W	0	0	Specifies whether to enable pull-up or pull-down of the GIO_P112 pin. 0: Enable, 1: Disable

(37) GIO_P[127:120] pin pull-up/pull-down/input enable control register

This register (CHG_PULL_G120: C014_033CH) selects pull-up or pull-down and enable inputs for the GIO_P[127:120] pins.

31	30	29	28	27	26	25	24
Reserved	GIO127_IE	GIO127_UPC	GIO127_POENB	Reserved	GIO126_IE	GIO126_UPC	GIO126_POENB
23	22	21	20	19	18	17	16
Reserved	GIO125_IE	GIO125_UPC	GIO125_POENB	Reserved	GIO124_IE	GIO124_UPC	GIO124_POENB
15	14	13	12	11	10	9	8
Reserved	GIO123_IE	GIO123_UPC	GIO123_POENB	Reserved	GIO122_IE	GIO122_UPC	GIO122_POENB
7	6	5	4	3	2	1	0
Reserved	GIO121_IE	GIO121_UPC	GIO121_POENB	Reserved	GIO120_IE	GIO120_UPC	GIO120_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
GIO127_IE	R/W	30	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P127 pin. 0: Masks inputs. 1: Enables inputs.
GIO127_UPC	R/W	29	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P127 pin. 0: Pull down, 1: Pull up
GIO127_POENB	R/W	28	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P127 pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
GIO126_IE	R/W	26	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P126 pin. 0: Masks inputs. 1: Enables inputs.
GIO126_UPC	R/W	25	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P126 pin. 0: Pull down, 1: Pull up
GIO126_POENB	R/W	24	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P126 pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
GIO125_IE	R/W	22	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P125 pin. 0: Masks inputs. 1: Enables inputs.
GIO125_UPC	R/W	21	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P125 pin. 0: Pull down, 1: Pull up
GIO125_POENB	R/W	20	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P125 pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.

Note The spare bits are provided in the register, but they do not indicate any hardware status.

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Name	R/W	Bit	After Reset	Function
GIO124_IE	R/W	18	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P124 pin. 0: Masks inputs. 1: Enables inputs.
GIO124_UPC	R/W	17	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P124 pin. 0: Pull down, 1: Pull up
GIO124_POENB	R/W	16	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P124 pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
GIO123_IE	R/W	14	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P123 pin. 0: Masks inputs. 1: Enables inputs.
GIO123_UPC	R/W	13	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P123 pin. 0: Pull down, 1: Pull up
GIO123_POENB	R/W	12	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P123 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
GIO122_IE	R/W	10	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P122 pin. 0: Masks inputs. 1: Enables inputs.
GIO122_UPC	R/W	9	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P122 pin. 0: Pull down, 1: Pull up
GIO122_POENB	R/W	8	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P122 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
GIO121_IE	R/W	6	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P121 pin. 0: Masks inputs. 1: Enables inputs.
GIO121_UPC	R/W	5	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P121 pin. 0: Pull down, 1: Pull up
GIO121_POENB	R/W	4	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P121 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
GIO120_IE	R/W	2	0	Spare bit[Note]. Specifies whether to enable inputting to the GIO_P120 pin. 0: Masks inputs. 1: Enables inputs.
GIO120_UPC	R/W	1	0	Spare bit[Note]. Specifies pull-up or pull-down of the GIO_P120 pin. 0: Pull down, 1: Pull up
GIO120_POENB	R/W	0	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the GIO_P120 pin. 0: Enable, 1: Disable

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(38) Pull-up/pull-down/input enable control register 0

This register (CHG_PULL0: C014_0380H) selects pull-up or pull-down and enable inputs for the URT0, IIC2, DTV, and DEN pins.

31	30	29	28	27	26	25	24
Reserved	URT0_SI_IE	URT0_SI_UPC	URT0_SI_POENB	Reserved	IIC2_IE	IIC2_UPC	IIC2_POENB
23	22	21	20	19	18	17	16
Reserved	DTV_V_IE	DTV_V_UPC	DTV_V_POENB	Reserved	DTV_S_IE	DTV_S_UPC	DTV_S_POENB
15	14	13	12	11	10	9	8
Reserved	DTV_D_IE	DTV_D_UPC	DTV_D_POENB	Reserved	DTV_CK_IE	DTV_CK_UPC	DTV_CK_POENB
7	6	5	4	3	2	1	0
Reserved					DEN_IE	DEN_UPC	DEN_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
URT0_SI_IE	R/W	30	0	Specifies whether to enable inputting to the URT0_SRIN pin. 0: Masks inputs. 1: Enables inputs.
URT0_SI_UPC	R/W	29	0	Specifies pull-up or pull-down of the URT0_SRIN pin. 0: Pull down, 1: Pull up
URT0_SI_POENB	R/W	28	0	Specifies whether to enable pull-up or pull-down of the URT0_SRIN pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
IIC2_IE	R/W	26	0	Spare bit[Note]. Specifies whether to enable inputting to the IIC_SCL and IIC_SDA pins. 0: Masks inputs. 1: Enables inputs.
IIC2_UPC	R/W	25	0	Specifies pull-up or pull-down of the IIC_SCL and IIC_SDA pins. 0: Pull down, 1: Pull up
IIC2_POENB	R/W	24	0	Specifies whether to enable pull-up or pull-down of the IIC_SCL and IIC_SDA pins. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
DTV_V_IE	R/W	22	0	Specifies whether to enable inputting to the DTV_VLD pin. 0: Masks inputs. 1: Enables inputs.
DTV_V_UPC	R/W	21	0	Specifies pull-up or pull-down of the DTV_VLD pin. 0: Pull down, 1: Pull up
DTV_V_POENB	R/W	20	0	Specifies whether to enable pull-up or pull-down of the DTV_VLD pin. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
DTV_S_IE	R/W	18	0	Specifies whether to enable inputting to the DTV_PSYNC pin. 0: Masks inputs. 1: Enables inputs.

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(2/2)

Name	R/W	Bit	After Reset	Function
DTV_S_UPC	R/W	17	0	Specifies pull-up or pull-down of the DTV_PSYNC pin. 0: Pull down, 1: Pull up
DTV_S_POENB	R/W	16	0	Specifies whether to enable pull-up or pull-down of the DTV_PSYNC pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
DTV_D_IE	R/W	14	0	Specifies whether to enable inputting to the DTV_DATA pin. 0: Masks inputs. 1: Enables inputs.
DTV_D_UPC	R/W	13	0	Specifies pull-up or pull-down of the DTV_DATA pin. 0: Pull down, 1: Pull up
DTV_D_POEN	R/W	12	0	Specifies whether to enable pull-up or pull-down of the DTV_DATA pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
DTV_CK_IE	R/W	10	0	Spare bit[Note]. Specifies whether to enable inputting to the DTV_BCLK pin. 0: Masks inputs. 1: Enables inputs.
DTV_CK_UPC	R/W	9	0	Specifies pull-up or pull-down of the DTV_BCLK pin. 0: Pull down, 1: Pull up
DTV_CK_POEN	R/W	8	0	Specifies whether to enable pull-up or pull-down of the DTV_BCLK pin. 0: Enable, 1: Disable
Reserved	R	7:3	–	Reserved. When these bits are read, 0 is returned for each bit.
DEN_IE	R/W	2	1	Specifies whether to enable inputting to the DEBUG_EN pin. 0: Masks inputs. 1: Enables inputs.
DEN_UPC	R/W	1	0	Specifies pull-up or pull-down of the DEBUG_EN pin. 0: Pull down, 1: Pull up
DEN_POENB	R/W	0	0	Specifies whether to enable pull-up or pull-down of the DEBUG_EN pin. 0: Enable, 1: Disable

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(39) Pull-up/pull-down/input enable control register 1

This register (CHG_PULL1: C014_0384H) selects pull-up or pull-down and enable inputs for the SP0, JT0A, JT0B, and JT0C pins.

31	30	29	28	27	26	25	24
Reserved	SP0_SO_IE	SP0_SO_UPC	SP0_SO_POENB	Reserved	SP0_SI_IE	SP0_SI_UPC	SP0_SI_POENB
23	22	21	20	19	18	17	16
Reserved	SP0_CS_IE	SP0_CS_UPC	SP0_CS_POENB	Reserved	SP0_CK_IE	SP0_CK_UPC	SP0_CK_POENB
15	14	13	12	11	10	9	8
Reserved	Spare			Reserved	JT0C_IE	JT0C_UPC	JT0C_POENB
7	6	5	4	3	2	1	0
Reserved	JT0B_IE	JT0B_UPC	JT0B_POENB	Reserved	JT0A_IE	JT0A_UPC	JT0A_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
SP0_SO_IE	R/W	30	0	Specifies whether to enable inputting to the SP0_SO pin. 0: Masks inputs. 1: Enables inputs.
SP0_SO_UPC	R/W	29	0	Specifies pull-up or pull-down of the SP0_SO pin. 0: Pull down, 1: Pull up
SP0_SO_POENB	R/W	28	0	Specifies whether to enable pull-up or pull-down of the SP0_SO pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
SP0_SI_IE	R/W	26	0	Specifies whether to enable inputting to the SP0_SI pin. 0: Masks inputs. 1: Enables inputs.
SP0_SI_UPC	R/W	25	0	Specifies pull-up or pull-down of the SP0_SI pin. 0: Pull down, 1: Pull up
SP0_SI_POENB	R/W	24	0	Specifies whether to enable pull-up or pull-down of the SP0_SI pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
SP0_CS_IE	R/W	22	0	Specifies whether to enable inputting to the SP0_CS[2:0] pins. 0: Masks inputs. 1: Enables inputs.
SP0_CS_UPC	R/W	21	0	Specifies pull-up or pull-down of the SP0_CS[2:0] pins. 0: Pull down, 1: Pull up
SP0_CS_POENB	R/W	20	0	Specifies whether to enable pull-up or pull-down of the SP0_CS[2:0] pins. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
SP0_CK_IE	R/W	18	0	Specifies whether to enable inputting to the SP0_CLK pin. 0: Masks inputs. 1: Enables inputs.
SP0_CK_UPC	R/W	17	0	Specifies pull-up or pull-down of the SP0_CLK pin. 0: Pull down, 1: Pull up

(2/2)

Name	R/W	Bit	After Reset	Function
SP0_CK_POENB	R/W	16	0	Specifies whether to enable pull-up or pull-down of the SP0_CLK pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
Spare	R/W	14:12	0	Spare bits[Note]
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
JT0C_IE	R/W	10	1	Specifies whether to enable inputting to the JT0_TDI and JT0_TMS pins. 0: Masks inputs. 1: Enables inputs.
JT0C_UPC	R/W	9	1	Specifies pull-up or pull-down of the JT0_TDI and JT0_TMS pins. 0: Pull down, 1: Pull up
JT0C_POENB	R/W	8	0	Specifies whether to enable pull-up or pull-down of the JT0_TDI and JT0_TMS pins. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
JT0B_IE	R/W	6	0	Spare bit[Note]. Specifies whether to enable inputting to the JT0_TCK pin. 0: Masks inputs. 1: Enables inputs.
JT0B_UPC	R/W	5	0	Specifies pull-up or pull-down of the JT0_TCK pin. 0: Pull down, 1: Pull up
JT0B_POENB	R/W	4	0	Specifies whether to enable pull-up or pull-down of the JT0_TCK pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
JT0A_IE	R/W	2	0	Spare bit[Note]. Specifies whether to enable inputting to the JT0_TRSTB pin. 0: Masks inputs. 1: Enables inputs.
JT0A_UPC	R/W	1	0	Specifies pull-up or pull-down of the JT0_TRSTB pin. 0: Pull down, 1: Pull up
JT0A_POENB	R/W	0	0	Specifies whether to enable pull-up or pull-down of the JT0_TRSTB pin. 0: Enable, 1: Disable

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(40) Pull-up/pull-down/input enable control register 2

This register (CHG_PULL2: C014_0388H) selects pull-up or pull-down and enable inputs for the PM0, SD0, and SD1 pins.

31	30	29	28	27	26	25	24
Reserved	PM0_EN_IE	PM0_EN_UPC	PM0_EN_POENB	Reserved	PM0_CK_IE	PM0_CK_UPC	PM0_CK_POENB
23	22	21	20	19	18	17	16
Reserved	SD1_D_IE	SD1_D_UPC	SD1_D_POENB	Reserved	SD1_CM_IE	SD1_CM_UPC	SD1_CM_POENB
15	14	13	12	11	10	9	8
Reserved	SD1_CK_IE	SD1_CK_UPC	SD1_CK_POENB	Reserved	SD0_D_IE	SD0_D_UPC	SD0_D_POENB
7	6	5	4	3	2	1	0
Reserved	SD0_CM_IE	SD0_CM_UPC	SD0_CM_POENB	Reserved	SD0_CK_IE	SD0_CK_UPC	SD0_CK_POENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
PM0_EN_IE	R/W	30	0	Specifies whether to enable inputting to the PM0_SEN pin. 0: Masks inputs. 1: Enables inputs.
PM0_EN_UPC	R/W	29	0	Specifies pull-up or pull-down of the PM0_SEN pin. 0: Pull down, 1: Pull up
PM0_EN_POENB	R/W	28	0	Specifies whether to enable pull-up or pull-down of the PM0_SEN pin. 0: Enable, 1: Disable
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
PM0_CK_IE	R/W	26	0	Spare bit[Note]. Specifies whether to enable inputting to the PM0_CLK pin. 0: Masks inputs. 1: Enables inputs.
PM0_CK_UPC	R/W	25	0	Specifies pull-up or pull-down of the PM0_CLK pin. 0: Pull down, 1: Pull up
PM0_CK_POENB	R/W	24	0	Specifies whether to enable pull-up or pull-down of the PM0_CLK pin. 0: Enable, 1: Disable
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
SD1_D_IE	R/W	22	0	Specifies whether to enable inputting to the SD1_D[3:0] pins. 0: Masks inputs. 1: Enables inputs.
SD1_D_UPC	R/W	21	0	Specifies pull-up or pull-down of the SD1_D[3:0] pins. 0: Pull down, 1: Pull up
SD1_D_POENB	R/W	20	0	Specifies whether to enable pull-up or pull-down of the SD1_D[3:0] pins. 0: Enable, 1: Disable
Reserved	R	19	–	Reserved. When this bit is read, 0 is returned.
SD1_CM_IE	R/W	18	0	Specifies whether to enable inputting to the SD1_CMD pin. 0: Masks inputs. 1: Enables inputs.
SD1_CM_UPC	R/W	17	0	Specifies pull-up or pull-down of the SD1_CMD pin. 0: Pull down, 1: Pull up

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(2/2)

Name	R/W	Bit	After Reset	Function
SD1_CM_POENB	R/W	16	0	Specifies whether to enable pull-up or pull-down of the SD1_CMD pin. 0: Enable, 1: Disable
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
SD1_CK_IE	R/W	14	0	Specifies whether to enable inputting to the SD1_CKO pins. 0: Masks inputs. 1: Enables inputs.
SD1_CK_UPC	R/W	13	0	Specifies pull-up or pull-down of the SD1_CKI and SD1_CKO pins. 0: Pull down, 1: Pull up
SD1_CK_POENB	R/W	12	1	Specifies whether to enable pull-up or pull-down of the SD1_CKI and SD1_CKO pins. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
SD0_D_IE	R/W	10	0	Specifies whether to enable inputting to the SD0_D[3:0] pins. 0: Masks inputs. 1: Enables inputs.
SD0_D_UPC	R/W	9	0	Specifies pull-up or pull-down of the SD0_D[3:0] pins. 0: Pull down, 1: Pull up
SD0_D_POENB	R/W	8	0	Specifies whether to enable pull-up or pull-down of the SD0_D[3:0] pins. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
SD0_CM_IE	R/W	6	0	Specifies whether to enable inputting to the SD0_CMD pin. 0: Masks inputs. 1: Enables inputs.
SD0_CM_UPC	R/W	5	0	Specifies pull-up or pull-down of the SD0_CMD pin. 0: Pull down, 1: Pull up
SD0_CM_POENB	R/W	4	0	Specifies whether to enable pull-up or pull-down of the SD0_CMD pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.
SD0_CK_IE	R/W	2	0	Specifies whether to enable inputting to the SD0_CKO pins. 0: Masks inputs. 1: Enables inputs.
SD0_CK_UPC	R/W	1	0	Specifies pull-up or pull-down of the SD0_CKI and SD0_CKO pins. 0: Pull down, 1: Pull up
SD0_CK_POENB	R/W	0	1	Specifies whether to enable pull-up or pull-down of the SD0_CKI and SD0_CKO pins. 0: Enable, 1: Disable

(41) Pull-up/pull-down/input enable control register 3

This register (CHG_PULL3: C014_038CH) selects pull-up or pull-down and enable inputs for the RSV0, RSV1, RSV2, and RSV3 pins.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	RSV3_IE	RSV3_UPC	RSV3_P0ENB	Reserved	RSV2_IE	RSV2_UPC	RSV2_P0ENB
7	6	5	4	3	2	1	0
Reserved	RSV1_IE	RSV1_UPC	RSV1_P0ENB	Reserved	RSV0_IE	RSV0_UPC	RSV0_P0ENB

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31:15	–	Reserved. When these bits are read, 0 is returned for each bit.
RSV3_IE	R/W	14	0	Spare bit[Note]. Specifies whether to enable inputting to the RSV3 pin. 0: Masks inputs. 1: Enables inputs.
RSV3_UPC	R/W	13	0	Spare bit[Note]. Specifies pull-up or pull-down of the RSV3 pin. 0: Pull down, 1: Pull up
RSV3_POENB	R/W	12	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the RSV3 pin. 0: Enable, 1: Disable
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
RSV2_IE	R/W	10	0	Spare bit[Note]. Specifies whether to enable inputting to the RSV2 pin. 0: Masks inputs. 1: Enables inputs.
RSV2_UPC	R/W	9	0	Spare bit[Note]. Specifies pull-up or pull-down of the RSV2 pin. 0: Pull down, 1: Pull up
RSV2_POENB	R/W	8	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the RSV2 pin. 0: Enable, 1: Disable
Reserved	R	7	–	Reserved. When this bit is read, 0 is returned.
RSV1_IE	R/W	6	0	Spare bit[Note]. Specifies whether to enable inputting to the RSV1 pin. 0: Masks inputs. 1: Enables inputs.
RSV1_UPC	R/W	5	0	Spare bit[Note]. Specifies pull-up or pull-down of the RSV1 pin. 0: Pull down, 1: Pull up
RSV1_POENB	R/W	4	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the RSV1 pin. 0: Enable, 1: Disable
Reserved	R	3	–	Reserved. When this bit is read, 0 is returned.

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(2/2)

Name	R/W	Bit	After Reset	Function
RSV0_IE	R/W	2	0	Spare bit[Note]. Specifies whether to enable inputting to the RSV0 pin. 0: Masks inputs. 1: Enables inputs.
RSV0_UPC	R/W	1	0	Spare bit[Note]. Specifies pull-up or pull-down of the RSV0 pin. 0: Pull down, 1: Pull up
RSV0_POENB	R/W	0	0	Spare bit[Note]. Specifies whether to enable pull-up or pull-down of the RSV0 pin. 0: Enable, 1: Disable

Note The spare bits are provided in the register, but they do not indicate any hardware status.

(42) Drive capability switch register 0

This register (CHG_DRIVE0: C014_0400H) switches the IO buffer drive capability.

31	30	29	28	27	26	25	24
IIC		GIO2		GIO1		ERR	
23	22	21	20	19	18	17	16
DTV_CK		DTV		DQS		DQM	
15	14	13	12	11	10	9	8
DQ		DDR_CK		DDR_A		AB_W	
7	6	5	4	3	2	1	0
AB_D		AB_CK		AB_ADV		AB_A	

Name	R/W	Bit	After Reset	Function
IIC	R/W	31:30	01b	Switches the driving capability of the IIC_SCL and IIC_SDA signals.
GIO2	R/W	29:28	01b	Switches the driving capability of the GIO_P[10:5] signals.
GIO1	R/W	27:26	01b	Switches the driving capability of the GIO_P[4:0], PWM0 and PWM1 signals.
ERR	R/W	25:24	01b	Switches the driving capability of the ERR_RST_REQB signal.
DTV_CK	R/W	23:22	01b	Switches the driving capability of the DTV_BCLK signal.
DTV	R/W	21:20	01b	Switches the driving capability of the DTV_DATA, DTV_PSYNC, and DTV_VLD signals.
DQS	R/W	19:18	00b	Switches the driving capability of the DDR_DQS[3:0] signals.
DQM	R/W	17:16	00b	Switches the driving capability of the DDR_DQM[3:0] signals.
DQ	R/W	15:14	00b	Switches the driving capability of the DDR_DATA[31:0] signals.
DDR_CK	R/W	13:12	00b	Switches the driving capability of the DDR_MCLK and DDR_MCLKB signals.
DDR_A	R/W	11:10	00b	Switches the driving capability of the DDR_A[13:0], DDR_CKE[1:0], DDR_CSB[1:0], DDR_BA[1:0] signals.
AB_W	R/W	9:8	01b	Switches the driving capability of the AB0_WAIT signal.
AB_D	R/W	7:6	01b	Switches the driving capability of the AB0_AD[15:0] signals.
AB_CK	R/W	5:4	01b	Switches the driving capability of the AB0_CLK signal.
AB_ADV	R/W	3:2	01b	Switches the driving capability of the AB0_ADV signal.
AB_A	R/W	1:0	01b	Switches the driving capability of the AB0_A[26:17], AB0_RDB, AB0_WRB, AB0_CSB[3:0], AB0_BEN[1:0] signals.

Bits [19:10]			Bits [31:20][9:8][1:0]			Bits [7:2]		
[1]	[0]	Drive Capability	[1]	[0]	Drive Capability	[1]	[0]	Drive Capability
0	0	4 mA (initial value)	0	0	2 mA	0	0	2 mA
0	1	6 mA	0	1	4 mA (initial value)	0	1	4 mA (initial value)
1	0	8 mA	1	0	6 mA	1	0	8 mA
1	1	12 mA	1	1	8 mA	1	1	12 mA

(43) Drive capability switch register 1

This register (CHG_DRIVE1: C014_0404H) switches the IO buffer drive capability.

31	30	29	28	27	26	25	24
SP0_CK		SP0		SD2_CK		SD2	
23	22	21	20	19	18	17	16
SD1_CK		SD1		SD0_CK		SD0	
15	14	13	12	11	10	9	8
REF_CK		PM1_CK		PM1		PM0	
7	6	5	4	3	2	1	0
LCD_CK		LCD		JT0		IIC2	

Name	R/W	Bit	After Reset	Function
SP0_CK	R/W	31:30	01b	Switches the driving capability of the SP0_CLK signal.
SP0	R/W	29:28	01b	Switches the driving capability of the SP0_SI, SP0_SO, and SP0_CS[2:0] signals.
SD2_CK	R/W	27:26	01b	Switches the driving capability of the SD2_CKO signal.
SD2	R/W	25:24	01b	Switches the driving capability of the SD2_CMD, SD2_DATA[3:0] and SD2_CKI signals.
SD1_CK	R/W	23:22	01b	Switches the driving capability of the SD1_CKO signals.
SD1	R/W	21:20	01b	Switches the driving capability of the SD1_CMD, SD1_DATA[3:0] and SD1_CKI signals.
SD0_CK	R/W	19:18	01b	Switches the driving capability of the SD0_CKO signal.
SD0	R/W	17:16	01b	Switches the driving capability of the SD0_CMD, SD0_DATA[3:0] and SD0_CKI signals.
REF_CK	R/W	15:14	01b	Switches the driving capability of the REFCLKO signal.
PM1_CK	R/W	13:12	01b	Switches the driving capability of the GIO_P79 signal.
PM1	R/W	11:10	01b	Switches the driving capability of the GIO_P[82:80] signals.
PM0	R/W	9:8	01b	Switches the driving capability of the PM0_CLK, PM0_SEN, PM0_SI, and PM0_SO signals.
LCD_CK	R/W	7:6	01b	Switches the driving capability of the LCD_PXCLK signals.
LCD	R/W	5:4	01b	Switches the driving capability of the LCD_R[5:0], LCD_G[5:0], LCD_B[5:0], LCD_HSYNC, LCD_VSYNC, and LCD_ENABLE signals.
JT0	R/W	3:2	01b	Switches the driving capability of the JT0_TCK, JT0_TRSTB, JT0_TMS, JT0_TDI, JT0_TDO, and JT0_RTCK signals.
IIC2	R/W	1:0	01b	Switches the driving capability of the IIC2_SCL and IIC2_SDA signals.

Bits [7:4]			Other Than Bits [7:4]		
[1]	[0]	Drive Capability	[1]	[0]	Drive Capability
0	0	2 mA	0	0	2 mA
0	1	4 mA (initial value)	0	1	4 mA (initial value)
1	0	8 mA	1	0	6 mA
1	1	12 mA	1	1	8 mA

(44) Drive capability switch register 2

This register (CHG_DRIVE2: C014_0408H) switches the IO buffer drive capability.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
DRIVE_RSV3		DRIVE_RSV2		DRIVE_RSV1		USB_STP	
15	14	13	12	11	10	9	8
Reserved		USB_CLK		USB		URT2	
7	6	5	4	3	2	1	0
URT1		URT0		SP1_CK		SP1	

Name	R/W	Bit	After Reset	Function
Reserved	R	31:24	–	Reserved. When these bits are read, 0 is returned for each bit.
DRIVE_RSV3	R/W	23:22	0	Spare bits for DRIVE_RSV3.
DRIVE_RSV2	R/W	21:20	0	Spare bits for DRIVE_RSV2.
DRIVE_RSV1	R/W	19:18	0	Spare bits for DRIVE_RSV1.
USB_STP	R/W	17:16	01b	Switches the driving capability of the USB_STP.
Reserved	R	15:14	–	Reserved. When these bits are read, 0 is returned for each bit.
USB_CLK	R/W	13:12	01b	Switches the driving capability of the USB_CLK signal.
USB	R/W	11:10	01b	Switches the driving capability of the USB_DATA[7:0], USB_DIR and USB_NXT signals.
URT2	R/W	9:8	01b	Switches the driving capability of the URT2_SRIN, URT2_SOUT, URT2_RTSB, and URT2_CTSB signals.
URT1	R/W	7:6	01b	Switches the driving capability of the GIO_P[86:85] signals
URT0	R/W	5:4	01b	Switches the driving capability of the URT0_SOUT signal.
SP1_CK	R/W	3:2	01b	Switches the driving capability of the SP1_CLK signal.
SP1	R/W	1:0	01b	Switches the driving capability of the SP1_SI, SP1_SO, and SP1_CS[3:0] signals.

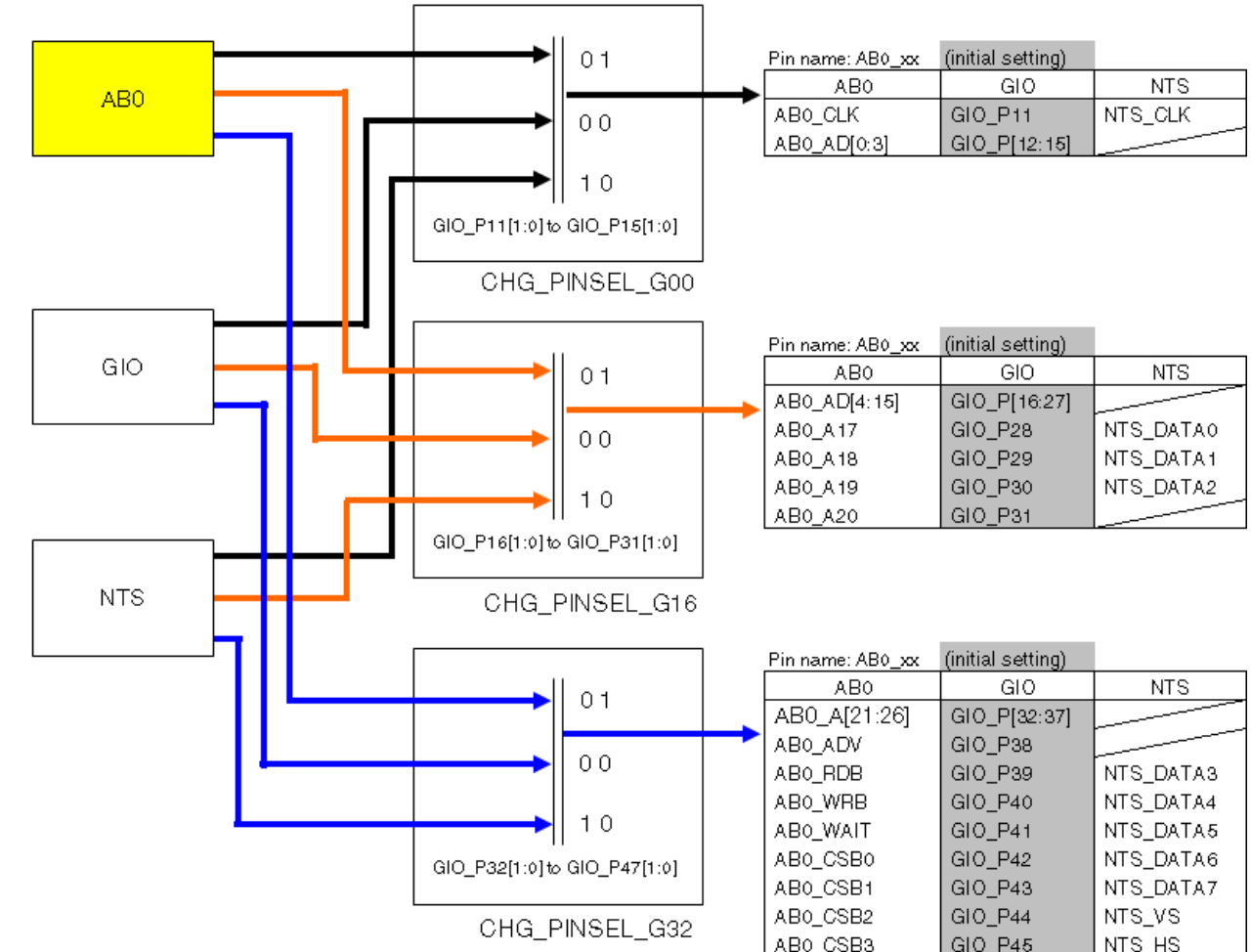
Bits [17:16], [13:10]			Bits [9:0]		
[1]	[0]	Drive Capability	[1]	[0]	Drive Capability
0	0	2 mA	0	0	2 mA
0	1	4 mA (initial value)	0	1	4 mA (initial value)
1	0	8 mA	1	0	6 mA
1	1	12 mA	1	1	8 mA

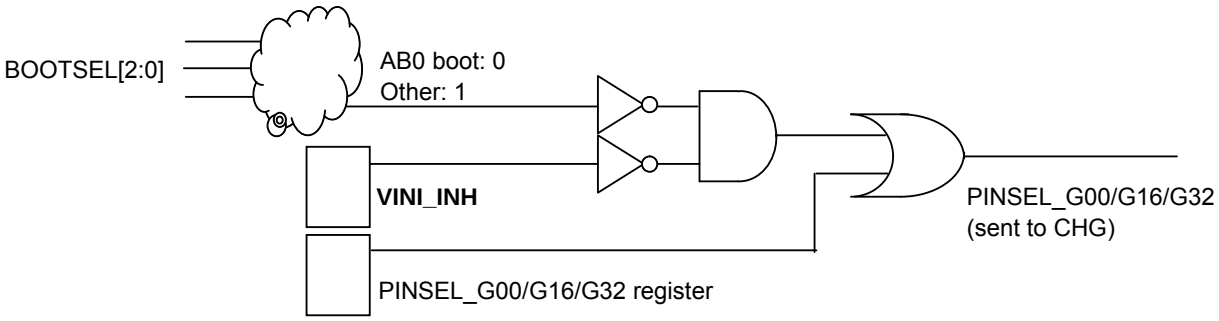
8.2 Selector Configuration

8.2.1 AB0 interface alternate-function pins

Figure 8-1 shows the selector configuration of the AB0 interface pins.

Figure 8-1. Selector Configuration of AB0 Interface Alternate-Function Pins

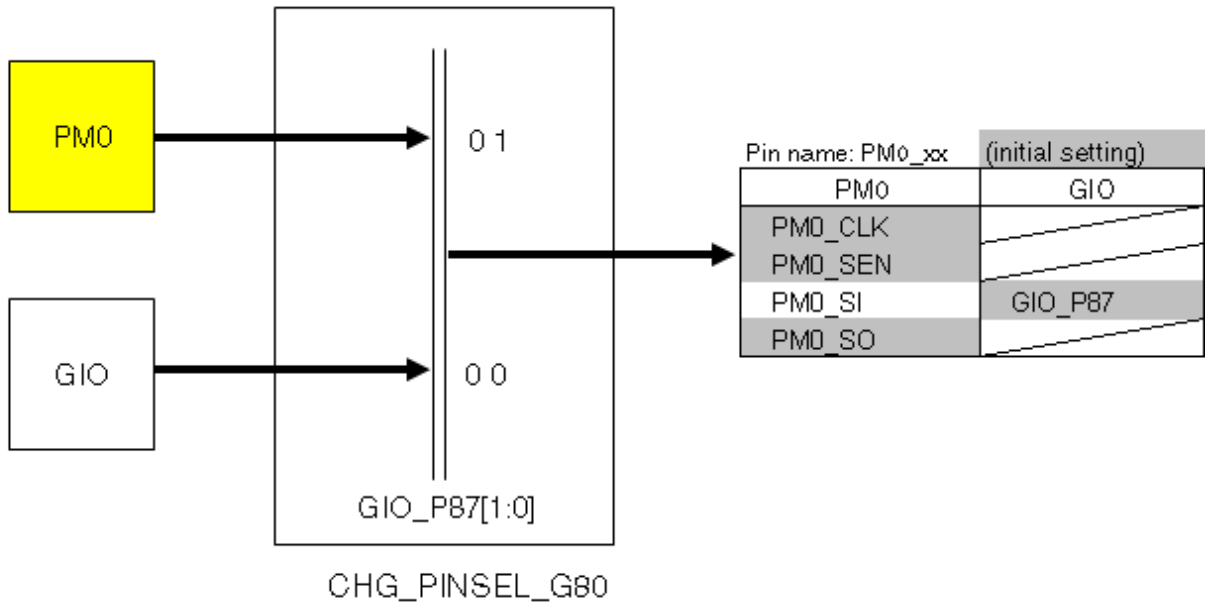




8.2.2 PCM0 interface alternate-function pins

Figure 8-2 shows the selector configuration of PM0 interface pins.

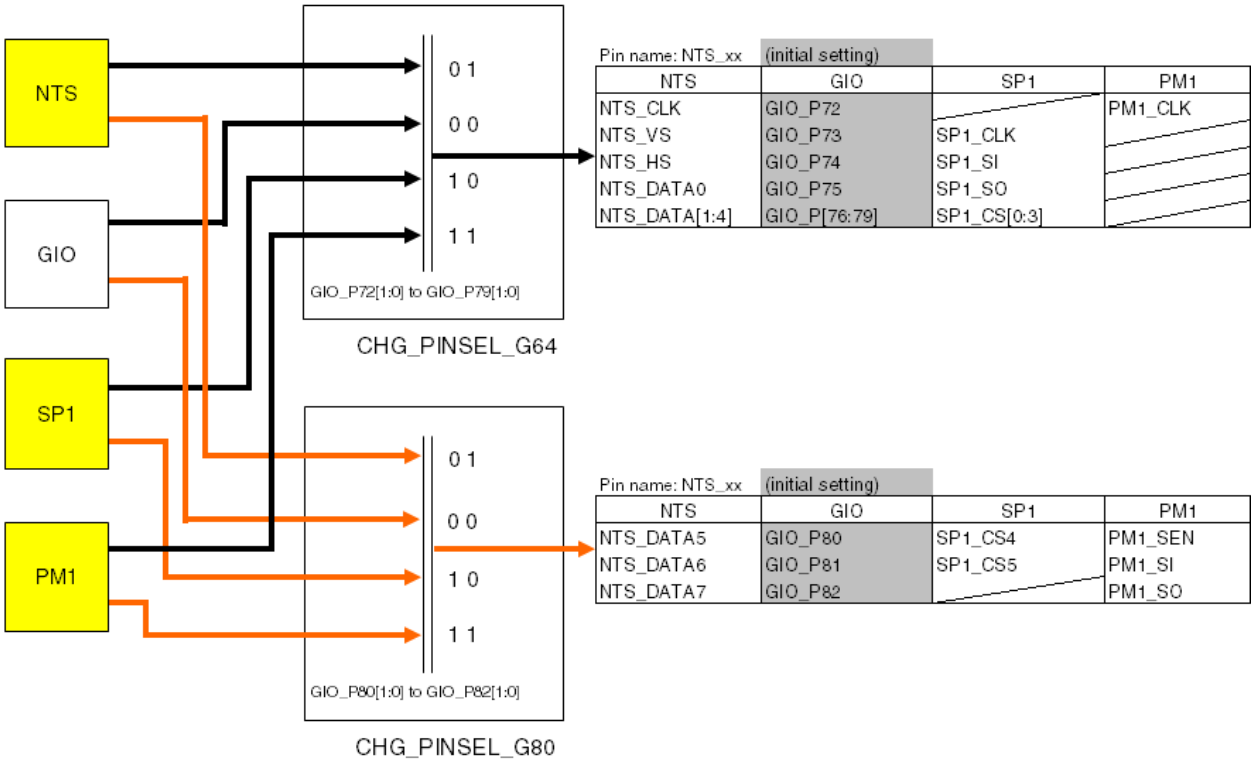
Figure 8-2. Selector Configuration of PCM0 Interface Alternate-Function Pins



8.2.3 ITU-R BT.656/SPI1/PCM1 interface alternate-function pins

Figure 8-3 shows the selector configuration of NTSC interface, SP1 interface, PM1 interface pins.

Figure 8-3. Selector Configuration of ITU-R BT.656/SPI1/PCM1 Interface Alternate-Function Pins



Pin name: NTS_xx (initial setting)

NTS	GIO	SP1	PM1
NTS_CLK	GIO_P72		PM1_CLK
NTS_VS	GIO_P73	SP1_CLK	
NTS_HS	GIO_P74	SP1_SI	
NTS_DATA0	GIO_P75	SP1_SO	
NTS_DATA[1:4]	GIO_P[76:79]	SP1_CS[0:3]	

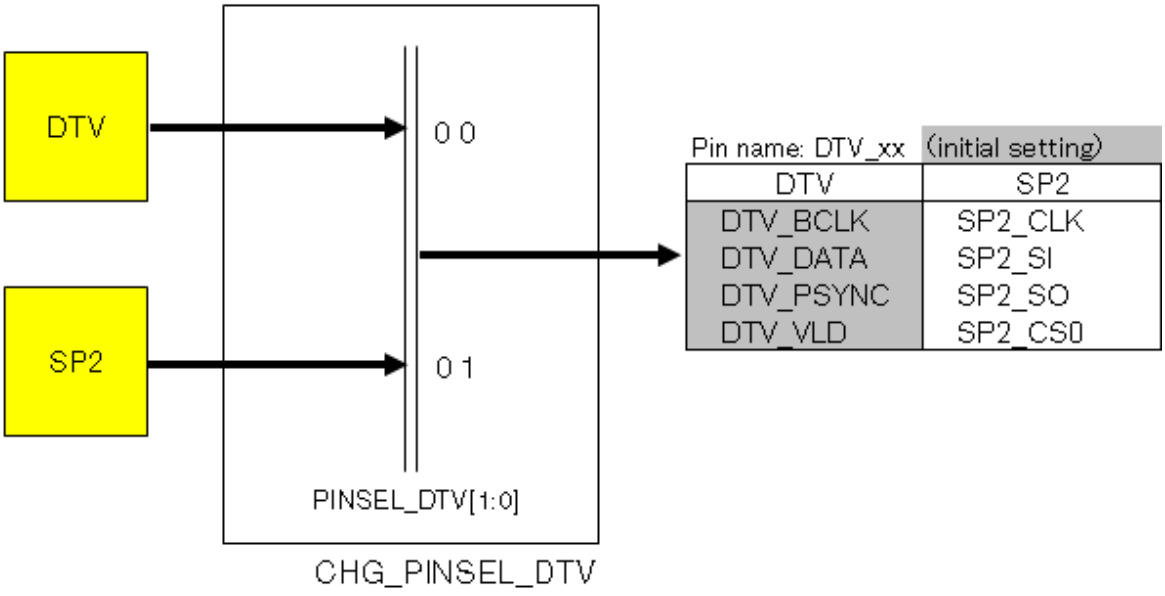
Pin name: NTS_xx (initial setting)

NTS	GIO	SP1	PM1
NTS_DATA5	GIO_P80	SP1_CS4	PM1_SEN
NTS_DATA6	GIO_P81	SP1_CS5	PM1_SI
NTS_DATA7	GIO_P82		PM1_SO

8.2.4 DTV/SPI2 interface alternate-function pins

Figure 8-4 shows the selector configuration of DTV interface and SP2 interface pins.

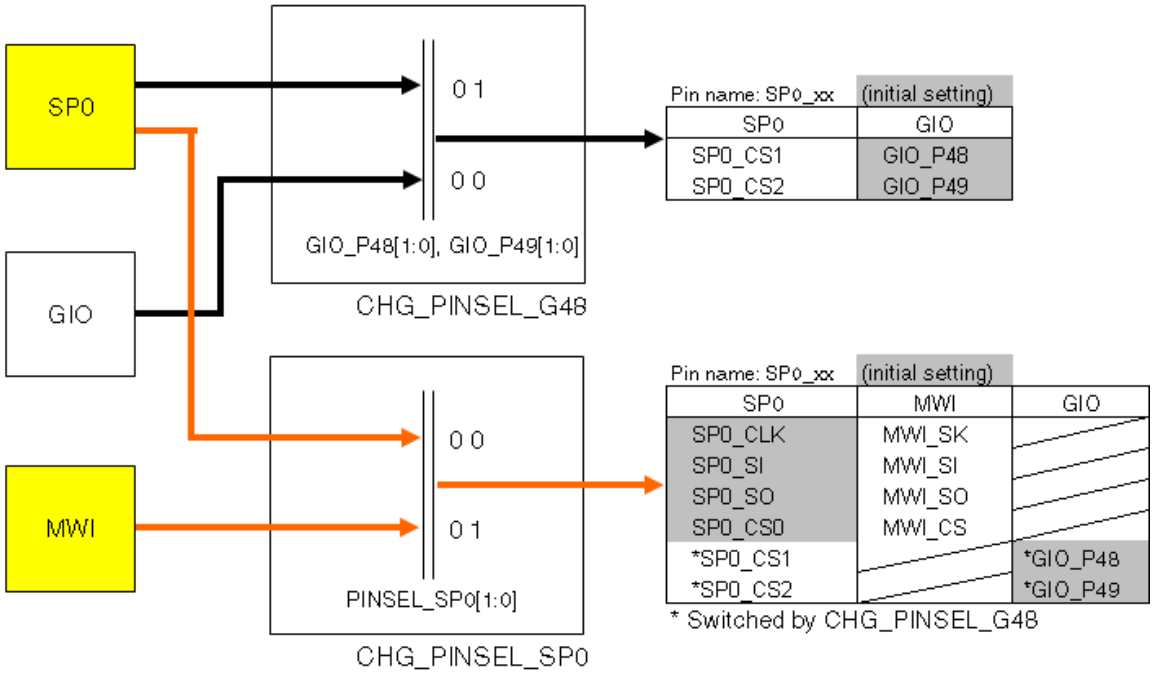
Figure 8-4. Selector Configuration of DTV/SPI2 Interface Alternate-Function Pins



8.2.5 SPI0/MWI interface alternate-function pins

Figure 8-5 shows the selector configuration of SP0 interface and MWI interface pins.

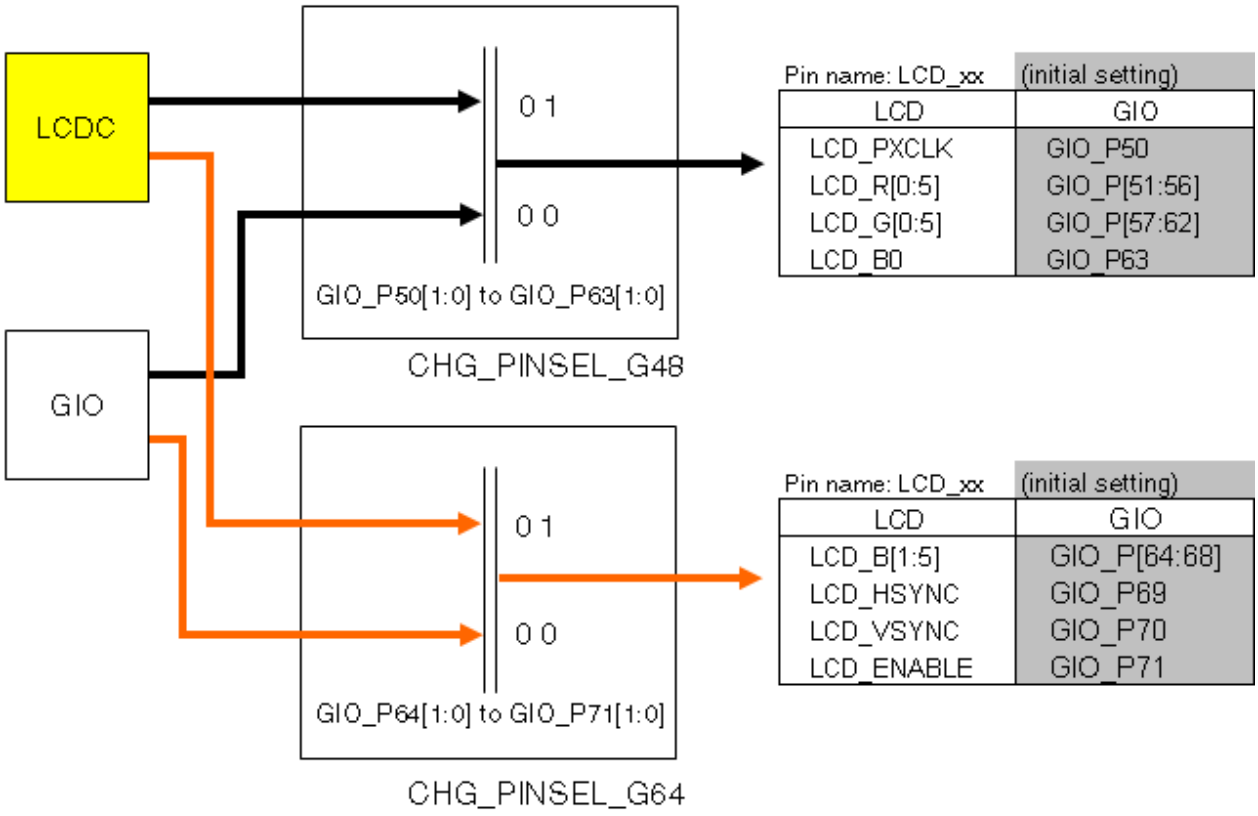
Figure 8-5. Selector Configuration of SPI0/MWI Interface Alternate-Function Pins



8.2.6 LCD interface alternate-function pins

Figure 8-6 shows the selector configuration of LCD interface pin.

Figure 8-6. Selector Configuration of LCD Interface Alternate-Function Pins



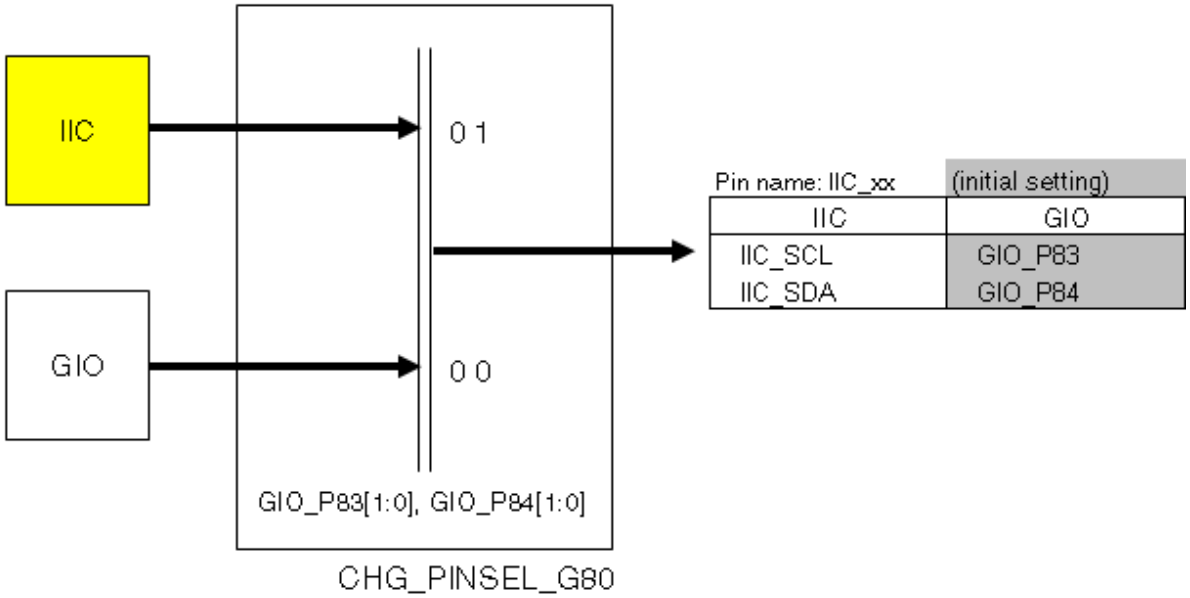
Pin name: LCD_xx	(initial setting)
LCD	GIO
LCD_PXCLK	GIO_P50
LCD_R[0:5]	GIO_P[51:56]
LCD_G[0:5]	GIO_P[57:62]
LCD_B0	GIO_P63

Pin name: LCD_xx	(initial setting)
LCD	GIO
LCD_B[1:5]	GIO_P[64:68]
LCD_HSYNC	GIO_P69
LCD_VSYNC	GIO_P70
LCD_ENABLE	GIO_P71

8.2.7 I²C interface alternate-function pins

Figure 8-7 shows the selector configuration of I²C interface pins.

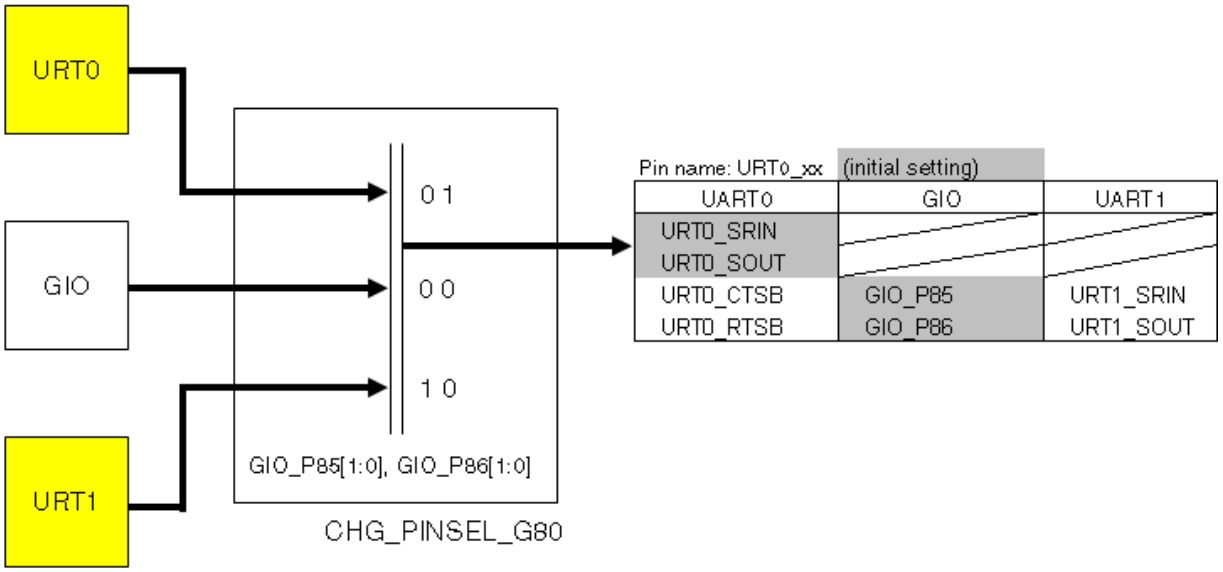
Figure 8-7. Selector Configuration of I²C Interface Alternate-Function Pins



8.2.8 UART0/UART1 interface alternate-function pins

Figure 8-8 shows the selector configuration of UART0 and UART1 interface pins.

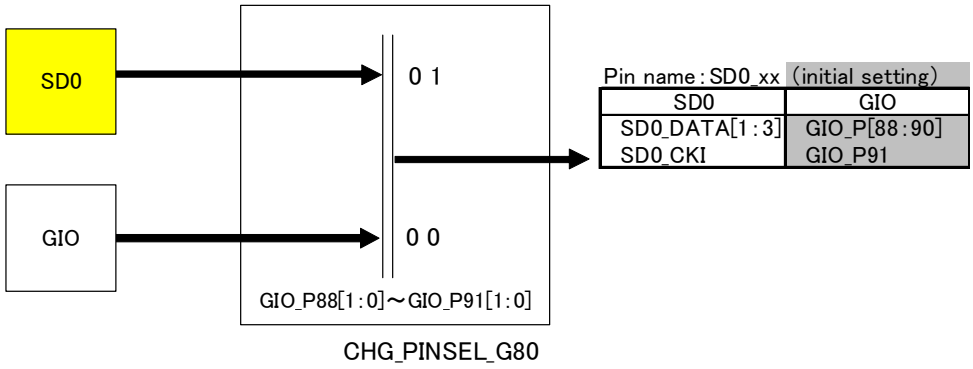
Figure 8-8. Selector Configuration of UART0/UART1 Interface Alternate-Function Pins



8.2.9 SD0 interface alternate-function pins

Figure 8-9 shows the selector configuration of SD0 interface pins.

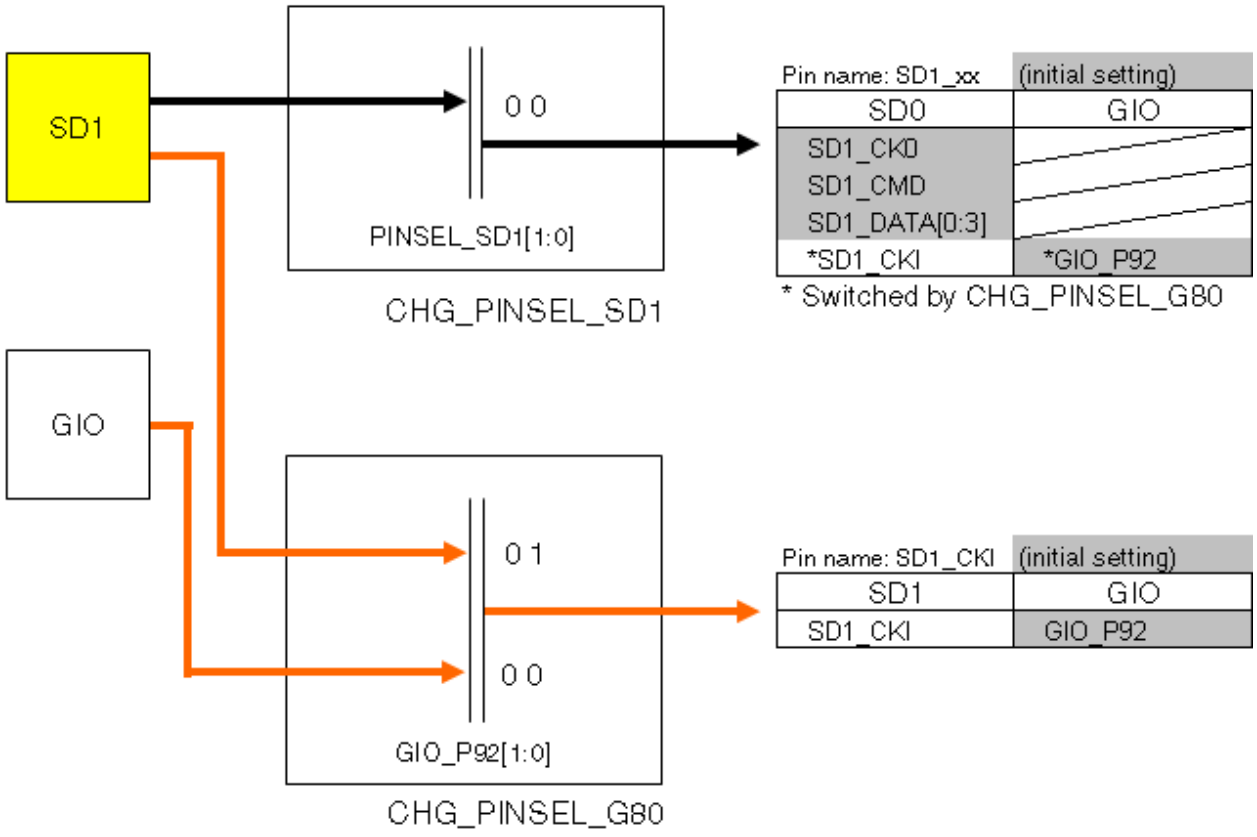
Figure 8-9. Selector Configuration of SD0 Interface Alternate-Function Pins



8.2.10 SD1 interface alternate-function pins

Figure 8-10 shows the selector configuration of SD1 interface pins.

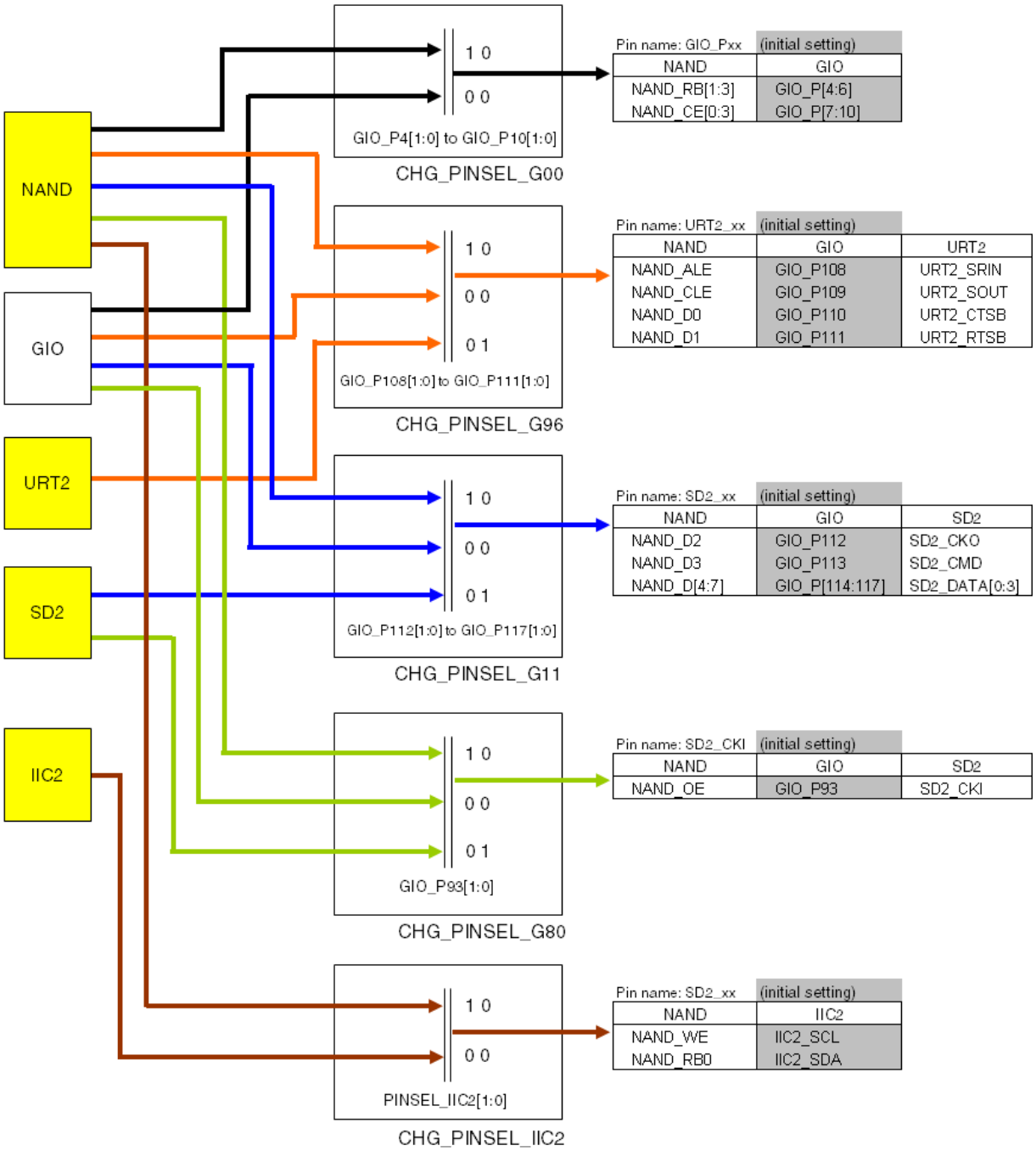
Figure 8-10. Selector Configuration of SD1 Interface Alternate-Function Pins



8.2.11 NAND/UART2/SD2/I²C2 interface alternate-function pins

Figure 8-11 shows the selector configuration of NAND Flash interface, UART2 interface, SD2 interface, and IIC2 interface pins.

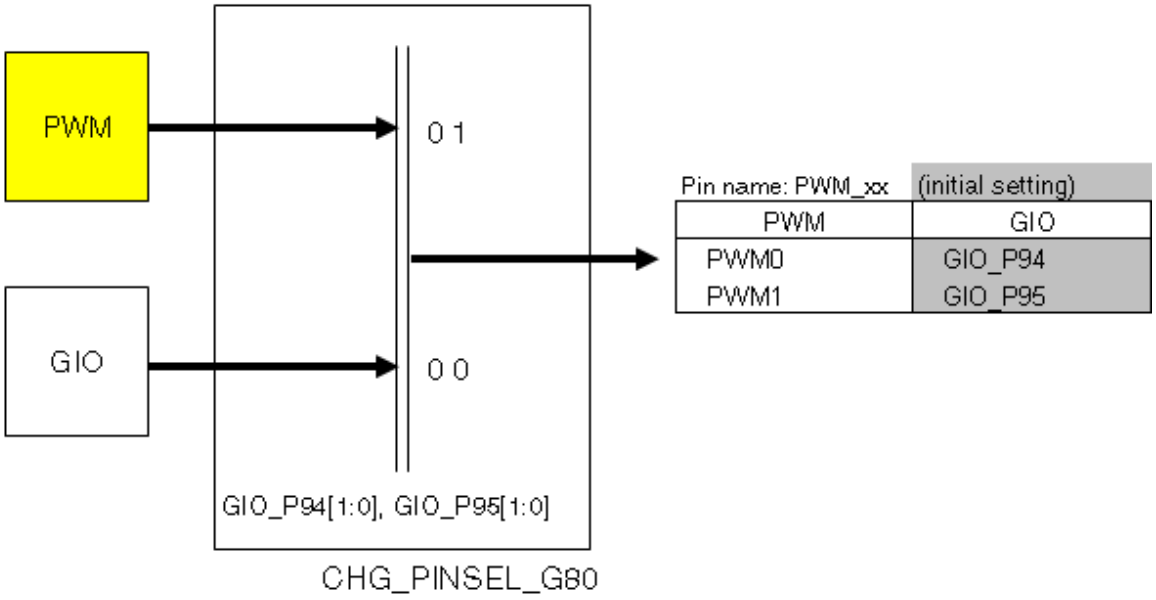
Figure 8-11. Selector Configuration of NAND/UART2/SD2/I²C2 Interface Alternate-Function Pins



8.2.12 PWM interface alternate-function pins

Figure 8-12 shows the selector configuration of PWM interface pins.

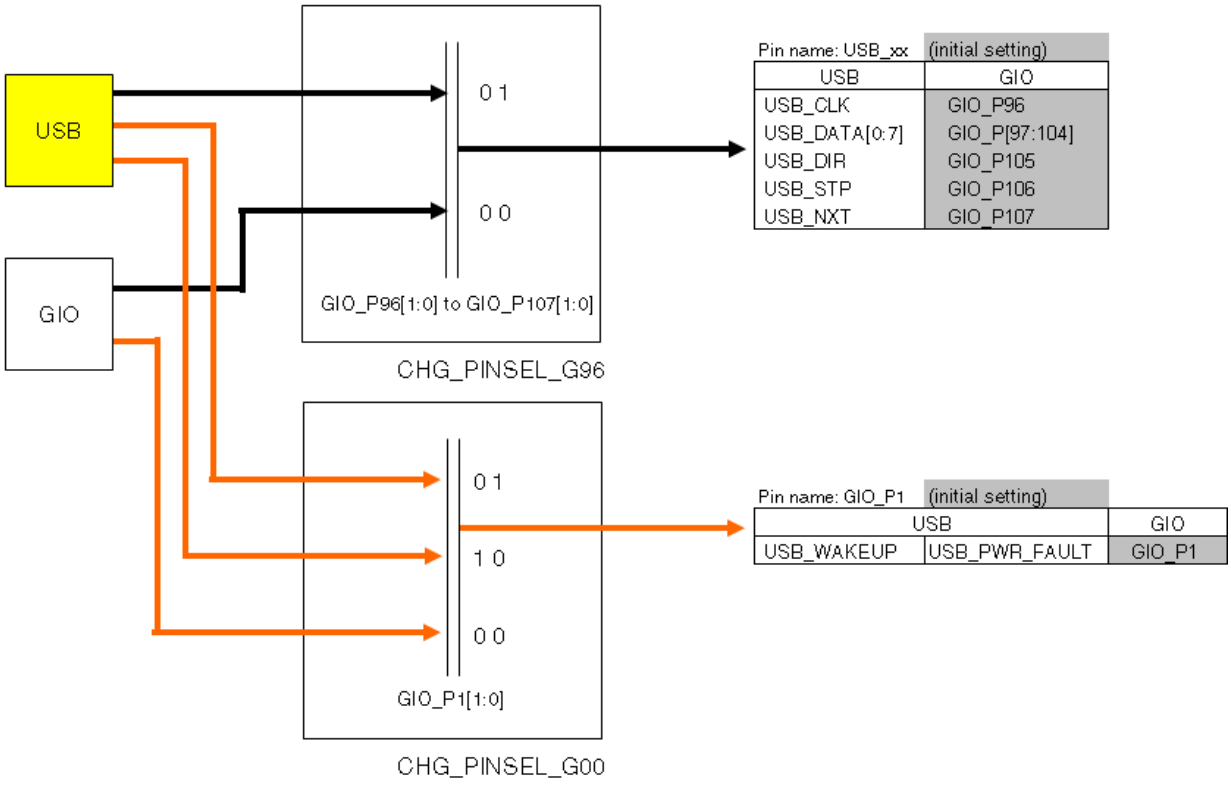
Figure 8-12. Selector Configuration of PWM Interface Alternate-Function Pins



8.2.13 USB interface alternate-function pins

Figure 8-13 shows the selector configuration of USB interface pins.

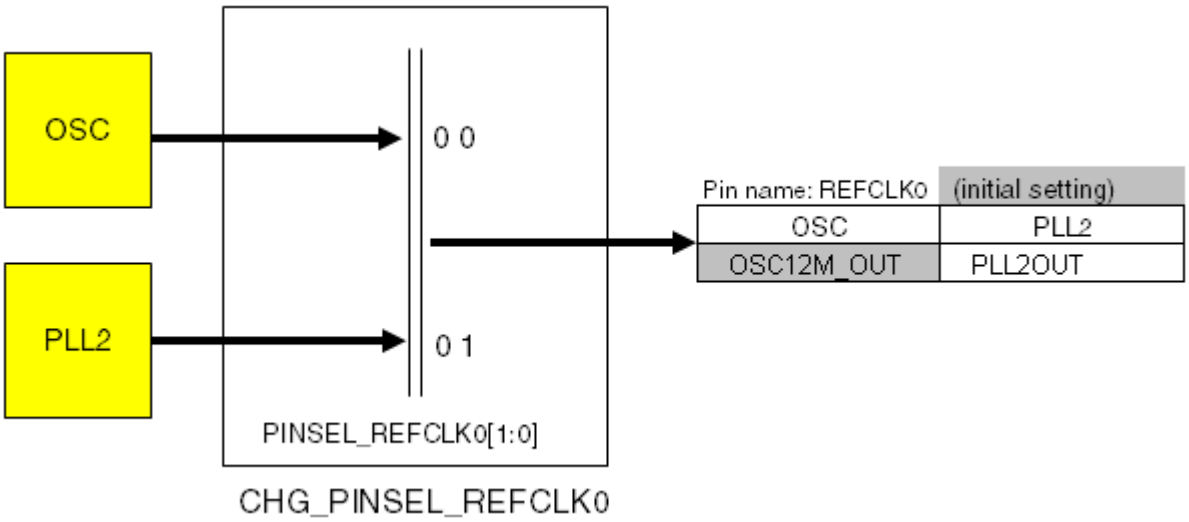
Figure 8-13. Selector Configuration of USB Interface Alternate-Function Pins



8.2.14 REFCLK0 pin

Figure 8-14 shows the selector configuration of the REFCLK0 pin.

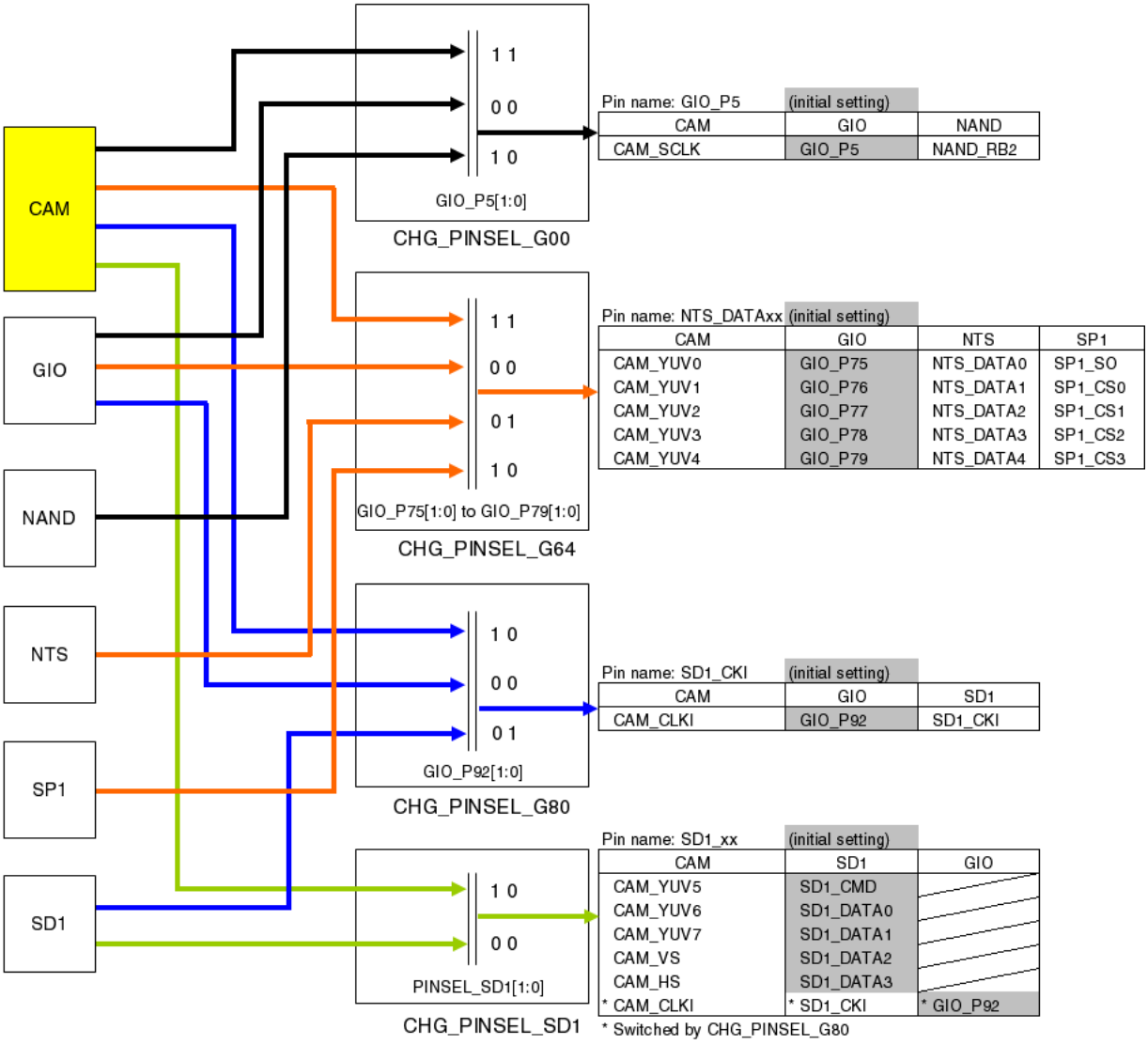
Figure 8-14. Selector Configuration of REFCLK0 Pin



8.2.15 Camera interface pins

Figure 8-15 shows the selector configuration of camera interface pins.

Figure 8-15. Selector Configuration of Camera Interface Pins



APPENDIX A REGISTERS

A.1 Registers

A.1.1 Asynchronous bus (AB0)

Base address: 2FFF_0000H

(1/3)

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Flash command start register	AB0_FLASHCOMSET	W	0000_0000H
0004H	Flash read data latch register	AB0_FLASHCOMLATCH	R	0000_0000H
0010H	Flash command (ADD0) setting register	AB0_FLASHCOMADD0	R/W	0000_0000H
0014H	Flash command (DATA0) setting register	AB0_FLASHCOMDATA0	R/W	0000_0000H
0018H	Flash command (ADD1) setting register	AB0_FLASHCOMADD1	R/W	0000_0000H
001CH	Flash command (DATA1) setting register	AB0_FLASHCOMDATA1	R/W	0000_0000H
0080H	Flash clock control register	AB0_FLASHCLKCTRL	R/W	0000_0001H
0084H	Flash read clock delay adjustment register	AB0_FLA_RCLK_DLY	RW	0000_1000H
0090H	WAIT pin status register	AB0_WAIT_STATUS	R	–
0100H	CS0 base address register	AB0_CS0BASEADD	R/W	0000_0000H
0104H	CS0 bit compare register	AB0_CS0BITCOMP	R/W	F000_0000H
0110H	CS1 base address register	AB0_CS1BASEADD	R/W	3FFF_0000H
0114H	CS1 bit compare register	AB0_CS1BITCOMP	R/W	FFFF_0000H
0120H	CS2 base address register	AB0_CS2BASEADD	R/W	3FFF_0000H
0124H	CS2 bit compare register	AB0_CS2BITCOMP	R/W	FFFF_0000H
0130H	CS3 base address register	AB0_CS3BASEADD	R/W	3FFF_0000H
0134H	CS3 bit compare register	AB0_CS3BITCOMP	R/W	FFFF_0000H
0140H-0154H	Reserved	–	–	–
0200H	CS0 wait control register	AB0_CS0WAITCTRL	R/W	000F_1F0FH
0204H	CS0 write wait control register	AB0_CS0WAITCTRL_W	R/W	000F_1F0FH
0208H	CS0 read mode register	AB0_CS0READCTRL	R/W	0000_0000H
020CH	CS0 wait mask register	AB0_CS0WAIT_MASK	R/W	0000_0000H
0210H	CS0 control register	AB0_CS0CONTROL	R/W	0001_0100H
0214H	CS0 read configuration register	AB0_CS0FLASHRCR	R/W	0000_D503H
0218H	CS0 write configuration register	AB0_CS0FLASHWCR	R/W	0000_0001H
0220H	CS1 wait control register	AB0_CS1WAITCTRL	R/W	000F_1F0FH
0224H	CS1 write wait control register	AB0_CS1WAITCTRL_W	R/W	000F_1F0FH
0228H	CS1 read mode register	AB0_CS1READCTRL	R/W	0000_0000H
022CH	CS1 wait mask register	AB0_CS1WAIT_MASK	R/W	0000_0000H
0230H	CS1 control register	AB0_CS1CONTROL	R/W	0001_0100H

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Address	Register Name	Register Symbol	R/W	After Reset
0234H	CS1 read configuration register	AB0_CS1FLASHRCR	R/W	0000_D503H
0238H	CS1 write configuration register	AB0_CS1FLASHWCR	R/W	0000_0001H
0240H	CS2 wait control register	AB0_CS2WAITCTRL	R/W	000F_1F0FH
0244H	CS2 write wait control register	AB0_CS2WAITCTRL_W	R/W	000F_1F0FH
0248H	CS2 read mode register	AB0_CS2READCTRL	R/W	0000_0000H
024CH	CS2 wait mask register	AB0_CS2WAIT_MASK	R/W	0000_0000H
0250H	CS2 control register	AB0_CS2CONTROL	R/W	0001_0100H
0254H	CS2 read configuration register	AB0_CS2FLASHRCR	R/W	0000_D503H
0258H	CS2 write configuration register	AB0_CS2FLASHWCR	R/W	0000_0001H
0260H	CS3 wait control register	AB0_CS3WAITCTRL	R/W	000F_1F0FH
0264H	CS3 write wait control register	AB0_CS3WAITCTRL_W	R/W	000F_1F0FH
0268H	CS3 read mode register	AB0_CS3READCTRL	R/W	0000_0000H
026CH	CS3 wait mask register	AB0_CS3WAIT_MASK	R/W	0000_0000H
0270H	CS3 control register	AB0_CS3CONTROL	R/W	0001_0100H
0274H	CS3 read configuration register	AB0_CS3FLASHRCR	R/W	0000_D503H
0278H	CS3 write configuration register	AB0_CS3FLASHWCR	R/W	0000_0001H
0280H-02B8H	Reserved	–	–	–
0300H	CS0 wait control register	AB0_CS0WAITCTRL2	R	000F_1F0FH
0304H	CS0 write wait control register	AB0_CS0WAITCTRL_W2	R	000F_1F0FH
0308H	CS0 read mode register	AB0_CS0READCTRL2	R	0000_0000H
030CH	CS0 wait mask register	AB0_CS0WAIT_MASK2	R	0000_0000H
0310H	CS0 control register	AB0_CS0CONTROL2	R	0001_0100H
0314H	CS0 read configuration register	AB0_CS0FLASHRCR2	R	0000_D503H
0318H	CS0 write configuration register	AB0_CS0FLASHWCR2	R	0000_0001H
0320H	CS1 wait control register	AB0_CS1WAITCTRL2	R	000F_1F0FH
0324H	CS1 write wait control register	AB0_CS1WAITCTRL_W2	R	000F_1F0FH
0328H	CS1 read mode register	AB0_CS1READCTRL2	R	0000_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
032CH	CS1 wait mask register	AB0_CS1WAIT_MASK2	R	0000_0000H
0330H	CS1 control register	AB0_CS1CONTROL2	R	0001_0100H
0334H	CS1 read configuration register	AB0_CS1FLASHRCR2	R	0000_D503H
0338H	CS1 write configuration register	AB0_CS1FLASHWCR2	R	0000_0001H
0340H	CS2 wait control register	AB0_CS2WAITCTRL2	R	000F_1F0FH
0344H	CS2 write wait control register	AB0_CS2WAITCTRL_W2	R	000F_1F0FH
0348H	CS2 read mode register	AB0_CS2READCTRL2	R	0000_0000H
034CH	CS2 wait mask register	AB0_CS2WAIT_MASK2	R	0000_0000H
0350H	CS2 control register	AB0_CS2CONTROL2	R	0001_0100H
0354H	CS2 read configuration register	AB0_CS2FLASHRCR2	R	0000_D503H
0358H	CS2 write configuration register	AB0_CS2FLASHWCR2	R	0000_0001H
0360H	CS3 wait control register	AB0_CS3WAITCTRL2	R	000F_1F0FH
0364H	CS3 write wait control register	AB0_CS3WAITCTRL_W2	R	000F_1F0FH
0368H	CS3 read mode register	AB0_CS3READCTRL2	R	0000_0000H
036CH	CS3 wait mask register	AB0_CS3WAIT_MASK2	R	0000_0000H
0370H	CS3 control register	AB0_CS3CONTROL2	R	0001_0100H
0374H	CS3 read configuration register	AB0_CS3FLASHRCR2	R	0000_D503H
0378H	CS3 write configuration register	AB0_CS3FLASHWCR2	R	0000_0001H
0380H-03B8H	Reserved	–	–	–

A.1.2 IPU (registers related to rotator functions)

Base address: 4008_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
0000H	Function setting register	ROT_MODE	R/W	0000_0000H
0004H	Frame selection register	ROT_FRAME	R/W	0000_0005H
0008H	Processing request register	ROT_REQ	W	0000_0000H
000CH	Processing status register	ROT_STATUS	R	0000_0000H
0010H-001CH	Reserved	–	–	–
0020H	Original image address addition value register	ROT_SRCSIZE	R/W	0000_0000H
0024H	Rotated image address addition value register	ROT_DSTSIZE	R/W	0000_0000H
0028H-002CH	Reserved	–	–	–
0030H	Original image Y address register (A frame)	ROT_SRCYADR_A	R/W	0000_0000H
0034H	Original image Y address register (B frame)	ROT_SRCYADR_B	R/W	0000_0000H
0038H	Original image Y address register (C frame)	ROT_SRCYADR_C	R/W	0000_0000H
003CH	Reserved	–	–	–
0040H	Rotated image Y address register (A frame)	ROT_DSTYADR_A	R/W	0000_0000H
0044H	Rotated image Y address register (B frame)	ROT_DSTYADR_B	R/W	0000_0000H
0048H	Rotated image Y address register (C frame)	ROT_DSTYADR_C	R/W	0000_0000H
004CH-005CH	Reserved	–	–	–
0060H	Original image UV address register (A frame)	ROT_SRCUVADR_A	R/W	0000_0000H
0064H	Original image UV address register (B frame)	ROT_SRCUVADR_B	R/W	0000_0000H
0068H	Original image UV address register (C frame)	ROT_SRCUVADR_C	R/W	0000_0000H
006CH	Reserved	–	–	–
0070H	Rotated image UV address register (A frame)	ROT_DSTUVADR_A	R/W	0000_0000H
0074H	Rotated image UV address register (B frame)	ROT_DSTUVADR_B	R/W	0000_0000H
0078H	Rotated image UV address register (C frame)	ROT_DSTUVADR_C	R/W	0000_0000H
007CH-008CH	Reserved	–	–	–
0090H	Original image horizontal size register	ROT_SRCHSIZE	R/W	0000_0010H
0094H-009CH	Reserved	–	–	–
00A0H	Original image vertical size register	ROT_SRCVSIZE	R/W	0000_0010H
00A4H-00ACH	Reserved	–	–	–
00B0H	Interrupt status register	ROT_INTSTATUS	R	0000_0000H
00B4H	Interrupt raw status register	ROT_INTRAWSTATUS	R	0000_0000H
00B8H	Interrupt enable set register	ROT_INTENSET	R/W	0000_0000H
00BCH	Interrupt enable clear register	ROT_INTENCLR	W	0000_0000H
00C0H	Interrupt source clear register	ROT_INTFFCLR	W	0000_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
00C4H	Error address register	ROT_ERRORADR	R/W	0000_0000H
00C8H	Image format register	ROT_FORMAT	R/W	0000_0000H
00CCH	Source image byte lane select register	ROT_SRCBYTE	R/W	0000_E4E4H
00D0H	Destination image byte lane select register	ROT_DSTBYTE	R/W	0000_E4E4H
00D4H	Original image V address register (A frame)	ROT_SRCVADR_A	R/W	0000_0000H
00D8H	Original image V address register (B frame)	ROT_SRCVADR_B	R/W	0000_0000H
00DCH	Original image V address register (C frame)	ROT_SRCVADR_C	R/W	0000_0000H
00E0H	Rotated image V address register (A frame)	ROT_DSTVADR_A	R/W	0000_0000H
00E4H	Rotated image V address register (B frame)	ROT_DSTVADR_B	R/W	0000_0000H
00E8H	Rotated image V address register (C frame)	ROT_DSTVADR_C	R/W	0000_0000H
00ECH	Register update reserve setting register	ROT_DUAL_FF	R/W	0000_0000H
00F0H	Source image byte lane select register (Y/UV planes divided)	ROT_SRCBYTE_CMP	R/W	0000_E4E4H
00F4H	Destination image byte lane select register (Y/UV planes divided)	ROT_DSTBYTE_CMP	R/W	0000_E4E4H
00F8H-FFFH	Reserved	–	–	–

A.1.3 DMA controller (DMAC)

Base address: 4009_0000H

(1) ACPU registers

(a) ACPU DMA control registers

Address	Register Name	Register Symbol	R/W	After Reset
0000H	ACPU DMA start control register	DMA_ARM_CONT	W	0000_0000H
0004H	ACPU DMA control status register	DMA_ARM_CONTSTATUS	R	0000_0000H
0008H	ACPU DMA end control register	DMA_ARM_END	W	0000_0000H
000CH-00FCH	Reserved	–	–	–

(b) ACPU interrupt registers

Address	Register Name	Register Symbol	R/W	After Reset
0800H	ARM/DSP interrupt output destination register (LCH0 to LCH3)	DMA_ARM_LCH0LCH3_INT_SEL	R/W	0000_0000H
0804H-0FFCH	Reserved	–	–	–
0100H	ACPU interrupt status register (LCH0 to LCH3)	DMA_ARM_PE0_LCH0LCH3_INT_CONT	R	0000_0000H
0104H	ACPU interrupt raw status register (LCH0 to LCH3)	DMA_ARM_PE0_LCH0LCH3_INT_RAW	R	0000_0000H
0108H	ACPU interrupt enable set register (LCH0 to LCH3)	DMA_ARM_PE0_LCH0LCH3_INT_ENABLE	R/W	0000_0000H
010CH	ACPU interrupt enable clear register (LCH0 to LCH3)	DMA_ARM_PE0_LCH0LCH3_INT_ENABLE_CL	W	0000_0000H
0110H	ACPU interrupt source clear register (LCH0 to LCH3)	DMA_ARM_PE0_LCH0LCH3_INT_REQ_CL	W	0000_0000H
0114H-03FCH	Reserved	–	–	–
0400H	DSP interrupt status register (LCH0 to LCH3)	DMA_ARM_DSP_LCH0LCH3_INT_CONT	R	0000_0000H
0404H	DSP interrupt raw status register (LCH0 to LCH3)	DMA_ARM_DSP_LCH0LCH3_INT_RAW	R	0000_0000H
0408H	DSP interrupt enable set register (LCH0 to LCH3)	DMA_ARM_DSP_LCH0LCH3_INT_ENABLE	R/W	0000_0000H
040CH	DSP interrupt enable clear register (LCH0 to LCH3)	DMA_ARM_DSP_LCH0LCH3_INT_ENABLE_CL	W	0000_0000H
0410H	DSP interrupt source clear register (LCH0 to LCH3)	DMA_ARM_DSP_LCH0LCH3_INT_REQ_CL	W	0000_0000H
0414H-07FCH	Reserved	–	–	–

(c) ACPU LCH0 setting registers (memory ↔ memory)

Address	Register Name	Register Symbol	R/W	After Reset
1000H	ACPU LCH0 source address register (start address)	DMA_ARM_LCH0_AADD	R/W	0000_0000H
1004H	ACPU LCH0 source address pointer register	DMA_ARM_LCH0_AADP	R	0000_0000H
1008H	ACPU LCH0 source address offset register	DMA_ARM_LCH0_AOFF	R/W	0000_0000H
100CH	Reserved	–	–	–
1010H	ACPU LCH0 source block count register	DMA_ARM_LCH0_ASIZE_COUNT	R/W	0000_0000H
1014H-101CH	Reserved	–	–	–
1020H	ACPU LCH0 destination address register (start address)	DMA_ARM_LCH0_BADD	R/W	0000_0000H
1024H	ACPU LCH0 destination address pointer register	DMA_ARM_LCH0_BADP	R	0000_0000H
1028H	ACPU LCH0 destination address offset register	DMA_ARM_LCH0_BOFF	R/W	0000_0000H
102CH	Reserved	–	–	–
1030H	ACPU LCH0 destination block count register	DMA_ARM_LCH0_BSIZE_COUNT	R/W	0000_0000H
1034H-103CH	Reserved	–	–	–
1040H	ACPU LCH0 length register	DMA_ARM_LCH0_LENG	R/W	0000_0000H
1044H	ACPU LCH0 read length count register	DMA_ARM_LCH0_LENG_RCOUNT	R	0000_0000H
1048H	ACPU LCH0 write length count register	DMA_ARM_LCH0_LENG_WCOUNT	R	0000_0000H
104CH	ACPU LCH0 block size register	DMA_ARM_LCH0_SIZE	R/W	0000_0000H
1050H	ACPU LCH0 mode register (read/write endian, repeat)	DMA_ARM_LCH0_MODE	R/W	E4E4_0000H
1054H-10FCH	Reserved	–	–	–

(d) ACPU LCH1 setting registers (memory ↔ memory)

Address	Register Name	Register Symbol	R/W	After Reset
1100H	ACPU LCH1 source address register (start address)	DMA_ARM_LCH1_AADD	R/W	0000_0000H
1104H	ACPU LCH1 source address pointer register	DMA_ARM_LCH1_AADP	R	0000_0000H
1108H	ACPU LCH1 source address offset register	DMA_ARM_LCH1_AOFF	R/W	0000_0000H
110CH	Reserved	–	–	–
1110H	ACPU LCH1 source block count register	DMA_ARM_LCH1_ASIZE_COUNT	R/W	0000_0000H
1114H-111CH	Reserved	–	–	–
1120H	ACPU LCH1 destination address register (start address)	DMA_ARM_LCH1_BADD	R/W	0000_0000H
1124H	ACPU LCH1 destination address pointer register	DMA_ARM_LCH1_BADP	R	0000_0000H
1128H	ACPU LCH1 destination address offset register	DMA_ARM_LCH1_BOFF	R/W	0000_0000H
112CH	Reserved	–	–	–
1130H	ACPU LCH1 destination block count register	DMA_ARM_LCH1_BSIZE_COUNT	R/W	0000_0000H
1134H-113CH	Reserved	–	–	–
1140H	ACPU LCH1 length register	DMA_ARM_LCH1_LENG	R/W	0000_0000H
1144H	ACPU LCH1 read length count register	DMA_ARM_LCH1_LENG_RCOUNT	R	0000_0000H
1148H	ACPU LCH1 write length count register	DMA_ARM_LCH1_LENG_WCOUNT	R	0000_0000H
114CH	ACPU LCH1 block size register	DMA_ARM_LCH1_SIZE	R/W	0000_0000H
1150H	ACPU LCH1 mode register (read/write endian, repeat)	DMA_ARM_LCH1_MODE	R/W	E4E4_0000H
1154H-11FCH	Reserved	–	–	–

(e) ACPU LCH2 setting registers (memory ↔ memory)

Address	Register Name	Register Symbol	R/W	After Reset
1200H	ACPU LCH2 source address register (start address)	DMA_ARM_LCH2_AADD	R/W	0000_0000H
1204H	ACPU LCH2 source address pointer register	DMA_ARM_LCH2_AADP	R	0000_0000H
1208H	ACPU LCH2 source address offset register	DMA_ARM_LCH2_AOFF	R/W	0000_0000H
120CH	Reserved	–	–	–
1210H	ACPU LCH2 source block count register	DMA_ARM_LCH2_ASIZE_COUNT	R/W	0000_0000H
1214H-121CH	Reserved	–	–	–
1220H	ACPU LCH2 destination address register (start address)	DMA_ARM_LCH2_BADD	R/W	0000_0000H
1224H	ACPU LCH2 destination address pointer register	DMA_ARM_LCH2_BADP	R	0000_0000H
1228H	ACPU LCH2 destination address offset register	DMA_ARM_LCH2_BOFF	R/W	0000_0000H
122CH	Reserved	–	–	–
1230H	ACPU LCH2 destination block count register	DMA_ARM_LCH2_BSIZE_COUNT	R/W	0000_0000H
1234H-123CH	Reserved	–	–	–
1240H	ACPU LCH2 length register	DMA_ARM_LCH2_LENG	R/W	0000_0000H
1244H	ACPU LCH2 read length count register	DMA_ARM_LCH2_LENG_RCOUNT	R	0000_0000H
1248H	ACPU LCH2 write length count register	DMA_ARM_LCH2_LENG_WCOUNT	R	0000_0000H
124CH	ACPU LCH2 block size register	DMA_ARM_LCH2_SIZE	R/W	0000_0000H
1250H	ACPU LCH2 mode register (read/write endian, repeat)	DMA_ARM_LCH2_MODE	R/W	E4E4_0000H
1254H-12FCH	Reserved	–	–	–

(f) ACPU LCH3 setting registers (memory ↔ memory)

Address	Register Name	Register Symbol	R/W	After Reset
1300H	ACPU LCH3 source address register (start address)	DMA_ARM_LCH3_AADD	R/W	0000_0000H
1304H	ACPU LCH3 source address pointer register	DMA_ARM_LCH3_AADP	R	0000_0000H
1308H	ACPU LCH3 source address offset register	DMA_ARM_LCH3_AOFF	R/W	0000_0000H
130CH	Reserved	–	–	–
1310H	ACPU LCH3 source block count register	DMA_ARM_LCH3_ASIZE_COUNT	R/W	0000_0000H
1314H-131CH	Reserved	–	–	–
1320H	ACPU LCH3 destination address register (start address)	DMA_ARM_LCH3_BADD	R/W	0000_0000H
1324H	ACPU LCH3 destination address pointer register	DMA_ARM_LCH3_BADP	R	0000_0000H
1328H	ACPU LCH3 destination address offset register	DMA_ARM_LCH3_BOFF	R/W	0000_0000H
132CH	Reserved	–	–	–
1330H	ACPU LCH3 destination block count register	DMA_ARM_LCH3_BSIZE_COUNT	R/W	0000_0000H
1334H-133CH	Reserved	–	–	–
1340H	ACPU LCH3 length register	DMA_ARM_LCH3_LENG	R/W	0000_0000H
1344H	ACPU LCH3 read length count register	DMA_ARM_LCH3_LENG_RCOUNT	R	0000_0000H
1348H	ACPU LCH3 write length count register	DMA_ARM_LCH3_LENG_WCOUNT	R	0000_0000H
134CH	ACPU LCH3 block size register	DMA_ARM_LCH3_SIZE	R/W	0000_0000H
1350H	ACPU LCH3 mode register (read endian, repeat)	DMA_ARM_LCH3_MODE	R/W	E4E4_0000H
1354H-13FCH	Reserved	–	–	–

(2) M2P (memory-to-peripheral transfer) registers

LCH6 to LCH8 and LCH11 are reserved channels, so there are no corresponding register bits.

(a) M2P DMA control registers

Address	Register Name	Register Symbol	R/W	After Reset
4000H	M2P DMA start control register	DMA_M2P_CONT	W	0000_0000H
4004H	M2P DMA control status register	DMA_M2P_CONTSTATUS	R	0000_0000H
4008H	M2P DMA end control register	DMA_M2P_END	W	0000_0000H
400CH-40FCH	Reserved	–	–	–

(b) M2P interrupt registers

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Address	Register Name	Register Symbol	R/W	After Reset
4800H	M2P interrupt output destination register (LCH0 to LCH14)	DMA_M2P_LCH0LCH14_INT_SEL	R/W	0000_0000H
4804H-4FFCH	Reserved	–	–	–
4100H	ACPU interrupt status register (LCH0 to LCH3)	DMA_M2P_PE0_LCH0LCH3_INT_CONT	R	0000_0000H
4104H	ACPU interrupt raw status register (LCH0 to LCH3)	DMA_M2P_PE0_LCH0LCH3_INT_RAW	R	0000_0000H
4108H	ACPU interrupt enable set register (LCH0 to LCH3)	DMA_M2P_PE0_LCH0LCH3_INT_ENABLE	R/W	0000_0000H
410CH	ACPU interrupt enable clear register (LCH0 to LCH3)	DMA_M2P_PE0_LCH0LCH3_INT_ENABLE_CL	W	0000_0000H
4110H	ACPU interrupt source clear register (LCH0 to LCH3)	DMA_M2P_PE0_LCH0LCH3_INT_REQ_CL	W	0000_0000H
4114H-411CH	Reserved	–	–	–
4120H	ACPU interrupt status register (LCH4 and LCH5)	DMA_M2P_PE0_LCH4LCH5_INT_CONT	R	0000_0000H
4124H	ACPU interrupt raw status register (LCH4 and LCH5)	DMA_M2P_PE0_LCH4LCH5_INT_RAW	R	0000_0000H
4128H	ACPU interrupt enable set register (LCH4 and LCH5)	DMA_M2P_PE0_LCH4LCH5_INT_ENABLE	R/W	0000_0000H
412CH	ACPU interrupt enable clear register (LCH4 and LCH5)	DMA_M2P_PE0_LCH4LCH5_INT_ENABLE_CL	W	0000_0000H
4130H	ACPU interrupt source clear register (LCH4 and LCH5)	DMA_M2P_PE0_LCH4LCH5_INT_REQ_CL	W	0000_0000H
4134H-413CH	Reserved	–	–	–
4140H	ACPU interrupt status register (LCH9 and LCH10)	DMA_M2P_PE0_LCH9LCH10_INT_CONT	R	0000_0000H
4144H	ACPU interrupt raw status register (LCH9 and LCH10)	DMA_M2P_PE0_LCH9LCH10_INT_RAW	R	0000_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
4148H	ACPU interrupt enable set register (LCH9 and LCH10)	DMA_M2P_PE0_LCH9LCH10_INT_ENABLE	R/W	0000_0000H
414CH	ACPU interrupt enable clear register (LCH9 and LCH10)	DMA_M2P_PE0_LCH9LCH10_INT_ENABLE_CL	W	0000_0000H
4150H	ACPU interrupt source clear register (LCH9 and LCH10)	DMA_M2P_PE0_LCH9LCH10_INT_REQ_CL	W	0000_0000H
4154H-415CH	Reserved	–	–	–
4160H	ACPU interrupt status register (LCH12 to LCH14)	DMA_M2P_PE0_LCH12LCH14_INT_CONT	R	0000_0000H
4164H	ACPU interrupt raw status register (LCH12 to LCH14)	DMA_M2P_PE0_LCH12LCH14_INT_RAW	R	0000_0000H
4168H	ACPU interrupt enable set register (LCH12 to LCH14)	DMA_M2P_PE0_LCH12LCH14_INT_ENABLE	R/W	0000_0000H
416CH	ACPU interrupt enable clear register (LCH12 to LCH14)	DMA_M2P_PE0_LCH12LCH14_INT_ENABLE_CL	W	0000_0000H
4170H	ACPU interrupt source clear register (LCH12 to LCH14)	DMA_M2P_PE0_LCH12LCH14_INT_REQ_CL	W	0000_0000H
4174H-43FCH	Reserved	–	–	–
4400H	DSP interrupt status register (LCH0 to LCH3)	DMA_M2P_DSP_LCH0LCH3_INT_CONT	R	0000_0000H
4404H	DSP interrupt raw status register (LCH0 to LCH3)	DMA_M2P_DSP_LCH0LCH3_INT_RAW	R	0000_0000H
4408H	DSP interrupt enable set register (LCH0 to LCH3)	DMA_M2P_DSP_LCH0LCH3_INT_ENABLE	R/W	0000_0000H
440CH	DSP interrupt enable clear register (LCH0 to LCH3)	DMA_M2P_DSP_LCH0LCH3_INT_ENABLE_CL	W	0000_0000H
4410H	DSP interrupt source clear register (LCH0 to LCH3)	DMA_M2P_DSP_LCH0LCH3_INT_REQ_CL	W	0000_0000H
4414H-441CH	Reserved	–	–	–
4420H	DSP interrupt status register (LCH4 and LCH5)	DMA_M2P_DSP_LCH4LCH5_INT_CONT	R	0000_0000H
4424H	DSP interrupt raw status register (LCH4 and LCH5)	DMA_M2P_DSP_LCH4LCH5_INT_RAW	R	0000_0000H
4428H	DSP interrupt enable set register (LCH4 and LCH5)	DMA_M2P_DSP_LCH4LCH5_INT_ENABLE	R/W	0000_0000H
442CH	DSP interrupt enable clear register (LCH4 and LCH5)	DMA_M2P_DSP_LCH4LCH5_INT_ENABLE_CL	W	0000_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
4430H	DSP interrupt source clear register (LCH4 and LCH5)	DMA_M2P_DSP_LCH4LCH5_INT_REQ_CL	W	0000_0000H
4434H-443CH	Reserved	–	–	–
4440H	DSP interrupt status register (LCH9 and LCH10)	DMA_M2P_DSP_LCH9LCH10_INT_CONT	R	0000_0000H
4444H	DSP interrupt raw status register (LCH9 and LCH10)	DMA_M2P_DSP_LCH9LCH10_INT_RAW	R	0000_0000H
4448H	DSP interrupt enable set register (LCH9 and LCH10)	DMA_M2P_DSP_LCH9LCH10_INT_ENABLE	R/W	0000_0000H
444CH	DSP interrupt enable clear register (LCH9 and LCH10)	DMA_M2P_DSP_LCH9LCH10_INT_ENABLE_CL	W	0000_0000H
4450H	DSP interrupt source clear register (LCH9 and LCH10)	DMA_M2P_DSP_LCH9LCH10_INT_REQ_CL	W	0000_0000H
4454H-445CH	Reserved	–	–	–
4460H	DSP interrupt status register (LCH12 to LCH14)	DMA_M2P_DSP_LCH12LCH14_INT_CONT	R	0000_0000H
4464H	DSP interrupt raw status register (LCH12 to LCH14)	DMA_M2P_DSP_LCH12LCH14_INT_RAW	R	0000_0000H
4468H	DSP interrupt enable set register (LCH12 to LCH14)	DMA_M2P_DSP_LCH12LCH14_INT_ENABLE	R/W	0000_0000H
446CH	DSP interrupt enable clear register (LCH12 to LCH14)	DMA_M2P_DSP_LCH12LCH14_INT_ENABLE_CL	W	0000_0000H
4470H	DSP interrupt source clear register (LCH12 to LCH14)	DMA_M2P_DSP_LCH12LCH14_INT_REQ_CL	W	0000_0000H
4474H-47FCH	Reserved	–	–	–

(c) M2P LCH0 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
5000H	M2P LCH0 source address register (start address)	DMA_M2P_LCH0_AADD	R/W	0000_0000H
5004H	M2P LCH0 source address pointer register	DMA_M2P_LCH0_AADP	R	0000_0000H
5008H	M2P LCH0 source address offset register	DMA_M2P_LCH0_AOFF	R/W	0000_0000H
500CH	M2P LCH0 source block size register	DMA_M2P_LCH0_ASIZE	R/W	0000_0000H
5010H	M2P LCH0 source block count register	DMA_M2P_LCH0_ASIZE_COUNT	R/W	0000_0000H
5014H-501CH	Reserved	–	–	–
5020H	M2P LCH0 destination address register	DMA_M2P_LCH0_BADD	R/W	0000_0000H
5024H-503CH	Reserved	–	–	–
5040H	M2P LCH0 length register	DMA_M2P_LCH0_LENG	R/W	0000_0000H
5044H	M2P LCH0 read length count register	DMA_M2P_LCH0_LENG_RCOUNT	R	0000_0000H
5048H	M2P LCH0 write length count register	DMA_M2P_LCH0_LENG_WCOUNT	R	0000_0000H
504CH	Reserved	–	–	–
5050H	M2P LCH0 mode register (timer setting, bit width, read/write endian, repeat)	DMA_M2P_LCH0_MODE	R/W	E4E4_0000H
5054H	M2P LCH0 timer register	DMA_M2P_LCH0_TIME	R/W	0000_0000H
5058H	M2P LCH0 timer count register	DMA_M2P_LCH0_TIME_COUNT	R	0000_0000H
505CH-50FCH	Reserved	–	–	–

(d) M2P LCH1 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
5100H	M2P LCH1 source address register (start address)	DMA_M2P_LCH1_AADD	R/W	0000_0000H
5104H	M2P LCH1 source address pointer register	DMA_M2P_LCH1_AADP	R	0000_0000H
5108H	M2P LCH1 source address offset register	DMA_M2P_LCH1_AOFF	R/W	0000_0000H
510CH	M2P LCH1 source block size register	DMA_M2P_LCH1_ASIZE	R/W	0000_0000H
5110H	M2P LCH1 source block count register	DMA_M2P_LCH1_ASIZE_COUNT	R/W	0000_0000H
5114H-511CH	Reserved	–	–	–
5120H	M2P LCH1 destination address register	DMA_M2P_LCH1_BADD	R/W	0000_0000H
5124H-513CH	Reserved	–	–	–
5140H	M2P LCH1 length register	DMA_M2P_LCH1_LENG	R/W	0000_0000H
5144H	M2P LCH1 read length count register	DMA_M2P_LCH1_LENG_RCOUNT	R	0000_0000H
5148H	M2P LCH1 write length count register	DMA_M2P_LCH1_LENG_WCOUNT	R	0000_0000H
514CH	Reserved	–	–	–
5150H	M2P LCH1 mode register (timer setting, bit width, read/write endian, repeat)	DMA_M2P_LCH1_MODE	R/W	E4E4_0000H
5154H	M2P LCH1 timer register	DMA_M2P_LCH1_TIME	R/W	0000_0000H
5158H	M2P LCH1 timer count register	DMA_M2P_LCH1_TIME_COUNT	R	0000_0000H
515CH-51FCH	Reserved	–	–	–

(e) M2P LCH2 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
5200H	M2P LCH2 source address register (start address)	DMA_M2P_LCH2_AADD	R/W	0000_0000H
5204H	M2P LCH2 source address pointer register	DMA_M2P_LCH2_AADP	R	0000_0000H
5208H	M2P LCH2 source address offset register	DMA_M2P_LCH2_AOFF	R/W	0000_0000H
520CH	M2P LCH2 source block size register	DMA_M2P_LCH2_ASIZE	R/W	0000_0000H
5210H	M2P LCH2 source block count register	DMA_M2P_LCH2_ASIZE_COUNT	R/W	0000_0000H
5214H-521CH	Reserved	–	–	–
5220H	M2P LCH2 destination address register	DMA_M2P_LCH2_BADD	R/W	0000_0000H
5224H-523CH	Reserved	–	–	–
5240H	M2P LCH2 length register	DMA_M2P_LCH2_LENG	R/W	0000_0000H
5244H	M2P LCH2 read length count register	DMA_M2P_LCH2_LENG_RCOUNT	R	0000_0000H
5248H	M2P LCH2 write length count register	DMA_M2P_LCH2_LENG_WCOUNT	R	0000_0000H
524CH	Reserved	–	–	–
5250H	M2P LCH2 mode register (timer setting, bit width, read/write endian, repeat)	DMA_M2P_LCH2_MODE	R/W	E4E4_0000H
5254H	M2P LCH2 timer register	DMA_M2P_LCH2_TIME	R/W	0000_0000H
5258H	M2P LCH2 timer count register	DMA_M2P_LCH2_TIME_COUNT	R	0000_0000H
525CH-52FCH	Reserved	–	–	–

(f) M2P LCH3 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
5300H	M2P LCH3 source address register (start address)	DMA_M2P_LCH3_AADD	R/W	0000_0000H
5304H	M2P LCH3 source address pointer register	DMA_M2P_LCH3_AADP	R	0000_0000H
5308H	M2P LCH3 source address offset register	DMA_M2P_LCH3_AOFF	R/W	0000_0000H
530CH	M2P LCH3 source block size register	DMA_M2P_LCH3_ASIZE	R/W	0000_0000H
5310H	M2P LCH3 source block count register	DMA_M2P_LCH3_ASIZE_COUNT	R/W	0000_0000H
5314H-531CH	Reserved	–	–	–
5320H	M2P LCH3 destination address register	DMA_M2P_LCH3_BADD	R/W	0000_0000H
5324H-4533CH	Reserved	–	–	–
5340H	M2P LCH3 length register	DMA_M2P_LCH3_LENG	R/W	0000_0000H
5344H	M2P LCH3 read length count register	DMA_M2P_LCH3_LENG_RCOUNT	R	0000_0000H
5348H	M2P LCH3 write length count register	DMA_M2P_LCH3_LENG_WCOUNT	R	0000_0000H
534CH	Reserved	–	–	–
5350H	M2P LCH3 mode register (bit width, read/write endian, repeat)	DMA_M2P_LCH3_MODE	R/W	E4E4_0000H
5354H-53FCH	Reserved	–	–	–

(g) M2P LCH4 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
5400H	M2P LCH4 source address register (start address)	DMA_M2P_LCH4_AADD	R/W	0000_0000H
5404H	M2P LCH4 source address pointer register	DMA_M2P_LCH4_AADP	R	0000_0000H
5408H	M2P LCH4 source address offset register	DMA_M2P_LCH4_AOFF	R/W	0000_0000H
540CH	M2P LCH4 source block size register	DMA_M2P_LCH4_ASIZE	R/W	0000_0000H
5410H	M2P LCH4 source block count register	DMA_M2P_LCH4_ASIZE_COUNT	R/W	0000_0000H
5414H-541CH	Reserved	–	–	–
5420H	M2P LCH4 destination address register	DMA_M2P_LCH4_BADD	R/W	0000_0000H
5424H-543CH	Reserved	–	–	–
5440H	M2P LCH4 length register	DMA_M2P_LCH4_LENG	R/W	0000_0000H
5444H	M2P LCH4 read length count register	DMA_M2P_LCH4_LENG_RCOUNT	R	0000_0000H
5448H	M2P LCH4 write length count register	DMA_M2P_LCH4_LENG_WCOUNT	R	0000_0000H
544CH	Reserved	–	–	–
5450H	M2P LCH4 mode register (bit width, read/write endian, repeat)	DMA_M2P_LCH4_MODE	R/W	E4E4_0000H
5454H-54FCH	Reserved	–	–	–

(h) M2P LCH5 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
5500H	M2P LCH5 source address register (start address)	DMA_M2P_LCH5_AADD	R/W	0000_0000H
5504H	M2P LCH5 source address pointer register	DMA_M2P_LCH5_AADP	R	0000_0000H
5508H	M2P LCH5 source address offset register	DMA_M2P_LCH5_AOFF	R/W	0000_0000H
550CH	M2P LCH5 source block size register	DMA_M2P_LCH5_ASIZE	R/W	0000_0000H
5510H	M2P LCH5 source block count register	DMA_M2P_LCH5_ASIZE_COUNT	R/W	0000_0000H
5514H-551CH	Reserved	–	–	–
5520H	M2P LCH5 destination address register	DMA_M2P_LCH5_BADD	R/W	0000_0000H
5524H-553CH	Reserved	–	–	–
5540H	M2P LCH5 length register	DMA_M2P_LCH5_LENG	R/W	0000_0000H
5544H	M2P LCH5 read length count register	DMA_M2P_LCH5_LENG_RCOUNT	R	0000_0000H
5548H	M2P LCH5 write length count register	DMA_M2P_LCH5_LENG_WCOUNT	R	0000_0000H
554CH	Reserved	–	–	–
5550H	M2P LCH5 mode register (bit width, read/write endian, repeat)	DMA_M2P_LCH5_MODE	R/W	E4E4_0000H
5554H-56FCH	Reserved	–	–	–

(i) M2P LCH9 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
5900H	M2P LCH9 source address register (start address)	DMA_M2P_LCH9_AADD	R/W	0000_0000H
5904H	M2P LCH9 source address pointer register	DMA_M2P_LCH9_AADP	R	0000_0000H
5908H	M2P LCH9 source address offset register	DMA_M2P_LCH9_AOFF	R/W	0000_0000H
590CH	M2P LCH9 source block size register	DMA_M2P_LCH9_ASIZE	R/W	0000_0000H
5910H	M2P LCH9 source block count register	DMA_M2P_LCH9_ASIZE_COUNT	R/W	0000_0000H
5914H-591CH	Reserved	–	–	–
5920H	M2P LCH9 destination address register	DMA_M2P_LCH9_BADD	R/W	0000_0000H
5924H-593CH	Reserved	–	–	–
5940H	M2P LCH9 length register	DMA_M2P_LCH9_LENG	R/W	0000_0000H
5944H	M2P LCH9 read length count register	DMA_M2P_LCH9_LENG_RCOUNT	R	0000_0000H
5948H	M2P LCH9 write length count register	DMA_M2P_LCH9_LENG_WCOUNT	R	0000_0000H
594CH	Reserved	–	–	–
5950H	M2P LCH9 mode register (bit width, read/write endian, repeat)	DMA_M2P_LCH9_MODE	R/W	E4E4_0000H
5954H-59FCH	Reserved	–	–	–

(j) M2P LCH10 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
5A00H	M2P LCH10 source address register (start address)	DMA_M2P_LCH10_AADD	R/W	0000_0000H
5A04H	M2P LCH10 source address pointer register	DMA_M2P_LCH10_AADP	R	0000_0000H
5A08H	M2P LCH10 source address offset register	DMA_M2P_LCH10_AOFF	R/W	0000_0000H
5A0CH	M2P LCH10 source block size register	DMA_M2P_LCH10_ASIZE	R/W	0000_0000H
5A10H	M2P LCH10 source block count register	DMA_M2P_LCH10_ASIZE_COUNT	R/W	0000_0000H
5A14H-5A1CH	Reserved	–	–	–
5A20H	M2P LCH10 destination address register	DMA_M2P_LCH10_BADD	R/W	0000_0000H
5A24H-5A3CH	Reserved	–	–	–
5A40H	M2P LCH10 length register	DMA_M2P_LCH10_LENG	R/W	0000_0000H
5A44H	M2P LCH10 read length count register	DMA_M2P_LCH10_LENG_RCOUNT	R	0000_0000H
5A48H	M2P LCH10 write length count register	DMA_M2P_LCH10_LENG_WCOUNT	R	0000_0000H
5A4CH	Reserved	–	–	–
5A50H	M2P LCH10 mode register (bit width, read/write endian, repeat)	DMA_M2P_LCH10_MODE	R/W	E4E4_0000H
5A54H-5AFCH	Reserved	–	–	–

(k) M2P LCH12 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
5C00H	M2P LCH12 source address register (start address)	DMA_M2P_LCH12_AADD	R/W	0000_0000H
5C04H	M2P LCH12 source address pointer register	DMA_M2P_LCH12_AADP	R	0000_0000H
5C08H	M2P LCH12 source address offset register	DMA_M2P_LCH12_AOFF	R/W	0000_0000H
5C0CH	M2P LCH12 source block size register	DMA_M2P_LCH12_ASIZE	R/W	0000_0000H
5C10H	M2P LCH12 source block count register	DMA_M2P_LCH12_ASIZE_COUNT	R/W	0000_0000H
5C14H-5C1CH	Reserved	–	–	–
5C20H	M2P LCH12 destination address register	DMA_M2P_LCH12_BADD	R/W	0000_0000H
5C24H-5C3CH	Reserved	–	–	–
5C40H	M2P LCH12 length register	DMA_M2P_LCH12_LENG	R/W	0000_0000H
5C44H	M2P LCH12 read length count register	DMA_M2P_LCH12_LENG_RCOUNT	R	0000_0000H
5C48H	M2P LCH12 write length count register	DMA_M2P_LCH12_LENG_WCOUNT	R	0000_0000H
5C4CH	Reserved	–	–	–
5C50H	M2P LCH12 mode register (bit width, read/write endian, repeat)	DMA_M2P_LCH12_MODE	R/W	E4E4_0000H
5C54H-5CFCH	Reserved	–	–	–

(l) M2P LCH13 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
5D00H	M2P LCH13 source address register (start address)	DMA_M2P_LCH13_AADD	R/W	0000_0000H
5D04H	M2P LCH13 source address pointer register	DMA_M2P_LCH13_AADP	R	0000_0000H
5D08H	M2P LCH13 source address offset register	DMA_M2P_LCH13_AOFF	R/W	0000_0000H
5D0CH	M2P LCH13 source block size register	DMA_M2P_LCH13_ASIZE	R/W	0000_0000H
5D10H	M2P LCH13 source block count register	DMA_M2P_LCH13_ASIZE_COUNT	R/W	0000_0000H
5D14H-5D1CH	Reserved	–	–	–
5D20H	M2P LCH13 destination address register	DMA_M2P_LCH13_BADD	R/W	0000_0000H
5D24H-5D3CH	Reserved	–	–	–
5D40H	M2P LCH13 length register	DMA_M2P_LCH13_LENG	R/W	0000_0000H
5D44H	M2P LCH13 read length count register	DMA_M2P_LCH13_LENG_RCOUNT	R	0000_0000H
5D48H	M2P LCH13 write length count register	DMA_M2P_LCH13_LENG_WCOUNT	R	0000_0000H
5D4CH	Reserved	–	–	–
5D50H	M2P LCH13 mode register (bit width, read/write endian, repeat)	DMA_M2P_LCH13_MODE	R/W	E4E4_0000H
5D54H-5DFCH	Reserved	–	–	–

(m) M2P LCH14 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
5E00H	M2P LCH14 source address register (start address)	DMA_M2P_LCH14_AADD	R/W	0000_0000H
5E04H	M2P LCH14 source address pointer register	DMA_M2P_LCH14_AADP	R	0000_0000H
5E08H	M2P LCH14 source address offset register	DMA_M2P_LCH14_AOFF	R/W	0000_0000H
5E0CH	M2P LCH14 source block size register	DMA_M2P_LCH14_ASIZE	R/W	0000_0000H
5E10H	M2P LCH14 source block count register	DMA_M2P_LCH14_ASIZE_COUNT	R/W	0000_0000H
5E14H-5E1CH	Reserved	–	–	–
5E20H	M2P LCH14 destination address register	DMA_M2P_LCH14_BADD	R/W	0000_0000H
5E24H-5E3CH	Reserved	–	–	–
5E40H	M2P LCH14 length register	DMA_M2P_LCH14_LENG	R/W	0000_0000H
5E44H	M2P LCH14 read length count register	DMA_M2P_LCH14_LENG_RCOUNT	R	0000_0000H
5E48H	M2P LCH14 write length count register	DMA_M2P_LCH14_LENG_WCOUNT	R	0000_0000H
5E4CH	Reserved	–	–	–
5E50H	M2P LCH14 mode register (bit width, read/write endian, repeat)	DMA_M2P_LCH14_MODE	R/W	E4E4_0000H
5E54H-5EFCH	Reserved	–	–	–

(3) P2M (peripheral-to-memory transfer) registers

LCH6 to LCH8 and LCH11 are reserved channels, so there are no corresponding register bits.

(a) P2M DMA control registers

Address	Register Name	Register Symbol	R/W	After Reset
6000H	P2M DMA start control register	DMA_P2M_CONT	W	0000_0000H
6004H	P2M DMA control status register	DMA_P2M_CONTSTATUS	R	0000_0000H
6008H	P2M DMA end control register	DMA_P2M_END	W	0000_0000H
600CH-60FCH	Reserved	–	–	–

(b) P2M interrupt registers

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Address	Register Name	Register Symbol	R/W	After Reset
6800H	P2M interrupt output destination register (LCH0 to LCH14)	DMA_P2M_LCH0LCH14_INT_SEL	R/W	0000_0000H
6804H-6FFCH	Reserved	–	–	–
6100H	ACPU interrupt status register (LCH0 to LCH3)	DMA_P2M_PE0_LCH0LCH3_INT_CONT	R	0000_0000H
6104H	ACPU interrupt raw status register (LCH0 to LCH3)	DMA_P2M_PE0_LCH0LCH3_INT_RAW	R	0000_0000H
6108H	ACPU interrupt enable set register (LCH0 to LCH3)	DMA_P2M_PE0_LCH0LCH3_INT_ENABLE	R/W	0000_0000H
610CH	ACPU interrupt enable clear register (LCH0 to LCH3)	DMA_P2M_PE0_LCH0LCH3_INT_ENABLE_CL	W	0000_0000H
6110H	ACPU interrupt source clear register (LCH0 to LCH3)	DMA_P2M_PE0_LCH0LCH3_INT_REQ_CL	W	0000_0000H
6114H-611CH	Reserved	–	–	–
6120H	ACPU interrupt status register (LCH4 and LCH5)	DMA_P2M_PE0_LCH4LCH5_INT_CONT	R	0000_0000H
6124H	ACPU interrupt raw status register (LCH4 and LCH5)	DMA_P2M_PE0_LCH4LCH5_INT_RAW	R	0000_0000H
6128H	ACPU interrupt enable set register (LCH4 and LCH5)	DMA_P2M_PE0_LCH4LCH5_INT_ENABLE	R/W	0000_0000H
612CH	ACPU interrupt enable clear register (LCH4 and LCH5)	DMA_P2M_PE0_LCH4LCH5_INT_ENABLE_CL	W	0000_0000H
6130H	ACPU interrupt source clear register (LCH4 and LCH5)	DMA_P2M_PE0_LCH4LCH5_INT_REQ_CL	W	0000_0000H
6134H-613FH	Reserved	–	–	–

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Address	Register Name	Register Symbol	R/W	After Reset
6140H	ACPU interrupt status register (LCH9 and LCH10)	DMA_P2M_PE0_LCH9LCH10_INT_CONT	R	0000_0000H
6144H	ACPU interrupt raw status register (LCH9 and LCH10)	DMA_P2M_PE0_LCH9LCH10_INT_RAW	R	0000_0000H
6148H	ACPU interrupt enable set register (LCH9 and LCH10)	DMA_P2M_PE0_LCH9LCH10_INT_ENABLE	R/W	0000_0000H
614CH	ACPU interrupt enable clear register (LCH9 and LCH10)	DMA_P2M_PE0_LCH9LCH10_INT_ENABLE_CL	W	0000_0000H
6150H	ACPU interrupt source clear register (LCH9 and LCH10)	DMA_P2M_PE0_LCH9LCH10_INT_REQ_CL	W	0000_0000H
6154H-615CH	Reserved	–	–	–
6160H	ACPU interrupt status register (LCH12 to LCH14)	DMA_P2M_PE0_LCH12LCH14_INT_CONT	R	0000_0000H
6164H	ACPU interrupt raw status register (LCH12 to LCH14)	DMA_P2M_PE0_LCH12LCH14_INT_RAW	R	0000_0000H
6168H	ACPU interrupt enable set register (LCH12 to LCH14)	DMA_P2M_PE0_LCH12LCH14_INT_ENABLE	R/W	0000_0000H
616CH	ACPU interrupt enable clear register (LCH12 to LCH14)	DMA_P2M_PE0_LCH12LCH14_INT_ENABLE_CL	W	0000_0000H
6170H	ACPU interrupt source clear register (LCH12 to LCH14)	DMA_P2M_PE0_LCH12LCH14_INT_REQ_CL	W	0000_0000H
6174H-63FCH	Reserved	–	–	–
6400H	DSP interrupt status register (LCH0 to LCH3)	DMA_P2M_DSP_LCH0LCH3_INT_CONT	R	0000_0000H
6404H	DSP interrupt raw status register (LCH0 to LCH3)	DMA_P2M_DSP_LCH0LCH3_INT_RAW	R	0000_0000H
6408H	DSP interrupt enable set register (LCH0 to LCH3)	DMA_P2M_DSP_LCH0LCH3_INT_ENABLE	R/W	0000_0000H
640CH	DSP interrupt enable clear register (LCH0 to LCH3)	DMA_P2M_DSP_LCH0LCH3_INT_ENABLE_CL	W	0000_0000H
6410H	DSP interrupt source clear register (LCH0 to LCH3)	DMA_P2M_DSP_LCH0LCH3_INT_REQ_CL	W	0000_0000H
6414H-641CH	Reserved	–	–	–
6420H	DSP interrupt status register (LCH4 and LCH5)	DMA_P2M_DSP_LCH4LCH5_INT_CONT	R	0000_0000H
6424H	DSP interrupt raw status register (LCH4 and LCH5)	DMA_P2M_DSP_LCH4LCH5_INT_RAW	R	0000_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
6428H	DSP interrupt enable set register (LCH4 and LCH5)	DMA_P2M_DSP_LCH4LCH5_INT_ENABLE	R/W	0000_0000H
642CH	DSP interrupt enable clear register (LCH4 and LCH5)	DMA_P2M_DSP_LCH4LCH5_INT_ENABLE_CL	W	0000_0000H
6430H	DSP interrupt source clear register (LCH4 and LCH5)	DMA_P2M_DSP_LCH4LCH5_INT_REQ_CL	W	0000_0000H
6434H-643CH	Reserved	–	–	–
6440H	DSP interrupt status register (LCH9 and LCH10)	DMA_P2M_DSP_LCH9LCH10_INT_CONT	R	0000_0000H
6444H	DSP interrupt raw status register (LCH9 and LCH10)	DMA_P2M_DSP_LCH9LCH10_INT_RAW	R	0000_0000H
6448H	DSP interrupt enable set register (LCH9 and LCH10)	DMA_P2M_DSP_LCH9LCH10_INT_ENABLE	R/W	0000_0000H
644CH	DSP interrupt enable clear register (LCH9 and LCH10)	DMA_P2M_DSP_LCH9LCH10_INT_ENABLE_CL	W	0000_0000H
6450H	DSP interrupt source clear register (LCH9 and LCH10)	DMA_P2M_DSP_LCH9LCH10_INT_REQ_CL	W	0000_0000H
6454H-645CH	Reserved	–	–	–
6460H	DSP interrupt status register (LCH12 to LCH14)	DMA_P2M_DSP_LCH12LCH14_INT_CONT	R	0000_0000H
6464H	DSP interrupt raw status register (LCH12 to LCH14)	DMA_P2M_DSP_LCH12LCH14_INT_RAW	R	0000_0000H
6468H	DSP interrupt enable set register (LCH12 to LCH14)	DMA_P2M_DSP_LCH12LCH14_INT_ENABLE	R/W	0000_0000H
646CH	DSP interrupt enable clear register (LCH12 to LCH14)	DMA_P2M_DSP_LCH12LCH14_INT_ENABLE_CL	W	0000_0000H
6470H	DSP interrupt source clear register (LCH12 to LCH14)	DMA_P2M_DSP_LCH12LCH14_INT_REQ_CL	W	0000_0000H
6474H-67FCH	Reserved	–	–	–

(c) P2M LCH0 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
7000H	P2M LCH0 source address register	DMA_P2M_LCH0_AADD	R/W	0000_0000H
7004H-701CH	Reserved	–	–	–
7020H	P2M LCH0 destination address register (start address)	DMA_P2M_LCH0_BADD	R/W	0000_0000H
7024H	P2M LCH0 destination address pointer register	DMA_P2M_LCH0_BADP	R	0000_0000H
7028H	P2M LCH0 destination address offset register	DMA_P2M_LCH0_BOFF	R/W	0000_0000H
702CH	P2M LCH0 destination block size register	DMA_P2M_LCH0_BSIZE	R/W	0000_0000H
7030H	P2M LCH0 destination block count register	DMA_P2M_LCH0_BSIZE_COUNT	R/W	0000_0000H
7034H-703CH	Reserved	–	–	–
7040H	P2M LCH0 length register	DMA_P2M_LCH0_LENG	R/W	0000_0000H
7044H	P2M LCH0 read length count register	DMA_P2M_LCH0_LENG_RCOUNT	R	0000_0000H
7048H	P2M LCH0 write length count register	DMA_P2M_LCH0_LENG_WCOUNT	R	0000_0000H
704CH	Reserved	–	–	–
7050H	P2M LCH0 mode register (timer setting, bit width, read/write endian, repeat)	DMA_P2M_LCH0_MODE	R/W	E4E4_0000H
7054H	P2M LCH0 timer register	DMA_P2M_LCH0_TIME	R/W	0000_0000H
7058H	P2M LCH0 timer count register	DMA_P2M_LCH0_TIME_COUNT	R	0000_0000H
705CH-70FCH	Reserved	–	–	–

(d) P2M LCH1 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
7100H	P2M LCH1 source address register	DMA_P2M_LCH1_AADD	R/W	0000_0000H
7104H-711CH	Reserved	–	–	–
7120H	P2M LCH1 destination address register (start address)	DMA_P2M_LCH1_BADD	R/W	0000_0000H
7124H	P2M LCH1 destination address pointer register	DMA_P2M_LCH1_BADP	R	0000_0000H
7128H	P2M LCH1 destination address offset register	DMA_P2M_LCH1_BOFF	R/W	0000_0000H
712CH	P2M LCH1 destination block size register	DMA_P2M_LCH1_BSIZE	R/W	0000_0000H
7130H	P2M LCH1 destination block count register	DMA_P2M_LCH1_BSIZE_COUNT	R/W	0000_0000H
7134H-713CH	Reserved	–	–	–
7140H	P2M LCH1 length register	DMA_P2M_LCH1_LENG	R/W	0000_0000H
7144H	P2M LCH1 read length count register	DMA_P2M_LCH1_LENG_RCOUNT	R	0000_0000H
7148H	P2M LCH1 write length count register	DMA_P2M_LCH1_LENG_WCOUNT	R	0000_0000H
714CH	Reserved	–	–	–
7150H	P2M LCH1 mode register (timer setting, bit width, read/write endian, repeat)	DMA_P2M_LCH1_MODE	R/W	E4E4_0000H
7154H	P2M LCH1 timer register	DMA_P2M_LCH1_TIME	R/W	0000_0000H
7158H	P2M LCH1 timer count register	DMA_P2M_LCH1_TIME_COUNT	R	0000_0000H
715CH-71FCH	Reserved	–	–	–

(e) P2M LCH2 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
7200H	P2M LCH2 source address register	DMA_P2M_LCH2_AADD	R/W	0000_0000H
7204H-721CH	Reserved	–	–	–
7220H	P2M LCH2 destination address register (start address)	DMA_P2M_LCH2_BADD	R/W	0000_0000H
7224H	P2M LCH2 destination address pointer register	DMA_P2M_LCH2_BADP	R	0000_0000H
7228H	P2M LCH2 destination address offset register	DMA_P2M_LCH2_BOFF	R/W	0000_0000H
722CH	P2M LCH2 destination block size register	DMA_P2M_LCH2_BSIZE	R/W	0000_0000H
7230H	P2M LCH2 destination block count register	DMA_P2M_LCH2_BSIZE_COUNT	R/W	0000_0000H
7234H-723CH	Reserved	–	–	–
7240H	P2M LCH2 length register	DMA_P2M_LCH2_LENG	R/W	0000_0000H
7244H	P2M LCH2 read length count register	DMA_P2M_LCH2_LENG_RCOUNT	R	0000_0000H
7248H	P2M LCH2 write length count register	DMA_P2M_LCH2_LENG_WCOUNT	R	0000_0000H
724CH	Reserved	–	–	–
7250H	P2M LCH2 mode register (timer setting, bit width, read/write endian, repeat)	DMA_P2M_LCH2_MODE	R/W	E4E4_0000H
7254H	P2M LCH2 timer register	DMA_P2M_LCH2_TIME	R/W	0000_0000H
7258H	P2M LCH2 timer count register	DMA_P2M_LCH2_TIME_COUNT	R	0000_0000H
725CH-72FCH	Reserved	–	–	–

(f) P2M LCH3 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
7300H	P2M LCH3 source address register	DMA_P2M_LCH3_AADD	R/W	0000_0000H
7304H-731CH	Reserved	–	–	–
7320H	P2M LCH3 destination address register (start address)	DMA_P2M_LCH3_BADD	R/W	0000_0000H
7324H	P2M LCH3 destination address pointer register	DMA_P2M_LCH3_BADP	R	0000_0000H
7328H	P2M LCH3 destination address offset register	DMA_P2M_LCH3_BOFF	R/W	0000_0000H
732CH	P2M LCH3 destination block size register	DMA_P2M_LCH3_BSIZE	R/W	0000_0000H
7330H	P2M LCH3 destination block count register	DMA_P2M_LCH3_BSIZE_COUNT	R/W	0000_0000H
7334H-733CH	Reserved	–	–	–
7340H	P2M LCH3 length register	DMA_P2M_LCH3_LENG	R/W	0000_0000H
7344H	P2M LCH3 read length count register	DMA_P2M_LCH3_LENG_RCOUNT	R	0000_0000H
7348H	P2M LCH3 write length count register	DMA_P2M_LCH3_LENG_WCOUNT	R	0000_0000H
734CH	Reserved	–	–	–
7350H	P2M LCH3 mode register (bit width, read/write endian, repeat)	DMA_P2M_LCH3_MODE	R/W	E4E4_0000H
7354H-73FCH	Reserved	–	–	–

(g) P2M LCH4 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
7400H	P2M LCH4 source address register	DMA_P2M_LCH4_AADD	R/W	0000_0000H
7404H-741CH	Reserved	–	–	–
7420H	P2M LCH4 destination address register (start address)	DMA_P2M_LCH4_BADD	R/W	0000_0000H
7424H	P2M LCH4 destination address pointer register	DMA_P2M_LCH4_BADP	R	0000_0000H
7428H	P2M LCH4 destination address offset register	DMA_P2M_LCH4_BOFF	R/W	0000_0000H
742CH	P2M LCH4 destination block size register	DMA_P2M_LCH4_BSIZE	R/W	0000_0000H
7430H	P2M LCH4 destination block count register	DMA_P2M_LCH4_BSIZE_COUNT	R/W	0000_0000H
7434H-743CH	Reserved	–	–	–
7440H	P2M LCH4 length register	DMA_P2M_LCH4_LENG	R/W	0000_0000H
7444H	P2M LCH4 read length count register	DMA_P2M_LCH4_LENG_RCOUNT	R	0000_0000H
7448H	P2M LCH4 write length count register	DMA_P2M_LCH4_LENG_WCOUNT	R	0000_0000H
744CH	Reserved	–	–	–
7450H	P2M LCH4 mode register (bit width, read/write endian, repeat)	DMA_P2M_LCH4_MODE	R/W	E4E4_0000H
7454H-74FCH	Reserved	–	–	–

(h) P2M LCH5 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
7500H	P2M LCH5 source address register	DMA_P2M_LCH5_AADD	R/W	0000_0000H
7504H-751CH	Reserved	–	–	–
7520H	P2M LCH5 destination address register (start address)	DMA_P2M_LCH5_BADD	R/W	0000_0000H
7524H	P2M LCH5 destination address pointer register	DMA_P2M_LCH5_BADP	R	0000_0000H
7528H	P2M LCH5 destination address offset register	DMA_P2M_LCH5_BOFF	R/W	0000_0000H
752CH	P2M LCH5 destination block size register	DMA_P2M_LCH5_BSIZE	R/W	0000_0000H
7530H	P2M LCH5 destination block count register	DMA_P2M_LCH5_BSIZE_COUNT	R/W	0000_0000H
7534H-753CH	Reserved	–	–	–
7540H	P2M LCH5 length register	DMA_P2M_LCH5_LENG	R/W	0000_0000H
7544H	P2M LCH5 read length count register	DMA_P2M_LCH5_LENG_RCOUNT	R	0000_0000H
7548H	P2M LCH5 write length count register	DMA_P2M_LCH5_LENG_WCOUNT	R	0000_0000H
754CH	Reserved	–	–	–
7550H	P2M LCH5 mode register (bit width, read/write endian, repeat)	DMA_P2M_LCH5_MODE	R/W	E4E4_0000H
7554H-76FCH	Reserved	–	–	–

(i) P2M LCH9 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
7900H	P2M LCH9 source address register	DMA_P2M_LCH9_AADD	R/W	0000_0000H
7904H-791CH	Reserved	–	–	–
7920H	P2M LCH9 destination address register (start address)	DMA_P2M_LCH9_BADD	R/W	0000_0000H
7924H	P2M LCH9 destination address pointer register	DMA_P2M_LCH9_BADP	R	0000_0000H
7928H	P2M LCH9 destination address offset register	DMA_P2M_LCH9_BOFF	R/W	0000_0000H
792CH	P2M LCH9 destination block size register	DMA_P2M_LCH9_BSIZE	R/W	0000_0000H
7930H	P2M LCH9 destination block count register	DMA_P2M_LCH9_BSIZE_COUNT	R/W	0000_0000H
7934H-793CH	Reserved	–	–	–
7940H	P2M LCH9 length register	DMA_P2M_LCH9_LENG	R/W	0000_0000H
7944H	P2M LCH9 read length count register	DMA_P2M_LCH9_LENG_RCOUNT	R	0000_0000H
7948H	P2M LCH9 write length count register	DMA_P2M_LCH9_LENG_WCOUNT	R	0000_0000H
794CH	Reserved	–	–	–
7950H	P2M LCH9 mode register (bit width, read/write endian, repeat)	DMA_P2M_LCH9_MODE	R/W	E4E4_0000H
7954H-79FCH	Reserved	–	–	–

(j) P2M LCH10 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
7A00H	P2M LCH10 source address register	DMA_P2M_LCH10_AADD	R/W	0000_0000H
7A04H-7A1CH	Reserved	–	–	–
7A20H	P2M LCH10 destination address register (start address)	DMA_P2M_LCH10_BADD	R/W	0000_0000H
7A24H	P2M LCH10 destination address pointer register	DMA_P2M_LCH10_BADP	R	0000_0000H
7A28H	P2M LCH10 destination address offset register	DMA_P2M_LCH10_BOFF	R/W	0000_0000H
7A2CH	P2M LCH10 destination block size register	DMA_P2M_LCH10_BSIZE	R/W	0000_0000H
7A30H	P2M LCH10 destination block count register	DMA_P2M_LCH10_BSIZE_COUNT	R/W	0000_0000H
7A34H-7A3CH	Reserved	–	–	–
7A40H	P2M LCH10 length register	DMA_P2M_LCH10_LENG	R/W	0000_0000H
7A44H	P2M LCH10 read length count register	DMA_P2M_LCH10_LENG_RCOUNT	R	0000_0000H
7A48H	P2M LCH10 write length count register	DMA_P2M_LCH10_LENG_WCOUNT	R	0000_0000H
7A4CH	Reserved	–	–	–
7A50H	P2M LCH10 mode register (bit width, read/write endian, repeat)	DMA_P2M_LCH10_MODE	R/W	E4E4_0000H
7A54H-7AFCH	Reserved	–	–	–

(k) P2M LCH12 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
7C00H	P2M LCH12 source address register	DMA_P2M_LCH12_AADD	R/W	0000_0000H
7C04H-7C1CH	Reserved	–	–	–
7C20H	P2M LCH12 destination address register (start address)	DMA_P2M_LCH12_BADD	R/W	0000_0000H
7C24H	P2M LCH12 destination address pointer register	DMA_P2M_LCH12_BADP	R	0000_0000H
7C28H	P2M LCH12 destination address offset register	DMA_P2M_LCH12_BOFF	R/W	0000_0000H
7C2CH	P2M LCH12 destination block size register	DMA_P2M_LCH12_BSIZE	R/W	0000_0000H
7C30H	P2M LCH12 destination block count register	DMA_P2M_LCH12_BSIZE_COUNT	R/W	0000_0000H
7C34H-7C3CH	Reserved	–	–	–
7C40H	P2M LCH12 length register	DMA_P2M_LCH12_LENG	R/W	0000_0000H
7C44H	P2M LCH12 read length count register	DMA_P2M_LCH12_LENG_RCOUNT	R	0000_0000H
7C48H	P2M LCH12 write length count register	DMA_P2M_LCH12_LENG_WCOUNT	R	0000_0000H
7C4CH	Reserved	–	–	–
7C50H	P2M LCH12 mode register (bit width, read/write endian, repeat)	DMA_P2M_LCH12_MODE	R/W	E4E4_0000H
7C54H-7C5FH	Reserved	–	–	–

(l) P2M LCH13 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
7D00H	P2M LCH13 source address register	DMA_P2M_LCH13_AADD	R/W	0000_0000H
7D04H-7D1CH	Reserved	–	–	–
7D20H	P2M LCH13 destination address register (start address)	DMA_P2M_LCH13_BADD	R/W	0000_0000H
7D24H	P2M LCH13 destination address pointer register	DMA_P2M_LCH13_BADP	R	0000_0000H
7D28H	P2M LCH13 destination address offset register	DMA_P2M_LCH13_BOFF	R/W	0000_0000H
7D2CH	P2M LCH13 destination block size register	DMA_P2M_LCH13_BSIZE	R/W	0000_0000H
7D30H	P2M LCH13 destination block count register	DMA_P2M_LCH13_BSIZE_COUNT	R/W	0000_0000H
7D34H-7D3CH	Reserved	–	–	–
7D40H	P2M LCH13 length register	DMA_P2M_LCH13_LENG	R/W	0000_0000H
7D44H	P2M LCH13 read length count register	DMA_P2M_LCH13_LENG_RCOUNT	R	0000_0000H
7D48H	P2M LCH13 write length count register	DMA_P2M_LCH13_LENG_WCOUNT	R	0000_0000H
7D4CH	Reserved	–	–	–
7D50H	P2M LCH13 mode register (bit width, read/write endian, repeat)	DMA_P2M_LCH13_MODE	R/W	E4E4_0000H
7D54H-7DFCH	Reserved	–	–	–

(m) P2M LCH14 setting registers

Address	Register Name	Register Symbol	R/W	After Reset
7E00H	P2M LCH14 source address register	DMA_P2M_LCH14_AADD	R/W	0000_0000H
7E04H-7E1CH	Reserved	–	–	–
7E20H	P2M LCH14 destination address register (start address)	DMA_P2M_LCH14_BADD	R/W	0000_0000H
7E24H	P2M LCH14 destination address pointer register	DMA_P2M_LCH14_BADP	R	0000_0000H
7E28H	P2M LCH14 destination address offset register	DMA_P2M_LCH14_BOFF	R/W	0000_0000H
7E2CH	P2M LCH14 destination block size register	DMA_P2M_LCH14_BSIZE	R/W	0000_0000H
7E30H	P2M LCH14 destination block count register	DMA_P2M_LCH14_BSIZE_COUNT	R/W	0000_0000H
7E34H-7E3CH	Reserved	–	–	–
7E40H	P2M LCH14 length register	DMA_P2M_LCH14_LENG	R/W	0000_0000H
7E44H	P2M LCH14 read length count register	DMA_P2M_LCH14_LENG_RCOUNT	R	0000_0000H
7E48H	P2M LCH14 write length count register	DMA_P2M_LCH14_LENG_WCOUNT	R	0000_0000H
7E4CH	Reserved	–	–	–
7E50H	P2M LCH14 mode register (bit width, read/write endian, repeat)	DMA_P2M_LCH14_MODE	R/W	E4E4_0000H
7E54H-7EFCH	Reserved	–	–	–

(4) Interrupt index registers

Address	Register Name	Register Symbol	R/W	After Reset
8000H	ACPU interrupt index register	DMA_PE0_INT_INDEX	R	0000_0000H
8004H-8008H	Reserved	–	–	–
800CH	DSP interrupt index register	DMA_DSP_INT_INDEX	R	0000_0000H
8010H-80FCH	Reserved	–	–	–
8100H	ACPU interrupt index register 2 (LCH is assigned per bit)	DMA_PE0_INT_INDEX2	R	0000_0000H
8104H-8108H	Reserved	–	–	–
810CH	DSP interrupt index register 2 (LCH is assigned per bit)	DMA_DSP_INT_INDEX2	R	0000_0000H
8110H-8FFCH	Reserved	–	–	–

A.1.4 IPU (registers related to image processor functions)

Base address: 400A_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
0000H	Function setting register	IMG_MODE	R/W	0000_0000H
0004H	Processing request register	IMG_REQ	W	0000_0000H
0008H	Processing status register	IMG_ACK	R	0000_0000H
000CH	Interrupt status register	IMG_STATUS	R	0000_0000H
0010H	Interrupt raw status register	IMG_RAWSTATUS	R	0000_0000H
0014H	Interrupt enable set register	IMG_ENSET	R/W	0000_0000H
0018H	Interrupt enable clear register	IMG_ENCLR	W	0000_0000H
001CH	Interrupt source clear register	IMG_FFCLR	W	0000_0000H
0020H	Source image (back image) address addition value register	IMG_SRCSIZE_B	R/W	0000_0010H
0024H	Source image (front image) address addition value register	IMG_SRCSIZE_F	R/W	0000_0010H
0028H	Destination image address addition value register	IMG_DSTSIZE	R/W	0000_0010H
002CH	Reserved	–	–	–
0030H	Source image (back image) Y/RGB plane address register	IMG_SRCYRGBADR_B	R/W	0000_0000H
0034H	Source image (front image) Y/RGB plane address register	IMG_SRCYRGBADR_F	R/W	0000_0000H
0038H	Destination image Y/RGB plane address register	IMG_DSTYRGBADR	R/W	0000_0000H
003CH	Reserved	–	–	–
0040H	Source image (back image) UV plane address register	IMG_SRCUVADR_B	R/W	0000_0000H
0044H	Source image (front image) UV plane address register	IMG_SRCUVADR_F	R/W	0000_0000H
0048H	Destination image UV plane address register	IMG_DSTUVADR	R/W	0000_0000H
004CH	Reserved	–	–	–
0050H	Source image (back image) horizontal size register	IMG_SRCHSIZE_B	R/W	0000_0008H
0054H	Source image (front image) horizontal size register	IMG_SRCHSIZE_F	R/W	0000_0008H
0058H	Source image (back image) vertical size register	IMG_SRCVSIZE_B	R/W	0000_0008H
005CH	Source image (front image) vertical size register	IMG_SRCVSIZE_F	R/W	0000_0008H
0060H	Display horizontal offset position register	IMG_OFFSETX	R/W	0000_0000H
0064H	Display vertical offset position register	IMG_OFFSETY	R/W	0000_0000H
0068H	Mask color register	IMG_MASKCOLR	R/W	0000_0000H
006CH	Transparency register	IMG_ALPHA	R/W	0000_00FFH
0070H	Resized destination image horizontal size register (set only for resize function)	IMG_DSTHSIZE	R/W	0000_0008H
0074H	Resized destination image vertical size register (set only for resize function)	IMG_DSTVSIZE	R/W	0000_0008H

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Address	Register Name	Register Symbol	R/W	After Reset
0078H	Destination image horizontal step register (set only for resize function)	IMG_HSTEP	R/W	0000_0040H
007CH	Destination image vertical step register (set only for resize function)	IMG_VSTEP	R/W	0000_0040H
0080H	Destination image horizontal magnification register (set only for resize function)	IMG_HFOLD	R/W	0000_0100H
0084H	Destination image vertical magnification register (set only for resize function)	IMG_VFOLD	R/W	0000_0100H
0088H-00A8H	Reserved	–	–	–
00ACH	I/O pixel data endian switch register	IMG_PEL_ENDIAN	R/W	0000_0000H
00B0H	AHB interface debug address register	IMG_DBG_HADDR	R	0000_0000H
00B4H-00BCH	Reserved	–	–	–
00C0H	Color space conversion matrix setting register (RGBYUV)	IMG_RGBYUV_CONF	R/W	0000_0000H
00C4H	Color space conversion matrix parameter register (RGBYUV00)	IMG_RGBYUV00	R/W	0000_004DH
00C8H	Color space conversion matrix parameter register (RGBYUV01)	IMG_RGBYUV01	R/W	0000_0096H
00CCH	Color space conversion matrix parameter register (RGBYUV02)	IMG_RGBYUV02	R/W	0000_001DH
00D0H	Color space conversion matrix parameter register (RGBYUV10)	IMG_RGBYUV10	R/W	0000_082CH
00D4H	Color space conversion matrix parameter register (RGBYUV11)	IMG_RGBYUV11	R/W	0000_0857H
00D8H	Color space conversion matrix parameter register (RGBYUV12)	IMG_RGBYUV12	R/W	0000_0083H
00DCH	Color space conversion matrix parameter register (RGBYUV20)	IMG_RGBYUV20	R/W	0000_0083H
00E0H	Color space conversion matrix parameter register (RGBYUV21)	IMG_RGBYUV21	R/W	0000_086EH
00E4H	Color space conversion matrix parameter register (RGBYUV22)	IMG_RGBYUV22	R/W	0000_0815H
00E8H	Color space conversion matrix setting register (YUVRGB)	IMG_YUVRGB_CONF	R/W	0000_0000H
00ECH	Color space conversion matrix parameter register (YUVRGB00)	IMG_YUVRGB00	R/W	0000_0100H
00F0H	Color space conversion matrix parameter register (YUVRGB01)	IMG_YUVRGB01	R/W	0000_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
00F4H	Color space conversion matrix parameter register (YUVRGB02)	IMG_YUVRGB02	R/W	0000_015FH
00F8H	Color space conversion matrix parameter register (YUVRGB10)	IMG_YUVRGB10	R/W	0000_0100H
00FCH	Color space conversion matrix parameter register (YUVRGB11)	IMG_YUVRGB11	R/W	0000_0856H
0100H	Color space conversion matrix parameter register (YUVRGB12)	IMG_YUVRGB12	R/W	0000_08B3H
0104H	Color space conversion matrix parameter register (YUVRGB20)	IMG_YUVRGB20	R/W	0000_0100H
0108H	Color space conversion matrix parameter register (YUVRGB21)	IMG_YUVRGB21	R/W	0000_01BBH
010CH	Color space conversion matrix parameter register (YUVRGB22)	IMG_YUVRGB22	R/W	0000_0000H
0110H	I/O image format register	IMG_FORMAT	R/W	0000_0000H
0114H	Input image byte lane select register	IMG_INDATABYTE	R/W	0000_E4E4H
0118H	Output image byte lane select register	IMG_OUTDATABYTE	R/W	0000_E4E4H
011CH	Source image (back image) V plane address register	IMG_SRCVADR_B	R/W	0000_0000H
0120H	Source image (front image) V plane address register	IMG_SRCVADR_F	R/W	0000_0000H
0124H	Destination image V plane address register	IMG_DSTVADR	R/W	0000_0000H
0128H	Register update reserve setting register	IMG_DUAL_FF	R/W	0000_0000H
012CH	Reserved	–	–	–
0130H	Input image (back image) byte lane select register (Y/UV planes divided)	IMG_INDATABYTE_B_CMP	R/W	0000_E4E4H
0134H	Input image (front image) byte lane select register (Y/UV planes divided)	IMG_INDATABYTE_F_CMP	R/W	0000_E4E4H
0138H	Output image byte lane select register (Y/UV planes divided)	IMG_OUTDATABYTE_CMP	R/W	0000_E4E4H
013CH	R brightness setting register	IMG_R_BRITNESS	R/W	0000_0000H
0140H	G brightness setting register	IMG_G_BRITNESS	R/W	0000_0000H
0144H	B brightness setting register	IMG_B_BRITNESS	R/W	0000_0000H
0148H-0FFFH	Reserved	–	–	–

A.1.5 Camera interface (CAM)

Base address: 400B_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
0000H	INT status register	CA_STATUS	R	0000_0000H
0004H	INT raw status register	CA_RAWSTATUS	R	0000_0000H
0008H	INT enable set register	CA_ENSET	R/W	0000_0000H
000CH	INT enable clear register	CA_ENCLR	W	0000_0000H
0010H	INT source clear register	CA_FFCLR	W	0000_0000H
0014H	Error address register	CA_ERRORADR	R/W	0000_0000H
0018H-001CH	Reserved	–	–	–
0020H	Camera control register	CA_CSR	R/W	0000_0000H
0024H-002CH	Reserved	–	–	–
0030H	Transfer start X coordinate register	CA_X1R	R/W	0000_0000H
0034H	Transfer end X coordinate register	CA_X2R	R/W	0000_0000H
0038H	Transfer start Y coordinate register	CA_Y1R	R/W	0000_0000H
003CH	Transfer end Y coordinate register	CA_Y2R	R/W	0000_0000H
0040H	Luminance signal offset register	CA_BNZR	R/W	0000_0000H
0044H	Luminance signal gain register	CA_BNGR	R/W	0000_0080H
0048H	U color difference signal offset register	CA_CBZR	R/W	0000_0000H
004CH	U color difference signal gain register	CA_CBGR	R/W	0000_0080H
0050H	V color difference signal offset register	CA_CRZR	R/W	0000_0000H
0054H	V color difference signal gain register	CA_CRGR	R/W	0000_0080H
0058H-007CH	Reserved	–	–	–
0080H	Transfer control register	CA_DMACNT	R/W	0000_0000H
0084H	Transfer frame register	CA_FRAME	R/W	0000_0005H
0088H	Transfer request register	CA_DMAREQ	R/W	0000_0000H
008CH	Transfer request cancellation register	CA_DMASTOP	W	0000_0000H
0090H-00FCH	Reserved	–	–	–
0100H	Address addition value register (main frame)	CA_LINESIZE_MAIN	R/W	0000_0000H
0104H	Horizontal reduction ratio register (main frame)	CA_XRATIO_MAIN	R/W	0000_0000H
0108H	Vertical reduction ratio register (main frame)	CA_YRATIO_MAIN	R/W	0000_0000H
010CH	Horizontal transfer size register (main frame)	CA_DMAX_MAIN	R/W	0000_0000H
0110H	Vertical transfer size register (main frame)	CA_DMAY_MAIN	R/W	0000_0000H
0114H	Y plane transfer address register (A frame)	CA_YPLANE_A	R/W	0000_0000H
0118H	UV plane transfer address register (A frame)	CA_UVPLANE_A	R/W	0000_0000H
011CH	Y plane transfer address register (B frame)	CA_YPLANE_B	R/W	0000_0000H
0120H	UV plane transfer address register (B frame)	CA_UVPLANE_B	R/W	0000_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
0124H-0228H	Reserved	–	–	–
022CH	Module control register	CA_MODULECONT	R/W	0000_0000H
0230H	Update register	CA_UPDATE	R/W	0000_0000H
0234H	Horizontal/vertical flip control register	CA_MIRROR	R/W	0000_0000H
0238H	Byte lane control register (dedicated to YUV 422 Interleave)	CA_OD_BYTELANE	R/W	0000_00E4H
023CH	Reserved	–	–	–
0240H	Transfer end X coordinate register (dedicated to enable signal sampling mode)	CA_X3R	R/W	0000_0000H
0244H	V plane transfer address register (A frame)	CA_VPLANE_A	R/W	0000_0000H
0248H	V plane transfer address register (B frame)	CA_VPLANE_B	R/W	0000_0000H
024CH-0250H	Reserved	–	–	–
0254H	Byte lane control register 2 (for video-system macros)	CA_OD_BYTELANE2	R/W	0000_E4E4H
0258H	Simple QoS setting register	CA_QOS	R/W	0000_0000H
025CH-FFFFH	Reserved	–	–	–

A.1.6 Audio/voice interface (PM1)

Base address: 400D_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Operation mode setting register	PM1_FUNC_SEL	R/W	0000_0000H
0004H	Data transfer enable set register	PM1_TXRX_EN	W	–
0008H	Data transfer enable clear register	PM1_TXRX_DIS	W	–
000CH	Data transfer cycle setting register	PM1_CYCLE	R/W	0000_0000H
0010H	Interrupt raw status register	PM1_RAW	R	0000_0000H
0014H	Interrupt status register	PM1_STATUS	R	0000_0000H
0018H	Interrupt enable set register	PM1_ENSET	W	–
001CH	Interrupt enable clear register	PM1_ENCLR	W	–
0020H	Interrupt clear register	PM1_CLEAR	W	–
0024H	Transmit data register	PM1_TXQ	R/W	0000_0000H
0028H	Receive data register	PM1_RXQ	R	0000_0000H
002CH	Reserved	–	–	–
0030H	Data transfer cycle setting register 2	PM1_CYCLE2	R/W	0000_0000H

A.1.7 PWM interface

Base address: 4010_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	PWM operation start/stop register	PWM_CH0_ CTRL	R/W	0000_0000H
0004H	PWM0 mode control register	PWM_CH0_MODE	R/W	0000_0000H
0010H	Ch0 counter 0 delay setting register	PWM_CH0_DELAY0	R/W	0000_0000H
0014H	Ch0 counter 0 leading edge setting register	PWM_CH0_LEDGE0	R/W	0000_0000H
0018H	Ch0 counter 0 trailing edge setting register	PWM_CH0_TEDGE0	R/W	0000_0000H
001CH	Ch0 counter 0 total cycle setting register	PWM_CH0_TOTAL0	R/W	0000_0000H
0020H	Ch0 counter loop count setting register	PWM_CH0_LOOP0	R/W	0000_0000H
0040H	Ch0 counter 1 delay setting register	PWM_CH0_DELAY1	R/W	0000_0000H
0044H	Ch0 counter 1 leading edge setting register	PWM_CH0_LEDGE1	R/W	0000_0000H
0048H	Ch0 counter 1 trailing edge setting register	PWM_CH0_TEDGE1	R/W	0000_0000H
004CH	Ch0 counter 1 total cycle setting register	PWM_CH0_TOTAL1	R/W	0000_0000H
0050H	Ch0 counter 1 loop count setting register	PWM_CH0_LOOP1	R/W	0000_0000H
0080H	Ch0 counter 2 delay setting register	PWM_CH0_DELAY2	R/W	0000_0000H
0084H	Ch0 counter 2 leading edge setting register	PWM_CH0_LEDGE2	R/W	0000_0000H
0088H	Ch0 counter 2 trailing edge setting register	PWM_CH0_TEDGE2	R/W	0000_0000H
008CH	Ch0 counter 2 total cycle setting register	PWM_CH0_TOTAL2	R/W	0000_0000H
0090H	Ch0 counter 2 loop count setting register	PWM_CH0_LOOP2	R/W	0000_0000H
0100H	PWM operation start/stop register	PWM_CH1_CTRL	R/W	0000_0000H
0104H	PWM0 mode control register	PWM_CH1_MODE	R/W	0000_0000H
0110H	Ch1 counter 0 delay setting register	PWM_CH1_DELAY0	R/W	0000_0000H
0114H	Ch1 counter 0 leading edge setting register	PWM_CH1_LEDGE0	R/W	0000_0000H
0118H	Ch1 counter 0 trailing edge setting register	PWM_CH1_TEDGE0	R/W	0000_0000H
011CH	Ch1 counter 0 total cycle setting register	PWM_CH1_TOTAL0	R/W	0000_0000H
0120H	Ch1 counter loop count setting register	PWM_CH1_LOOP0	R/W	0000_0000H
0140H	Ch1 counter 1 delay setting register	PWM_CH1_DELAY1	R/W	0000_0000H
0144H	Ch1 counter 1 leading edge setting register	PWM_CH1_LEDGE1	R/W	0000_0000H
0148H	Ch1 counter 1 trailing edge setting register	PWM_CH1_TEDGE1	R/W	0000_0000H
014CH	Ch1 counter 1 total cycle setting register	PWM_CH1_TOTAL1	R/W	0000_0000H
0150H	Ch1 counter 1 loop count setting register	PWM_CH1_LOOP1	R/W	0000_0000H
0180H	Ch1 counter 2 delay setting register	PWM_CH1_DELAY2	R/W	0000_0000H
0184H	Ch1 counter 2 leading edge setting register	PWM_CH1_LEDGE2	R/W	0000_0000H
0188H	Ch1 counter 2 trailing edge setting register	PWM_CH1_TEDGE2	R/W	0000_0000H
018CH	Ch1 counter 2 total cycle setting register	PWM_CH1_TOTAL2	R/W	0000_0000H
0190H	Ch1 counter 2 loop count setting register	PWM_CH1_LOOP2	R/W	0000_0000H
0400H	PWM interrupt status register	PWM_INTSTATUS	R	0000_0000H
0404H	PWM interrupt raw status register	PWM_INTRAWSTATUS	R	0000_0000H
0408H	PWM interrupt enable set register	PWM_INTENSET	R/W	0000_0000H
040CH	PWM interrupt enable clear register	PWM_INTENCLR	W	0000_0000H
0410H	PWM interrupt source clear register	PWM_INTFFCLR	W	0000_0000H

A.1.8 SPI interface (SP2)

Base address: 4013_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Mode register	SP2_MODE	R/W	0000_0002H
0004H	SPI polarity register	SP2_POL	R/W	0000_7000H
0008H	Control register	SP2_CONTROL	R/W	0000_8040H
000CH	Reserved	–	–	–
0010H	Transmit data register	SP2_TX_DATA	W	0000_0000H
0014H	Receive data register	SP2_RX_DATA	R	0000_000xH
0018H	Interrupt status register	SP2_STATUS	R	0000_0000H
001CH	Interrupt raw status register	SP2_RAW_STATUS	R	0000_0000H
0020H	Interrupt enable set register	SP2_ENSET	R/W	0000_0000H
0024H	Interrupt enable clear register	SP2_ENCLR	W	0000_0000H
0028H	Interrupt source clear register	SP2_FFCLR	W	0000_0000H
002CH-0030H	Reserved	–	–	–
0034H	Control register 2	SP2_CONTROL2	R/W	0000_0000H
0038H	CS fix register	SP2_TIECS	R/W	0000_0000H
003CH-FFFFH	Reserved	–	–	–

A.1.9 Terrestrial digital TV interface (DTV)

Base address: 4015_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Interrupt status register	DT_STATUS	R	0000_0000H
0004H	Interrupt raw status register	DT_RAWSTATUS	R	0000_0000H
0008H	Interrupt enable set register	DT_ENSET	R/W	0000_0000H
000CH	Interrupt enable clear register	DT_ENCLR	W	0000_0000H
0010H	Interrupt source clear register	DT_FFCLR	W	0000_0000H
0014H	Error address register	DT_ERRORADR	R/W	0000_0000H
0020H	Transfer control register	DT_DMACNT	R/W	0000_0003H
0024H	Transfer request register	DT_DMAREQ	R/W	0000_0000H
0028H	Transfer request cancellation register	DT_DMASTOP	W	0000_0000H
002CH	Start address register	DT_START	R/W	0000_0000H
0030H	Buffer size register	DT_BUFSIZE	R/W	0000_0000H
0034H	Blank size register	DT_BLANK	R/W	0000_0000H
0038H	Current packet register	DT_CURRENT	R	0000_0000H
003CH	DMA completion interrupt setting register	DT_INTCONT	R/W	0000_0000H
0040H	Module control register	DT_MODULECONT	R/W	0000_0000H

A.1.10 ITU-R BT.656 interface (NTS)

Base address: 4012_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Control register	NTS_CONTROL	R/W	0000_0000H
0004H	Display register	NTS_OUT	R/W	0000_0000H
0008H	Status register	NTS_STATUS	R	0000_0000H
000CH	Display area address register YA	NTS_YAREAAD_A	R/W	0000_0000H
0010H	Display area address register YB	NTS_YAREAAD_B	R/W	0000_0000H
0014H	Display area address register YC	NTS_YAREAAD_C	R/W	0000_0000H
0018H	Display area address register UVA	NTS_UVAREAAD_A	R/W	0000_0000H
001CH	Display area address register UVB	NTS_UVAREAAD_B	R/W	0000_0000H
0020H	Display area address register UVC	NTS_UVAREAAD_C	R/W	0000_0000H
0024H	Address addition value register	NTS_HOFFSET	R/W	0000_0000H
0028H	Frame select register	NTS_FRAMESEL	R/W	0000_0001H
002CH-005CH	Reserved	–	–	–
0060H	Interrupt status register	NTS_INTSTATUS	R	0000_0000H
0064H	Interrupt raw status register	NTS_INTRAWSTATUS	R	0000_0000H
0068H	Interrupt enable set register	NTS_INTENSET	R/W	0000_0000H
006CH	Interrupt enable clear register	NTS_INTENCLR	W	0000_0000H
0070H	Interrupt source clear register	NTS_INTFFCLR	W	0000_0000H
0074H	Error address register	NTS_ERRORADR	R/W	0000_0000H
0078H	Software reset register	NTS_SWRESET	R/W	0000_0000H
007CH-00FCH	Reserved	–	–	–

A.1.11 NAND Flash interface (NAND)

Base address: 4022: 0000H

(1) AHB/mode/interrupt control registers (BBC)

Address	Register Name	Register Symbol	R/W	After Reset
0000H	AHB base address convert register	NAND_ATBAR	R/W	0000_0000H
0004H	AHB count convert register	NAND_ATCR	R	0000_0000H
0008H	AHB address convert register	NAND_ATACR	R	0000_0000H
000CH	Mode set register	NAND_MSR	R/W	0000_0000H
0010H	Interrupt status register	NAND_INTSTATUS	R	0000_0000H
0014H	Interrupt raw status register	NAND_RAWINTSTATUS	R	0000_0000H
0018H	Interrupt enable set register	NAND_INTENSET	R/W	0000_0000H
001CH	Interrupt enable clear register	NAND_INTENCLR	W	–
0020H	AHB interrupt source clear register	AHB_INTFFCLR	W	–
0024H	Flash read data register	NAND_FRD	R	0000_0000H
0280H-00FCH	Reserved	–	–	–

(2) EMMU block registers (Flash interface control)

(1/3)

Address	Register Name	Register Symbol	R/W	After Reset
0200H	Control register	NAND_CR	R/W	0000_0000H
0204H	Status register	NAND_ESR	R	–
0208H	Interrupt control register	NAND_EICR	R/W	0000_0000H
020CH	Interrupt raw status register	NAND_EIRSR	R	–
0210H	Interrupt source clear register	NAND_EICLR	W	–
0214H	CE control register	NAND_CECR	R/W	0000_000FH
0218H	Compare data register	NAND_CDR	R/W	0000_FF00H
021CH	Status check control register	NAND_SCCR	R/W	0000_0370H
0220H	Channel A command write register	NAND_CHA_CWR	W	–
0224H	Channel A address write register	NAND_CHA_AWR	W	–
0228H	Channel A last address write register	NAND_CHA_LAWR	W	–
022CH	Channel A data write register	NAND_CHA_DWR	W	–
0230H	Channel A data read register (read trigger write)	NAND_CHA_DRR	W	–
0234H	Channel A byte data write register	NAND_CHA_BDWR	W	–
0238H	Channel A byte data read register (read trigger write)	NAND_CHA_BDRR	W	–
023CH	Channel A flash programming status check register (read trigger write)	NAND_CHA_FPSCR	W	–
0240H	Channel A flash write status register	NAND_CHA_FWSR	R	–
0244H-025FH	Reserved	–	–	–
0260H	Channel B command write register	NAND_CHB_CWR	W	–

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Address	Register Name	Register Symbol	R/W	After Reset
0264H	Channel B address write register	NAND_CHB_AWR	W	–
0268H	Channel B last address write register	NAND_CHB_LAWR	W	–
026CH	Channel B data write register	NAND_CHB_DWR	W	–
0270H	Channel B data read register (read trigger write)	NAND_CHB_DRR	W	–
0274H	Channel B byte data write register	NAND_CHB_BDWR	W	–
0278H	Channel B byte data read register (read trigger write)	NAND_CHB_BDRR	W	–
027CH	Channel B flash programming status check register (read trigger write)	NAND_CHB_FPSCR	W	–
0280H	Channel B flash write status register	NAND_CHB_FWSR	R	–
0284H-029FH	Reserved	–	–	–
02A0H	RS status register	NAND_RSSR	R	0000_0000H
02A4H-02BFH	Reserved	–	–	–
02C0H	Channel A RS error value 0 register	NAND_CHA_RSEV0R	R	0000_0000H
02C4H	Channel A RS error value 1 register	NAND_CHA_RSEV1R	R	0000_0000H
02C8H	Channel A RS error value 2 register	NAND_CHA_RSEV2R	R	0000_0000H
02CCH	Channel A RS error value 3 register	NAND_CHA_RSEV3R	R	0000_0000H
02D0H	Channel A RS error place 0 register	NAND_CHA_RSEP0R	R	0000_0000H
02D4H	Channel A RS error place 1 register	NAND_CHA_RSEP1R	R	0000_0000H
02D8H	Channel A RS error place 2 register	NAND_CHA_RSEP2R	R	0000_0000H
02DCH	Channel A RS error place 3 register	NAND_CHA_RSEP3R	R	0000_0000H
02E0H	Channel B RS error value 0 register	NAND_CHB_RSEV0R	R	0000_0000H
02E4H	Channel B RS error value 1 register	NAND_CHB_RSEV1R	R	0000_0000H
02E8H	Channel B RS error value 2 register	NAND_CHB_RSEV2R	R	0000_0000H
02ECH	Channel B RS error value 3 register	NAND_CHB_RSEV3R	R	0000_0000H
02F0H	Channel B RS error place 0 register	NAND_CHB_RSEP0R	R	0000_0000H
02F4H	Channel B RS error place 1 register	NAND_CHB_RSEP1R	R	0000_0000H
02F8H	Channel B RS error place 2 register	NAND_CHB_RSEP2R	R	0000_0000H
02FCH	Channel B RS error place 3 register	NAND_CHB_RSEP3R	R	0000_0000H
0300H	Channel A spare data hold 0 register	NAND_CHA_SDH0R	R/W	0000_0000H
0304H	Channel A spare data hold 1 register	NAND_CHA_SDH1R	R/W	0000_0000H
0308H	Channel A spare data hold 2 register	NAND_CHA_SDH2R	R/W	0000_0000H
030CH	Channel A spare data hold 3 register	NAND_CHA_SDH3R	R	0000_0000H
0310H	Channel A spare data hold 4 register	NAND_CHA_SDH4R	R	0000_0000H
0314H	Channel A spare data hold 5 register	NAND_CHA_SDH5R	R	0000_0000H
0318H	Channel A spare data hold 6 register	NAND_CHA_SDH6R	R	0000_0000H
031CH	Channel A spare data hold 7 register	NAND_CHA_SDH7R	R	0000_0000H
0320H	Channel B spare data hold 0 register	NAND_CHB_SDH0R	R/W	0000_0000H
0324H	Channel B spare data hold 1 register	NAND_CHB_SDH1R	R/W	0000_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
0328H	Channel B spare data hold 2 register	NAND_CHB_SDH2R	R/W	0000_0000H
032CH	Channel B spare data hold 3 register	NAND_CHB_SDH3R	R	0000_0000H
0330H	Channel B spare data hold 4 register	NAND_CHB_SDH4R	R	0000_0000H
0334H	Channel B spare data hold 5 register	NAND_CHB_SDH5R	R	0000_0000H
0338H	Channel B spare data hold 6 register	NAND_CHB_SDH6R	R	0000_0000H
033CH	Channel B spare data hold 7 register	NAND_CHB_SDH7R	R	0000_0000H
0340H-03FFH	Reserved	–	–	–

(3) PSC block registers (programmable sequencer control (equivalent to command control))

(1/2)

Address	Register Name	Register Symbol	R/W	After Reset
0400H	Programmable sequencer control register	NAND_PSCR	R/W	0000_0000H
0404H	Instruction pointer register	NAND_IPR	R/W	0000_0000H
0408H	Interrupt identification data register	NAND_IIDR	R	0000_0000H
040CH-041FH	Reserved	–	–	–
0420H	Instruction table register (pointer 0H)	NAND_ITR	R/W	0000_0000H
0424H	Instruction table register (pointer 1H)	NAND_ITR	R/W	0000_0000H
0428H	Instruction table register (pointer 2H)	NAND_ITR	R/W	0000_0000H
042CH	Instruction table register (pointer 3H)	NAND_ITR	R/W	0000_0000H
0430H	Instruction table register (pointer 4H)	NAND_ITR	R/W	0000_0000H
0434H	Instruction table register (pointer 5H)	NAND_ITR	R/W	0000_0000H
0438H	Instruction table register (pointer 6H)	NAND_ITR	R/W	0000_0000H
043CH	Instruction table register (pointer 7H)	NAND_ITR	R/W	0000_0000H
0440H	Instruction table register (pointer 8H)	NAND_ITR	R/W	0000_0000H
0444H	Instruction table register (pointer 9H)	NAND_ITR	R/W	0000_0000H
0448H	Instruction table register (pointer AH)	NAND_ITR	R/W	0000_0000H
044CH	Instruction table register (pointer BH)	NAND_ITR	R/W	0000_0000H
0450H	Instruction table register (pointer CH)	NAND_ITR	R/W	0000_0000H
0454H	Instruction table register (pointer DH)	NAND_ITR	R/W	0000_0000H
0458H	Instruction table register (pointer EH)	NAND_ITR	R/W	0000_0000H
045CH	Instruction table register (pointer FH)	NAND_ITR	R/W	0000_0000H
0460H	Instruction table register (pointer 10H)	NAND_ITR	R/W	0000_0000H
0464H	Instruction table register (pointer 11H)	NAND_ITR	R/W	0000_0000H
0468H	Instruction table register (pointer 12H)	NAND_ITR	R/W	0000_0000H
046CH	Instruction table register (pointer 13H)	NAND_ITR	R/W	0000_0000H
0470H	Instruction table register (pointer 14H)	NAND_ITR	R/W	0000_0000H
0474H	Instruction table register (pointer 15H)	NAND_ITR	R/W	0000_0000H

(2/2)

Address	Register Name	Register Symbol	R/W	After Reset
0478H	Instruction table register (pointer 16H)	NAND_ITR	R/W	0000_0000H
047CH	Instruction table register (pointer 17H)	NAND_ITR	R/W	0000_0000H
0480H	Instruction table register (pointer 18H)	NAND_ITR	R/W	0000_0000H
0484H	Instruction table register (pointer 19H)	NAND_ITR	R/W	0000_0000H
0488H	Instruction table register (pointer 1AH)	NAND_ITR	R/W	0000_0000H
048CH	Instruction table register (pointer 1BH)	NAND_ITR	R/W	0000_0000H
0490H	Instruction table register (pointer 1CH)	NAND_ITR	R/W	0000_0000H
0494H	Instruction table register (pointer 1DH)	NAND_ITR	R/W	0000_0000H
0498H	Instruction table register (pointer 1EH)	NAND_ITR	R/W	0000_0000H
049CH	Instruction table register (pointer 1FH)	NAND_ITR	R/W	0000_0000H
04A0H-04FFH	Reserved	–	–	–

(4) LDMA block registers (local bus control)

Address	Register Name	Register Symbol	R/W	After Reset
0600H	Control register	NAND_LCR	R/W	0000_0000H
0604H-0608H	Reserved	–	–	–
060CH	Interrupt control register	NAND_LICR	R/W	0000_0000H
0610H	Interrupt raw status register	NAND_LIRSR	R	0000_0000H
0614H	Interrupt source clear register	NAND_LICLR	W	–
0618H-061CH	Reserved	–	–	–
0620H	LDMA transfer current count register	NAND_TCCR	R	0000_0000H
0624H-067FH	Reserved	–	–	–

A.1.12 IPU (registers related to Graphics DMA functions)

Base address: 4025_0000H

(1/2)

Address	Register Name	Register Symbol	R/W	After Reset
0000H	DMA function setting register	DMA_MODE	R/W	0000_0000H
0004H	DMA processing request register	DMA_REQ	W	0000_0000H
0008H	DMA processing status register	DMA_ACK	R	0000_0000H
000CH	DMA interrupt status register	DMA_STATUS	R	0000_0000H
0010H	DMA interrupt raw status register	DMA_RAWSTATUS	R	0000_0000H
0014H	DMA interrupt enable set register	DMA_ENSET	R/W	0000_0000H
0018H	DMA interrupt enable clear register	DMA_ENCLR	W	0000_0000H
001CH	DMA interrupt source clear register	DMA_FFCLR	W	0000_0000H
0020H	DMA source image 1 address addition value register	DMA_SRCSIZE_1	R/W	0000_0008H
0024H	DMA source image 2 address addition value register	DMA_SRCSIZE_2	R/W	0000_0008H
0028H	DMA destination image address addition value register	DMA_DSTSIZE	R/W	0000_0008H
002CH	Reserved	–	–	–
0030H	DMA source image 1 Y/RGB plane address register	DMA_SRCYRGBADR_1	R/W	0000_0000H
0034H	DMA source image 2 Y/RGB plane address register	DMA_SRCYRGBADR_2	R/W	0000_0000H
0038H	DMA destination image Y/RGB plane address register	DMA_DSTYRGBADR	R/W	0000_0000H
003CH	Reserved	–	–	–
0040H	DMA source image 1 UV plane address register	DMA_SRCUVADR_1	R/W	0000_0000H
0044H	DMA source image 2 UV plane address register	DMA_SRCUVADR_2	R/W	0000_0000H
0048H	DMA destination image UV plane address register	DMA_DSTUVADR	R/W	0000_0000H
004CH	Reserved	–	–	–
0050H	DMA source image 1 V plane address register	DMA_SRCVADR_1	R/W	0000_0000H
0054H	DMA source image 2 V plane address register	DMA_SRCVADR_2	R/W	0000_0000H
0058H	DMA destination image V plane address register	DMA_DSTVADR	R/W	0000_0000H
005CH	Reserved	–	–	–
0060H	DMA horizontal size register	DMA_HSIZE	R/W	0000_0008H
0064H	DMA vertical size register	DMA_VSIZE	R/W	0000_0008H
0068H	DMA mask color register	DMA_MASKCOLR	R/W	0000_0000H
006CH	DMA filling data register	DMA_FILLDATA	R/W	0000_0000H
0070H	DMA image format register	DMA_FORMAT	R/W	0000_0000H
0074H	DMA source image 1 byte lane select register	DMA_SRCBYTE_1	R/W	0000_E4E4H
0078H	DMA source image 2 byte lane select register	DMA_SRCBYTE_2	R/W	0000_E4E4H
007CH	DMA destination image byte lane select register	DMA_DSTBYTE	R/W	0000_E4E4H
0080H	DMA register update reserve setting register	DMA_DUAL_FF	R/W	0000_0000H
0084H-008CH	Reserved	–	–	–

(2/2)

Address	Register Name	Register Symbol	R/W	After Reset
0090H	DMA source image 1 byte lane select register (Y/UV planes divided)	DMA_SRCBYTE_1_CMP	R/W	0000_E4E4H
0094H	DMA source image 2 byte lane select register (Y/UV planes divided)	DMA_SRCBYTE_2_CMP	R/W	0000_E4E4H
0098H	DMA destination image byte lane select register (Y/UV planes divided)	DMA_DSTBYTE_CMP	R/W	0000_E4E4H
009CH	Reserved	–	–	–
00A0H	DMA auto scan register	DMA_AUTO_SCAN	R/W	0000_0000H
00A4H-0FFFH	Reserved	–	–	–

A.1.13 Image composer (IMC)

Base address: 4026_0000H

Caution Among addresses 0000H to FFFCH, the addresses not listed in the following tables are reserved. Write accessing reserved areas is prohibited. An undefined value is returned for read access.

(1/3)

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Control register	IMC_CONTROL	R/W	0000_0000H
0004H	Update reserve register	IMC_REFRESH	R/W	0000_0000H
0010H	Startup register	IMC_START	R/W	0000_0000H
0014H	Status register	IMC_STATUS	R	0000_0000H
0018H	CPU double buffer control register	IMC_CPUBUFSEL	R/W	0000_0000H
0020H	Gamma correction control register	IMC_GAMMA_EN	R/W	0000_0000H
0024H	Gamma correction table address register	IMC_GAMMA_ADR	R/W	0000_0000H
0028H	Gamma correction table data register	IMC_GAMMA_DATA	R/W	0000_0000H
0040H	Display area address register	IMC_WB_AREAADR	R/W	0000_0000H
0044H	Address addition value register	IMC_WB_HOFFSET	R/W	0000_0000H
0048H	Format register	IMC_WB_FORMAT	R/W	0000_0000H
004CH	WB image size register	IMC_WB_SIZE	R/W	0000_0000H
0100H	Horizontal/vertical flip setting register	IMC_MIRROR	R/W	0000_0000H
0104H	Y gain offset register	IMC_YGAINOFFSET	R/W	0000_0080H
0108H	U gain offset register	IMC_UGAINOFFSET	R/W	0000_0080H
010CH	V gain offset register	IMC_VGAINOFFSET	R/W	0000_0080H
0110H	YUV2RGB conversion mode register	IMC_YUV2RGB	R/W	0000_0000H
0114H	Custom coefficient register (Coef R0)	IMC_COEF_R0	R/W	0000_0000H
0118H	Custom coefficient register (Coef R1)	IMC_COEF_R1	R/W	0000_0000H
011CH	Custom coefficient register (Coef R2)	IMC_COEF_R2	R/W	0000_0000H
0120H	Custom coefficient register (Coef R3)	IMC_COEF_R3	R/W	0000_0000H
0124H	Custom coefficient register (Coef G0)	IMC_COEF_G0	R/W	0000_0000H
0128H	Custom coefficient register (Coef G1)	IMC_COEF_G1	R/W	0000_0000H
012CH	Custom coefficient register (Coef G2)	IMC_COEF_G2	R/W	0000_0000H
0130H	Custom coefficient register (Coef G3)	IMC_COEF_G3	R/W	0000_0000H
0134H	Custom coefficient register (Coef B0)	IMC_COEF_B0	R/W	0000_0000H
0138H	Custom coefficient register (Coef B1)	IMC_COEF_B1	R/W	0000_0000H
013CH	Custom coefficient register (Coef B2)	IMC_COEF_B2	R/W	0000_0000H
0140H	Custom coefficient register (Coef B3)	IMC_COEF_B3	R/W	0000_0000H
0200H	Layer 0 control register	IMC_L0_CONTROL	R/W	0000_0000H
0204H	Layer 0 format register	IMC_L0_FORMAT	R/W	0000_0000H
0210H	Layer 0 transparent color control register	IMC_L0_KEYENABLE	R/W	0000_0000H
0214H	Layer 0 transparent control register	IMC_L0_KEYCOLOR	R/W	0000_0000H
0218H	Layer 0 alpha register	IMC_L0_ALPHA	R/W	0000_0000H

(2/3)

Address	Register Name	Register Symbol	R/W	After Reset
0220H	Layer 0 resize register	IMC_L0_RESIZE	R/W	0000_0000H
0230H	Layer 0 address addition value register	IMC_L0_OFFSET	R/W	0000_0000H
0234H	Layer 0 start address register	IMC_L0_FRAMEADR	R/W	0000_0000H
0250H	Layer 0 display position register	IMC_L0_POSITION	R/W	0000_0000H
0254H	Layer 0 display size register	IMC_L0_SIZE	R/W	0000_0000H
0300H	Layer 1A control register	IMC_L1A_CONTROL	R/W	0000_0000H
0304H	Layer 1x format register	IMC_L1X_FORMAT	R/W	0000_0000H
0310H	Layer 1A transparent color control register	IMC_L1A_KEYENABLE	R/W	0000_0000H
0314H	Layer 1x transparent control register	IMC_L1X_KEYCOLOR	R/W	0000_0000H
0318H	Layer 1A alpha register	IMC_L1A_ALPHA	R/W	0000_0000H
0320H	Layer 1x resize register	IMC_L1X_RESIZE	R/W	0000_0000H
0330H	Layer 1x address addition value register	IMC_L1X_OFFSET	R/W	0000_0000H
0334H	Layer 1A start address register	IMC_L1A_FRAMEADR	R/W	0000_0000H
0350H	Layer 1A display position register	IMC_L1A_POSITION	R/W	0000_0000H
0354H	Layer 1A display size register	IMC_L1A_SIZE	R/W	0000_0000H
0400H	Layer 1B control register	IMC_L1B_CONTROL	R/W	0000_0000H
0410H	Layer 1B transparent color control register	IMC_L1B_KEYENABLE	R/W	0000_0000H
0418H	Layer 1B alpha register	IMC_L1B_ALPHA	R/W	0000_0000H
0434H	Layer 1B start address register	IMC_L1B_FRAMEADR	R/W	0000_0000H
0450H	Layer 1B display position register	IMC_L1B_POSITION	R/W	0000_0000H
0454H	Layer 1B display size register	IMC_L1B_SIZE	R/W	0000_0000H
0500H	Layer 1C control register	IMC_L1C_CONTROL	R/W	0000_0000H
0510H	Layer 1C transparent color control register	IMC_L1C_KEYENABLE	R/W	0000_0000H
0518H	Layer 1C alpha register	IMC_L1C_ALPHA	R/W	0000_0000H
0534H	Layer 1C start address register	IMC_L1C_FRAMEADR	R/W	0000_0000H
0550H	Layer 1C display position register	IMC_L1C_POSITION	R/W	0000_0000H
0554H	Layer 1C display size register	IMC_L1C_SIZE	R/W	0000_0000H
0600H	Layer 2A control register	IMC_L2A_CONTROL	R/W	0000_0000H
0604H	Layer 2A format register	IMC_L2A_FORMAT	R/W	0000_0000H
0608H	Layer 2A double buffer control register	IMC_L2A_BUFSEL	R/W	0000_0000H
060CH	Layer 2A byte lane register	IMC_L2A_BYTELANE	R/W	0000_E4E4H
0620H	Layer 2A resize register	IMC_L2A_RESIZE	R/W	0000_0000H
0624H	Layer 2A horizontal/vertical flip control register	IMC_L2A_MIRROR	R/W	0000_0000H
0630H	Layer 2A address addition value register	IMC_L2A_OFFSET	R/W	0000_0000H
0634H	Layer 2A start address register (YP)	IMC_L2A_FRAMEADR_YP	R/W	0000_0000H
0638H	Layer 2A start address register (UP)	IMC_L2A_FRAMEADR_UP	R/W	0000_0000H
063CH	Layer 2A start address register (VP)	IMC_L2A_FRAMEADR_VP	R/W	0000_0000H
0640H	Layer 2A start address register (YQ)	IMC_L2A_FRAMEADR_YQ	R/W	0000_0000H
0644H	Layer 2A start address register (UQ)	IMC_L2A_FRAMEADR_UQ	R/W	0000_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
0648H	Layer 2A start address register (VQ)	IMC_L2A_FRAMEADR_VQ	R/W	0000_0000H
0650H	Layer 2A display position register	IMC_L2A_POSITION	R/W	0000_0000H
0654H	Layer 2A display size register	IMC_L2A_SIZE	R/W	0000_0000H
0700H	Layer 2B control register	IMC_L2B_CONTROL	R/W	0000_0000H
0704H	Layer 2B format register	IMC_L2B_FORMAT	R/W	0000_0000H
0708H	Layer 2B double buffer control register	IMC_L2A_BUFSEL	R/W	0000_0000H
070CH	Layer 2B byte lane register	IMC_L2B_BYTELANE	R/W	0000_E4E4H
0720H	Layer 2B resize register	IMC_L2B_RESIZE	R/W	0000_0000H
0724H	Layer 2B horizontal/vertical flip control register	IMC_L2B_MIRROR	R/W	0000_0000H
0730H	Layer 2B address addition value register	IMC_L2B_OFFSET	R/W	0000_0000H
0734H	Layer 2B start address register (YP)	IMC_L2B_FRAMEADR_YP	R/W	0000_0000H
0738H	Layer 2B start address register (UP)	IMC_L2B_FRAMEADR_UP	R/W	0000_0000H
073CH	Layer 2B start address register (VP)	IMC_L2B_FRAMEADR_VP	R/W	0000_0000H
0740H	Layer 2B start address register (YQ)	IMC_L2B_FRAMEADR_YQ	R/W	0000_0000H
0744H	Layer 2B start address register (UQ)	IMC_L2B_FRAMEADR_UQ	R/W	0000_0000H
0748H	Layer 2B start address register (VQ)	IMC_L2B_FRAMEADR_VQ	R/W	0000_0000H
0750H	Layer 2B display position register	IMC_L2B_POSITION	R/W	0000_0000H
0754H	Layer 2B display size register	IMC_L2B_SIZE	R/W	0000_0000H
0804H	Layer BG format register	IMC_BG_FORMAT	R/W	0000_0000H
0820H	Layer BG resize register	IMC_BG_RESIZE	R/W	0000_0000H
0830H	Layer BG address addition value register	IMC_BG_OFFSET	R/W	0000_0000H
0834H	Layer BG start address register	IMC_BG_FRAMEADR	R/W	0000_0000H
0900H	Interrupt status register	IMC_INTSTATUS	R	0000_0000H
0904H	Interrupt raw status register	IMC_INTRAWSTATUS	R	0000_0000H
0908H	Interrupt enable set register	IMC_INTENSET	R/W	0000_0000H
090CH	Interrupt enable clear register	IMC_INTENCLR	W	0000_0000H
0910H	Interrupt source clear register	IMC_INTFFCLR	W	0000_0000H
0914H	AHBR error address register	IMC_AHBRERRADR	R/W	0000_0000H
0918H	AHBW error address register	IMC_AHBWERRADR	R/W	0000_0000H
1000H	ARGB4444 mode register	IMC_ARGBMODE	R/W	0000_0000H

A.1.14 LCD controller (LCD)

Base address: 4027_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Control register	LCD_CONTROL	R/W	0000_0000H
0004H	Simple QoS setting register	LCD_QOS	R/W	0000_0000H
0008H	Data request cycle register	LCD_DATAREQ	R/W	0000_0000H
0010H	Display register	LCD_LCDOUT	R/W	0000_0000H
0014H	Access bus select register	LCD_BUSSEL	R/W	0000_0000H
0018H	Status register	LCD_STATUS	R	0000_0000H
001CH	Fixed-color output value register	LCD_BACKCOLOR	R/W	0000_0000H
0020H	Display area address register	LCD_AREAADR	R/W	0000_0000H
0024H	Address addition value register	LCD_HOFFSET	R/W	0000_0000H
0028H	Input format register	LCD_IFORMAT	R/W	0000_0000H
002CH	Simple resize register	LCD_RESIZE	R/W	0000_0000H
0030H	Horizontal direction total register	LCD_HTOTAL	R/W	0000_0000H
0034H	Horizontal direction display area register	LCD_HAREA	R/W	0000_0000H
0038H	Horizontal synchronization edge 1 register	LCD_HEDGE1	R/W	0000_0000H
003CH	Horizontal synchronization edge 2 register	LCD_HEDGE2	R/W	0000_0000H
0040H	Vertical direction total register	LCD_VTOTAL	R/W	0000_0000H
0044H	Vertical direction display area register	LCD_VAREA	R/W	0000_0000H
0048H	Vertical synchronization edge 1 register	LCD_VEDGE1	R/W	0000_0000H
004CH	Vertical synchronization edge 2 register	LCD_VEDGE2	R/W	0000_0000H
0050H-005CH	Reserved	–	–	–
0060H	Interrupt status register	LCD_INTSTATUS	R	0000_0000H
0064H	Interrupt raw status register	LCD_INTRAWSTATUS	R	0000_0000H
0068H	Interrupt enable set register	LCD_INTENSET	R/W	0000_0000H
006CH	Interrupt enable clear register	LCD_INTENCLR	W	0000_0000H
0070H	Interrupt source clear register	LCD_INTFFCLR	W	0000_0000H
0074H	Frame count interrupt setting register	LCD_FRAMECOUNT	R/W	0000_0000H

A.1.15 UART0 (U70)

Base address: 5000_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Receive buffer register	RBR	R	Undefined
	Transmit hold register	THR	W	
0004H	Interrupt enable register	IER	R/W	0000H
0008H	Interrupt identification register	IIR	R	0001H
000CH	FIFO control register	FCR	R/W	0000H
0010H	Line control register	LCR	R/W	0000H
0014H	Modem control register	MCR	R/W	0000H
0018H	Line status register	LSR	R	0060H
001CH	Modem status register	MSR	R	000xH
0020H	Scratch register	SCR	R/W	0000H
0024H	Divisor latch LS byte register	DLL	R/W	0000H
0028H	Divisor latch MS byte register	DLM	R/W	0000H
002CH	Hardware control register	HCR0	R/W	0000H
0030H	Hardware status register 2	HCR2	R	0000H
0034H	Hardware status register 3	HCR3	R	0000H
0038H-003CH	Reserved	–	–	–
0040H	IR control register 0	IRCR0	R/W	0000H
0044H	IR control register 1	IRCR1	R/W	0002H
0048H	IR control register 2	IRCR2	R/W	0000H
004CH	IR control register 3	IRCR3	R/W	0000H
0050H	IR control register 4	IRCR4	R/W	0000H

A.1.16 UART1 (U71)

Base address: 5001_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Receive buffer register	RBR	R	Undefined
	Transmit hold register	THR	W	
0004H	Interrupt enable register	IER	R/W	0000H
0008H	Interrupt identification register	IIR	R	0001H
000CH	FIFO control register	FCR	R/W	0000H
0010H	Line control register	LCR	R/W	0000H
0014H	Modem control register	MCR	R/W	0000H
0018H	Line status register	LSR	R	0060H
001CH	Modem status register	MSR	R	000xH
0020H	Scratch register	SCR	R/W	0000H
0024H	Divisor latch LS byte register	DLL	R/W	0000H
0028H	Divisor latch MS byte register	DLM	R/W	0000H
002CH	Hardware control register	HCR0	R/W	0000H
0030H	Hardware status register 2	HCR2	R	0000H
0034H	Hardware status register 3	HCR3	R	0000H
0038H-003CH	Reserved	–	–	–
0040H	IR control register 0	IRCR0	R/W	0000H
0044H	IR control register 1	IRCR1	R/W	0002H
0048H	IR control register 2	IRCR2	R/W	0000H
004CH	IR control register 3	IRCR3	R/W	0000H
0050H	IR control register 4	IRCR4	R/W	0000H

A.1.17 UART2 (U72)

Base address: 5002_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Receive buffer register	RBR	R	Undefined
	Transmit hold register	THR	W	
0004H	Interrupt enable register	IER	R/W	0000H
0008H	Interrupt identification register	IIR	R	0001H
000CH	FIFO control register	FCR	R/W	0000H
0010H	Line control register	LCR	R/W	0000H
0014H	Modem control register	MCR	R/W	0000H
0018H	Line status register	LSR	R	0060H
001CH	Modem status register	MSR	R	000xH
0020H	Scratch register	SCR	R/W	0000H
0024H	Divisor latch LS byte register	DLL	R/W	0000H
0028H	Divisor latch MS byte register	DLM	R/W	0000H
002CH	Hardware control register	HCR0	R/W	0000H
0030H	Hardware status register 2	HCR2	R	0000H
0034H	Hardware status register 3	HCR3	R	0000H
0038H-003CH	Reserved	–	–	–
0040H	IR control register 0	IRCR0	R/W	0000H
0044H	IR control register 1	IRCR1	R/W	0002H
0048H	IR control register 2	IRCR2	R/W	0000H
004CH	IR control register 3	IRCR3	R/W	0000H
0050H	IR control register 4	IRCR4	R/W	0000H

A.1.18 I^2C2 (IIC2)

Base address: 5003_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	IIC0 shift register	IIC2_IIC0	R/W	0000H
0008H	IIC0 control register	IIC2_IICC0	R/W	0000H
000CH	Slave address register	IIC2_SVA0	R/W	0000H
0010H	IIC0 clock select register	IIC2_IICCL0	R/W	0000H
0014H-0018H	Reserved	–	–	–
001CH	IIC0 status register (read-only register for emulation)	IIC2_IICSE0	R	0000H
0020H-0024H	Reserved	–	–	–
0028H	IIC0 flag register	IIC2_IICF0	R/W	0000H

A.1.19 I^2C (IIC)

Base address: 5004_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	IIC0 shift register	IIC_IIC0	R/W	0000H
0008H	IIC0 control register	IIC_IICC0	R/W	0000H
000CH	Slave address register	IIC_SVA0	R/W	0000H
0010H	IIC0 clock select register	IIC_IICCL0	R/W	0000H
0014H-0018H	Reserved	–	–	–
001CH	IIC0 status register (read-only register for emulation)	IIC_IICSE0	R	0000H
0020H-0024H	Reserved	–	–	–
0028H	IIC0 flag register	IIC_IICF0	R/W	0000H

A.1.20 SD0 interface (SDIA)

Base address: 5005_0000H

(1/2)

Address	Register Name	Register Symbol	R/W	After Reset
0000H	SD memory card command register	SDIA_CMD	R/W	0000_0000H
0004H	SD memory card port select register	SDIA_PORT	R/W	0000_0100H
0008H	SD memory card command argument register 0	SDIA_ARG0	R/W	0000_0000H
000CH	SD memory card command argument register 1	SDIA_ARG1	R/W	0000_0000H
0010H	SD stop register	SDIA_STOP	R/W	0000_0000H
0014H	SD memory card transfer sector count register	SDIA_SECCNT	R/W	0000_0000H
0018H	SD memory card response register 0	SDIA_RSP0	RO	0000_0000H
001CH	SD memory card response register 1	SDIA_RSP1	RO	0000_0000H
0020H	SD memory card response register 2	SDIA_RSP2	RO	0000_0000H
0024H	SD memory card response register 3	SDIA_RSP3	RO	0000_0000H
0028H	SD memory card response register 4	SDIA_RSP4	RO	0000_0000H
002CH	SD memory card response register 5	SDIA_RSP5	RO	0000_0000H
0030H	SD memory card response register 6	SDIA_RSP6	RO	0000_0000H
0034H	SD memory card response register 7	SDIA_RSP7	RO	0000_0000H
0038H	SD memory card information register 1	SDIA_INFO1	R/W, RO	Undefined (0000_068DH)
003CH	SD memory card information register 2	SDIA_INFO2	R/W, RO	Undefined (0000_2080H)
0040H	SD memory card information mask register 1	SDIA_INFO1_MASK	R/W	0000_031DH
0044H	SD memory card information mask register 2	SDIA_INFO2_MASK	R/W	0000_8B7FH
0048H	SD memory card transfer clock control register	SDIA_CLK_CTRL	R/W	0000_0020H
004CH	SD memory card transfer data size register	SDIA_SIZE	R/W	0000_0200H
0050H	SD memory card option setting register	SDIA_OPTION	R/W	0000_00EEH
0054H	Reserved	–	–	–
0058H	SD memory card error status register 1	SDIA_ERR_STS1	RO	0000_2000H
005CH	SD memory card error status register 2	SDIA_ERR_STS2	RO	0000_0000H
0060H	SD data buffer 0	SDIA_BUF0	R/W	Undefined
0064H	Reserved	–	–	–
0068H	SDIO mode setting register	SDIA_SDIO_MODE	R/W	0000_0000H
006CH-	SDIO information register	SDIA_SDIO_INFO1	R/W	0000_0000H
0070H	SDIO information mask register	SDIA_SDIO_INFO1_MASK	R/W	0000_C007H
0074H-01ACH	Reserved	–	–	–
01B0H	Extension mode control register	SDIA_CC_EXT_MODE	RO, R/W	0000_1000H

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Address	Register Name	Register Symbol	R/W	After Reset
01B4H-01BCH	Reserved	–	–	–
01C0H	Software reset register	SDIA_SOFT_RST	R/W	0000_0000H
01C4H	Version register	SDIA_VERSION	RO	0000_000BH
01C8H-01E0H	Reserved	–	–	–
0200H	SDIA use register	SDIA_USER	R/W, RO	0000_0004H
0204H	SDIA use 2 register	SDIA_USER2	R/W	0000_0000H
0210H-02FCH	Reserved	–	–	–
0300H	DMA mode SD buffer register	–	R/W	–

A.1.21 SD1 interface (SDIB)

Base address: 5006_0000H

(1/2)

Address	Register Name	Register Symbol	R/W	After Reset
0000H	SD memory card command register	SDIB_CMD	R/W	0000_0000H
0004H	SD memory card port select register	SDIB_PORT	R/W	0000_0100H
0008H	SD memory card command argument register 0	SDIB_ARG0	R/W	0000_0000H
000CH	SD memory card command argument register 1	SDIB_ARG1	R/W	0000_0000H
0010H	SD stop register	SDIB_STOP	R/W	0000_0000H
0014H	SD memory card transfer sector count register	SDIB_SECCNT	R/W	0000_0000H
0018H	SD memory card response register 0	SDIB_RSP0	RO	0000_0000H
001CH	SD memory card response register 1	SDIB_RSP1	RO	0000_0000H
0020H	SD memory card response register 2	SDIB_RSP2	RO	0000_0000H
0024H	SD memory card response register 3	SDIB_RSP3	RO	0000_0000H
0028H	SD memory card response register 4	SDIB_RSP4	RO	0000_0000H
002CH	SD memory card response register 5	SDIB_RSP5	RO	0000_0000H
0030H	SD memory card response register 6	SDIB_RSP6	RO	0000_0000H
0034H	SD memory card response register 7	SDIB_RSP7	RO	0000_0000H
0038H	SD memory card information register 1	SDIB_INFO1	R/W, RO	Undefined (0000_068DH)
003CH	SD memory card information register 2	SDIB_INFO2	R/W, RO	Undefined (0000_2080H)
0040H	SD memory card information mask register 1	SDIB_INFO1_MASK	R/W	0000_031DH
0044H	SD memory card information mask register 2	SDIB_INFO2_MASK	R/W	0000_8B7FH
0048H	SD memory card transfer clock control register	SDIB_CLK_CTRL	R/W	0000_0020H
004CH	SD memory card transfer data size register	SDIB_SIZE	R/W	0000_0200H
0050H	SD memory card option setting register	SDIB_OPTION	R/W	0000_00EEH
0054H	Reserved	–	–	–
0058H	SD memory card error status register 1	SDIB_ERR_STS1	RO	0000_2000H
005CH	SD memory card error status register 2	SDIB_ERR_STS2	RO	0000_0000H
0060H	SD data buffer 0	SDIB_BUF0	R/W	Undefined
0064H	Reserved	–	–	–
0068H	SDIO mode setting register	SDIB_SDIO_MODE	R/W	0000_0000H
006CH	SDIO information register	SDIB_SDIO_INFO1	R/W	0000_0000H
0070H	SDIO information mask register	SDIB_SDIO_INFO1_MASK	R/W	0000_C007H
0074H-01ACH	Reserved	–	–	–
01B0H	Extension mode control register	SDIB_CC_EXT_MODE	RO, R/W	0000_1000H

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Address	Register Name	Register Symbol	R/W	After Reset
01B4H 01BCH	Reserved	–	–	–
01C0H	Software reset register	SDIB_SOFT_RST	R/W	0000_0000H
01C4H	Version register	SDIB_VERSION	RO	0000_000BH
01C8H- 01E0H	Reserved	–	–	–
0200H	SDIB use register	SDIB_USER	R/W, RO	0000_0004H
0204H	SDIB use 2 register	SDIB_USER2	R/W	0000_0000H
0210H- 02FCH	Reserved	–	–	–
0300H	DMA mode SD buffer register	–	R/W	–

A.1.22 Asynchronous bus interface (AB1)

Base address: 5007_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Error information register	AB1_ERROR	R/W	0000_0000H
0004H	Auxiliary register	AB1_GENERAL	R/W	0000_0000H
0008H	Debug register	AB1_DEBUG0	R	0000_0000H

A.1.23 SD2 interface (SDIC)

Base address: 5009_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
0000H	SD memory card command register	SDIC_CMD	R/W	0000_0000H
0004H	SD memory card port select register	SDIC_PORT	R/W	0000_0100H
0008H	SD memory card command argument register 0	SDIC_ARG0	R/W	0000_0000H
000CH	SD memory card command argument register 1	SDIC_ARG1	R/W	0000_0000H
0010H	SD stop register	SDIC_STOP	R/W	0000_0000H
0014H	SD memory card transfer sector count register	SDIC_SECCNT	R/W	0000_0000H
0018H	SD memory card response register 0	SDIC_RSP0	RO	0000_0000H
001CH	SD memory card response register 1	SDIC_RSP1	RO	0000_0000H
0020H	SD memory card response register 2	SDIC_RSP2	RO	0000_0000H
0024H	SD memory card response register 3	SDIC_RSP3	RO	0000_0000H
0028H	SD memory card response register 4	SDIC_RSP4	RO	0000_0000H
002CH	SD memory card response register 5	SDIC_RSP5	RO	0000_0000H
0030H	SD memory card response register 6	SDIC_RSP6	RO	0000_0000H
0034H	SD memory card response register 7	SDIC_RSP7	RO	0000_0000H
0038H	SD memory card information register 1	SDIC_INFO1	R/W, RO	Undefined (0000_068DH)
003CH	SD memory card information register 2	SDIC_INFO2	R/W, RO	Undefined (0000_2080H)
0040H	SD memory card information mask register 1	SDIC_INFO1_MASK	R/W	0000_031DH
0044H	SD memory card information mask register 2	SDIC_INFO2_MASK	R/W	0000_8B7FH
0048H	SD memory card transfer clock control register	SDIC_CLK_CTRL	R/W	0000_0020H
004CH	SD memory card transfer data size register	SDIC_SIZE	R/W	0000_0200H
0050H	SD memory card option setting register	SDIC_OPTION	R/W	0000_00EEH
0054H	Reserved	–	–	–
0058H	SD memory card error status register 1	SDIC_ERR_STS1	RO	0000_2000H
005CH	SD memory card error status register 2	SDIC_ERR_STS2	RO	0000_0000H
0060H	SD data buffer 0	SDIC_BUF0	R/W	UNKNOWN
0064H	Reserved	–	–	–
0068h	SDIO mode setting register	SDIC_SDIO_MODE	R/W	0000_0000H
006CH	SDIO information register	SDIC_SDIO_INFO1	R/W	0000_0000H
0070H	SDIO information mask register	SDIC_SDIO_INFO1_MASK	R/W	0000_C007H
0074H-01ACH	Reserved	–	–	–
01B0H	Extension mode control register	SDIC_CC_EXT_MODE	RO, R/W	0000_1000h

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Address	Register Name	Register Symbol	R/W	After Reset
01B4H-01BCH	Reserved	–	–	–
01C0H	Software reset register	SDIC_SOFT_RST	R/W	0000_0000H
01C4H	Version register	SDIC_VERSION	RO	0000_000BH
01C8H-01E0H	Reserved	–	–	–
0200H	SDIC use register	SDIC_USER	R/W, RO	0000_0004H
0204H	SDIC use 2 register	SDIC_USER2	R/W	0000_0000H
0210H-02FCH	Reserved	–	–	–
0300H	DMA mode SD buffer register	–	R/W	–

A.1.24 USB interface (USB)

Base address: 6000_0000H

(1/2)

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Identification register	ID	R	0042_FA05H
0004H	General HW parameter register	HWGENERAL	R	0000_0085H
0008H	Host HW parameter register	HWHOST	R	1002_0001H
000CH	Device HW parameter register	HWDEVICE	R	0000_0011H
0010H	TX buffer HW parameter register	HWTXBUF	R	0007_0A08H
0014H	RX buffer HW parameter register	HWRXBUF	R	0000_0088H
0018H-007CH	Reserved	–	–	–
0080H	General-purpose timer 0 load register	GPTIMER0LD	R/W	0000_0000H
0084H	General-purpose timer 0 control register	GPTIMER0CTRL	R/W	0000_0000H
0088H	General-purpose timer 1 load register	GPTIMER1LD	R/W	0000_0000H
008CH	General-purpose timer 1 control register	GPTIMER1CTRL	R/W	0000_0000H
0090H-00FCH	Reserved	–	–	–
0100H	Capability register length/ Host IF version number register	CAPLENGTH/ HCIVERSION	R	0100_0040H
0104H	Host control structural parameter register	HCSPARAMS	R	0001_0011H
0108H	Host control capability parameter register	HCCPARAMS	R	0000_0006H
010CH-011FH	Reserved	–	–	–
0120H	Device IF version number register	DCIVERSION	R	0000_0001H
0124H	Host control capability parameter register	DCCPARAMS	R	0000_0188H
0128H-013CH	Reserved	–	–	–
0140H	USB command register	USBCMD	R/W	0008_0000H
0144H	USB status register	USBSTS	R	0000_0000H
0148H	USB interrupt enable register	USBINTR	R/W	0000_0000H
014CH	USB frame index register	FRINDEX	R/W	0000_0000H
0150H	Reserved	–	–	–
0154H	Frame list base address register/ USB device address register	PERIODICLISTBASE Device Addr	R/W	0000_0000H
0158H	Next asynchronous list address register/ Address at endpoint list in memory register	ASYNCLISTADDR Endpointlist Addr	R/W	0000_0000H
015CH	TT status/control register	TTCTRL	R/W	0000_0000H
0160H	Programmable burst size register	BURSTSIZE	R/W	0000_0808H
0164H	Host transmit pre-buffer packet tuning register	TXFILLTUNING	R/W	0000_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
0168H	Host TT transmit pre-buffer packet tuning register	TXTTFILLTUNING		–
016CH	Reserved	–	–	–
0170H	ULPI viewport register	ULPI Viewport		0800_0000H
0174H	Reserved	–	–	–
0178H	Endpoint NAK register	ENDPTNAK		0000_0000H
017CH	Endpoint NAK enable register	ENDPTNAKEN		0000_0000H
0180H	Configuration flag register	CONFIGFLAG		0000_0001H
0184H	Port 1 control/status register	PORTSC1		8000_0x0xH
0188H	Port 2 control/status register	PORTSC2		8000_0x0xH
018CH	Port 3 control/status register	PORTSC3		8000_0x0xH
0190H	Port 4 control/status register	PORTSC4		8000_0x0xH
0194H	Port 5 control/status register	PORTSC5		8000_0x0xH
0198H	Port 6 control/status register	PORTSC6		8000_0x0xH
019CH	Port 7 control/status register	PORTSC7		8000_0x0x**H**
01A0H	Port 8 control/status register	PORTSC8		8000_0x0xH
01A4H	OTG control/status register	OTGSC		0000_0020H
01A8H	USB device mode register	USBMODE		0000_000xH
01ACH	Endpoint setup status register	ENPDTSETUPSTAT		0000_0000H
01B0H	Endpoint initialize register	ENDPTPRIME		0000_0000H
01B4H	Endpoint de-initialize register	ENDPTFLUSH		0000_0000H
01B8H	Endpoint status register	ENDPTSTATUS		0000_0000H
01BCH	Endpoint complete register	ENDPTCOMPLETE		0000_0000H
01C0H	Endpoint 0 control register	ENDPTCTRL0		0800_0080H
01C4H	Endpoint 1 control register	ENDPTCTRL1		0000_0000H
01C8H	Endpoint 2 control register	ENDPTCTRL2		0000_0000H
01CCH	Endpoint 3 control register	ENDPTCTRL3		0000_0000H
01D0H	Endpoint 4 control register	ENDPTCTRL4		0000_0000H
01D4H	Endpoint 5 control register	ENDPTCTRL5		0000_0000H
01D8H	Endpoint 6 control register	ENDPTCTRL6		0000_0000H
01DCH	Endpoint 7 control register	ENDPTCTRL7		0000_0000H
01E0H	Endpoint 8 control register	ENDPTCTRL8		0000_0000H
01E4H	Endpoint 9 control register	ENDPTCTRL9		0000_0000H
01E8H	Endpoint 10 control register	ENDPTCTRL10		0000_0000H
01ECH	Endpoint 11 control register	ENDPTCTRL11		0000_0000H
01F0H	Endpoint 12 control register	ENDPTCTRL12		0000_0000H
01F4H	Endpoint 13 control register	ENDPTCTRL13		0000_0000H
01F8H	Endpoint 14 control register	ENDPTCTRL14		0000_0000H
01FCH	Endpoint 15 control register	ENDPTCTRL15		0000_0000H

A.1.25 Timers (TI0, TI1, TI2, TI3, TW0, TW1, TW2, TW3, TG0, TG1, TG2, TG3, TG4, TG5)

Base address: C000_0000H

PB1_PADDR[31:0]	Module	PB1_PADDR[31:0]	Module
0000H	TI0	2000H	TG0
0100H	TI1	2100H	TG1
0200H	TI2	2200H	TG2
0300H	TI3	2300H	TG3
1000H	TW0	2400H	TG4
1100H	TW1	2500H	TG5
1200H	TW2		
1300H	TW3		

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Timer operation register	xxx_OP	R/W	0000_0000H
0004H	Timer clear register	xxx_CLR	W	0000_0000H
0008H	Timer value setting register	xxx_SET	R/W	0000_0000H
000CH	Real count read register	xxx_RCR	R	0000_0000H
0010H	Reserved	–	–	–
0014H	Timer value setting monitor register	xxx_SCLR	R/W	0000_0000H
0018H-00FCH	Reserved	–	–	–

(xxx = TI0/TI1/TI2/TI3/TW0/TW1/TW2/TW3/TG0/TG1/TG2/TG3/TG4/TG5)

A.1.26 Audio/voice interface (PM0)

Base address: C001_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Operation mode setting register	PM0_FUNC_SEL	R/W	0000_0000H
0004H	Data transfer enable set register	PM0_TXRX_EN	W	–
0008H	Data transfer enable clear register	PM0_TXRX_DIS	W	–
000CH	Data transfer cycle setting register	PM0_CYCLE	R/W	0000_0000H
0010H	Interrupt raw status register	PM0_RAW	R	0000_0000H
0014H	Interrupt status register	PM0_STATUS	R	0000_0000H
0018H	Interrupt enable set register	PM0_ENSET	W	–
001CH	Interrupt enable clear register	PM0_ENCLR	W	–
0020H	Interrupt clear register	PM0_CLEAR	W	–
0024H	Transmit data register	PM0_TXQ	R/W	0000_0000H
0028H	Receive data register	PM0_RXQ	R	0000_0000H
002CH	Reserved	–	–	–
0030H	Data transfer cycle setting register 2	PM0_CYCLE2	R/W	0000_0000H

A.1.27 Interrupt controller unit (AINT)

Base address: C002_0000H

(1/2)

Address	Register Name	Register Symbol	R/W	After Reset
0000H	ACPU interrupt enable setting register 0	IT0_IEN0	R/W	0000_0000H
0004H	ACPU interrupt enable setting register 1	IT0_IEN1	R/W	0000_0000H
0008H	ACPU interrupt disable setting register 0	IT0_IDS0	W	–
000CH	ACPU interrupt disable setting register 1	IT0_IDS1	W	–
0010H	ACPU interrupt raw status register 0	IT0_RAW0	R	0000_0000H
0014H	ACPU interrupt raw status register 1	IT0_RAW1	R	0000_0000H
0018H	ACPU interrupt mask status register 0	IT0_MST0	R	0000_0000H
001CH	ACPU interrupt mask status register 1	IT0_MST1	R	0000_0000H
0020H	Reserved	–	–	–
0024H	ACPU interrupt status reset register	IT0_IIR	W	-
0028H-0038H	Reserved	–	–	–
003CH	ACPU-to-ADSP interprocessor communication set register	IT0_IPI3_SET	R/W	0000_0000H
0040H-0058H	Reserved	–	–	–
005CH	ADSP-to-ACPU interprocessor communication clear register	IT3_IPI0_CLR	W	–
0060H-007CH	Reserved	–	–	–
0080H	ACPU FIQ interrupt enable register	IT0_FIE	R/W	0000_0000H
0084H	ACPU FIQ interrupt disable register	IT0_FID	W	0000_0000H
0088H-00FFH	Reserved	–	–	–
0100H	ACPU interrupt enable setting register 2	IT0_IEN2	R/W	0000_0000H
0104H	ACPU interrupt disable setting register 2	IT0_IDS2	W	–
0108H	ACPU interrupt raw status register 2	IT0_RAW2	R	0000_0000H
010CH	ACPU interrupt mask status register 2	IT0_MST2	R	0000_0000H
0110H-02FCH	Reserved	–	–	–
0300H	Interrupt input polarity inversion enable set register 0	IT_PINV_SET0	R/W	0000_0000H
0304H	Interrupt input polarity inversion enable set register 1	IT_PINV_SET1	R/W	0000_0000H
0308H	Interrupt input polarity inversion enable set register 2	IT_PINV_SET2	R/W	0000_0000H
030CH	Reserved	–	–	–
0310H	Interrupt input polarity inversion disable set register 0	IT_PINV_CLR0	W	–
0314H	Interrupt input polarity inversion disable set register 1	IT_PINV_CLR1	W	–
0318H	Interrupt input polarity inversion disable set register 2	IT_PINV_CLR2	W	–
031CH	Reserved	–	–	–
0320H	Internal interrupt status set register	IT_LIIS	W	0000_0000H
0324H	Internal interrupt status reset register	IT_LIIR	W	0000_0000H
0328H-1FFCH	Reserved	–	–	–

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Address	Register Name	Register Symbol	R/W	After Reset
C000H	ADSP interrupt enable setting register 0	IT3_IEN0	R/W	0000_0000H
C004H	ADSP interrupt enable setting register 1	IT3_IEN1	R/W	0000_0000H
C008H	ADSP interrupt disable setting register 0	IT3_IDS0	W	–
C00CH	ADSP interrupt disable setting register 1	IT3_IDS1	W	–
C010H	ADSP interrupt raw status register 0	IT3_RAW0	R	0000_0000H
C014H	ADSP interrupt raw status register 1	IT3_RAW1	R	0004_0000H
C018H	ADSP interrupt mask status register 0	IT3_MST0	R	0000_0000H
C01CH	ADSP interrupt mask status register 1	IT3_MST1	R	0000_0000H
C020H	Reserved	–	–	–
C024H	ADSP interrupt status reset register	IT3_IIR	W	–
C028H-C02CH	Reserved	–	–	–
C030H	ADSP-to-ACPU interprocessor communication set register	IT3_IPI0_SET	R/W	0000_0000H
C034H-C04CH	Reserved	–	–	–
C050H	ACPU-to-ADSP interprocessor communication clear register	IT0_IPI3_CLR	W	–
C054H-C08FH	Reserved	–	–	–
C090H	Interrupt vector base address register	ID_VBS	R/W	0000_0000H
C094H	Interrupt output signal clear register	ID_CLR	W	–
C098H-C0FFH	Reserved	–	–	–
C100H	ADSP interrupt enable setting register 2	IT3_IEN2	R/W	0000_0000H
C104H	ADSP interrupt disable setting register 2	IT3_IDS2	W	–
C108H	ADSP interrupt raw status register 2	IT3_RAW2	R	0000_0000H
C10CH	ADSP interrupt mask status register 2	IT3_MST2	R	0000_0000H
C110H-DFFCH	Reserved	–	–	–

A.1.28 ACPU Secure INT (ACPU secure interrupt controller unit)

Base address: CC01_0000H

Address	Register Name	Register Symbol	R/W	After Reset
E000H-E1FFH	Reserved	–	–	–
E200H	ACPU secure interrupt enable setting register 0	IT0_IENS0	R/W	0000_0000H
E204H	ACPU secure interrupt enable setting register 1	IT0_IENS1	R/W	0000_0000H
E208H	ACPU secure interrupt enable setting register 2	IT0_IENS2	R/W	0000_0000H
E20CH	ACPU secure interrupt disable setting register 0	IT0_IDSS0	W	–
E210H	ACPU secure interrupt disable setting register 1	IT0_IDSS1	W	–
E214H	ACPU secure interrupt disable setting register 2	IT0_IDSS2	W	–
E218H-FFFCH	Reserved	–	–	–

A.1.29 General-purpose I/O interface (GIO)

Base address: C005_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
0000H	GPIO[31:0] port switch setting register (output setting)	GIO_E1_L	W	0000_0000H
0004H	GPIO[31:0] port switch setting register (input setting)	GIO_E0_L	W	0000_0000H
0004H	GPIO[31:0] I/O port status monitor register	GIO_EM_L	R	0000_0000H
0008H	GPIO[15:0] output data setting register	GIO_OL_L	W	0000_0000H
000CH	GPIO[31:16] output data setting register	GIO_OH_L	W	0000_0000H
0010H	GPIO[31:0] input data read register	GIO_I_L	R	–
0014H	GPIO[31:0] input port interrupt enable specification register	GIO_IIA_L	R/W	0000_0000H
0018H	GPIO[31:0] input port interrupt enable register (mask cancel)	GIO_IEN_L	W	0000_0000H
001CH	GPIO[31:0] input port interrupt disable register (mask setting)	GIO_IDS_L	W	0000_0000H
001CH	GPIO[31:0] input port interrupt enable monitor register	GIO_IIM_L	R	0000_0000H
0020H	GPIO[31:0] input port interrupt raw status register	GIO_RAW_L	R	0000_0000H
0024H	GPIO[31:0] input port interrupt maskable status register	GIO_MST_L	R	0000_0000H
0028H	GPIO[31:0] input port interrupt source reset register	GIO_IIR_L	W	0000_0000H
002CH-0030H	Reserved	–	–	–
003CH	GPIO[31:0]GIO_INT_FIQ pin connection register	GIO_GSW_L	R/W	0000_0000h
0100H	GPIO[7:0] input port interrupt detection mode register	GIO_IDT0_L	R/W	0000_0000H
0104H	GPIO[15:8] input port interrupt detection mode register	GIO_IDT1_L	R/W	0000_0000H
0108H	GPIO[23:16] input port interrupt detection mode register	GIO_IDT2_L	R/W	0000_0000H
010CH	GPIO[31:24] input port interrupt detection mode register	GIO_IDT3_L	R/W	0000_0000H
0110H	GPIO[15:0] interrupt status register (in both edge detection mode)	GIO_RAWBL_L	R	0000_0000H
0114H	GPIO[31:16] interrupt status register (in both edge detection mode)	GIO_RAWBH_L	R	0000_0000H
0118H	GPIO[15:0] interrupt source clear register (in both edge detection mode)	GIO_IRBL_L	W	0000_0000H
011CH	GPIO[31:16] interrupt source clear register (in both edge detection mode)	GIO_IRBH_L	W	0000_0000H
0040H	GPIO[63:32] port switch setting register (output setting)	GIO_E1_H	W	0000_0000H
0044H	GPIO[63:32] port switch setting register (input setting)	GIO_E0_H	W	0000_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
0044H	GPIO[63:32] I/O port status monitor register	GIO_EM_H	R	0000_0000H
0048H	GPIO[47:32] output data setting register	GIO_OL_H	W	0000_0000H
004CH	GPIO[63:48] output data setting register	GIO_OH_H	W	0000_0000H
0050H	GPIO[63:32] input data read register	GIO_I_H	R	–
0054H	GPIO[63:32] input port interrupt enable specification register	GIO_IIA_H	R/W	0000_0000H
0058H	GPIO[63:32] input port interrupt enable register (mask cancel)	GIO_IEN_H	W	0000_0000H
005CH	GPIO[63:32] input port interrupt disable register (mask setting)	GIO_IDS_H	W	0000_0000H
005CH	GPIO[63:32] input port interrupt enable monitor register	GIO_IIM_H	R	0000_0000H
0060H	GPIO[63:32] input port interrupt raw status register	GIO_RAW_H	R	0000_0000H
0064H	GPIO[63:32] input port interrupt maskable status register	GIO_MST_H	R	0000_0000H
0068H	GPIO[63:32] input port interrupt source reset register	GIO_IIR_H	W	0000_0000H
006CH-0070H	Reserved	–	–	–
007CH	GPIO[63:32] GIO_INT_FIQ pin connection register	GIO_GSW_H	R/W	0000_0000H
0140H	GPIO[39:32] input port interrupt detection mode register	GIO_IDT0_H	R/W	0000_0000H
0144H	GPIO[47:40] input port interrupt detection mode register	GIO_IDT1_H	R/W	0000_0000H
0148H	GPIO[55:48] input port interrupt detection mode register	GIO_IDT2_H	R/W	0000_0000H
014CH	GPIO[63:56] input port interrupt detection mode register	GIO_IDT3_H	R/W	0000_0000H
0150H	GPIO[47:32] interrupt status register (in both edge detection mode)	GIO_RAWBL_H	R	0000_0000H
0154H	GPIO[63:48] interrupt status register (in both edge detection mode)	GIO_RAWBH_H	R	0000_0000H
0158H	GPIO[47:32] interrupt source clear register (in both edge detection mode)	GIO_IRBL_H	W	0000_0000H
015CH	GPIO[63:48] interrupt source clear register (in both edge detection mode)	GIO_IRBH_H	W	0000_0000H
0080H	GPIO[95:64] port switch setting register (output setting)	GIO_E1_HH	W	0000_0000H
0084H	GPIO[95:64] port switch setting register (input setting)	GIO_E0_HH	W	0000_0000H
0084H	GPIO[95:64] I/O port status monitor register	GIO_EM_HH	R	0000_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
0088H	GPIO[79:64] output data setting register	GIO_OL_HH	W	0000_0000H
008CH	GPIO[95:80] output data setting register	GIO_OH_HH	W	0000_0000H
0090H	GPIO[95:64] input data read register	GIO_I_HH	R	–
0094H	GPIO[95:64] input port interrupt enable specification register	GIO_IIA_HH	R/W	0000_0000H
0098H	GPIO[95:64] input port interrupt enable register (mask cancel)	GIO_IEN_HH	W	0000_0000H
009CH	GPIO[95:64] input port interrupt disable register (mask setting)	GIO_IDS_HH	W	0000_0000H
009CH	GPIO[95:64] input port interrupt enable monitor register	GIO_IIM_HH	R	0000_0000H
00A0H	GPIO[95:64] input port interrupt raw status register	GIO_RAW_HH	R	0000_0000H
00A4H	GPIO[95:64] input port interrupt maskable status register	GIO_MST_HH	R	0000_0000H
00A8H	GPIO[95:64] input port interrupt source reset register	GIO_IIR_HH	W	0000_0000H
00ACH-00B0H	Reserved	–	–	–
00BCH	GPIO[95:64] GIO_INT_FIQ pin connection register	GIO_GSW_HH	R/W	0000_0000H
0180H	GPIO[71:64] input port interrupt detection mode register	GIO_IDT0_HH	R/W	0000_0000H
0184H	GPIO[79:72] input port interrupt detection mode register	GIO_IDT1_HH	R/W	0000_0000H
0188H	GPIO[87:80] input port interrupt detection mode register	GIO_IDT2_HH	R/W	0000_0000H
018CH	GPIO[95:88] input port interrupt detection mode register	GIO_IDT3_HH	R/W	0000_0000H
0190H	GPIO[71:64] interrupt status register (in both edge detection mode)	GIO_RAWBL_HH	R	0000_0000H
0194H	GPIO[79:72] interrupt status register (in both edge detection mode)	GIO_RAWBH_HH	R	0000_0000H
0198H	GPIO[87:80] interrupt source clear register (in both edge detection mode)	GIO_IRBL_HH	W	0000_0000H
019CH	GPIO[95:88] interrupt source clear register (in both edge detection mode)	GIO_IRBH_HH	W	0000_0000H
0200H	GPIO[127:96] port switch setting register (output setting)	GIO_E1_HHH	W	0000_0000H
0204H	GPIO[127:96] port switch setting register (input setting)	GIO_E0_HHH	W	0000_0000H
0204H	GPIO[127:96] I/O port status monitor register	GIO_EM_HHH	R	0000_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
0208H	GPIO[111:96] output data setting register	GIO_OL_HHH	W	0000_0000H
020CH	GPIO[127:112] output data setting register	GIO_OH_HHH	W	0000_0000H
0210H	GPIO[127:96] input data read register	GIO_I_HHH	R	–
0214H	GPIO[127:96] input port interrupt enable specification register	GIO_IIA_HHH	R/W	0000_0000H
0218H	GPIO[127:96] input port interrupt enable register (mask cancel)	GIO_IEN_HHH	W	0000_0000H
021CH	GPIO[127:96] input port interrupt disable register (mask setting)	GIO_IDS_HHH	W	0000_0000H
021CH	GPIO[127:96] input port interrupt enable monitor register	GIO_IIM_HHH	R	0000_0000H
0220H	GPIO[127:96] input port interrupt raw status register	GIO_RAW_HHH	R	0000_0000H
0224H	GPIO[127:96] input port interrupt maskable status register	GIO_MST_HHH	R	0000_0000H
0228H	GPIO[127:96] input port interrupt source reset register	GIO_IIR_HHH	W	0000_0000H
022CH-0230H	Reserved	–	–	–
023CH	GPIO[127:96] GIO_INT_FIQ pin connection register	GIO_GSW_HHH	R/W	0000_0000H
0300H	GPIO[103:96] input port interrupt detection mode register	GIO_IDT0_HHH	R/W	0000_0000H
0304H	GPIO[111:104] input port interrupt detection mode register	GIO_IDT1_HHH	R/W	0000_0000H
0308H	GPIO[119:112] input port interrupt detection mode register	GIO_IDT2_HHH	R/W	0000_0000H
030CH	GPIO[127:120] input port interrupt detection mode register	GIO_IDT3_HHH	R/W	0000_0000H
0310H	GPIO[103:96] interrupt status register (in both edge detection mode)	GIO_RAWBL_HHH	R	0000_0000H
0314H	GPIO[111:104] interrupt status register (in both edge detection mode)	GIO_RAWBH_HHH	R	0000_0000H
0318H	GPIO[119:112] interrupt source clear register (in both edge detection mode)	GIO_IRBL_HHH	W	0000_0000H
031CH	GPIO[127:120] interrupt source clear register (in both edge detection mode)	GIO_IRBH_HHH	W	0000_0000H

A.1.30 PCM DMA (PDMA)

Base address: C008_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	PDMA/DMA selection register (exclusively switched)	PDMA_DMA_SEL	R/W	0000_0000H
0004H	Transfer start/reserve register (used for both starting and reserving transfer)	PDMA_CONT	W	0000_0000H
0008H	Status register (stopped/transferring/reserved)	PDMA_STATUS	R	0000_0000H
000CH	Reservation cancel register	PDMA_RSV_CANCEL	W	0000_0000H
0010H	Forced end register	PDMA_END	W	0000_0000H
0014H-001CH	Reserved	–	–	–
0020H	Transfer start address register (for reservation, 4-byte alignment)	PDMA_RSV_ADD	R/W	0000_0000H
0024H	Transfer length register (for reservation, in word (4 bytes) units)	PDMA_RSV_LENG	R/W	0000_0000H
0028H	Transfer start address register (during transfer, 4-byte alignment)	PDMA_RUN_ADD	R	0000_0000H
002CH	Transfer length register (during transfer, in word (4 bytes) units)	PDMA_RUN_LENG	R	0000_0000H
0030H	Interrupt status register	PDMA_INT_STATUS	R	0000_0000H
0034H	Interrupt raw status register	PDMA_INT_RAW_STATUS	R	0000_0000H
0038H	Interrupt enable set register	PDMA_INT_ENABLE	R/W	0000_0000H
003CH	Interrupt enable clear register	PDMA_INT_ENABLE_CL	W	0000_0000H
0040H	Interrupt source clear register	PDMA_INT_REQ_CL	W	0000_0000H
0050H	Address pointer register (during transfer, 4-byte alignment)	PDMA_RUN_ADP	R	0000_0000H
0054H	Error register (operational violation)	PDMA_ERR	R/W	0000_0000H
0058H	Temporary register (can be used for reservation management)	PDMA_TMP	R/W	0000_0000H
005CH	AXI address pointer (for debugging)	PDMA_AXI_ADP	R	0000_0000H

A.1.31 DDR SDRAM interface (MEMC)

Base address: C00A_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Cache/prefetch setting register	MEMC_CACHE_MODE	R/W	0000_0000H
0004H	Reserved	–	–	–
0008H	Degenerate function register	MEMC_DEGFUN	R/W	0000_0000H
000CH	Reserved	–	–	–
0010H	Reserved	–	–	–
0014H	ACPU interrupt status register	MEMC_INTSTATUS_A	R	0000_0000H
0018H	ACPU interrupt raw status register	MEMC_INTRAWSTATUS_A	R	0000_0000H
001CH	ACPU interrupt enable set register	MEMC_INTENSET_A	R/W	0000_0000H
0020H	ACPU interrupt enable clear register	MEMC_INTENCLR_A	W	–
0024H	ACPU interrupt source clear register	MEMC_INTFFCLR_A	W	–
0028H-0064H	Reserved	–	–	–
0068H	Error master ID register	MEMC_ERRMID	R	0000_0000H
006CH	Error address register	MEMC_ERRADR	R/W	0000_0000H
0070H-0080H	Reserved	–	–	–
1000H	Memory request scheduling mode register	MEMC_REQSCH	R/W	0000_0000H
2000H	Memory connection register	MEMC_DDR_CONFIGF	R/W	0000_0000H
2004H	AC timing setting register 1	MEMC_DDR_CONFIGA1	R/W	5444_3203H
2008H	AC timing setting register 2	MEMC_DDR_CONFIGA2	R/W	00DA_0000H
200CH	Software command issuance register 1	MEMC_DDR_CONFIGC1	R/W	4040_0003H
2010H	Software command issuance register 2	MEMC_DDR_CONFIGC2	R/W	0000_03C0H
2014H	Refresh function setting register 1	MEMC_DDR_CONFIGR1	R/W	7FFF_7FFFH
2018H	Refresh function setting register 2	MEMC_DDR_CONFIGR2	R/W	1F5F_7C7CH
201CH	Refresh function setting register 3	MEMC_DDR_CONFIGR3	R/W	0000_3F3FH
2020H	Automatic DQS timing setting register 1	MEMC_DDR_CONFIGT1	R/W	0000_0003H
2024H	Automatic DQS timing setting register 2	MEMC_DDR_CONFIGT2	R/W	0000_0000H
2028H	Automatic DQS timing setting register 3	MEMC_DDR_CONFIGT3	R/W	0000_0000H
202CH	Memory status check register	MEMC_DDR_STATE8	R/W	0000_0000H

A.1.32 ADSP address converter (DCV)

Base address: C00D_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	DSP-bank 0 corresponding offset setting register	DCV_BANK0_OFFSET	R/W	0000_0200H
0004H	DSP-bank 1 corresponding offset setting register	DCV_BANK1_OFFSET	R/W	0000_0000H
0008H	DSP-bank 2 corresponding offset setting register	DCV_BANK2_OFFSET	R/W	0000_0000H
000CH	DSP-bank 3 corresponding offset setting register	DCV_BANK3_OFFSET	R/W	0000_0000H
0010H	DSP-bank 4 corresponding offset setting register	DCV_BANK4_OFFSET	R/W	0000_0100H
0014H	DSP-bank 5 corresponding offset setting register	DCV_BANK5_OFFSET	R/W	0000_0000H
0018H	DSP-bank 6 corresponding offset setting register	DCV_BANK6_OFFSET	R/W	0000_0000H
001CH	DSP-bank 7 corresponding offset setting register	DCV_BANK7_OFFSET	R/W	0000_0000H
0020H	DSP-bank 8 corresponding offset setting register	DCV_BANK8_OFFSET	R/W	0000_0240H
0024H	DSP-bank 9 corresponding offset setting register	DCV_BANK9_OFFSET	R/W	0000_0000H
0028H	DSP-bank 10 corresponding offset setting register	DCV_BANK10_OFFSET	R/W	0000_0000H
002CH	DSP-bank 11 corresponding offset setting register	DCV_BANK11_OFFSET	R/W	0000_0000H
0030H	DSP-bank 12 corresponding offset setting register	DCV_BANK12_OFFSET	R/W	0000_0000H
0034H	DSP-bank 13 corresponding offset setting register	DCV_BANK13_OFFSET	R/W	0000_0000H
0038H	DSP-bank 14 corresponding offset setting register	DCV_BANK14_OFFSET	R/W	0000_0000H
003CH	DSP-bank 15 corresponding offset setting register	DCV_BANK15_OFFSET	R/W	0000_0000H
0040H	DSP-bank 0 correspondence setting register	DCV_BANK0_SET	R/W	0000_0003H
0044H	DSP-bank 1 correspondence setting register	DCV_BANK1_SET	R/W	0000_0000H
0048H	DSP-bank 2 correspondence setting register	DCV_BANK2_SET	R/W	0000_0000H
004CH	DSP-bank 3 correspondence setting register	DCV_BANK3_SET	R/W	0000_0000H
0050H	DSP-bank 4 correspondence setting register	DCV_BANK4_SET	R/W	0000_0003H
0054H	DSP-bank 5 correspondence setting register	DCV_BANK5_SET	R/W	0000_0000H
0058H	DSP-bank 6 correspondence setting register	DCV_BANK6_SET	R/W	0000_0000H
005CH	DSP-bank 7 correspondence setting register	DCV_BANK7_SET	R/W	0000_0000H
0060H	DSP-bank 8 correspondence setting register	DCV_BANK8_SET	R/W	0000_0003H
0064H	DSP-bank 9 correspondence setting register	DCV_BANK9_SET	R/W	0000_0000H
0068H	DSP-bank 10 correspondence setting register	DCV_BANK10_SET	R/W	0000_0000H
006CH	DSP-bank 11 correspondence setting register	DCV_BANK11_SET	R/W	0000_0000H
0070H	DSP-bank 12 correspondence setting register	DCV_BANK12_SET	R/W	0000_0004H
0074H	DSP-bank 13 correspondence setting register	DCV_BANK13_SET	R/W	0000_000CH
0078H	DSP-bank 14 correspondence setting register	DCV_BANK14_SET	R/W	0000_000AH
007CH	DSP-bank 15 correspondence setting register	DCV_BANK15_SET	R/W	0000_0000H
0080H	Interrupt status register	DCV_INTSTATUS	R	0000_0000H
0084H	Interrupt raw status register	DCV_INTRAWSTATUS	R	0000_0000H
0088H	Interrupt enable set register	DCV_INTENSET	R/W	0000_0000H
008CH	Interrupt enable clear register	DCV_INTENCLR	R/W	0000_0000H
0090H	Interrupt source clear register	DCV_INTFFCLR	R/W	0000_0000H
0094H	Interrupt information register	DCV_INTINFO	R/W	0000_0000H

A.1.33 Power management unit (PMU)

Base address: C010_0004H

Address	Register Name	Register Symbol	R/W	After Reset
0004H	Program counter (command RAM address) register	PMU_PC	R/W	0000_0000H
0008H	PMU start register	PMU_START	R/W	0000_0000H
0030H	Power-on sequence start PC register	PMU_POWER_ON_PC	R/W	0000_0000H
0060H	WDT count enable register	PMU_WDT_COUNT_EN	R/W	0000_0000H
0064H	WDT count limit register	PMU_WDT_COUNT_LMT	R/W	0003_FFFFH
0068H	Interrupt handler PC	PMU_INT_HANDLER_PC	R/W	0000_0000H
0070H	Program status register	PMU_PSR	R	0000_0000H
0074H	TRIG_WAIT command status register	PMU_TRIG_STATUS	R	0000_0000H
0078H	General-purpose register A	PMU_REGA	R	0000_0000H
007CH	General-purpose register B	PMU_REGB	R	0000_0000H
0080H	ACPU interrupt status register	PMU_INTSTATUS_A	R	0000_0000H
0084H	ACPU interrupt raw status register	PMU_INTRAWSTATUS_A	R	0000_0000H
0088H	ACPU interrupt enable set register	PMU_INTENSET_A	R/W	0000_0000H
008CH	ACPU interrupt enable clear register	PMU_INTENCLR_A	W	0000_0000H
0090H	ACPU interrupt source clear register	PMU_INTFFCLR_A	W	0000_0000H
00A8H	PC error address register	PMU_PCERR	R/W	0000_0000H
1000H-1FFCH	Command buffer RAM register (1024 words from 1000H to 1FFCH)	PMU_CMD_BUF_RAM	R/W	–
2000H-203CH	Command buffer FF register (16 words from 2000H to 203CH)	PMU_CMD_BUF_FF	R/W	–

A.1.34 System management unit (ASMU)

Base address: C011_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
0000H	Reset control register 0	RESETCTRL0	R/W	0000_0000H
0004H	Reset request register 0	RESETREQ0	R/W	8790_0007H
0008H	RESETREQ0 set/reset enable register	RESETREQ0ENA	R/W	0000_0000H
000CH	Reset request register 1	RESETREQ1	R/W	0000_0090H
0010H	RESETREQ1 set/reset enable register	RESETREQ1ENA	R/W	0000_0000H
0014H	Reserved	–	–	–
0018H	Reset request register 2	RESETREQ2	R/W	0000_140FH
001CH	RESETREQ2 set/reset enable register	RESETREQ2ENA	R/W	0000_0000H
0020H	Watchdog timer forced reset control register	WDT_INT_RESET	R/W	0000_0000H
0024H	Inserted clock setting register	RESET_PCLK_COUNT	R/W	1F1F_1F1FH
0028H-0078H	Reserved	–	–	–
007CH	Automatic mode transition enable register	AUTO_MODE_EN	R/W	0000_0000H
0080H	Clock mode selection register	CLK_MODE_SEL	R/W	0000_0F00H
0084H	PLL1 for system setting register 0	PLL1CTRL0	R/W	0000_0079H
0088H	PLL1 for system setting register 1	PLL1CTRL1	R/W	0000_00FFH
008CH	Serial clock PLL2 setting register 0	PLL2CTRL0	R/W	0000_0079H
0090H	Serial clock PLL2 setting register 1	PLL2CTRL1	R/W	0000_00FFH
0094H	PLL3 for system setting register 0	PLL3CTRL0	R/W	0000_0037H
0098H	PLL3 for system setting register 1	PLL3CTRL1	R/W	0000_0000H
009CH	PLL lockup time setting register	PLLLOCKTIME	R/W	0003_0003H
00A0H-00A4H	Reserved	–	–	–
00A8H	Automatic PLL standby mode register	AUTO_PLL_STANDBY	R/W	0000_0002H
00ACH-00B0H	Reserved	–	–	–
00B4H	PLL power stabilization time setting register	PLLVDDWAIT	R/W	0000_0000H
00B8H-00C0H	Reserved	–	–	–
00C4H	Clock stop instruction signal status register	CLKSTOPSIG_ST	R	–
00C8H	32.768 kHz clock status register	CLK32_STATUS	R	–
00CCH	General-purpose register for power record	POWER_RECORD	R/W	0000_0000H
00D0H	Interrupt status register	ASMU_INT_STATUS	R	0000_0000H
00D4H	Interrupt raw status register	ASMU_INT_RAW_STATUS	R	0000_0000H
00D8H	Interrupt enable set register	ASMU_INT_ENSET	R/W	0000_0000H
00DCH	Interrupt enable clear register	ASMU_INT_ENCLR	W	0000_0000H
00E0H	Interrupt enable monitor register	ASMU_INT_ENMON	R	0000_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
00E4H	Interrupt clear register	ASMU_INT_CLEAR	W	0000_0000H
00F0H	Normal mode A clock frequency division setting register	NORMALA_DIV	R/W	0035_5300H
00F4H	Normal mode B clock frequency division setting register	NORMALB_DIV	R/W	0035_5300H
00F8H	Normal mode C clock frequency division setting register	NORMALC_DIV	R/W	0035_5300H
00FCH	Normal mode D clock frequency division setting register	NORMALD_DIV	R/W	0035_5300H
0100H	Economy mode clock frequency division setting register	ECONOMY_DIV	R/W	0035_5500H
0104H	Standby/Sleep mode clock frequency division setting register	STANDBY_DIV	R/W	0055_5500H
0108H	Power ON mode clock frequency division setting register	POWERON_DIV	R/W	0013_3100H
0110H-0114H	Reserved	–	–	–
0118H	SP0_SCLK frequency division setting register	DIVSP0SCLK	R/W	0000_0004H
011CH	SP1_SCLK frequency division setting register	DIVSP1SCLK	R/W	0000_0004H
0120H	SP2_SCLK frequency division setting register	DIVSP2SCLK	R/W	0000_0004H
0124H	Reserved	–	–	–
0128H	MEMC_RCLK frequency division setting register	DIVMEMCRCLK	R/W	0000_0004H
012CH	CAM_SCLK frequency division setting register	DIVCAMSCLK	R/W	0000_0119H
0130H	LCD_LCLK frequency division setting register	DIVLCDLCLK	R/W	0000_0190H
0134H	IIC_SCLK frequency division setting register	DIVIICSCLK	R/W	0053_0053H
0138H	TI0_TIN / TW0_TIN setting register	TI0TIN_SEL	R/W	0001_0001H
013CH	TI1_TIN / TW1_TIN setting register	TI1TIN_SEL	R/W	0001_0001H
0140H	TI2_TIN / TW2_TIN setting register	TI2TIN_SEL	R/W	0001_0001H
0144H	TI3_TIN / TW3_TIN setting register	TI3TIN_SEL	R/W	0001_0001H
0148H	TG0-5_TIN setting register	TGnTIN_SEL	R/W	0011_1111H
014CH	Timer clock frequency division setting register	DIVTIMTIN	R/W	0000_00F4H
0150H	MWI_SCLK frequency division setting register	DIVMWISCLK	R/W	0000_00F4H
0154H	DMA_TCLK frequency division setting register	DIVDMATCLK	R/W	0000_00F4H
0158H	U70_SCLK frequency division setting register	DIVU70SCLK	R/W	0000_00F4H
015CH	U71_SCLK frequency division setting register	DIVU71SCLK	R/W	0000_00F4H
0160H	U72_SCLK frequency division setting register	DIVU72SCLK	R/W	0000_00F4H
0164H-0168H	Reserved	–	–	–
016CH	PM0_SCLK frequency division setting register	DIVPM0SCLK	R/W	0000_00F4H
0170H	PM1_SCLK frequency division setting register	DIVPM1SCLK	R/W	0000_00F4H

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Address	Register Name	Register Symbol	R/W	After Reset
0174H	Reserved	–	–	–
0178H	REFCLK frequency division setting register	DIVREFCLK	R/W	0000_0028H
017CH-0180H	Reserved	–	–	–
0184H	PWMPWCLK frequency division setting register	DIVPWMPWCLK	R/W	00F4_00F4H
0188H-0194H	Reserved	–	–	–
01A0H	AHB macro clock control register 0	AHBCLKCTRL0	R/W	0000_0000H
01A4H	AHB macro clock control register 1	AHBCLKCTRL1	R/W	0000_0000H
01A8H	APB slave macro clock control register 0	APBCLKCTRL0	R/W	0000_0000H
01ACH	APB slave macro clock control register 1	APBCLKCTRL1	R/W	0000_0000H
01B0H	Clock control register	CLKCTRL	R/W	0000_0000H
01B4H	Macro clock gate control register 0	GCLKCTRL0	R/W	767F_FCE3H
01B8H	GCLKCTRL0 set/reset enable register	GCLKCTRL0ENA	R/W	0000_0000H
01BCH	Macro clock gate control register 1	GCLKCTRL1	R/W	FFFF_DFF7H
01C0H	GCLKCTRL1 set/reset enable register	GCLKCTRL1ENA	R/W	0000_0000H
01C4H	Macro clock gate control register 2	GCLKCTRL2	R/W	67F0_79FEH
01C8H	GCLKCTRL2 set/reset enable register	GCLKCTRL2ENA	R/W	0000_0000H
01CCH	Macro clock gate control register 3	GCLKCTRL3	R/W	3FF8_7FFFH
01D0H	GCLKCTRL3 set/reset enable register	GCLKCTRL3ENA	R/W	3800_0000H
01D4H-01D8H	Reserved	–	–	–
01DCH	Automatic frequency switch control register	AUTO_FRQ_CHANGE	R/W	3000_0000H
01E0H	Automatic frequency switch control register REQMASK 0	AUTO_FRQ_MASK0	R/W	0000_0000H
01E4H	Automatic frequency switch control register REQMASK 1	AUTO_FRQ_MASK1	R/W	0007_ DCFCH
01E8H	Automatic frequency control half mode register	DFS_HALFMODE	R/W	0000_0000H
01F0H	FLA_CLK delay adjustment register	FLA_CLK_DLY	R/W	0000_1000H
01F4H-01F8H	Reserved	–	–	–
01FCH	MEMC_CLK270 switch register	MEMCCLK270_SEL	R/W	0000_0000H
0200H-0204H	Reserved	–	–	–
0208H	barrier gate control register	ASMU_BGCTRL	R/W	0000_0000H
020CH-021CH	Reserved	–	–	–
0220H	Quick recovery backup enable setting register	QR_ENA	R/W	0053_4100H
0224H	Quick recovery clock divider setting register	QR_CLKDIV	R/W	0002_0401H
0228H-0234H	Reserved	–	–	–

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Address	Register Name	Register Symbol	R/W	After Reset
0238H	ADSP/ACPU fake mode register	FAKE_MODE	R/W	0000_0000H
023CH	Power status register	POWERSW_STATUS	R	0000_0003H
0240H	Power supply switch enable setting register	POWERSW_ENA	R/W	0000_0000H
0244H	L1 power switch control	L1_POWERSW	R/W	0000_0000H
0248H	ACPU power switch control register	ACPU_POWERSW	R/W	0000_0000H
024CH	ADSP power switch control register	ADSP_POWERSW	R/W	0000_0000H
0250H	Reserved	–	–	–
0254H	ADSP barrier gate control register	ADSP_BUB	R/W	0000_0003H
0258H	ACPU barrier gate control register	ACPU_BUB	R/W	0000_0000H
025CH	Automatic power switch control enable register	POWERSW_ACTRL_EN	R/W	0000_0000H
0260H	Automatic L1 power switch control trigger register	LOG1SW_ACTRL	R/W	0000_0001H
0264H	Automatic ADSP power switch control trigger register	ADSPSW_ACTRL	R/W	0000_0001H
0268H	L1 barrier gate control register	L1_BUZ	R/W	1001_1111H
026CH	L1 barrier gate control register 2	L1_BUZ2	R/W	0000_0011H
0270H-0284H	Reserved	–	–	–
0288H	ACPU bufferable write control register	ACPUBUFTYPE	R/W	0000 0000H
028CH	ADSP bufferable write control register	ADSPBUFTYPE	R/W	0000 0000H
0290H	HXB bufferable write control register	HXBBUFTYPE	R/W	0000 0000H
0294H-031CH	Reserved	–	–	–
0320H-035CH	Status history register	STATUS_RECORD0 to 15	R	–
0360H	ACPU_INIT register	ACPU_INIT	R/W	0006 0000H
0364H-03BCH	Reserved	–	–	–
03C0H	U70 wait control register	AB1_U70WAITCTRL	R/W	000F_1F0FH
03C4H	U71 wait control register	AB1_U71WAITCTRL	R/W	000F_1F0FH
03C8H	U72 wait control register	AB1_U72WAITCTRL	R/W	000F_1F0FH
03CCH	IIC2 wait control register	AB1_IIC2WAITCTRL	R/W	000F_1F0FH
03D0H	IIC wait control register	AB1_IICWAITCTRL	R/W	000F_1F0FH
03D4H	U70 read mode register	AB1_U70READCTRL	R/W	0000_0000H
03D8H	U71 read mode register	AB1_U71READCTRL	R/W	0000_0000H
03DCH	U72 read mode register	AB1_U72 READCTRL	R/W	0000_0000H
03E0H	IIC2 read mode register	AB1_IIC2READCTRL	R/W	0000_0000H
03E4H	IIC read mode register	AB1_IICREADCTRL	R/W	0000_0000H
03E8H	SDIB wait control register	AB1_SDIBWAITCTRL	R/W	000F_1F0FH
03ECH	SDIB read mode register	AB1_SDIBREADCTRL	R/W	0000_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
03F0H	SDIC wait control register	AB1_SDICWAITCTRL	R/W	000F_1F0FH
03F4H	SDIC read mode register	AB1_SDICREADCTRL	R/W	0000_0000H
03F8H-0490H	Reserved	–	–	–
0494H	FLASHCLK control register	FLASHCLK_CTRL	R/W	0000_0000H
0498H-04FCH	Reserved	–	–	–
0500H	L2 (USB) power switch barrier gate control register	L2_POWERSW_BUZ	R/W	0001_0100H
0504H	Automatic L2 (USB) power switch control enable register	LOG2SW_ACTRLEN	R/W	0000_0000H
0508H	L2 (USB) power switch control register	LOG2SW_ACTRL	R/W	0001_0001H
050CH	L3 (AVC) power switch barrier gate control register	L3_POWERSW_BUZ	R/W	0001_0100H
0510H	Automatic L3 (AVC) power switch control enable register	LOG3SW_ACTRLEN	R/W	0000_0000H
0514H	L3 (AVC) power switch control register	LOG3SW_ACTRL	R/W	0001_0001H
0518H-051CH	Reserved	–	–	–
0520H	PLL status register	PLL_STATUS	R	–
0524H-0810H	Reserved	–	–	–
0814H	MEMCIO (L0)-MEMC (L1) barrier gate control register	IO_L0_LM_BUZ	R/W	0000_0101H
0818H-0838H	Reserved	–	–	–
083CH	Reset request register 3	RESETREQ3	R/W	0000_0000H
0840H	RESETREQ3 set/reset enable register	RESETREQ3ENA	R/W	0000_0000H
0844H	Reserved	–	–	–
0848H	APB (PB0) slave macro clock control register 2	APBCLKCTRL2	R/W	0000_000CH
084CH	Macro clock gate control register 4 clock ON/OFF control register	GCLKCTRL4	R/W	0000_03F0H
0850H	GCLKCTRL4 set/reset enable register	GCLKCTRL4ENA	R/W	0000_0000H
0854H-085CH	Reserved	–	–	–
0860H	Automatic frequency switch control REQMASK register 3	AUTO_FRQ_MASK3	R/W	0000_0007H
0864H	Automatic frequency control FIFO space mode register	DFS_FIFOMODE	R/W	0000_0000H
0868H	Automatic frequency switch control FIFOMODE_REQMASK register	DFS_FIFO_REQMASK	R/W	0000_0003H
086CH	Automatic frequency LCD_FIFO threshold register	LCD_FIFOTHRESHOLD	R/W	0000_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
0870H	Automatic frequency CAM_FIFO threshold register	CAM_FIFOTHRESHOLD	R/W	0000_0000H
0874H	Reserved	–	–	–
0878H	CAM safe reset register	CAM_SAFE_RESET	R/W	0000_0001H
087CH	Reserved	–	–	–
0880H	DTV safe reset register	DTV_SAFE_RESET	R/W	0000_0001H
0884H	USB safe reset register	USB_SAFE_RESET	R/W	0000_0001H
0888H	Reserved	–	–	–
088CH	Clock control register 1	CLKCTRL1	R/W	0000_0003H
0890H	SDIA wait control register	AB1_SDIAWAITCTRL	R/W	000F_1F0FH
0894H	SDIA read mode register	AB1_SDIAREADCTRL	R/W	0000_0000H
0898H-089CH	Reserved	–	–	–
08A0H	ASMU-MEMC handshake function switch register	MEMC_HAND_SHAKE_FAKE	R/W	0000_0000H
08A4H-08B4H	Reserved	–	–	–
08B8H	USB core select register	SEL_BIGWEST	R/W	0000_0000H
08BCH-FFFCH	Reserved	–	–	–

A.1.35 SPI interface (SP0)

Base address: C012_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Mode register	SP0_MODE	R/W	0000_0002H
0004H	SPI polarity register	SP0_POL	R/W	0000_7000H
0008H	Control register	SP0_CONTROL	R/W	0000_8040H
000CH	Reserved	–	–	–
0010H	Transmit data register	SP0_TX_DATA	W	0000_0000H
0014H	Receive data register	SP0_RX_DATA	R	0000_000xH
0018H	Interrupt status register	SP0_STATUS	R	0000_0000H
001CH	Interrupt raw status register	SP0_RAW_STATUS	R	0000_0000H
0020H	Interrupt enable set register	SP0_ENSET	R/W	0000_0000H
0024H	Interrupt enable clear register	SP0_ENCLR	W	0000_0000H
0028H	Interrupt source clear register	SP0_FFCLR	W	0000_0000H
002CH-0030H	Reserved	–	–	–
0034H	Control register 2	SP0_CONTROL2	R/W	0000_0000H
0038H	CS fix register	SP0_TIECS	R/W	0000_0000H
003CH-FFFFH	Reserved	–	–	–

A.1.36 SPI interface (SP1)

Base address: C013_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Mode register	SP1_MODE	R/W	0000_0002H
0004H	SPI polarity register	SP1_POL	R/W	0000_7000H
0008H	Control register	SP1_CONTROL	R/W	0000_8040H
000CH	Reserved	–	–	–
0010H	Transmit data register	SP1_TX_DATA	W	0000_0000H
0014H	Receive data register	SP1_RX_DATA	R	0000_000xH
0018H	Interrupt status register	SP1_STATUS	R	0000_0000H
001CH	Interrupt raw status register	SP1_RAW_STATUS	R	0000_0000H
0020H	Interrupt enable set register	SP1_ENSET	R/W	0000_0000H
0024H	Interrupt enable clear register	SP1_ENCLR	W	0000_0000H
0028H	Interrupt source clear register	SP1_FFCLR	W	0000_0000H
002CH-0030H	Reserved	–	–	–
0034H	Control register 2	SP1_CONTROL2	R/W	0000_0000H
0038H	CS fix register	SP1_TIECS	R/W	0000_0000H
003CH-FFFFH	Reserved	–	–	–

A.1.37 CHGREG (alternate pin function switching)

Base address: C014_0000H

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Address	Register Name	Register Symbol	R/W	After Reset
0000H	Boot mode register	CHG_BOOT_MODE	R	–
0004H	L1 OFF data hold control register	CHG_L1_HOLD	R/W	0000_0000H
0010H	LSI revision register	CHG_LSI_REVISION	R	0000_0010H
0014H-0100H	Reserved	–	–	–
0104H	SDI (A, B, C) interrupt mask register	CHG_CTRL_SDINT	R/W	0000_0007H
0108H	AB0 (ASYNC) boot switch register	CHG_CTRL_AB0_BOOT	R/W	0000_0000H
0110H	OSC control register	CHG_CTRL_OSC	R/W	0000_0000H
0114H-01FCH	Reserved	–	–	–
0200H	GIO_P[15:0] pin alternate function switch register	CHG_PINSEL_G00	R/W	0000_0000H
0204H	GIO_P[31:16] pin alternate function switch register	CHG_PINSEL_G16	R/W	0000_0000H
0208H	GIO_P[47:32] pin alternate function switch register	CHG_PINSEL_G32	R/W	0000_0000H
020CH	GIO_P[63:48] pin alternate function switch register	CHG_PINSEL_G48	R/W	0000_0000H
0210H	GIO_P[79:64] pin alternate function switch register	CHG_PINSEL_G64	R/W	0000_0000H
0214H	GIO_P[95:80] pin alternate function switch register	CHG_PINSEL_G80	R/W	0000_0000H
0218H	GIO_P[111:96] pin alternate function switch register	CHG_PINSEL_G96	R/W	0000_0000H
021CH	GIO_P[117:112] pin alternate function switch register	CHG_PINSEL_G112	R/W	0000_0000H
0220H-027CH	Reserved	–	–	–
0280H	SP0 pin alternate function switch register	CHG_PINSEL_SP0	R/W	0000_0000H
0280H	DTV pin alternate function switch register	CHG_PINSEL_DTV	R/W	0000_0000H
0288H	SD0 pin alternate function switch register	CHG_PINSEL_SD0	R/W	0000_0000H
028CH	SD1 pin alternate function switch register	CHG_PINSEL_SD1	R/W	0000_0000H
0290H	IIC2 pin alternate function switch register	CHG_PINSEL_IIC2	R/W	0000_0000H
0294H	REFCLKO clock pin switch register	CHG_PINSEL_REFCLKO	R/W	0000_0000H
0298H-029CH	Reserved	–	–	–
0300H	GIO_P[7:0] pin PU/PD/IE control register	CHG_PULL_G00	R/W	0000_0000H
0304H	GIO_P[15:8] pin PU/PD/IE control register	CHG_PULL_G08	R/W	0000_0000H
0308H	GIO_P[23:16] pin PU/PD/IE control register	CHG_PULL_G16	R/W	0000_0000H
030CH	GIO_P[31:24] pin PU/PD/IE control register	CHG_PULL_G24	R/W	0000_0000H
0310H	GIO_P[39:32] pin PU/PD/IE control register	CHG_PULL_G32	R/W	0000_0000H
0314H	GIO_P[47:40] pin PU/PD/IE control register	CHG_PULL_G40	R/W	0000_2200H
0318H	GIO_P[55:48] pin PU/PD/IE control register	CHG_PULL_G48	R/W	1111_1111H
031CH	GIO_P[63:56] pin PU/PD/IE control register	CHG_PULL_G56	R/W	1111_1111H
0320H	GIO_P[71:64] pin PU/PD/IE control register	CHG_PULL_G64	R/W	1111_1111H
0324H	GIO_P[79:72] pin PU/PD/IE control register	CHG_PULL_G72	R/W	0000_0000H

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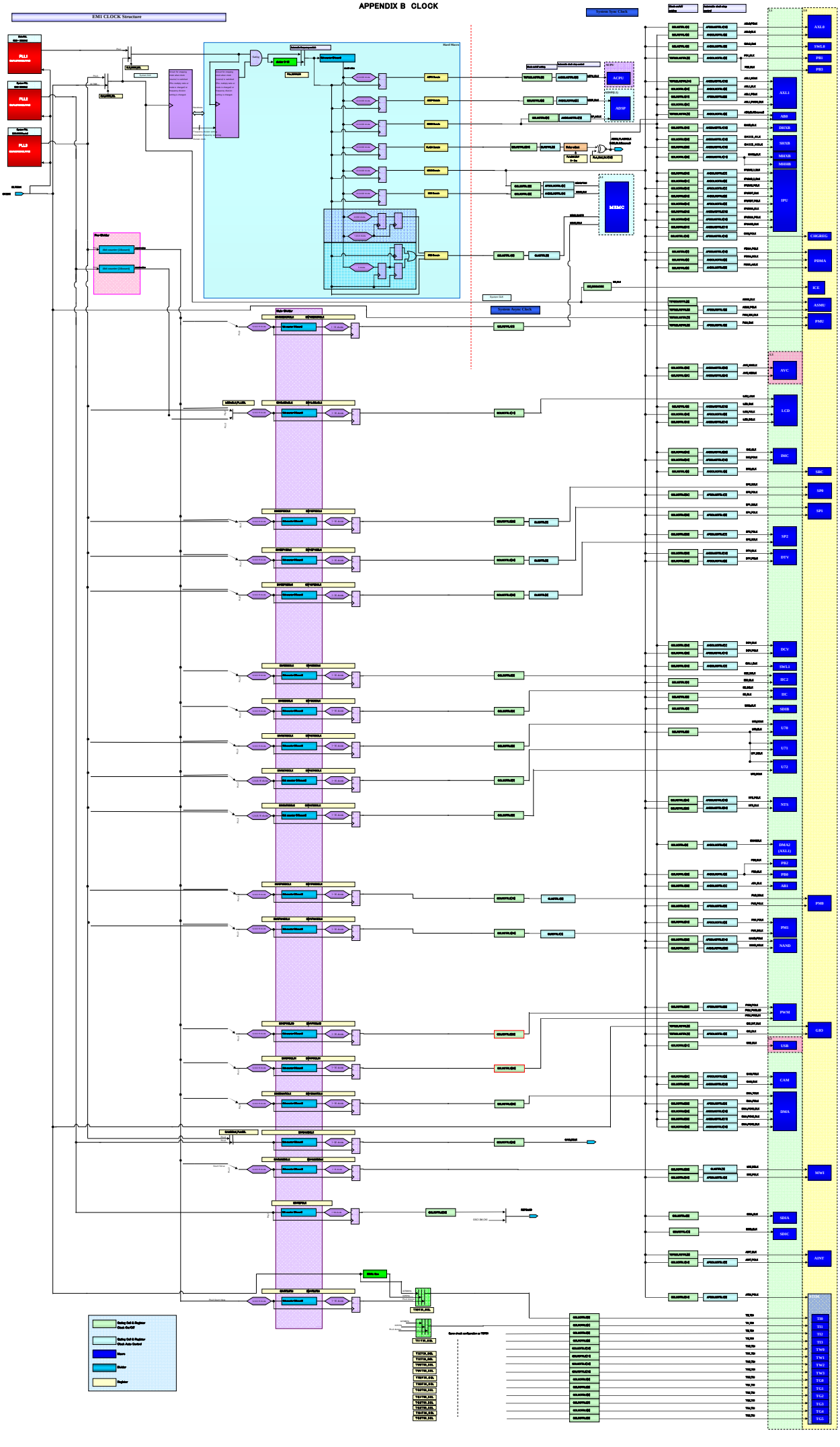
Address	Register Name	Register Symbol	R/W	After Reset
0328H	GIO_P[87:80] pin PU/PD/IE control register	CHG_PULL_G80	R/W	0000_0000H
032CH	GIO_P[95:88] pin PU/PD/IE control register	CHG_PULL_G88	R/W	0000_0000H
0330H	GIO_P[103:96] pin PU/PD/IE control register	CHG_PULL_G96	R/W	0000_0000H
0334H	GIO_P[111:104] pin PU/PD/IE control register	CHG_PULL_G104	R/W	0000_0000H
0338H	GIO_P[119:112] pin PU/PD/IE control register	CHG_PULL_G112	R/W	0000_0000H
033CH	GIO_P[127:120] pin PU/PD/IE control register	CHG_PULL_G120	R/W	0000_0000H
0340H-037CH	Reserved	–	–	–
0380H	PU/PD/IE control register 0	CHG_PULL0	R/W	0000_0004H
0384H	PU/PD/IE control register 1	CHG_PULL1	R/W	0000_0600H
0388H	PU/PD/IE control register 2	CHG_PULL2	R/W	0000_1001H
038CH	PU/PD/IE control register 3	CHG_PULL3	R/W	0000_0000H
0390H-039CH	Reserved	–	–	–
0400H	Drive capability switch register 0	CHG_DRIVE0	R/W	5550_0155H
0404H	Drive capability switch register 1	CHG_DRIVE1	R/W	5555_5555H
0408H	Drive capability switch register 2	CHG_DRIVE2	R/W	0001_1555H

A.1.38 MICROWIRE interface (MWI)

Base address: C016_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	System control register	MWI_CONT	R/W	0000_0000H
0004H	CS0 setting register	MWI_CS0	R/W	0000_0001H
0008H	CS1 setting register	MWI_CS1	R/W	0000_0001H
000CH	Transmission start register	MWI_START	R/W	0000_0000H
0020H	Interrupt status register	MWI_INTSTATUS	R	0000_0000H
0024H	Interrupt raw status register	MWI_INTRAW	R	0000_0000H
0028H	Interrupt clear register	MWI_INTFFCLR	W	0000_0000H
002CH	Interrupt enable set register	MWI_INTENSET	R/W	0000_0000H
0030H	Interrupt enable clear register	MWI_INTENCLR	W	0000_0000H
0040H	Transmit address register	MWI_TXQA	R/W	0000_0000H
0050H	Transmit data register	MWI_TXQ	R/W	0000_0000H
0060H	Receive data register	MWI_RXQ	R	0000_0000H

APPENDIX B CLOCK



APPENDIX C BOOT LOADER IN ROM

C.1 Overview

This chapter explains the boot loader in ROM, which performs the starting processing of EM1-D512.
EM1-D512 has the following ROM boot modes.

- SD boot: Copies Miniboot from SD to SRAM.
- eMMC boot: Copies Miniboot from eMMC to SRAM.

C.1.1 Restrictions

- SD boot: None.
- eMMC boot: If multiple devices are connected, Miniboot is loaded from the eMMC-NAND in which RCA is set to 0x01.

C.1.2 Cautions

<1> Examples in this chapter are given on the assumption that the size of the SRAM is 128 KB.
<2> This boot loader uses only the internal SRAM as RAM. (The setting of SDR is performed in the Miniboot that is loaded by this boot loader to SRAM.)
<3> The boot loader in this document indicates a boot loader that loads the OS kernel.

○ SD boot
<1> Operates at PLL3 frequency (229.376 MHz).
<2> Since UART0 is used, the UART0 alternate-function pins (two pins) must be switched to UART mode.
<3> The UART0 speed is 9,600 baud.
<4> The SD card clock frequency is 1/4 that of the macro clock (LBUS DOMAIN); that is, 14.336 MHz.
<5> The binary file “sdboot.bin” must be written to the root directory of the SD card that has been formatted to FAT16 (more than 32 MB) in a Windows PC. (Cards formatted so that the number of bytes per sector is other than 512 are not supported.)
<6> The maximum size of the sdboot.bin file is 64 KB.
<7> The power supply LSI is manipulated by SP0 (Addr: 06H, Data: 06H).

○ eMMC boot
<1> Operates at PLL3 frequency (229.376 MHz).
<2> Since UART0 is used, the UART0 alternate-function pins (two pins) must be switched to UART mode.
<3> The UART0 speed is 9,600 baud.
<4> The eMMC clock frequency is 1/4 that of the macro clock (LBUS DOMAIN); that is, 14.336 MHz.

<5> The boot loader reads the master boot record (MBR) from the eMMC-NAND in which RCA is set to 0x01, and reads 4,096 bytes from the LBA of the first active partition table.

<6> The power supply LSI is manipulated by SP0 (Addr: 06H, Data: 02H).

<7> The boot loader switches sector access and byte access according to the SEND_OP_COND command response.

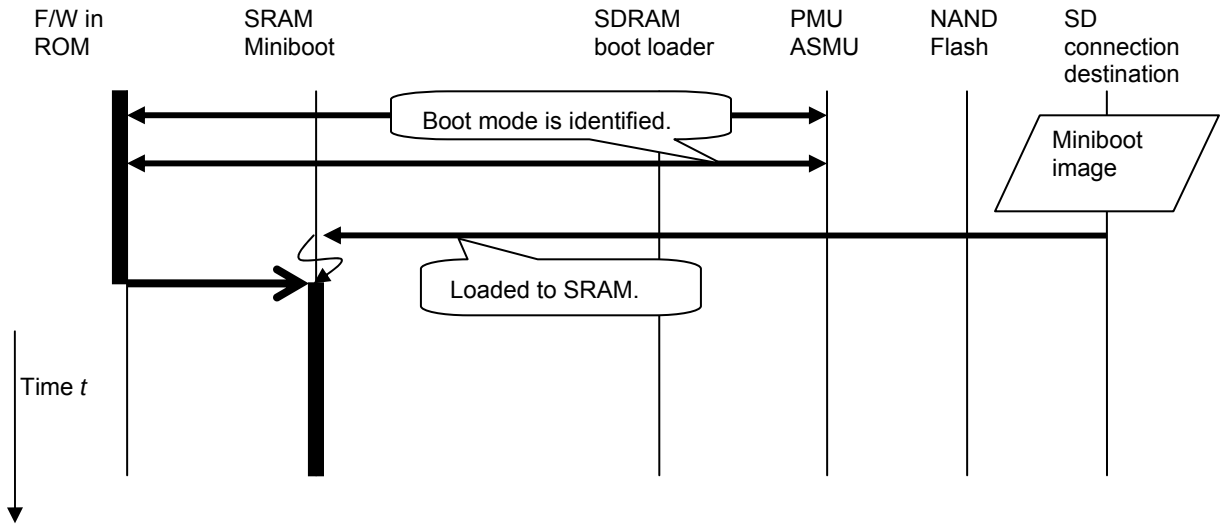
C.2 Operational Overview

The boot loader in ROM requires the boot processing described below.

This document explains the firmware part of this operation in ROM.

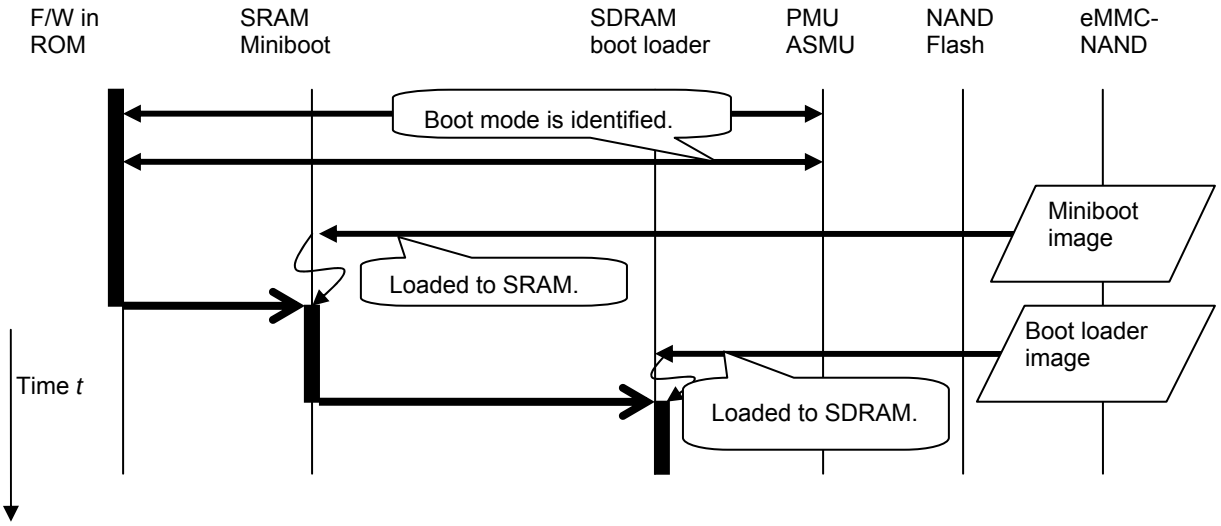
C.2.1 SD boot

If SD boot is identified according to the setting of the CHG_BOOT_MODE register in CHG, the Miniboot image in SD is written to SRAM and execution jumps to the Miniboot



C.2.2 eMMC boot

If eMMC boot is identified according to the setting of the CHG_BOOT_MODE register in CHG, the Miniboot image in eMMC-NAND with RCA = 01 is written to SRAM and execution jumps to the Miniboot.



C.3 Function Overview

C.3.1 Basic functions of boot loader in ROM

<1> The boot loader identifies whether the boot area is SD or eMMC and jumps to the respective boot mode.

<2> If the ROMTEST mode is set, the boot loader jumps to the ROMTEST mode.

C.3.2 SD boot

The boot loader:

<1> Turns on the power to the SD device.

<2> Sets UART.

<3> Initializes the SD0 interface of EM1-D512.

<4> Initializes SD card reading.

<5> Acquires FAT information.

<6> Copies the image written to the SD card (file name: sdboot.bin) to SRAM.

<7> Jumps to Miniboot.

C.3.3 eMMC boot

The boot loader:

<1> Turns on the power to the eMMC-NAND device.

<2> Sets UART.

<3> Initializes the SD2 interface of EM1-D512.

<4> Initializes eMMC-NAND reading.

<5> Acquires information on eMMC-NAND device connected.

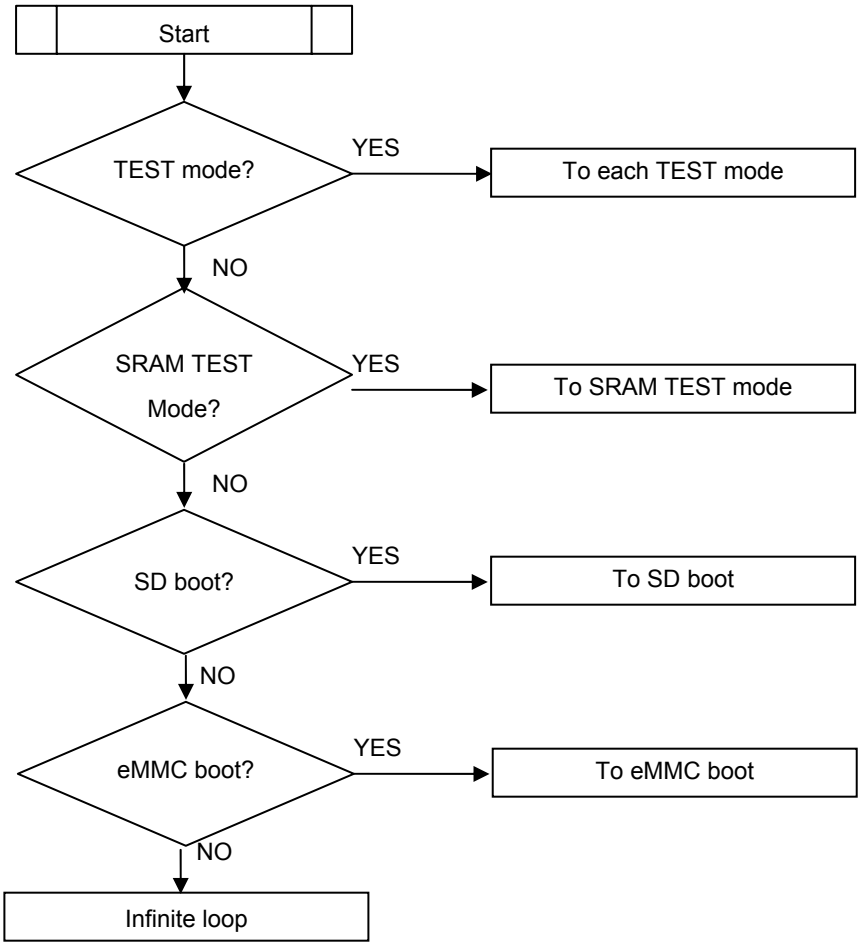
<6> Acquires the master boot record (MBR) from the eMMC-NAND in which RCA is set to 0x01.

<7> Copies 4,096 bytes from the LBA of the first active partition table to SRAM.
(If there is no active partition table, the first partition table is used.)

<8> Jumps to Miniboot.

C.4 Processing Flow

C.4.1 Basic function processing flow of boot loader in ROM



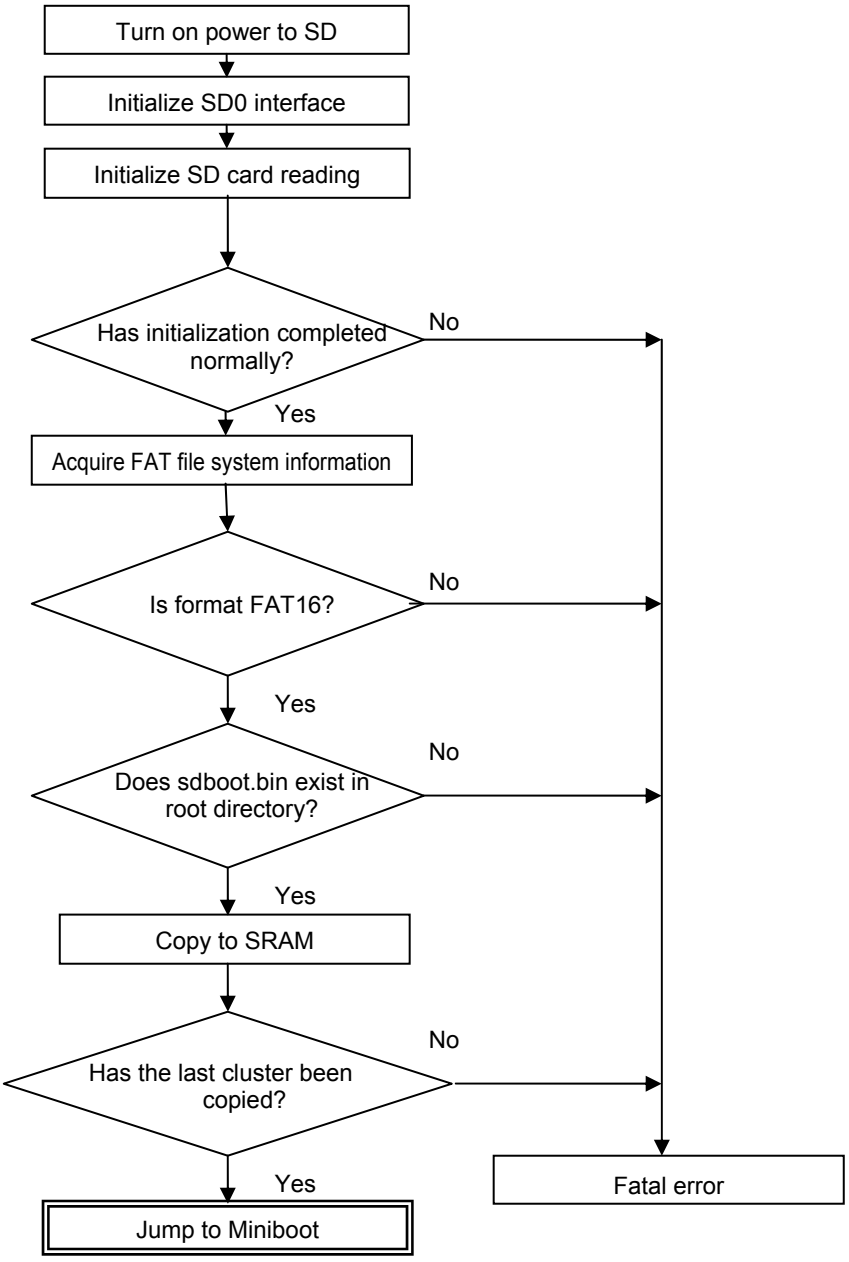
(1) Register values for basic processing of boot loader in ROM

The registers that must be set for basic processing of the boot loader in ROM are listed below.

No.	Register Name	Register Address	Set Value	Remark
1	ASMU_RESETREQ0ENA	0xC011_0008	0xFFFF_DFE7	Reset release (except LCD and ADSP)
	ASMU_RESETREQ0	0xC011_0004	0xFFFF_DFE7	
	ASMU_RESETREQ0ENA	0xC011_0008	0x0000_0000	
2	ASMU_RESETREQ1ENA	0xC011_0010	0xFFFF_FFFF	Reset release of all macros.
	ASMU_RESETREQ1	0xC011_000C	0xFFFF_FFFF	
	ASMU_RESETREQ1ENA	0xC011_0010	0x0000_0000	
3	ASMU_RESETREQ2ENA	0xC011_001C	0xFFFF_FFFF	Reset release of all macros.
	ASMU_RESETREQ2	0xC011_0018	0xFFFF_FFFF	
	ASMU_RESETREQ2ENA	0xC011_001C	0x0000_0000	
4	ASMU_RESETREQ3ENA	0xC011_0840	0xFFFF_FFFF	Reset release of all macros.
	ASMU_RESETREQ3	0xC011_083C	0xFFFF_FFFF	
	ASMU_RESETREQ3ENA	0xC011_0840	0x0000_0000	

C.4.2 SD boot processing flow

(1) SD boot basic processing flow



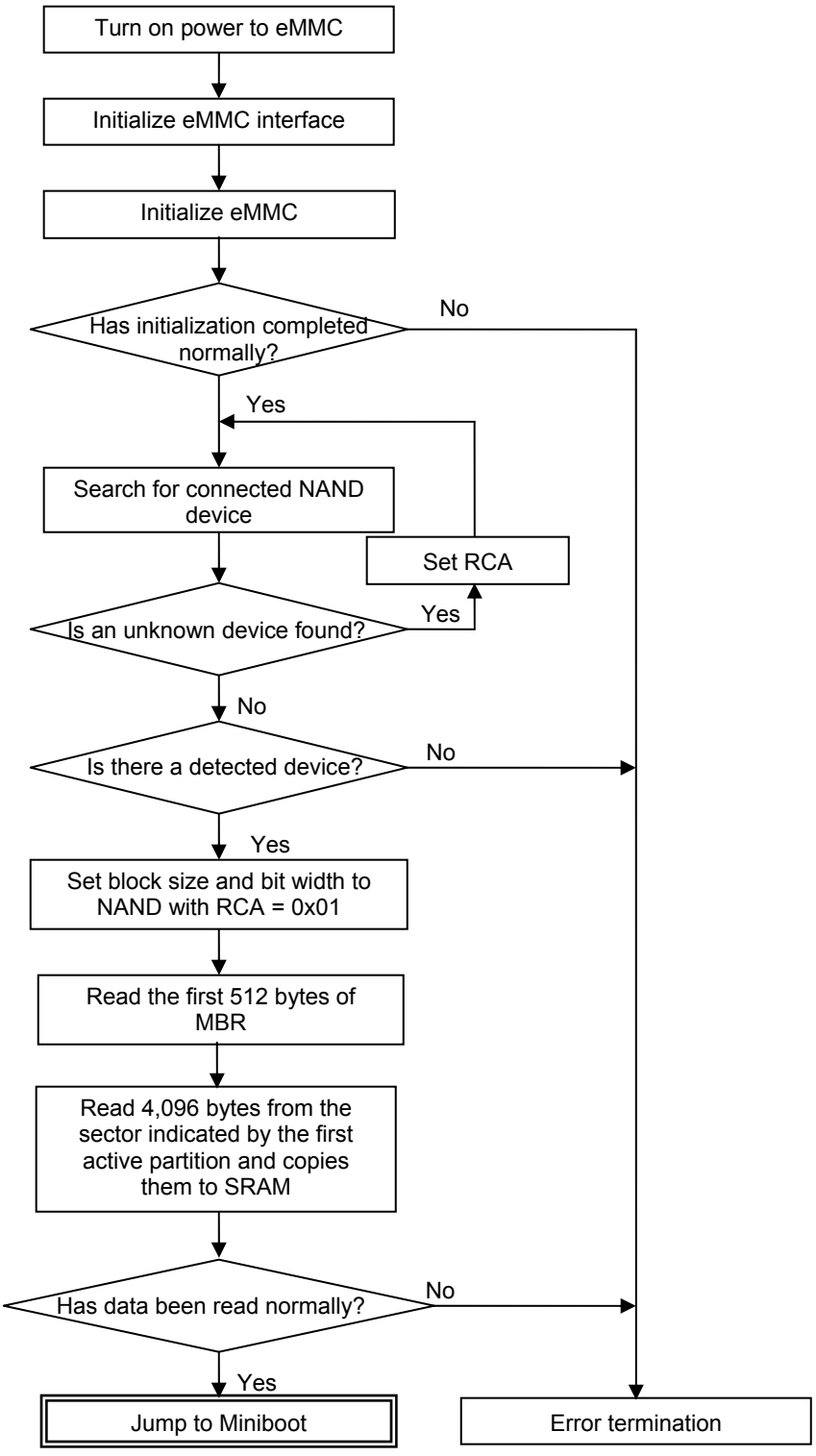
(2) ASMU register setting values for SD boot

The registers that are set when an SD boot is executed are listed below (except SD boot main processing).

No.	Register Name	Register Address	Set Value	Remark
1	ASMU_GCLKCTRL0ENA	0xC011_01B8	0x0000_0003	Stops ADSP_ACLK and ADSP_CLK
	ASMU_GCLKCTRL0	0xC011_01B4	0x0000_0000	
	ASMU_GCLKCTRL0ENA	0xC011_01B8	0x0000_0000	
2	ASMU_GCLKCTRL1ENA	0xC011_01C0	0x0300_0000	Stops DCV_CLK and DCV_PCLK
	ASMU_GCLKCTRL1	0xC011_01BC	0x0000_0000	
	ASMU_GCLKCTRL1ENA	0xC011_01C0	0x0000_0000	
3	ASMU_AHBCLKCTRL0	0xC011_01A0	0xFFDE_FFF2	Macros excluding ACPU = on
4	ASMU_AHBCLKCTRL1	0xC011_01A4	0x0000_FFD1	Macros excluding SRC, PB1, PB0, AB1, SWT = on
5	ASMU_APBCLKCTRL0	0xC011_01A8	0x0001_F1FF	All macros = on
6	ASMU_APBCLKCTRL1	0xC011_01AC	0x0000_8D56	Macros excluding CHG, GIO, SP0, TI, ASMU = on
7	ASMU_CLKCTRL	0xC011_01B0	0x0000_003F	All macros = on
8	ASMU_DIVU70SCLK	0xC011_0158	0x0000_0000	Frequency undivided (based on PLL3)
9	CHG_PINSEL_G80	0xC014_0214	0x0040_0000	Switches the alternate pin function to SD0 mode GIO_P91 → CKI
10	CHG_PULL2	0xC014_0388	0x0000_0611	Changes pull setting for SD CKO: Pull release CMD, DATA0: Pull-up, mask release
11	CHG_PULL_G88	0xC014_032C	0x0000_0444	Changes pull setting for SD DATA1 to DATA3: Pull-down, mask release
12	ASMU_AB1_SDIAWAIT CTRL	0xC011_0890	0x0000_0300	Sets the SD0 wait control register

C.4.3 eMMC boot processing flow

(1) eMMC boot basic processing flow



(2) ASMU register setting values for eMMC boot

The registers that are set when an eMMC boot is executed are listed below (except eMMC boot main processing).

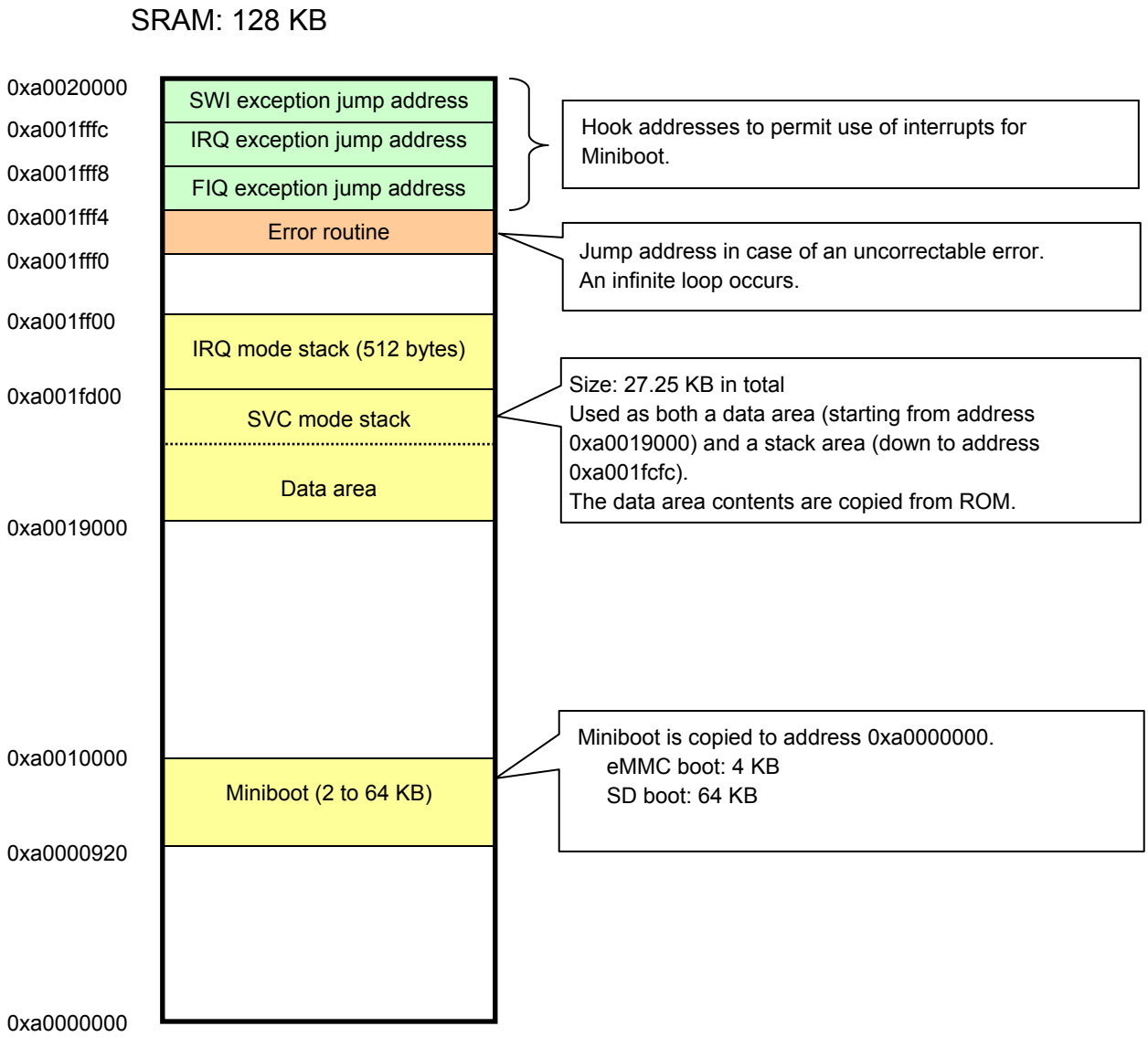
No.	Register Name	Register Address	Set Value	Remark
1	ASMU_GCLKCTRL0ENA	0xC011_01B8	0x0000_0003	Stops ADSP_ACLK and ADSP_CLK
	ASMU_GCLKCTRL0	0xC011_01B4	0x0000_0000	
	ASMU_GCLKCTRL0ENA	0xC011_01B8	0x0000_0000	
2	ASMU_GCLKCTRL1ENA	0xC011_01C0	0x0300_0000	Stops DCV_CLK and DCV_PCLK
	ASMU_GCLKCTRL1	0xC011_01BC	0x0000_0000	
	ASMU_GCLKCTRL1ENA	0xC011_01C0	0x0000_0000	
3	ASMU_AHBCLKCTRL0	0xC011_01A0	0xFFDE_FFE2	Macros excluding ACPU = on
4	ASMU_AHBCLKCTRL1	0xC011_01A4	0x0000_FFD1	Macros excluding SRC, PB1, PB0, AB1, SWT = on
5	ASMU_APBCLKCTRL0	0xC011_01A8	0x0001_F1FF	All macros = on
6	ASMU_APBCLKCTRL1	0xC011_01AC	0x0000_8D56	Macros excluding CHG, GIO, SP0, TI, ASMU = on
7	ASMU_CLKCTRL	0xC011_01B0	0x0000_003F	All macros = on
8	ASMU_DIVU70SCLK	0xC011_0158	0x0000_0000	Frequency undivided (based on PLL3)
9	CHG_PINSEL_G80	0xC014_0214	0x0400_0000	Switches the alternate pin function to SD2 mode GIO_P93 → CKI
10	CHG_PINSEL_G112	0xC014_021C	0x0000_0555	Switches the alternate pin function to SD2 mode GIO_P112 to GIO_P117 → CKO/CMD/DATA0 to DATA3
11	CHG_PULL_G112	0xC014_0338	0x0066_6661	Changes pull setting for SD2 CKO: Pull release CMD, DATA0 to DATA3: Pull-up, mask release
12	ASMU_AB1_SDICWAIT CTRL	0xC011_03F0	0x0000_0300	Sets SD2 wait control register

C.5 Memory Allocation

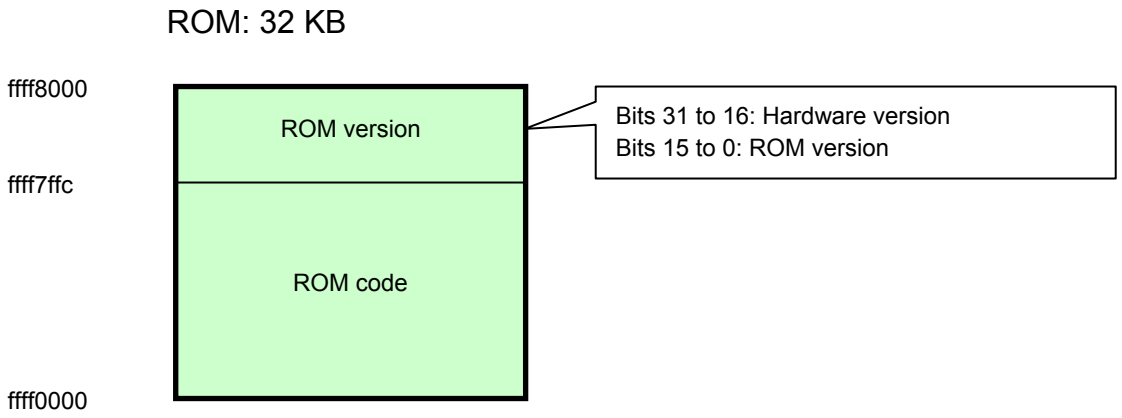
C.5.1 SRAM

The memory allocations of the internal SRAM used by this ROM boot loader are shown below.

During cold boot, these areas are used as the data and stack areas for the ROM boot loader.



C.5.2 ROM


ROM: 32 KB
ffff8000
ffff7ffc
ffff0000
ROM version
ROM code
Bits 31 to 16: Hardware version
Bits 15 to 0: ROM version

APPENDIX D SIGNAL PINS

D.1 Signal Pins

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IO Voltage	Group	Pin Name	Normal IO	Alternate Function (Initial Function)												Switching Unit	Normal Initial Status (After DET1 Release)					Normal/Economy/ Sleep/Deep Sleep		Power OFF State	
				Alternate Function 1 (Default: 00)			Alternate Function 2 (01)			Alternate Function 3 (10)			Alternate Function 4 (11)				IO	Output Value	Pull	AND, Thru, Mask	Initial Value			DET1 = 0 (Only IO Power is On)	
				Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function							Pull	Drive	Pin Status	Internal Status
1.8 V	MODE	BOOTSEL0	IN	BOOTSEL0	IN	Boot mode select 0											IN				2 mA	–	–	Hi-Z	–
1.8 V		BOOTSEL1	IN	BOOTSEL1	IN	Boot mode select 1											IN				2 mA	–	–	Hi-Z	–
1.8 V		BOOTSEL2	IN	BOOTSEL2	IN	Boot mode select 2											IN				2 mA	–	–	Hi-Z	–
1.8 V		BOOTSEL3	IN	BOOTSEL3	IN	Boot mode select 3											IN				2 mA	–	–	Hi-Z	–
3.3 V	SYSTEM	DET1	IN	DET1	IN	Power-on reset											IN				–	–	–	Hi-Z	–
3.3 V		A_RESETB	IN	A_RESETB	IN	System reset											IN				2 mA	–	–	Hi-Z	L
3.3 V		C32K	IN	C32K	IN	32.768 kHz clock											IN				2 mA	–	–	Hi-Z	–

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IO Voltage	Group	Pin Name	Normal IO	Alternate Function (Initial Function)												Switching Unit	Normal Initial Status (After DET1 Release)					Normal/Economy/ Sleep/Deep Sleep		Power OFF State DET1 = 0 (Only IO Power is On)	
				Alternate Function 1 (Default: 00)			Alternate Function 2 (01)			Alternate Function 3 (10)			Alternate Function 4 (11)				IO	Output Value	Pull	AND, Thru, Mask	Initial Value				
				Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function							Pull	Drive	Pin Status	Internal Status
3.3 V	SYSTEM	REFCLKO	OUT	OSC12M_OUT	OUT	Internal OSC output	PLL2OUT	OUT	Internal PLL2 output							Individually	OUT			Mask	4 mA	–	2/4/6/8mA	Hi-Z	L
3.3 V		ERR_RST_ REQB	OUT	ERR_RST_ REQB	OUT	Autonomous reset request											OUT	H		Mask	4 mA	–	2/4/6/8mA	Hi-Z	L
1.8 V		OSC12M_CKI	IN	OSC12M_CKI	IN	OSC XT1											IN		PD		–	–	–	PD	PD
1.8 V		OSC12M_CKO	OUT	OSC12M_CKO	out	OSC XT2											IN		PU		–	–	–	PU	PU
1.8 V	JTAG	DEBUG_EN	IN	DEBUG_EN	IN	ICE											IN		PD	Thru	2 mA	–/PD/PU	–	PD	L
3.3 V		JT0_TCK	IN	JT0_TCK	IN	ICE											IN		PD	Thru	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		JT0_TRSTB	IN	JT0_TRSTB	IN	ICE											IN		PD	Thru	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		JT0_TMS	IN	JT0_TMS	IN	ICE											IN		PU	Thru	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		JT0_TDI	IN	JT0_TDI	IN	ICE											IN		PU	Thru	4 mA		2/4/6/8mA	Hi-Z	L
3.3 V		JT0_TDO	OUT	JT0_TDO	OUT	ICE											OUT	H/L		Mask	4 mA	–	2/4/6/8mA	Hi-Z	L
3.3 V		JT0_RTCK	OUT	JT0_RTCK	OUT	ICE											OUT	H/L		Mask	4 mA	–	2/4/6/8mA	Hi-Z	L
1.8 V	AB	AB0_CLK	OUT	GIO_P11	IO	GPIO	AB0_CLK	OUT	AB	NTS_CLK	IN	NTSC				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		AB0_AD0	IO	GIO_P12	IO	GPIO	AB0_AD0	IO	AB							Individually	IN				4 mA	–	2/4/8/12mA	L	L
1.8 V		AB0_AD1	IO	GIO_P13	IO	GPIO	AB0_AD1	IO	AB							Individually	IN				4 mA	–	2/4/8/12mA	L	L
1.8 V		AB0_AD2	IO	GIO_P14	IO	GPIO	AB0_AD2	IO	AB							Individually	IN				4 mA	–	2/4/8/12mA	L	L
1.8 V		AB0_AD3	IO	GIO_P15	IO	GPIO	AB0_AD3	IO	AB							Individually	IN				4 mA	–	2/4/8/12mA	L	L
1.8 V		AB0_AD4	IO	GIO_P16	IO	GPIO	AB0_AD4	IO	AB							Individually	IN				4 mA	–	2/4/8/12mA	L	L
1.8 V		AB0_AD5	IO	GIO_P17	IO	GPIO	AB0_AD5	IO	AB							Individually	IN				4 mA	–	2/4/8/12mA	L	L
1.8 V		AB0_AD6	IO	GIO_P18	IO	GPIO	AB0_AD6	IO	AB							Individually	IN				4 mA	–	2/4/8/12mA	L	L

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IO Voltage	Group	Pin Name	Normal IO	Alternate Function (Initial Function)												Switching Unit	Normal Initial Status (After DET1 Release)					Normal/Economy/ Sleep/Deep Sleep		Power OFF State	
				Alternate Function 1 (Default: 00)			Alternate Function 2 (01)			Alternate Function 3 (10)			Alternate Function 4 (11)				IO	Output Value	Pull	AND, Thru, Mask	Initial Value			DET1 = 0 (Only IO Power is On)	
				Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function							Pull	Drive	Pin Status	Internal Status
1.8 V		AB0_AD7	IO	GIO_P19	IO	GPIO	AB0_AD7	IO	AB							Individually	IN				4 mA	–	2/4/8/12mA	L	L
1.8 V		AB0_AD8	IO	GIO_P20	IO	GPIO	AB0_AD8	IO	AB							Individually	IN				4 mA	–	2/4/8/12mA	L	L
1.8 V		AB0_AD9	IO	GIO_P21	IO	GPIO	AB0_AD9	IO	AB							Individually	IN				4 mA	–	2/4/8/12mA	L	L
1.8 V		AB0_AD10	IO	GIO_P22	IO	GPIO	AB0_AD10	IO	AB							Individually	IN				4 mA	–	2/4/8/12mA	L	L
1.8 V		AB0_AD11	IO	GIO_P23	IO	GPIO	AB0_AD11	IO	AB							Individually	IN				4 mA	–	2/4/8/12mA	L	L
1.8 V		AB0_AD12	IO	GIO_P24	IO	GPIO	AB0_AD12	IO	AB							Individually	IN				4 mA	–	2/4/8/12mA	L	L
1.8 V		AB0_AD13	IO	GIO_P25	IO	GPIO	AB0_AD13	IO	AB							Individually	IN				4 mA	–	2/4/8/12mA	L	L
1.8 V		AB0_AD14	IO	GIO_P26	IO	GPIO	AB0_AD14	IO	AB							Individually	IN				4 mA	–	2/4/8/12mA	L	L
1.8 V		AB0_AD15	IO	GIO_P27	IO	GPIO	AB0_AD15	IO	AB							Individually	IN				4 mA	–	2/4/8/12mA	L	L
1.8 V		AB0_A17	OUT	GIO_P28	IO	GPIO	AB0_A17/ AB0_A1	OUT	AB	NTS_DATA0	OUT	NTSC				Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_A18	OUT	GIO_P29	IO	GPIO	AB0_A18/ AB0_A2	OUT	AB	NTS_DATA1	OUT	NTSC				Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_A19	OUT	GIO_P30	IO	GPIO	AB0_A19/ AB0_A3	OUT	AB	NTS_DATA2	OUT	NTSC				Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_A20	OUT	GIO_P31	IO	GPIO	AB0_A20/ AB0_A4	OUT	AB							Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_A21	OUT	GIO_P32	IO	GPIO	AB0_A21/ AB0_A5	OUT	AB							Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_A22	OUT	GIO_P33	IO	GPIO	AB0_A22/ AB0_A6	OUT	AB							Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_A23	OUT	GIO_P34	IO	GPIO	AB0_A23/ AB0_A7	OUT	AB							Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L

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IO Volt-age	Group	Pin Name	Nor-mal IO	Alternate Function (Initial Function)												Switching Unit	Normal Initial Status (After DET1 Release)					Normal/Economy/ Sleep/Deep Sleep		Power OFF State DET1 = 0 (Only IO Power is On)	
				Alternate Function 1 (Default: 00)			Alternate Function 2 (01)			Alternate Function 3 (10)			Alternate Function 4 (11)				IO	Output Value	Pull	AND, Thru, Mask	Initial Value				
				Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function							Pull	Drive	Pin Status	Internal Status
1.8 V		AB0_A24	OUT	GIO_P35	IO	GPIO	AB0_A24/ AB0_A8	OUT	AB							Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_A25	OUT	GIO_P36	IO	GPIO	AB0_A25/ AB0_A9	OUT	AB							Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_A26	OUT	GIO_P37	IO	GPIO	AB0_A26/ AB0_A10	OUT	AB							Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_ADV	OUT	GIO_P38	IO	GPIO	AB0_ADV	OUT	AB							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		AB0_RDB	OUT	GIO_P39	IO	GPIO	AB0_RDB	OUT	AB	NTS_DATA3	OUT	NTSC				Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_WRB	OUT	GIO_P40	IO	GPIO	AB0_WRB	OUT	AB	NTS_DATA4	OUT	NTSC				Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_WAIT	IN	GIO_P41	IO	GPIO	AB0_WAIT	IN	AB	NTS_DATA5	OUT	NTSC				Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_CSB0	OUT	GIO_P42	IO	GPIO	AB0_CSB0	OUT	AB	NTS_DATA6	OUT	NTSC				Individually	IN		PU		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_CSB1	OUT	GIO_P43	IO	GPIO	AB0_CSB1	OUT	AB	NTS_DATA7	OUT	NTSC				Individually	IN		PU		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_CSB2	OUT	GIO_P44	IO	GPIO	AB0_CSB2	OUT	AB	NTS_VS	OUT	NTSC				Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_CSB3	OUT	GIO_P45	IO	GPIO	AB0_CSB3	OUT	AB	NTS_HS	OUT	NTSC				Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_BEN0	OUT	GIO_P46	IO	GPIO	AB0_BEN0	OUT	AB							Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L
1.8 V		AB0_BEN1	OUT	GIO_P47	IO	GPIO	AB0_BEN1	OUT	AB							Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	PD	L
3.3 V		PM0_CLK	IO	PM0_CLK	IO	DAC out											IN		PD		4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		PM0_SEN	IO	PM0_SEN	IO	DAC out											IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		PM0_SI	IN	GIO_P87	IO	GPIO	PM0_SI	IN	DAC out							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		PM0_SO	OUT	PM0_SO	OUT	DAC out											OUT	L		Mask	4 mA		2/4/6/8mA	Hi-Z	L
3.3 V		SP0_CLK	IO	SP0_CLK	IO	SPI0	MWI_SK	OUT	MWI							PINSEL_SP0	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L

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IO Voltage	Group	Pin Name	Normal IO	Alternate Function (Initial Function)												Switching Unit	Normal Initial Status (After DET1 Release)					Normal/Economy/ Sleep/Deep Sleep		Power OFF State DET1 = 0 (Only IO Power is On)	
				Alternate Function 1 (Default: 00)			Alternate Function 2 (01)			Alternate Function 3 (10)			Alternate Function 4 (11)				IO	Output Value	Pull	AND, Thru, Mask	Initial Value				
				Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function							Pull	Drive	Pin Status	Internal Status
3.3 V		SP0_SI	IN	SP0_SI	IN	SPI0	MWI_SI	IN	MWI							PINSEL_SP0	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SP0_SO	OUT	SP0_SO	OUT	SPI0	MWI_SO	OUT	MWI							PINSEL_SP0	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SP0_CS0	OUT	SP0_CS0	OUT	SPI0PMU	MWI_CS	OUT	MWI							PINSEL_SP0	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SP0_CS1	OUT	GIO_P48	IO	GPIO	SP0_CS1	OUT	SPI0							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SP0_CS2	OUT	GIO_P49	IO	GPIO	SP0_CS2	OUT	SPI0							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V	DTV	DTV_BCLK	IN	DTV_BCLK	IN	DTV Serial	SP2_CLK	IO	SPI2							PINSEL_DTV	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		DTV_DATA	IN	DTV_DATA	IN	DTV Serial	SP2_SI	IN	SPI2							PINSEL_DTV	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		DTV_PSYNC	IN	DTV_PSYNC	IN	DTV Serial	SP2_SO	OUT	SPI2							PINSEL_DTV	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		DTV_VLD	IN	DTV_VLD	IN	DTV Serial	SP2_CS0	OUT	SPI2							PINSEL_DTV	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
1.8 V	LCD	LCD_PXCLK	OUT	GIO_P50	IO	GPIO	LCD_PXCLK	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_R0	OUT	GIO_P51	IO	GPIO	LCD_R0	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_R1	OUT	GIO_P52	IO	GPIO	LCD_R1	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_R2	OUT	GIO_P53	IO	GPIO	LCD_R2	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_R3	OUT	GIO_P54	IO	GPIO	LCD_R3	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V	LCD	LCD_R4	OUT	GIO_P55	IO	GPIO	LCD_R4	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_R5	OUT	GIO_P56	IO	GPIO	LCD_R5	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L

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IO Voltage	Group	Pin Name	Normal IO	Alternate Function (Initial Function)												Switching Unit	Normal Initial Status (After DET1 Release)					Normal/Economy/ Sleep/Deep Sleep		Power OFF State DET1 = 0 (Only IO Power is On)	
				Alternate Function 1 (Default: 00)			Alternate Function 2 (01)			Alternate Function 3 (10)			Alternate Function 4 (11)				IO	Output Value	Pull	AND, Thru, Mask	Initial Value				
				Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function							Pull	Drive	Pin Status	Internal Status
1.8 V		LCD_G0	OUT	GIO_P57	IO	GPIO	LCD_G0	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_G1	OUT	GIO_P58	IO	GPIO	LCD_G1	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_G2	OUT	GIO_P59	IO	GPIO	LCD_G2	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_G3	OUT	GIO_P60	IO	GPIO	LCD_G3	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_G4	OUT	GIO_P61	IO	GPIO	LCD_G4	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_G5	OUT	GIO_P62	IO	GPIO	LCD_G5	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_B0	OUT	GIO_P63	IO	GPIO	LCD_B0	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_B1	OUT	GIO_P64	IO	GPIO	LCD_B1	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_B2	OUT	GIO_P65	IO	GPIO	LCD_B2	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_B3	OUT	GIO_P66	IO	GPIO	LCD_B3	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_B4	OUT	GIO_P67	IO	GPIO	LCD_B4	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_B5	OUT	GIO_P68	IO	GPIO	LCD_B5	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_HSYNC	OUT	GIO_P69	IO	GPIO	LCD_HSYNC	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_VSYNC	OUT	GIO_P70	IO	GPIO	LCD_VSYNC	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		LCD_ENABLE	OUT	GIO_P71	IO	GPIO	LCD_ENABLE	OUT	LCD							Individually	IN			Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		USB_CLK	IN	GIO_P96	IO	GPIO	USB_CLK	IN	ULPI							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		USB_DATA0	IO	GIO_P97	IO	GPIO	USB_DATA0	IO	ULPI							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		USB_DATA1	IO	GIO_P98	IO	GPIO	USB_DATA1	IO	ULPI							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		USB_DATA2	IO	GIO_P99	IO	GPIO	USB_DATA2	IO	ULPI							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		USB_DATA3	IO	GIO_P100	IO	GPIO	USB_DATA3	IO	ULPI							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		USB_DATA4	IO	GIO_P101	IO	GPIO	USB_DATA4	IO	ULPI							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		USB_DATA5	IO	GIO_P102	IO	GPIO	USB_DATA5	IO	ULPI							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		USB_DATA6	IO	GIO_P103	IO	GPIO	USB_DATA6	IO	ULPI							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L

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IO Voltage	Group	Pin Name	Normal IO	Alternate Function (Initial Function)												Switching Unit	Normal Initial Status (After DET1 Release)					Normal/Economy/ Sleep/Deep Sleep		Power OFF State DET1 = 0 (Only IO Power is On)	
				Alternate Function 1 (Default: 00)			Alternate Function 2 (01)			Alternate Function 3 (10)			Alternate Function 4 (11)				IO	Output Value	Pull	AND, Thru, Mask	Initial Value	Pull	Drive	Pin Status	Internal Status
				Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function										
1.8 V		USB_DATA7	IO	GIO_P104	IO	GPIO	USB_DATA7	IO	ULPI							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V	NTSC	USB_DIR	IN	GIO_P105	IO	GPIO	USB_DIR	IN	ULPI							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		USB_STP	OUT	GIO_P106	IO	GPIO	USB_STP	OUT	ULPI							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
1.8 V		USB_NXT	IO	GIO_P107	IO	GPIO	USB_NXT	IO	ULPI							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/8/12mA	PD	L
3.3 V		NTS_CLK	IN	GIO_P72	IO	GPIO	NTS_CLK	IN	NTSC				PM1_CLK	IO	PCM1	Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		NTS_VS	OUT	GIO_P73	IO	GPIO	NTS_VS	OUT	NTSC	SP1_CLK	IO	SPI1				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		NTS_HS	OUT	GIO_P74	IO	GPIO	NTS_HS	OUT	NTSC	SP1_SI	IN	SPI1				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V	NTSC	NTS_DATA0	OUT	GIO_P75	IO	GPIO	NTS_DATA0	OUT	NTSC	SP1_SO	OUT	SPI1	CAM_YUV0	IN	CAM	Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		NTS_DATA1	OUT	GIO_P76	IO	GPIO	NTS_DATA1	OUT	NTSC	SP1_CS0	IO	SPI1	CAM_YUV1	IN	CAM	Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		NTS_DATA2	OUT	GIO_P77	IO	GPIO	NTS_DATA2	OUT	NTSC	SP1_CS1	OUT	SPI1	CAM_YUV2	IN	CAM	Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		NTS_DATA3	OUT	GIO_P78	IO	GPIO	NTS_DATA3	OUT	NTSC	SP1_CS2	OUT	SPI1	CAM_YUV3	IN	CAM	Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		NTS_DATA4	OUT	GIO_P79	IO	GPIO	NTS_DATA4	OUT	NTSC	SP1_CS3	OUT	SPI1	CAM_YUV4	IN	CAM	Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		NTS_DATA5	OUT	GIO_P80	IO	GPIO	NTS_DATA5	OUT	NTSC	SP1_CS4	OUT	SPI1	PM1_SEN	IO	PCM1	Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		NTS_DATA6	OUT	GIO_P81	IO	GPIO	NTS_DATA6	OUT	NTSC	SP1_CS5	OUT	SPI1	PM1_SI	IN	PCM1	Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		NTS_DATA7	OUT	GIO_P82	IO	GPIO	NTS_DATA7	OUT	NTSC				PM1_SO	OUT	PCM1	Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		IIC_SCL	IO	GIO_P83	IO	IIC	IIC_SCL	IO	IIC							Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		IIC_SDA	IO	GIO_P84	IO	IIC	IIC_SDA	IO	IIC							Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		URT0_SRIN	IN	URT0_SRIN	IN	UART0											IN		PD	Mask	2 mA	–/PD/PU	–	Hi-Z	L
3.3 V		URT0_SOUT	OUT	URT0_SOUT	OUT	UART0											OUT	H		Mask	4 mA	–	2/4/6/8mA	Hi-Z	L
3.3 V		URT0_CTSB	IN	GIO_P85	IO	UART0	URT0_CTSB	IN	UART0	URT1_SRIN	IN	UART1				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		URT0_RTSB	OUT	GIO_P86	IO	UART0	URT0_RTSB	OUT	UART0	URT1_SOUT	OUT	UART1				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SD0_CKO	OUT	SD0_CKO	OUT	SD Card											OUT	L		Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SD0_CMD	IO	SD0_CMD	IO	SD Card											IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L

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IO Voltage	Group	Pin Name	Normal IO	Alternate Function (Initial Function)												Switching Unit	Normal Initial Status (After DET1 Release)					Normal/Economy/ Sleep/Deep Sleep		Power OFF State DET1 = 0 (Only IO Power is On)	
				Alternate Function 1 (Default: 00)			Alternate Function 2 (01)			Alternate Function 3 (10)			Alternate Function 4 (11)				IO	Output Value	Pull	AND, Thru, Mask	Initial Value	Pull	Drive	Pin Status	Internal Status
				Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function										
3.3 V		SD0_DATA0	IO	SD0_DATA0	IO	SD Card											IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V	SD0	SD0_DATA1	IO	GIO_P88	IO	SD Card	SD0_DATA1	IO	SD Card							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V	SD1	SD0_DATA2	IO	GIO_P101	IO	SD Card	SD0_DATA2	IO	SD Card							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SD0_DATA3	IO	GIO_P90	IO	SD Card	SD0_DATA3	IO	SD Card							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SD0_CKI	IN	GIO_P91	IO	GPIO	SD0_CKI	IN	SD Card							Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SD1_CKO	OUT	SD1_CKO	OUT	SD1											OUT	L		Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SD1_CMD	IO	SD1_CMD	IO	SD1				CAM_YUV5	IN	CAM				PINSEL_SD1	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SD1_DATA0	IO	SD1_DATA0	IO	SD1				CAM_YUV6	IN	CAM				PINSEL_SD1	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V	SD1	SD1_DATA1	IO	SD1_DATA1	IO	SD1				CAM_YUV7	IN	CAM				PINSEL_SD1	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SD1_DATA2	IO	SD1_DATA2	IO	SD1				CAM_VS	IN	CAM				PINSEL_SD1	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SD1_DATA3	IO	SD1_DATA3	IO	SD1				CAM_HS	IN	CAM				PINSEL_SD1	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SD1_CKI	IO	GIO_P92	IO	GPIO	SD1_CKI	IN	SD1	CAM_CLKI	IN	CAM				Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V	UART2	URT2_SRIN	IN	GIO_P108	IO	GPIO	URT2_SRIN	IN	UART2	NAND_ALE	OUT	NAND				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		URT2_SOUT	OUT	GIO_P109	IO	GPIO	URT2_SOUT	OUT	UART2	NAND_CLE	OUT	NAND				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		URT2_CTSB	IN	GIO_P110	IO	GPIO	URT2_CTSB	IN	UART2	NAND_D0	IO	NAND				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		URT2_RTSB	OUT	GIO_P111	IO	GPIO	URT2_RTSB	OUT	UART2	NAND_D1	IO	NAND				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V	SD2	SD2_CKO	OUT	GIO_P112	IO	GPIO	SD2_CKO	OUT	eMMC	NAND_D2	IO	NAND				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SD2_CMD	OUT	GIO_P113	IO	GPIO	SD2_CMD	OUT	eMMC	NAND_D3	IO	NAND				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L

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IO Voltage	Group	Pin Name	Normal IO	Alternate Function (Initial Function)												Switching Unit	Normal Initial Status (After DET1 Release)					Normal/Economy/ Sleep/Deep Sleep		Power OFF State DET1 = 0 (Only IO Power is On)	
				Alternate Function 1 (Default: 00)			Alternate Function 2 (01)			Alternate Function 3 (10)			Alternate Function 4 (11)				IO	Output Value	Pull	AND, Thru, Mask	Initial Value				
				Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function							Pull	Drive	Pin Status	Internal Status
3.3 V		SD2_DATA0	IO	GIO_P114	IO	GPIO	SD2_DATA0	IO	eMMC	NAND_D4	IO	NAND				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SD2_DATA1	IO	GIO_P115	IO	GPIO	SD2_DATA1	IO	eMMC	NAND_D5	IO	NAND				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SD2_DATA2	IO	GIO_P116	IO	GPIO	SD2_DATA2	IO	eMMC	NAND_D6	IO	NAND				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SD2_DATA3	IO	GIO_P117	IO	GPIO	SD2_DATA3	IO	eMMC	NAND_D7	IO	NAND				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		SD2_CKI	IN	GIO_P93	IO	GPIO	SD2_CKI	IN	eMMC	NAND_OE	OUT	NAND				Individually	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V	IIC2 PWM	IIC2_SCL	IO	IIC2_SCL	IO	IIC2				NAND_WE	OUT	NAND				PINSEL_IIC2	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		IIC2_SDA	IO	IIC2_SDA	IO	IIC2				NAND_RB0	IN	NAND				PINSEL_IIC2	IN		PD		4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		PWM0	OUT	GIO_P94	IO	GPIO	PWM0	OUT	BL							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		PWM1	OUT	GIO_P95	IO	GPIO	PWM1	OUT	LED							Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V	GIO	GIO_P0	IO	GIO_P0	IO	GPIO										Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		GIO_P1	IO	GIO_P1	IO	GPIO	USB_WAKEUP	OUT	USB	USB_PWR_FAULT	IN	USB				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		GIO_P2	IO	GIO_P2	IO	GPIO										Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V	GIO	GIO_P3	IO	GIO_P3	IO	GPIO										Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		GIO_P4	IO	GIO_P4	IO	GPIO				NAND_RB1	IN	NAND				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		GIO_P5	IO	GIO_P5	IO	GPIO				NAND_RB2	IN	NAND	CAM_SCLK	OUT	CAM	Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		GIO_P6	IO	GIO_P6	IO	GPIO				NAND_RB3	IN	NAND				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		GIO_P7	IO	GIO_P7	IO	GPIO				NAND_CE0	OUT	NAND				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		GIO_P8	IO	GIO_P8	IO	GPIO				NAND_CE1	OUT	NAND				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		GIO_P9	IO	GIO_P9	IO	GPIO				NAND_CE2	OUT	NAND				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L
3.3 V		GIO_P10	IO	GIO_P10	IO	GPIO				NAND_CE3	OUT	NAND				Individually	IN		PD	Mask	4 mA	–/PD/PU	2/4/6/8mA	Hi-Z	L

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IIO Voltage	Group	Pin Name	Normal IO	Alternate Function (Initial Function)												Switching Unit	Normal Initial Status (After DET1 Release)					Normal/Economy/ Sleep/Deep Sleep		Power OFF State DET1 = 0 (Only IO Power is On)	
				Alternate Function 1 (Default: 00)			Alternate Function 2 (01)			Alternate Function 3 (10)			Alternate Function 4 (11)				IO	Output Value	Pull	AND, Thru, Mask	Initial Value				
				Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function	Signal Name	IO	Function							Pull	Drive	Pin Status	Internal Status
1.8 V	TEST	UTEST	IN	UTEST	IN	Test (fixed to normal 0)											IN		PD	Thru	2 mA	PD	–	Hi-Z	–
1.8 V		TESTRSTB	IN	TESTRSTB	IN	Test (async reset for testing)											IN		PU		2 mA	PU	–	PU	L
1.8 V		TRSTB	IN	TRSTB	IN	Test (TESTACT)											IN		PD		2 mA	PD	–	PD	L
1.8 V		TE1	IN	TE1	IN	Test (CTR3 = H: PU/PD OFF)											IN		PD		–	PD	–	PD	–
1.8 V		TE2	IN	TE2	IN	Test (CTR6 = H: IOLH 2 mA)											IN		PD		–	PD	–	PD	–

APPENDIX E EXTERNAL BUS INTERFACE

E.1 Registers

Tables E-1, E-2 and E-3 list the external bus interface (AB0) registers.

The base address of each register is 2FFF_0000H.

Table E-1 shows the registers for system control.

Table E-1. System Control Registers

Address	Register Name	Register Symbol	R/W	Bit	After Reset
0000H	Flash command start register	AB0_FLASHCOMSET	W	7	0000_0000H
0004H	Flash read data latch register	AB0_FLASHCOMLATCH	R	16	0000_0000H
0010H	Flash command (ADD0) setting register	AB0_FLASHCOMADD0	R/W	29	0000_0000H
0014H	Flash command (DATA0) setting register	AB0_FLASHCOMDATA0	R/W	16	0000_0000H
0018H	Flash command (ADD1) setting register	AB0_FLASHCOMADD1	R/W	31	0000_0000H
001CH	Flash command (DATA1) setting register	AB0_FLASHCOMDATA1	R/W	16	0000_0000H
0080H	Flash clock control register	AB0_FLASHCLKCTRL	R/W	1	0000_0001H
0084H	Flash read clock delay adjustment register	AB0_FLA_RCLK_DLY	RW	16	0000_1000H
0090H	WAIT pin status register	AB0_WAIT_STATUS	R	1	–
0100H	CS0 base address register	AB0_CS0BASEADD	R/W	14	0000_0000H
0104H	CS0 bit compare register	AB0_CS0BITCOMP	R/W	16	F000_0000H
0110H	CS1 base address register	AB0_CS1BASEADD	R/W	14	3FFF_0000H
0114H	CS1 bit compare register	AB0_CS1BITCOMP	R/W	16	FFFF_0000H
0120H	CS2 base address register	AB0_CS2BASEADD	R/W	14	3FFF_0000H
0124H	CS2 bit compare register	AB0_CS2BITCOMP	R/W	16	FFFF_0000H
0130H	CS3 base address register	AB0_CS3BASEADD	R/W	14	3FFF_0000H
0134H	CS3 bit compare register	AB0_CS3BITCOMP	R/W	16	FFFF_0000H

Caution If an internal register area of AB0 outside the defined range is accessed, writing is ignored. If this area is read, 0 is returned.

E.1.1 Parameter registers

Caution The parameter registers in Table E-2 are of dual structure and cannot be written directly. By starting each slave by using the flash command start register, the value of the parameter register is reflected in the respective internal parameter hold register.

Table E-2. Parameter Registers

Address	Register Name	Register Symbol	R/W	Bit	After Reset
0200H	CS0 wait control register	AB0_CS0WAITCTRL	R/W	16	000F_1F0FH
0204H	CS0 write wait control register	AB0_CS0WAITCTRL_W	R/W	13	000F_1F0FH
0208H	CS0 read mode register	AB0_CS0READCTRL	R/W	4	0000_0000H
020CH	CS0 wait mask register	AB0_CS0WAIT_MASK	R/W	1	0000_0000H
0210H	CS0 control register	AB0_CS0CONTROL	R/W	9	0001_0100H
0214H	CS0 read configuration register	AB0_CS0FLASHRCR	R/W	10	0000_D503H
0218H	Reserved	–	–	–	–
0220H	CS1 wait control register	AB0_CS1WAITCTRL	R/W	16	000F_1F0FH
0224H	CS1 write wait control register	AB0_CS1WAITCTRL_W	R/W	13	000F_1F0FH
0228H	CS1 read mode register	AB0_CS1READCTRL	R/W	4	0000_0000H
022CH	CS1 wait mask register	AB0_CS1WAIT_MASK	R/W	1	0000_0000H
0230H	CS1 control register	AB0_CS1CONTROL	R/W	9	0001_0100H
0234H	CS1 read configuration register	AB0_CS1FLASHRCR	R/W	10	0000_D503H
0238H	Reserved	–	–	–	–
0240H	CS2 wait control register	AB0_CS2WAITCTRL	R/W	16	000F_1F0FH
0244H	CS2 write wait control register	AB0_CS2WAITCTRL_W	R/W	9	000F_1F0FH
0248H	CS2 read mode register	AB0_CS2READCTRL	R/W	4	0000_0000H
024CH	CS2 wait mask register	AB0_CS2WAIT_MASK	R/W	1	0000_0000H
0250H	CS2 control register	AB0_CS2CONTROL	R/W	9	0001_0100H
0254H	CS2 read configuration register	AB0_CS2FLASHRCR	R/W	10	0000_D503H
0258H	Reserved	–	–	–	–
0260H	CS3 wait control register	AB0_CS3WAITCTRL	R/W	16	000F_1F0FH
0264H	CS3 write wait control register	AB0_CS3WAITCTRL_W	R/W	9	000F_1F0FH
0268H	CS3 read mode register	AB0_CS3READCTRL	R/W	4	0000_0000H
026CH	CS3 wait mask register	AB0_CS3WAIT_MASK	R/W	1	0000_0000H
0270H	CS3 control register	AB0_CS3CONTROL	R/W	9	0001_0100H
0274H	CS3 read configuration register	AB0_CS3FLASHRCR	R/W	10	0000_D503H
0278H	Reserved	–	–	–	–

Caution If an internal register area of AB0 outside the defined range is accessed, writing is ignored. If this area is read, 0 is returned.

E.1.2 Parameter retention registers

Caution The parameter hold registers in Table E-3 are of dual structure and cannot be written directly. By starting each slave by using the flash command start register, the value of the parameter register is reflected in the respective internal parameter hold register

Table E-3. Parameter Retention Registers

Address	Register Name	Register Symbol	R/W	Bit	After Reset
0300H	CS0 wait control register	AB0_CS0WAITCTRL2	R	16	000F_1F0FH
0304H	CS0 write wait control register	AB0_CS0WAITCTRL_W2	R	13	000F_1F0FH
0308H	CS0 read mode register	AB0_CS0READCTRL2	R	4	0000_0000H
030CH	CS0 wait mask register	AB0_CS0WAIT_MASK2	R	1	0000_0000H
0310H	CS0 control register	AB0_CS0CONTROL2	R	9	0001_0100H
0314H	CS0 read configuration register	AB0_CS0FLASHRCR2	R	10	0000_D503H
0318H	Reserved	–	–	–	–
0320H	CS1 wait control register	AB0_CS1WAITCTRL2	R	16	000F_1F0FH
0324H	CS1 write wait control register	AB0_CS1WAITCTRL_W2	R	9	000F_1F0FH
0328H	CS1 read mode register	AB0_CS1READCTRL2	R	4	0000_0000H
032CH	CS1 wait mask register	AB0_CS1WAIT_MASK2	R	1	0000_0000H
0330H	CS1 control register	AB0_CS1CONTROL2	R	9	0001_0100H
0334H	CS1 read configuration register	AB0_CS1FLASHRCR2	R	10	0000_D503H
0338H	Reserved	–	–	–	–
0340H	CS2 wait control register	AB0_CS2WAITCTRL2	R	16	000F_1F0FH
0344H	CS2 write wait control register	AB0_CS2WAITCTRL_W2	R	9	000F_1F0FH
0348H	CS2 read mode register	AB0_CS2READCTRL2	R	4	0000_0000H
034CH	CS2 wait mask register	AB0_CS2WAIT_MASK2	R	1	0000_0000H
0350H	CS2 control register	AB0_CS2CONTROL2	R	9	0001_0100H
0354H	CS2 read configuration register	AB0_CS2FLASHRCR2	R	10	0000_D503H
0358H	Reserved	–	–	–	–
0360H	CS3 wait control register	AB0_CS3WAITCTRL2	R	16	000F_1F0FH
0364H	CS3 write wait control register	AB0_CS3WAITCTRL_W2	R	9	000F_1F0FH
0368H	CS3 read mode register	AB0_CS3READCTRL2	R	4	0000_0000H
036CH	CS3 wait mask register	AB0_CS3WAIT_MASK2	R	1	0000_0000H
0370H	CS3 control register	AB0_CS3CONTROL2	R	9	0001_0100H
0374H	CS3 read configuration register	AB0_CS3FLASHRCR2	R	10	0000_D503H
0378H	Reserved	–	–	–	–

Caution If an internal register area of AB0 outside the defined range is accessed, writing is ignored. If this area is read, 0 is returned.

E.2 Register Details

(1) Flash command start register

When CS (0 to 3) of this register (AB0_FLASHCOMSET: 2FFF_0000H) is set, the value of the parameter register specified for the ***slave*** is copied to the respective parameter hold register of AB0.

After that, a command is issued to an external device (***slave***) selected, depending on the status of the SET_MODE bit.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	SET_MODE	Reserved	Reserved	CS3	CS2	CS1	CS0

Name	R/W	Bit	After Reset	Function
Reserved	R	31:7	–	Reserved. When these bits are read, 0 is returned for each bit.
SET_MODE	W	6	0	Sets whether to issue a command to flash memory. 0: Does not issue 1: Issues
Reserved	R	5	–	Reserved. When this bit is read, 0 is returned.
Reserved	R	4	–	Reserved. When this bit is read, 0 is returned.
CS3	W	3	0	Starts CS3 (parameter copy). 0: – 1: Starts
CS2	W	2	0	Starts CS2 (parameter copy). 0: – 1: Starts
CS1	W	1	0	Starts CS1 (parameter copy). 0: – 1: Starts
CS0	W	0	0	Starts CS0 (parameter copy). 0: – 1: Starts

Caution A command can be issued to only one CS. If two or more CSs are selected, the CS with the smallest number has the highest priority.

If no CS is specified, the flash command is issued (by setting SET_MODE bit) to CS0.

Example 1) CS0 bit = 1, CS1 bit = 1, SET_MODE bit = 1

→ The parameter register is copied to the parameter hold register for CS0 and CS1.
The Flash command is issued to CS0.

Example 2) CS0 bit = 1, CS1 bit = 1, SET_MODE bit = 0

→ The parameter register is copied to the parameter hold register for CS0 and CS1.
The Flash command is not issued to CS0 and CS1.

(2) Flash read data latch register

Data read by the device command of Intel StrataFlash Wireless Memory is latched to this register (AB0_FLASHCOMLATCH: 2FFF_0004H). Since the read command is issued only in the “Second Bus Cycle”, a command that reads data in the “Second Bus Cycle” is always latched.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
READ_COM							
7	6	5	4	3	2	1	0
READ_COM							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	–	Reserved. When these bits are read, 0 is returned for each bit.
READ_COM	R	15:0	0	Latches the data read by flash memory command.

(3) Flash command (ADD0) setting register

This register (AB0_FLASHCOMADD0: 2FFF_0010H) sets the command to the Intel flash memory. This register sets the write address of the first command cycle.

31	30	29	28	27	26	25	24
Reserved			ADD0				
23	22	21	20	19	18	17	16
ADD0							
15	14	13	12	11	10	9	8
ADD0							
7	6	5	4	3	2	1	0
ADD0							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:29	–	Reserved. When these bits are read, 0 is returned for each bit.
ADD0	R/W	28:0	0	Sets the address of the first bus cycle.

(4) Flash command (DATA0) setting register

This register (AB0_FLASHCOMDATA0: 2FFF_0014H) sets the command to the Intel flash memory. This register sets the data of the first command cycle.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
DATA0							

7	6	5	4	3	2	1	0
DATA0							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	–	Reserved. When these bits are read, 0 is returned for each bit.
DATA0	R/W	15:0	0000H	Sets the data of the first bus cycle.

(5) Flash command (ADD1) setting register

This register (AB0_FLASHCOMADD1: 2FFF_0018H) sets the command to the Intel flash memory. This register sets an address in the second command cycle and reading or writing.

This register is used when the command to the flash memory is a two-cycle command and, when it is used, set the ValidBit bit to 1.

If a read operation is performed at this command address (second command cycle), the read data is latched to the AB0_FLASHCOMLATCH register.

31	30	29	28	27	26	25	24
ValidBit	RW	Reserved	ADD1				

23	22	21	20	19	18	17	16
ADD1							

15	14	13	12	11	10	9	8
ADD1							

7	6	5	4	3	2	1	0
ADD1							

Name	R/W	Bit	After Reset	Function
ValidBit	R/W	31	0	Set to 1 if the second bus cycle is necessary.
RW	R/W	30	0	Sets read/write in the second bus cycle. 0: Read, 1: Write
Reserved	R	29	–	Reserved. When this bit is read, 0 is returned.
ADD1	R/W	28:0	0	Sets the address of the second bus cycle.

(6) Flash command (DATA1) setting register

This register (AB0_FLASHCOMDATA1: 2FFF_001CH) sets the command to the Intel flash memory. This register sets the data in the second command cycle.

This register is used when the command to the flash memory is a two-cycle command and, when it is used, set the ValidBit bit of the AB0_FLASHCOMADD1 register to 1.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
DATA1							
7	6	5	4	3	2	1	0
DATA1							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	–	Reserved. When these bits are read, 0 is returned for each bit.
DATA1	R/W	15:0		Sets the data of the second bus cycle.

(7) Flash clock control register

This register (AB0_FLASHCLKCTRL: 2FFF_0080H) sets a frequency ratio of the AB0 clock to the flash memory clock (FLA_CLK).

- 1: AB0 clock → FLA_CLK = 2:1 (166 MHz: 83 MHz is assumed.)
- 0: AB0 clock → FLA_CLK = 1:1

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							CLK_MODE

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	–	Reserved. When these bits are read, 0 is returned for each bit.
CLK_MODE	R/W	0	1	Sets external memory clock mode (frequency ratio). 0: AB0 → FLA_CLK = 1:1 1: AB0 → FLA_CLK = 2:1

(8) Flash read clock delay adjustment register

AB0_FLA_RCLK_DLY: 2FFF_0084H

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved			DATA_DLY	Reserved		CLK_SEL	NEG_SEL

15	14	13	12	11	10	9	8
Reserved			RCLK_PHASE	RCLK_DLY			

7	6	5	4	3	2	1	0
RCLK_DLY							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:21	–	Reserved. When these bits are read, 0 is returned for each bit.
DATA_DLY	R/W	20	0	Sets AB0 internal data capturing timing. 0: No delay 1: 1-clock delay
Reserved	R	19:18		Reserved. When these bits are read, 0 is returned for each bit.
CLK_SEL	R/W	17	0	Selects clock source of first-stage F/F of read data. 0: RCLK 1: CLK
NEG_SEL	R/W	16	0	Sets phase of data for RCLK of data that switches between RCLK and CLK. 0: Positive edge 1: Negative edge
Reserved	R	15:13	–	Reserved. When these bits are read, 0 is returned for each bit.
RCLK_PHASE	R/W	12	1B	Controls phase of RCLK. 0: Inverted 1: Normal
RCLK_DLY	R/W	11:0	000H	Selects an RCLK delay amount. 000H: 0 ns 001H: 0.5 ns 003H: 1.0 ns 007H: 1.5 ns 00FH: 2.0 ns 01FH: 2.5 ns 03FH: 3.0 ns 07FH: 3.5 ns 0FFH: 4.0 ns 1FFH: 4.5 ns 3FFH: 5.0 ns 7FFH: 5.5 ns FFFH: 6.0 ns

(9) Wait pin status register

AB0_WAIT_STATUS: 2FFF_0090H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							WAIT

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	–	Reserved. When these bits are read, 0 is returned for each bit.
WAIT	R/W	0	1	Indicates the WAIT pin status. 0: WAIT pin is low level 1: WAIT pin is high level

(10) CSn base address register

AB0_***slave***BASEADD: 2FFF_0100H + nx10H (n represents the slave number)

31	30	29	28	27	26	25	24
Reserved		ADD					
23	22	21	20	19	18	17	16
ADD							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

Name	R/W	Bit	After Reset	Function
Reserved	R/W	31:30	–	Reserved. When these bits are read, 0 is returned for each bit.
ADD	R/W	29:16	See table below	Slave base address
Reserved	R/W	15:0	–	Reserved. When these bits are read, 0 is returned for each bit.

The initial values are as follows.

Table E-4. Initial Values (BASEADD)

Slave No.	Initial Value
0	0000_0000H
1 to 3	3FFF_0000H

This register sets the base address for each slave. However, [31:30] and [15:0] are fixed to 0 and cannot be set.

The settable range is 0000_0000H to 2FFF_0000H, except for 2FFF_0000H to 2FFF_FFFFH, because these areas are reserved for the AB0 local registers.

The base address cannot be set extending from one bank to another.

This register must be set together with the AB0_***slave***BITCOMP register.

Caution If the same address range or base address is set for separate CSs, the CS with the lower index is activated.

(11) CSn bit compare register

AB0_***slave***BITCOMP: 2FFF_0104H + nx10H (n represents the slave number)

31	30	29	28	27	26	25	24
BITCOMP							
23	22	21	20	19	18	17	16
BITCOMP							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

Name	R/W	Bit	After Reset	Function
BITCOMP	R/W	31:16	See table below	Specifies the valid bit range (bit range of [31:30] is ignored because of the relationship with the base address register).
Reserved	R/W	15:0	–	Reserved. When these bits are read, 0 is returned for each bit.

The initial values are as follows.

Table E-5. Initial Values (BITCOMP)

Slave No.	Initial Value
0	F000_0000H
1 to 3	FFFF_0000H

This register sets the address range for each slave. This register enables the CSZ pin of a slave, using the following logic.

AB0_***slave***BASEADD & AB0_***slave***BITCOMP = (input address) & AB0_*slave*BITCOMP

Setting example 1

When setting 1010_0000H to 101F_FFFFH as slave 1:

AB0_CS1BASEADD = 1010_0000H, AB0_CS1BITCOMP = FFF0_0000H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CS1BITCOMP	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
CS1BASEADD	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

ADDR	ADDR[31:20] and BASEAD[31:20] are compared. If they match, this field is selected.	

Setting example 2

When setting 0000_0000H to 0FFF_FFFFH as slave 0:

AB0_CS0BASEADD = 0000_0000H, AB0_CS0BITCOMP = F000_0000H

	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CS0BITCOMP	1	1	1	1	0	0	0	0	0	0	0	0	0	0

	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CS0BASEADD	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	31:28
ADDR	ADDR[31:28]

(12) CSn wait control register

AB0_***slave***WAITCTRL: 2FFF_0200H + nx20H (n represents the slave number)

31	30	29	28	27	26	25	24
Reserved					CSInt		
23	22	21	20	19	18	17	16
Reserved				T2			
15	14	13	12	11	10	9	8
Reserved			T1				
7	6	5	4	3	2	1	0
Reserved				T0			

Name	R/W	Bit	After Reset	Function
Reserved	R	31:27	–	Reserved. When these bits are read, 0 is returned for each bit.
CSInt	R/W	26:24	0H	CS = H period control. CSInt + 1 cycle is set.
Reserved	R	23:20	–	Reserved. When these bits are read, 0 is returned for each bit.
T2	R/W	19:16	FH	Controls T2 waits.
Reserved	R	15:13	–	Reserved. When these bits are read, 0 is returned for each bit.
T1	R/W	12:8	1FH	Controls T1 waits. Set 1 or larger value.
Reserved	R	7:4	–	Reserved. When these bits are read, 0 is returned for each bit.
T0	R/W	3:0	FH	Controls T0 waits.

This register sets read wait timing parameters T0, T1, T2, and CSInt for the asynchronous bus control signal.

CSInt is also used for writing.

The set value is based on the number of FLA_CLK cycles.

Therefore, the set value is doubled in AB0 in the clock ratio 2:1 mode.

For example, a wait shown in the following examples will be inserted.

- CLK = 100 MHz and FLA_CLK = 50 MHz (in 2:1 clock ratio mode): 20 ns, where T1 = 1
- CLK = 100 MHz and FLA_CLK = 100 MHz (in 1:1 clock ratio mode): 10 ns, where T1 = 1

[Setting range]

T0: Can be set in a range from 0 to 15. The initial value is wait = 15 cycles.

T1: Can be set in a range from 1 to 31. The initial value is wait = 31 cycles.

T2: Can be set in a range from 0 to 15. The initial value is wait = 15 cycles.

CSInt: Can be set in a range from 0 to 7. The initial value is 0. A CSInt cycle is the set value + 1.

Cautions 1. In single/page read mode

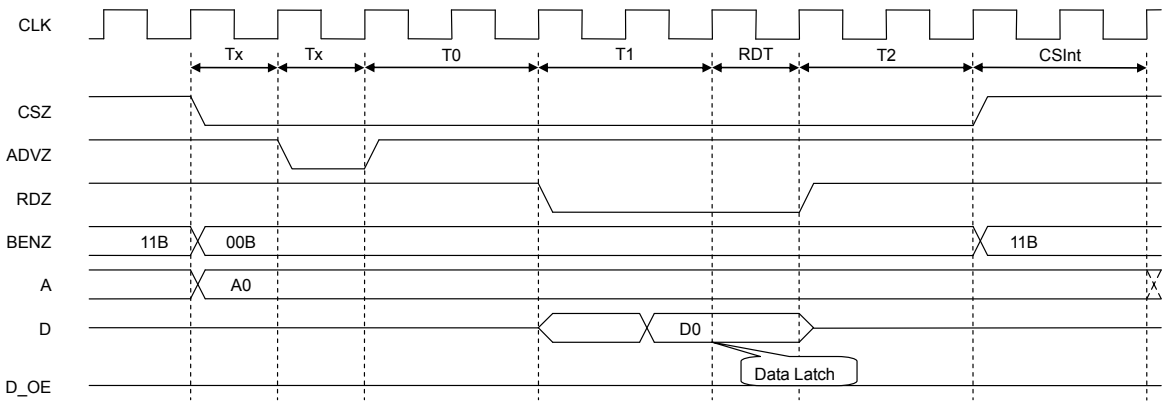
- **In the clock ratio 2:1 mode, make sure that the total of the set values of RDT, T2, and CSInt is 1 or more.**
- **In the clock ratio 1:1 mode, make sure that the total of the set values of RDT, T2, and CSInt is 2 or more.**

2. The MIN value of T1 is "1". Even if "0" is set, the operation is performed in the same manner as when "1" is set.

3. If the set value of T0 is "0" when the AD-Mux bus is used, the operation is performed in the same manner as when "1" is set.

Figure E-1 shows the single read timing with Non Mux.

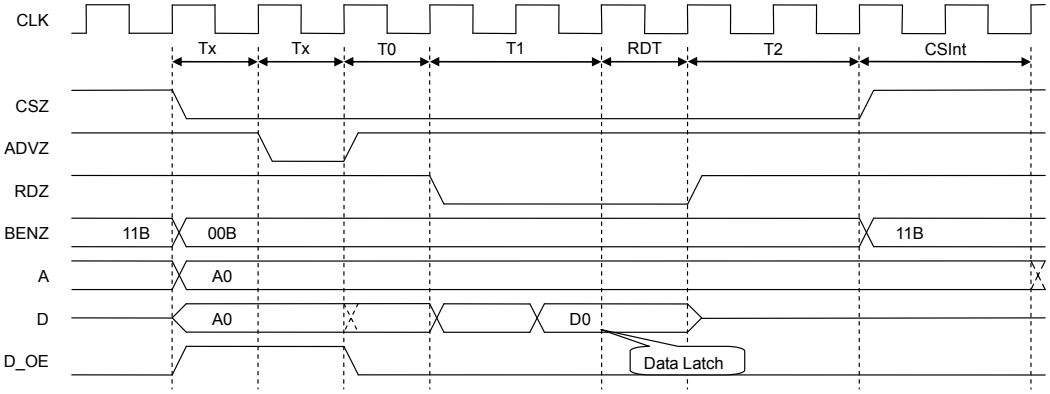
Figure E-1. Single Read Timing (Non Mux)



It's possible to choose Tx in ADV_WIDTH:AB0_slaveCONTROL[8].

Figure E-2 shows the single read timing with AD-Mux.

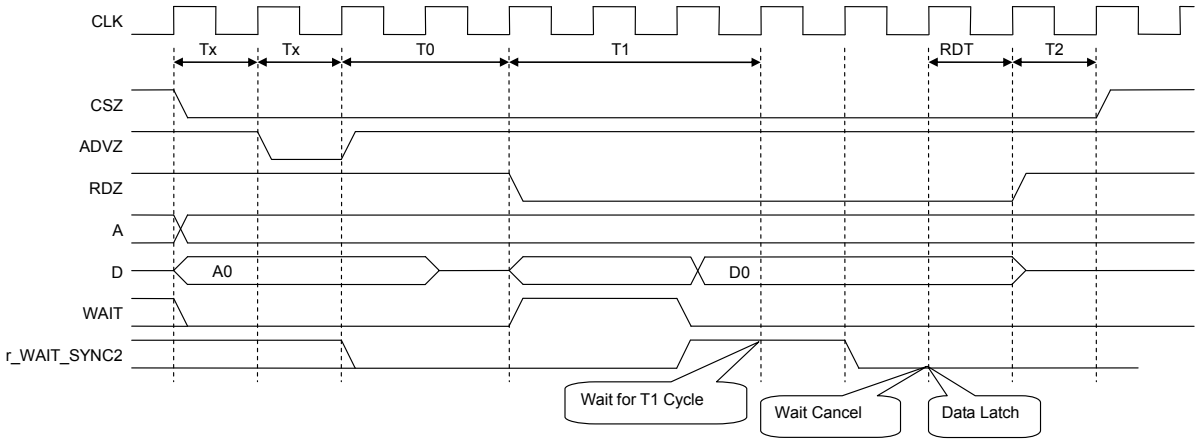
Figure E-2. Single Read Timing (AD-Mux)



It's possible to choose Tx in ADV_WIDTH:AB0_slaveCONTROL[8].

Figure E-3 shows the wait timing chart in the single read mode. The WAIT signal is delayed by two clocks because of synchronization. The WAIT signal is masked by the AB0_***slave***WAIT_MASK register.

Figure E-3. Wait Timing (Single Read)



It's possible to choose Tx in ADV_WIDTH:AB0_slaveCONTROL[8].

Caution Set the value of T1 so that it lasts three clocks or longer after the delay of the WAIT signal.

(13) CSn write wait control register

AB0_***slave***WAITCTRL_W: 2FFF_0204H + nx20H (n represents the slave number)

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved				T2_W			

15	14	13	12	11	10	9	8
Reserved			T1_W				

7	6	5	4	3	2	1	0
Reserved				T0_W			

Name	R/W	Bit	After Reset	Function
Reserved	R	31:20	–	Reserved. When these bits are read, 0 is returned for each bit.
T2_W	R/W	19:16	FH	Controls T2_W WAIT waits.
Reserved	R	15:13	–	Reserved. When these bits are read, 0 is returned for each bit.
T1_W	R/W	12:8	1FH	Controls T1_W WAIT waits. Set 1 or a larger value.
Reserved	R	7:4	–	Reserved. When these bits are read, 0 is returned for each bit.
T0_W	R/W	3:0	FH	Controls T0_W waits.

This register sets write wait timing parameters (T0_W, T1_W, and T2_W) for asynchronous bus control signal. The setting for CSInt during read is used (see **(12) CSn wait control register**).

Caution T1_W is the set cycle + one clock. CSInt during write is (set value + 1) cycles + one clock.

The set value is based on the number of the flash memory clock (FLA_CLK) cycles .

Therefore, the set value is doubled in AB0 in the clock ratio 2:1 mode.

For example, a wait shown in the following examples will be inserted.

- CLK = 100 MHz and FLA_CLK = 50 MHz (2:1 clock ratio mode): 20 + 10 = 30 ns, where T1_W = 1
- CLK = 100 MHz and FLA_CLK = 100 MHz (1:1 clock ratio mode): 10 + 10 = 20 ns, where T1_W = 1

[Setting range]

T0: Can be set in a range from 0 to 15. The initial value is wait = 15 cycles.

T1: Can be set in a range from 1 to 31. The initial value is wait = 31 cycles.

T2: Can be set in a range from 0 to 15. The initial value is wait = 15 cycles.

CSInt: References the value of the CSInt bit of AB0_***slave***WAITCTRL for wait value during read.

Cautions 1. In burst write mode (one NAND access), set CSInt to a value of 1 or more.

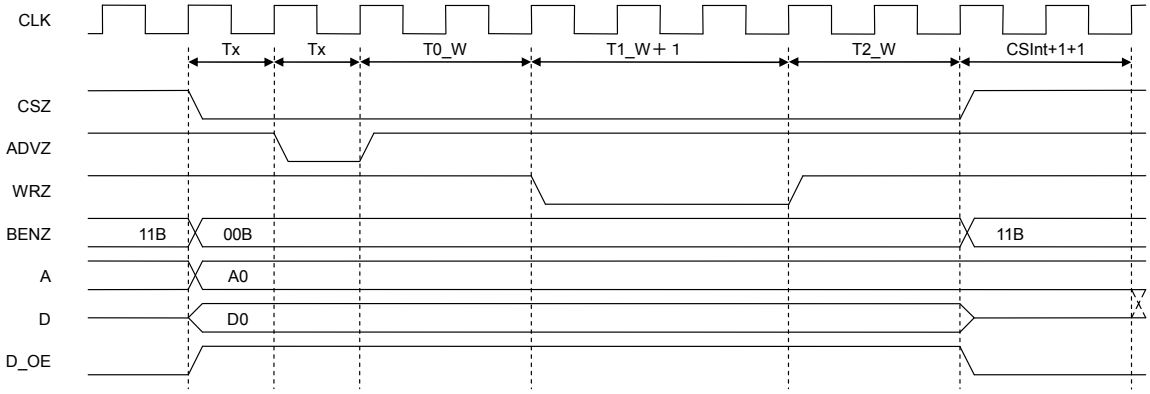
2. In single write mode, set T2_W to a value of 1 or more.

3. The MIN value of T1 is "1". Even if "0" is set, the operation is performed in the same manner as when "1" is set.

4. If T0_W = 0 when the AD-Mux bus is used, the address is extended by one clock cycle because it is held. Consequently, output of write data is delayed by one clock. At this time, set T1_W to a value of 2 or more.

Figure E-4 shows the single write timing with Non Mux.

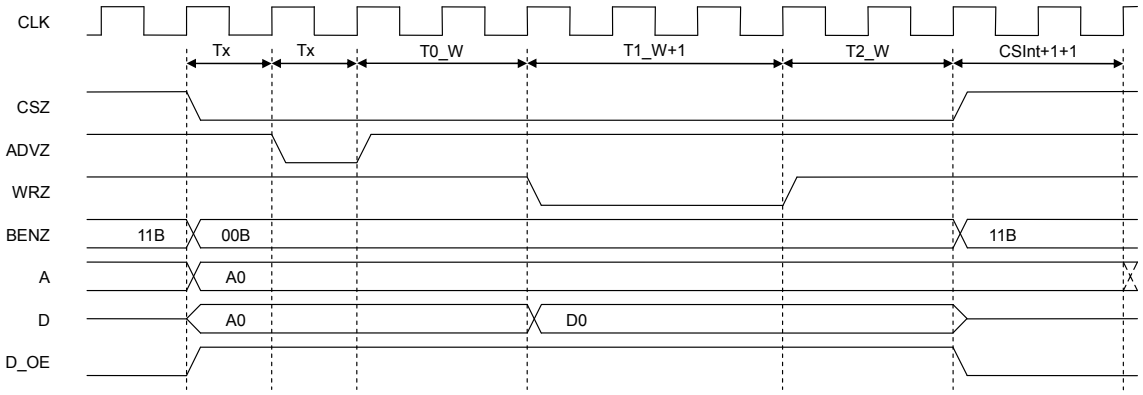
Figure E-4. Single Write Timing (Non Mux) (Clock Ratio = 1:1)



It's possible to choose Tx in ADV_WIDTH:AB0_slaveCONTROL[8].

Figure E-5 shows the single write timing with AD-Mux when T0 > 0.

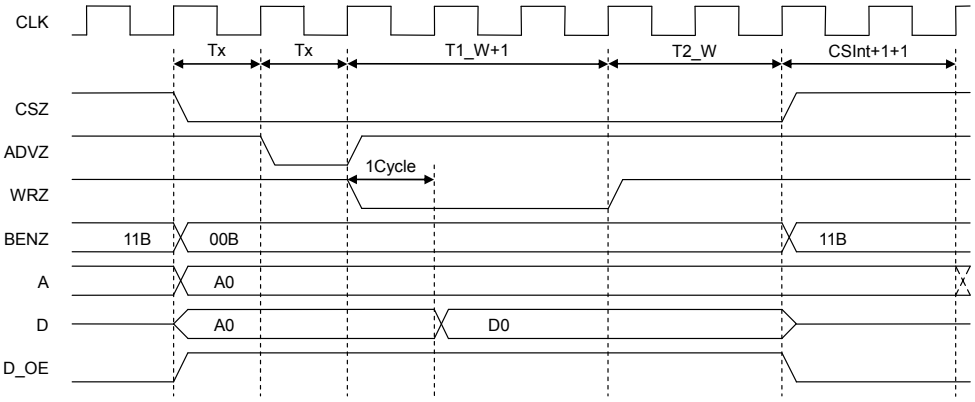
Figure E-5. Single Write Timing (AD-Mux) (T0 > 0) (Clock Ratio = 1:1)



It's possible to choose Tx in ADV_WIDTH:AB0_slaveCONTROL[8].

Figure E-6 shows the single write timing with AD-Mux when T0_W = 0.

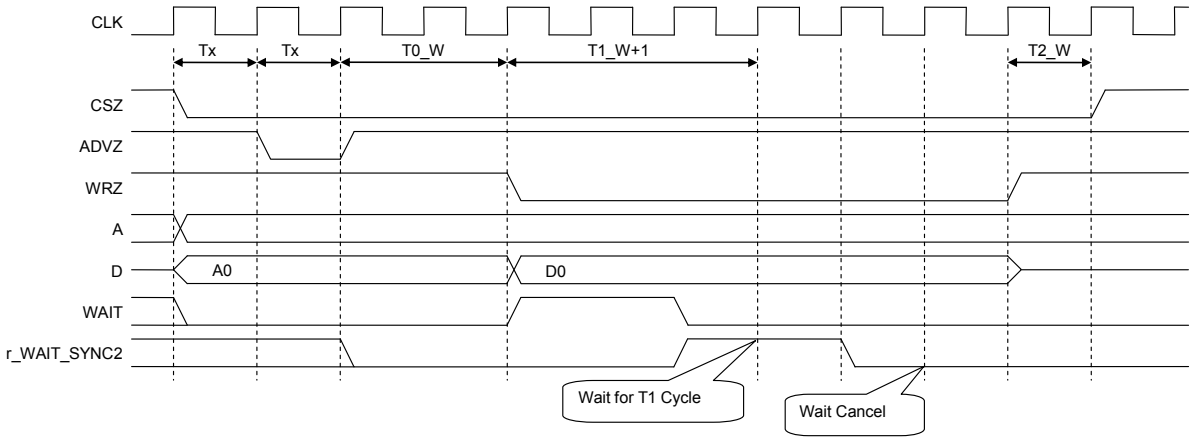
Figure E-6. Single Write Timing (AD-Mux) (T0_W = 0) (Clock Ratio = 1:1)



It's possible to choose Tx in ADV_WIDTH:AB0_slaveCONTROL[8].

Figure E-7 shows the wait timing chart in the single write mode. The WAIT signal is delayed by two clocks because of synchronization. The WAIT signal is masked by the AB0_***slave***WAIT_MASK register.

Figure E-7. Wait Timing (Single Write) (Clock Ratio = 1:1)



It's possible to choose Tx in ADV_WIDTH:AB0_slaveCONTROL[8].

Caution Set the value of T1_W so that it lasts three clocks or longer after the delay of the WAIT signal.

(14) CSn read mode register

AB0_***slave***READCTRL: 2FFF_0208H + nx20H (n represents the slave number)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved			RDT		Reserved		READMODE

Name	R/W	Bit	After Reset	Function
Reserved	R	31:6	–	Reserved. When these bits are read, 0 is returned for each bit.
RDT	R/W	5:4	0H	Sets the timing of changing read data latch. 0: Deasserts RDZ signal 1 clock after latch timing. 1: Deasserts RDZ signal 2 clocks after latch timing. 2: Deasserts RDZ signal 3 clocks after latch timing. 3: Deasserts RDZ signal 4 clocks after latch timing.
Reserved	R	3:2	–	Reserved. When these bits are read, 0 is returned for each bit.
READMODE	R/W	1:0	0H	Sets the read mode. 0: Single read mode 1: Single read mode 2: Page read mode 3: Setting prohibitted

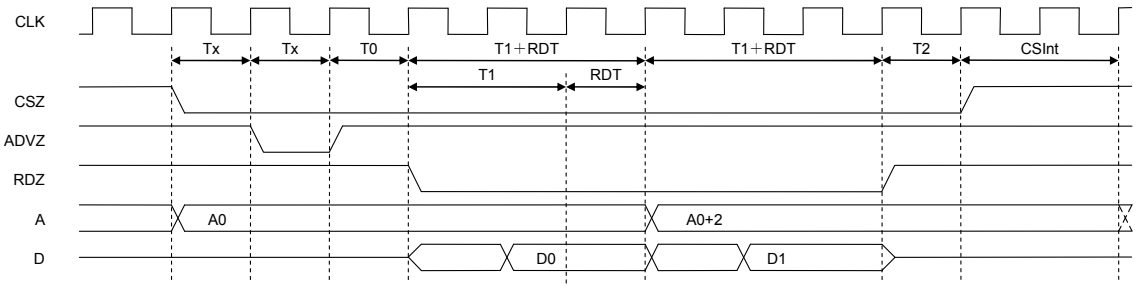
The RDT set value is based on the number of FLA_CLK cycles.
Therefore, the set value is doubled in AB0 in the clock ratio 2:1 mode.

In the read cycle, data is captured to an internal register when a T1 period of T1 + RDT has passed and can be held during the period specified by RDT.

Cautions 1. Set RDT to a value of 1 or more in the page read mode in the clock ratio 1:1 mode.

Figure E-8 shows the read timing in the page read mode.

Figure E-8. Page Read Timing (Clock Ratio = 1:1)



It's possible to choose Tx in ADV_WIDTH:AB0_slaveCONTROL[8].

(15) CSn wait mask register

This register (AB0_***slave***WAIT_MASK: 2FFF_020CH + nx20H masks the WAIT pin. (n represents the slave number)

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							WAIT_MASK

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	–	Reserved. When these bits are read, 0 is returned for each bit.
WAIT MASK	R/W	0	0	Masks WAIT pin. 0: Masks WAIT pin. 1: Unmasks WAIT pin.

Caution The WAIT pin is masked after reset.

Set this bit together with WP of the AB0_*slave*FLASHRCRCSx register in (17).

(16) CSn control register

AB0_***slave***CONTROL: 2FFF_0210H + nx20H (n represents the slave number)

31	30	29	28	27	26	25	24
Reserved							CS_FCLK

23	22	21	20	19	18	17	16
Reserved						CS_ADV	

15	14	13	12	11	10	9	8
Reserved							ADV_WIDTH

7	6	5	4	3	2	1	0
Reserved					AD_OE	ADDR_SEL	ADMUX_SEL

Name	R/W	Bit	After Reset	Function
Reserved	R	31:25	–	Reserved. When these bits are read, 0 is returned for each bit.
CS_FCLK	R/W	24	0	Sets the FLA_CLK output start timing. 0: After the falling edge of CSZ 1: One clock after the falling edge of CSZ
Reserved	R	23:18	–	Reserved. When these bits are read, 0 is returned for each bit.
CS_ADV	R/W	17:16	1	Sets the timing between CSZ and ADVZ. 0: 0 cycles between CSZ and ADVZ 1: 1 cycle between CSZ and ADVZ 2: 2 cycles between CSZ and ADVZ 3: 3 cycles between CSZ and ADVZ
Reserved	R	15:9	–	Reserved. When these bits are read, 0 is returned for each bit.
ADV__WIDTH	R/W	8	1	Sets the ADV signal width. 0: 1 clock 1: 2 clocks
Reserved	R	7:3	–	Reserved. When these bits are read, 0 is returned for each bit.
AD_OE	R/W	2	0	Controls Hi-Z timing of address output to AD bus when the AD-Mux bus is read. 0: Hi-Z at rising edge of ADVZ 1: Hi-Z one clock before falling edge of RDZ
ADDR_SEL	R/W	1	0	Selects address output. 0: Outputs A26 to A17. 1: Outputs A10 to A1.
ADMUX_SEL	R/W	0	0	Selects AD-Mux device or Non Mux device. 0: AD-MUX 1: Non MUX (A-D Separate)

(17) CSn read configuration register

AB0_***slave***FLASHRCR: 2FFF_0214H + nx20H (n represents the slave number)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
RM	Reserved				WP	Reserved	WD
7	6	5	4	3	2	1	0
Reserved							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	–	Reserved. When these bits are read, 0 is returned for each bit.
RM	R/W	15	1H	Read mode 0: Synchronous burst mode read 1: Asynchronous page mode read (default)
Reserved	R	14:11	–	Reserved. When these bits are read, 0 is returned for each bit.
WP	R/W	10	1H	Polarityof WAIT signal 0: Active low 1: Active high (default)
Reserved	R	9	–	Reserved. When this bit is read, 0 is returned.
WD	R/W	8	1H	Wait delay 0: WAIT is deasserted with valid data (Not supported in AB0) 1: WAIT is deasserted one clock before valid data (default)
Reserved	R	7:0	–	Reserved. When these bits are read, 0 is returned for each bit.

APPENDIX F INTERRUPT (AINT)

F.1 Register Function Details

The following shows the bit configuration of interrupt registers (see **APPENDIX A REGISTERS** for the registers).

F.1.1 Interrupt mask registers

The following registers are available for setting interrupt masking.

<1> ACPU (address offset: C002_xxxxH)

IT0_IEN0/1/2: Interrupt enable setting register (mask cancel)

IT0_IDS0/1/2: Interrupt disable setting register (mask setting)

<2> ADSP (address offset: C002_xxxxH)

IT3_IEN0/1/2: Interrupt enable setting register (mask cancel)

IT3_IDS0/1/2: Interrupt disable setting register (mask setting)

<3> MSE (address offset: CC01_xxxxH)

IT4_IEN0/1/2: Interrupt enable setting register (mask cancel)

IT4_IDS0/1/2: Interrupt disable setting register (mask setting)

Caution The interrupt mask status can be checked by reading ITx_IENx. The disable settings made with ITx_IDSx are reflected to the corresponding bits of the ITx_IENx register.

Set interrupts by using the above two types of registers (IEN/IDS). To enable or disable an interrupt source, set the relevant bit to “1”.

(1) ACPU interrupt enable setting register 0

IT0_IEN0: C002_0000H

31	30	29	28	27	26	25	24
IEN_[31:24]							
23	22	21	20	19	18	17	16
IEN_[23:16]							
15	14	13	12	11	10	9	8
IEN_[15:8]							
7	6	5	4	3	2	1	0
IEN_[7:0]							

Name	R/W	Bit	After Reset	Function
IEN_**	W	31:0	0	The IEN_[31:0] bits correspond to INT[31:0]. 1: Enables interrupts (cancels interrupt masking). 0: No operation
IEN_**	R	31:0	0	1: Interrupts enabled 0: Interrupts disabled

(2) ACPU interrupt enable setting register 1

IT0_IEN1: C002_0004H

31	30	29	28	27	26	25	24
IEN_[63:56]							
23	22	21	20	19	18	17	16
IEN_[55:48]							
15	14	13	12	11	10	9	8
IEN_[47:40]							
7	6	5	4	3	2	1	0
IEN_[39:32]							

Name	R/W	Bit	After Reset	Function
IEN_**	W	31:0	0	The IEN_[63:32] bits correspond to INT[63:32]. 1: Enables interrupts (cancels interrupt masking). 0: No operation
IEN_**	R	31:0	0	1: Interrupts enabled 0: Interrupts disabled

(3) ACPU interrupt enable setting register 2

IT0_IEN2: C002_0100H

31	30	29	28	27	26	25	24
IEN_[95:88]							
23	22	21	20	19	18	17	16
IEN_[87:80]							
15	14	13	12	11	10	9	8
IEN_[79:72]							
7	6	5	4	3	2	1	0
IEN_[71:64]							

Name	R/W	Bit	After Reset	Function
IEN_**	W	31:0	0	The IEN_[95:64] bits correspond to INT[95:64]. 1: Enables interrupts (cancels interrupt masking). 0: No operation
IEN_**	R	31:0	0	1: Interrupts enabled 0: Interrupts disabled

(4) ACPU interrupt disable setting register 0

IT0_IDS0: C002_0008H

31	30	29	28	27	26	25	24
IDS_[31:24]							
23	22	21	20	19	18	17	16
IDS_[23:16]							
15	14	13	12	11	10	9	8
IDS_[15:8]							
7	6	5	4	3	2	1	0
IDS_[7:0]							

Name	R/W	Bit	After Reset	Function
IDS_**	W	31:0	0	The IDS_[31:0] bits correspond to INT[31:0]. 1: Disables interrupts (mask setting). 0: No operation

(5) ACPU interrupt disable setting register 1

IT0_IDS1: C002_000CH

31	30	29	28	27	26	25	24
IDS_[63:56]							
23	22	21	20	19	18	17	16
IDS_[55:48]							
15	14	13	12	11	10	9	8
IDS_[47:40]							
7	6	5	4	3	2	1	0
IDS_[39:32]							

Name	R/W	Bit	After Reset	Function
IDS_**	W	31:0	0	The IDS_[63:32] bits correspond to INT[63:32]. 1: Disables interrupts (mask setting). 0: No operation

(6) ACPU interrupt disable setting register 2

IT0_IDS2: C002_0104H

31	30	29	28	27	26	25	24
IDS_[95:88]							
23	22	21	20	19	18	17	16
IDS_[87:80]							
15	14	13	12	11	10	9	8
IDS_[79:72]							
7	6	5	4	3	2	1	0
IDS_[71:64]							

Name	R/W	Bit	After Reset	Function
IDS_**	W	31:0	0	The IDS_[95:64] bits correspond to the [95:64]. 1: Disables interrupts (mask setting). 0: No operation

(7) ADSP interrupt enable setting register 0

IT3_IEN0: C002_C000H

31	30	29	28	27	26	25	24
IEN_[31:24]							
23	22	21	20	19	18	17	16
IEN_[23:16]							
15	14	13	12	11	10	9	8
IEN_[15:8]							
7	6	5	4	3	2	1	0
IEN_[7:0]							

Name	R/W	Bit	After Reset	Function
IEN_**	W	31:0	0	The IEN_[31:0] bits correspond to INT[31:0]. 1: Enables interrupts (cancels interrupt masking). 0: No operation
IEN_**	R	31:0	0	1: Interrupts enabled 0: Interrupts disabled

(8) ADSP interrupt enable setting register 1

IT3_IEN1: C002_C004H

31	30	29	28	27	26	25	24
IEN_[63:56]							
23	22	21	20	19	18	17	16
IEN_[55:48]							
15	14	13	12	11	10	9	8
IEN_[47:40]							
7	6	5	4	3	2	1	0
IEN_[39:32]							

Name	R/W	Bit	After Reset	Function
IEN_**	W	31:0	0	The IEN_[63:32] bits correspond to INT[63:32]. 1: Enables interrupts (cancels interrupt masking). 0: No operation
IEN_**	R	31:0	0	1: Interrupts enabled 0: Interrupts disabled

(9) ADSP interrupt enable setting register 2

IT3_IEN2: C002_C100H

31	30	29	28	27	26	25	24
IEN_[95:88]							
23	22	21	20	19	18	17	16
IEN_[87:80]							
15	14	13	12	11	10	9	8
IEN_[79:72]							
7	6	5	4	3	2	1	0
IEN_[71:64]							

Name	R/W	Bit	After Reset	Function
IEN_**	W	31:0	0	The IEN_[95:64] bits correspond to INT[95:64]. 1: Enables interrupts (cancels interrupt masking). 0: No operation
IEN_**	R	31:0	0	1: Interrupts enabled 0: Interrupts disabled

(10) ADSP interrupt disable setting register 0

IT3_IDS0: C002_C008H

31	30	29	28	27	26	25	24
IDS_[31:24]							
23	22	21	20	19	18	17	16
IDS_[23:16]							
15	14	13	12	11	10	9	8
IDS_[15:8]							
7	6	5	4	3	2	1	0
IDS_[7:0]							

Name	R/W	Bit	After Reset	Function
IDS_**	W	31:0	0	The IDS_[31:0] bits correspond to INT[31:0]. 1: Disables interrupts (mask setting). 0: No operation

(11) ADSP interrupt disable setting register 1

IT3_IDS1: C002_C00CH

31	30	29	28	27	26	25	24
IDS_[63:56]							
23	22	21	20	19	18	17	16
IDS_[55:48]							
15	14	13	12	11	10	9	8
IDS_[47:40]							
7	6	5	4	3	2	1	0
IDS_[39:32]							

Name	R/W	Bit	After Reset	Function
IDS_**	W	31:0	0	The IDS_[63:32] bits correspond to INT[63:32]. 1: Disables interrupts (mask setting). 0: No operation

(12) ADSP interrupt disable setting register 2

IT3_IDS2: C002_C104H

31	30	29	28	27	26	25	24
IDS_[95:88]							
23	22	21	20	19	18	17	16
IDS_[87:80]							
15	14	13	12	11	10	9	8
IDS_[79:72]							
7	6	5	4	3	2	1	0
IDS_[71:64]							

Name	R/W	Bit	After Reset	Function
IDS_**	W	31:0	0	The IDS_[95:64] bits correspond to INT[95:64]. 1: Disables interrupts (mask setting). 0: No operation

F.1.2 Interrupt source status registers

The following registers are available for showing the interrupt source statuses.

<1> ACPU (address offset: C002_xxxxH)

IT0_RAW0/1/2: Interrupt raw status register

IT0_MST0/1/2: Interrupt mask status register

<2> ADSP (address offset: C002_xxxxH)

IT3_RAW0/1/2: Interrupt raw status register

IT3_MST0/1/2: Interrupt mask status register

(1) ACPU interrupt raw status register 0

IT0_RAW0: C002_0010

31	30	29	28	27	26	25	24
RAW_[31:24]							
23	22	21	20	19	18	17	16
RAW_[23:16]							
15	14	13	12	11	10	9	8
RAW_[15:8]							
7	6	5	4	3	2	1	0
RAW_[7:0]							

Name	R/W	Bit	After Reset	Function
RAW_**	R	31:0	0	The RAW_[31:0] bits correspond to INT[31:0]. 1: Interrupts detected. 0: Interrupts not detected.

(2) ACPU interrupt raw status register 1

IT0_RAW1: C002_0014H

31	30	29	28	27	26	25	24
RAW_[63:56]							
23	22	21	20	19	18	17	16
RAW_[55:48]							
15	14	13	12	11	10	9	8
RAW_[47:40]							
7	6	5	4	3	2	1	0
RAW_[39:32]							

Name	R/W	Bit	After Reset	Function
RAW_**	R	31:0	0	The RAW_[63:32] bits correspond to INT[63:32]. 1: Interrupts detected. 0: Interrupts not detected.

(3) ACPU interrupt raw status register 2

IT0_RAW2: C002_0108H

31	30	29	28	27	26	25	24
RAW_[95:88]							
23	22	21	20	19	18	17	16
RAW_[87:80]							
15	14	13	12	11	10	9	8
RAW_[79:72]							
7	6	5	4	3	2	1	0
RAW_[71:64]							

Name	R/W	Bit	After Reset	Function
RAW_**	R	31:0	0	The RAW_[95:64] bits correspond to INT[95:64]. 1: Interrupts detected. 0: Interrupts not detected.

(4) ACPU interrupt mask status register 0

IT0_MST0: C002_0018H

31	30	29	28	27	26	25	24
MST_[31:24]							
23	22	21	20	19	18	17	16
MST_[23:16]							
15	14	13	12	11	10	9	8
MST_[15:8]							
7	6	5	4	3	2	1	0
MST_[7:0]							

Name	R/W	Bit	After Reset	Function
MST_**	R	31:0	0	The MST_[31:0] bits correspond to INT[31:0]. When a bit that masks the corresponding interrupt is read, 0 is returned. 1: Interrupts detected. 0: Interrupts not detected.

(5) ACPU interrupt mask status register 1

IT0_MST1: C002_001CH

31	30	29	28	27	26	25	24
MST_[63:56]							
23	22	21	20	19	18	17	16
MST_[55:48]							
15	14	13	12	11	10	9	8
MST_[47:40]							
7	6	5	4	3	2	1	0
MST_[39:32]							

Name	R/W	Bit	After Reset	Function
MST_**	R	31:0	0	The MST_[63:32] bits correspond to INT[63:32]. When a bit that masks the corresponding interrupt is read, 0 is returned. 1: Interrupts detected. 0: Interrupts not detected.

(6) ACPU interrupt mask status register 2

IT0_MST2: C002_010CH

31	30	29	28	27	26	25	24
MST_[95:88]							
23	22	21	20	19	18	17	16
MST_[87:80]							
15	14	13	12	11	10	9	8
MST_[79:72]							
7	6	5	4	3	2	1	0
MST_[71:64]							

Name	R/W	Bit	After Reset	Function
MST_**	R	31:0	0	The MST_[95:64] bits correspond to INT[95:64]. When a bit that masks the corresponding interrupt is read, 0 is returned. 1: Interrupts detected. 0: Interrupts not detected.

(7) ADSP interrupt raw status register 0

IT3_RAW0: C002_C010H

31	30	29	28	27	26	25	24
RAW_[31:24]							
23	22	21	20	19	18	17	16
RAW_[23:16]							
15	14	13	12	11	10	9	8
RAW_[15:8]							
7	6	5	4	3	2	1	0
RAW_[7:0]							

Name	R/W	Bit	After Reset	Function
RAW_**	R	31:0	0	The RAW_[31:0] bits correspond to INT[31:0]. 1: Interrupts detected. 0: Interrupts not detected.

(8) ADSP interrupt raw status register 1

IT3_RAW1: C002_C014H

31	30	29	28	27	26	25	24
RAW_[63:56]							
23	22	21	20	19	18	17	16
RAW_[55:48]							
15	14	13	12	11	10	9	8
RAW_[47:40]							
7	6	5	4	3	2	1	0
RAW_[39:32]							

Name	R/W	Bit	After Reset	Function
RAW_**	R	31:0	4000_0000	The RAW_[63:32] bits correspond to INT[63:32]. 1: Interrupts detected. 0: Interrupts not detected.

(9) ADSP interrupt raw status register 2

IT3_RAW2: C002_C108H

31	30	29	28	27	26	25	24
RAW_[95:88]							
23	22	21	20	19	18	17	16
RAW_[87:80]							
15	14	13	12	11	10	9	8
RAW_[79:72]							
7	6	5	4	3	2	1	0
RAW_[71:64]							

Name	R/W	Bit	After Reset	Function
RAW_**	R	31:0	0	The RAW_[95:64] bits correspond to INT[95:64]. 1: Interrupts detected. 0: Interrupts not detected.

(10) ADSP interrupt mask status register 0

IT3_MST0: C002_C018H

31	30	29	28	27	26	25	24
MST_[31:24]							
23	22	21	20	19	18	17	16
MST_[23:16]							
15	14	13	12	11	10	9	8
MST_[15:8]							
7	6	5	4	3	2	1	0
MST_[7:0]							

Name	R/W	Bit	After Reset	Function
MST_**	R	31:0	0	The MST_[31:0] bits correspond to INT[31:0]. When a bit that masks the corresponding interrupt is read, 0 is returned. 1: Interrupts detected. 0: Interrupts not detected.

(11) ADSP interrupt mask status register 1

IT3_MST1: C002_C01CH

31	30	29	28	27	26	25	24
MST_[63:56]							
23	22	21	20	19	18	17	16
MST_[55:48]							
15	14	13	12	11	10	9	8
MST_[47:40]							
7	6	5	4	3	2	1	0
MST_[39:32]							

Name	R/W	Bit	After Reset	Function
MST_**	R	31:0	0	The MST_[63:32] bits correspond to INT[63:32]. When a bit that masks the corresponding interrupt is read, 0 is returned. 1: Interrupts detected. 0: Interrupts not detected.

(12) ADSP interrupt mask status register 2

IT3_MST2: C002_C10CH

31	30	29	28	27	26	25	24
MST_[95:88]							
23	22	21	20	19	18	17	16
MST_[87:80]							
15	14	13	12	11	10	9	8
MST_[79:72]							
7	6	5	4	3	2	1	0
MST_[71:64]							

Name	R/W	Bit	After Reset	Function
MST_**	R	31:0	0	The MST_[95:64] bits correspond to INT[95:64]. When a bit that masks the corresponding interrupt is read, 0 is returned. 1: Interrupts detected. 0: Interrupts not detected.

F.1.3 Interrupt source status reset registers

These registers reset the interrupt source status bits. These registers target the modules that report occurrence of interrupts by using pulses. In the modules that report the occurrence of interrupts by using level signals, interrupts are automatically reset when the interrupt input signal is deasserted (High → Low).

<1> ACPU (address offset: C002_xxxxH)
IT0_IIR: Source status reset register
<2> ADSP (address offset: C002_xxxxH)
IT3_IIR: Source status reset register

(1) ACPU interrupt status reset register

IT0_IIR: C002_0024H

31	30	29	28	27	26	25	24
0	0	IIR_61	IIR_60	IIR_59	IIR_58	IIR_57	IIR_56
23	22	21	20	19	18	17	16
IIR_55	IIR_54	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	IIR_46	IIR_45	IIR_44	IIR_43	0	0	0
7	6	5	4	3	2	1	0
IIR_39	0	0	IIR_36	IIR_35	IIR_34	IIR_33	0

Name	R/W	Bit	After Reset	Function
IIR_**	W	31:0	0	The IIR_xx bits correspond to INTxx. 1: Clears the interrupt source status (RAW/MST). 0: No operation

(2) ADSP interrupt status reset register

IT3_IIR: C002_C024H

31	30	29	28	27	26	25	24
0	0	IIR_61	IIR_60	IIR_59	IIR_58	IIR_57	IIR_56
23	22	21	20	19	18	17	16
IIR_55	IIR_54	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	IIR_46	IIR_45	IIR_44	IIR_43	0	0	0
7	6	5	4	3	2	1	0
IIR_39	0	0	IIR_36	IIR_35	IIR_34	IIR_33	0

Name	R/W	Bit	After Reset	Function
IIR_**	W	31:0	0	The IIR_xx bits correspond to INTxx. 1: Clears the interrupt source status (RAW/MST). 0: No operation

F.1.4 Interprocessor communication registers

The following lists the registers for interprocessor communication.

(1) ACPU-to-ADSP interprocessor communication set register

IT0_IPI3_SET: C002_003CH

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		S03_5	S03_4	S03_3	S03_2	S03_1	S03_0

Name	R/W	Bit	After Reset	Function
Reserved	R	31:6	–	Fix these bits to 0.
S03_*	W	5:0	0	Sends messages from the ACPU to ADSP by using S03_[5:0]. 1: Sets the S03_[5:0] bits to 1. 0: No operation
S03_*	R	5:0	0	Can be used to read the status of a message reported from the ACPU to the ADSP.

(2) ADSP-to-ACPU interprocessor communication clear register

IT3_IPI0_CLR: C002_005CH

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		C03_5	C03_4	C03_3	C03_2	C03_1	C03_0

Name	R/W	Bit	After Reset	Function
Reserved	R	31:6	–	Fix these bits to 0.
C03_*	W	5:0	0	Clears the C03_[5:0] bits. 1: Clears the C03_[5:0] bits to 0. 0: No operation

(3) ADSP-to-ACPU interprocessor communication set register

IT3_IPI0_SET: C002_C030H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		S30_5	S30_4	S30_3	S30_2	S30_1	S30_0

Name	R/W	Bit	After Reset	Function
Reserved	R	31:6	–	Fix these bits to 0.
S30_*	W	5:0	0	Sends messages from the ADSP to ACPU by using S30_[5:0]. 1: Sets the S30_[5:0] bits to 1. 0: No operation
S30_*	R	5:0	0	Can be used to read the status of a message reported from the ADSP to the ACPU.

(4) ACPU-to-ADSP interprocessor communication clear register

IT0_IPI3_CLR: C002_C050H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		C30_5	C30_4	C30_3	C30_2	C30_1	C30_0

Name	R/W	Bit	After Reset	Function
Reserved	R	31:6	–	Fix these bits to 0.
C30_*	W	5:0	0	Clears the C30_[5:0] bits. 1: Clears the C30_[5:0] bits to 0. 0: No operation

F.1.5 FIQ interrupt mask registers (for ACPU only)

Two registers, the ACPU FIQ interrupt enable register (IT0_FIE) and the ACPU FIQ interrupt disable register (IT0_FID), are available for setting FIQ interrupt signals for the ACPU. The FIQ interrupt enable status can be checked by reading the interrupt enable register.

FIQ interrupts and IRQ interrupts occur independently. An IRQ interrupt signal can be asserted while an FIQ interrupt signal has been asserted, and vice versa.

<1> ACPU (address offset: C002_xxxxH)

IT0_FIE: ACPU FIQ interrupt enable register

IT0_FID: ACPU FIQ interrupt disable register

(1) ACPU FIQ interrupt enable register

IT0_FIE: C002_0080H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							FIQ_EN

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	–	Fix these bits to 0.
FIQ_EN	W	0	0	Enables FIQ interrupts. 1: Enables interrupts. 0: No operation
FIQ_EN	R	0	0	Indicates whether FIQ interrupts are enabled. 1: Enabled. 0: Disabled.

(2) ACPU FIQ interrupt disable register

IT0_FID: C002_0084H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							FIQ_DS

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	–	Fix these bits to 0.
FIQ_DS	W	0	0	Disables FIQ interrupts. 1: Disables interrupts. 0: No operation

F.1.6 Interrupt vector address register (for ACPU only)

The interrupt vector base address register (ID_VBS: C090H) sets the vector address to which execution jumps when an interrupt occurs in the ADSP. Bits 31 to 16 and bits 1 and 0 are fixed to “0”, so setting is not available. This setting is input to the ADSP via the INTVEC[31:1] signals.

The available setting range is 0000_0000H to 0000_FFFCH. Since the lower 2 bits are fixed to “0”, only an address on a 4-byte boundary can be set.

(1) Interrupt vector base address register

ID_VBS: C002_C090H

31	30	29	28	27	26	25	24
0							
23	22	21	20	19	18	17	16
0							
15	14	13	12	11	10	9	8
IB_15	IB_14	IB_13	IB_12	IB_11	IB_10	IB_9	IB_8
7	6	5	4	3	2	1	0
IB_7	IB_6	IB_5	IB_4	IB_3	IB_2	0	0

Name	R/W	Bit	After Reset	Function
IB_[15:2]	R/W	15:2	0	Sets the vector address to which execution jumps when an interrupt occurs in the aDSP.
0	R	1:0	0	Fix these bits to 0.

Table F-1 lists the correspondence between the IB_[15:0] bits of the ID_VBS register and the INTVEC[15:1] signals.

Bits [31:16] of the ID_VBS register and the INTVEC[31:16] signals (higher 16 bits) are omitted because they are fixed to “0”.

Table F-1. Vector Address Set Values

Set Value	ID_VBS Register [15:0]	INTVEC[15:1]
0000H	0000_0000_0000_0000B	0000_0000_0000_000B
0004H	0000_0000_0000_0100B	0000_0000_0000_010B
0008H	0000_0000_0000_1000B	0000_0000_0000_100B
000CH	0000_0000_0000_1100B	0000_0000_0000_110B
0010H	0000_0000_0001_0000B	0000_0000_0001_000B
:	:	:
0800H	0000_1000_0000_0000B	0000_1000_0000_000B
:	:	:
FFF0H	1111_1111_1111_0000B	1111_1111_1111_000B
FFF4H	1111_1111_1111_0100B	1111_1111_1111_010B
FFF8H	1111_1111_1111_1000B	1111_1111_1111_100B
FFFCH	1111_1111_1111_1100B	1111_1111_1111_110B

F.1.7 Interrupt output signal clear register

The interrupt output signal clear register (ID_CLR: C094H) is used to deassert (make inactive) the interrupt output signals from the ADSP (ADSP_INTP).

(1) Interrupt output signal clear register

ID_CLR: C002_C094H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							IC_D

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	–	Fix these bits to 0.
IC_D	W	0	0	Deasserts the interrupt output signals from the ADSP (ADSP_INTP). 0: No operation 1: Deasserts ADSP_INTP. (After that, this bit is automatically cleared to “0”.)

F.1.8 Interrupt input polarity registers

The following registers are available for setting the interrupt input polarity inversion.

<1> Common (address offset: C002_xxxxH)

IT_PINV_SET0/1/2: Interrupt input polarity inversion enable set register (Enables polarity inversion)

IT_PINV_CLR0/1/2: Interrupt input polarity inversion disable set register (Disables polarity inversion)

Set polarity inversion by using the above two types of registers (SET/CLR). To enable or disable polarity inversion, set the relevant bit to “1”.

(1) Interrupt input polarity inversion enable set register 0

IT_PINV_SET0: C002_0300H

31	30	29	28	27	26	25	24
PINV_SET_[31:24]							
23	22	21	20	19	18	17	16
PINV_SET_[23:16]							
15	14	13	12	11	10	9	8
PINV_SET_[15:8]							
7	6	5	4	3	2	1	0
PINV_SET_[7:0]							

Name	R/W	Bit	After Reset	Function
PINV_SET_**	W	31:0	0	PINV_SET_[31:0] bits correspond to INT[31:0]. 1: Inverts the polarity of the corresponding interrupts. 0: No operation
PINV_SET_**	R	31:0	0	Indicates the interrupt signal polarity inversion status. 1: Polarity inverted 0: Polarity not inverted

Caution The reserved interrupt sources must always be disabled (default).

(2) Interrupt input polarity inversion enable set register 1

IT_PINV_SET1: C002_0304H

31	30	29	28	27	26	25	24
PINV_SET_[63:56]							
23	22	21	20	19	18	17	16
PINV_SET_[55:48]							
15	14	13	12	11	10	9	8
PINV_SET_[47:40]							
7	6	5	4	3	2	1	0
PINV_SET_[39:32]							

Name	R/W	Bit	After Reset	Function
PINV_SET_**	W	31:0	0	The PINV_SET_[63:32] bits correspond to INT[63:32]. 1: Inverts the polarity of the corresponding interrupts. 0: No operation
PINV_SET_**	R	31:0	0	Indicates the interrupt signal polarity inversion status. 1: Polarity inverted 0: Polarity not inverted

Caution The reserved interrupt sources must always be disabled (default).

(3) Interrupt input polarity inversion enable set register 2

IT_PINV_SET2: C002_0308H

31	30	29	28	27	26	25	24
PINV_SET_[95:88]							
23	22	21	20	19	18	17	16
PINV_SET_[87:80]							
15	14	13	12	11	10	9	8
PINV_SET_[79:72]							
7	6	5	4	3	2	1	0
PINV_SET_[71:64]							

Name	R/W	Bit	After Reset	Function
PINV_SET_**	W	31:0	0	The PINV_SET_[95:64] bits correspond to INT[95:64]. 1: Inverts the polarity of the corresponding interrupts. 0: No operation
PINV_SET_**	R	31:0	0	Indicates the interrupt signal polarity inversion status. 1: Polarity inverted 0: Polarity not inverted

Caution The reserved interrupt sources must always be disabled (default).

(4) Interrupt input polarity inversion disable set register 0

IT_PINV_CLR0: C002_0310H

31	30	29	28	27	26	25	24
PINV_CLR_[31:24]							
23	22	21	20	19	18	17	16
PINV_CLR_[23:16]							
15	14	13	12	11	10	9	8
PINV_CLR_[15:8]							
7	6	5	4	3	2	1	0
PINV_CLR_[7:0]							

Name	R/W	Bit	After Reset	Function
PINV_CLR_**	W	31:0	0	The PINV_CLR_[31:0] bits correspond to INT[31:0]. 1: Does not invert the polarity of the corresponding interrupts. 0: No operation

(5) Interrupt input polarity inversion disable set register 1

IT_PINV_CLR1: C002_0314H

31	30	29	28	27	26	25	24
PINV_CLR_[63:56]							
23	22	21	20	19	18	17	16
PINV_CLR_[55:48]							
15	14	13	12	11	10	9	8
PINV_CLR_[47:40]							
7	6	5	4	3	2	1	0
PINV_CLR_[39:32]							

Name	R/W	Bit	After Reset	Function
PINV_CLR_**	W	31:0	0	The PINV_CLR_[63:32] bits correspond to INT[63:32]. 1: Does not invert the polarity of the corresponding interrupts. 0: No operation

(6) Interrupt input polarity inversion disable set register 2

IT_PINV_CLR2: C002_0318H

31	30	29	28	27	26	25	24
PINV_CLR_[95:88]							
23	22	21	20	19	18	17	16
PINV_CLR_[87:80]							
15	14	13	12	11	10	9	8
PINV_CLR_[79:72]							
7	6	5	4	3	2	1	0
PINV_CLR_[71:64]							

Name	R/W	Bit	After Reset	Function
PINV_CLR_**	W	31:0	0	The PINV_CLR_[95:64] bits correspond to INT[95:64]. 1: Does not invert the polarity of the corresponding interrupts. 0: No operation

Remark This register is invalid for INT81 to INT84 (assigned to interrupt status set/reset registers).

F.1.9 Internal interrupt status set registers

The following registers sets or clears the interrupt status in AINT, in 1-bit units. An interrupt signal is issued to a processor by setting the set register, and the interrupt signal is cleared by setting the reset register. LIIS0 to LIIS3 of these registers correspond to AINT interrupts INT81 to INT84. This register is commonly used by processors.

(1) Internal interrupt status set register

IT_LIIS: C002_0320H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				IT_LIIS[3:0]			

Name	R/W	Bit	After Reset	Function
IT_LIIS*	W	3:0	0	Sets an AINT interrupt signal. 1: Sets an interrupt signal. 0: No operation

(2) Internal interrupt status reset register

IT_LIIR: C002_0324H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				IT_LIIR[3:0]			

Name	R/W	Bit	After Reset	Function
IT_LIIR*	W	3:0	0	Clears an AINT interrupt signal 1: Clears an interrupt signal. 0: No operation

F.1.10 ACPU secure interrupt mask registers

By using the registers described in this section, ACPU interrupt output (PMU_IRQ0Z), ACPU interrupt raw statuses (shown in IT0_RAW[2:0]) can be masked, as well as ACPU interrupt mask statuses (shown in IT0_MST[2:0]). The following registers are available for setting ACPU secure interrupt masking.

<1> MSE (address offset: CC01_xxxxH)

IT0_IENS0/1/2: ACPU secure interrupt enable setting register (mask cancel)

IT0_IDSS0/1/2: ACPU secure interrupt disable setting register (mask setting)

Caution The interrupt mask status can be checked by reading IT0_IENSx. The disable settings made with IT0_IDSSx are reflected to the corresponding bits of the IT0_IENSx register.

Set interrupts by using the above two types of registers (IENS/IDSS). To enable or disable an interrupt source, set the relevant bit to “1”.

Example The execution result varies depending on the order of writing to the registers.

Set IT0_IENS0 to 0101_0101 → Enables interrupts corresponding to bits 6, 4, 2 and 0 are set.

Set IT0_IDSS0 to 0001_0001 → Disables interrupts corresponding to bits 4 and 0.

Read IT0_IENS0 = 0100_0100 → Interrupts corresponding to bits 6 and 2 remain enabled.

When interrupts are disabled in these registers (reset values are applied), the raw status signal, mask status signal, clock start signal (PE0START), and interrupt output signals (PMU_IRQ0Z) are not asserted.

Figure F-1. Interrupt Signal Control (for Level Detection Interrupts)

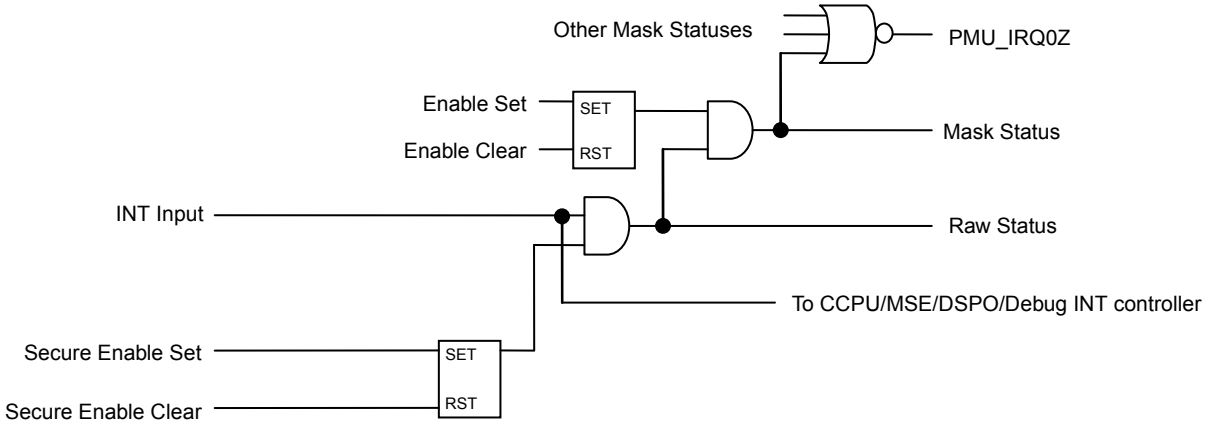
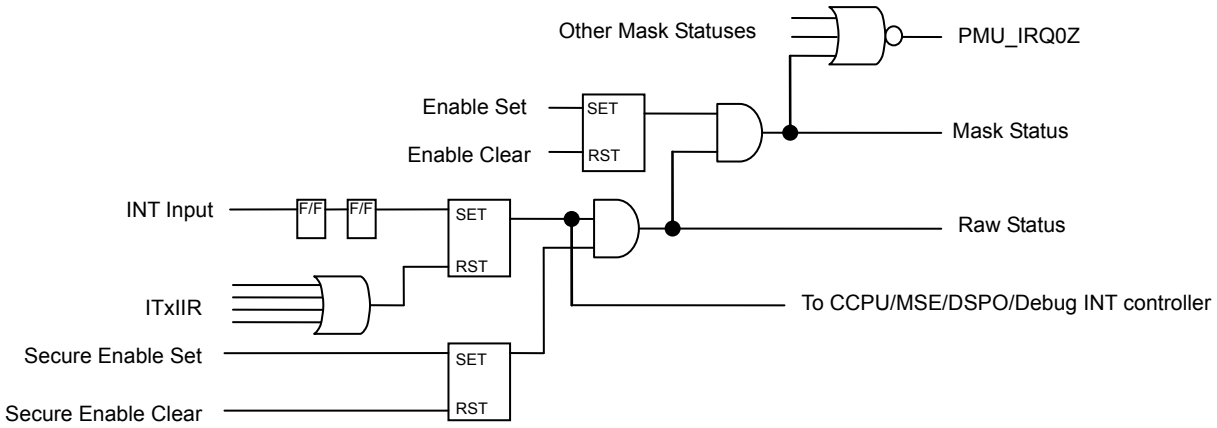


Figure F-2. Interrupt Signal Control (for Edge Detection Interrupts)



(1) ACPU secure interrupt enable setting register 0

IT0_IENS0: CC01_E200H

31	30	29	28	27	26	25	24
IENS_[31:24]							
23	22	21	20	19	18	17	16
IENS_[23:16]							
15	14	13	12	11	10	9	8
IENS_[15:8]							
7	6	5	4	3	2	1	0
IENS_[7:0]							

Name	R/W	Bit	After Reset	Function
IENS_**	W	31:0	0	The IENS_[31:0] bits correspond to INT[31:0]. 1: Enables interrupts (cancels interrupt masking). 0: No operation
IENS_**	R	31:0	0	Indicates the interrupt enable status. 1: Interrupts enabled. 0: Interrupts disabled.

(2) ACPU secure interrupt enable setting register 1

IT0_IENS1: CC01_E204H

31	30	29	28	27	26	25	24
IENS_[63:56]							
23	22	21	20	19	18	17	16
IENS_[55:48]							
15	14	13	12	11	10	9	8
IENS_[47:40]							
7	6	5	4	3	2	1	0
IENS_[39:32]							

Name	R/W	Bit	After Reset	Function
IENS_**	W	31:0	0	The IENS_[63:32] bits correspond to INT[63:32]. 1: Enables interrupts (cancels interrupt masking). 0: No operation
IENS_**	R	31:0	0	Indicates the interrupt enable status. 1: Interrupts enabled. 0: Interrupts disabled.

(3) ACPU secure interrupt enable setting register 2

IT0_IENS2: CC01_E208H

31	30	29	28	27	26	25	24
IENS_[95:88]							
23	22	21	20	19	18	17	16
IENS_[87:80]							
15	14	13	12	11	10	9	8
IENS_[79:72]							
7	6	5	4	3	2	1	0
IENS_[71:64]							

Name	R/W	Bit	After Reset	Function
IENS_**	W	31:0	0	The IENS_[95:64] bits correspond to INT[95:64]. 1: Enables interrupts (cancels interrupt masking). 0: No operation
IENS_**	R	31:0	0	Indicates the interrupt enable status. 1: Interrupts enabled. 0: Interrupts disabled.

(4) ACPU secure interrupt disable setting register 0

IT0_IDSS0: CC01_E20CH

31	30	29	28	27	26	25	24
IDSS_[31:24]							
23	22	21	20	19	18	17	16
IDSS_[23:16]							
15	14	13	12	11	10	9	8
IDSS_[15:8]							
7	6	5	4	3	2	1	0
IDSS_[7:0]							

Name	R/W	Bit	After Reset	Function
IDSS_**	W	31:0	0	The IDSS_[31:0] bits correspond to INT[31:0]. 1: Disables interrupts (mask setting). 0: No operation

(5) ACPU secure interrupt disable setting register 1

IT0_IDSS1: CC01_E210H

31	30	29	28	27	26	25	24
IDSS_[63:56]							
23	22	21	20	19	18	17	16
IDSS_[55:48]							
15	14	13	12	11	10	9	8
IDSS_[47:40]							
7	6	5	4	3	2	1	0
IDSS_[39:32]							

Name	R/W	Bit	After Reset	Function
IDSS_**	W	31:0	0	The IDSS_[63:32] bits correspond to INT[63:32]. 1: Disables interrupts (mask setting). 0: No operation

(6) ACPU secure interrupt disable setting register 2

IT0_IDSS2: CC01_E214H

31	30	29	28	27	26	25	24
IDSS_[95:88]							
23	22	21	20	19	18	17	16
IDSS_[87:80]							
15	14	13	12	11	10	9	8
IDSS_[79:72]							
7	6	5	4	3	2	1	0
IDSS_[71:64]							

Name	R/W	Bit	After Reset	Function
IDSS_**	W	31:0	0	The IDSS_[95:64] bits correspond to INT[95:64]. 1: Disables interrupts (mask setting). 0: No operation

F.2 How to Control AINT

F.2.1 Interprocessor communication processing example

Interprocessor communication refers to the operation that reports messages between processors (ACPU and ADSP), via a 6-bit buffer. (Sending of messages causes interrupt for the receiver processor.)

The following shows an example of ACPU-to-ADSP interprocessor communication that involves an IRQ interrupt.

Setting of ACPU:

None.

Setting of ADSP:

○ IT0_IPI1_CLR: ACPU-to-ADSP interprocessor communication clear

- Writing 0000_003FH clears the IT0_IPI1_MON register.

○ IT0_IPI1_CLR: ACPU-to-ADSP interprocessor communication clear

- IT1_IEN0: Interrupt enable register
- Writing 0000_0001H enables interrupt caused by communication from the ACPU.

Addresses seen from the message sender side

	Communication	Set Register	Monitor Register	Address	Clear Register	Address
ACPU	ACPU → ADSP	IT0_IPI1_SET	IT0_IPI1_MON	00_34H	IT0_IPI1_CLR	40_50H
ADSP	ADSP → ACPU	IT1_IPI0_SET	IT1_IPI0_MON	40_30H	IT1_IPI0_CLR	00_54H

Addresses seen from the message receiver side

	Communication	Clear Register	Address	Set Register	Monitor Register	Address
ACPU	ADSP → ACPU	IT1_IPI0_CLR	00_54H	IT1_IPI0_SET	IT1_IPI0_MON	40_30H
ADSP	ACPU → ADSP	IT0_IPI1_CLR	40_50H	IT0_IPI1_SET	IT0_IPI1_MON	00_34H

The following registers are available for setting interrupt sources and showing the interrupt source statuses.

- ITx_RAW0: Interrupt raw status register 0
- ITx_MST0: Interrupt maskable status register 0

APPENDIX G SRC/INTERNAL SRAM

G.1 Overview

This module consists of a 128 KB on-chip single-port SRAM and an SRAM controller (SRC).

The SRC is a controller used for accessing SRAM via internal buses. Mapping frequently-accessed areas to SRAM enables high-speed (lower latency than DRAM because of 64-bit AXI connection) and low-power (lower power consumed than DRAM because I/O ports are not driven and no refresh is required) operations.

G.1.1 Function overview

- ○ Conforms to ARM AXI protocol.
- ○ Conforms to AMBA system bus architecture (Rev. 3.0).
- ○ Operates at 166 MHz max.
- ○ Requests clock via SRC_CLKREQ signal.

G.1.2 Address map

SRAM memory spaces are allocated to A000_0000H to A001_FFFFH.

G.1.3 Slave interface (AXI)

This module has a 64-bit AXI slave interface.

SWT	Connected Master
AXL0, AXL1	ACPU, ADSP, DHXB (IMC, DMA), MHXB (DMA, IPU, AVC), SHXB (NAND, DTV, NTS)

The slave interface conforms to the AMBA AXI specifications.

APPENDIX H ADSP ADDRESS CONVERTER (DCV)

H.1 ADSP Address Converter (DCV)

H.1.1 Overview

DCV is an address converter that converts the AXI bus address map in a DSP core (DSPK701) into that of EM1-D512.

- ○ Address translation

  DCV has an address conversion function that is used to map physical addresses to the DSP cacheable area, bufferable area, and unbufferable area. Conversion BANK and offset setting for each bank is possible.
- ○ AXI transactions from the corresponding ADSP

  32-bit single read/write

  16-bit single read/write

  8-bit single read/write

  64-bit INCR8 read/write
- ○ DCV does not perform processing for BUSERR, NMIACKP, and NMIP.
- ○ If EXOKAY, SLVERR, or DECERR is returned via a response signal (RRESP, BRESP) from the read data channel or write response channel, DVC reports an interrupt occurrence to the ACPU and stores information of the ID and response signal.
- ○ The APB interface block operates at 83 MHz, and the address translation block operates at 166 MHz. Use a synchronous clock for these blocks. The clock frequency ratio of the APB interface block and address translation block is 1:2. If another ratio is used, an interrupt source may not be retained correctly if the interrupt source occurs at the same time as an interrupt is cleared.

Caution Switching bank/offset parameters dynamically is not recommended.

H.1.2 Register functions

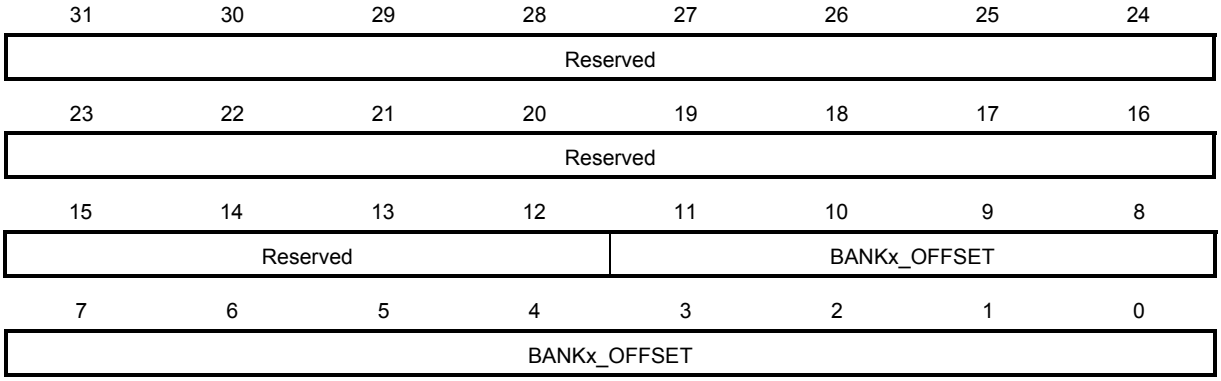
(1) Offset setting registers

For details on address translation, see **H.1.3 Address translation processing**.

Table H-1. BANKx_OFFSET Registers

Address	Register Name	Register Symbol	R/W	After Reset
C00D_0000H	DSP-bank 0 corresponding offset setting register	DCV_BANK0_OFFSET	R/W	0000_0200H
C00D_0004H	DSP-bank 1 corresponding offset setting register	DCV_BANK1_OFFSET	R/W	0000_0000H
C00D_0008H	DSP-bank 2 corresponding offset setting register	DCV_BANK2_OFFSET	R/W	0000_0000H
C00D_000CH	DSP-bank 3 corresponding offset setting register	DCV_BANK3_OFFSET	R/W	0000_0000H
C00D_0010H	DSP-bank 4 corresponding offset setting register	DCV_BANK4_OFFSET	R/W	0000_0100H
C00D_0014H	DSP-bank 5 corresponding offset setting register	DCV_BANK5_OFFSET	R/W	0000_0000H
C00D_0018H	DSP-bank 6 corresponding offset setting register	DCV_BANK6_OFFSET	R/W	0000_0000H
C00D_001CH	DSP-bank 7 corresponding offset setting register	DCV_BANK7_OFFSET	R/W	0000_0000H
C00D_0020H	DSP-bank 8 corresponding offset setting register	DCV_BANK8_OFFSET	R/W	0000_0240H
C00D_0024H	DSP-bank 9 corresponding offset setting register	DCV_BANK9_OFFSET	R/W	0000_0000H
C00D_0028H	DSP-bank 10 corresponding offset setting register	DCV_BANK10_OFFSET	R/W	0000_0000H
C00D_002CH	DSP-bank 11 corresponding offset setting register	DCV_BANK11_OFFSET	R/W	0000_0000H
C00D_0030H	DSP-bank 12 corresponding offset setting register	DCV_BANK12_OFFSET	R/W	0000_0000H
C00D_0034H	DSP-bank 13 corresponding offset setting register	DCV_BANK13_OFFSET	R/W	0000_0000H
C00D_0038H	DSP-bank 14 corresponding offset setting register	DCV_BANK14_OFFSET	R/W	0000_0000H
C00D_003CH	DSP-bank 15 corresponding offset setting register	DCV_BANK15_OFFSET	R/W	0000_0000H

Caution Switching bank/offset parameters dynamically is not recommended.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:12	0H	Reserved. When these bits are read, 0 is returned for each bit.
BANKx_OFFSET	R/W	11:0	**Note**	BANKx offset setting

Remark x = 0 to 15

Note See **Table H-1** for the reset values.

(2) BANK setting registers

For details on address translation, see **H.1.3 Address translation processing**.

○ DCV_BANKx_SET

These registers set the banks to make them correspond to DSP-BANKx.

Table H-2. BANKx_SET Registers

Address	Register Name	Register Symbol	R/W	After Reset
C00D_0040H	DSP-bank 0 correspondence setting register	DCV_BANK0_SET	R/W	0000_0003H
C00D_0044H	DSP-bank 1 correspondence setting register	DCV_BANK1_SET	R/W	0000_0000H
C00D_0048H	DSP-bank 2 correspondence setting register	DCV_BANK2_SET	R/W	0000_0000H
C00D_004CH	DSP-bank 3 correspondence setting register	DCV_BANK3_SET	R/W	0000_0000H
C00D_0050H	DSP-bank 4 correspondence setting register	DCV_BANK4_SET	R/W	0000_0003H
C00D_0054H	DSP-bank 5 correspondence setting register	DCV_BANK5_SET	R/W	0000_0000H
C00D_0058H	DSP-bank 6 correspondence setting register	DCV_BANK6_SET	R/W	0000_0000H
C00D_005CH	DSP-bank 7 correspondence setting register	DCV_BANK7_SET	R/W	0000_0000H
C00D_0060H	DSP-bank 8 correspondence setting register	DCV_BANK8_SET	R/W	0000_0003H
C00D_0064H	DSP-bank 9 correspondence setting register	DCV_BANK9_SET	R/W	0000_0000H
C00D_0068H	DSP-bank 10 correspondence setting register	DCV_BANK10_SET	R/W	0000_0000H
C00D_006CH	DSP-bank 11 correspondence setting register	DCV_BANK11_SET	R/W	0000_0000H
C00D_0070H	DSP-bank 12 correspondence setting register	DCV_BANK12_SET	R/W	0000_0004H
C00D_0074H	DSP-bank 13 correspondence setting register	DCV_BANK13_SET	R/W	0000_000CH
C00D_0078H	DSP-bank 14 correspondence setting register	DCV_BANK14_SET	R/W	0000_000AH
C00D_007CH	DSP-bank 15 correspondence setting register	DCV_BANK15_SET	R/W	0000_0000H

Caution Switching bank/offset parameters dynamically is not recommended.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				BANKx_SET			

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0H	Reserved. When these bits are read, 0 is returned for each bit.
BANKx_SET	R/W	3:0	**Note**	Setting of banks that correspond to DSP-bank x

Remark x = 0 to 15

Note See **Table H-2** for the reset values.

(3) Interrupt status register

DCV_INTSTATUS: C00D_0080H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							DCV_INTSTATUS

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	–	Reserved. When these bits are read, 0 is returned for each bit.
DCV_INTSTSTUS	R	0	0	Indicates the interrupt status. Indicates the status of interrupt sources enabled (mask cancelled). Value 0 is read from the bits corresponding to the interrupt sources disabled (masked).

(4) Interrupt raw status register

DCV_INTRAWSTATUS: C00D_0084H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							DCV_INTRAWSTATUS

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	–	Reserved. When these bits are read, 0 is returned for each bit.
DCV_INTRAWSTSTUS	R	0	0	Indicates the interrupt raw status. Indicates the status of interrupt sources regardless of the interrupt enable/disable settings.

(5) Interrupt enable set register

DCV_INTENSET: C00D_0088H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							DCV_INTENSET

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	–	Reserved. When these bits are read, 0 is returned for each bit.
DCV_INTENSET	R/W	0	0	Enables interrupt sources. Writing 1 to this bit enables (cancels masking) the interrupt sources corresponding to the bit.

(6) Interrupt enable clear register

DCV_INTENCLR: C00D_008CH

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							DCV_INTENCLR

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	–	Reserved. When these bits are read, 0 is returned for each bit.
DCV_INTENCLR	W	0	0	Disables interrupt sources. Writing 1 to this bit disables (masks interrupts) the interrupt sources corresponding to the bit.

(7) Interrupt source clear register

DCV_INTFFCLR: C00D_0090H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							DCV_INTFFCLR

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	–	Reserved. When these bits are read, 0 is returned for each bit.
DCV_INTFFCLR	W	0	0	Clears interrupt sources. Writing 1 to this bit clears the interrupt source corresponding to the bit.

If setting and clearing of an interrupt source are performed at the same time, setting takes precedence.

(8) Interrupt information register

DCV_INTINFO: C00D_0094H

31	30	29	28	27	26	25	24
CLEAR	Reserved						
23	22	21	20	19	18	17	16
Reserved		ERR_DBRESP		ERR_DBID			
15	14	13	12	11	10	9	8
Reserved		ERR_DRRESP		ERR_DRID			
7	6	5	4	3	2	1	0
Reserved		ERR_IRRESP		ERR_IRID			

Name	R/W	Bit	After Reset	Function
CLEAR	W	31	0	Writing 1 clears error information stored in this register. When this bit is read, 0 is returned.
Reserved	R	30:22	–	Reserved. When these bits are read, 0 is returned for each bit.
ERR_DBRESP	R	21:20	0	Indicates RESP information upon an error occurrence in the Data Write data back channel.
ERR_DBID	R	19:16	0	Indicates ID information upon an error occurrence in the Data Write data back channel.
Reserved	R	15:14	–	Reserved. When these bits are read, 0 is returned for each bit.
ERR_DRRESP	R	13:12	0	Indicates RESP information upon an error occurrence in the Data Read data channel.
ERR_DRID	R	11:8	0	Indicates ID information upon an error occurrence in the Data Read data channel.
Reserved	R	7:6	–	Reserved. When these bits are read, 0 is returned for each bit.
ERR_IRRESP	R	5:4	0	Indicates RESP information upon an error occurrence in the Instruction Read data channel.
ERR_IRID	R	3:0	0	Indicates ID information upon an error occurrence in the Instruction Read data channel.

When the RESP signal sent from the IR (instruction read), DR (data read) or DB (data write data back) channel is other than OKAY (EXOKAY, SLVERR, or DECERR), RESP and ID information is stored in this register. This register only stores the information of the error that has occurred first in each of the IR, DR, and DB channels. When the RESP signals indicating an error status are returned from the IR, DR and DB channels at the same time, information on multiple errors is retained.

Writing 1 to the CLEAR bit clears this register.

H.1.3 Address translation processing

DVC performs address translation to make the address accessed from the DSP match the address on EM1-D512 memory map, as shown in Figure H-1.

(1) Higher 4 bits (BANK): When accessed from the DSP, the higher 4 bits are translated into the corresponding bank address, according to the setting in the DCV_BANKxx_SET register.

(2) Middle 12 bits (bits 27:16)
When accessed from the DSP, the offset value corresponding to the higher 4 bits (DSP bank address) (values set to each DCV_BANKxx_OFFSET register) is added to the middle 12 bits.

(3) Lower 16 bits: The lower 16 bits are output to the system bus as is.

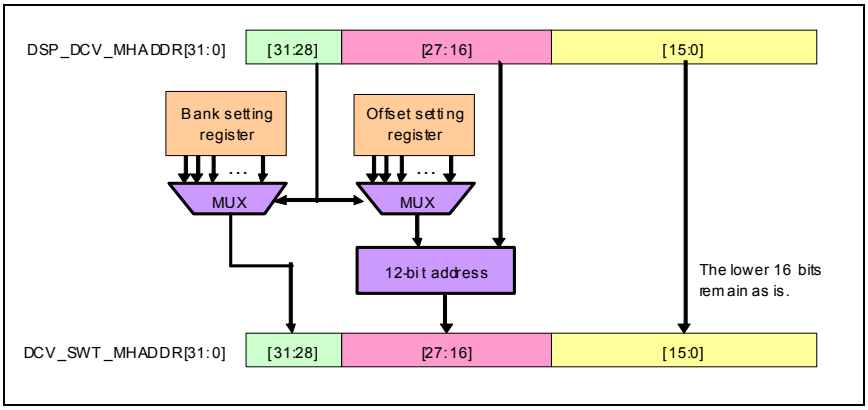
Example When DSP_DCV_MHADDR [31:0] are set to 0000_0000H (default setting)

(1) Since the higher 4 bits are 0H (DSP bank 0), they are translated into the bank address set by DCV_BANK0_SET. It is 3H (BANK3) by default.

(2) Middle 12 bits
Since the higher 4 bits are set to 0H (DSP bank 0), the offset value (200H by default) set by the DCV_BANK0_OFFSET register is added.
Here, the middle 12 bits are 000H, so 000H + 200H = 200H is set.

(3) The lower 16 bits remain as is, so DCV_SWT_MHADDR[31:0] are set to 3200_0000H.

Figure H-1. Address Translation



Cautions 1. Switching bank/offset parameters dynamically is not recommended. If parameters are switched dynamically, the operation is not performed correctly during ADSP debugging.

2. If the result of the addition of "DSP_DCV_MHADDR[27:16] + OFFSET_ADDR" exceeds FFFH (overflow), the carry is ignored when an overflow occurs and the DSP cruises the corresponding bank from the top.

Figure H-2. Address Translation Overflow Operation

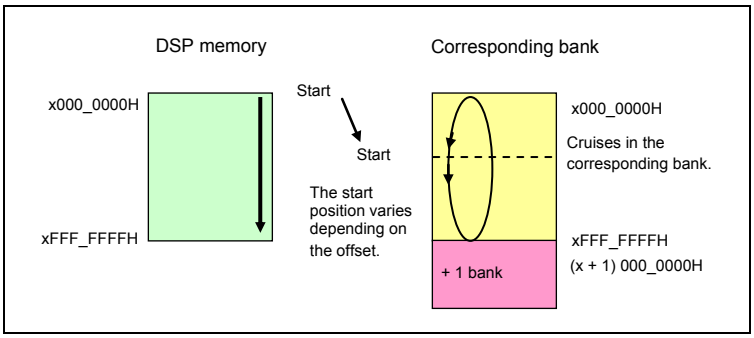


Table H-3. Address Translation Table

DSP Memory Bank	Memory Bank		Offset Value		Memory Map
	Default Value	Setting Register	Default Value	Setting Register	Default setting
DSP-Bank0	BANK3	DCV_BANK0_SET	200H	DCV_BANK0_OFFSET	3200_0000H
DSP-Bank1	BANK0	DCV_BANK1_SET	0H	DCV_BANK1_OFFSET	0000_0000H
DSP-Bank2	BANK0	DCV_BANK2_SET	0H	DCV_BANK2_OFFSET	0000_0000H
DSP-Bank3	BANK0	DCV_BANK3_SET	0H	DCV_BANK3_OFFSET	0000_0000H
DSP-Bank4	BANK3	DCV_BANK4_SET	100H	DCV_BANK4_OFFSET	3100_0000H
DSP-Bank5	BANK0	DCV_BANK5_SET	0H	DCV_BANK5_OFFSET	0000_0000H
DSP-Bank6	BANK0	DCV_BANK6_SET	0H	DCV_BANK6_OFFSET	0000_0000H
DSP-Bank7	BANK0	DCV_BANK7_SET	0H	DCV_BANK7_OFFSET	0000_0000H
DSP-Bank8	BANK3	DCV_BANK8_SET	240H	DCV_BANK8_OFFSET	3240_0000H
DSP-Bank9	BANK0	DCV_BANK9_SET	0H	DCV_BANK9_OFFSET	0000_0000H
DSP-Bank10	BANK0	DCV_BANK10_SET	0H	DCV_BANK10_OFFSET	0000_0000H
DSP-Bank11	BANK0	DCV_BANK11_SET	0H	DCV_BANK11_OFFSET	0000_0000H
DSP-Bank12	BANK4	DCV_BANK12_SET	0H	DCV_BANK12_OFFSET	4000_0000H
DSP-Bank13	BANK12	DCV_BANK13_SET	0H	DCV_BANK13_OFFSET	C000_0000H
DSP-Bank14	BANK10	DCV_BANK14_SET	0H	DCV_BANK14_OFFSET	A000_0000H
DSP-Bank15	BANK0	DCV_BANK15_SET	0H	DCV_BANK15_OFFSET	0000_0000H

Caution Change the setting of each value before use.

H.1.4 Reset

DCV uses synchronous reset. To initialize DCV, input a reset for at least five cycles of DCV_HCLK and DCV_PCLK.

APPENDIX I PMU

I.1 PMU (Power ON/OFF Control Sequence)

I.1.1 General

The PMU is a module that controls the power supply for the logic block of EM1-D512 (excluding ADSP) and switches the clock in place of the ACPU. Some control operations are performed by the ASMU. The power supply is controlled by the PMU using commands so to enable flexible handling of various situations related to peripheral devices or the power save mode.

I.1.2 Function overview

- The operating mode can be switched to LCD direct mode by the ACPU during Normal mode.
- Serves as an APB master while the power of the ACPU is off, and controls the power supply.
- Reads and writes various registers as an APB master.
- Detects interrupts upon command fetch while serving as a master. If an interrupt is detected, the operation automatically transits to the power-on sequence.
- Controls the clock to reduce power consumption in the PMU.
- Incorporates a WDT (32.768 kHz, 18 bits), and outputs a system reset request signal to the external power supply LSI upon occurrence of a timeout.

I.1.3 WDT control and reset request

The PMU judges errors using the WDT to prevent deadlock if an error occurs. When an error occurs (that is, the WDT count reaches the specified limit value), the PMU requests the ASMU to reset the entire EM1-D512 block.

The WDT_COUNT_EN register setting needs to be enabled to control the WDT; otherwise, the WDT does not operate.

The WDT-based control functions only when the PMU starts operating. Because the WDT count is cleared when the PMU starts or stops, counting starts after the clear operation has been completed. The output of reset requests from the PMU is masked while PMU_START is disabled, or the WDT count clear operation has not been completed (while a clear request is being issued).

I.1.4 Transition to power-on sequence by interrupt signal

(1) Transition to power-on sequence during Normal mode

When the PMU is operating, the PMU judges whether an interrupt input (INT_IRQ0Z_PMU or INT_FIQ0Z_PMU) is asserted when fetching a command from a command register. If either of the interrupt inputs is asserted, execution immediately jumps to the PC value set in the PMU_POWER_ON_PC register and power-on sequence is executed.

I.2 Registers

The PMU registers can only be accessed in 32-bit (word) units.

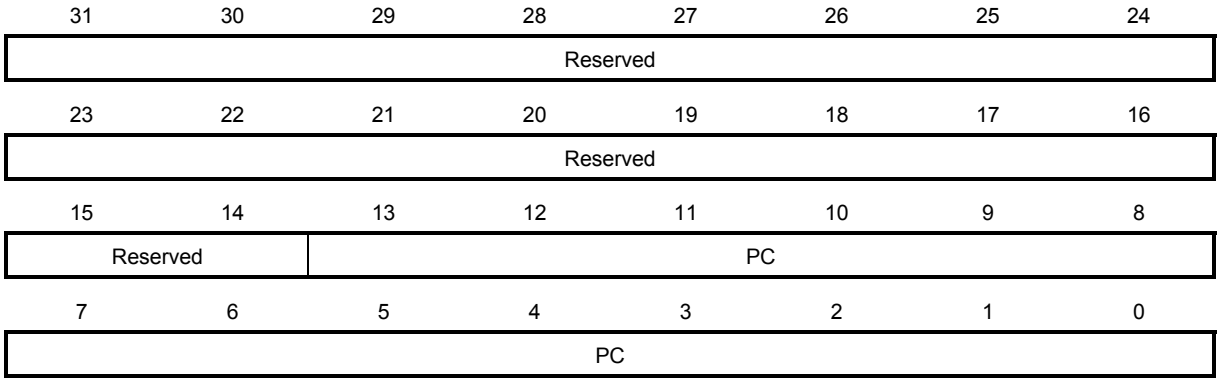
Base address: C010_0000H

Address	Register Name	Symbol	R/W	After Reset
0004H	Program counter (command RAM address) register	PMU_PC	R/W	0000_0000H
0008H	PMU start register	PMU_START	R/W	0000_0000H
0030H	Power-on sequence start PC register	PMU_POWER_ON_PC	R/W	0000_0000H
0060H	Watchdog timer count enable register	PMU_WDT_COUNT_EN	R/W	0000_0000H
0064H	Watchdog timer count limit register	PMU_WDT_COUNT_LMT	R/W	0003_FFFFH
0068H	Interrupt handler PC register	PMU_INT_HANDLER_PC	R/W	0000_0000H
0070H	Program status register	PMU_PSR	R	0000_0000H
0074H	TRIG_WAIT command status register	PMU_TRIG_STATUS	R	0000_0000H
0078H	General-purpose register A	PMU_REGA	R	0000_0000H
007CH	General-purpose register B	PMU_REGB	R	0000_0000H
0080H	ACPU interrupt status register	PMU_INTSTATUS_A	R	0000_0000H
0084H	ACPU interrupt raw status register	PMU_INTRAWSTATUS_A	R	0000_0000H
0088H	ACPU interrupt enable set register	PMU_INTENSET_A	R/W	0000_0000H
008CH	ACPU interrupt enable clear register	PMU_INTENCLR_A	W	0000_0000H
0090H	ACPU interrupt source clear register	PMU_INTFFCLR_A	W	0000_0000H
00A8H	PC error address register	PMU_PCERR	R/W	0000_0000H
1000H-1FFCH	Command buffer RAM register (1024 words from 1000H to 1FFCH)	PMU_CMD_BUF_RAM	R/W	–
2000H-203CH	Command buffer FF register (16 words from 2000H to 203CH)	PMU_CMD_BUF_FF	R/W	–

I.2.1 Register functions

(1) Program counter (command RAM address) register

PMU_PC: C010_0004H



Name	R/W	Bit	After Reset	Function
Reserved	R	31:14	–	Reserved. When these bits are read, 0 is returned for each bit. Writing is ignored.
PC	R/W	13:0	000H	Sets the program counter (command register address) of the command buffer. If the power-off sequence is entered by using the PMU_START command, execution starts from the command stored at the address set by this register. The command register addresses under processing are held while the PMU is operating. (It can be checked by using the debug monitor function).

Caution Be sure to set this register before starting the PMU by using PMU_START.

(2) PMU start register

PMU_START: C010_0008H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							PMU_START

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	–	Reserved. When these bits are read, 0 is returned for each bit. Writing is ignored.
PMU_START	R/W	0	0	0: PMU has been stopped 1: PMU has been started (operating) The PMU starts by setting this bit to 1. If WDT_COUNT_EN is enabled, the watchdog timer starts counting from 0. When the PMU starts, it issues PMUCLK_REQ first (requesting starts from the write clock cycle operation). Next, the PMU confirms that STANDBYWFI has been asserted. Interrupts input during this period are handled by the ACPU. Since the PMU is in the WFI (Wait for Interrupt) state during the servicing by the ACPU, read this register via the ACPU in the interrupt servicing sequence. If 1 is read, write 0 to stop the PMU. Interrupt signals INT_IRQ0Z and INT_FIQ0Z are masked in the PMU and are output to the ACPU from when WFI is detected until the PMU is stopped by the PMU_END command, or until the interrupt masking is released by the ARMINT_MASK command. The ACPU references the PMU_PC register and fetches commands from a command register, and operates according to the value. The conditions for terminating the operation are as follows. 1: Issuance of PMU_END command 2: When the WDT is counted up to the upper limit and a reset request is output (forced stop by reset)

(3) Power-on sequence start PC register

PMU_POWER_ON_PC: C010_0030H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		POWER_ON_PC					
7	6	5	4	3	2	1	0
POWER_ON_PC							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:14	–	Reserved. When these bits are read, 0 is returned for each bit. Writing is ignored.
POWER_ON_PC	R/W	13:0	000H	Sets the command register address at which the first command when the power-on sequence starts is stored. These bits are referenced when the power-on sequence is automatically entered by interrupt input.

Caution Be sure to set this register before starting the PMU by using PMU_START.

(4) Watchdog timer count enable register

PMU_WDT_COUNT_EN: C010_0060H

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							WDT_COUNT_EN

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	–	Reserved. When these bits are read, 0 is returned for each bit. Writing is ignored.
WDT_COUNT_EN	R/W	0	0	Sets whether to use the WDT while the PMU is operating. 0: Does not use the WDT (default) 1: Uses the WDT. If the PMU is started while this bit is set to 1, reset requests by the WDT are enabled. The WDT does not operate when this bit is set to 0.

Caution Be sure to set this register before starting the PMU by using PMU_START.

(5) Watchdog timer count limit register

PMU_WDT_COUNT_LMT: C010_0064H

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved						WDT_COUNT_LMT	

15	14	13	12	11	10	9	8
WDT_COUNT_LMT							

7	6	5	4	3	2	1	0
WDT_COUNT_LMT							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:18	–	Reserved. When these bits are read, 0 is returned for each bit. Writing is ignored.
WDT_COUNT_LMT	R/W	17:0	3_FFFFH	Sets the WDT count limit value while the PMU is operating. When WDT_COUNT_EN is set to 1, the WDT operating at 32.768 kHz starts counting from 0 by setting the PMU_START register to 1. When the WDT count reaches the same value as that specified by this register, the PMU asserts a signal for requesting reset of the entire EM1-D512 block. (This request signal is cancelled by reset.)

Caution Be sure to set this register before starting the PMU by using PMU_START.

Setting WDT_COUNT_LMT to 0 and changing the value during PMU operation are prohibited.

(6) Interrupt handler PC register

PMU_INT_HANDLER_PC: C010_0068H

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved		PMU_INT_HANDLER_PC					

7	6	5	4	3	2	1	0
PMU_INT_HANDLER_PC							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:14	–	Reserved. When these bits are read, 0 is returned for each bit. Writing is ignored.
PMU_INT_HANDLER_PC	R/W	13:0	000H	When the PMU issues an interrupt, the program counter jumps to the address set in this register. The PMU issues an interrupt when the PMU command PC points to an address outside the range of CMD_BUF_RAM and CMD_BUF_FF, or when a security error occurs.

Caution Be sure to set this register before starting the PMU by using PMU_START.

(7) Program status register

This register (PMU_PSR: C010_0070H) stores the result of an operation command executed in the PMU. The commands subject to storage are CMP1 and CMP2. If the comparison results in match, 1 is stored; otherwise, 0 is stored. The value stored in this register is referenced upon execution of the BRANCH instruction.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							ZERO_FLAG

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	–	Reserved. When these bits are read, 0 is returned for each bit. Writing is ignored.
ZERO_FLAG	R	0	0	Stores the result of comparison when CMP1 or CMP2 is executed.

(8) TRIG_WAIT command status register

This register (PMU_TRIG_STATUS: C010_0074H) is cleared in the TRIG_WAIT command decoding cycle. After that, this register retains information on triggers that occurred during execution of TRIG_WAIT (multiple entries possible). The trigger information subject to each TRIG_WAIT command is specified by bits [24:19] of the command.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved		INT	Reserved				TIMER

Name	R/W	Bit	After Reset	Function
Reserved	R	31:6	–	Reserved. When these bits are read, 0 is returned for each bit. Writing is ignored.
INT	R	5	0	If INT is set in the TRIG field of the TRIG_WAIT command and the command is executed, this bit is set to 1 when occurrence of INT is detected.
Reserved	R	4:1	0	Reserved. When these bits are read, 0 is returned for each bit. Writing is ignored.
TIMER	R	0	0	If TIMER is set in the TRIG field of the TRIG_WAIT command and the command is executed, this bit is set to 1 when a time-up occurs in the PMU internal timer.

(9) General-purpose register A

PMU_REGA: C010_0078H

31	30	29	28	27	26	25	24
REGA							
23	22	21	20	19	18	17	16
REGA							
15	14	13	12	11	10	9	8
REGA							
7	6	5	4	3	2	1	0
REGA							

Name	R/W	Bit	After Reset	Function
REGA	R	32:0	0000_0000H	Used for operations in the PMU.

(10) General-purpose register B

PMU_REGB: C010_007CH

31	30	29	28	27	26	25	24
REGB							
23	22	21	20	19	18	17	16
REGB							
15	14	13	12	11	10	9	8
REGB							
7	6	5	4	3	2	1	0
REGB							

Name	R/W	Bit	After Reset	Function
REGB	R	32:0	0000_0000H	Used for operations in the PMU.

(11) ACPU interrupt status register

This register (PMU_INTSTATUS_A: C010_0080H) indicates the status of interrupt sources enabled (mask cancelled). Value 0 is read from the bits corresponding to the interrupt sources disabled (masked).

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						PMU_PCERR	PMU_SERR_A

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	–	Reserved. When these bits are read, 0 is returned for each bit. Writing is ignored.
PMU_PCERR	R	1	0	Command PC error 0: No command PC error interrupt source 1: Command PC error interrupt source occurred
PMU_SERR_A	R	0	0	Indicates the status of the ACPU security error interrupt source. 0: No security error interrupt source 1: Security error interrupt source occurred

(12) ACPU interrupt raw status register

This register (PMU_INTRAWSTATUS_A: C010_0084H) indicates the status of interrupt sources, regardless of the interrupt source enable/disable status.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						PMU_PCERR	PMU_RAWSERR_A

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	–	Reserved. When these bits are read, 0 is returned for each bit. Writing is ignored.
PMU_PCERR	R	1	0	Command PC error 0: No command PC error interrupt source 1: Command PC error interrupt source occurred
PMU_RAWSERR_A	R	0	0	Indicates the raw status of the ACPU security error interrupt source. 0: No security error interrupt source 1: Security error interrupt source occurred

(13) ACPU interrupt enable set register

This register (PMU_INTENSET_A: C010_0088H) enables (cancels masking of) interrupt sources by writing 1 to the corresponding bits.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						PMU_PCERR	PMU_SERREN_A

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	–	Reserved. When these bits are read, 0 is returned for each bit. Writing is ignored.
PMU_PCERR	R	1	0	Indicates whether issuance of the command PC error interrupt request is enabled. 0: Not enabled 1: Enabled
	W			Enables issuance of the command PC error interrupt request. 1: Enables the interrupt (cancels the mask).
PMU_SERREN_A	R	0	0	Indicates whether issuance of the ACPU security error request is enabled. 0: Not enabled 1: Enabled
	W			Enables issuance of the ACPU security error interrupt request. 1: Enables the interrupt (cancels the mask).

(14) ACPU interrupt enable clear register

This register (PMU_INTENCLR_A: C010_008CH) disables (masks) interrupt sources by writing 1 to the corresponding bits.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						PMU_PCERR	PMU_SERRMSK_A

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	–	Reserved. When these bits are read, 0 is returned for each bit. Writing is ignored.
PMU_PCERR	W	1	0	Disables issuance of the command PC error interrupt request. 1: Disables the interrupt.
PMU_SERRMSK_A	W	0	0	Disables issuance of the ACPU security error interrupt request. 1: Disables the interrupt.

(15) ACPU interrupt source clear register

This register (PMU_INTFFCLR_A: C010_0090H) clears interrupt sources by writing 1 to the corresponding bits.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						PMU_PCERR	PMU_SERR CLR_A

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	–	Reserved. When these bits are read, 0 is returned for each bit. Writing is ignored.
PMU_PCERR	W	1	0	Clears the command PC error interrupt source (ACPU). 1: Clears the interrupt source.
PMU_SERRCLR_A	W	0	0	Clears the ACPU security error interrupt source. 1: Clears the interrupt source.

(16) PC error address register

PMU_PCERR: C010_00A8H

31	30	29	28	27	26	25	24
Clear	Reserved						

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved		ERRPC					

7	6	5	4	3	2	1	0
ERRPC							

Name	R/W	Bit	After Reset	Function
Clear	W	31	0	Writing 1 to this bit clears the value of ERRPC.
Reserved	R	30:14	0	Reserved. When these bits are read, 0 is returned for each bit. Writing is ignored.
ERRPC	R	13:0	0	Indicates the address of the command that caused a PC error.

Caution When a PC error occurs, the address of the command is stored in ERRPC and the value is retained until ERRPC is cleared.

(17) Command buffer RAM register

PMU_CMD_BUF_RAM: C010_1000H to C010_1FFCH

31	30	29	28	27	26	25	24
CMD_BUF_RAM							
23	22	21	20	19	18	17	16
CMD_BUF_RAM							
15	14	13	12	11	10	9	8
CMD_BUF_RAM							
7	6	5	4	3	2	1	0
CMD_BUF_RAM							

Name	R/W	Bit	After Reset	Function
CMD_BUF_RAM	R/W	31:0	–	Stores the command to be processed while the PMU is operating. A command consists of 1,024 words. A byte enable command issued for this field is ignored. Be sure to access this field in word units.

Caution Store REG_WRITE for clearing SP0_INT following the SP0_WRITE command. Because REG_WRITE will not be executed if the power-on sequence is entered by inputting INT_IRQ0Z or INT_FIQ0Z, store the SP0_INT clear instruction in POWER_ON_PC as the first command executed.

The same command cannot be set to CMD_BUF_RAM and CMD_BUF_FF.

(18) Command buffer FF register

PMU_CMD_BUF_FF: C010_2000 to C010_203CH

31	30	29	28	27	26	25	24
CMD_BUF_FF							
23	22	21	20	19	18	17	16
CMD_BUF_FF							
15	14	13	12	11	10	9	8
CMD_BUF_FF							
7	6	5	4	3	2	1	0
CMD_BUF_FF							

Name	R/W	Bit	After Reset	Function
CMD_BUF_FF	R/W	31:0	–	Stores the command to be processed while the PMU is operating. A command consists of 16 words. A byte enable command issued for this field is ignored. Be sure to access this field in word units.

Caution Store REG_WRITE for clearing SP0_INT following the SP0_WRITE command. Because REG_WRITE will not be executed if the power-on sequence is entered by inputting INT_IRQ0Z or INT_FIQ0Z, store the SP0_INT clear instruction in POWER_ON_PC as the first command executed. CMD_BUF_FF can be read or written regardless of the voltage. The same command cannot be set to CMD_BUF_RAM and CMD_BUF_FF.

I.3 Function Details

I.3.1 PMU commands

The REG_WRITE, REG_READ and RMW commands can be used to access APB slave registers. The macro is selected by using the MacroSelect bit in each command. The macro can be selected according to the following table.

Table I-1. APB Slave Macro Selection Bits

Slave Name	MacroSelect	Address
ATIM	00H	C000_0000H to C000_FFFCH
AINT	01H	C002_0000H to C002_FFFCH
LCD	02H	C004_0000H to C004_FFFCH
GIO	03H	C005_0000H to C005_FFFCH
SI1	04H	C008_0000H to C008_FFFCH
MEMC	05H	C00A_0000H to C00A_FFFCH
PWM	06H	C00B_0000H to C00B_FFFCH
Reserved	07H	C00C_0000H to C00C_FFFCH
Reserved	08H	C00D_0000H to C00D_FFFCH
PMU	09H	C010_0000H to C010_FFFCH
ASMU	0AH	C011_0000H to C011_FFFCH
SPI0	0BH	C012_0000H to C012_FFFCH
SPI1	0CH	C013_0000H to C013_FFFCH
CHG	0DH	C014_0000H to C014_FFFCH
SI0	0EH	C00E_0000H to C00E_FFFCH
AXL0	0FH	C00F_0000H to C00F_FFFCH
Reserved	10H	C803_0000H to C803_FFFCH
ASMU_S2	11H	CC00_0000H to CC00_FFFCH
AINT_S2	12H	CC01_0000H to CC01_FFFCH
MEMC_S2	13H	CC02_0000H to CC02_FFFCH
Reserved	14H	CC03_0000H to CC03_FFFCH

The 31st bit in the first word of a command is used for break processing. If this bit is set to 1, execution is kept waiting after command execution until an interrupt from GIO (GIO_INT) is input. To avoid break processing, set this bit to 0.

Set bit fields that are not assigned to any setting to 0.

Caution The command buffer area is allocated from 1000H to 203CH. Operation is not guaranteed if the program counter is set outside this range.

I.4 PMU Commands

This section explains the commands that are executed while the PMU is operating.

(1) Register access commands

Command name	Bit width: 32 (31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)	Function
REG_WRITE	BK | 00h | MacroSelect | Address[15:0] Data[31:0]	Register write (2-word command) The MacroSelect bit specification is as shown in Table I-1. Use RMW.
SP0_WRITE	BK | 01h | Address[15:0] Data[31:0]	SP0 register write (2-word command) Waits until SP0_INT occurs after write access is completed. After execution of this command, execute the REG_WRITE command to clear SP0_INT.
REG_READ	BK | 02h | A/B | MacroSelect | Address[15:0]	Register read (1-word command) Stores the register read value to REGA or REGB according to the A/B bit field setting. A/B: 0: REGA 1: REGB
RMW	BK | 03h | MacroSelect | Address[15:0] Data[31:0] Data_EN[31:0]	Register read/modify/write (3-word command) Writes data only to enabled bits (Data_EN = 1). The MacroSelect bit specification is as shown in Table I-1.
MOVE	BK | 04h | A/B Data[31:0]	General-purpose register set command (2-word command) Stores Data[31:0] to a register according to the A/B bit field setting. A/B: 0: REGA 1: REGB
REG_WRITE2	BK | 09h | A/B | MacroSelect | Address[15:0]	Register write 2 (1 word command) The MacroSelect bit specification is as shown in Table I-1. Writes data in the register specified by the A/B bit field to the specified address. A/B: 0: REGA 1: REGB

(2) Logical operation commands

Command name	Bit width: 32 (31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)	Function
AND	BK | 05h | A/B Data[31: 0]	AND command (2-word command) REG(A/B) = REG (A/B) AND Data ANDs the data in the register specified by the A/B bit field and Data[31:0] and stores the result in the specified register. A/B: 0: REGA 1: REGB
EXOR	BK | 06h | A/B Data[31: 0]	EXOR command (2-word command) REG(A/B) = REG (A/B)EXOR Data EXORs the data in the register specified by the A/B bit field and Data[31:0] and stores the result in the specified register. A/B: 0: REGA 1: REGB
CMP1	BK | 07h	Compare command (1-word command) Compares the values of REGA and REGB and stores the result in bit 0 of PSR. If the values match, 1 is stored; otherwise, 0 is stored.
CMP2	BK | 08h | A/B Data[31: 0]	Compare command (2-word command) Compares the values of REG(A/B) and Data and stores the result in bit 0 of PSR. If the values match, 1 is stored; otherwise, 0 is stored. A/B: 0: REGA 1: REGB

(3) Branch and jump commands

Command name	Bit width: 32																										Function
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
BRANCH	BK	10h						OP											JUMP value[13:0]														Conditional branch command (1-word command) References bit 0 of the PSR register and jumps to the PC for the absolute JUMP value according to op. Jumps to PC + 4 if the value of bit 0 differs. op: 0: beq 1: bne
JUMP	BK	11h																	JUMP value[13:0]														Relative JUMP (1-word command) (Current PC + JUMP value) Set the jump destination in the minus direction by using the 2's complement.
AJUMP	BK	12h																	JUMP value[13:0]														Absolute JUMP (1-word command) Jumps to the specified PC.
SUBROUTINE_START	BK	13h																	JUMP value[13:0]														Jump to specified absolute JUMP value (1-word command) JUMP, AJUMP, and BRANCH within a subroutine is possible, but nesting inside another subroutine in a subroutine is not possible.
RFS	BK	14h																															Return From Subroutine (1-word command) Jumps to PC + 4 of the SUBROUTINE_START command that was executed immediately before this command. Only one address can be saved.

(4) Wait commands

Command name	Bit width: 32 (31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)	Function
TIMERWAIT	BK (31) = BK; 20h (30–25) = 20h; INT (24) = INT; Count value[15:0] (15–0) = Count value[15:0]	32.768 kHz 16-bit timer (1-word command) Waits until timer counting ends (about 2 seconds max.). Use this command for waiting when the clock frequency is switched. Issues WDT clear when counting starts and ends. Waits first until completion of the previous TIMERWAIT end processing, if it is not complete. Set the WDT count value (WDT_COUNT_LMT) to the TIMERWAIT count value or higher. Setting the count value to 0 is prohibited. The handling of interrupt signals during the TIMERWAIT period can be changed by using the INT bit field. 0: Stop waiting when INT_IRQ0Z or INT_FIQ0Z is input during TIMERWAIT. 1: Continue waiting even if INT_IRQ0Z or INT_FIQ0Z is input.
INTWAIT	BK (31) = BK; 21h (30–25) = 21h	Waits until INT_IRQ0Z or INT_FIQ0Z is issued from AINT. Clears the WDT when waiting starts and ends. If the operation is to be kept waiting for a long period, store the WDT_STOP command before this command. Clears the WDT if an interrupt is active from the beginning and executes command processing.
SMU_READY_WAIT	BK (31) = BK; 23h (30–25) = 23h; LEVEL (24) = LEVEL	Waits until the ASMU operation enters the specified state. The operation is kept waiting even if INT_IRQ0Z or INT_FIQ0Z is input during the wait period. LEVEL: 0: Low level 1: High level
TRIG_WAIT	BK (31) = BK; 24h (30–25) = 24h; TRIG (24) = TRIG; TRIG (19) = TRIG; Count value[15:0] (15–0) = Count value[15:0]	Trigger wait Clears the PMU_TRIG_STATUS register after a command is decoded. After that, the operation is kept waiting until the level of the trigger specified by TRIG is detected. The wait state is immediately released if the specified trigger has already occurred upon command execution. The trigger that occurred is stored in the PMU_TRIG_STATUS register and REGA. The TRIG bit field shows the following. [24]: Specifies INT as a trigger. [19]: Specifies TIMER. Multiple triggers can be specified. TIMER of this command specifies the use of a 32.768 kHz clock and specifies the number of countable cycles in 16-bit units. Be sure to set the count value to a value of 1 or larger, regardless of whether the TIMER is specified as a trigger. (Setting TIMER to 0 is prohibited.) If 0 is set, the subsequent TIMERWAIT command may end without a wait period being inserted. Waits until processing of the TIMERWAIT or TRIG_WAIT executed before completion of this command, if it has not been completed. Set the WDT count value to the count value of this command or larger.
QR_WAIT	BK (31) = BK; 25h (30–25) = 25h; B/R (24) = B/R	QR operation end wait The B/R bit field shows the following. The operation is kept waiting until completion of the specified backup or restore processing. 0: Backup processing 1: Restore processing If INT_IRQ0Z or INT_WAIT is input during the wait period, backup processing wait is released but restore processing wait is not released.
CYCLE_WAIT	BK (31) = BK; 26h (30–25) = 26h; INT (24) = INT; Count value[9:0] (9–0) = Count value[9:0]	Wait for the specified number of clock cycles The count can be set in 10-bit units (up to 1,023). The number of cycles is counted based on PMU_CLK. The minimum count is 5 cycles (TBD). Setting a lower count is prohibited. PMU_CLK is set by the ASMU. Normal mode: 1/6 or 1/8 of main PLL Economy mode: 1/16 of main PLL Sleep/Standby mode: 1/4 or 1/8 of PLL3 DeepSleep/PowerDown mode: 32.768 kHz The handling of interrupt signals during the TIMERWAIT period can be changed by using the INT bit field. 0: Stop waiting when INT_IRQ0Z or INT_FIQ0Z is input during TIMERWAIT. 1: Continue waiting even if INT_IRQ0Z or INT_FIQ0Z is input.
LCD_MODE_WAIT	BK (31) = BK; 27h (30–25) = 27h	LCD-SDRAM direct mode transition wait Monitors the mode status signal from the LCD controller and waits for completion of switching to the direct mode. After execution of this command, clear the interrupt from the LCD controller by using the REG_WRITE command.

(5) Interrupt commands

Command name	Bit width: 32 (31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)	Function
INT_MASK	BK (31) / 30h (30 29 28 27 26 25) / MASK (24) / (23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)	Interrupt mask While interrupts are masked, the power-on sequence is not entered automatically when a command is fetched by an interrupt. This setting only suppresses transition to the power-on sequence. When an interrupt occurs, the TIMERWAIT state is released. MASK: 0: Releases interrupt masking 1: Masks interrupts.
ARMINT_MASK	BK (31) / 31h (30 29 28 27 26 25) / MASK (24) / (23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)	Masks and releases masking of interrupt signals issued to ARM. If an interrupt has already been issued upon execution of this command, the interrupt is reported to the ACPU. MASK: 0: Releases interrupt masking 1: Masks interrupts

(6) Other commands

Command name	Bit width: 32 (31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)	Function
WDT_CLEAR	BK (31) / 32h (30 29 28 27 26 25 24) / (23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)	WDT count clear
WDT_STOP	BK (31) / 33h (30 29 28 27 26 25 24) / (23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)	WDT operation suspension
WDT_RESTART	BK (31) / 34h (30 29 28 27 26 25 24) / (23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)	WDT count resumption
PMU_END	BK (31) / 35h (30 29 28 27 26 25 24) / (23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)	PMU operation termination Clears the WDT and stops the timer. After that, clears the PMU_START register and makes PMU_CLKREQ to the ASMU low level. Makes PMU_PB1_PREADY high level and ends the PMU master operation. If QR is restored, write H to the ARMNORMAL register in the ASMU immediately before executing this command.
NOP	BK (31) / Others (30 29 28 27 26 25 24) / (23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)	No operation

I.4.1 BREAK function

A PMU command can be used to execute a BREAK function by setting the highest bit in the command's first word to 1. When the command that execute the BREAK function is executed, the operation is kept waiting until the BREAK state is released in the next command fetch cycle.

BREAK can be released by using inputs from GIO. The GIO pins to which the BREAK release function can be assigned are shown below.

GIO Pins to Which BREAK Release Function Can Be Assigned
GPIO1
GPIO6
GPIO9
GPIO18

Assign the BREAK release function to GIO pins by using registers in CHG. If any of the above pins is assigned, the BREAK signal is asserted by an input from the GIO. In the PMU, BREAK is released when an edge of the BREAK signal is detected.

APPENDIX J DDR connection setting

J.1 Recommendation set value

The following set value is recommended about Mobile DDR SDRAM connection setting in EM1-D512.

item	classification	contents
Drive ability setting	Logic	It's possible to move by all DDR output terminal 4mA. Address C014_0400H CHG_DRIVE[19:10] 00 00 00 00 00b
	Mobile DDR SDRAM	1/2 setting Address C00A_200CH MEMC_DDR_CONFIGC1[22:21] (EMRS[6:5]) 01b
Register setting	Clock delayed amount	Address C00A_2020H MEMC_DDR_CONFIGT1[31:8] 000D08h MCLK_DELAY (MCLK delayed adjustment) 0h DQS_O_DELAY (DQS Write delayed adjustment) 8h CLK270_DELAY (DQ, DQM output delayed adjustment) Dh
Calibratuion (S/W)	DQS (Read) correction fixed number	The following is reflected as the correction Offset value to a Calibration result. DQS0=-2 DQS1=-2 DQS2=-2 DQS3=-2

Note: Timing at the time of a reed is decided about by the calibration program mounted on OS automatically.

J.2 AC Parameter

MEMC_DDR_CONFIGA1：C00A_2004H = 53443203H

31	30	29	28	27	26	25	24
tDCRRD=1H			tRRD=2H			tRP=3H	

23	22	21	20	19	18	17	16
tRCD=4H				RCL=1H		WCL=0	

15	14	13	12	11	10	9	8
Reserved	tRWD=3H			Reserved	tWRD=2H		

7	6	5	4	3	2	1	0
Reserved	tRPD=0			Reserved	tWPD=3H		

MEMC_DDR_CONFIGA2：C00A_2008H = 20da1042H

31	30	29	28	27	26	25	24
Reserved				CS1H=0	CS0H=0	ADD_HZ=0	CMD_HZ=0

23	22	21	20	19	18	17	16
tSREX=dH				tRFC=aH			

15	14	13	12	11	10	9	8
Reserved			LowFrqTyp=1	DQS_mask_Ext=0	DQS_mask=0		DQM_HZ=0

7	6	5	4	3	2	1	0
IO_HZ=0	AutoPre=1	CLK_MODE=0		PstamblExt=0	PreamblExt=0	DBParkEna=1	Reserved

Revision Histoy

Date	Revision	Comments
February 10, 2009	1.0	−
April 27, 2009	2.0	Incremental update from comments to the 1.0. The function related to the CAM is added.
June 30, 2009	3.0	Incremental update from comments to the 2.0.
September 30, 2009	4.0	Incremental update from comments to the 3.0. UTEST pins : Handling When Not Used : Leave open -> “L” level hold. The item of the system state transition is added. (chapter 5.2)
December 22, 2009	5.0	Incremental update from comments to the 4.0.
February 15, 2010	6.0	Incremental update from comments to the 5.0.
March 31, 2010	7.0	Product name change (MC-10118 -> MC-10118B)
June 30, 2010	8.0	Incremental update from comments to the 7.0.

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