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RENESAS

Preliminary User's Manual

Memory Controller

NB85E, NB85ET

NB85E500
NU85E500
NU85E502

Document No. A14206EJ5V1UM00 (5th edition)
Date Published January 2002 NS CP(N)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Major Revisions in This Edition

Page	Description
p.17	Addition of bank precharge command in **Figure 1-2 SDRAM Sequential Write Cycle (Bank Change)**
p.19	Addition of **Note** in **1.2.1 (1) SRAM/I/O controller**
p.19	Modification of **1.2.1 (2) Page ROM controller**
p.23	Modification of **1.2.3 (2) (c) Bus arbitration controller**
p.30	Modification of **1.3.2 (3) (m) CSZ7 to CSZ0, (n) BENZ3 to BENZ0, and (q) SELFREF**
p.36	Modification of **Caution** in **Figure 1-5 Bus Cycle Type Configuration Registers 0 and 1 (BCT0 and BCT1)**
p.40	Addition of description in **1.4.4 (1) External wait function**
p.40	Addition of description and figure in **1.4.4 (2) Data wait control registers and external waits**
p.45	Modification of **Figure 1-12 SRAM write timing**
pp.50, 51	Addition of **Caution** in **Figure 1-16 Page ROM Configuration Register (PRC)**
pp.55, 56	Modification of **Figure 1-20 Page ROM Read Timing**
p.58	Modification of **1.4.8 (1) Bus hold procedure**, **(2) Bus hold release procedure**
p.60	Addition of **Caution** in **1.4.9 Bus cycle period control register (BCP)**
p.65	Modification of **Figure 1-28 User Logic Design Example (NU85E500)**
p.81	Addition of **Remark** in **2.1 Outline**
p.82	Modification of **2.1.1 Features**
p.91	Modification and addition of **Cautions** in **2.3.1 SDRAM configuration register n (SCRn)**
p.92	Modification of **Figure 2-4 SDRAM Configuration Register n (SCRn)**
pp.94 to 97	Addition of **2.3.1 (1) Address outputs and SDRAM connection, (2) Bank address outputs**
p.98	Modification of **Figure 2-5 64 Mbit SDRAM Connection Example**
p.101	Modification of **2.3.2 (2) Bus timing**
p.103	Modification of **Figure 2-9 SDRAM Single Read Cycle (32-Bit Data Bus, Word Access)**
p.105	Modification of **Figure 2-10 SDRAM Single Write Cycle (32-Bit Data Bus, Word Access)**
p.111	Modification of **Figure 2-15 SDRAM Sequential Write Cycle (16-Bit Data Bus, Word Access, Bank Change, CAS Latency = 2, BCW = 1)**
p.112	Modification of **Figure 2-16 SDRAM Sequential Write Cycle (8-Bit Data Bus, Word Access, Bank Change, CAS Latency = 2, BCW = 1)**
p.114	Addition of **Caution** in **Figure 2-17 SDRAM Refresh Control Register n (RFSn)**
p.115	Addition of **2.3.4 CBR refresh function**
p.116	Modification of **Figure 2-18 SDRAM CBR Refresh Timing**
p.117	Modification of **2.3.5 Self-refresh function**
p.118	Modification of **Figure 2-19 SDRAM Self-Refresh Timing**
p.119	Addition of **2.3.6 Notes for refresh function**
pp.124 to 126	Addition of **APPENDIX B REVISION HISTORY**

The mark ⋆ shows major revised points.

PREFACE

Target Readers

This manual is intended for users who wish to understand the functions of the memory controllers (NB85E500, NU85E500, and NU85E502) for the NB85E and NB85ET CPU cores for CBICs and who design application systems using these CPU cores.

Purpose

This manual's purpose is to help the user understand the functions of the NB85E500, NU85E500, and NU85E502.

Organization

This manual is organized as follows.

CHAPTER 1 NB85E500 AND NU85E500

This chapter explains the NB85E500 and NU85E500, which are the basic macros for controlling external memory.

The NB85E500 is a memory controller for the NB85E and NB85ET, and the NU85E500 is a memory controller for the NB85E. The NB85E500 and NU85E500 contain an on-chip SRAM/I/O controller, and page ROM controller.

CHAPTER 2 NU85E502

This chapter explains the NU85E502, which is an SDRAM controller.

How to Use This Manual

This manual assumes that the reader has general knowledge of electrical engineering, logic circuits, microcontrollers, SRAM, page ROM, and SDRAM.

To gain a general understanding of the NB85E500, NU85E500, and NU85E502 functions, be sure to read:

→ This manual according to the **CONTENTS**

For information about the functions of the NB85E and NB85ET, be sure to read:

→ **NB85E Hardware User's Manual (A13971E), NB85ET Hardware User's Manual (A14342E)**

In this manual, the memory controllers (NB85E500, NU85E500, and NU85E502) are referred to as MEMC. Unless specified otherwise, the NB85E is described as the representative CPU core in this manual. When using the NB85ET, read the CPU core name as NB85ET.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	xxxZ (Z is appended to pin or signal name)
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numerical representation:	Binary … xxxx or xxxxB
	Decimal … xxxx
	Hexadecimal … xxxxH
Prefix indicating the power of 2 (address space, memory capacity):	
	K (kilo): $2^{10} = 1,024$
	M (mega): $2^{20} = 1,024^2$
	G (giga): $2^{30} = 1,024^3$
Data types:	Word … 32 bits
	Halfword … 16 bits
	Byte … 8 bits

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- NB85E Hardware User's Manual (A13971E)
- NB85ET Hardware User's Manual (A14342E)
- CB-9 Family VX/VM Type NB85E, NB85ET Design Manual (A14335E)
- CB-9 Family VX/VM Type Core Library CPU Core, Memory Controller Design Manual (A13195E)
- How to Use SDRAM and SGRAM User's Manual (M13132E)
- Synchronous DRAM Application Note (M12394E)

The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

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LIST OF FIGURES (1/2)

LIST OF FIGURES (2/2)

LIST OF TABLES

CHAPTER 1 NB85E500 AND NU85E500

The NB85E500 is a memory controller for the NB85E and NB85ET, and the NU85E500 is a memory controller for the NB85E.

The Nx85E500 is used as follows according to the type of external memory to be connected.

Target CPU Core	Type of External Memory to Be Connected	Memory Controller (MEMC)
NB85E	SRAM, ROM, page ROM, flash memory	NB85E500/NU85E500
	SDRAM	NB85E500/NU85E500 + NU85E502
NB85ET	SRAM, ROM, page ROM, flash memory	NB85E500
	SDRAM	NB85E500 + NU85E502

Remark Refer to **CHAPTER 2 NU85E502** for details of the NU85E502.

In this chapter, Nx85E500 represents the NB85E500 and NU85E500. Differences between the NB85E500 and NU85E500 are explained separately, but other parts in common are explained together as the Nx85E500.

1.1 Differences Between NB85E500 and NU85E500

The differences between the NB85E500 and NU85E500 are shown below.

Item		NB85E500	NU85E500
External memory data bus pin		D31 to D0 (I/O)	DI31 to DI0 (Input), DO31 to DO0 (Output)[Note]
SDRAM sequential write timing		Refer to **Figures 1-1** and **1-2**.	
	Write data output value to SDRAM	The values of the VBD31 to VBD0 pins are output from the D31 to D0 pins	The values of the VBD31 to VBD0 pins are output from the DO31 to DO0 pins after being latched in the NU85E500
	Setup time of 2nd and subsequent write data	0.5 clock	1 clock
	On-page cycle	1 clock earlier in the NB85E500 than in the NU85E500	

Note The DO31 to DO0 pins are not 3-state output.

The SDRAM sequential write timing examples are shown below.

Remarks 1. These timing examples are for the following cases.

- Data bus width 8 bits
- Word access
- CAS latency = 2
- Number of wait states set using the BCW1 and BCW0 bits of the NU85E502 SCRn register = 1 (n = 7 to 0)

2. The signals in the timing examples are the signals of the NU85E502.

3. Broken-line portions of the VBD31 to VBD0 and VBWAIT signals indicate a weak unknown state; a state entered when the NB85E internal bus holder is driving. The level of the broken-line portions of the D31 to D0 and DO31 to DO0 signals is undefined.

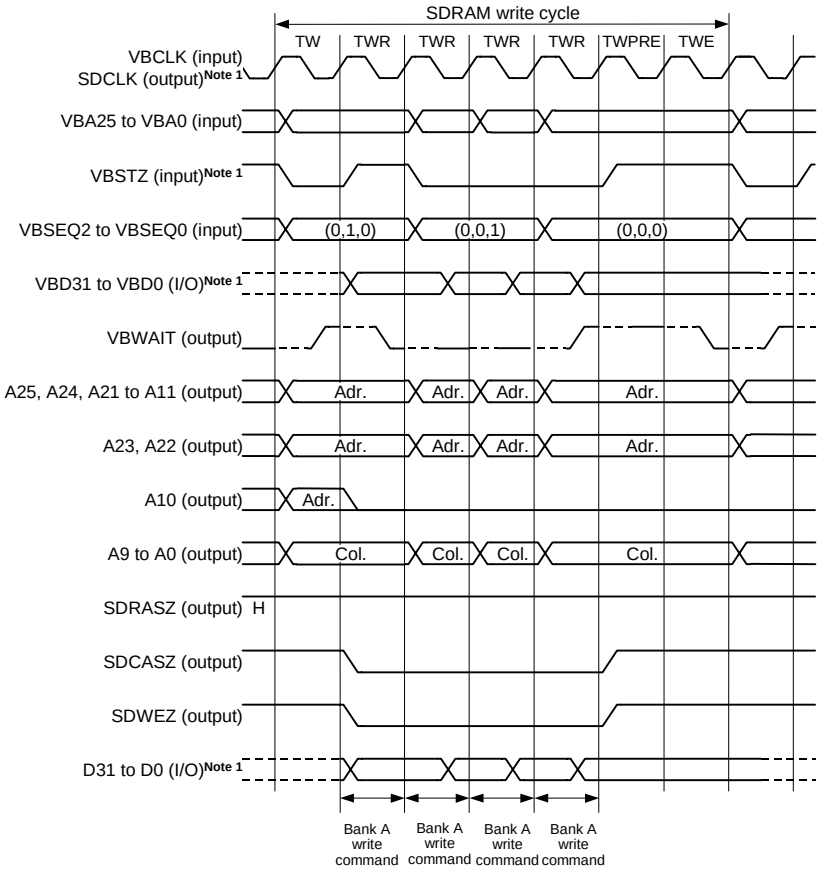
4. Refer to **NB85E Hardware User's Manual (A13971E)** for details of the VSB signals (VBxxx, VDxxx).

5. TACT state: State of the bank active command
TW state: Wait state
TWE state: State that indicates write cycle end
TWPRE state: State that indicates precharge
TWR state: State of the write command

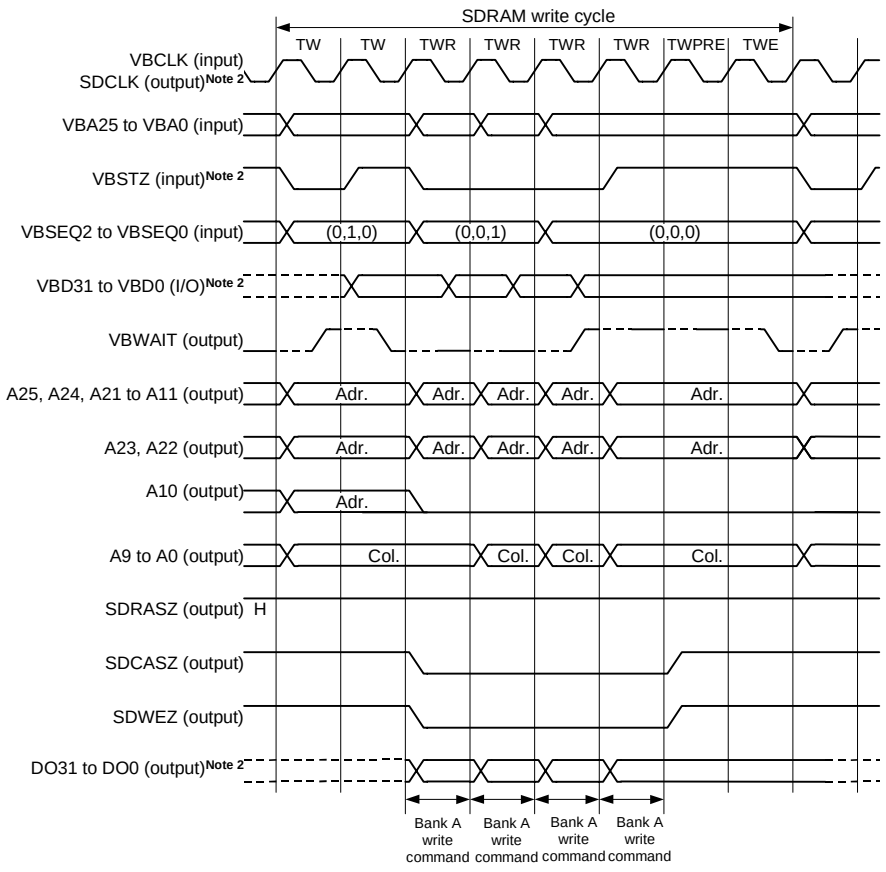
6. BCW: Wait state set by the BCW1 and BCW0 bits of the SCRn register (n = 7 to 0).

Figure 1-1. SDRAM Sequential Write Cycle (On-Page)

(a) NB85E500



(b) NU85E500

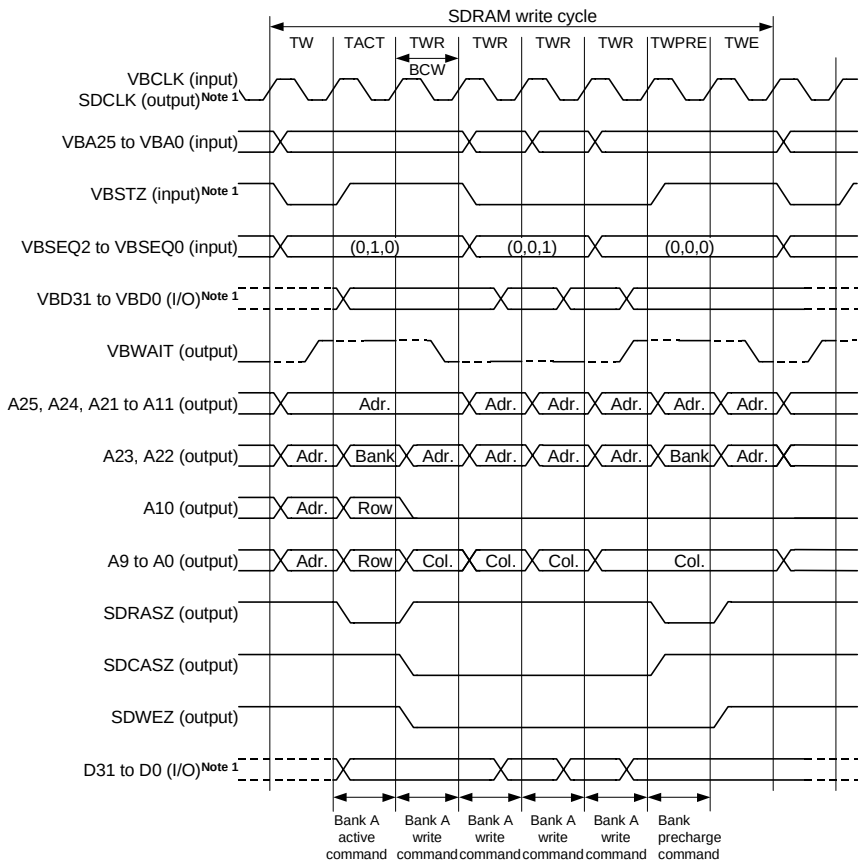


Notes 1. NB85E500 signal

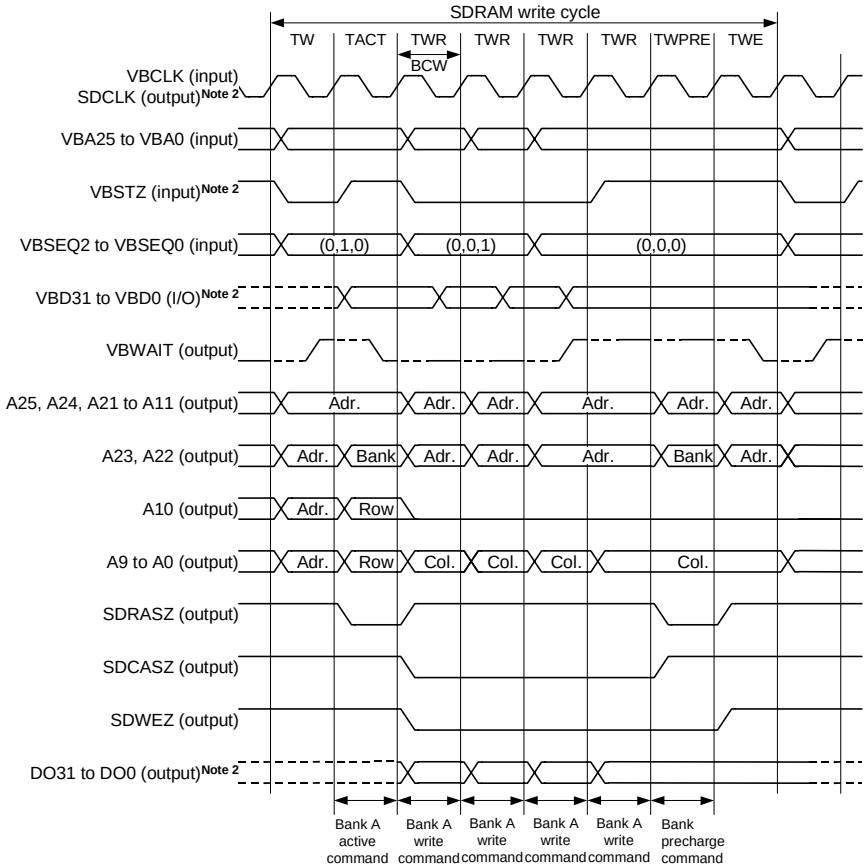
Notes 2. NU85E500 signal

Figure 1-2. SDRAM Sequential Write Cycle (Bank Change)

(a) NB85E500



(b) NU85E500



Notes 1. NB85E500 signal

Notes 2. NU85E500 signal

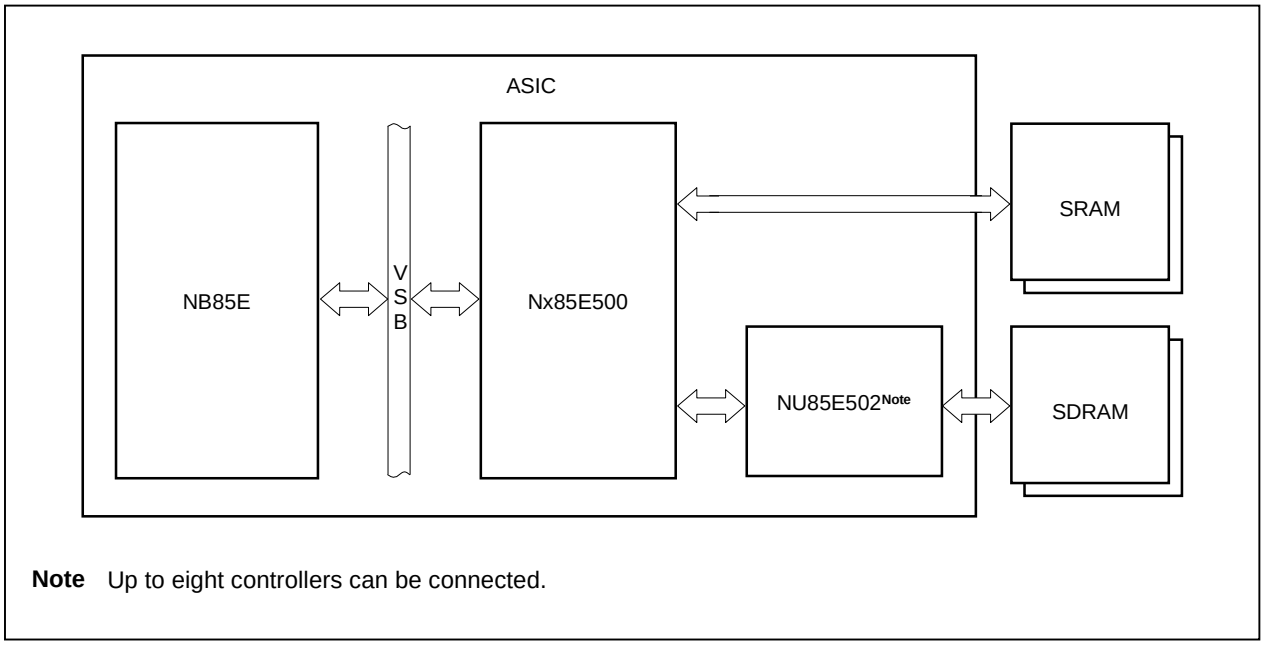
1.2 Outline

The Nx85E500, which is the basic macro for controlling external memory, contains an on-chip SRAM/I/O controller, and page ROM controller.

An external bus cycle can be started by connecting the Nx85E500 to the NB85E via the VSB.

Also, SDRAM can be controlled by connecting the SDRAM controller (NU85E502) to the Nx85E500 (see **Figure 1-3**).

Figure 1-3. SRAM and SDRAM Connection Example



Note Up to eight controllers can be connected.

1.2.1 Features

(1) SRAM/I/O controller

The Nx85E500 has one on-chip SRAM/I/O controller, which controls access to all CSn areas (n = 7 to 0). Its main features are outlined below.

- SRAM can be accessed in at least 2 states.
- Up to 7 programmable data wait states can be inserted by means of DWC0 and DWC1 register settings.
- Up to 3 address setting wait states can be inserted by means of an ASC register setting.
- The data wait can be controlled by WAITZ input.
- Up to 3 idle states can be inserted after a read/write cycle by means of a BCC register setting.
- A DMA flyby cycle[Note] (SRAM → I/O or I/O → SRAM) can be started.

★ **Note** Flyby transfer using SDRAM is not supported.

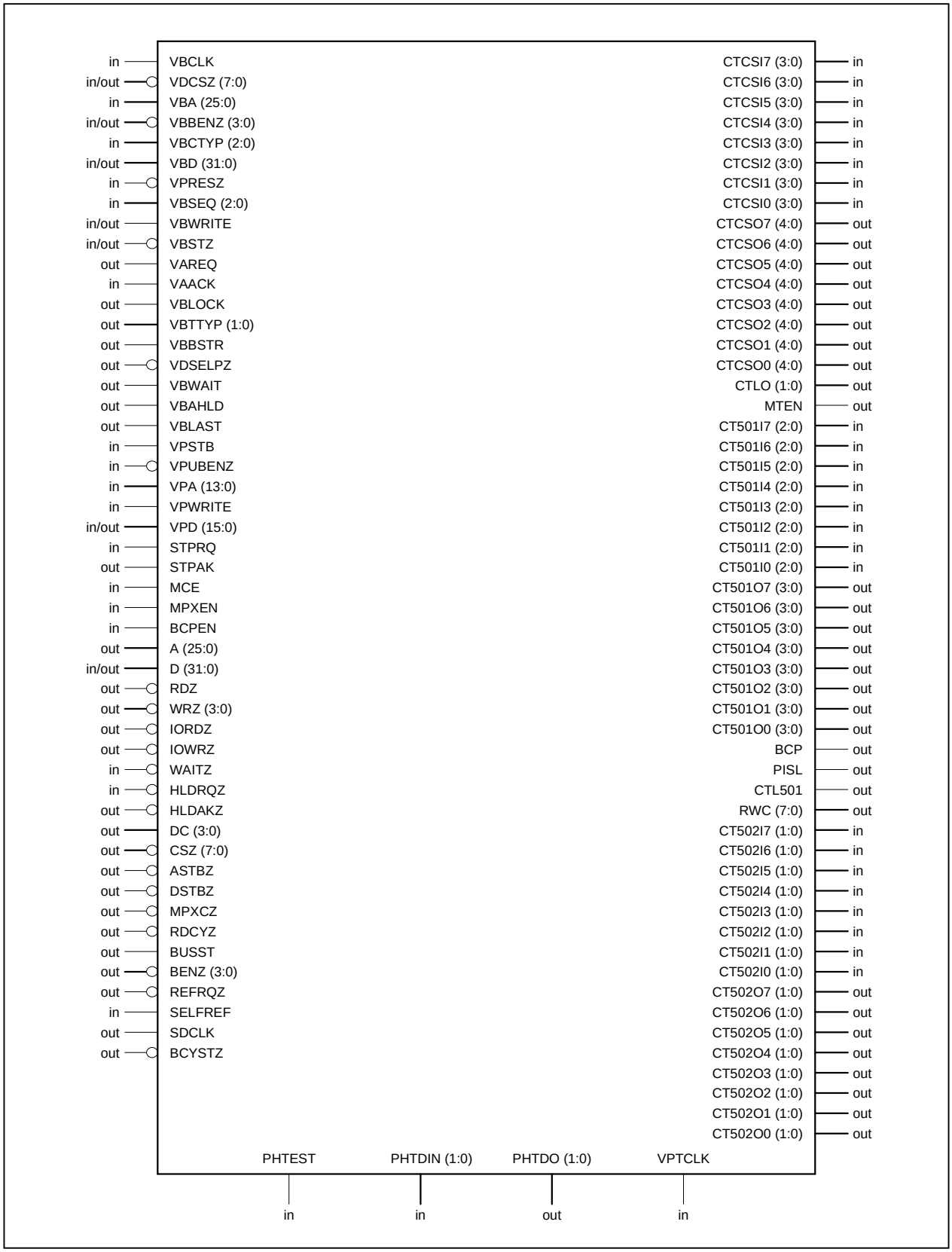
(2) Page ROM controller

The Nx85E500 has one on-chip page ROM controller, which controls access to all CSn areas (n = 7 to 0). The basic bus cycles are the same as those of the SRAM/I/O controller, but this controller has a page access function. Its main features are outlined below.

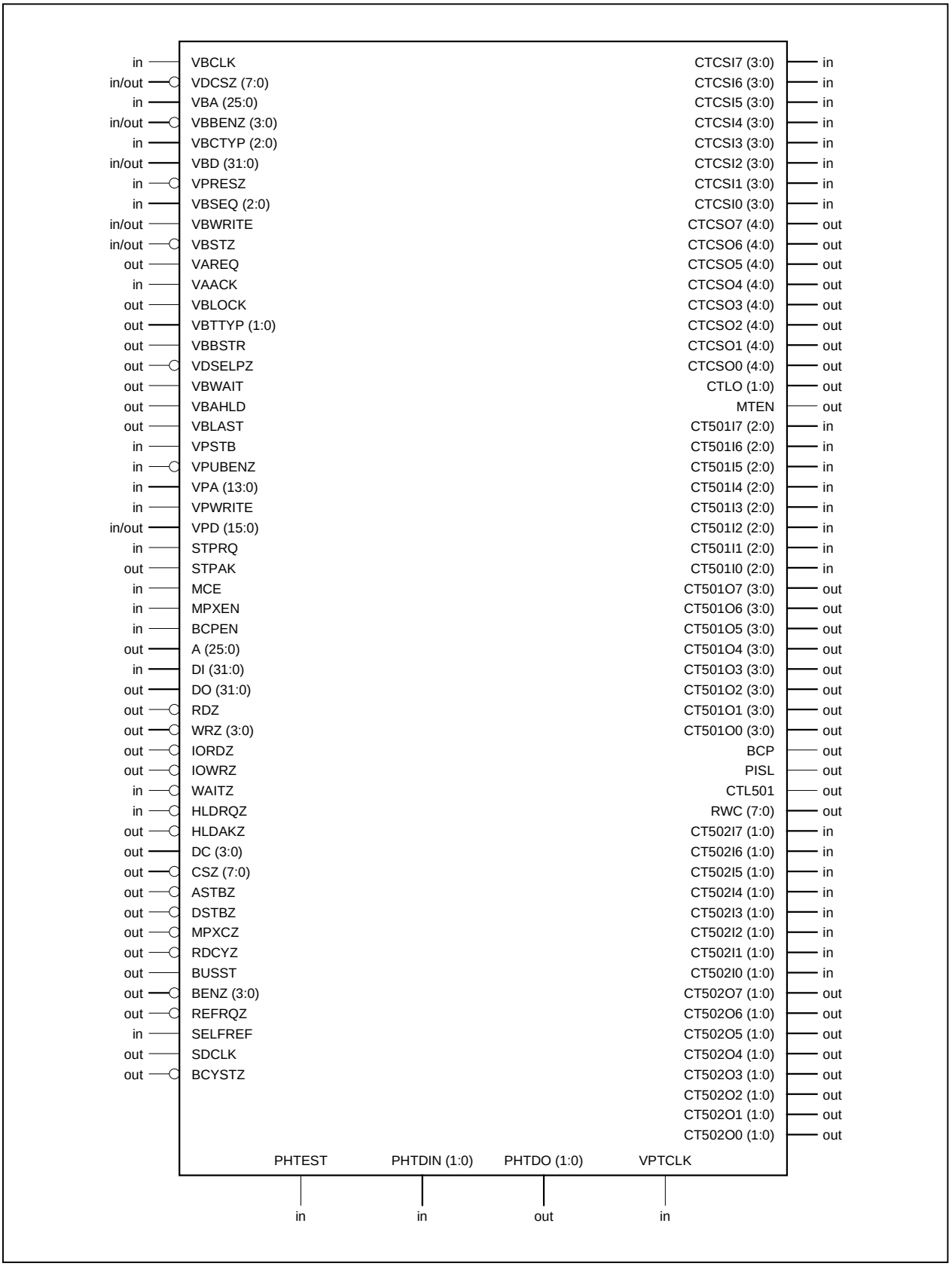
- Page ROM can be accessed in at least 2 states.
- An on-page judgement function is available.
- The address to be compared can be changed by means of a PRC register setting.
- ★ For an on-page cycle, the active level (low level) for the RDZ signal is maintained while the VBSEQ2 to VBSEQ0 signals indicate consecutive transfer (except the value VBSEQ2 to VBSEQ0 = 000) until the VBSEQ2 to VBSEQ0 = 000 cycle is terminated.
- Up to 7 programmable data wait states can be inserted during an off-page cycle by means of DWC0 and DWC1 register settings.
- Up to 7 programmable data wait states can be inserted during an on-page cycle by means of a PRC register setting.
- The data wait can be controlled by WAITZ input.
- A DMA flyby cycle (page ROM → I/O) can be started.
- When there is a write cycle request for the CSn area to which the page ROM is connected, an SRAM write cycle is executed.

1.2.2 Symbol diagram

(1) NB85E500

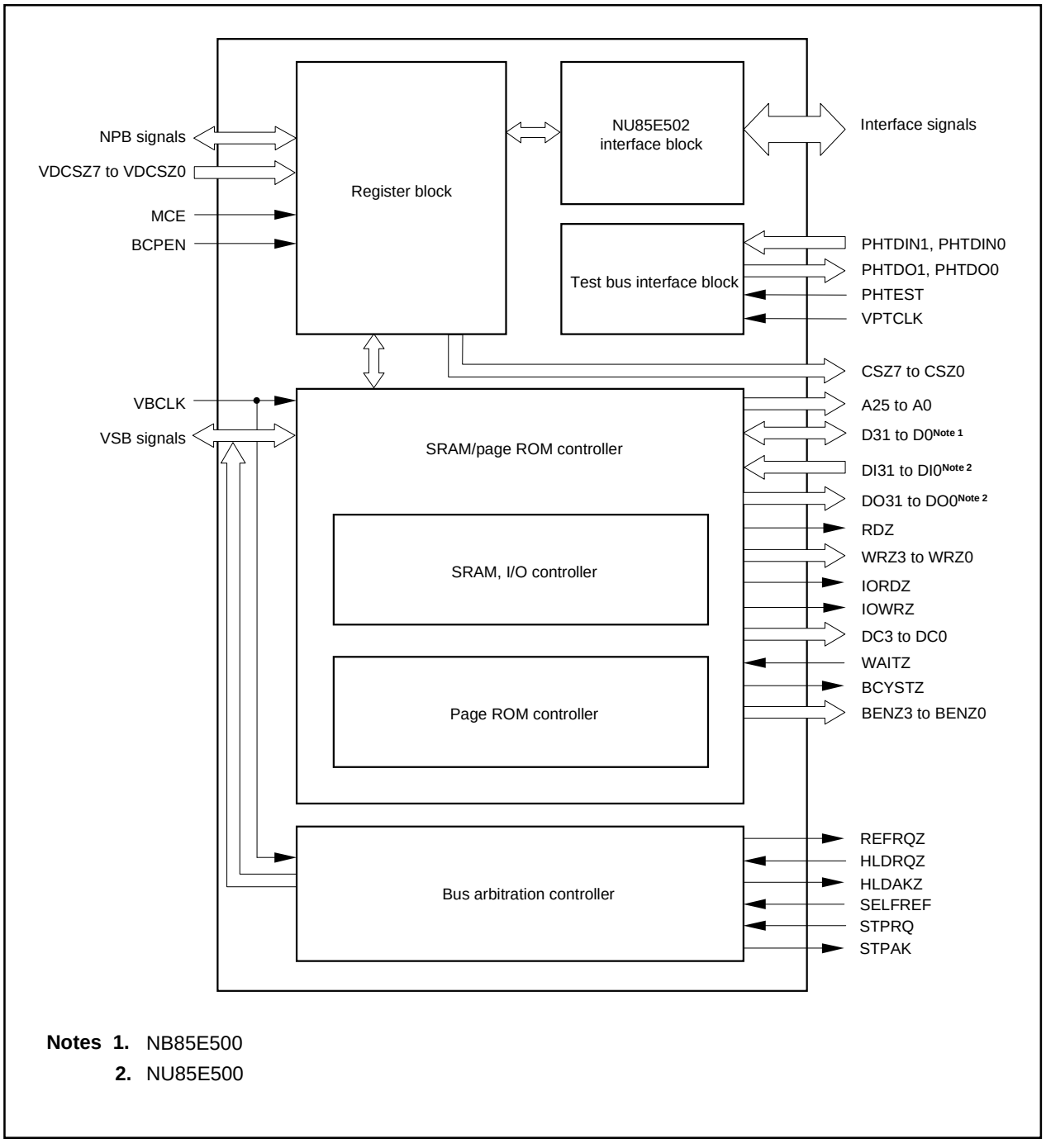


(2) NU85E500


in VBCLK
in/out VDCSZ (7:0)
in VBA (25:0)
in/out VBBENZ (3:0)
in VBCTYP (2:0)
in/out VBD (31:0)
in VPRESZ
in VBSEQ (2:0)
in/out VBWRITE
in/out VBSTZ
out VAREQ
in VAACK
out VBLOCK
out VBTTYP (1:0)
out VBBSTR
out VDSELPZ
out VBWAIT
out VBAHLD
out VBLAST
in VPSTB
in VPUBENZ
in VPA (13:0)
in VPWRITE
in/out VPD (15:0)
in STPRQ
out STPAK
in MCE
in MPXEN
in BCPEN
out A (25:0)
in DI (31:0)
out DO (31:0)
out RDZ
out WRZ (3:0)
out IORDZ
out IOWRZ
in WAITZ
in HLDRQZ
out HLDAKZ
out DC (3:0)
out CSZ (7:0)
out ASTBZ
out DSTBZ
out MPXCZ
out RDCYZ
out BUSST
out BENZ (3:0)
out REFRQZ
in SELFREF
out SDCLK
out BCYSTZ
CTCSI7 (3:0) in
CTCSI6 (3:0) in
CTCSI5 (3:0) in
CTCSI4 (3:0) in
CTCSI3 (3:0) in
CTCSI2 (3:0) in
CTCSI1 (3:0) in
CTCSI0 (3:0) in
CTCSO7 (4:0) out
CTCSO6 (4:0) out
CTCSO5 (4:0) out
CTCSO4 (4:0) out
CTCSO3 (4:0) out
CTCSO2 (4:0) out
CTCSO1 (4:0) out
CTCSO0 (4:0) out
CTLO (1:0) out
MTEN out
CT501I7 (2:0) in
CT501I6 (2:0) in
CT501I5 (2:0) in
CT501I4 (2:0) in
CT501I3 (2:0) in
CT501I2 (2:0) in
CT501I1 (2:0) in
CT501I0 (2:0) in
CT501O7 (3:0) out
CT501O6 (3:0) out
CT501O5 (3:0) out
CT501O4 (3:0) out
CT501O3 (3:0) out
CT501O2 (3:0) out
CT501O1 (3:0) out
CT501O0 (3:0) out
BCP out
PISL out
CTL501 out
RWC (7:0) out
CT502I7 (1:0) in
CT502I6 (1:0) in
CT502I5 (1:0) in
CT502I4 (1:0) in
CT502I3 (1:0) in
CT502I2 (1:0) in
CT502I1 (1:0) in
CT502I0 (1:0) in
CT502O7 (1:0) out
CT502O6 (1:0) out
CT502O5 (1:0) out
CT502O4 (1:0) out
CT502O3 (1:0) out
CT502O2 (1:0) out
CT502O1 (1:0) out
CT502O0 (1:0) out
PHTEST in
PHTDIN (1:0) in
PHTDO (1:0) out
VPTCLK in

1.2.3 Block diagram

(1) Internal block diagram



Notes 1. NB85E500

2. NU85E500

(2) Internal units

(a) Register block

The register block contains on-chip registers for controlling the bus cycle. These registers can be used to select external memory, set the number of idle or wait states, or set the number of consecutive reads of page ROM.

Reading from or writing to the registers is done via the NPB.

(b) SRAM/page ROM controller

The SRAM/page ROM controller controls read and write operations for SRAM, page ROM, and external I/O. Access to all CSn areas can be controlled by this controller alone (n = 7 to 0).

(c) Bus arbitration controller

When the bus arbitration controller receives a STOP mode request signal (STPRQ) from the NB85E, it stops the operation of the memory controller by outputting an acknowledge signal for the STPRQ signal (STPAK) to the NB85E. The VBCLK signal is also stopped at this time.

★ Also, when the bus arbitration controller receives a self-refresh request signal (SELFREF), CBR refresh request from the NU85E502, or external bus hold request signal (HLDRQZ), it sets the bus mastership request signal (VAREQ) to active level so that the external memory becomes the bus master. The bus priority order is as follows.

★ External bus hold request > Refresh request > Bus request from inside the NB85E.

(d) NU85E502 interface block

This is a block for interfacing with the NU85E502. It has a control signal for each CSn area (n = 7 to 0).

(e) Test bus interface block

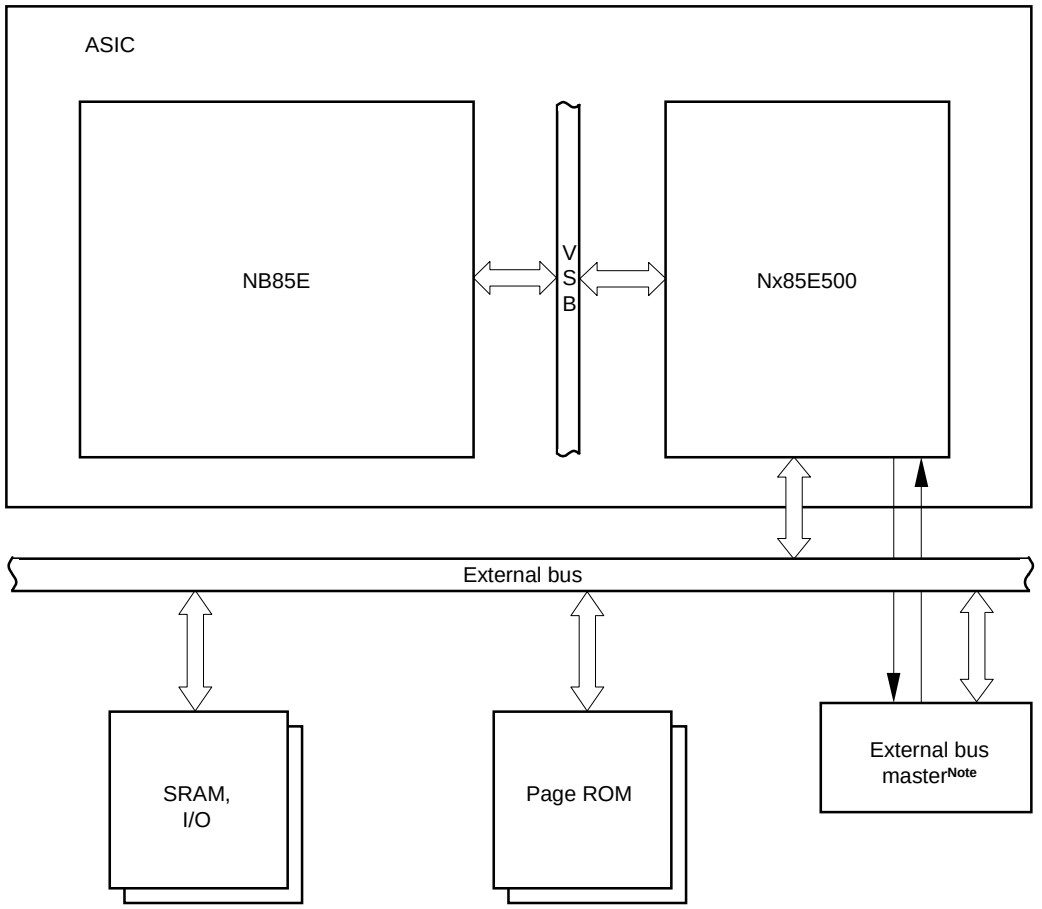
This is a block for interfacing with signals used for testing the Nx85E500. The Nx85E500 can be tested by using the NB85E test mode.

1.2.4 Configuration example

The Nx85E500 starts bus cycles for external memory.

The following figure shows an application example using the Nx85E500.

Figure 1-4. Application Example



Note The Nx85E500 has an external bus master arbitration function, which is controlled by the HLDRQZ and HLDAKZ signals.

1.3 Pin Functions

1.3.1 List of pin functions

(1/3)

Pin Name		I/O	Function
NB85E connection pins	VBCLK	Input	Internal system clock input
	VDCSZ7 to VDCSZ0	I/O	Chip select input/output
	VBA25 to VBA0	Input	Address input
	VBBENZ3 to VBBENZ0	I/O	Byte enable input/output
	VBCTYP2 to VBCTYP0	Input	Bus cycle status input
	VBD31 to VBD0	I/O	Data input/output
	VPRESZ	Input	Reset input
	VBSEQ2 to VBSEQ0	Input	Sequential status input
	VBWRITE	I/O	Read/write status input/output
	VBSTZ	I/O	Transfer start input/output
	VAREQ	Output	Bus use request output
	VAACK	Input	Bus use request acknowledge input
	VBLOCK	Output	Bus lock output
	VBTTYP1, VBTTYP0	Output	Bus transfer type output
	VBBSTR	Output	Burst read status output
	VDSELPZ	Output	Peripheral macro access status output
	VBWAIT	Output	Wait response output
	VBAHLD	Output	Address hold response output
	VBLAST	Output	Last response output
	VPSTB	Input	Data strobe input (for NPB)
	VPUBENZ	Input	Higher byte enable input (for NPB)
	VPA13 to VPA0	Input	Address input (for NPB)
	VPWRITE	Input	Write access strobe input (for NPB)
	VPD15 to VPD0	I/O	Data input/output (for NPB)
	STPRQ	Input	STOP mode request input
	STPAK	Output	Acknowledge output for STPRQ input
Initialization pins	MCE	Input	BCT register MEn bit reset value control input (n = 7 to 0)
	BCPEN	Input	BCP register BCP bit reset value control input
External memory connection pins	A25 to A0	Output	External memory address output
	D31 to D0[Note 1]	I/O	External memory data input/output
	DI31 to DI0[Note 2]	Input	External memory data input
	DO31 to DO0[Note 2]	Output	External memory data output
	RDZ	Output	SRAM/page ROM read strobe output

Notes 1. NB85E500

2. NU85E500

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Pin Name		I/O	Function
External memory connection pins	WRZ3 to WRZ0	Output	SRAM/page ROM write strobe output
	IORDZ	Output	External I/O read strobe output
	IOWRZ	Output	External I/O write strobe output
	WAITZ	Input	Wait request input
	HLDRQZ	Input	External bus hold request input
	HLDAKZ	Output	External bus hold request acknowledge output
	DC3 to DC0	Output	Data bus control output
	CSZ7 to CSZ0	Output	Chip select output
	BENZ3 to BENZ0	Output	Byte enable output
	BCYSTZ	Output	Bus cycle start status output
	REFRQZ	Output	Refresh status output
	SELFREF	Input	Self-refresh request input
	SDCLK	Output	SDRAM synchronization clock output
NU85E502 connection pins	CTCSI73 to CTCSI70	Input	Control input from NU85E502 (for CS7 area)
	CTCSI63 to CTCSI60	Input	Control input from NU85E502 (for CS6 area)
	CTCSI53 to CTCSI50	Input	Control input from NU85E502 (for CS5 area)
	CTCSI43 to CTCSI40	Input	Control input from NU85E502 (for CS4 area)
	CTCSI33 to CTCSI30	Input	Control input from NU85E502 (for CS3 area)
	CTCSI23 to CTCSI20	Input	Control input from NU85E502 (for CS2 area)
	CTCSI13 to CTCSI10	Input	Control input from NU85E502 (for CS1 area)
	CTCSI03 to CTCSI00	Input	Control input from NU85E502 (for CS0 area)
	CTCSO74 to CTCSO70	Output	Control output to NU85E502 (for CS7 area)
	CTCSO64 to CTCSO60	Output	Control output to NU85E502 (for CS6 area)
	CTCSO54 to CTCSO50	Output	Control output to NU85E502 (for CS5 area)
	CTCSO44 to CTCSO40	Output	Control output to NU85E502 (for CS4 area)
	CTCSO34 to CTCSO30	Output	Control output to NU85E502 (for CS3 area)
	CTCSO24 to CTCSO20	Output	Control output to NU85E502 (for CS2 area)
	CTCSO14 to CTCSO10	Output	Control output to NU85E502 (for CS1 area)
	CTCSO04 to CTCSO00	Output	Control output to NU85E502 (for CS0 area)
	CTLO1, CTLO0	Output	Control output to NU85E502
	MTEN	Output	Test mode enable output to NU85E502
	CT502I71, CT502I70	Input	Control input from NU85E502 (for CS7 area)
	CT502I61, CT502I60	Input	Control input from NU85E502 (for CS6 area)
	CT502I51, CT502I50	Input	Control input from NU85E502 (for CS5 area)
	CT502I41, CT502I40	Input	Control input from NU85E502 (for CS4 area)
	CT502I31, CT502I30	Input	Control input from NU85E502 (for CS3 area)
	CT502I21, CT502I20	Input	Control input from NU85E502 (for CS2 area)
	CT502I11, CT502I10	Input	Control input from NU85E502 (for CS1 area)
	CT502I01, CT502I00	Input	Control input from NU85E502 (for CS0 area)

(3/3)

Pin Name		I/O	Function
NU85E502 connection pins	CT502O71, CT502O70	Output	Control output to NU85E502 (for CS7 area)
	CT502O61, CT502O60	Output	Control output to NU85E502 (for CS6 area)
	CT502O51, CT502O50	Output	Control output to NU85E502 (for CS5 area)
	CT502O41, CT502O40	Output	Control output to NU85E502 (for CS4 area)
	CT502O31, CT502O30	Output	Control output to NU85E502 (for CS3 area)
	CT502O21, CT502O20	Output	Control output to NU85E502 (for CS2 area)
	CT502O11, CT502O10	Output	Control output to NU85E502 (for CS1 area)
	CT502O01, CT502O00	Output	Control output to NU85E502 (for CS0 area)
Test mode pins	PHTEST	Input	Peripheral test mode status input
	PHTDIN1, PHTDIN0	Input	Peripheral macro test input
	PHTDO1, PHTDO0	Output	Peripheral macro test output
	VPTCLK	Input	Test clock input
NEC reserved pins	MPXEN	Input	NEC reserved pin (Input low level)
	ASTBZ	Output	NEC reserved pin (Leave open)
	DSTBZ	Output	NEC reserved pin (Leave open)
	MPXCZ	Output	NEC reserved pin (Leave open)
	RDCYZ	Output	NEC reserved pin (Leave open)
	BUSST	Output	NEC reserved pin (Leave open)
	CT501I72 to CT501I70	Input	NEC reserved pin (Input low level)
	CT501I62 to CT501I60	Input	NEC reserved pin (Input low level)
	CT501I52 to CT501I50	Input	NEC reserved pin (Input low level)
	CT501I42 to CT501I40	Input	NEC reserved pin (Input low level)
	CT501I32 to CT501I30	Input	NEC reserved pin (Input low level)
	CT501I22 to CT501I20	Input	NEC reserved pin (Input low level)
	CT501I12 to CT501I10	Input	NEC reserved pin (Input low level)
	CT501I02 to CT501I00	Input	NEC reserved pin (Input low level)
	CT501O73 to CT501O70	Output	NEC reserved pin (Leave open)
	CT501O63 to CT501O60	Output	NEC reserved pin (Leave open)
	CT501O53 to CT501O50	Output	NEC reserved pin (Leave open)
	CT501O43 to CT501O40	Output	NEC reserved pin (Leave open)
	CT501O33 to CT501O30	Output	NEC reserved pin (Leave open)
	CT501O23 to CT501O20	Output	NEC reserved pin (Leave open)
	CT501O13 to CT501O10	Output	NEC reserved pin (Leave open)
	CT501O03 to CT501O00	Output	NEC reserved pin (Leave open)
	BCP	Output	NEC reserved pin (Leave open)
	PISL	Output	NEC reserved pin (Leave open)
	CTL501	Output	NEC reserved pin (Leave open)
	RWC7 to RWC0	Output	NEC reserved pin (Leave open)

1.3.2 Explanation of pin functions

(1) NB85E connection pins

(a) VSB pins (VBxxx, VDxxx, and VAxxx)

Refer to the **NB85E Hardware User's Manual (A13971E)**.

(b) NPB pins (VPxxx)

Refer to the **NB85E Hardware User's Manual (A13971E)**.

(c) STPRQ (input) and STPAK (output)

Refer to the **NB85E Hardware User's Manual (A13971E)**.

(2) Initialization pins

(a) MCE (input)

This is a pin for specifying whether memory controller operation is enabled when a reset occurs.

The reset value of the MEn bit of the BCT0 or BCT1 register is as follows according to the level input to this pin (n = 7 to 0).

Make sure that the level of this pin does not change before and after reset.

- Low level: 0 (memory controller operation is disabled)
- High level: 1 (memory controller operation is enabled)

(b) BCPEN (input)

This is a pin for specifying the length of the bus cycle period when a reset occurs.

The reset value of the BCP bit of the BCP register is as follows according to the level input to this pin.

Make sure that the level of this pin does not change before and after reset.

- Low level: 0 (normal)
- High level: 1 (double)

(3) External memory connection pins

(a) A25 to A0 (output)

These pins constitute the external memory address bus.

When the NU85E502 is active, all of the pins A25 to A0 output a low-level signal.

(b) D31 to D0 (I/O) (NB85E500)

These pins constitute a bidirectional data bus for external memory.

(c) DI31 to DI0 (input) (NU85E500)

These pins constitute the input data bus for external memory.

(d) DO31 to DO0 (output) (NU85E500)

These pins constitute the output data bus for external memory.

(e) RDZ (output)

This is the read strobe output pin for making SRAM or page ROM active.

(f) WRZ3 to WRZ0 (output)

These are the write strobe output pins for making SRAM or external I/O active.

Pin Name	NB85E500	NU85E500
WRZ3	For D31 to D24	For DO31 to DO24
WRZ2	For D23 to D16	For DO23 to DO16
WRZ1	For D15 to D8	For DO15 to DO8
WRZ0	For D7 to D0	For DO7 to DO0

(g) IORDZ (output)

This is the read strobe output pin for making external I/O active during a DMA flyby cycle.

(h) IOWRZ (output)

This is the write strobe output pin for making external I/O active during a DMA flyby cycle.

(i) WAITZ (input)

This is the pin to which a wait request is input from external memory.

(j) HLDRQZ (input)

This is the pin to which a bus hold request is input from an external source.
An active level must be maintained during a bus hold.

(k) HLDAKZ (output)

This is the pin from which a bus hold acknowledge is output to an external source.
It indicates that a bus hold is permitted.

(l) DC3 to DC0 (output)

These are the output pins for controlling the data bus input/output buffer direction. They output a high level when a read is performed and a low level when a write is performed.

Pin Name	NB85E500	NU85E500
DC3	For D31 to D24	For DI31 to DI24, DO31 to DO24
DC2	For D23 to D16	For DI23 to DI16, DO23 to DO16
DC1	For D15 to D8	For DI15 to DI8, DO15 to DO8
DC0	For D7 to D0	For DI7 to DI0, DO7 to DO0

(m) CSZ7 to CSZ0 (output)

These are the chip select output pins.

★ Values input to the VDCSZ7 to VDCSZ0 pins are output.

CSZ7 ... For CS7 area
CSZ6 ... For CS6 area
CSZ5 ... For CS5 area
CSZ4 ... For CS4 area
CSZ3 ... For CS3 area
CSZ2 ... For CS2 area
CSZ1 ... For CS1 area
CSZ0 ... For CS0 area

(n) BENZ3 to BENZ0 (output)

★ These are the byte enable output pins. Values input to the VBBENZ3 to VBBENZ0 pins of the NB85E are output.

(o) BCYSTZ (output)

This is the pin for indicating the bus cycle start status.

(p) REFRQZ (output)

This is the pin for indicating the execution status of the refresh cycle to SDRAM. It is used when an NU85E502 is connected.

This pin outputs a low level when a refresh cycle is executed and a high level when a refresh cycle is not executed.

If this pin outputs a low level during a bus hold, it indicates that a refresh request has been generated for the external bus master.

(q) SELFREF (input)

★ This is the pin to which a self-refresh request is input. It is used when an NU85E502 is connected.

The input level to this pin indicates whether or not there is a self-refresh request.

- Low level: There is no self-refresh request.
- High level: There is a self-refresh request.

(r) SDCLK (output)

This is the synchronization clock output pin for external SDRAM. It is used when an NU85E502 is connected.

(4) NU85E502 connection pins

(a) CTCSIn3 to CTCSIn0 (n = 7 to 0) (input)

These are the pins for controlling input from the NU85E502 for each CSn area (n = 7 to 0).

CTCSI73 to CTCSI70 ... For CS7 area
CTCSI63 to CTCSI60 ... For CS6 area
CTCSI53 to CTCSI50 ... For CS5 area
CTCSI43 to CTCSI40 ... For CS4 area
CTCSI33 to CTCSI30 ... For CS3 area
CTCSI23 to CTCSI20 ... For CS2 area
CTCSI13 to CTCSI10 ... For CS1 area
CTCSI03 to CTCSI00 ... For CS0 area

(b) CTCSOn4 to CTCSOn0 (n = 7 to 0) (output)

These are the pins for controlling output to the NU85E502 for each CSn area (n = 7 to 0).

CTCSO74 to CTCSO70 ... For CS7 area
CTCSO64 to CTCSO60 ... For CS6 area
CTCSO54 to CTCSO50 ... For CS5 area
CTCSO44 to CTCSO40 ... For CS4 area
CTCSO34 to CTCSO30 ... For CS3 area
CTCSO24 to CTCSO20 ... For CS2 area
CTCSO14 to CTCSO10 ... For CS1 area
CTCSO04 to CTCSO00 ... For CS0 area

(c) CTLO1 and CTLO0 (output)

These are pins for controlling output to the NU85E502.

(d) MTEN (output)

This is the pin for specifying whether test mode is enabled for the NU85E502.

(e) CT502In1 and CT502In0 (n = 7 to 0) (input)

These are the pins for controlling input from the NU85E502 for each CSn area (n = 7 to 0).

CT502I71 and CT502I70 ... For CS7 area
CT502I61 and CT502I60 ... For CS6 area
CT502I51 and CT502I50 ... For CS5 area
CT502I41 and CT502I40 ... For CS4 area
CT502I31 and CT502I30 ... For CS3 area
CT502I21 and CT502I20 ... For CS2 area
CT502I11 and CT502I10 ... For CS1 area
CT502I01 and CT502I00 ... For CS0 area

(f) CT502On1 and CT502On0 (n = 7 to 0) (output)

These are the pins for controlling output to the NU85E502 for each CSn area (n = 7 to 0).

CT502O71 and CT502O70 ... For CS7 area
CT502O61 and CT502O60 ... For CS6 area
CT502O51 and CT502O50 ... For CS5 area
CT502O41 and CT502O40 ... For CS4 area
CT502O31 and CT502O30 ... For CS3 area
CT502O21 and CT502O20 ... For CS2 area
CT502O11 and CT502O10 ... For CS1 area
CT502O01 and CT502O00 ... For CS0 area

(5) Test mode pins

(a) PHTEST (input)

This is the status input pin, which indicates the test mode status of the memory controller. It is connected to the PHTEST pin of the NB85E.

(b) PHTDIN1 and PHTDIN0 (input)

These are the test input pins.

(c) PHTDO1 and PHTDO0 (output)

These are the test output pins.

(d) VPTCLK (input)

This is the test clock input pin.

(6) NEC reserved pins

(a) MPXEN, CT501In2 to CT501In0 (n = 7 to 0) (input)

These are NEC reserved pins. Be sure to input a low level.

(b) ASTBZ, DSTBZ, MPXCZ, RDCYZ, BUSST, CT501On3 to CT501On0 (n = 7 to 0), BCP, PISL, CTL501, and RWC7 to RWC0 (output)

These are NEC reserved pins. Leave open.

1.3.3 Recommended connection of unused pins

(1/2)

Pin Name		I/O	Recommended Connection Method
NB85E connection pins	VBCLK, VBA25 to VBA0, VBCTYP2 to VBCTYP0, VPRESZ, VBSEQ2 to VBSEQ0, VAACK, VPSTB, VPUBENZ, VPA13 to VPA0, VPWRITE, STPRQ	Input	—
	VAREQ, VBLOCK, VBTTYP1, VBTTYP0, VBBSTR, VDSELPZ, VBWAIT, VBAHLD, VBLAST, STPAK	Output	
	VDCSZ7 to VDCSZ0, VBBENZ3 to VBBENZ0, VBD31 to VBD0, VBWRITE, VBSTZ, VPD15 to VPD0	I/O	
Initialization pins	MCE	Input	Input high level.
	BCPEN	Input	Input low level.
External memory connection pins	A25 to A0, DO31 to DO0[Note 1], RDZ, WRZ3 to WRZ0, IORDZ, IOWRZ, HLDAKZ, DC3 to DC0, CSZ7 to CSZ0, BENZ3 to BENZ0, BCYSTZ, REFRQZ, SDCLK	Output	Leave open.
	D31 to D0[Note 2]	I/O	Connect to bus holder.
	DI31 to DI0[Note 1], SELFREF	Input	Input low level.
	WAITZ, HLDRQZ	Input	Input high level.
NU85E502 connection pins	CTCSI73 to CTCSI70, CTCSI63 to CTCSI60, CTCSI53 to CTCSI50, CTCSI43 to CTCSI40, CTCSI33 to CTCSI30, CTCSI23 to CTCSI20, CTCSI13 to CTCSI10, CTCSI03 to CTCSI00, CT502I71, CT502I70, CT502I61, CT502I60, CT502I51, CT502I50, CT502I41, CT502I40, CT502I31, CT502I30, CT502I21, CT502I20, CT502I11, CT502I10, CT502I01, CT502I00	Input	Input low level.
	CTCSO74 to CTCSO70, CTCSO64 to CTCSO60, CTCSO54 to CTCSO50, CTCSO44 to CTCSO40, CTCSO34 to CTCSO30, CTCSO24 to CTCSO20, CTCSO14 to CTCSO10, CTCSO04 to CTCSO00, CTLO1, CTLO0, MTEN, CT502O71, CT502O70, CT502O61, CT502O60, CT502O51, CT502O50, CT502O41, CT502O40, CT502O31, CT502O30, CT502O21, CT502O20, CT502O11, CT502O10, CT502O01, CT502O00	Output	Leave open.
Test mode pins	PHTEST, PHTDIN1, PHTDIN0, VPTCLK	Input	—
	PHTDO1, PHTDO0	Output	

Notes 1. NU85E500

2. NB85E500

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Pin Name		I/O	Recommended Connection Method
NEC reserved pins	MPXEN, CT501I72 to CT501I70, CT501I62 to CT501I60, CT501I52 to CT501I50, CT501I42 to CT501I40, CT501I32 to CT501I30, CT501I22 to CT501I20, CT501I12 to CT501I10, CT501I02 to CT501I00	Input	Input low level.
	ASTBZ, DSTBZ, MPXCZ, RDCYZ, BUSST, CT501O73 to CT501O70, CT501O63 to CT501O60, CT501O53 to CT501O50, CT501O43 to CT501O40, CT501O33 to CT501O30, CT501O23 to CT501O20, CT501O13 to CT501O10, CT501O03 to CT501O00, BCP, PISL, CTL501, RWC7 to RWC0	Output	Leave open.

1.3.4 Pin status

The following table shows the status in each operating mode of the pins that have output functions.

Table 1-1. Pin Status in Each Operating Mode (1/2)

Pin Name		Pin Status				
		Reset	STOP Mode	HALT Mode	Bus Hold	Test Mode
NB85E connection pins	VDCSZ7 to VDCSZ0	Hi-Z	H	Hi-Z[Note]	H	Hi-Z
	VBBENZ3 to VBBENZ0	Hi-Z	H	Hi-Z[Note]	H	Hi-Z
	VBD31 to VBD0	Hi-Z	Hi-Z	Operating	Hi-Z	Operating
	VBWRITE	Hi-Z	L	Hi-Z[Note]	L	Hi-Z
	VBSTZ	Hi-Z	H	Hi-Z[Note]	H	Hi-Z
	VAREQ	L	H	Operating	H	Operating
	VBLOCK	Hi-Z	H	Hi-Z[Note]	H	Hi-Z
	VBTTYP1, VBTTYP0	Hi-Z	L	Hi-Z[Note]	L	Hi-Z
	VBBSTR	Hi-Z	L	Hi-Z[Note]	L	Hi-Z
	VDSELPZ	Hi-Z	H	Hi-Z[Note]	H	Hi-Z
	VBWAIT	Hi-Z	Hi-Z	Operating	Hi-Z	Operating
	VBAHLD	Hi-Z	Hi-Z	Operating	Hi-Z	Operating
	VBLAST	Hi-Z	Hi-Z	Operating	Hi-Z	Operating
	VPD15 to VPD0	Hi-Z	Hi-Z	Operating	Hi-Z	Operating
	STPAK	L	H	Operating	L	Operating

Note If a refresh occurs in HALT mode and the Nx85E500 becomes the bus master, the same value is output as shown for STOP mode.

Remark L: Low-level output
H: High-level output
Hi-Z: High impedance

Table 1-1. Pin Status in Each Operating Mode (2/2)

Pin Name		Pin Status				
		Reset	STOP Mode	HALT Mode	Bus Hold	Test Mode
External memory connection pins	A25 to A0	Undefined	Maintain	Operating	Maintain	Operating
	D31 to D0[Note 1]	Hi-Z	Hi-Z	Operating	Hi-Z	Operating
	DO31 to DO0[Note 2]	Undefined	Maintain	Operating	Undefined	Operating
	RDZ	H	H	Operating	H	Operating
	WRZ3 to WRZ0	H	H	Operating	H	Operating
	IORDZ	H	H	Operating	H	Operating
	IOWRZ	H	H	Operating	H	Operating
	HLDAKZ	H	H	Operating	L	Operating
	DC3 to DC0	H	H	Operating	H	Operating
	CSZ7 to CSZ0	H	H	Operating	H	Operating
	BENZ3 to BENZ0	H	H	Operating	H	Operating
	BCYSTZ	H	H	Operating	H	Operating
	REFRQZ	H	L	Operating	H[Note 3]	Operating
	SDCLK	Operating	Same as VBCLK	Operating	Operating	Operating

Notes 1. NB85E500. Since these pins will be in a high-impedance state when a reset occurs, take action such as connecting an I/O buffer with a pull-up resistor.

2. NU85E500

3. If there is a refresh request from the NU85E502 during a bus hold, the pin status becomes a low-level output.

Remark L: Low-level output
H: High-level output
Hi-Z: High impedance
Maintain: Maintains the previous status

1.4 Bus Cycle Function

1.4.1 Bus cycle type configuration registers 0 and 1 (BCT0 and BCT1)

The Nx85E500 can connect four types of external memory (when connecting SDRAM, the NU85E502 is necessary).

The BCT0 and BCT1 registers specify the controller and set whether operation is enabled for each CSn area (n = 7 to 0).

The BCT0 and BCT1 registers can be read or written in 16-bit units.

Figure 1-5. Bus Cycle Type Configuration Registers 0 and 1 (BCT0 and BCT1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset
BCT0	ME3	0	BT31	BT30	ME2	0	BT21	BT20	ME1	0	BT11	BT10	ME0	0	BT01	BT00	FFFFF480H	**Note**
BCT1	ME7	0	BT71	BT70	ME6	0	BT61	BT60	ME5	0	BT51	BT50	ME4	0	BT41	BT40	FFFFF482H	**Note**

Bit position	Bit name	Description
15, 11, 7, 3	MEn	Set whether operation of the memory controller is enabled for each CSn area. 0: Operation is disabled (no response to the NB85E) 1: Operation is enabled
13, 12, 9, 8, 5, 4, 1, 0	BTn1, BTn0	Set the type of external memory to be connected for each CSn area.

BTn1	BTn0	External memory type
0	0	SRAM, I/O
0	1	Page ROM
1	0	Setting prohibited
1	1	SDRAM (when the NU85E502 is connected)

Note When a high level is input to the MCE pin: 8888H
When a low level is input to the MCE pin: 0000H

★ **Caution The BTn1 and BTn0 bits of the BCT0 and BCT1 registers should be set immediately after reset, and their settings should not be subsequently changed (except for the MEn bit, which can be changed).**

Remark n = 7 to 0

1.4.2 Address setting wait control register (ASC)

The Nx85E500 can insert address setting wait states at the beginning of an SRAM or page ROM cycle. The number of address setting wait states to be inserted can be set for each CSn area by using the ASC register (n = 7 to 0).

The ASC register can be read or written in 16-bit units.

Remarks 1. The settings of this register are invalid during an SDRAM cycle.

2. The external wait function using the WAITZ input is invalid during an address setting wait period.

Figure 1-6. Address Setting Wait Control Register (ASC)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
ASC	AC7 1	AC7 0	AC6 1	AC6 0	AC5 1	AC5 0	AC4 1	AC4 0	AC3 1	AC3 0	AC2 1	AC2 0	AC1 1	AC1 0	AC0 1	AC0 0	Address FFFFF48AH	After reset FFFFH

Bit position	Bit name	Description
15 to 0	ACn1, ACn0	Set the number of address setting wait states to be inserted before an SRAM or page ROM cycle for each CSn area.

ACn1	ACn0	Number of wait states
0	0	None
0	1	1
1	0	2
1	1	3

Remark n = 7 to 0

1.4.3 Bus cycle control register (BCC)

The Nx85E500 can insert idle states at the end of a read or write cycle of an SRAM or page ROM, and at the end of a read cycle of an SDRAM. The number of idle states to be inserted can be set for each CSn area by using the BCC register (n = 7 to 0).

These idle states are used to guarantee the interval until the external data bus is released by memory. The next bus cycle is started after the idle state(s).

The BCC register can be read or written in 16-bit units.

Remark The settings of this register do not affect the insertion of idle states for access to ROM connected to the V850E fetch bus (VFB) of the NB85E or for access to RAM connected to the V850E data bus (VDB) of the NB85E.

Figure 1-7. Bus Cycle Control Register (BCC)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
BCC	BC7 1	BC7 0	BC6 1	BC6 0	BC5 1	BC5 0	BC4 1	BC4 0	BC3 1	BC3 0	BC2 1	BC2 0	BC1 1	BC1 0	BC0 1	BC0 0	Address FFFFF488H	After reset FFFFH

Bit position	Bit name	Description
15 to 0	BCn1, BCn0	Set the number of idle states to be inserted after a memory read or write cycle for each CSn area.

BCn1	BCn0	Number of idle states
0	0	None
0	1	1
1	0	2
1	1	3

Remark n = 7 to 0

1.4.4 Data wait control registers 0 and 1 (DWC0 and DWC1)

The Nx85E500 can insert programmable data wait states for each CSn area (n = 7 to 0). The DWC0 and DWC1 registers control the data wait states when accessing SRAM, I/O, and page ROM (off-page cycle).

The DWC0 and DWC1 registers can be read or written in 16-bit units.

Remark The programmable wait function using these registers is invalid when accessing ROM that is connected to the V850E fetch bus (VFB) and RAM that is connected to the V850E data bus (VDB) of the NB85E. These areas are always accessed with no waits.

Figure 1-8. Data Wait Control Registers 0 and 1 (DWC0 and DWC1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
DWC0	0	DW32	DW31	DW30	0	DW22	DW21	DW20	0	DW12	DW11	DW10	0	DW02	DW01	DW00	Address FFFFF484H	After reset 7777H
DWC1	0	DW72	DW71	DW70	0	DW62	DW61	DW60	0	DW52	DW51	DW50	0	DW42	DW41	DW40	Address FFFFF486H	After reset 7777H

Bit position	Bit name	Description
14 to 12, 10 to 8, 6 to 4, 2 to 0	DWn2 to DWn0	Set the number of wait states when accessing SRAM, I/O or page ROM for each CSn area.

DWn2	DWn1	DWn0	Number of wait states
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Remark n = 7 to 0

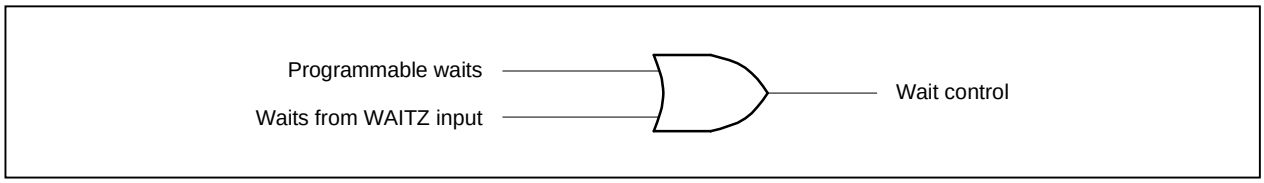
(1) External wait function

When the Nx85E500 is connected to a low-speed device or I/O, or to an asynchronous system, wait states can be inserted in the bus cycle by using the external wait pin (WAITZ).

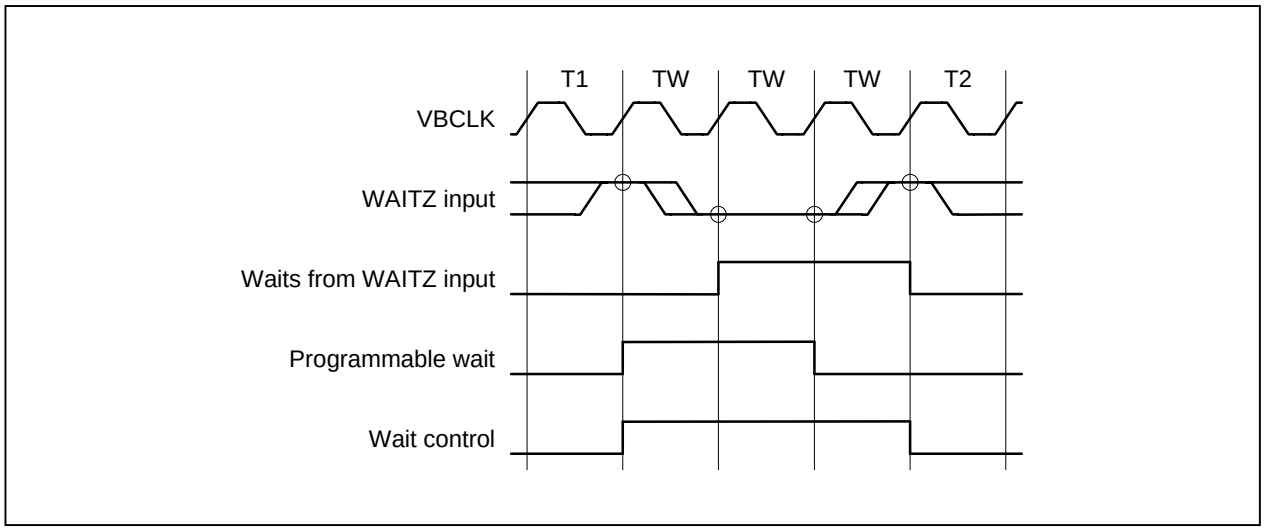
★ The WAITZ input is sampled at the rising edge of the VBCLK signal between the T1 cycle (or TW cycle) and the next cycle, and waits are only inserted in the data wait cycle.

(2) Data wait control registers and external waits

The logical sum (OR) of the number of waits set by data wait control registers 0 and 1 (DWC0 and DWC1) and the number of external waits from the WAITZ input is inserted for the wait cycle. Therefore, the number of wait cycles that are inserted is equal to the larger of these two numbers of waits.



★ For example, when the programmable wait and the WAITZ input are at the following timing, the bus cycle contains 3 waits.



1.4.5 SRAM cycle

(1) Connection example

Figure 1-9. SRAM Connection Example (NB85E500)

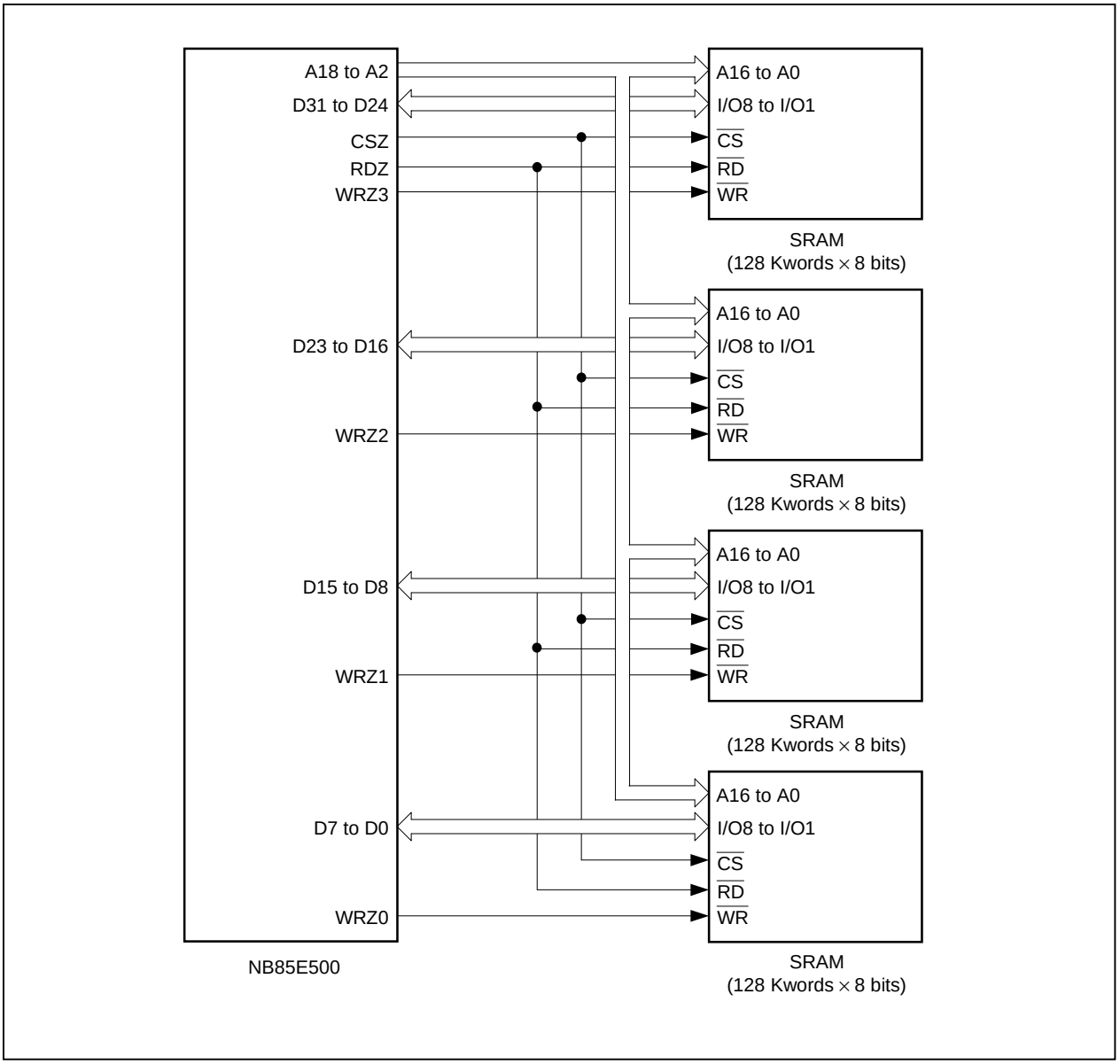
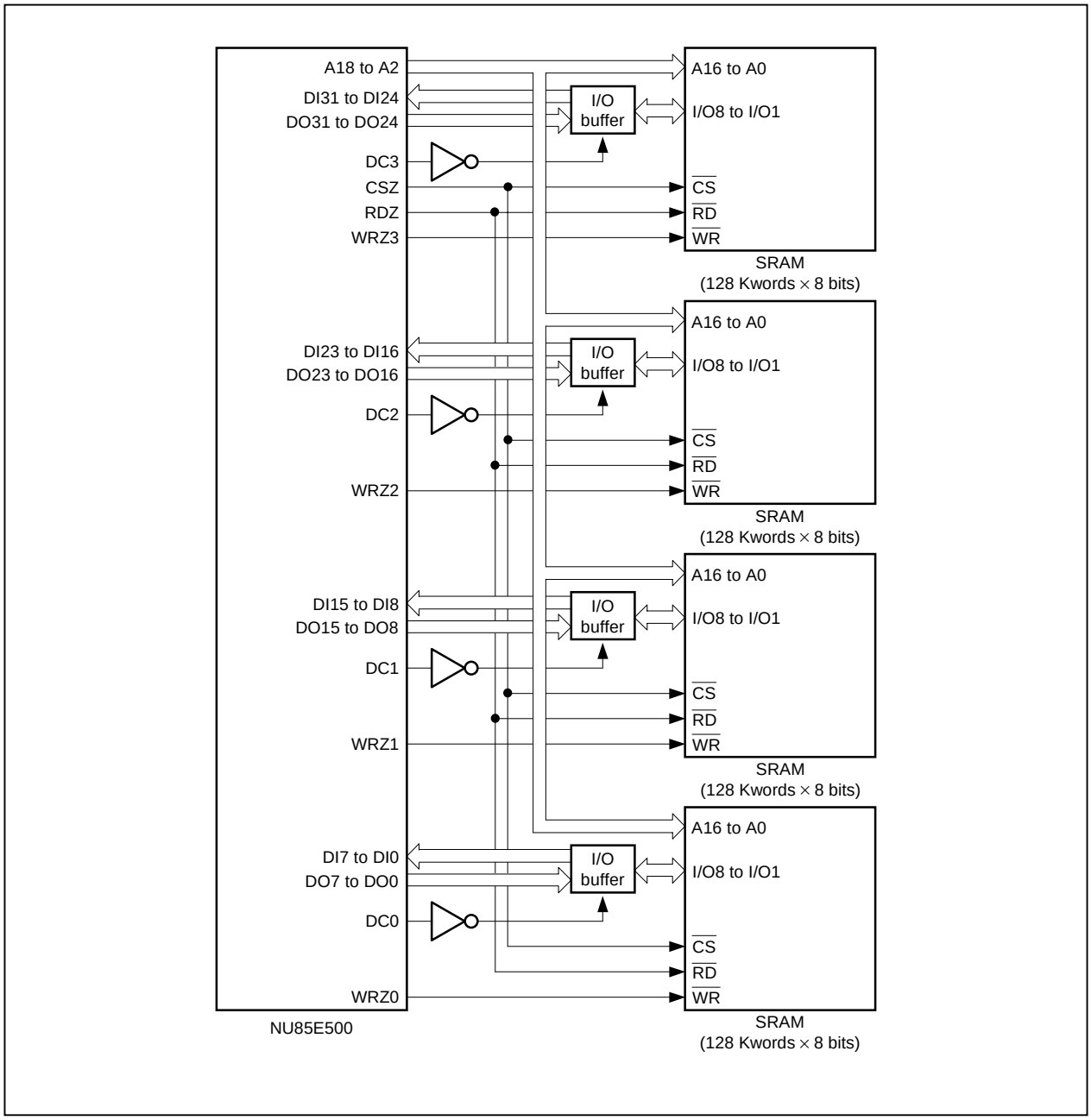


Figure 1-10. SRAM Connection Example (NU85E500)



(2) Bus timing

Examples of the bus timing for an SRAM read or write are shown below. An SRAM bus cycle consists of the following states.

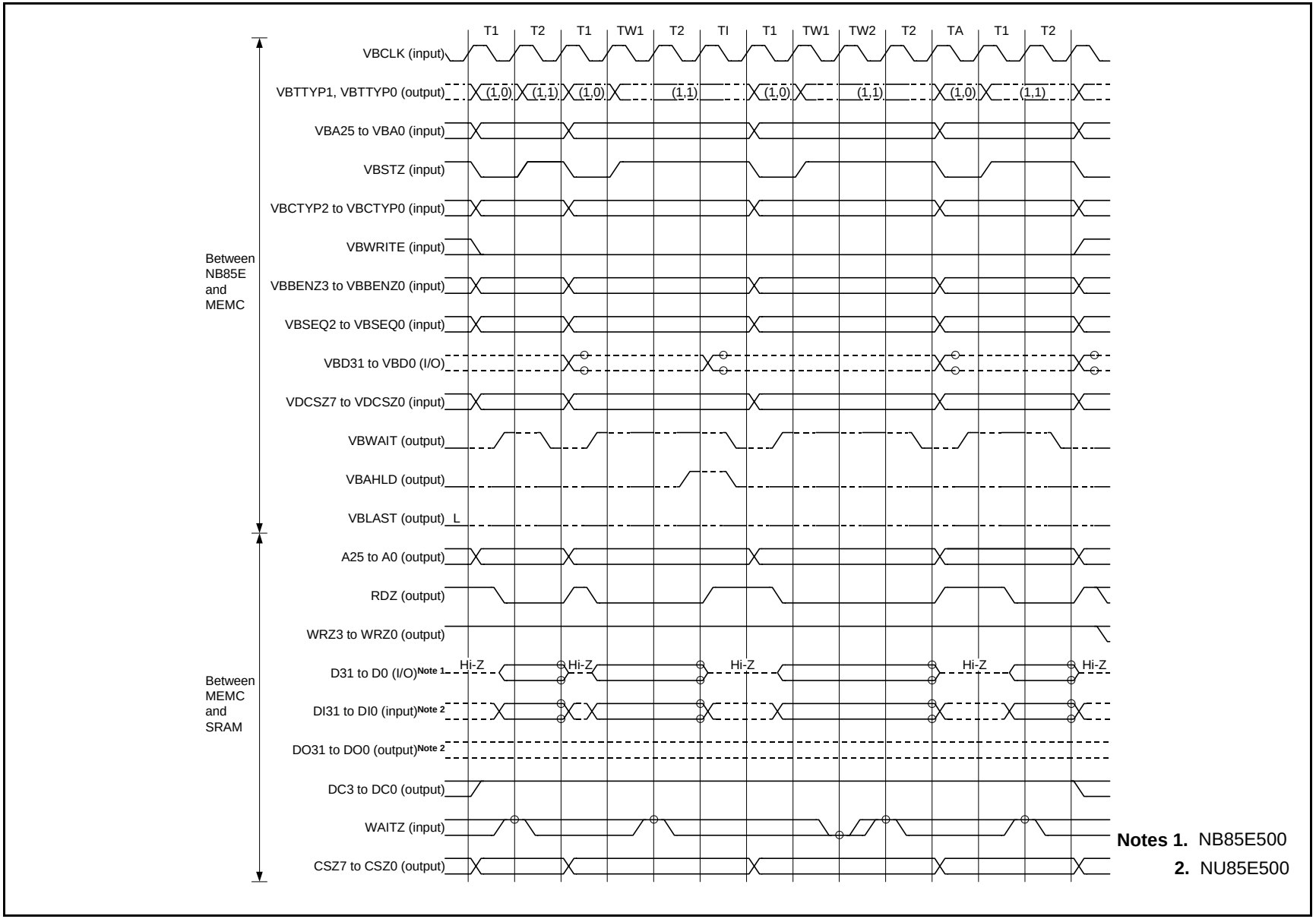
- T1 and T2 states: Basic states for access by the Nx85E500.
- T3 state: Basic state that is added during a flyby transfer.
- TA state: Address setting wait state that is inserted according to the ASC register settings.
- TI state: Idle state that is inserted according to the BCC register settings.
- TW1 state: Wait state that is inserted according to the DWC0 and DWC1 register settings.
- TW2 state: Wait state caused by WAITZ input.

Remarks 1. The broken-line portions of the VBTTYP1, VBTTYP0, VBCTYP2 to VBCTYP0, VBSEQ2 to VBSEQ0, VBD31 to VBD0, VBWAIT, VBAHLD, and VBLAST signals indicate a weak unknown state; a state entered when the NB85E internal bus holder is driving. The level of broken-line portions of the D31 to D0, DI31 to DI0, and DO31 to DO0 signals is undefined (except for the portion indicated by Hi-Z).

2. Circles indicate sampling timing.

3. For details of VSB signals (VBxxx, VDxxx), refer to the **NB85E Hardware User's Manual (A13971E)**.

Figure 1-11. SRAM Read Timing



★ **Figure 1-12. SRAM Write Timing**

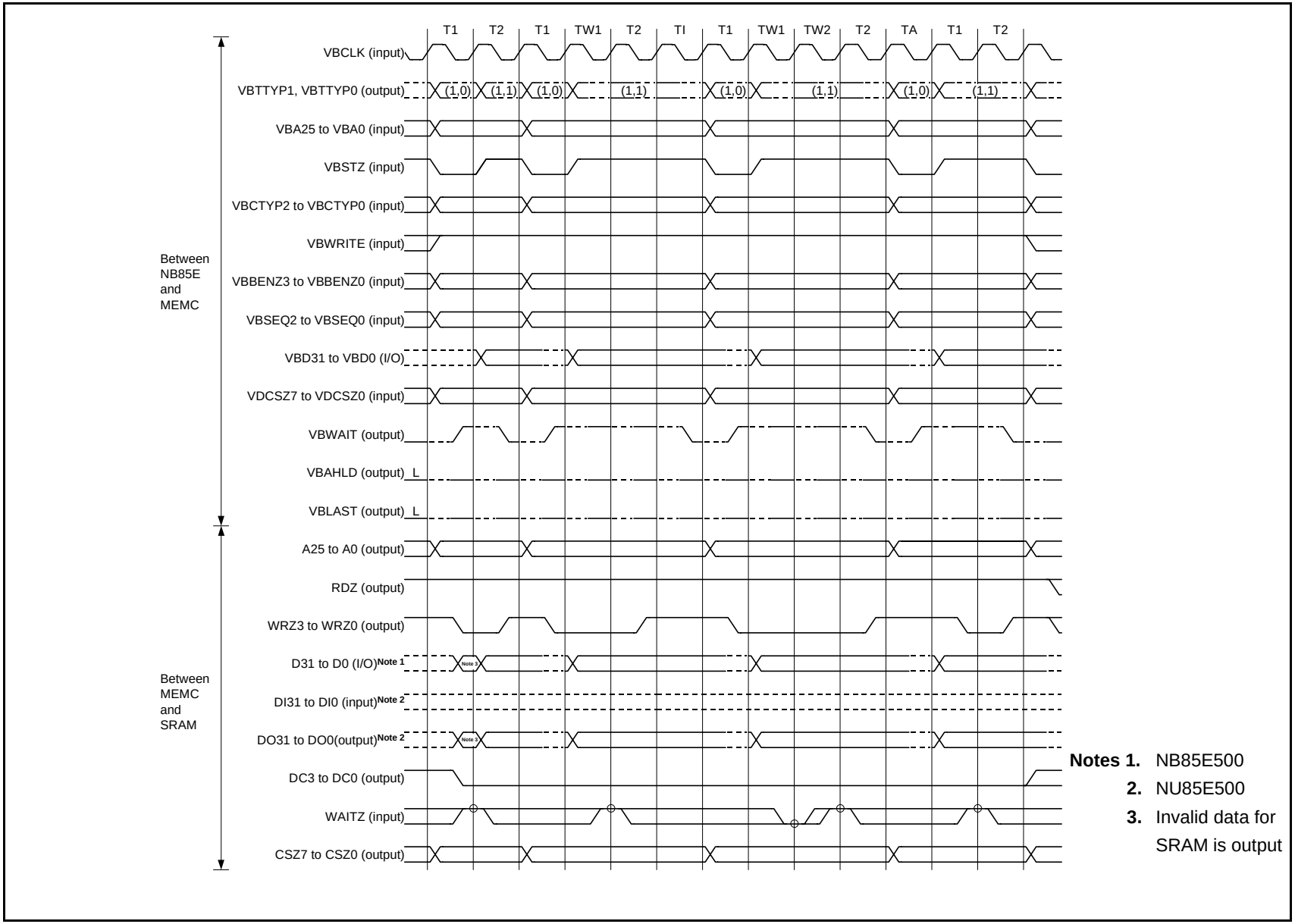
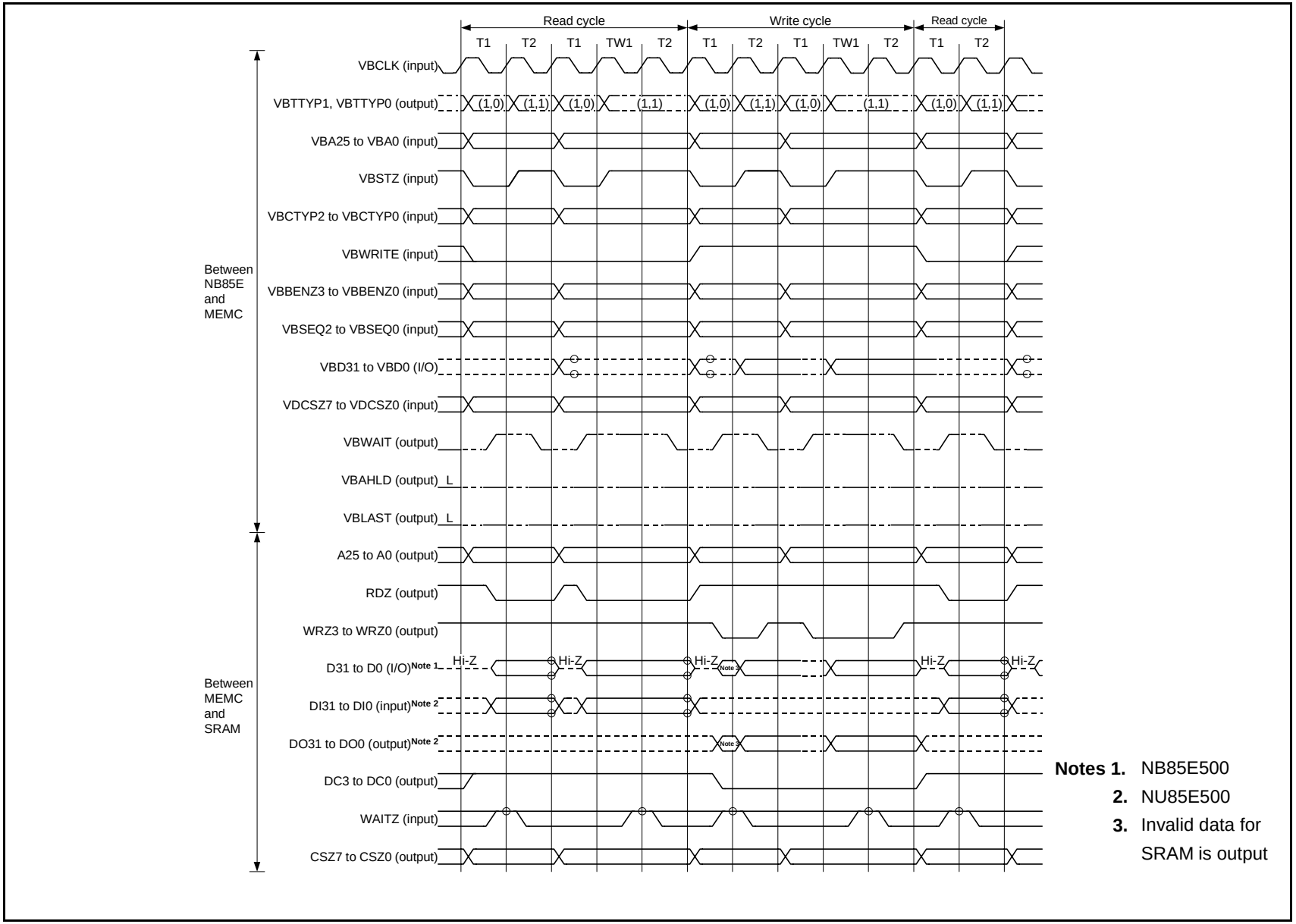


Figure 1-13. SRAM Read/Write Timing



Examples of DMA flyby cycle timing are shown below.

A DMA flyby cycle transfers data between external memory and I/O on a request from the DMA controller in the NB85E.

Figure 1-14. SRAM Flyby Cycle Timing (SRAM → I/O)

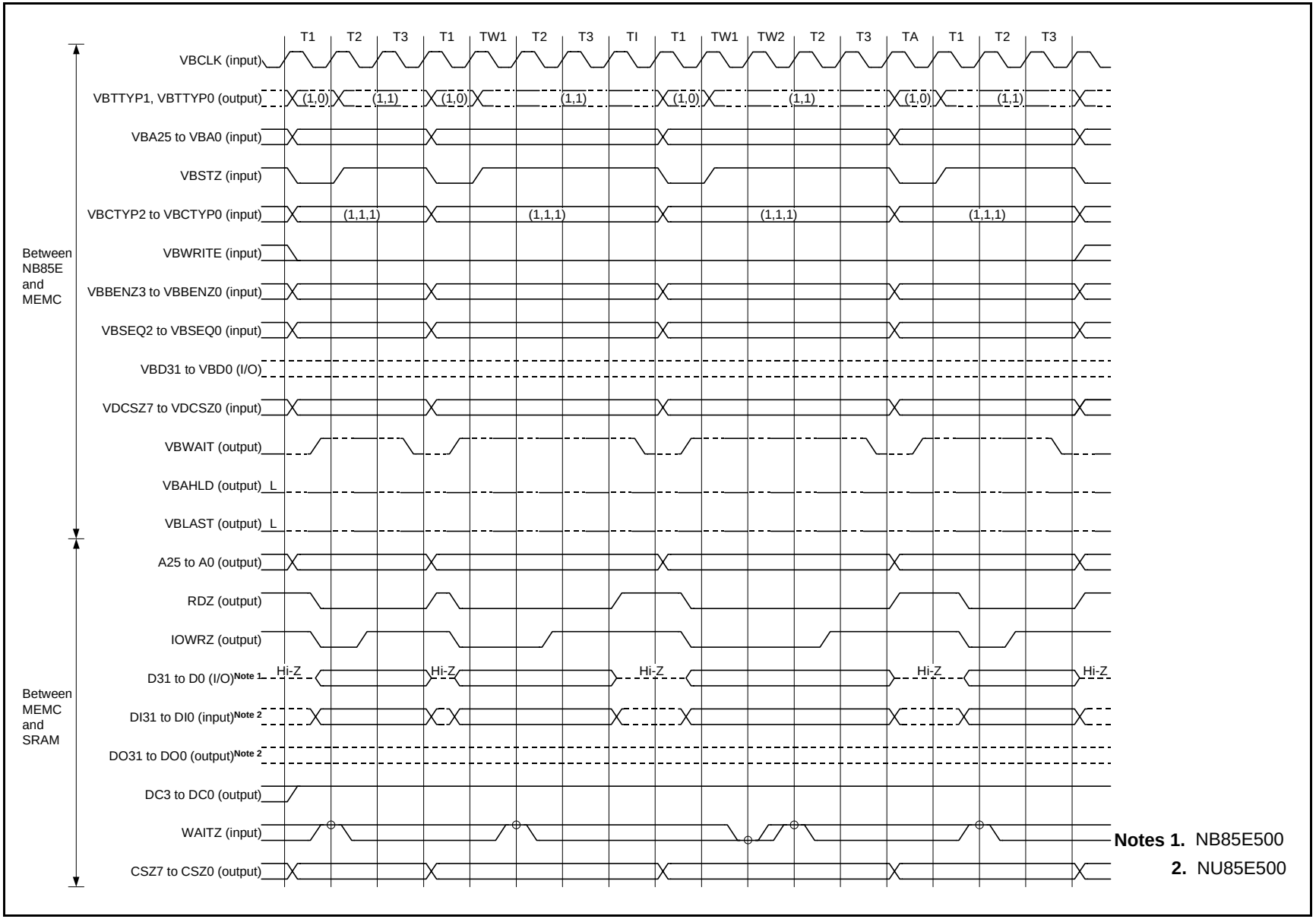
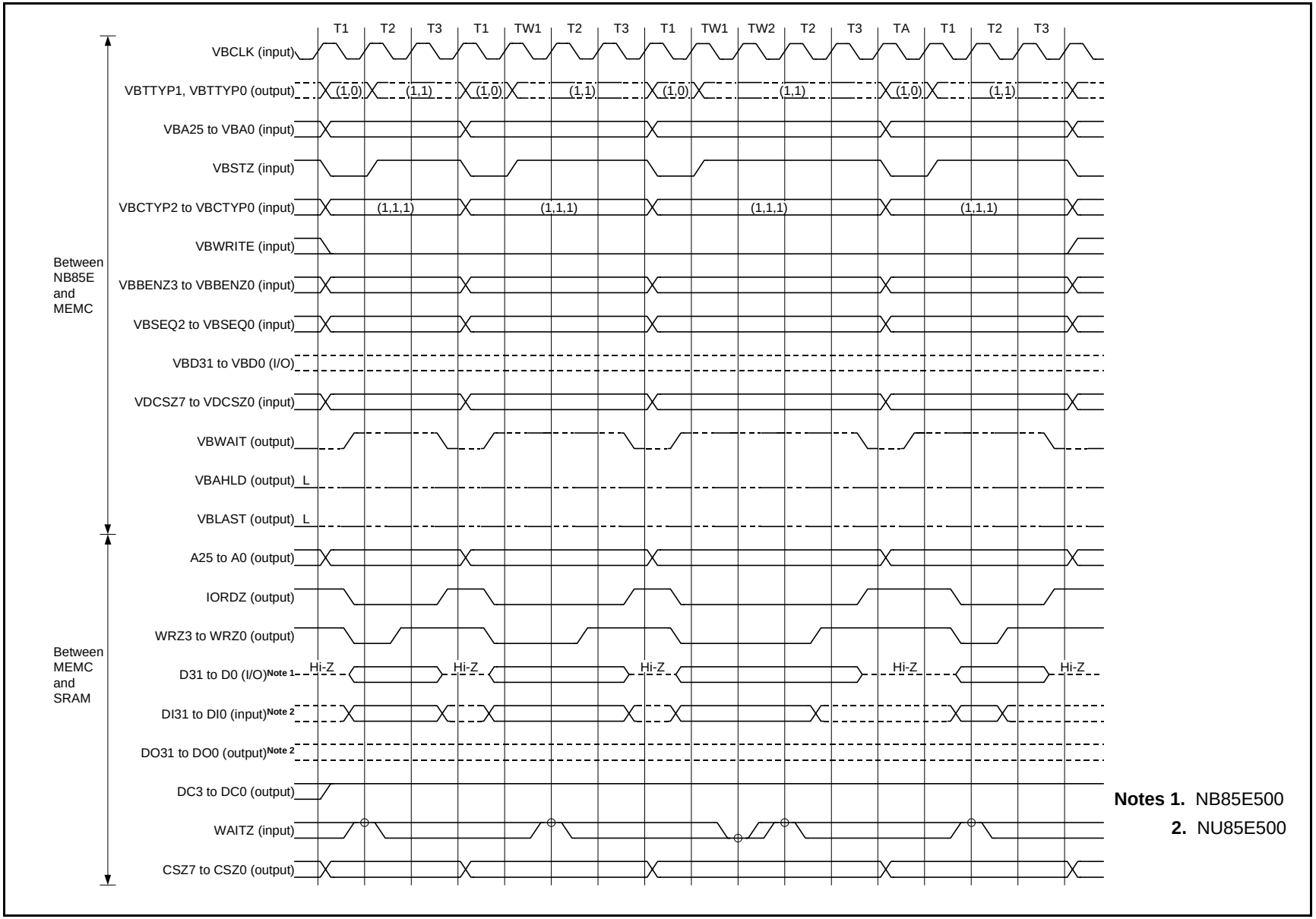


Figure 1-15. SRAM Flyby Cycle Timing (I/O → SRAM)



Notes 1. NB85E500

2. NU85E500

1.4.6 Page ROM configuration register (PRC)

When a page ROM bus cycle occurs, the Nx85E500 judges whether or not it is an on-page access by comparing the address immediately after the page ROM cycle that occurred with the current address.

The address comparison width and the number of wait states during an on-page cycle are set using this register.

This register can be read or written in 16-bit units.

Caution The number of wait states during an off-page cycle is set using the DWC0 and DWC1 registers.

Figure 1-16. Page ROM Configuration Register (PRC) (1/2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset
PRC	0	PRW2	PRW1	PRW0	0	0	0	0	0	0	0	0	MA6	MA5	MA4	MA3	FFFFF49AH	7000H

Bit position	Bit name	Description
14 to 12	PRW2 to PRW0	Set the number of data wait states during a page ROM on-page read cycle.

PRW2	PRW1	PRW0	Number of data wait states
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

★ **Caution The setting values of the DWC0 and DWC1 registers are used to specify for the number of wait states during the first read (off-page read) from the page ROM. Subsequently, if on-page address reading is performed successively, the number of wait states set by the PRW2 to PRW0 bits is employed. Therefore, set the number of wait states that satisfy the off-page read access time of the page ROM to be connected to the DWC0 and DWC1 registers, and set the number of wait states that satisfy the on-page read access time to bits PRW2 to PRW0.**

Figure 1-16. Page ROM Configuration Register (PRC) (2/2)

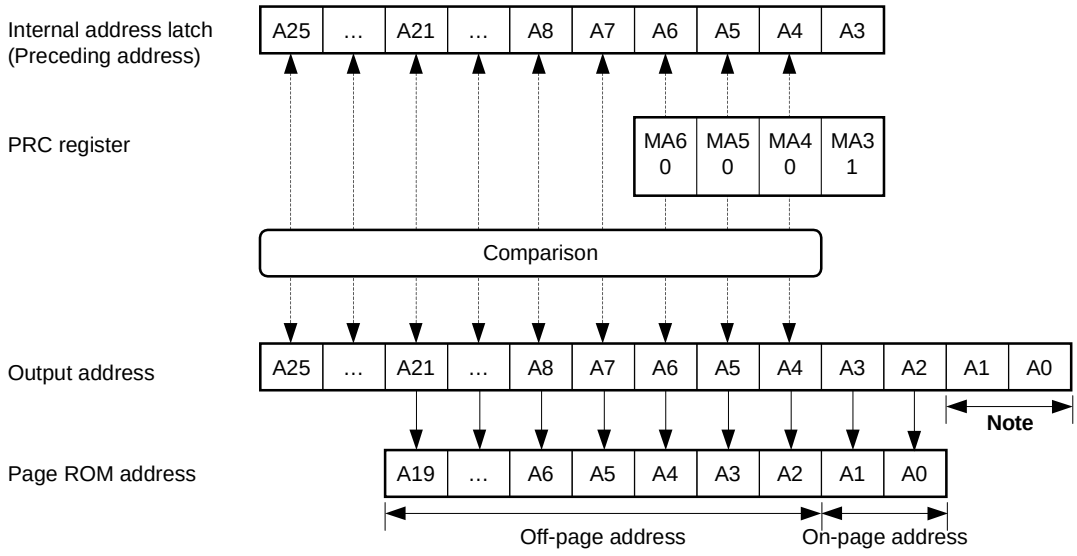
Bit position	Bit name	Description
3 to 0	MA6 to MA3	Set the mask bits for comparing addresses.

MA6	MA5	MA4	MA3	Number of consecutive reads
0	0	0	0	32 bits × 2, 16 bits × 4, 8 bits × 8
0	0	0	1	32 bits × 4, 16 bits × 8, 8 bits × 16
0	0	1	1	32 bits × 8, 16 bits × 16, 8 bits × 32
0	1	1	1	32 bits × 16, 16 bits × 32, 8 bits × 64
1	1	1	1	32 bits × 32, 16 bits × 64, 8 bits × 128

★ **Caution The MA6 to MA3 bits are not used to set the number of consecutive accesses. Set the number of on-page-accessible consecutive reads of the page ROM to be connected to these bits.**

An example of address mask control when four 1 Mword × 8-bit page ROMs are connected is shown below.

Figure 1-17. Example of Control Using Bits MA6 to MA3

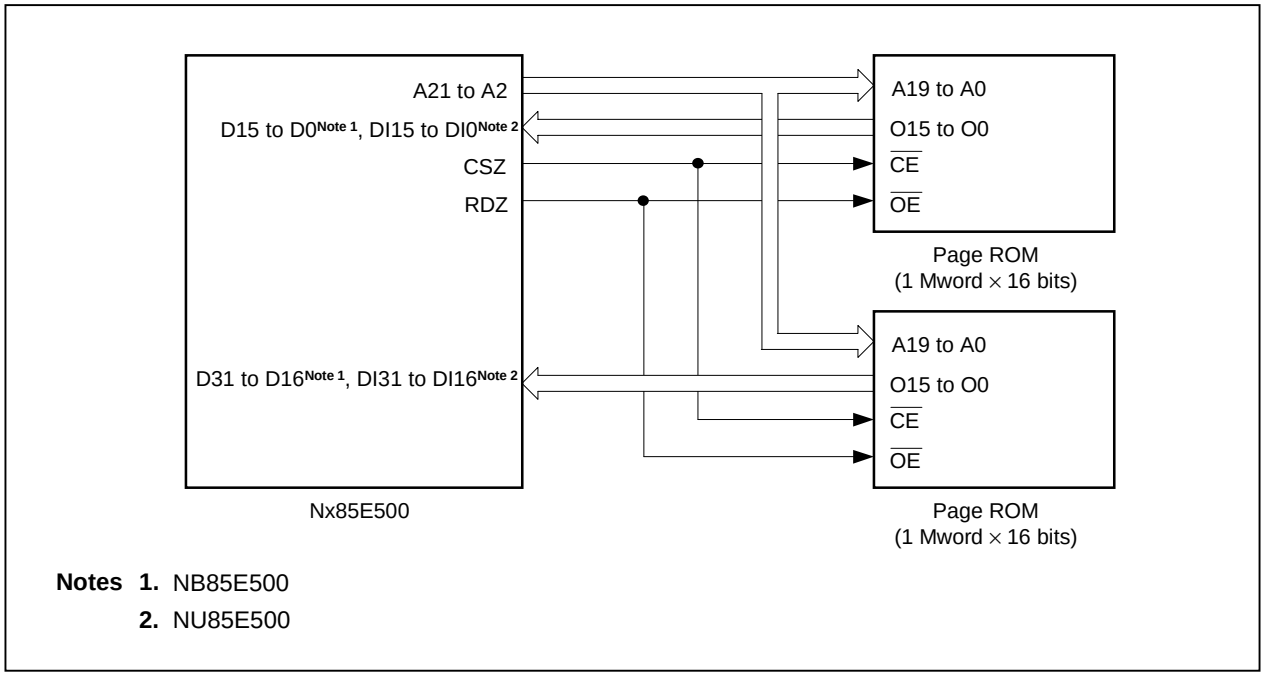


Note Not used for a 32-bit data bus.

1.4.7 Page ROM cycle

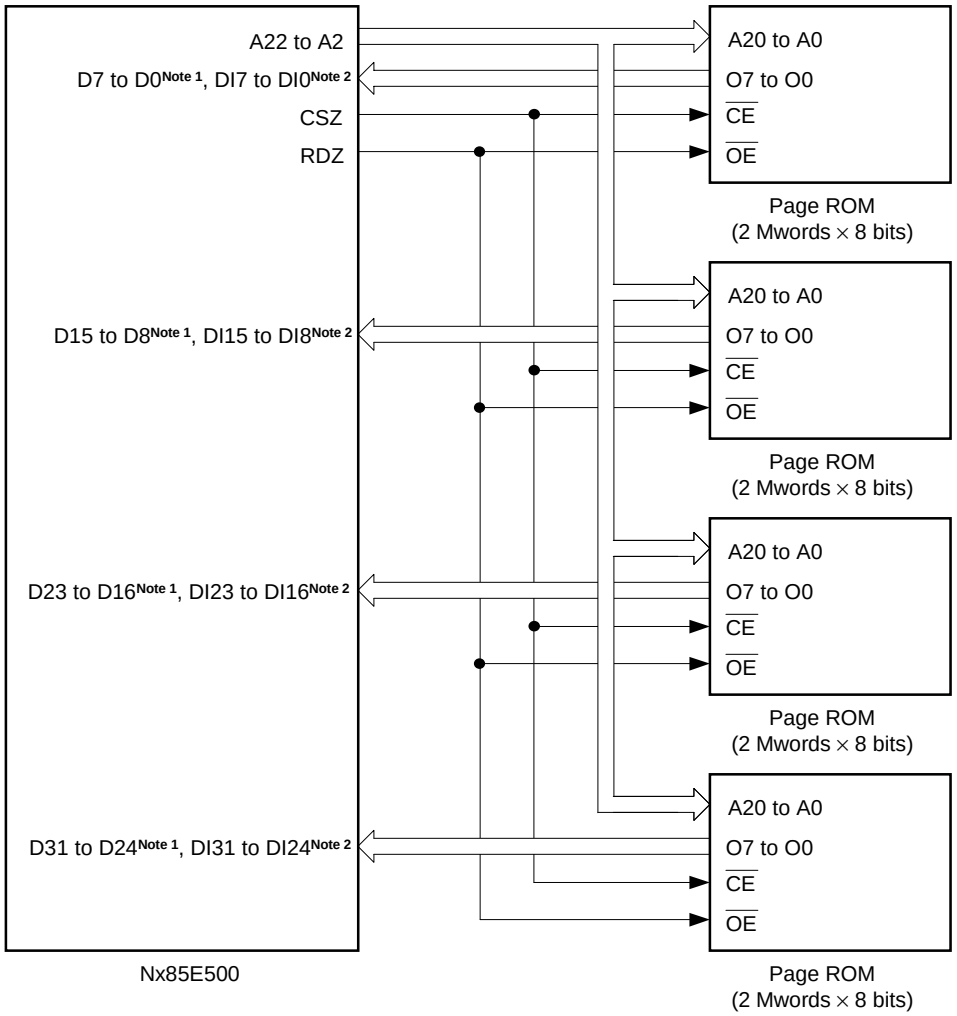
(1) Connection example

Figure 1-18. Page ROM Connection Example (for 16-Bit Data Bus)



Notes 1. NB85E500
2. NU85E500

Figure 1-19. Page ROM Connection Example (for 8-Bit Data Bus)



Notes 1. NB85E500

2. NU85E500

(2) Bus timing

Examples of the bus timing for a page ROM read are shown below. A page ROM bus cycle consists of the following states.

- T1 and T2 states: Basic states for access by the Nx85E500.
- T3 state: Basic state that is added during a flyby transfer.
- TA state: Address setting wait state that is inserted according to the ASC register settings.
- TD state: Dummy state that is inserted when the BCP register's BCP bit = 1.
- TI state: Idle state that is inserted according to the BCC register settings.
- TO1 and TO2 states: Sequential transfer basic states at the time of a page ROM read.
- TW1 state: Wait state that is inserted according to the DWC0 and DWC1 register settings.
- TW2 state: Wait state caused by the WAITZ input.
- TW3 state: Data wait state inserted according to the PRC register settings during a page ROM on-page read cycle.

Remarks 1. The level of broken-line portions indicates a weak unknown state; a state entered when the NB85E internal bus holder is driving (except for the portion indicated by Hi-Z).

2. Circles indicate sampling timing.

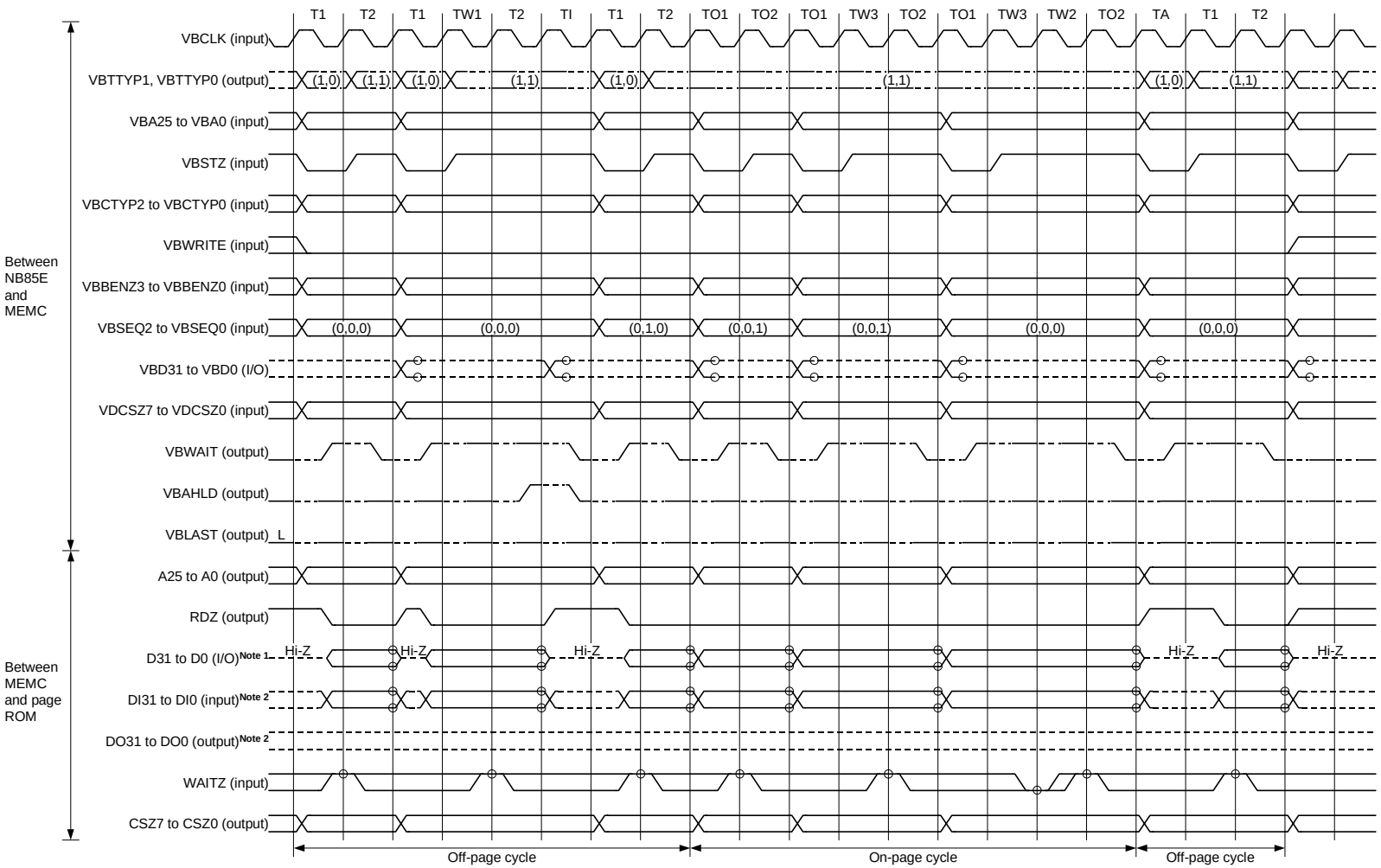
3. For details of VSB signals (VBxxx, VDxxx), refer to the **NB85E Hardware User's Manual (A13971E)**.

★ **Figure 1-20. Page ROM Read Timing (1/2)**

Notes 1. NB85E500

Notes 2. NU85E500

Figure 1-20. Page ROM Read Timing (2/2)

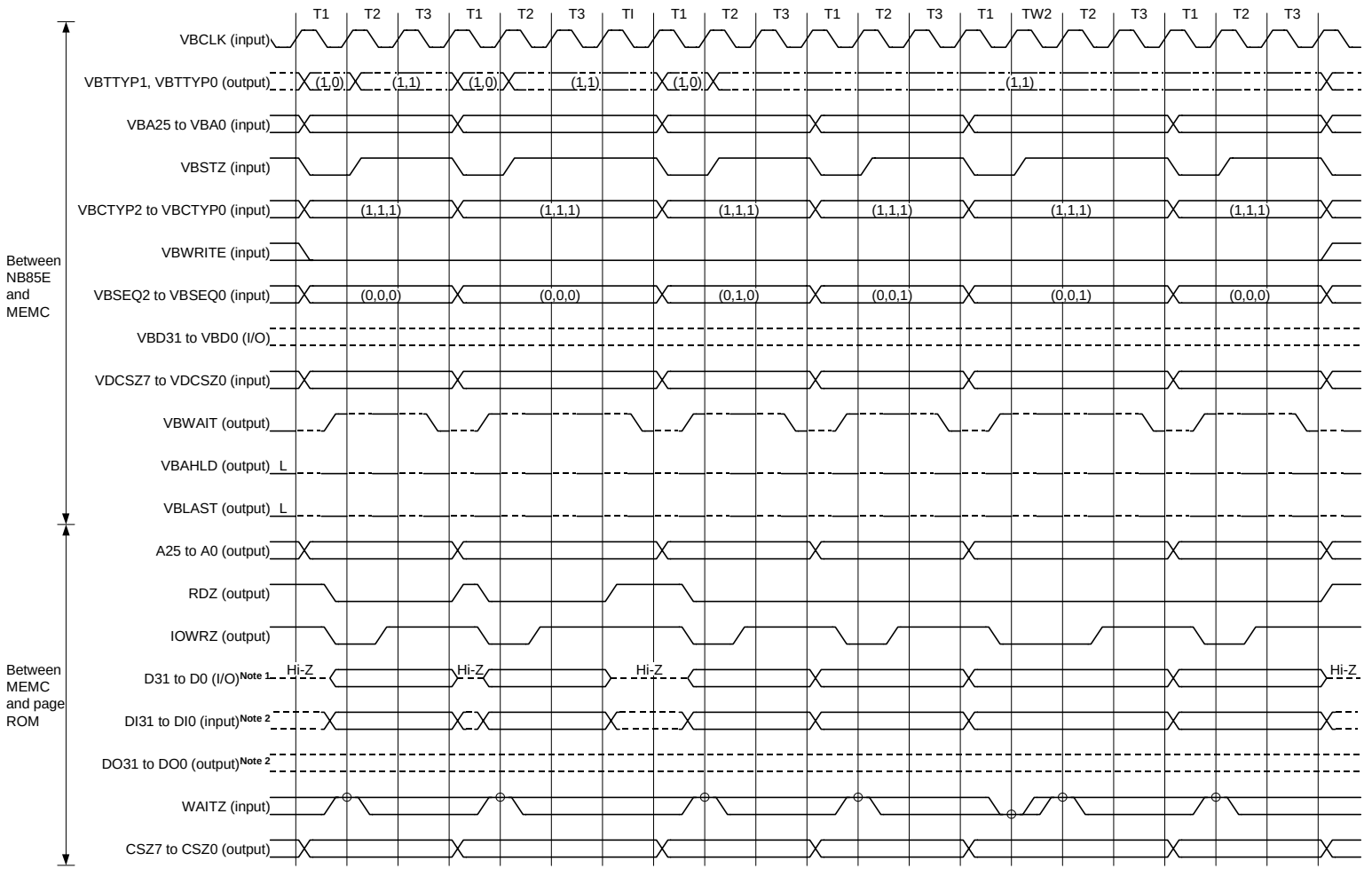


Notes 1. NB85E500

Notes 2. NU85E500

Remark This figure shows the timing when the RDZ signal remains active (low level) during an on-page cycle (only when the VBSEQ2 to VBSEQ0 signals indicate consecutive transfer).

Figure 1-21. Page ROM Flyby Cycle Timing (Page ROM → I/O)



Notes 1. NB85E500

Notes 2. NU85E500

1.4.8 Bus hold function

When the HLDRQZ signal becomes active, the Nx85E500 shifts to the bus hold status. When the transition to the bus hold status is completed, the HLDAKZ signal becomes active. The HLDAKZ signal maintains an active level during a bus hold.

During a bus hold, the bus master of the VSB becomes the external bus master side, and the external memory data bus pins (D31 to D0) of the NB85E500 enter a high-impedance state. Since other external memory connection pins are not in a high-impedance state, design on the user logic side so that signals do not conflict during a bus hold. For details of pin statuses during a bus hold, refer to **Table 1-1 Pin Status in Each Operating Mode**.

When the HLDRQZ signal becomes inactive, the Nx85E500 shifts to the normal status.

(1) Bus hold procedure

★ <1> An external bus hold request signal (HLDRQZ) is input for the Nx85E500 from the external bus master.
<2> The Nx85E500 outputs a VSB mastership request signal (VAREQ) for the NB85E.
<3> The current bus cycle ends.
<4> An acknowledge signal for the VAREQ signal (VAACK) is input to the Nx85E500 from the NB85E.
<5> The Nx85E500 returns an acknowledge signal for the HLDRQZ signal (HLDAKZ) to external memory.

(2) Bus hold release procedure

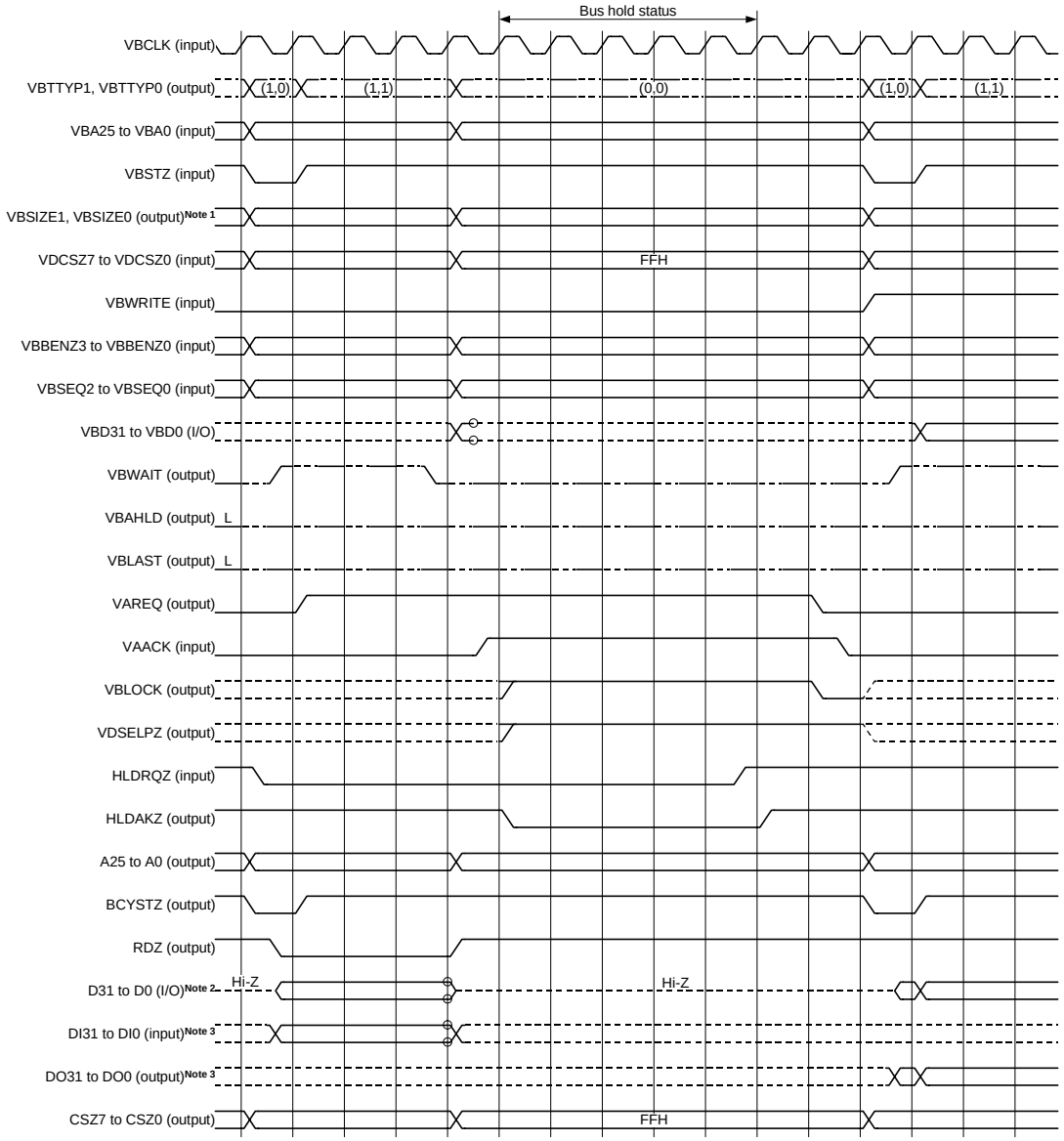
<1> The HLDRQZ signal becomes inactive.
<2> The bus hold request is released externally and the HLDAKZ signal becomes inactive.
★ <3> After the refresh cycle ends if a refresh request has been generated, or immediately if there is no refresh request, the VAREQ signal to the NB85E becomes inactive.
<4> The VAACK signal from the NB85E becomes inactive and the bus hold status ends.
<5> The NB85E becomes the master and a VSB bus cycle begins.

(3) Bus hold timing

An example of bus hold timing is shown below.

Remarks **1.** The level of broken-line portions indicates a weak unknown state; a state entered when the NB85E internal bus holder is driving (except for the portion indicated by Hi-Z).
2. Circles indicate sampling timing.
3. For details of VSB signals (VBxxx, VDxxx), refer to the **NB85E Hardware User's Manual (A13971E)**.

Figure 1-22. Bus Hold Timing



Notes 1. NB85E signal. This signal is not connected to MEMC.

2. NB85E500

3. NU85E500

1.4.9 Bus cycle period control register (BCP)

The Nx85E500 can double the bus cycle period when accessing SRAM or page ROM. Control of the bus cycle period is performed using the BCP register.

When the BCP bit of the BCP register is set (to 1), a dummy state is inserted before each state of the bus cycle.

The BCP register can be read or written in 8-bit or 1-bit units.

★ **Caution This register's settings are only valid when accessing SRAM or page ROM (invalid when accessing SDRAM).**

Figure 1-23. Bus Cycle Period Control Register (BCP)

	7	6	5	4	3	2	1	0	Address	After reset
BCP	BCP	0	0	0	0	0	0	0	FFFFF48CH	**Note**

Bit position	Bit name	Description
7	BCP	Sets the length of the bus cycle period. 0: Normal 1: Double

Note On high-level input to BCPEN pin: 80H
On low-level input to BCPEN pin: 00H

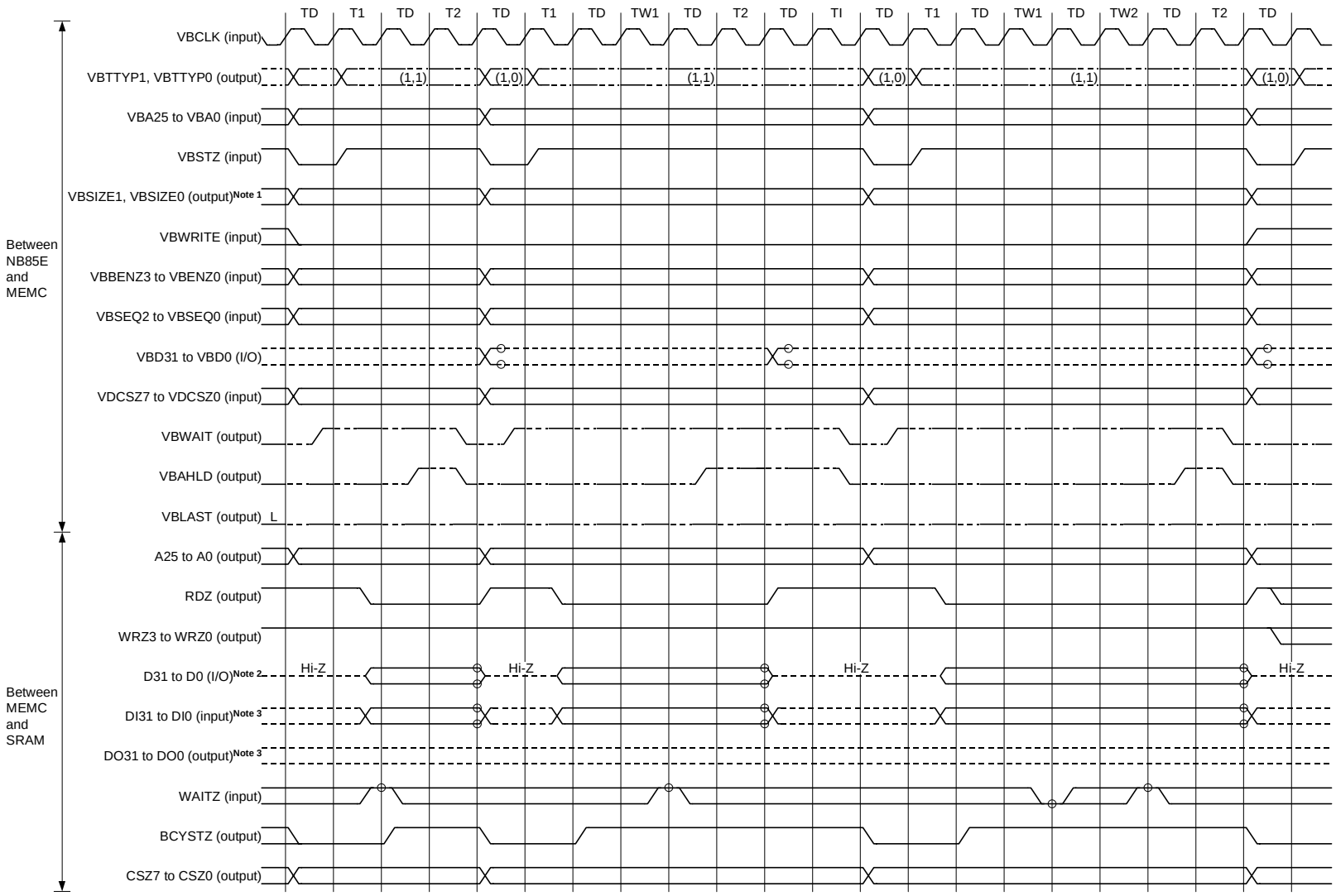
An example of the timing when the bus cycle period is doubled is shown below.

Remarks 1. The level of broken-line portions indicates a weak unknown state; a state entered when the NB85E internal bus holder is driving (except for the portion indicated by Hi-Z).

2. Circles indicate sampling timing.

3. For details of VSB signals (VBxxx, VDxxx), refer to the **NB85E Hardware User's Manual (A13971E)**.

Figure 1-24. SRAM Read Timing (Bus Cycle Period Doubled)



Notes 1. NB85E signal. This signal is not connected to MEMC.

Notes 2. NB85E500

Notes 3. NU85E500

1.4.10 STOP function

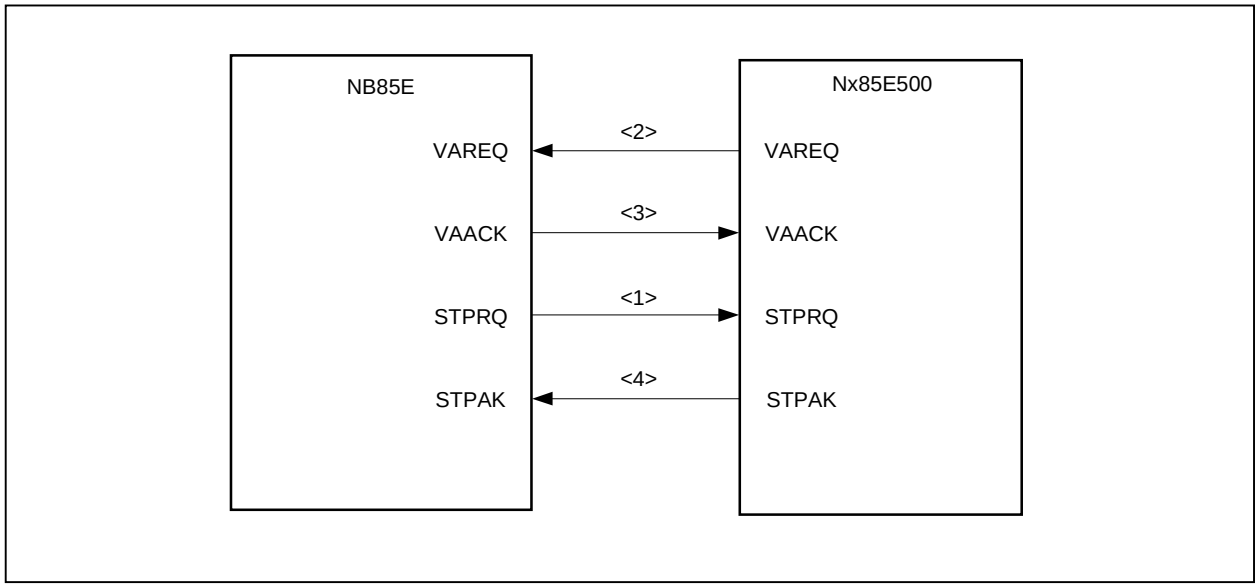
When the NB85E undergoes a transition to STOP mode, the Nx85E500 operates according to the following sequence (see **Figure 1-25**).

<1> When a hardware STOP or software STOP is executed, a STOP mode request signal (STPRQ) is input from the NB85E to the Nx85E500.
<2> The Nx85E500 outputs a VSB mastership request signal (VAREQ) for the NB85E.
<3> An acknowledge signal for the VAREQ signal (VAACK) is input from the NB85E to the Nx85E500.
<4> The Nx85E500 returns an acknowledge signal for the STPRQ signal (STPAK) to the NB85E.

The Nx85E500 returns the STPAK signal no less than two clocks after receiving the STPRQ signal.

Moreover, if an NU85E502 is connected to the Nx85E500, the STPAK signal becomes active after the SDRAM self-refresh cycle is executed.

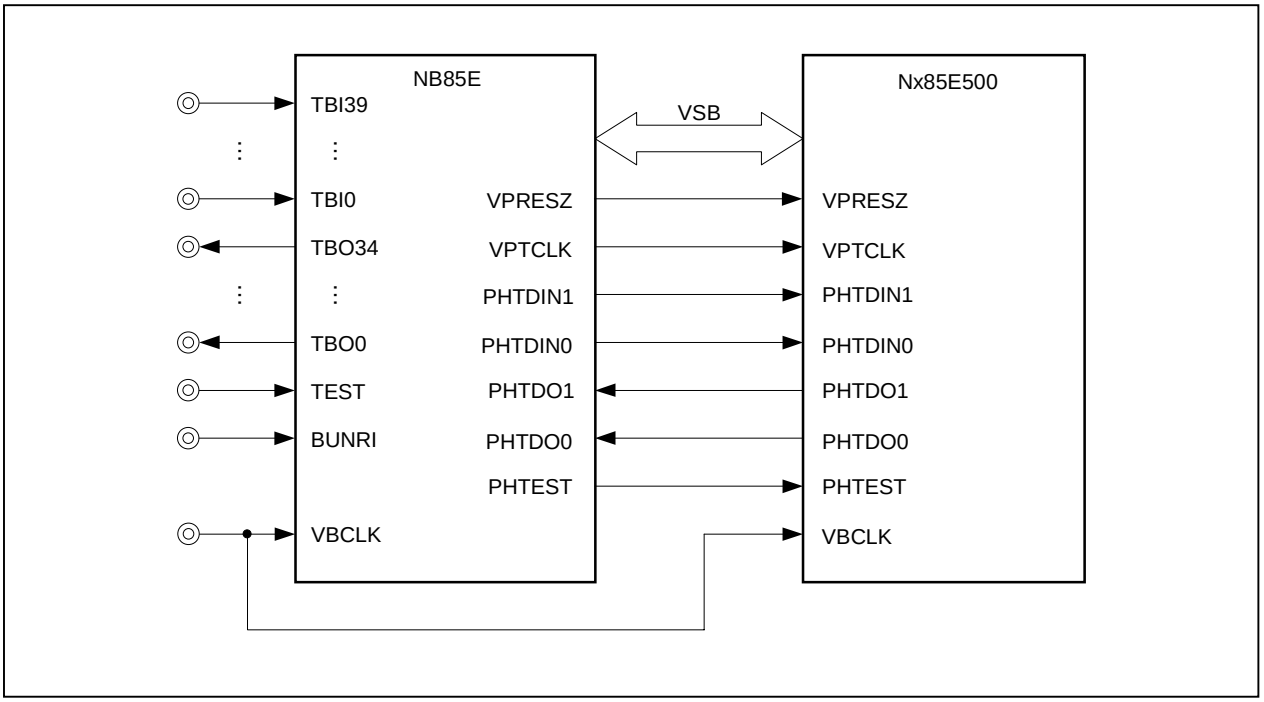
Figure 1-25. Nx85E500 Operation at Time of STOP Mode Transition



1.5 Test Function

The Nx85E500 can be tested using the NB85E test mode.
To test the Nx85E500, connect it to the NB85E as follows.

Figure 1-26. Connection of Nx85E500 to NB85E in Test Mode



Remark For details about test modes, refer to the **NB85E Hardware User's Manual (A13971E)**.

1.5.1 Pin processing when in test mode

(1) External memory connection pins

These operate the same in test mode as in normal mode (Refer to **1.3.4 Pin status** regarding the pin status). If user logic, or SRAM (etc.) is connected to the data bus (D31 to D0[Note 1], DI31 to DI0[Note 2]), data bus signals may conflict when in test mode. In order to avoid this, design on the user logic side so that pins D31 to D0 and DI31 to DI0 are high impedance when in test mode (see **Figures 1-27** and **1-28**).

Make pins other than D31 to D0 and DI31 to DI0 the same as in normal mode. (If they are unused, process them according to **1.3.3 Recommended connection of unused pins**).

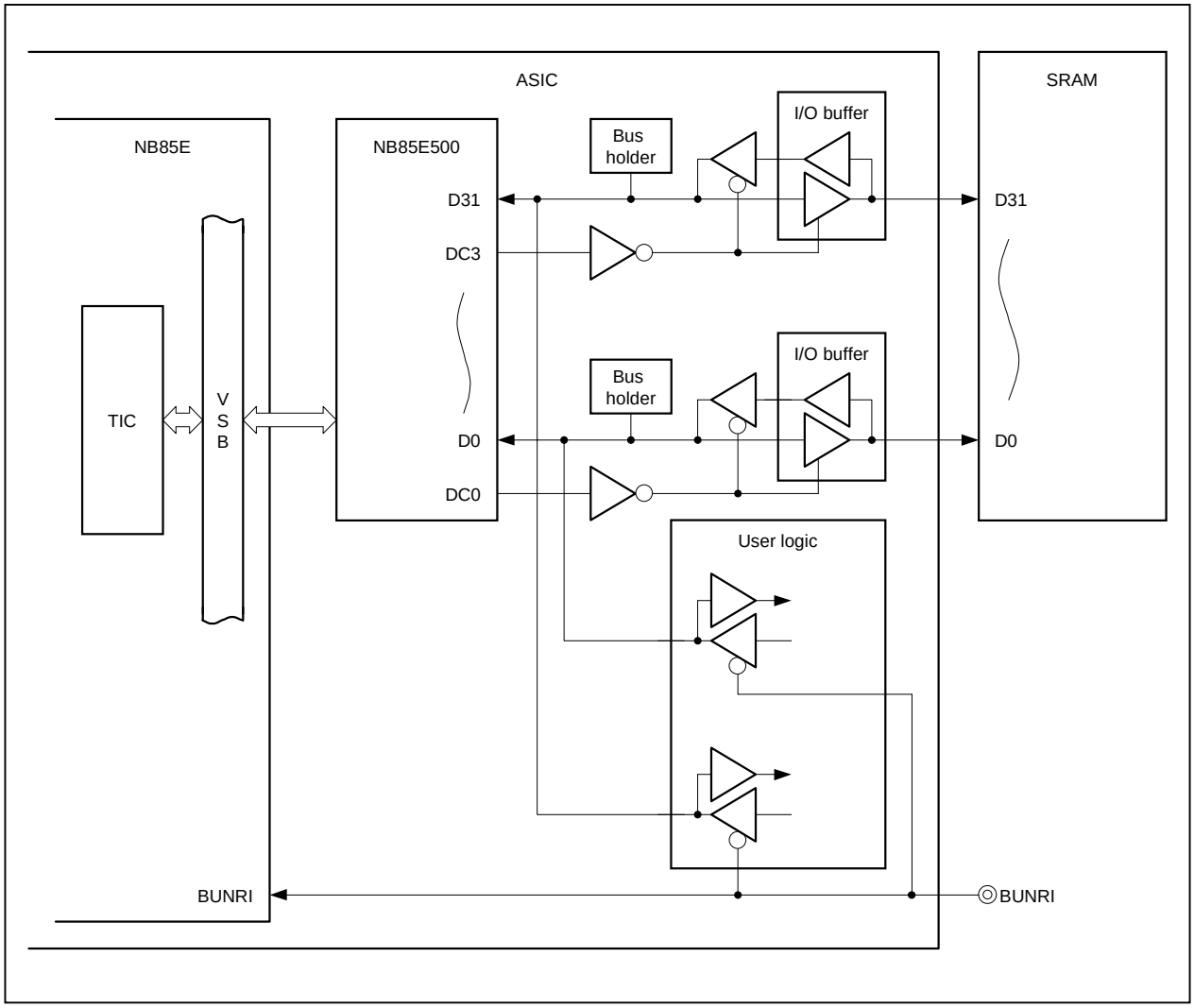
Input pins (HLDRQZ, WAITZ, and SELFREF) are ignored regardless of the values that are input.

Notes 1. NB85E500

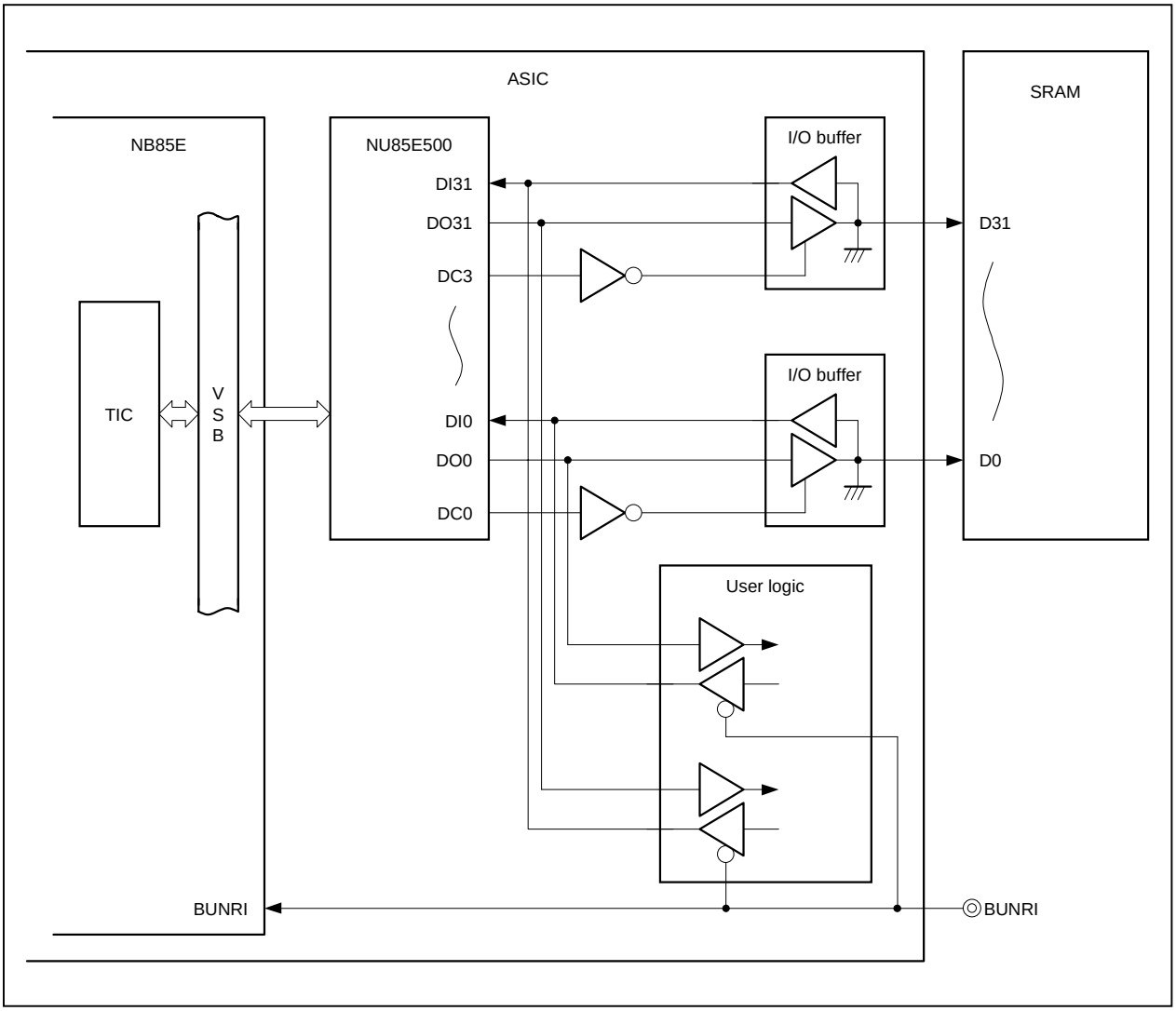
2. NU85E500

Caution Note that the test bus automatic connection tool provided by NEC does not support the NB85E. The test bus connection must be done by the user.

Figure 1-27. User Logic Design Example (NB85E500)



★ **Figure 1-28. User Logic Design Example (NU85E500)**



(2) Test mode pins

Connect test mode pins to the NB85E as shown in Figure 1-26.

(3) Other pins

Make other pins the same as in normal mode. (If they are unused, process them according to **1.3.3 Recommended connection of unused pins**.) Refer to **1.3.4 Pin status** regarding the pin status.

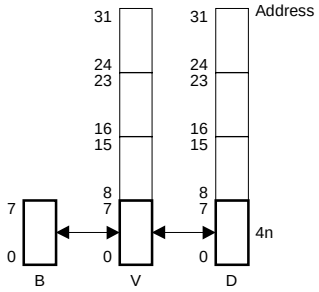
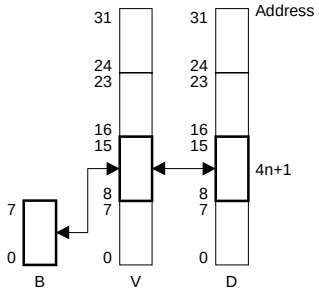
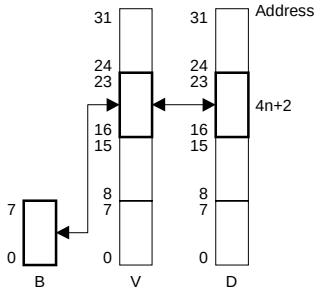
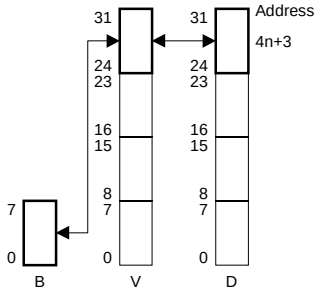
1.6 Data Flow

The flow of data transfer to external memory differs according to the register settings, starting addresses, and data width.

Data flows are shown below for each condition.

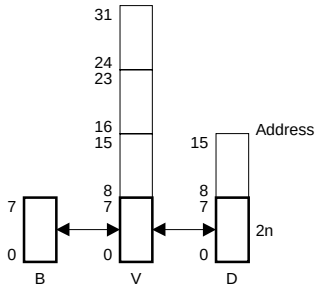
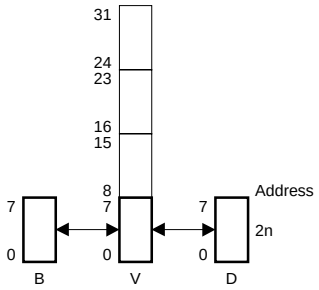
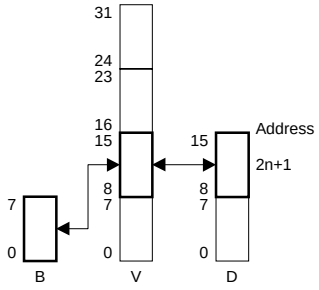
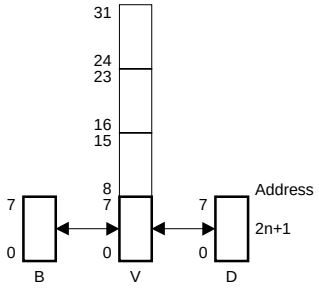
1.6.1 Data flow for byte access (8 bits)

Figure 1-29. Byte Access (Little Endian) (1/2)

Address to Be Accessed	Data Transfer Flow
	External Data Bus: 32 Bits
4n	
4n + 1	
4n + 2	
4n + 3	

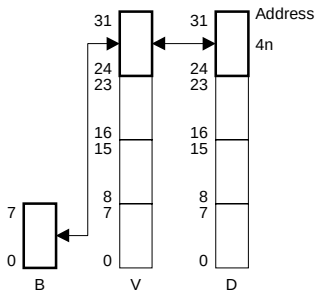
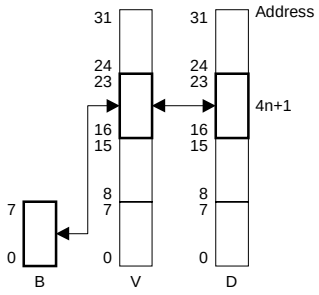
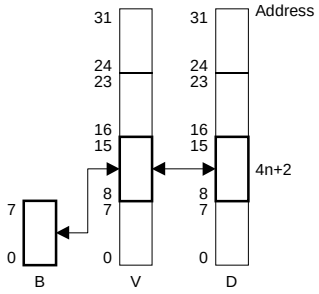
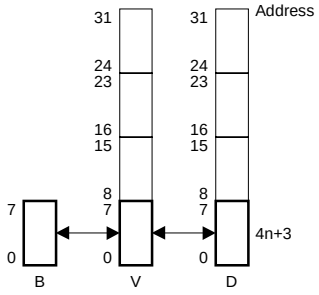
Remark B: Byte data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-29. Byte Access (Little Endian) (2/2)

Address to Be Accessed	Data Transfer Flow	
	External Data Bus: 16 Bits	External Data Bus: 8 Bits
2n		
2n + 1		

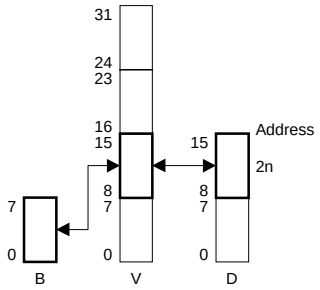
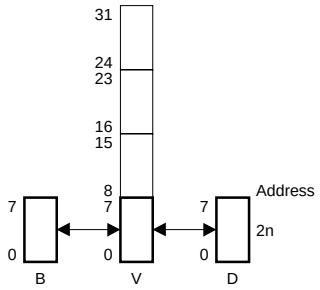
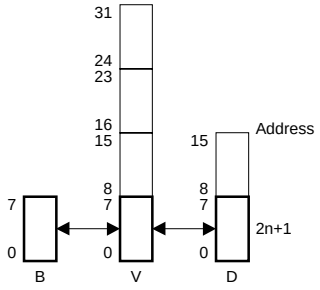
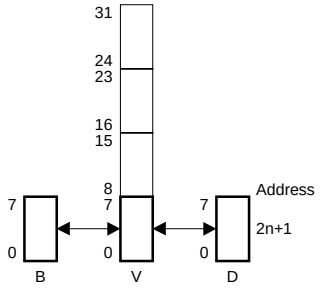
Remark B: Byte data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-30. Byte Access (Big Endian) (1/2)

Address to Be Accessed	Data Transfer Flow External Data Bus: 32 Bits
4n	
4n + 1	
4n + 2	
4n + 3	

Remark B: Byte data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-30. Byte Access (Big Endian) (2/2)

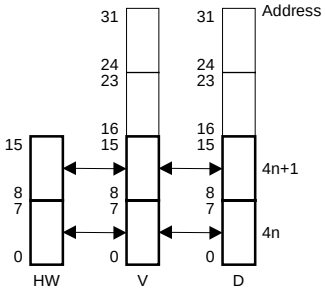
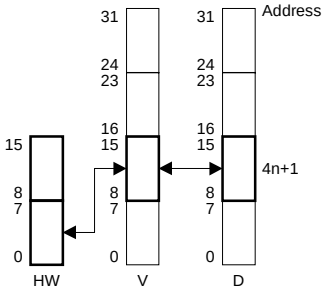
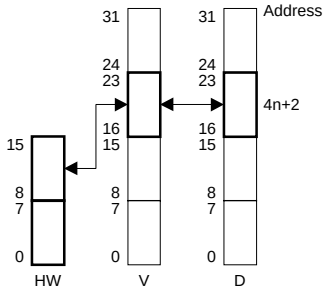
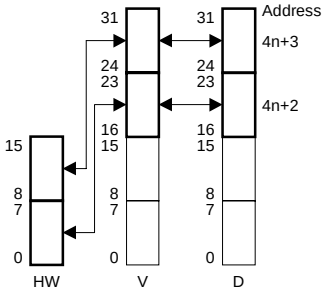
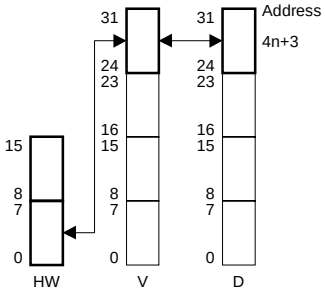
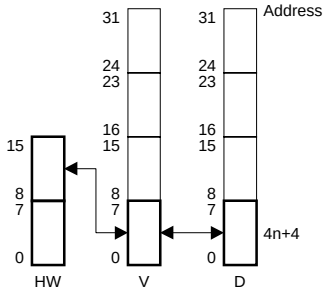
Address to Be Accessed	Data Transfer Flow	
	External Data Bus: 16 Bits	External Data Bus: 8 Bits
2n		
2n + 1		

Remark B: Byte data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

1.6.2 Data flow for halfword access (16 bits)

Figure 1-31. Halfword Access (Little Endian) (1/2)

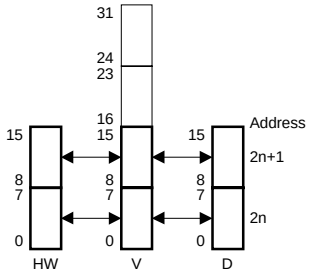
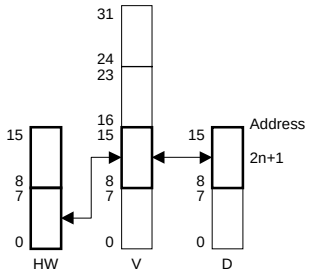
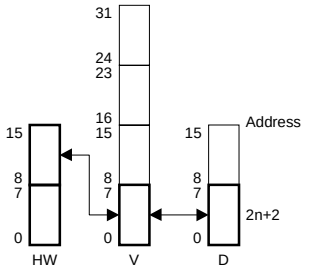
(a) External data bus: 32 bits

Address to Be Accessed	Data Transfer Flow	
	First Time	Second Time
4n		—
4n + 1		
4n + 2		—
4n + 3		

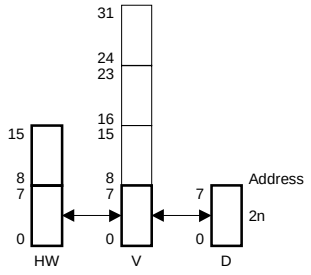
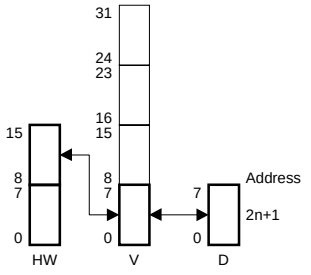
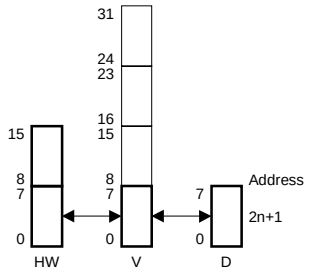
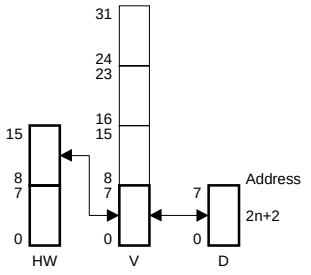
Remark HW: Halfword data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-31. Halfword Access (Little Endian) (2/2)

(b) External data bus: 16 bits

Address to Be Accessed	Data Transfer Flow	
	First Time	Second Time
2n		—
2n + 1		

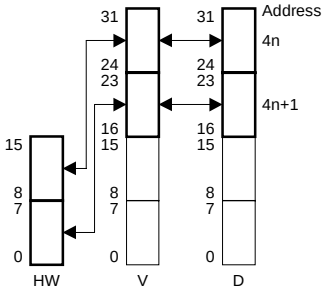
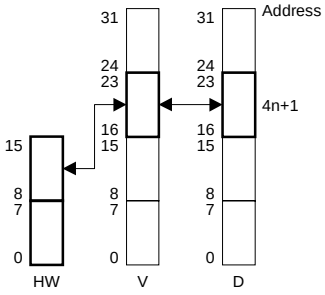
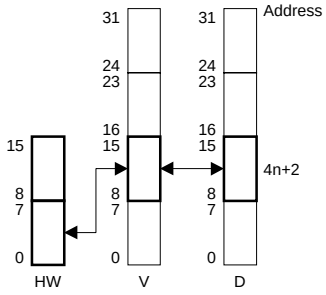
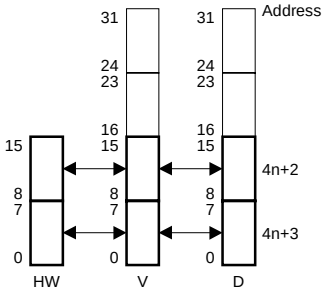
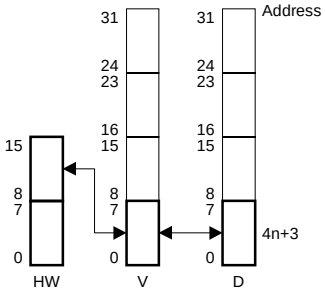
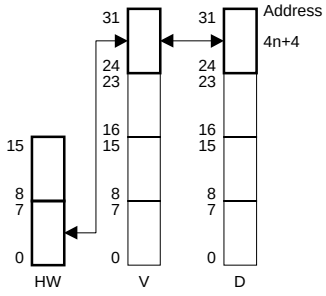
(c) External data bus: 8 bits

Address to Be Accessed	Data Transfer Flow	
	First Time	Second Time
2n		
2n + 1		

Remark HW: Halfword data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-32. Halfword Access (Big Endian) (1/2)

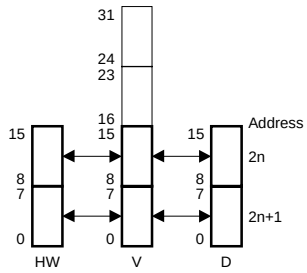
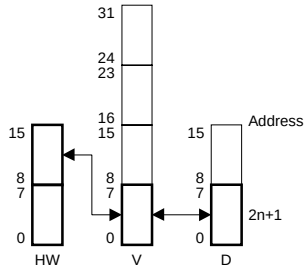
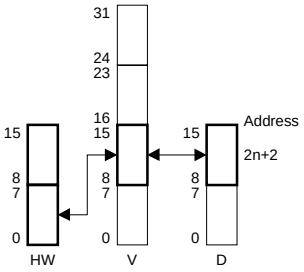
(a) External data bus: 32 bits

Address to Be Accessed	Data Transfer Flow	
	First Time	Second Time
4n		—
4n + 1		
4n + 2		—
4n + 3		

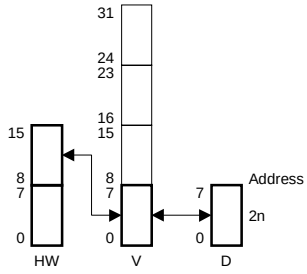
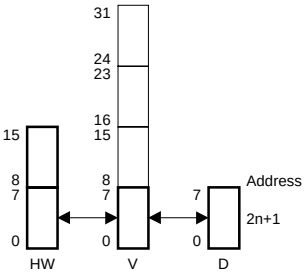
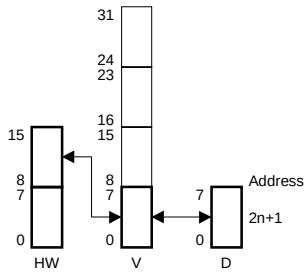
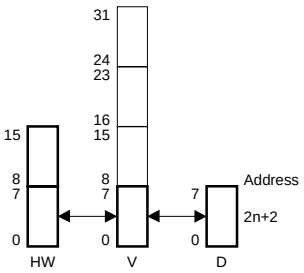
Remark HW: Halfword data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-32. Halfword Access (Big Endian) (2/2)

(b) External data bus: 16 bits

Address to Be Accessed	Data Transfer Flow	
	First Time	Second Time
2n		—
2n + 1		

(c) External data bus: 8 bits

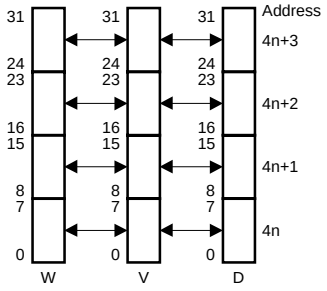
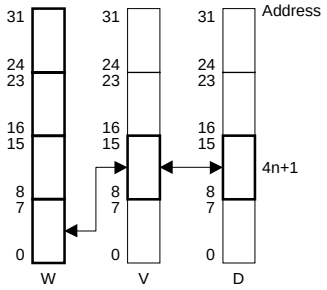
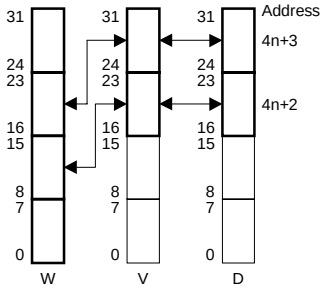
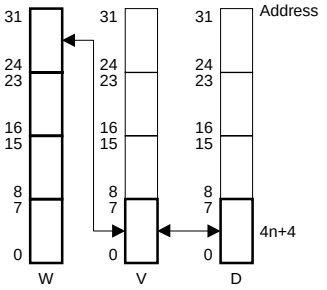
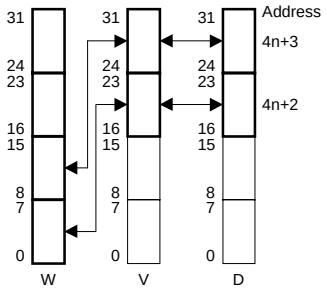
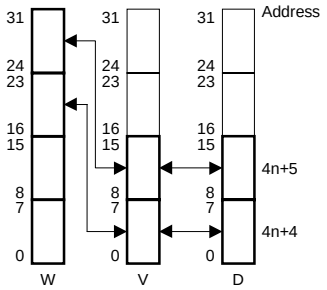
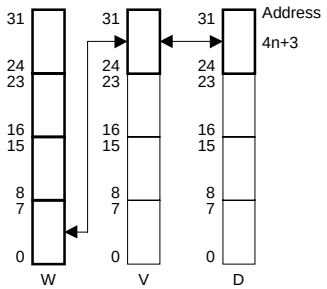
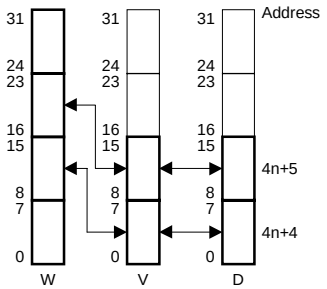
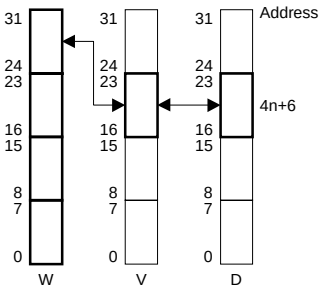
Address to Be Accessed	Data Transfer Flow	
	First Time	Second Time
2n		
2n + 1		

Remark HW: Halfword data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

1.6.3 Data flow for word access (32 bits)

Figure 1-33. Word Access (Little Endian) (1/3)

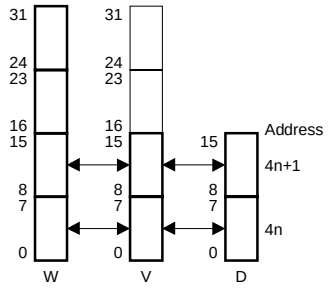
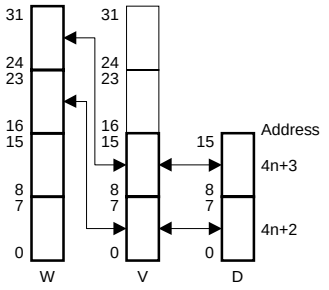
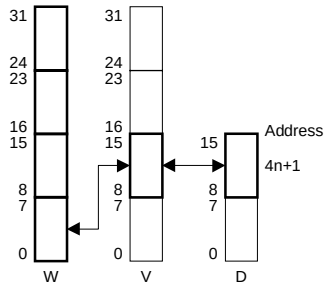
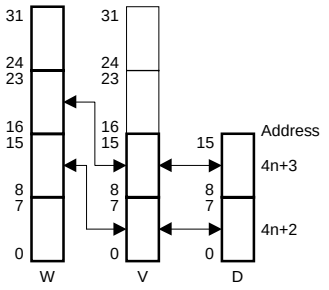
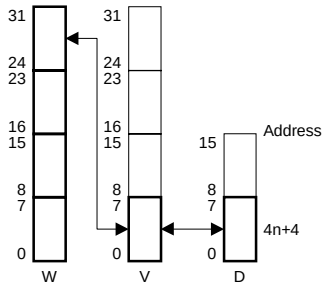
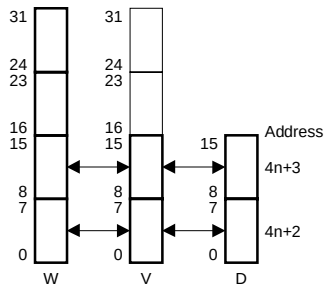
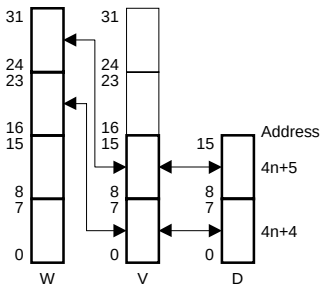
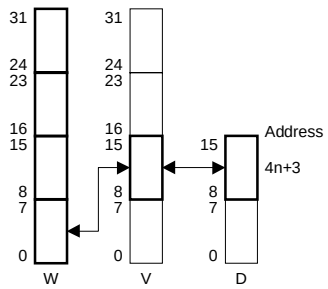
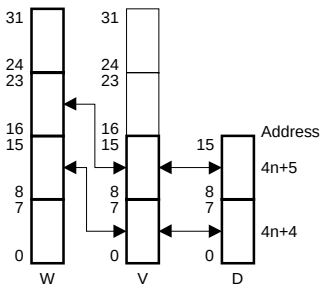
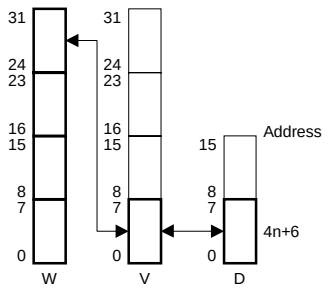
(a) External data bus: 32 bits

Address to Be Accessed	Data Transfer Flow		
	First Time	Second Time	Third Time
4n		—	—
4n + 1			
4n + 2			—
4n + 3			

Remark W: Word data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-33. Word Access (Little Endian) (2/3)

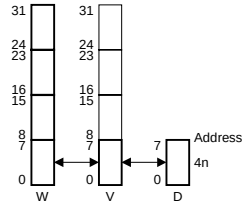
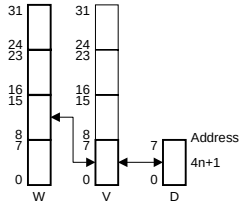
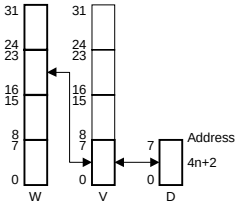
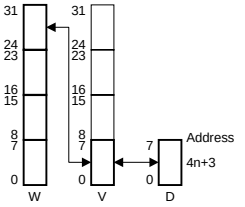
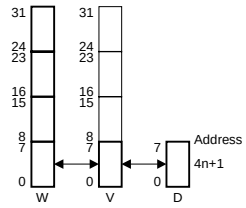
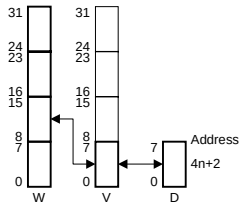
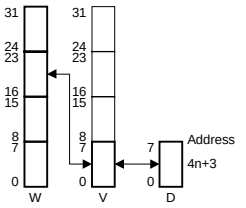
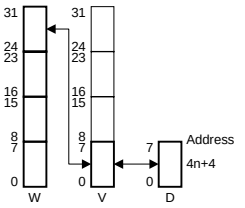
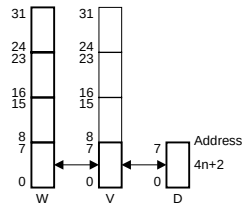
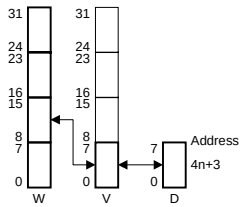
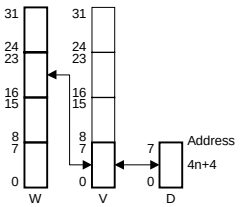
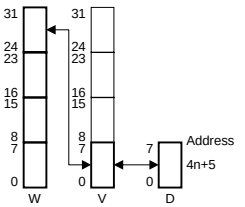
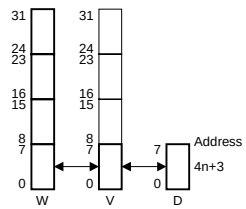
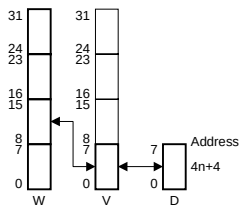
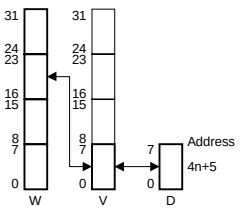
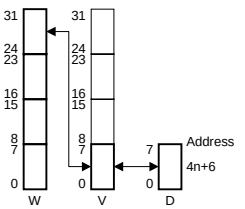
(b) External data bus: 16 bits

Address to Be Accessed	Data Transfer Flow		
	First Time	Second Time	Third Time
4n			—
4n + 1			
4n + 2			—
4n + 3			

Remark W: Word data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-33. Word Access (Little Endian) (3/3)

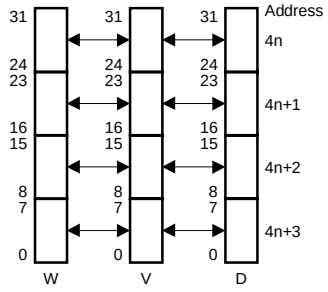
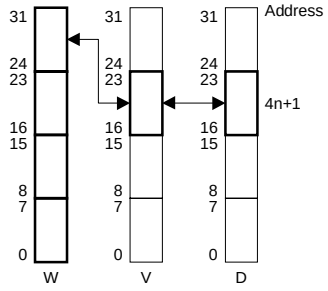
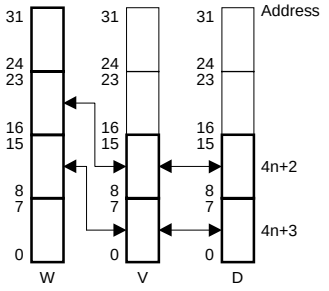
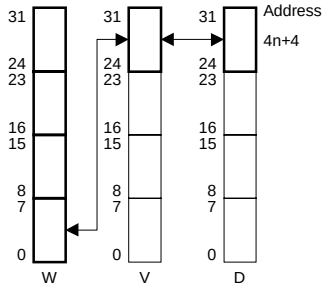
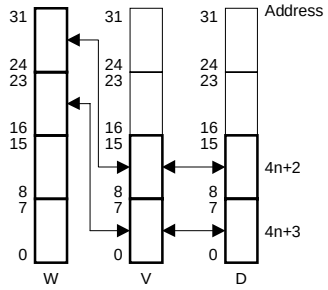
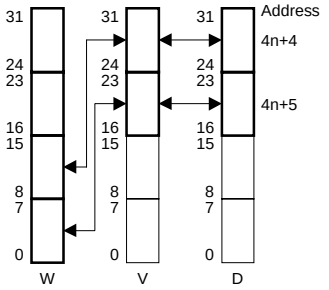
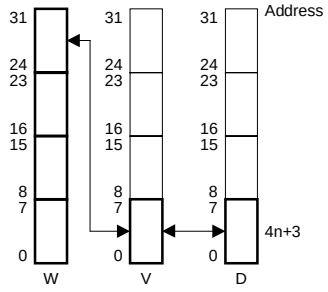
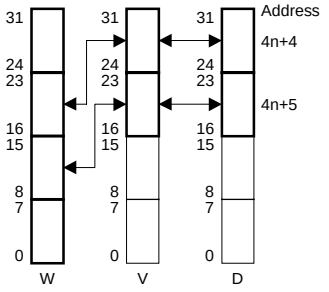
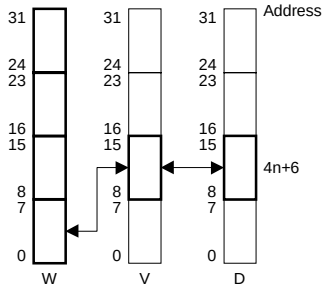
(c) External data bus: 8 bits

Address to Be Accessed	Data Transfer Flow			
	First Time	Second Time	Third Time	Fourth Time
4n				
4n + 1				
4n + 2				
4n + 3				

Remark W: Word data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-34. Word Access (Big Endian) (1/3)

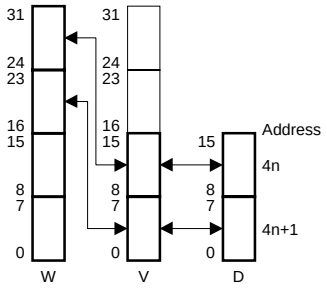
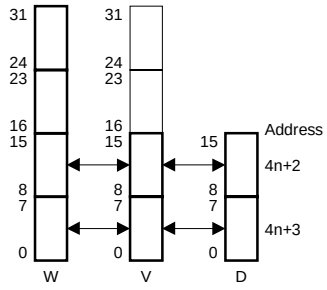
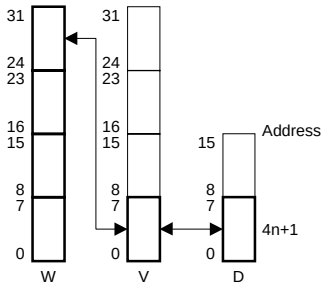
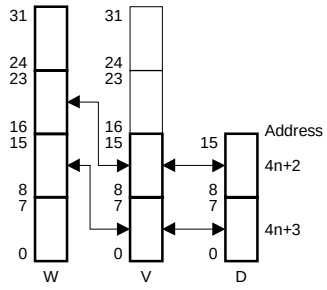
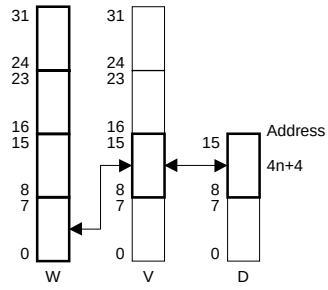
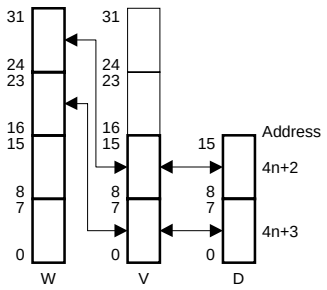
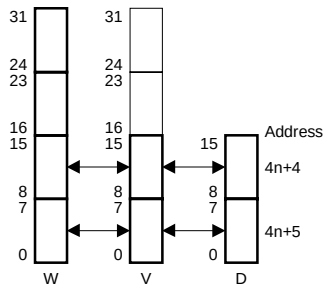
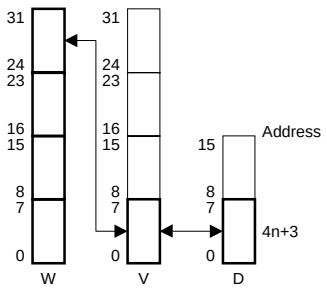
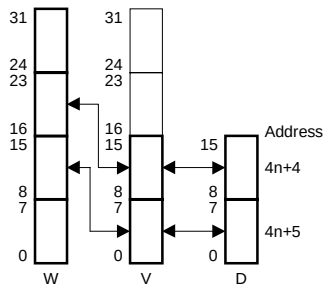
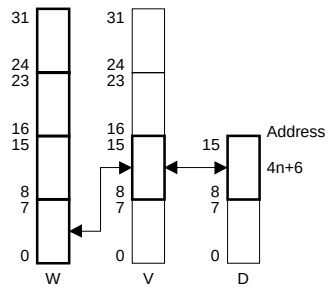
(a) External data bus: 32 bits

Address to Be Accessed	Data Transfer Flow		
	First Time	Second Time	Third Time
4n		—	—
4n + 1			
4n + 2			—
4n + 3			

Remark W: Word data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-34. Word Access (Big Endian) (2/3)

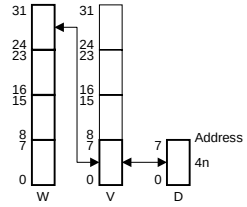
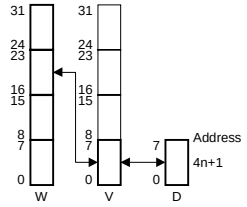
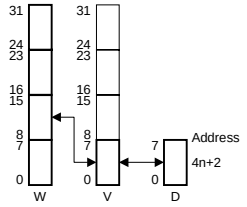
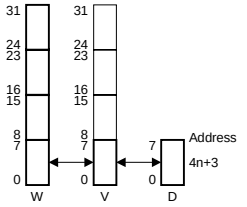
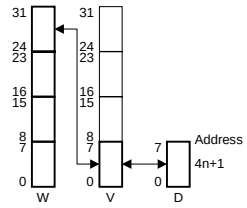
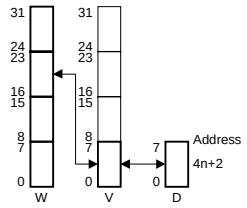
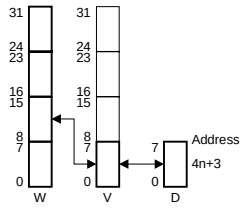
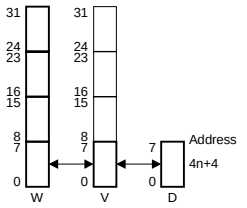
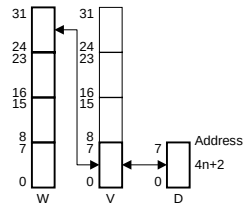
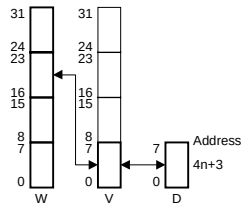
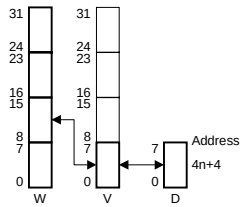
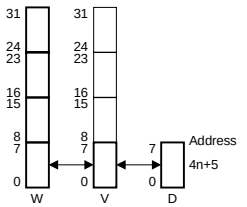
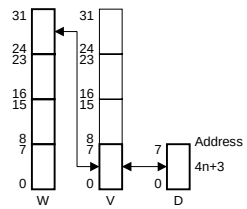
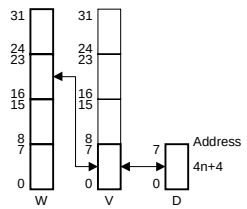
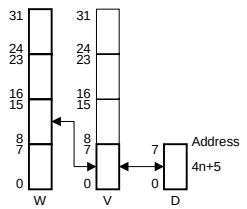
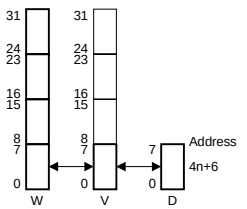
(b) External data bus: 16 bits

Address to Be Accessed	Data Transfer Flow		
	First Time	Second Time	Third Time
4n			—
4n + 1			
4n + 2			—
4n + 3			

Remark W: Word data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

Figure 1-34. Word Access (Big Endian) (3/3)

(c) External data bus: 8 bits

Address to Be Accessed	Data Transfer Flow			
	First Time	Second Time	Third Time	Fourth Time
4n				
4n + 1				
4n + 2				
4n + 3				

Remark W: Word data
V: VSB
D: External data bus
n = 0, 1, 2, 3, …

CHAPTER 2 NU85E502

The NU85E502 is an SDRAM controller for the NB85E and the NB85ET.

The NU85E502 is used connected to the NB85E500 or the NU85E500, depending on the target CPU core.

Target CPU Core	Type of External Memory to Be Connected	Memory Controller (MEMC)
NB85E	SDRAM	NB85E500/NU85E500 + NU85E502
NB85ET		NB85E500 + NU85E502

In this chapter, it is assumed that the NU85E500 and the NU85E502 are used as the MEMC for the NB85E. The SDRAM sequential write timing differs between the NB85E500 and NU85E500. Refer to **1.1 Differences Between NB85E500 and NU85E500** for details.

2.1 Outline

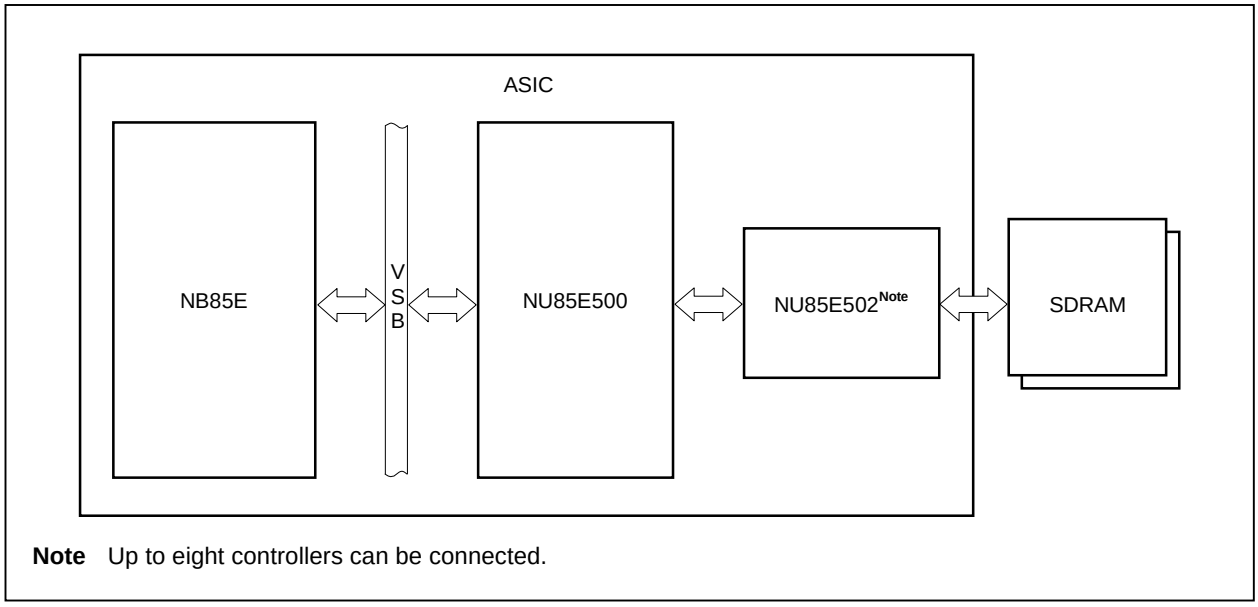
The NU85E502 is a macro for controlling synchronous DRAM (SDRAM).

An external SDRAM bus cycle can be started by connecting the NU85E502 to the NB85E via the NU85E500 and the VSB.

The NU85E502 is used connected to the NU85E500.

Up to eight NU85E502 controllers can be connected.

Figure 2-1. NU85E500 and NU85E502 Connection Example



Note Up to eight controllers can be connected.

★ **Remark** The NU85E502 only supports 12 row addresses and 10 column addresses. Therefore, only SDRAMs of 128 Mbits or less can be connected.

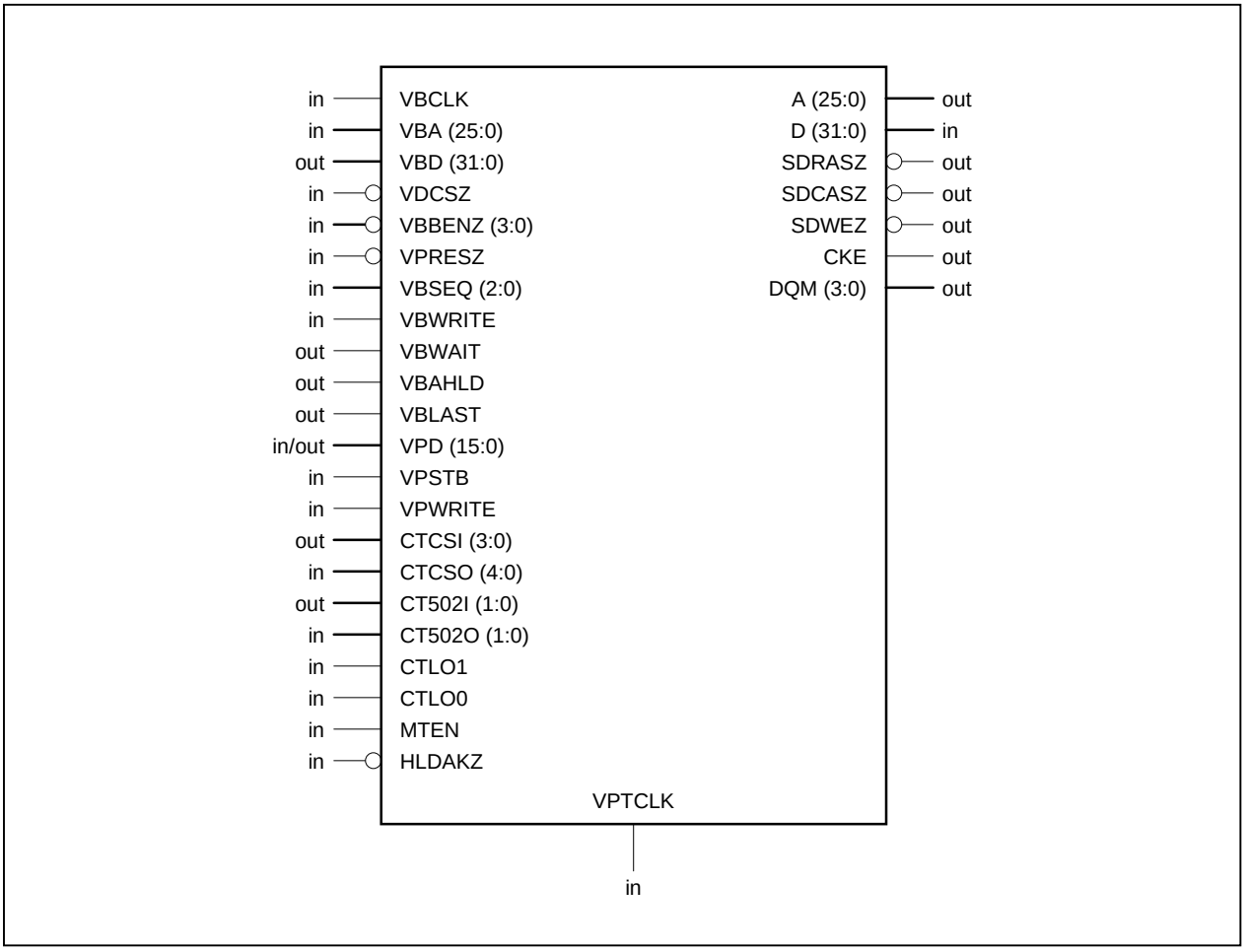
The maximum CS area in 256 MB mode is the 64 MB area of CS1, CS3, CS4, and CS6. If assigning SDRAMs to all of this 64 MB area, it is necessary that this area supports 512 Mbits (64 MB) with a 128 Mbits (4 Mwords × 8 bits × 4 banks) × 4 configuration, and 32 bit bus access.

2.1.1 Features

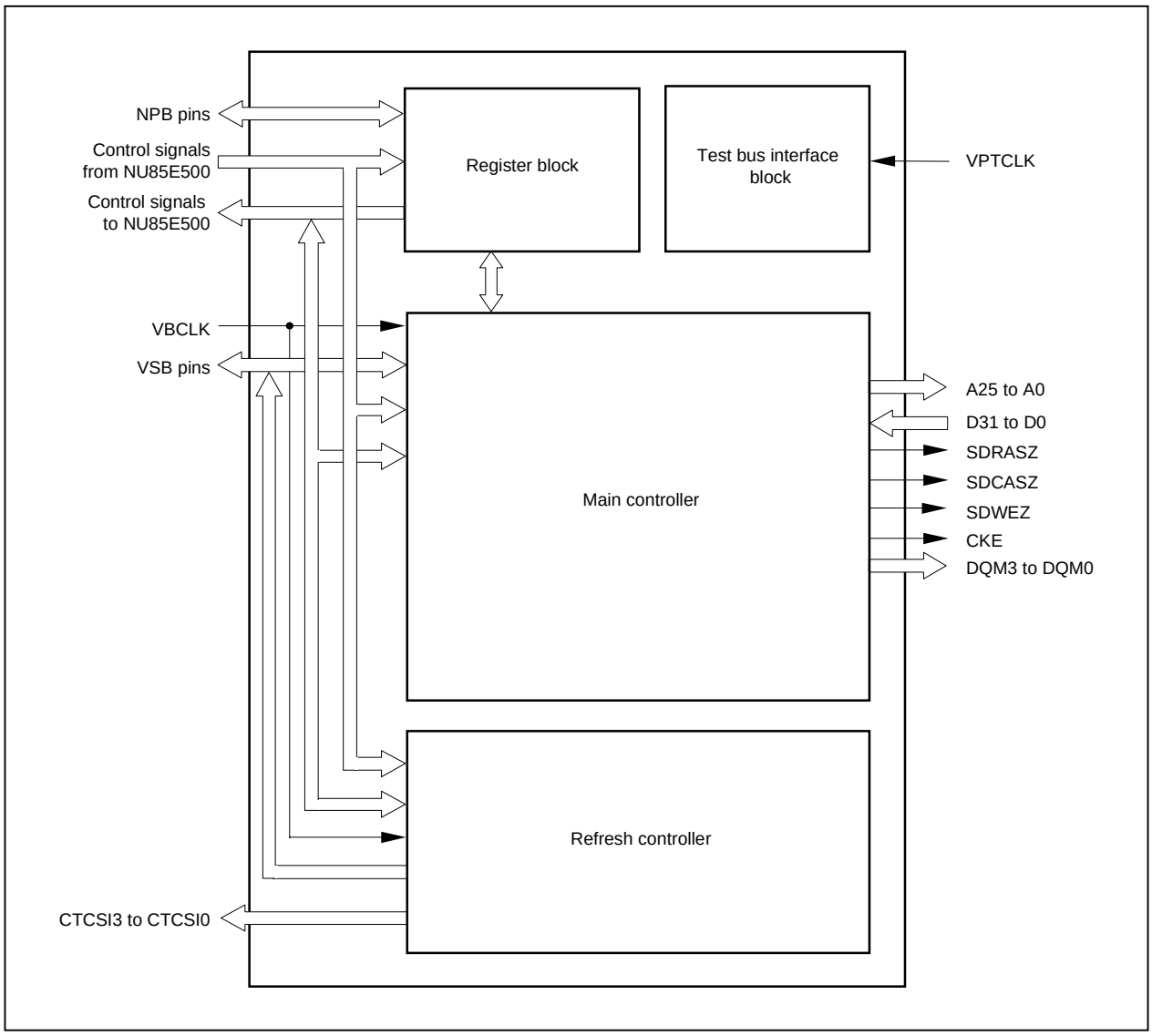
- Only a single access can be started. When the external data bus is 32 bits, burst access of 32-bit data cannot be started. Burst access can be started only in the following cases.
  - When the external data bus is 8 bits and 16-/32-bit data is being read/written
  - When the external data bus is 16 bits and 32-bit data is being read/written
  - ★ When the instruction cache/data cache is being refilled
- A command for continuous access indicated by the VBSEQ2 to VBSEQ0 pins can be issued consecutively in a one-clock interval.
- CAS latency = 2 and 3 are supported.
- An address multiplex function is available.
- The address multiplex width can be changed by means of an SCRn register setting.
- Up to 3 wait states can be inserted by means of an SCRn register setting.
- A register write operation can be executed for each write access to the SCRn register.
- A CBR (CAS before RAS) refresh command can be issued.

Remark n = 7 to 0

2.1.2 Symbol diagram



2.1.3 Block diagram

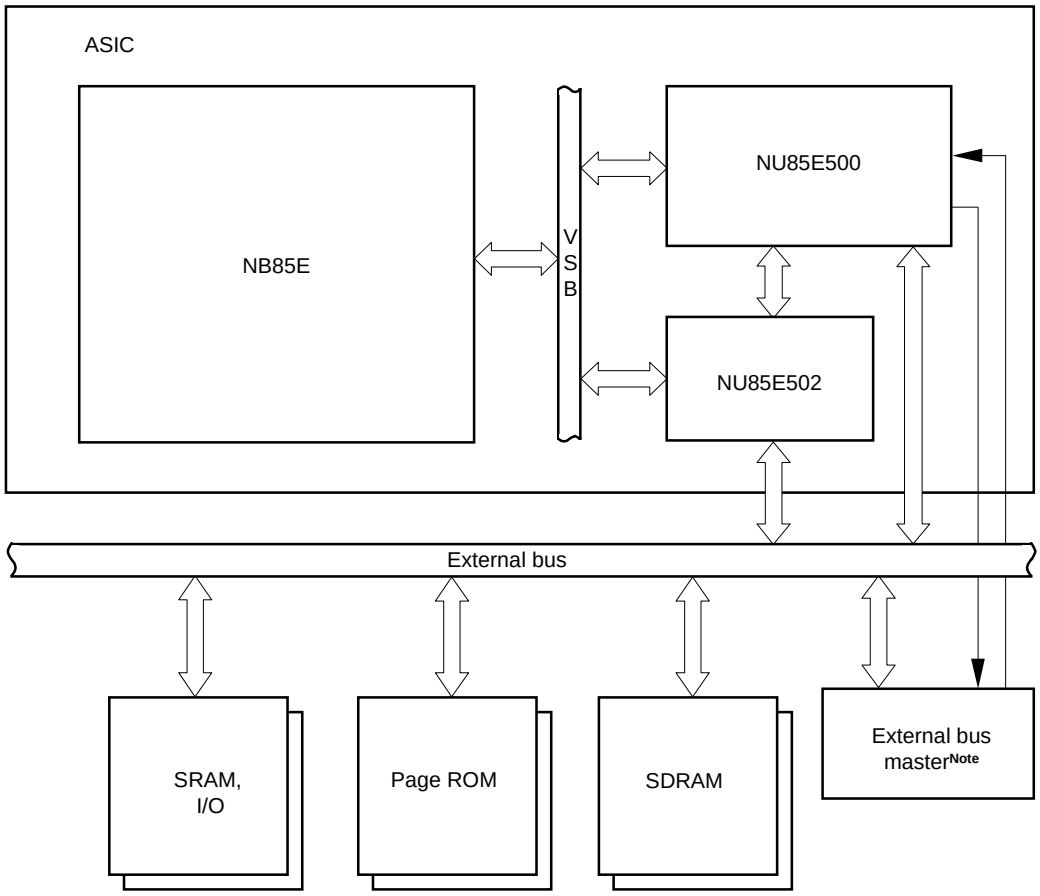


2.1.4 Configuration example

The NU85E502 starts bus cycles for external SDRAM.

The following figure shows an application example using the NU85E502.

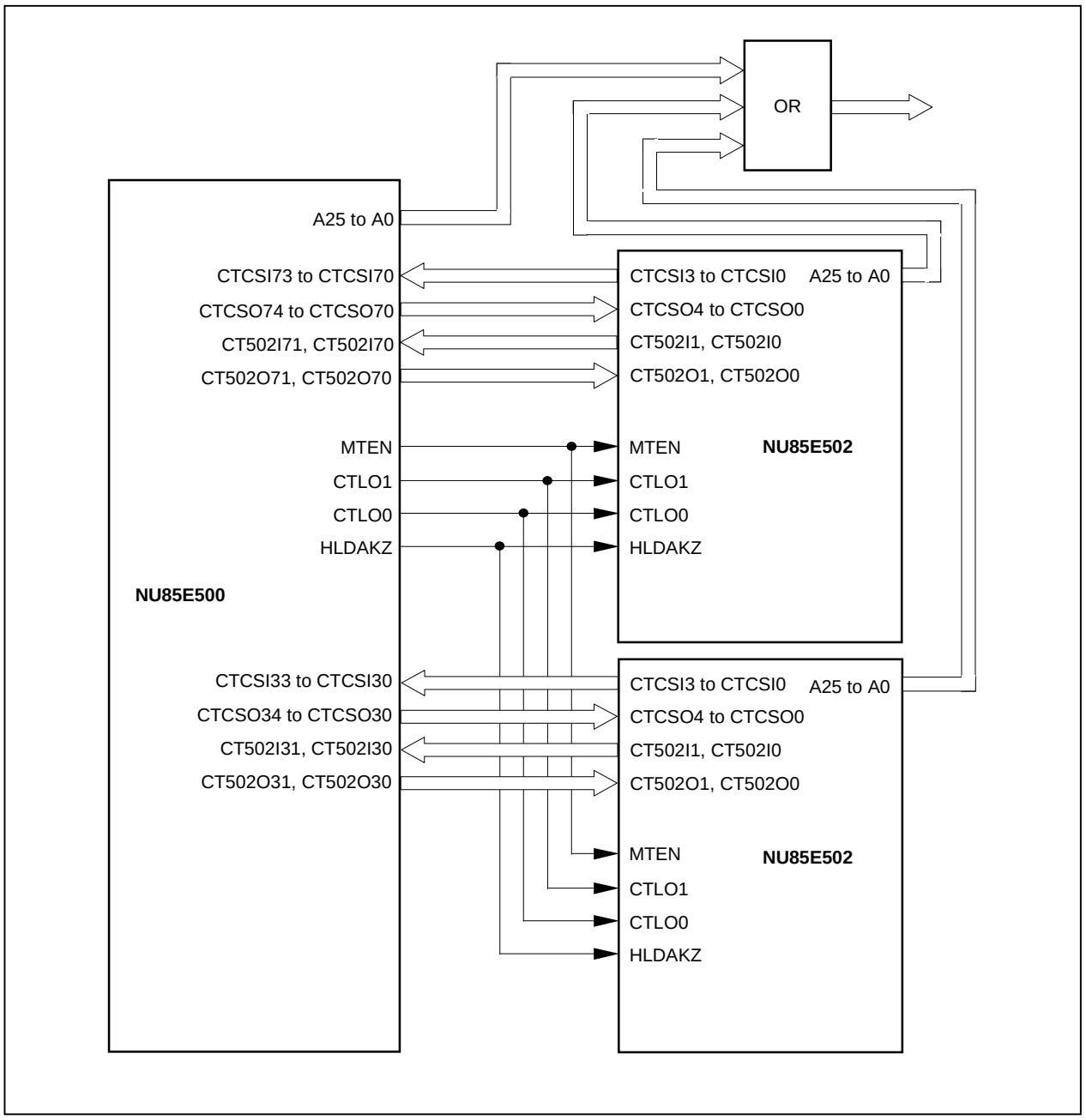
Figure 2-2. Application Example



Note The NU85E500 has an external bus master arbitration function, which is controlled by the HLDRQZ and HLDAKZ signals.

The following figure shows an example of the connections between the NU85E500 and NU85E502 controllers. In this example, the NU85E502 controllers are connected to the CS7 and CS3 areas.

Figure 2-3. Connection Example



2.2 Pin Functions

2.2.1 List of pin functions

Pin Name		I/O	Function
NB85E connection pins	VBCLK	Input	Internal system clock input
	VBA25 to VBA0	Input	Address input
	VBD31 to VBD0	Output	Data output
	VDCSZ	Input	Chip select input
	VBBENZ3 to VBBENZ0	Input	Byte enable input
	VPRESZ	Input	Reset input
	VBSEQ2 to VBSEQ0	Input	Sequential status input
	VBWRITE	Input	Read/write status input
	VBWAIT	Output	Wait response output
	VBAHLD	Output	Address hold response output
	VBLAST	Output	Last response output
	VPD15 to VPD0	I/O	Data input/output (for NPB)
	VPSTB	Input	Data strobe input (for NPB)
	VPWRITE	Input	Write access strobe input (for NPB)
NU85E500 connection pins	CTCSI3 to CTCSI0	Output	Control output to NU85E500
	CTCSO4 to CTCSO0	Input	Control input from NU85E500
	CT502I1, CT502I0	Output	Control output to NU85E500
	CT502O1, CT502O0	Input	Control input from NU85E500
	CTLO1, CTLO0	Input	Control input from NU85E500
	MTEN	Input	Test mode enable input from NU85E500
	HLDAKZ	Input	Bus hold status input from NU85E500
External memory connection pins	A25 to A0	Output	External memory address output
	D31 to D0	Input	External memory data input
	SDRASZ	Output	SDRAM row address strobe output
	SDCASZ	Output	SDRAM column address strobe output
	SDWEZ	Output	SDRAM data write enable output
	CKE	Output	Clock enable output
	DQM3 to DQM0	Output	Data mask output
Test mode pin	VPTCLK	Input	Test clock input

2.2.2 Explanation of pin functions

(1) NB85E connection pins

(a) VSB pins (VBxxx and VDxxx)

Refer to the **NB85E Hardware User's Manual (A13971E)**.

(b) NPB pins (VPxxx)

Refer to the **NB85E Hardware User's Manual (A13971E)**.

(2) NU85E500 connection pins

(a) CTCSI3 to CTCSI0 (output)

These are pins for controlling output to the NU85E500.

(b) CTCSO4 to CTCSO0 (input)

These are pins for controlling input from the NU85E500.

(c) CT502I1 and CT502I0 (output)

These are pins for controlling output to the NU85E500.

(d) CT502O1 and CT502O0 (input)

These are pins for controlling input from the NU85E500.

(e) CTLO1 and CTLO0 (input)

These are pins for controlling input from the NU85E500.

(f) MTEN (input)

This is the pin to which the test mode enable is input from the NU85E500.

(g) HLDAKZ (input)

This is the pin to which the bus hold status is input from the NU85E500.

This is used only when the external bus master accesses SDRAM during a bus hold. Input a high level when not being used.

Caution Do not rewrite SDRAM configuration register n (SCRn) (n =7 to 0) using the external bus master during a bus hold.

Remark After releasing a bus hold, when the NU85E502 regains bus mastership and accesses SDRAM, access starts from all bank precharge.

(3) External memory connection pins

(a) A25 to A0 (output)

These pins constitute the external SDRAM address bus.

When the VDCSZ signal is inactive, all of the pins A25 to A0 output a low-level signal.

(b) D31 to D0 (input)

These pins constitute the external SDRAM data bus.

(c) SDRASZ (output)

This is the row address strobe output pin for external SDRAM.

(d) SDCASZ (output)

This is the column address strobe output pin for external SDRAM.

(e) SDWEZ (output)

This is the data write enable output pin for external SDRAM.

(f) CKE (output)

This is the clock enable output pin for external SDRAM.

This pin outputs an inactive (low level) during a self-refresh cycle.

(g) DQM3 to DQM0 (output)

These are the data mask output pins for external SDRAM.

During a write cycle, they output the same values as the VBBENZ3 to VBBENZ0 signals of the NB85E when a write command is executed. During a read cycle, the DQM3 to DQM0 pins output a low level after a read command.

(4) Test mode pin

(a) VPTCLK (input)

This is a test clock input pin.

2.2.3 Recommended connection of unused pins

Pin Name		I/O	Recommended Connection Method
External memory connection pins	A25 to A0, SDRASZ, SDCASZ, SDWEZ, CKE, DQM3 to DQM0	Output	Leave open.
	D31 to D0	Input	Input low level.

2.2.4 Pin status

The following table shows the status in each operating mode of the pins that have output functions.

Table 2-1. Pin Status in Each Operating Mode

Pin Name		Pin Status				
		Reset	STOP Mode	HALT Mode	Bus Hold	Test Mode
NB85E connection pins	VBD31 to VBD0	Hi-Z	Hi-Z	Operating	Hi-Z	Operating
	VBWAIT	Hi-Z	Hi-Z	Operating	Hi-Z	Operating
	VBAHLD	Hi-Z	Hi-Z	Operating	Hi-Z	Operating
	VBLAST	Hi-Z	Hi-Z	Operating	Hi-Z	Operating
	VPD15 to VPD0	Hi-Z	Hi-Z	Operating	Hi-Z	Operating
External memory connection pins	A25 to A0	Undefined	Maintain	Operating	Maintain	Operating
	SDRASZ	H	H	Operating	H	Operating
	SDCASZ	H	H	Operating	H	Operating
	SDWEZ	H	H	Operating	H	Operating
	CKE	H	L	Operating	H	Operating
	DQM3 to DQM0	H	H	Operating	H	Operating

Remark L: Low-level output
H: High-level output
Hi-Z: High impedance
Maintain: Maintains the previous status

2.3 Bus Cycle Function

2.3.1 SDRAM configuration register n (SCRn)

This register sets the number of waits and the address multiplex width.

When more than one NU85E502 is incorporated in the system, settings can be made for each CSn area (n = 7 to 0).

If this register is written to, the NU85E502 will start a register write operation.

This register can be read or written in 16-bit units.

Cautions 1. An SDRAM read/write cycle will not be generated prior to the execution of a register write operation.

Access SDRAM after waiting 20 clocks following execution of a program that writes to the SCRn register. When setting the SCRn register again after accessing SDRAM, first clear (to 0) the ME bit of the BCT0 and BCT1 registers in the NU85E500, and then set (1) again. ★

2. Do not execute continuous write instructions to the SCRn register. Be sure to insert and execute another instruction between write instructions to the SCRn register.

3. When two or more NU85E502 are used, do not access the SDRAM area before completing all the settings of the SCRn register (n = 7 to 0). ★

Remarks 1. n of the register name corresponds to the CSn area number.

2. The address decoder is in the NU85E500. For the addresses of each CSn area, refer to the **NB85E Hardware User's Manual (A13971E)**.

Figure 2-4. SDRAM Configuration Register n (SCRn) (1/2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset
SCRn	0	LTM2	LTM1	LTM0	0	0	0	0	BCW1	BCW0	SSO1	SSO0	RAW1	RAW0	SAW1	SAW0	FFFFF4A0H + 4n	0000H

Bit position	Bit name	Description
14 to 12	LTM2 to LTM0	Set the CAS latency value of a read operation.

LTM2	LTM1	LTM0	CAS latency
0	0	Don't care	Setting prohibited
0	1	0	2
0	1	1	3
1	Don't care	Don't care	Setting prohibited

Remark n = 7 to 0

Figure 2-4. SDRAM Configuration Register n (SCRn) (2/2)

Bit position	Bit name	Description
7, 6	BCW1, BCW0	Set the number of wait states between the bank active command and the read/write command, or between the precharge command and the bank active command.

BCW1	BCW0	Number of wait states
0	0	Setting prohibited
0	1	1
1	0	2
1	1	3

Bit position	Bit name	Description
5, 4	SSO1, SSO0	Set the address shift width during On-page judgment. When the data bus size has been set to either 16 bits or 32 bits, the system does not use the lower addresses (A0 or A1 and A0).

SSO1	SSO0	Address shift width
0	0	0 bits (8-bit data bus)
0	1	1 bit (16-bit data bus)
1	0	2 bits (32-bit data bus)
1	1	Setting prohibited

Bit position	Bit name	Description
3, 2	RAW1, RAW0	Set the row address width.

RAW1	RAW0	Row address width
0	0	11 bits
0	1	12 bits
1	Don’t care	Setting prohibited

Bit position	Bit name	Description
★ 1, 0	SAW1, SAW0	Set the column address width.

SAW1	SAW0	Column address width
0	0	8 bits
0	1	9 bits
1	0	10 bits
1	1	Setting prohibited

Caution The SCRn register should be set immediately after reset, and its setting should not be subsequently changed (n = 7 to 0).

Table 2-2. Row Address Output

Address Pin	A25 to A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SAW1 and SAW0 bits = 10	a25 to a18	a17	a16	a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a13	a12	a11	a10
SAW1 and SAW0 bits = 01	a25 to a18	a17	a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a13	a12	a11	a10	a9
SAW1 and SAW0 bits = 00	a25 to a18	a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a13	a12	a11	a10	a9	a8

Table 2-3. Column Address Output

(a) All bank precharge commands

Address Pin	A25 to A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SSO1 and SSO0 bits = 00	a25 to a18	a17	a16	a15	a14	a13	a12	a11	1	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0
SSO1 and SSO0 bits = 01	a25 to a18	a17	a16	a15	a14	a13	a12	1	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0
SSO1 and SSO0 bits = 10	a25 to a18	a17	a16	a15	a14	a13	1	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0

(b) Register write command

Address Pin	A25 to A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SSO1 and SSO0 bits = 00	0	0	0	0	0	0	0	0	0	0	0	0	LTM2	LTM1	LTM0	0	0	0	0
SSO1 and SSO0 bits = 01	0	0	0	0	0	0	0	0	0	0	0	LTM2	LTM1	LTM0	0	0	0	0	0
SSO1 and SSO0 bits = 10	0	0	0	0	0	0	0	0	0	0	LTM2	LTM1	LTM0	0	0	0	0	0	0

(c) Read/write command

Address Pin	A25 to A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SSO1 and SSO0 bits = 00	a25 to a18	a17	a16	a15	a14	a13	a12	a11	0	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0
SSO1 and SSO0 bits = 01	a25 to a18	a17	a16	a15	a14	a13	a12	0	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0
SSO1 and SSO0 bits = 10	a25 to a18	a17	a16	a15	a14	a13	0	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0

★ **(1) Address outputs and SDRAM connection**

The settings of SDRAM configuration register n (SCRn), physical addresses, address outputs from the NU85E502, and connection of the NU85E502 and SDRAM for each data bus width (8 bits, 16 bits, and 32 bits) are described below.

(a) 8-bit data bus

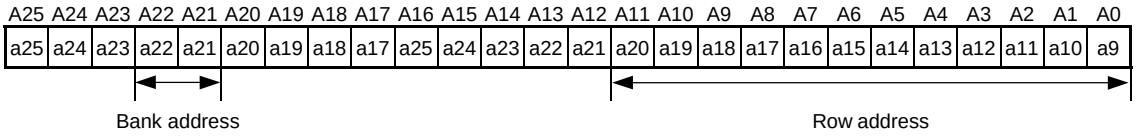
A connection example of 64 Mbit SDRAM (2 Mwords × 8 bits × 4 banks) when using an 8-bit data bus is shown below.

- SCRn register settings
  SSO1, SSO0 = 00: Data bus width = 8 bits
  RAW1, RAW0 = 01: Row address width = 12 bits
  SAW1, SAW0 = 01: Column address width = 9 bits

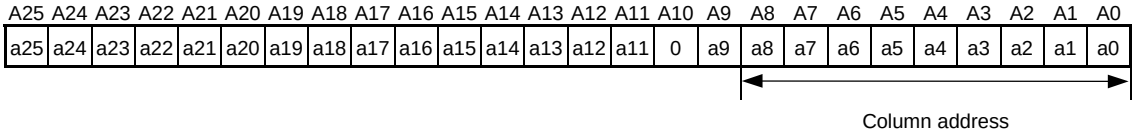
- Physical addresses
  A22, A21: Bank address
  A20 to A9: Row address
  A8 to A0: Column address

- Addresses output from the NU85E502
  A22, A21: Bank address
  A11 to A0: Row address (12 bits), column address (9 bits)

  Row addresses and bank addresses output upon active command



  Column addresses output upon read/write command



- Connection of the NU85E502 and SDRAM
  A22, A21 (NU85E502) → BA0 (A13), BA1 (A12) (SDRAM)
  A11 to A0 (NU85E502) → A11 to A0 (SDRAM)

(b) 16-bit data bus

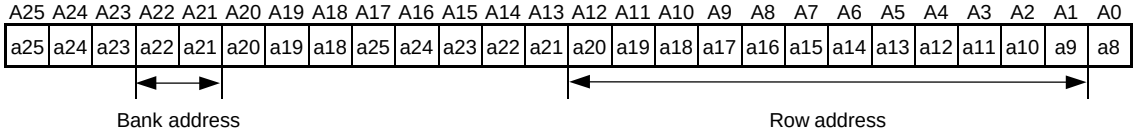
A connection example of 64 Mbit SDRAM (1 Mword × 16 bits × 4 banks) when using a 16-bit data bus is shown below.

- SCRn register settings
  SSO1, SSO0 = 01: Data bus width = 16 bits
  RAW1, RAW0 = 01: Row address width = 12 bits
  SAW1, SAW0 = 00: Column address width = 8 bits

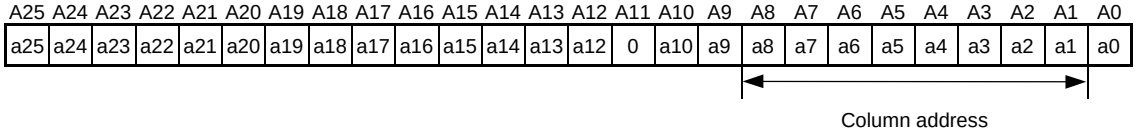
- Physical addresses
  A22, A21: Bank address
  A20 to A9: Row address
  A8 to A1: Column address

- Addresses output from the NU85E502
  A22, A21: Bank address
  A12 to A1: Row address (12 bits), column address (8 bits)

  Row addresses and bank addresses output upon active command



  Column addresses output upon read/write command



- Connection of the NU85E502 and SDRAM
  A22, A21 (NU85E502) → BA0 (A13), BA1 (A12) (SDRAM)
  A12 to A1 (NU85E502) → A11 to A0 (SDRAM)

(c) 32-bit data bus

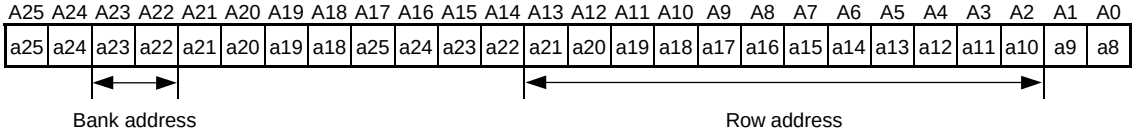
A connection example of 128 Mbit SDRAM (64 Mbit SDRAM (1 Mword × 16 bits × 4 banks) × 2) when using a 32-bit data bus is shown below.

- SCRn register settings
  SSO1, SSO0 = 10: Data bus width = 32 bits
  RAW1, RAW0 = 01: Row address width = 12 bits
  SAW1, SAW0 = 00: Column address width = 8 bits

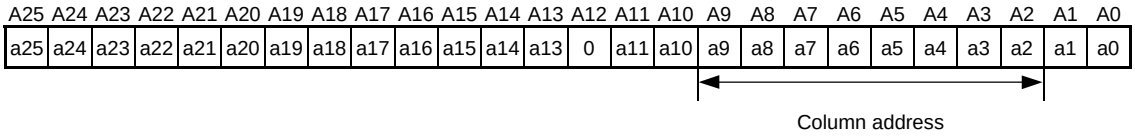
- Physical addresses
  A23, A22: Bank address
  A21 to A10: Row address
  A9 to A2: Column address

- Addresses output from the NU85E502
  A23, A22: Bank address
  A13 to A2: Row address (12 bits), column address (8 bits)

  Row addresses and bank addresses output upon active command



  Column addresses output upon read/write command



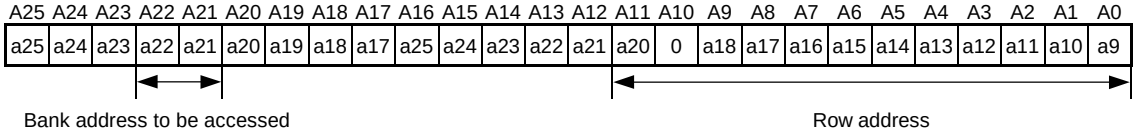
- Connection of the NU85E502 and SDRAM
  A23, A22 (NU85E502) → BA0 (A13), BA1 (A12) (SDRAM)
  A13 to A2 (NU85E502) → A11 to A0 (SDRAM)

★ **(2) Bank address output**

The NU85E502 precharges the bank to be accessed at the row address output immediately after a page change as a bank precharge command. In addition, after a bank change, the NU85E502 precharges the bank accessed last at the column address output. Therefore, since a bank precharge is performed either at the row address output or the column address output, always connect the pins (A22 and A21) of the NU85E502 that output bank addresses to the bank address pins (A13 and A12) of the SDRAM when connection is performed according to the description in **2.3.1 (1) (a) 8-bit data bus.** Examples of address output upon bank precharge command at a page change and a bank change when connection is performed according to the description in **2.3.1 (1) (a) 8-bit data bus** are described below.

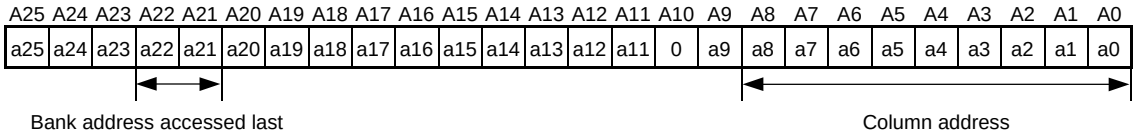
(a) At a page change (8-bit data bus)

Since the bank to be accessed is precharged, the physical addresses (A25 to A9) to be accessed are output from the A25 to A9 pins of the NU85E502.



(b) At a bank change (8-bit data bus)

Since the bank accessed last is precharged, the physical addresses (A25 to A9) accessed last are output from the A25 to A9 pins of the NU85E502.

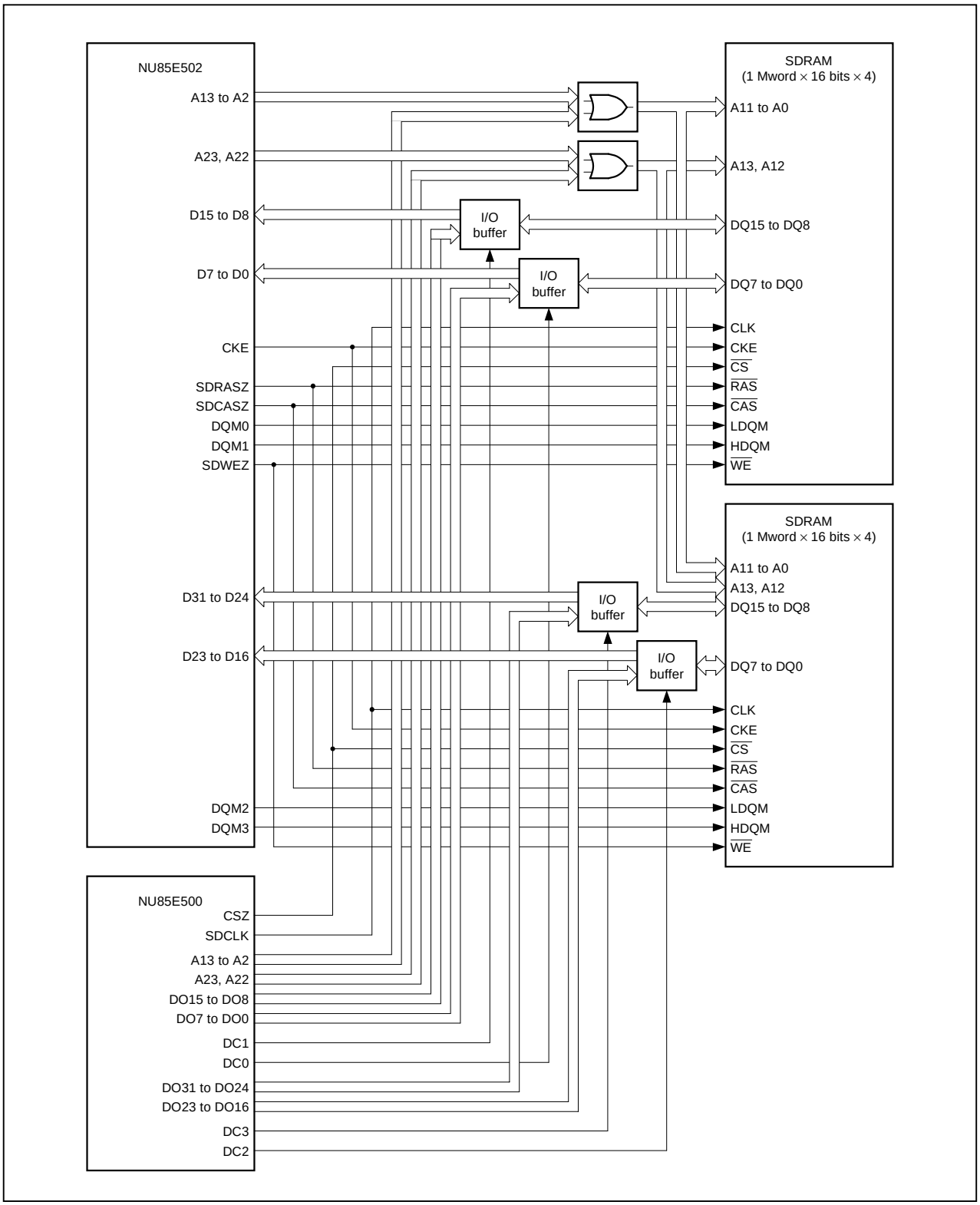


The bit that specifies the precharge mode (A10: 8-bit data bus, A11: 16-bit data bus, A12: 32-bit data bus) outputs a high level upon an all bank precharge command, and a low level during other precharges.

2.3.2 SDRAM cycle

(1) Connection example

★ **Figure 2-5. 64 Mbit SDRAM Connection Example**



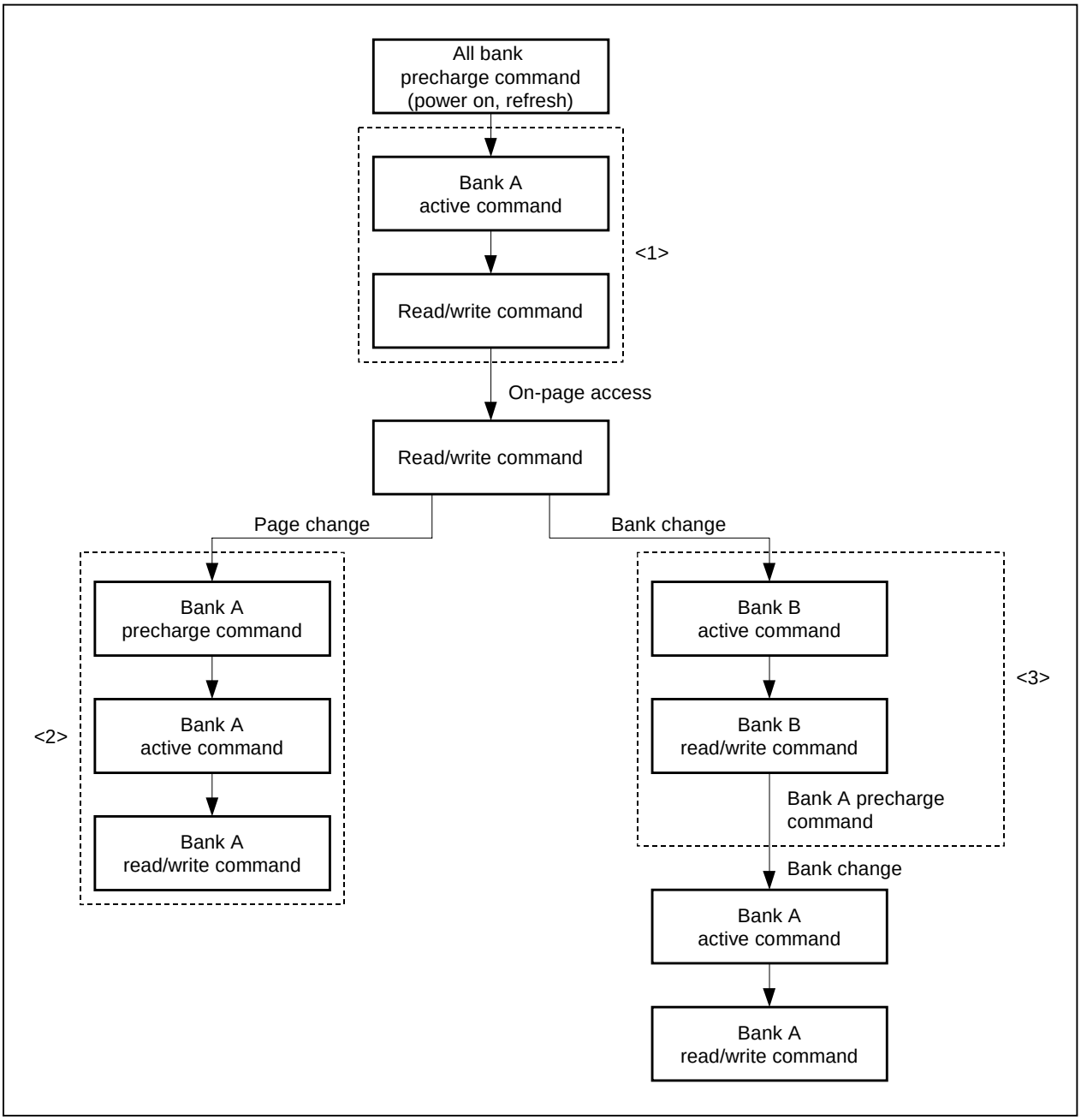
(2) Bus timing

During power on or refresh, an all bank precharge command is always issued to the SDRAM. Therefore, when the SDRAM is accessed after this, the active command and read/write command are issued in order (<1> in **Figure 2-6**).

When a page change occurs, the precharge command, active command, and read/write command are issued in order (<2> in **Figure 2-6**).

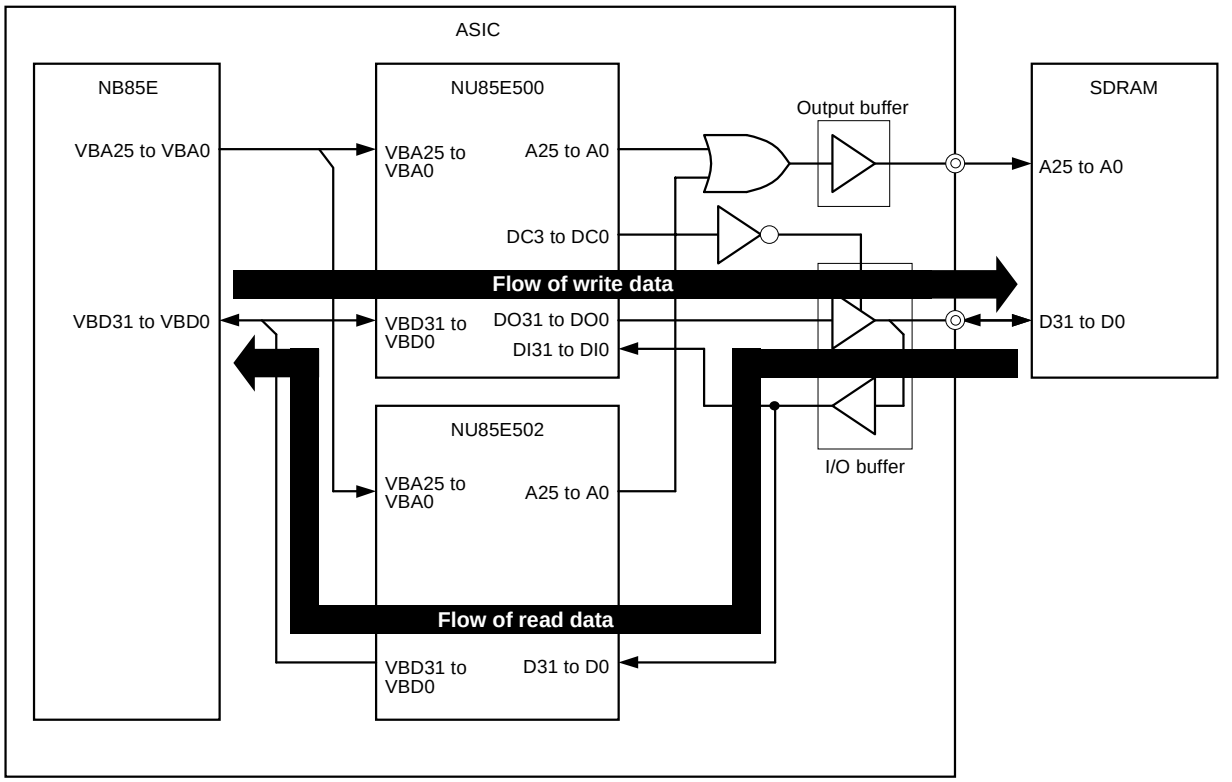
When a bank change occurs, the active command and read/write command for the bank to be accessed next are issued in order. Immediately after the read/write command, the precharge command for the bank that was accessed immediately before the currently accessed bank is issued (<3> in **Figure 2-6**).

Figure 2-6. State Transition of SDRAM Access



The write data to the SDRAM is output from the NU85E500, and the read data from the SDRAM is input to the NU85E502.

Figure 2-7. Read/Write Data Flow for SDRAM



Remark When the addresses (A25 to A0) are output from the NU85E502 to the SDRAM, A25 to A0 output from the NU85E500 becomes low level.

Examples of the bus timing for an SDRAM read or write are shown below. An SDRAM bus cycle consists of the following states.

- ALLPRE state: All bank precharge command state.
- REFW state: Refresh wait state.
- REGW state: Register write command state.
- TACT state: Bank active command state.
- TBCW state: Wait state that is inserted when BCW is set to 2 or 3.
- TI state Idle state that is inserted according to the setting of the BCC register (inserted only during a read operation).
- TLATE state: Latency-amount wait state.
- TPREC state: Bank precharge command state.
- TREAD state: Read command state.
- TREF state: Refresh command state.
- TRPW state: Wait state between the read/write cycles following a register write operation.
- TW state: Wait state.
- TW0 state: Wait state indicating the status of waiting prior to the start of a register write operation.
- TWE state: State indicating the end of the write cycle.
- ★ TWPRE state: State indicating precharge. Precharges the bank accessed last only when the bank changes.
- TWR state: Write command state.

Remarks 1. The broken-line portions of the VBTTYP1, VBTTYP0, VBSIZE1, VBSIZE0, VBCTYP2 to VBCTYP0, VBSEQ2 to VBSEQ0, VBD31 to VBD0, VBWAIT, VBAHLT, and VBLAST signals indicate a weak unknown state; a state entered when the NB85E internal bus holder is driving. The level of broken-line portions of the D31 to D0 and DO31 to DO0 signals is undefined.

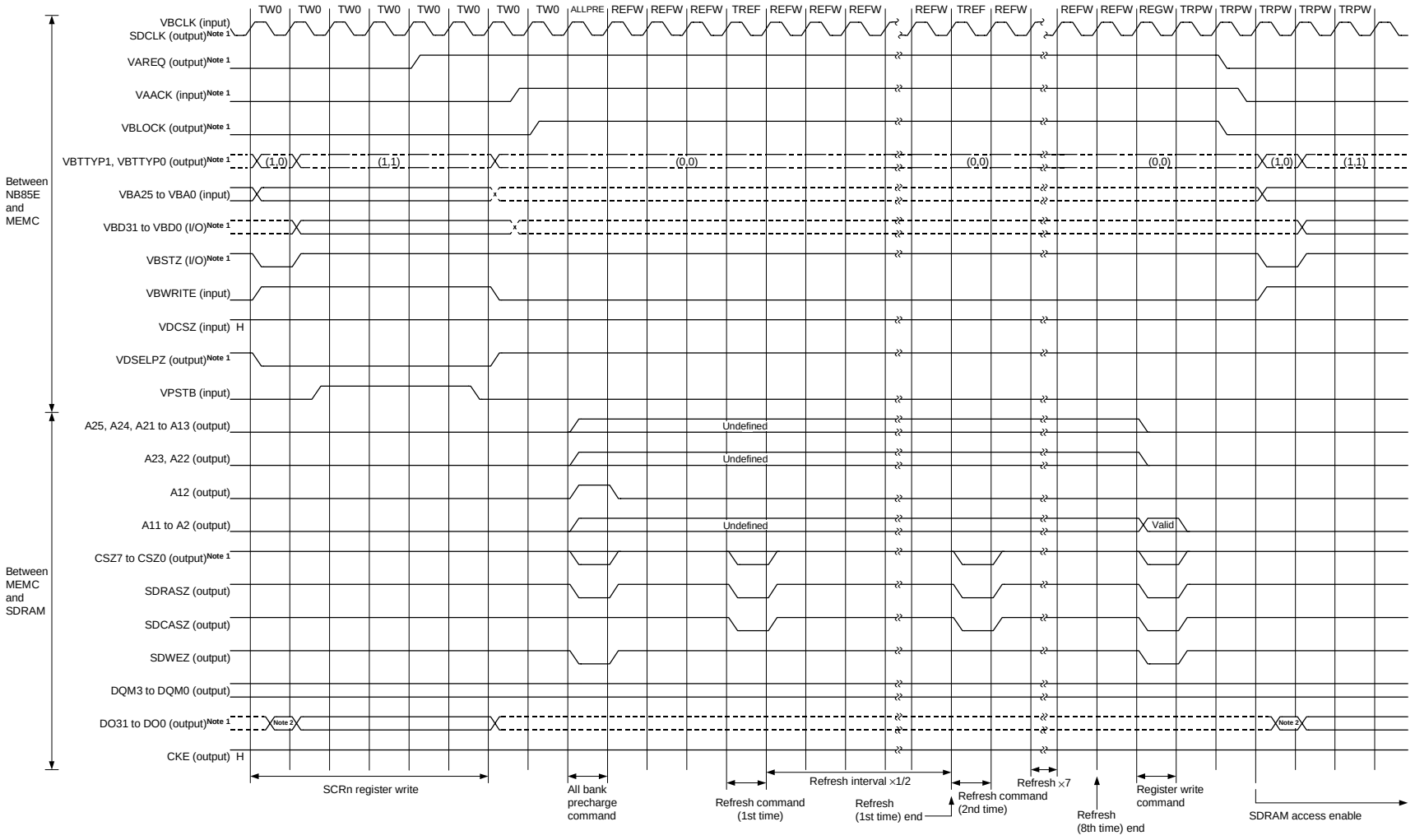
2. Circles indicate sampling timing.

3. For details of VSB signals (VBxxx, VDxxx), refer to the **NB85E Hardware User's Manual (A13971E)**.

4. BCW: Wait state set by the BCW1 and BCW0 bits of the SCRn register (n = 7 to 0)

★ **5.** The address/bank address output upon a bank precharge command is the address/bank address accessed last.

Figure 2-8. SDRAM Register Write Operation Timing



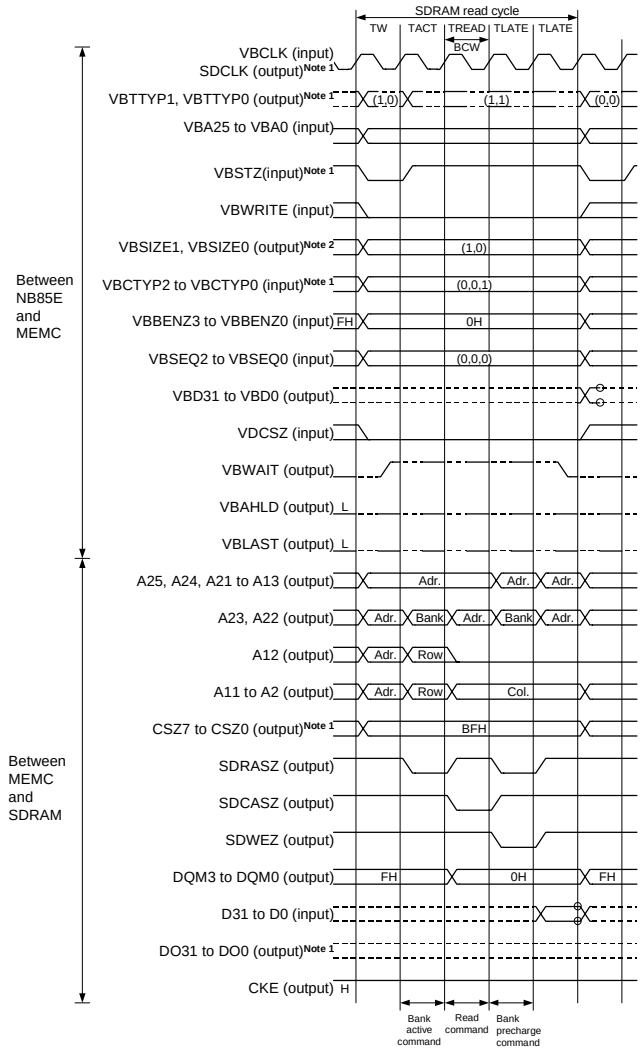
Notes 1. NU85E500 signal

2. Invalid data for SDRAM is output.

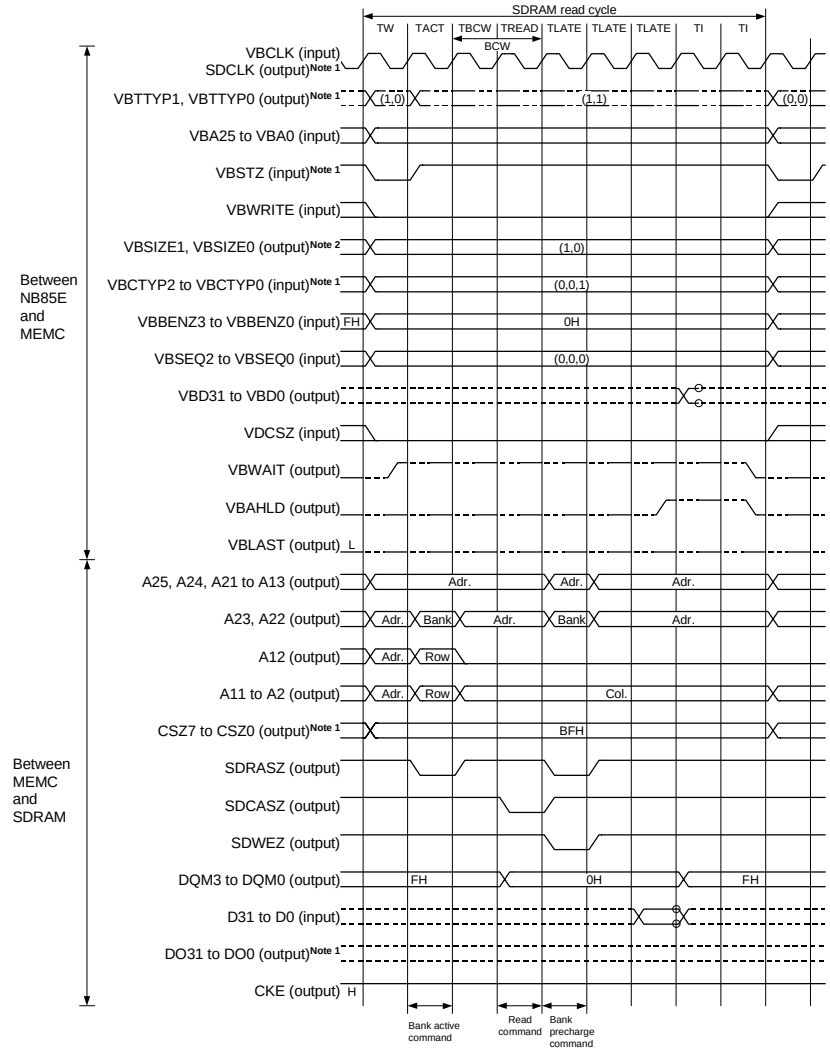
Remark Refresh interval × 1/2: Half period of the refresh interval set by the RFSn register (n = 7 to 0)

Figure 2-9. SDRAM Single Read Cycle (32-Bit Data Bus, Word Access) (1/2)

(a) Off-page, bank change, CAS latency = 2, BCW = 1



(b) Off-page, bank change, CAS latency = 3, BCW = 2, idle state = 2

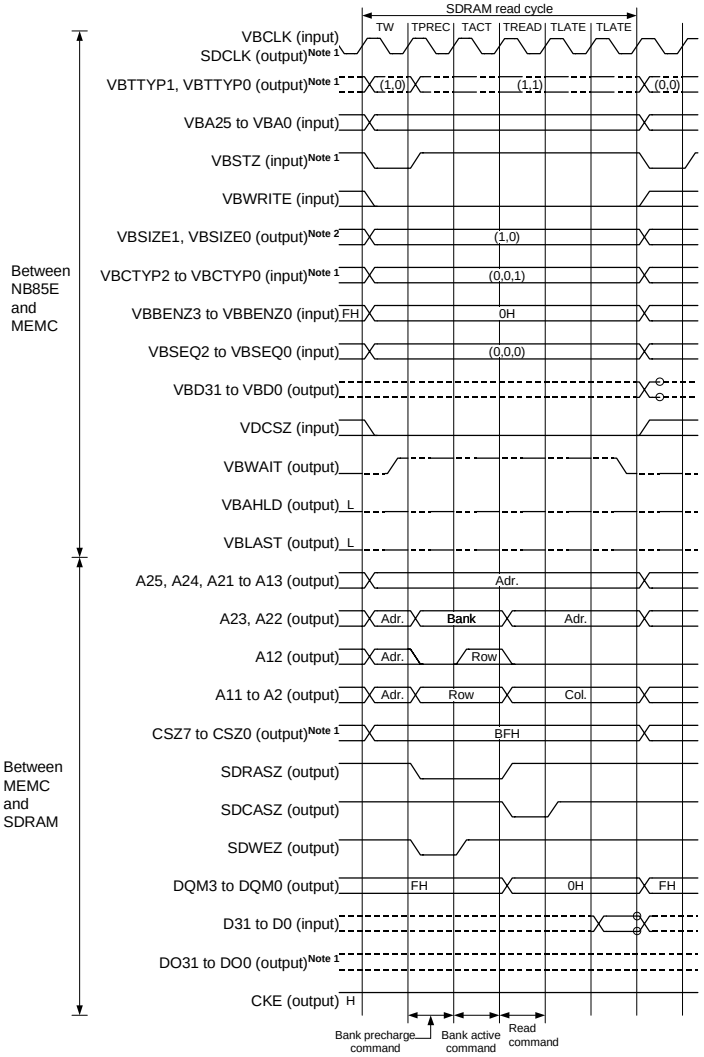


Notes 1. NU85E500 signal

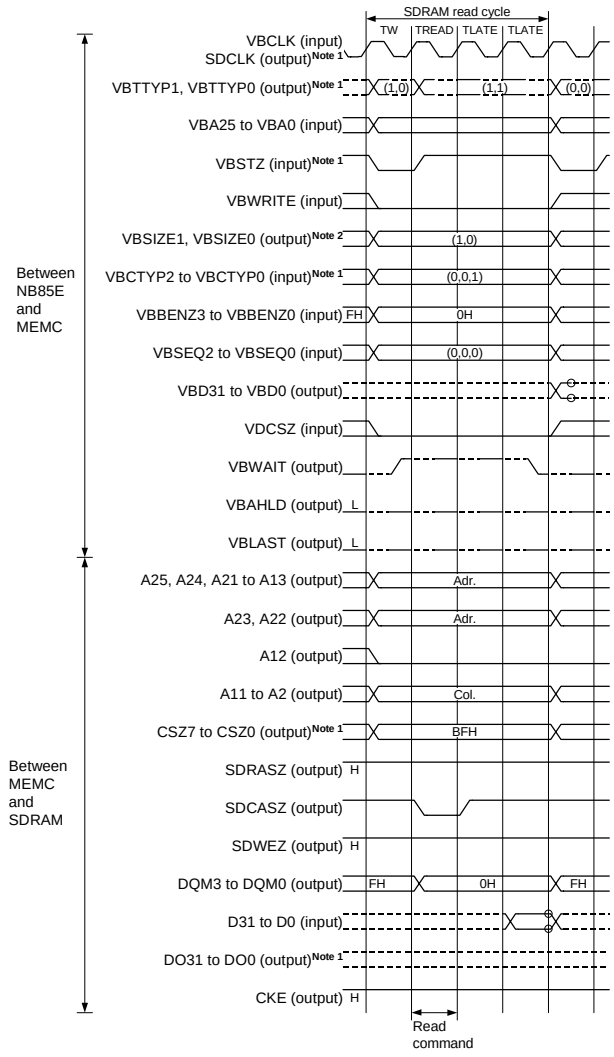
Notes 2. NB85E signal. This signal is not connected to MEMC.

Figure 2-9. SDRAM Single Read Cycle (32-Bit Data Bus, Word Access) (2/2)

(c) Off-page, page change



(d) On-page, CAS latency = 2

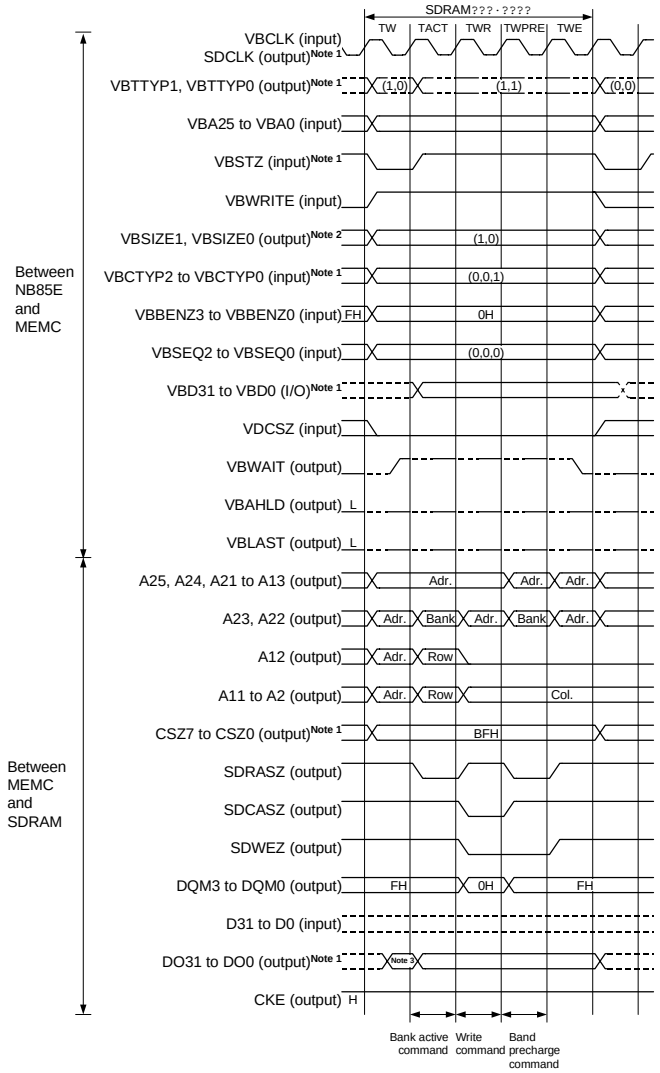


Notes 1. NU85E500 signal

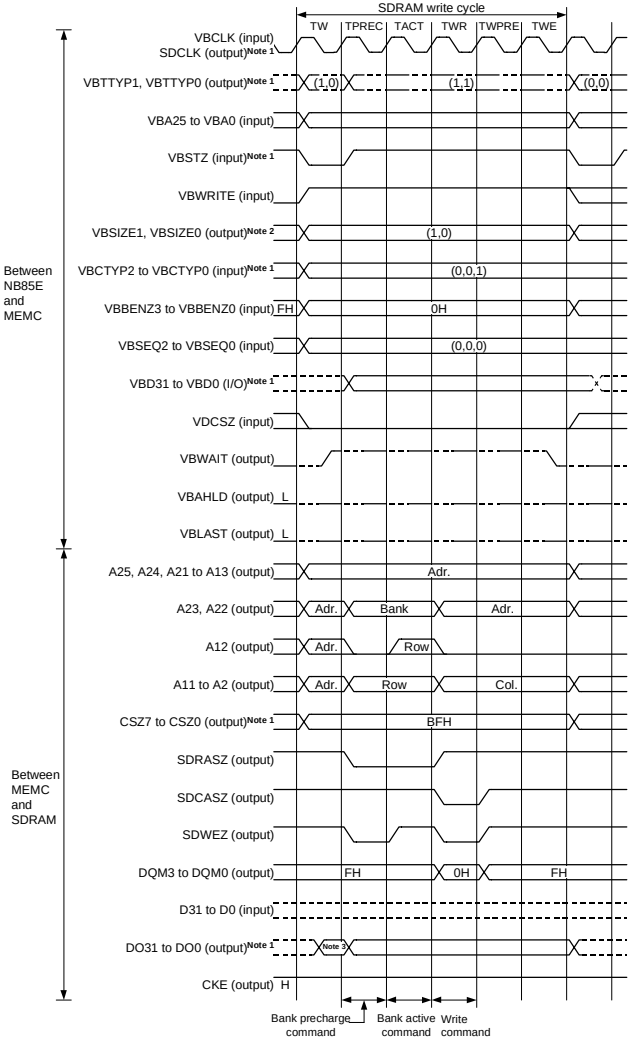
Notes 2. NB85E signal. This signal is not connected to MEMC.

Figure 2-10. SDRAM Single Write Cycle (32-Bit Data Bus, Word Access) (1/2)

(a) Off-page, bank change



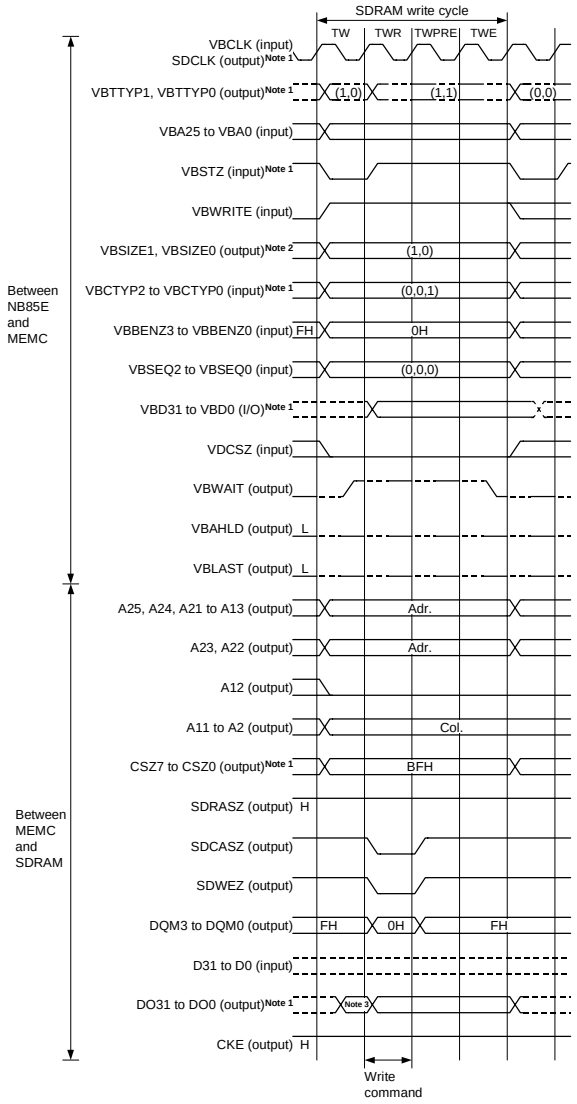
(b) Off-page, page change



Notes 1. NU85E500 signal **Notes 2.** NB85E signal. This signal is not connected to MEMC. **Notes 3.** Invalid data for SDRAM is output.

Figure 2-10. SDRAM Single Write Cycle (32-Bit Data Bus, Word Access) (2/2)

(c) On-page

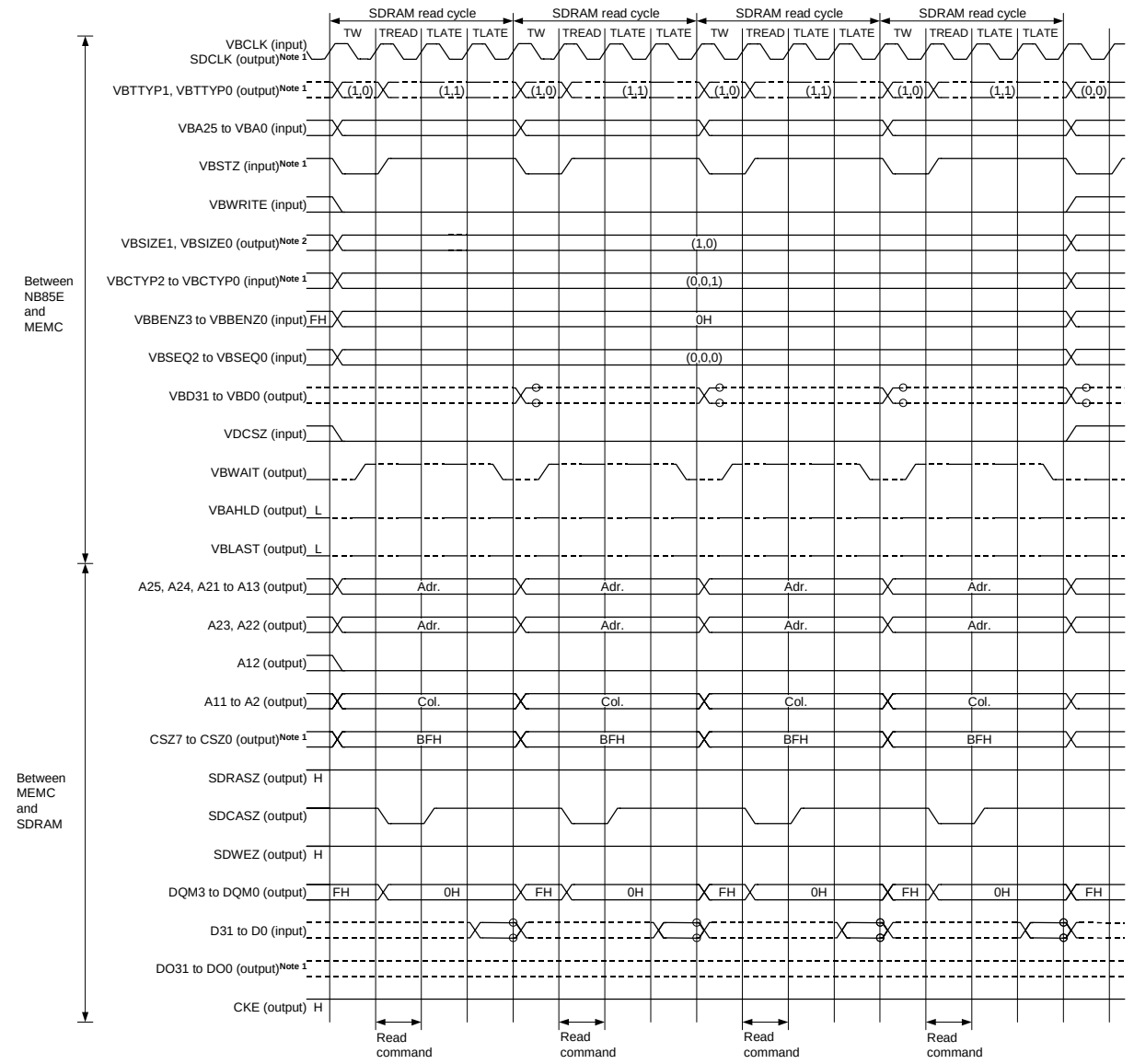


Notes 1. NU85E500 signal

2. NB85E signal. This signal is not connected to MEMC.

3. Invalid data for SDRAM is output.

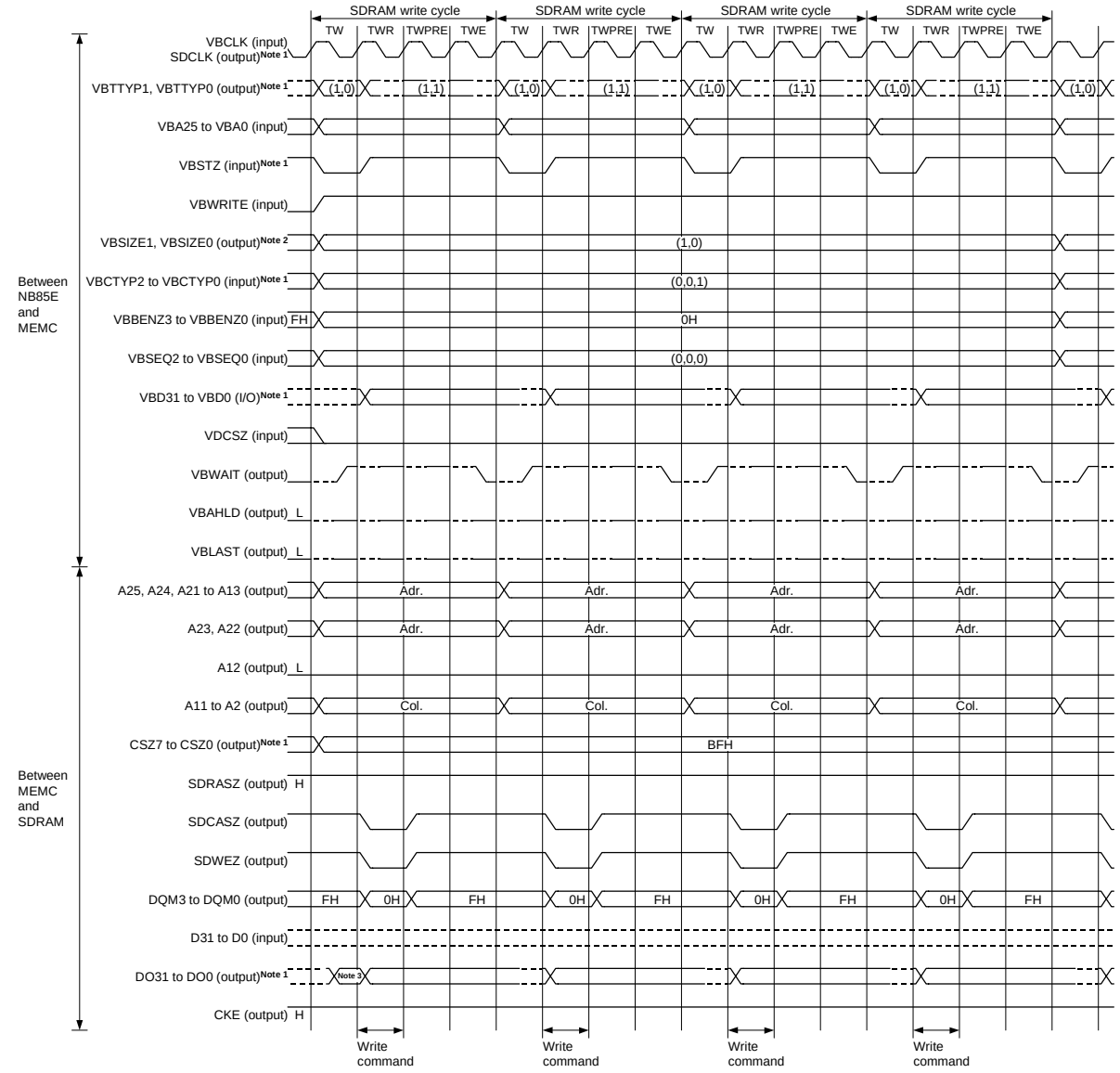
Figure 2-11. SDRAM Continuous Read Cycle (32-Bit Data Bus, Word Access, On-Page)



Notes 1. NU85E500 signal

2. NB85E signal. This signal is not connected to MEMC.

Figure 2-12. SDRAM Continuous Write Cycle (32-Bit Data Bus, Word Access, On-Page)

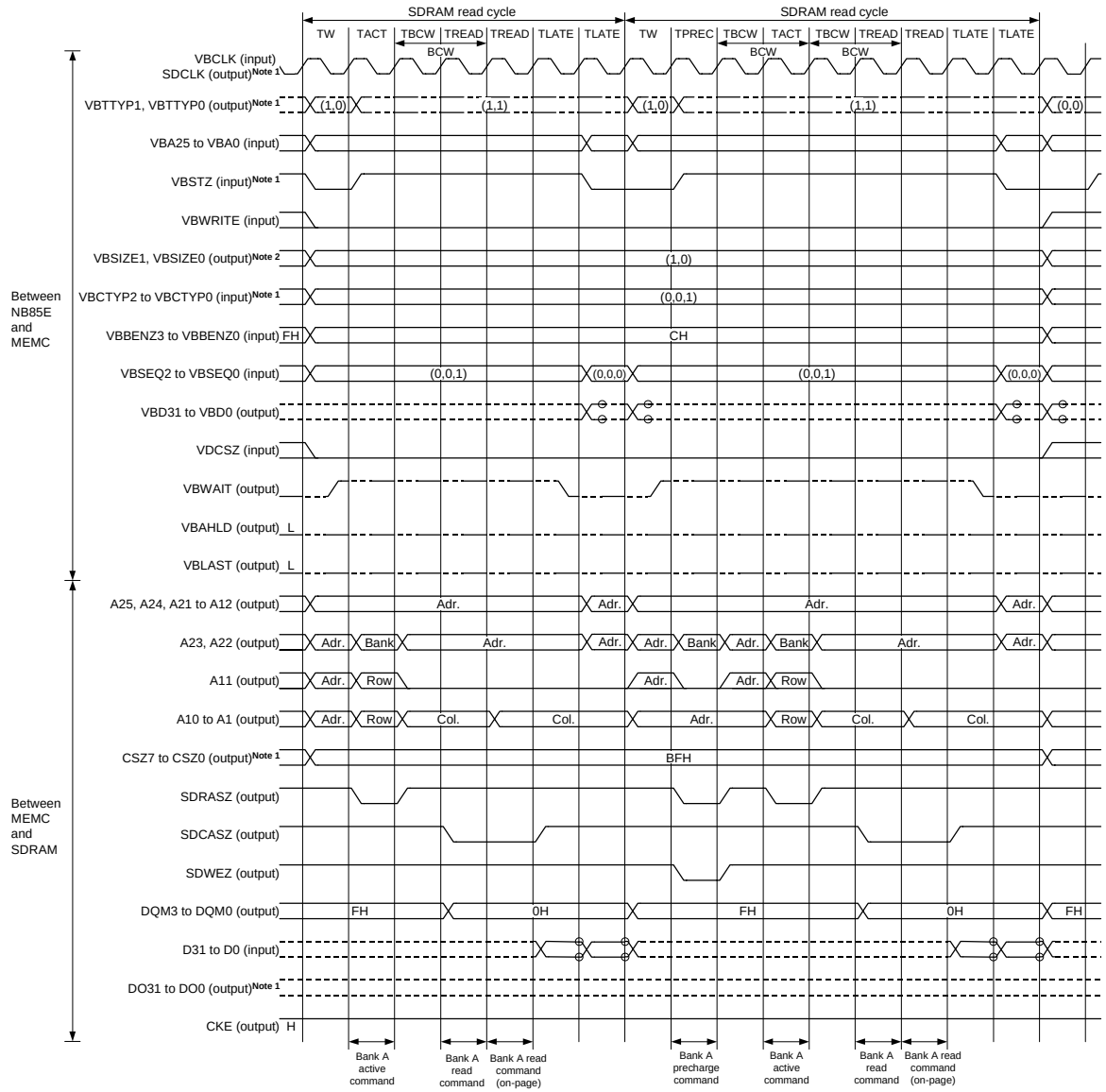


Notes 1. NU85E500 signal

2. NB85E signal. This signal is not connected to MEMC.

3. Invalid data for SDRAM is output.

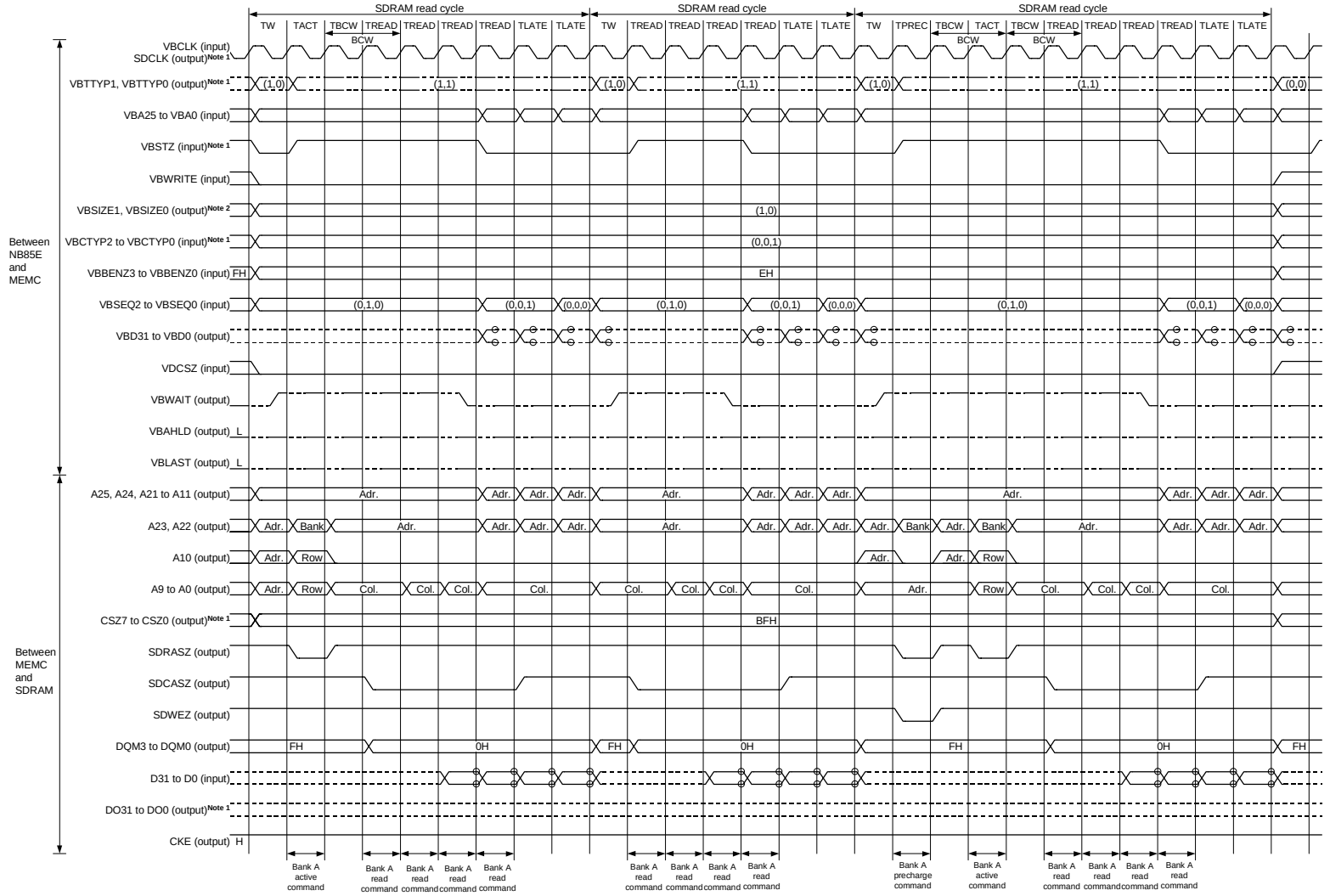
Figure 2-13. SDRAM Sequential Read Cycle (16-Bit Data Bus, Word Access, Page Change, CAS Latency = 2, BCW = 2)



Notes 1. NU85E500 signal

2. NB85E signal. This signal is not connected to MEMC.

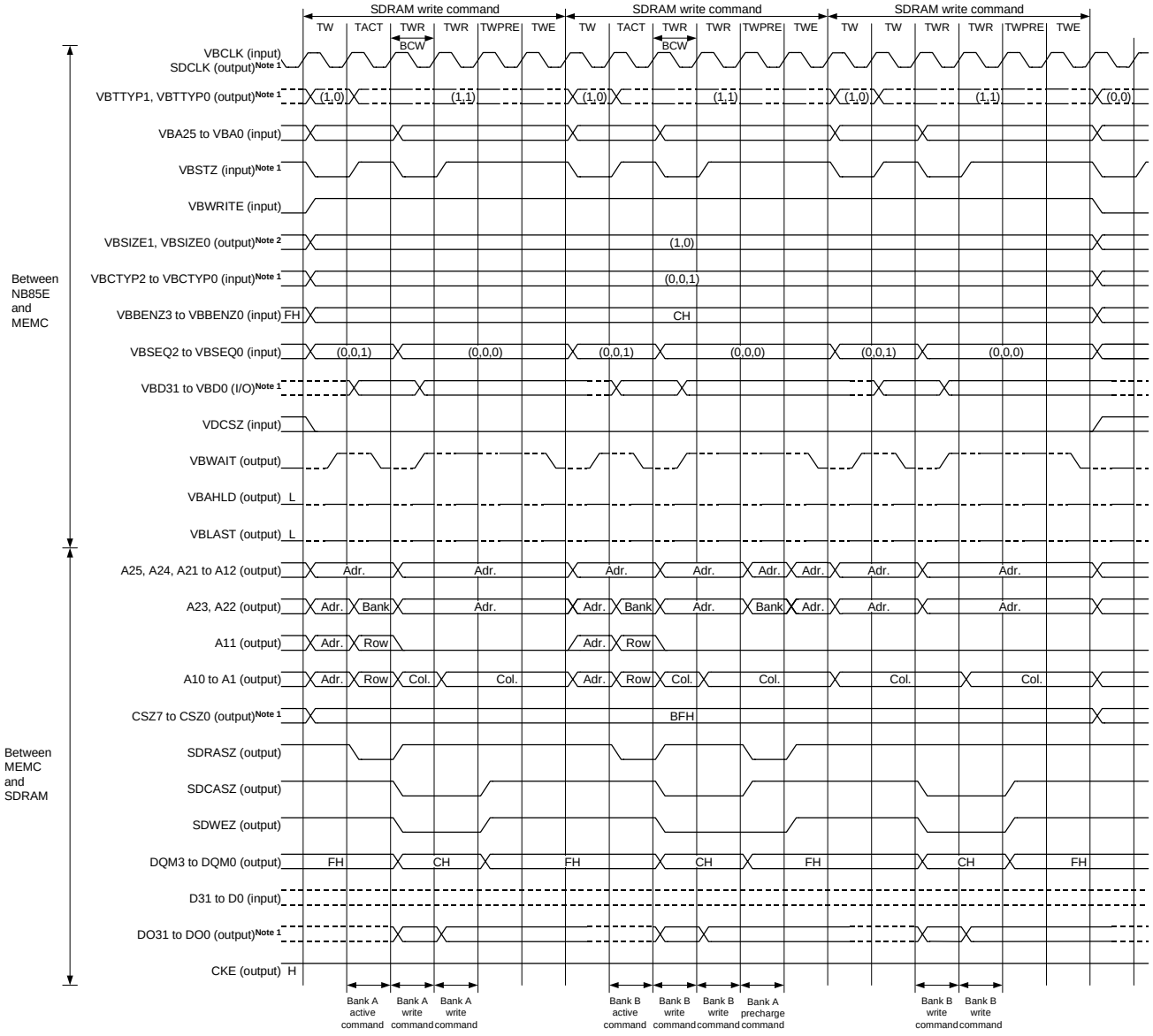
Figure 2-14. SDRAM Sequential Read Cycle (8-Bit Data Bus, Word Access, Page Change, CAS Latency = 2, BCW = 2)



Notes 1. NU85E500 signal

2. NB85E signal.
This signal is not connected to MEMC.

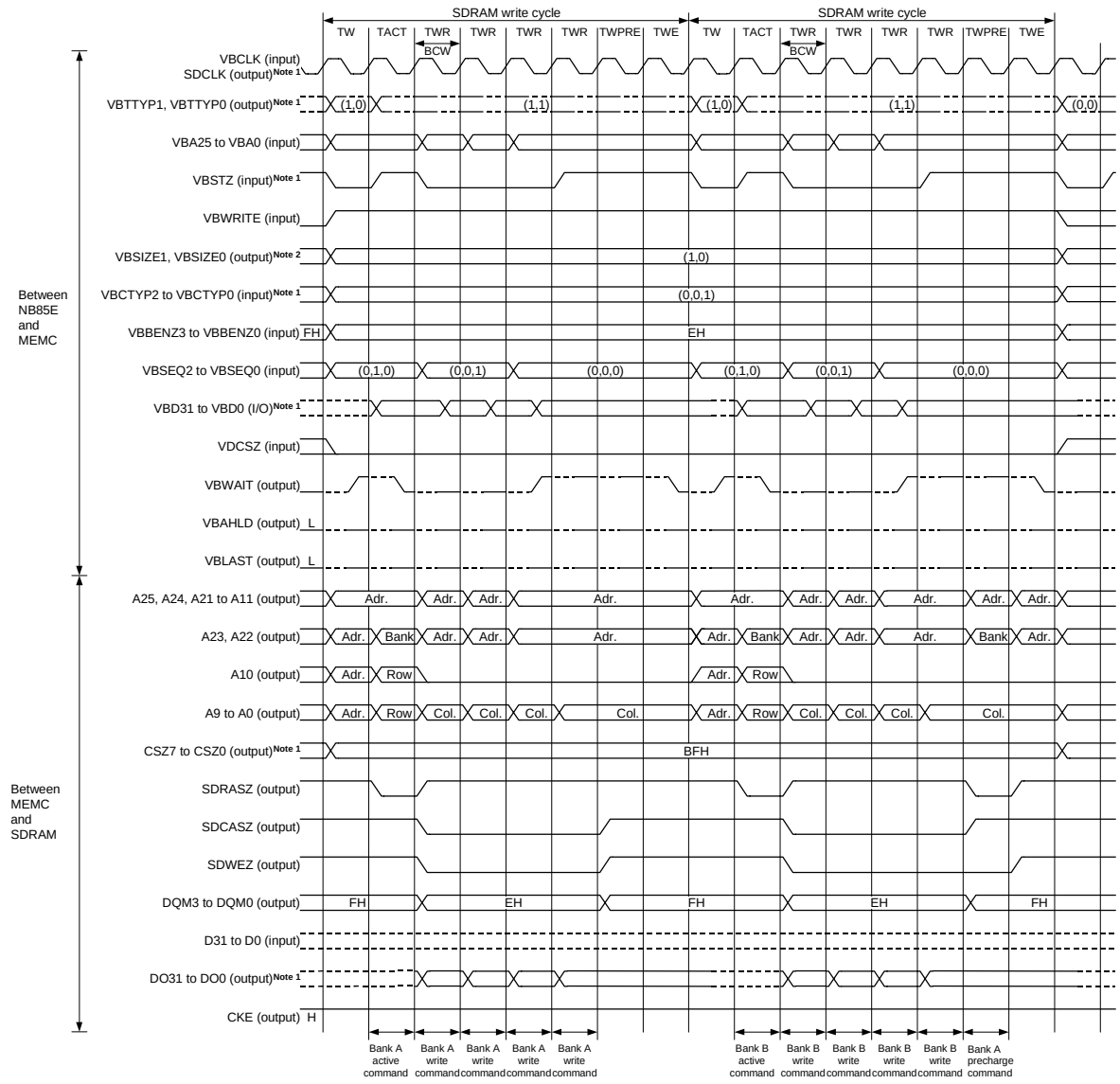
Figure 2-15. SDRAM Sequential Write Cycle (16-Bit Data Bus, Word Access, Bank Change, CAS Latency = 2, BCW = 1)



Notes 1. NU85E500 signal

2. NB85E signal. This signal is not connected to MEMC.

Figure 2-16. SDRAM Sequential Write Cycle (8-Bit Data Bus, Word Access, Bank Change, CAS Latency = 2, BCW = 1)



Notes 1. NU85E500 signal

2. NB85E signal. This signal is not connected to MEMC.

★

2.3.3 SDRAM refresh control register n (RFSn)

It is possible to generate an SDRAM CBR refresh cycle and a self-refresh cycle in the NU85E502. Refresh enable and the refresh interval are set by this register.

When more than one NU85E502 is incorporated in the system, settings can be made for each CSn area (n = 7 to 0).

This register can be read or written in 16-bit units.

Remarks 1. n of the register name corresponds to the CSn area number.

2. The address decoder is in the NU85E500. For the addresses of each CSn area, refer to the **NB85E Hardware User's Manual (A13971E)**.

Figure 2-17. SDRAM Refresh Control Register n (RFSn) (1/2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset
RFSn	REN	0	0	0	0	0	RCC1	RCC0	0	0	RIN5	RIN4	RIN3	RIN2	RIN1	RIN0	FFFFF4A2H + 4n	0000H

Bit position	Bit name	Description
15	REN	Sets refresh enable. REN: 0 = Refresh disabled; 1 = Refresh enabled
9, 8	RCC1, RCC0	Set the source clock factor for the refresh interval counter. RCC1 = 0, RCC0 = 0: Count source clock factor (Cfac) = 32 RCC1 = 0, RCC0 = 1: Cfac = 128 RCC1 = 1, RCC0 = 0: Cfac = 256 RCC1 = 1, RCC0 = 1: Setting prohibited **Remark** Refresh count clock (Trcy) = Cfac/ϕ ϕ: internal system clock (VBCLK)

Remark n = 7 to 0

Figure 2-17. SDRAM Refresh Control Register n (RFSn) (2/2)

Bit position	Bit name	Description
5 to 0	RIN5 to RIN0	Set the refresh interval factor.

RIN5	RIN4	RIN3	RIN2	RIN1	RIN0	Interval factor (Ifac)
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
:	:	:	:	:	:	:
1	1	1	1	1	1	64

★ **Caution To change the settings of the RFSn register, follow the procedure below (n = 7 to 0).**
<1> Clear (0) the REN bit.
<2> Set the new values to the RCC1, RCC0 and RIN5 to RIN0 bits and set (1) the REN bit.
In addition, when changing the refresh interval, set a value that allows a refresh to be performed in time during the interval change.

Table 2-4. Examples of SDRAM Refresh Intervals

Refresh Interval Prescribed Value (μs)	Refresh Count Clock (Trcy)	Interval Factor (Ifac)[Note]			
		When ϕ = 20 MHz	When ϕ = 33 MHz	When ϕ = 50 MHz	When ϕ = 66 MHz
15.6	32/ϕ	9 (14.4)	16 (15.5)	24 (15.4)	32 (15.5)
	128/ϕ	2 (12.8)	4 (15.5)	6 (15.4)	8 (15.5)
	256/ϕ	1 (12.8)	2 (15.5)	3 (15.4)	4 (15.5)

Note Values in parentheses indicate the calculated refresh interval values (μs).
Refresh interval (μs) = Trcy $\times$ Ifac

Remark ϕ : internal system clock (VBCLK)

★ 2.3.4 CBR refresh function

The NU85E502 activates a CBR refresh cycle for every refresh interval set to the RFSn register (n = 7 to 0).

(1) CBR refresh flow

<1> When a refresh request is generated from the settings of the RFSn register, a CBR refresh request is sent to the NU85E500 from the NU85E502.
<2> The NU85E500 outputs the VSB mastership request signal (VAREQ) to the NB85E.
<3> An acknowledge signal (VAACK) for the VAREQ signal is returned from the NB85E to the NU85E500.
<4> When the VAACK signal is received, the NU85E500 activates the REFRQZ signal from the rising edge of the VBCLK signal, and starts a CBR refresh.

(2) CBR refresh timing

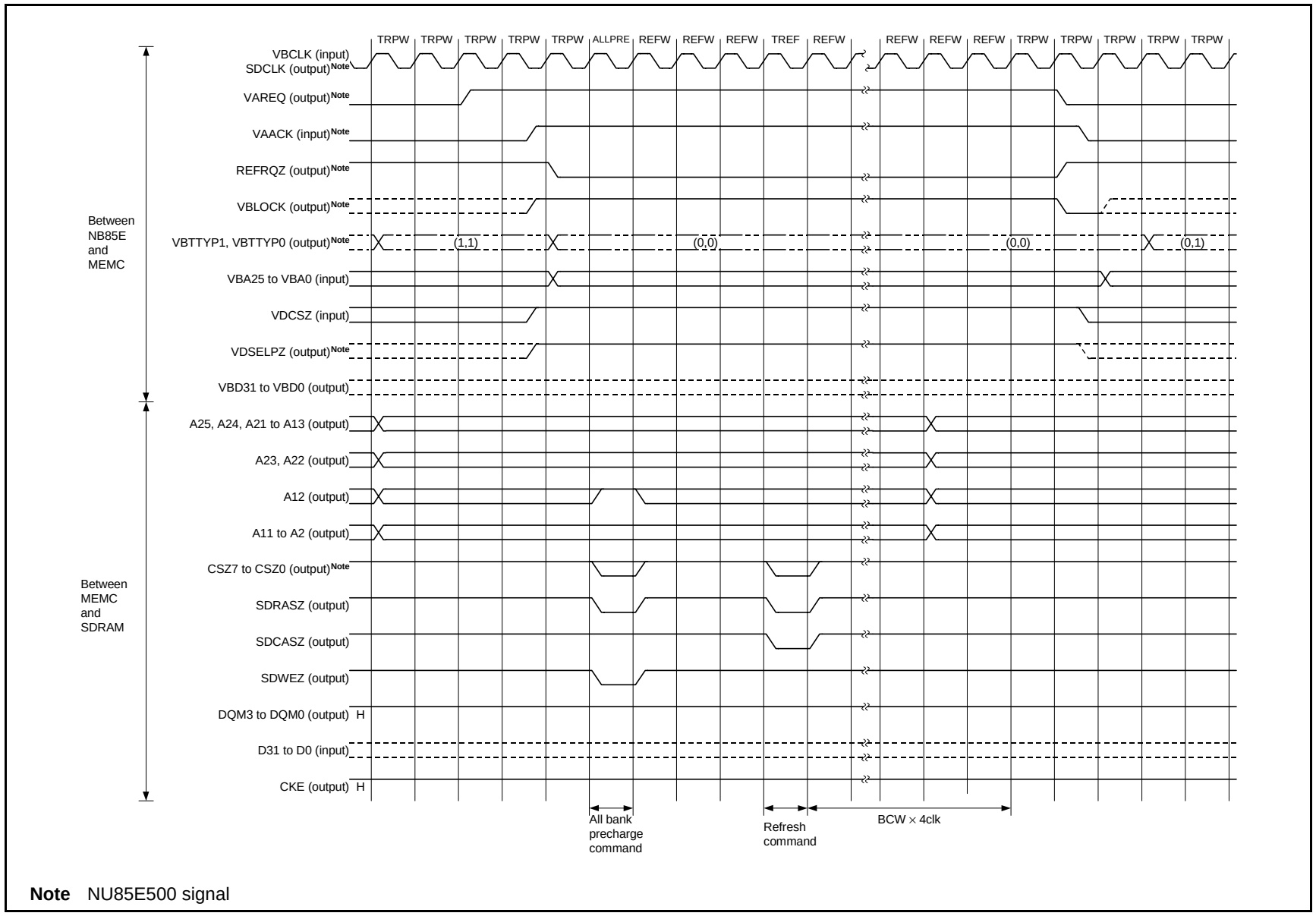
An example of CBR refresh timing is shown below.

Remarks 1. The level of broken-line portions indicates a weak unknown state; a state entered when the NB85E internal bus holder is driving.

2. For details of VSB signals (VBxxx, VDxxx), refer to the **NB85E Hardware User's Manual (A13971E)**.

3. BCW × 4clk: The number of wait states set by the BCW1 and BCW0 bits of the SCRn register × a 4-clock wait are inserted (n = 7 to 0).

Figure 2-18. SDRAM CBR Refresh Timing



Note NU85E500 signal

2.3.5 Self-refresh function

If either the NB85E undergoes a transition to STOP mode, or the SELFREF signal of the NU85E500 becomes active, the NU85E500 becomes the VSB bus master and the external SDRAM self-refresh cycle is started.

(1) Self-refresh flow

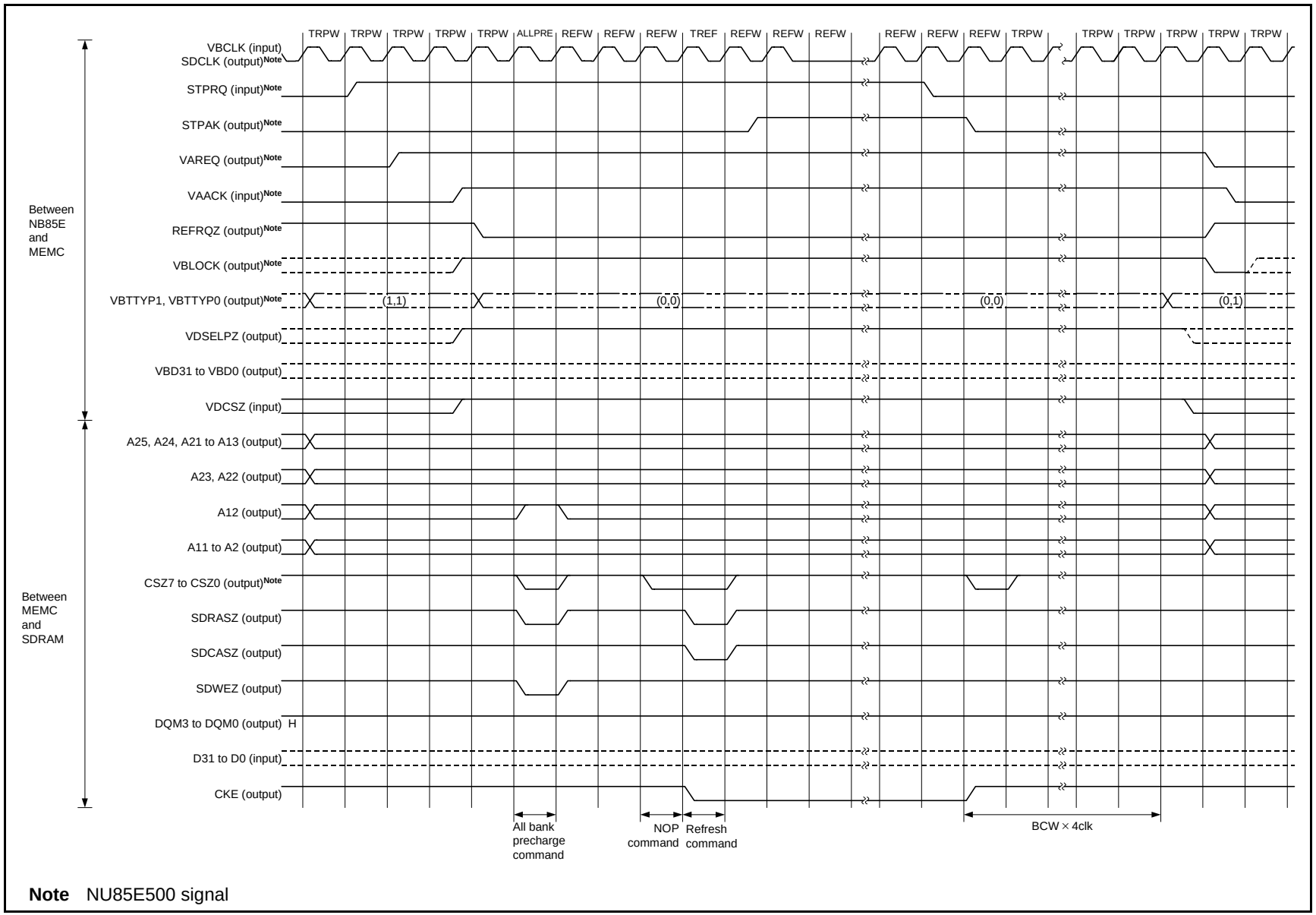
★ <1> Either a STOP mode request signal (STPRQ) is input to the NU85E500 from the NB85E, or a self-refresh request signal (SELFREF) is input to the NU85E500 from outside the NU85E500.
<2> The NU85E500 outputs a VSB mastership request signal (VAREQ) to the NB85E.
<3> The NB85E returns an acknowledge signal for the VAREQ signal (VAACK) to the NU85E500.
★ <4> After receiving the VAACK signal, the NU85E500 activates the REFRQZ signal from the rising edge of the next VBCLK signal, and starts a self-refresh.
<5> Transition into the self-refresh status in the entire SDRAM is completed.
<6> The NU85E500 returns an acknowledge signal for the STPRQ signal (STPAK) to the NB85E.
<7> The STPRQ signal becomes inactive.
<8> Suspension of self-refresh begins.
<9> Suspension of self-refresh in the entire SDRAM is completed.
<10> The VAREQ signal becomes inactive.
<11> Normal status resumes.

(2) Self-refresh timing

An example of self-refresh timing is shown below.

Remarks 1. The level of broken-line portions indicates a weak unknown state; a state entered when the NB85E internal bus holder is driving.
2. For details of VSB signals (VBxxx, VDxxx), refer to the **NB85E Hardware User's Manual (A13971E)**.
3. BCW × 4clk: The number of wait states set by the BCW1 and BCW0 bits of the SCRn register × a 4-clock wait are inserted (n = 7 to 0).

Figure 2-19. SDRAM Self-Refresh Timing



Note NU85E500 signal

★ 2.3.6 Notes on refresh function

The SDRAM refresh is not always performed in the interval set by the SCRn register.

If a refresh request is generated in the case below, the bus cycle ends and the refresh request is held pending until the NB85E500 secures bus mastership.

(1) When the NB85E operates as the bus master and the VSB bus cycle is generated

The following cases:

- While memory instruction fetch and data access (including NPB access) are being performed from the NB85E via the VSB.
- During DMA transfer using the VSB (held pending until the current DMA transfer ends in the case of single transfer, single-step transfer, and block transfer. In line transfer, held pending until the one line (four transfers) ends).
- During instruction cache and data cache refill (held pending until one-line refill (four words) ends when a miss-hit has been generated and one-line refill is performed from memory to the VSB. In the case of an instruction auto-fill, held pending until the one-line (four words) refill ends (since the VBLOCK signal becomes inactive, bus can be released every one line, so the refresh request can be acknowledged)).

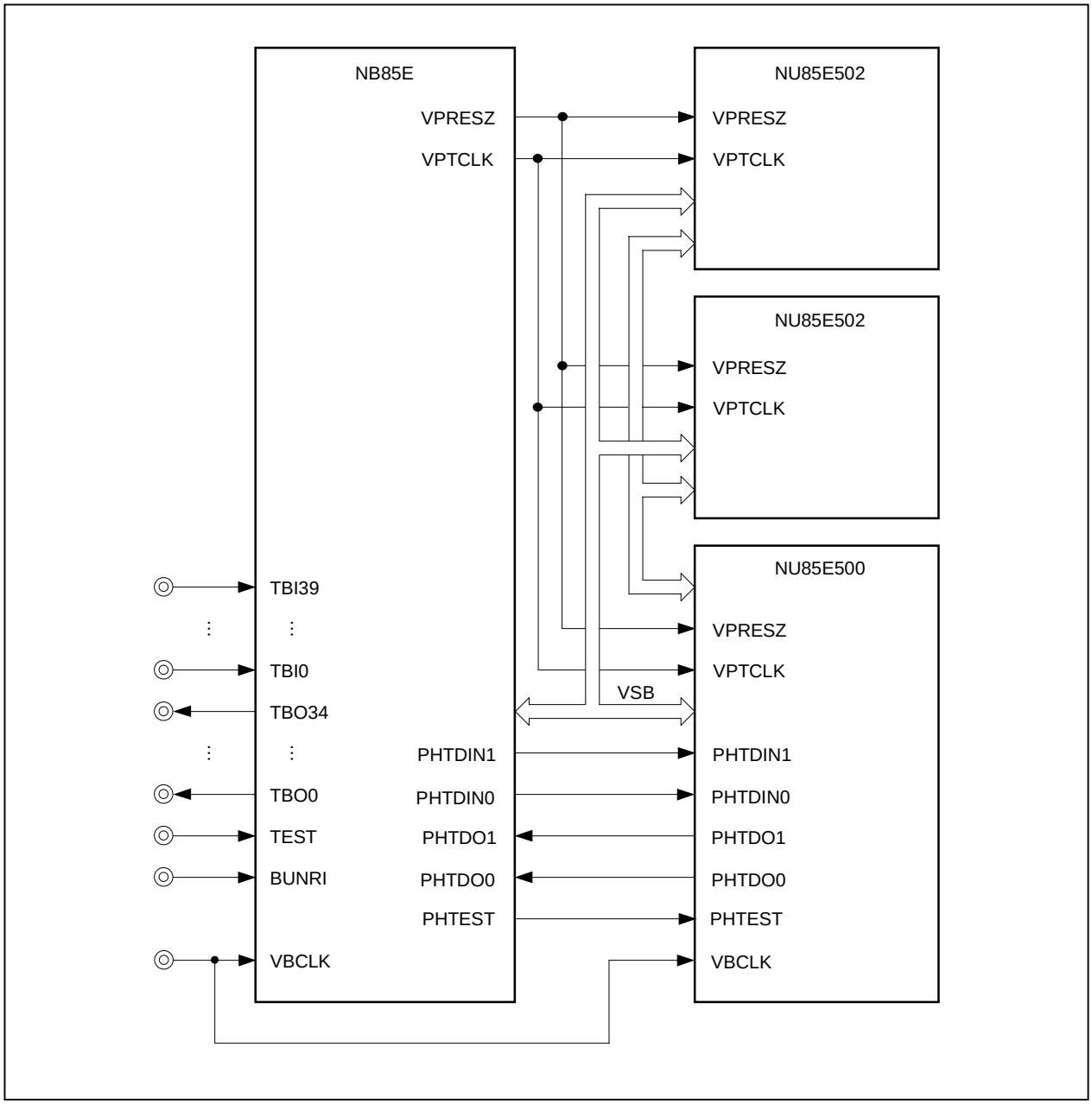
(2) In a bus hold state set by an external bus master

If a bus hold request and a refresh request conflict, the bus hold request takes precedence. When a refresh request is generated during a bus hold, the REFRQZ signal of the NU85E500 becomes active and refresh request generation notification can be sent to the external bus master. To shift to the refresh cycle, cancel the bus hold request using this signal. If no external devices can be the bus master and the HLDRQZ pin is fixed to high-level input, the bus hold request is not generated. So, in that case, it is not necessary to consider conflict with a bus hold.

2.4 Test Function

The NU85E502 can be tested using the NB85E test mode.
To test the NU85E502, connect it to the NB85E as follows.

Figure 2-20. Connection of NU85E502 to NB85E in Test Mode



Remark For details about test modes, refer to the **NB85E Hardware User's Manual (A13971E)**.

2.4.1 Pin processing when in test mode

(1) External memory connection pins

These operate the same in test mode as in normal mode. Refer to **2.2.4 Pin status** regarding the pin status. Input pins (D31 to D0) are ignored regardless of the values that are input.

(2) Test mode pins

Connect test mode pins to the NB85E as shown in Figure 2-20.

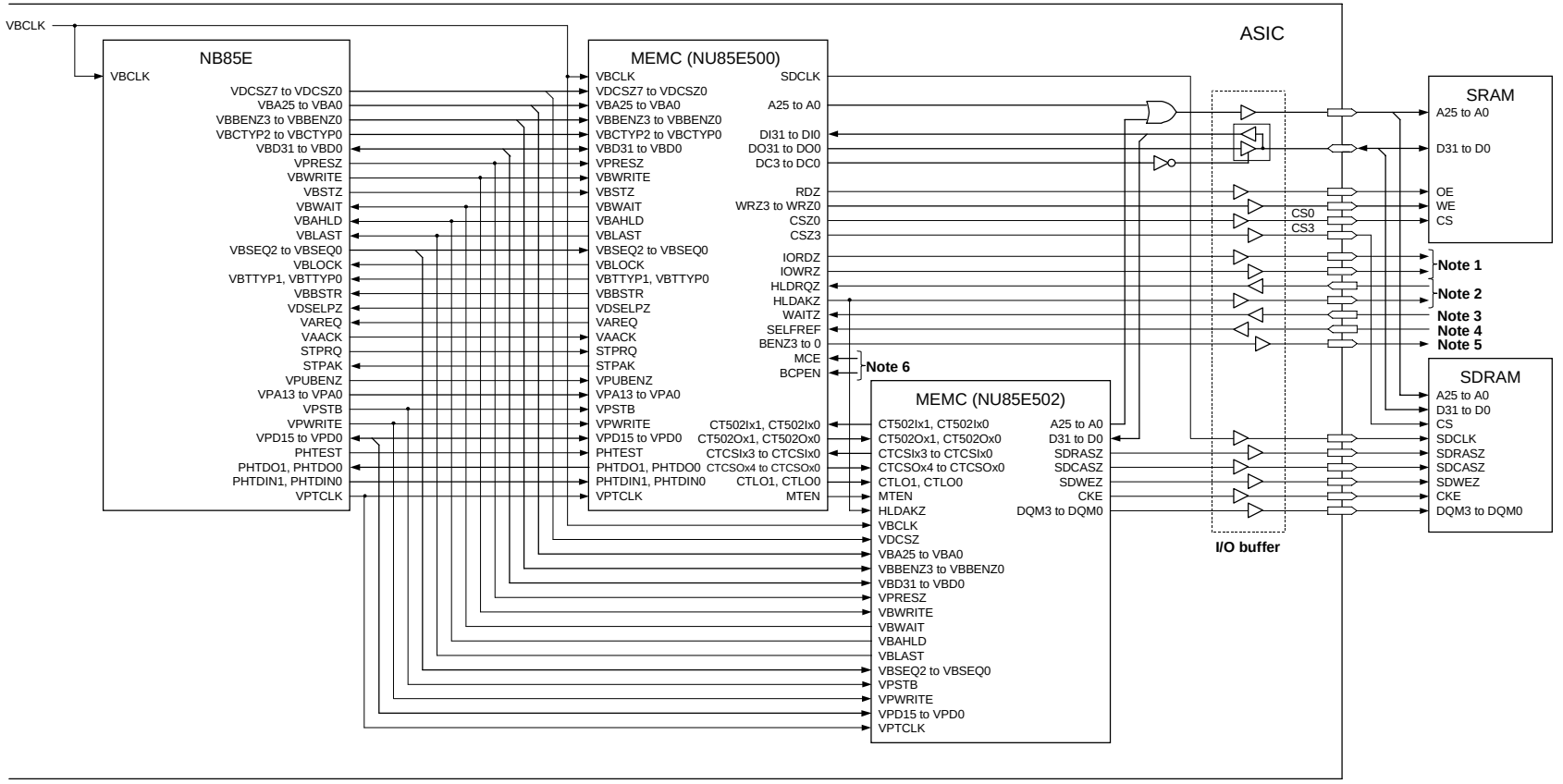
(3) Other pins

Make other pins the same as in normal mode. Refer to **2.2.4 Pin status** regarding the pin status.

APPENDIX A CONNECTION EXAMPLE

An example of the connection of the NB85E, MEMCs (NU85E500 and NU85E502), and external memories (SRAM and SDRAM) is shown below.

Figure A-1. Connection Example of NB85E, MEMCs (NU85E500 and NU85E502), and External Memories (SRAM and SDRAM)



Notes 1. Used for DMA flyby transfer

2. Used for bus hold cycle

3. Used for external wait control

Notes 4. Used for self-refresh request

5. When byte enable is used

6. For initial settings

★

APPENDIX B REVISION HISTORY

Revisions up to the previous edition are shown below. The “Page” column indicates pages in the older documents.

(1) 1st edition → 2nd edition

Page	Description
PREFACE	Addition of NB85ET as a target CPU core
Throughout	• Change of description “chip select” to “CSn area” • Change of name of SDRAM controller from “NB85E502” to “NU85E502”
pp.16, 18	Deletion of description regarding multiplexed bus
pp.24, 30	Change of pins MPXEN, ASTBZ, DSTBZ, MPXCZ, RDCYZ, and BUSST to NEC reserved pins
p.31	**1.2.3 Recommended connection of unused pins** Change of recommended connection method of pins A25 to A0, RDZ, WRZ3 to WRZ0, IORDZ, IOWRZ, CSZ7 to CSZ0, DC3 to DC0, D31 to D0, and CT501In2 (n = 7 to 0)
pp.32, 33	Addition of the pin status during a bus hold in **Table 1-1. Pin Status in Each Operating Mode**
p.34	Change of bits 14, 10, 6, and 2 to 0 fixed in **Figure 1-4. Bus Cycle Type Configuration Registers 0 and 1 (BCT0 and BCT1)**
p.37	Modification of remark in **1.3.4 Data wait control registers 0 and 1 (DWC0 and DWC1)**
p.39	Modification of **Figure 1-8. SRAM Connection Example**
pp.40 to 46	Modification of **1.3.5 (2) Bus timing**
p.49	Modification of **Figure 1-16. Page ROM Connection Example (for 16-Bit Data Bus)**
p.49	Modification of **Figure 1-17. Page ROM Connection Example (for 8-Bit Data Bus)**
pp.50 to 52	Modification of **1.3.7 (2) Bus timing**
p.54	Modification of **Figure 1-20. Bus Hold Timing**
p.56	Modification of **Figure 1-22. SRAM Read Timing (Bus Cycle Period Doubled)**
p.59	Modification of **Caution** and Figure in **1.4.1 (1) External memory connection pins**
p.98	Addition of **2.2.3 Recommended connection of unused pins**
p.98	Addition of the pin status during a bus hold in **Table 2-1. Pin Status in Each Operating Mode**
p.100	Modification of description regarding RHD bit in **Figure 2-4. DRAM Configuration Register n (DRCn)**
p.103	Modification of **Figure 2-6. 64-Mbit DRAM Connection Example**
p.104	Modification of **Figure 2-7. 16-Mbit DRAM Connection Example**
pp.105 to 119	Modification of **2.3.2 (2) Bus timing**
pp.121 to 124	Modification of DRAM read timing figures
p.129	Modification of **Figure 2-29. DRAM CBR Refresh Timing**
p.131	Modification of **Figure 2-30. DRAM Self-Refresh Timing**
p.143	Addition of **3.2.3 Recommended connection of unused pins**
p.144	Addition of the pin status during a bus hold in **Table 3-1. Pin Status in Each Operating Mode**
pp.149 to 153	Modification of **3.3.2 (2) Bus timing**
p.156	Modification of **Figure 3-11. SDRAM CBR Refresh Timing**
p.158	Modification of **Figure 3-12. SDRAM Self-Refresh Timing**
pp.161, 162	Addition of **APPENDIX CONNECTION EXAMPLE**

(2) 2nd edition → 3rd edition

Page	Description
Throughout	• Change of name of SDRAM controller from NB85E502 to NU85E502 • Deletion of description regarding DRAM controller (NB85E501)
p.16	Correction of **1.1.1 (2) Page ROM controller**
p.32	**Figure 1-3 Bus Cycle Type Configuration Registers 0 and 1 (BCT0 and BCT1)** Correction of description of BTn1 and BTn0 bits
p.34	Correction of **1.3.3 Bus cycle control register (BCC)**
p.51	Correction of **1.3.8 (1) Bus hold procedure**
p.52	Correction of **Figure 1-19 Bus Hold Timing**
p.67	**Figure 1-29 (a) External data bus: 32 bits** Correction of second data transfer flow of address 4n + 2 to be accessed
p.70	**Figure 1-30 (a) External data bus: 32 bits** Correction of address of data transfer flow of address 4n to be accessed
p.74	Correction of **2.1.1 Features**
pp.75, 78 to 80	Addition of description regarding HLDAKZ pin
p.81	Correction of **2.2.2 (3) (f) CKE** and **(g) DQM3 to DQM0**
pp.87 to 100	Modification of **2.3.2 (2) Bus timing**
p.103	Modification of **Figure 2-18 SDRAM CBR Refresh Timing**
p.105	Modification of **Figure 2-19 SDRAM Self-Refresh Timing**
p.106	Addition of **2.3.5 Bus hold function**

(3) 3rd edition → 4th edition

Page	Description
Throughout	Addition of descriptions on the NU85E500
pp.15 to 18	Addition of **1.1 Differences Between NB85E500 and NU85E500**
pp.37, 92, 110	Addition of **Cautions** on the BCT0, BCT1, SCR0 to SCR7, and RFS0 to RFS7 registers
p.59	Modification of the range of the bus hold status indicated by an arrow in **Figure 1-22 Bus Hold Timing**
p.81	Addition of description on the NU85E502 target CPU core
p.96	Modification of **Figure 2-7 Read/Write Data Flow for SDRAM**
pp.98 to 108, 111, 113	Modification of the SDRAM bus timing examples
p.106 in the 3rd edition	Deletion of **2.3.5 Bus hold function**
p.118	Modification of **Figure A-1 Connection Example of NB85E, MEMCs (NU85E500 and NU85E502), and External Memories (SRAM and SDRAM)**

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