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Preliminary User's Manual

Memory Controller

NA85E535, NBA85E535Vxx

Target CPU Cores

NU85EA
NU85ET
NDU85ETVxx

Document No. A15555EJ2V0UM00 (2nd edition)
Date Published October 2002 N CP(N)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Major Revisions in This Edition (1/2)

Page	Description
p.17	Addition of description to **1.2 (2) Page ROM connection function**
pp.17, 18	Addition of power-saving SDRAM connection function, **Caution**, and **Remark** to **1.2. (3) SDRAM connection function**
p.18	Addition of **1.2 (5) DMA acknowledge, chip select, and terminal count handling functions**
p.18	Change of description in **1.2 (7) Variable internal system clock function**
p.19	Change of **1.3 Symbol Diagram**
p.20	Change of **1.4.1 Internal block diagram**
p.21	Change of description in **1.4.2 (2) Divider block**
p.23	Addition of description to **1.4.2 (7) Data read control block**
p.27	Addition and change of description in **1.6 Comparison with NT85E500 and NT85E502**
pp.28 to 30	Change of **2.1 Pin Function List**
p.31	Addition of **Caution** to **2.2.1 (1) (b) VSA25 to VSA0**
p.34	Addition of transfer response to **Table 2-5 Transfer Response**
p.35	Addition of description and **Remark** to **2.2.1 (2) (b) VPRETR**
p.36	Change of description in **2.2.1 (3) (a) VBCLK**
p.36	Addition of **2.2.1 (3) (b) VBCLK2**
p.37	Change of description in **2.2.2 (2) CKMD1 and CKMD0**
p.37	Change of **Table 2-6 CKMD1 and DKMD0 Pins**
p.39	Addition of description to **2.2.3 (7) IORDZR and IORDZF**
p.39	Addition of description to **2.2.3 (8) IOWRZ**
p.40	Addition of **Caution** to **2.2.3 (15) BCYSTZ**
p.41	Change of description in **2.2.3 (18) BUSCLK**
p.41	Addition of **2.2.3 (19) BUSCLK2**
pp.41, 42	Addition of description to **2.2.3 (20) SDRASZ**, **(21) SDCASZ**, **(22) SDWEZ**, **(23) CKE**, and **(24) DQM3 to DQM0**
p.42	Change of **2.2.3 (26) ME7 to ME0** to external memory connection pins
p.43	Addition of description to **2.2.4 (2) DMTCOM3 to DMTCOM0**, **(4) DMACTVM3 to DMACTVM0**, **(6) DMXTCM13 to DMXTCM10 and DMXTCM03 to DMXTCM00**, and **(8) DMXCZM13 to DMXCZM10 and DMXCZM03 to DMXCZM00**
p.44	Addition of PHTDIN1, PHTDIN0, VPTCLK, PHTDO1, and PHTDO0 to **2.2.6 Pins reserved by NEC**
p.45	Change of **2.3 Connection of Unused Pins**
pp.46, 47	Change of **Table 2-8 Pin Status in Each Operation Mode**
pp.48, 49	Addition of BCP, ESCn register n to **Table 3-1 Control Register List**
p.53	Addition of **3.1.4 Flyby transfer strobe control register (BCP)**
pp.64 to 66	Addition of **3.1.9 Setting register for MobileRAM expansion mode register n (ESCn)**
p.68	Addition of **3.1.10 (1) Recommended setting of speculative read function**
pp.69, 70	Change of **3.1.11 Bus mode control register (BMC)**
p.71	Addition of **Figure 3-14 Procedure of Setting PDWN Bit (1)**
p.71	Addition of **Figure 3-15 Procedure of Clearing PDWN Bit (0)**

Major Revisions in This Edition (2/2)

Page	Description
p.72	Addition of **Figure 3-16 Procedure of Setting CKM1 and CKM0 Bits**
pp.85, 86	Change and addition of description in **3.3 STOP Function**
p.86	Addition of **3.3 (2) Timing of setting/releasing STOP mode**
pp.87 to 90	Addition of **Figure 3-27 Timing of Setting/Releasing STOP Mode (Without SDRAM Setting)**
p.91	Addition of **Caution** to **3.4 Bus Hold Function**
p.92	Modification of **Figure 3-28 Bus Hold Timing**
pp.93 to 98	Addition of **3.5 Cautions**
pp.99 to 102	Addition of **Table 4-1 Examples of Memory Access Timing**
pp.104 to 118	Modification of **Figure 4-1 Example of SRAM Access Timing (a) to (i) and (k) to (o)**, and addition of **(j)**
pp.119 to 132	Modification of **Figure 4-2 Example of SDRAM Access Timing (a) to (l) and (n)**, and addition of **(m)**
pp.133 to 138	Modification of **Figure 4-3 Example of Page ROM Access Timing (a) to (d)**, and addition of **(e) and (f)**
pp.139 to 154	Addition of **Figures 4-4 to 4-13 Example of DMA Transfer Timing (Flyby Transfer)**
pp.155 to 178	Addition of **Figures 4-14 to 4-21 Example of DMA Transfer Timing (2-Cycle Transfer)**
p.179	Modification of **Figure 4-22 SDRAM CBR Refresh Timing**
p.180	Modification of **Figure 4-23 SDRAM Self-Refresh Timing (STOP Timing)**
p.181	Addition of **Figure 4-24 MobileRAM Deep Power Down Timing (STOP Timing)**
p.182	Modification of **Figure 4-25 SDRAM Mode Register Write Operation Timing**
p.183	Addition of **Figure 4-26 MobileRAM Expansion Mode Register Write Operation Timing**
p.127 in old edition	Deletion of **5.1 Test in Peripheral Test Mode of NU85E**
p.186	Addition of **5.2 Notes on Wiring Test Bus**
p.203	Modification of **Figure A-1 Example of Connecting CPU Core, NA85E535, and External Memory (SRAM or SDRAM)**

The mark ★ shows major revised points.

INTRODUCTION

Target Readers

This manual is intended for users who wish to understand the functions of the memory controllers NA85E535 and NBA85E535Vxx for the CBIC CPU cores NU85EA, NU85ET, and NDU85ETVxx, and to design application systems using these memory controllers.

- NA85E535 (CB-10 Family VX type): Target CPU core (NU85EA, NU85ET)
- NBA85E535Vxx (CB-12 Family M type): Target CPU core (NDU85ETVxx)

Purpose

This manual is intended to give users an understanding of the functions of the NA85E535 and NBA85E535Vxx.

Organization

This manual consists of the following chapters.

- Overview
- Pin functions
- Bus control function
- Examples of memory access timing
- Test function
- Data flow

How to Read This Manual

It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, microcontrollers, SRAM, page ROM, and SDRAM.

To understand the overall functions of the NA85E535 and NBA85E535Vxx
→ Read this manual in the order of the contents.

To learn the details of a function whose name is already known
→ Refer to **APPENDIX B GENERAL INDEX**.

To learn the functions of the NU85EA
→ Refer to **NU85E Hardware User's Manual (A14874E)**.

To learn the functions of the NU85ET and NDU85ETV14
→ Refer to **NU85ET Hardware User's Manual (A15015E)**.

Unless otherwise specified, the NA85E535 is treated as the representative memory controller in this manual. When using the NBA85E535Vxx, read the macro name of the memory controller (NA85E535) as "NBA85E535Vxx" and read the macro name of the DMA controller (NA85E300) as "NBA85E300Vxx". In addition, the NU85EA is treated as the representative CPU core in this manual. When using the NU85ET or NDU85ETVxx, therefore, read the CPU core name as NU85ET or NDU85ETVxx.

Conventions	Data significance:	Higher digits on the left and lower digits on the right
	Active low representation:	xxxZ (Z suffixed to a pin or signal name)
	Note:	Footnote for item marked with **Note** in the text
	Caution:	Information requiring particular attention
	Remark:	Supplementary information
	Numerical representation:	Binary … xxxx or xxxxB
		Decimal … xxxx
		Hexadecimal … xxxxH
	Prefix indicating power of 2 (address space and memory capacity):	
		K (kilo) … $2^{10} = 1024$
		M (mega) … $2^{20} = 1024^2$
		G (giga) … $2^{30} = 1024^3$
	Data type:	Word … 32 bits
		Halfword … 16 bits
		Byte … 8 bits

Related documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

• NU85E Hardware User's Manual	(A14874E)
• NU85ET Hardware User's Manual	(A15015E)
• CB-10 Family VX Type NU85E, NU85ET Design Manual	(A15401E)
• CB-10 Family VX Type Core Library for CPU Core, Peripheral Design Manual	(A15133E)
• HOW TO USE SDRAM User's Manual	(J0123N[Note])
• SYNCHRONOUS DRAM User's Manual	(J0124N[Note])

Note This is a document published by Elpida Memory, Inc. (http://www.elpida-memory.com/).

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CHAPTER 1 OVERVIEW

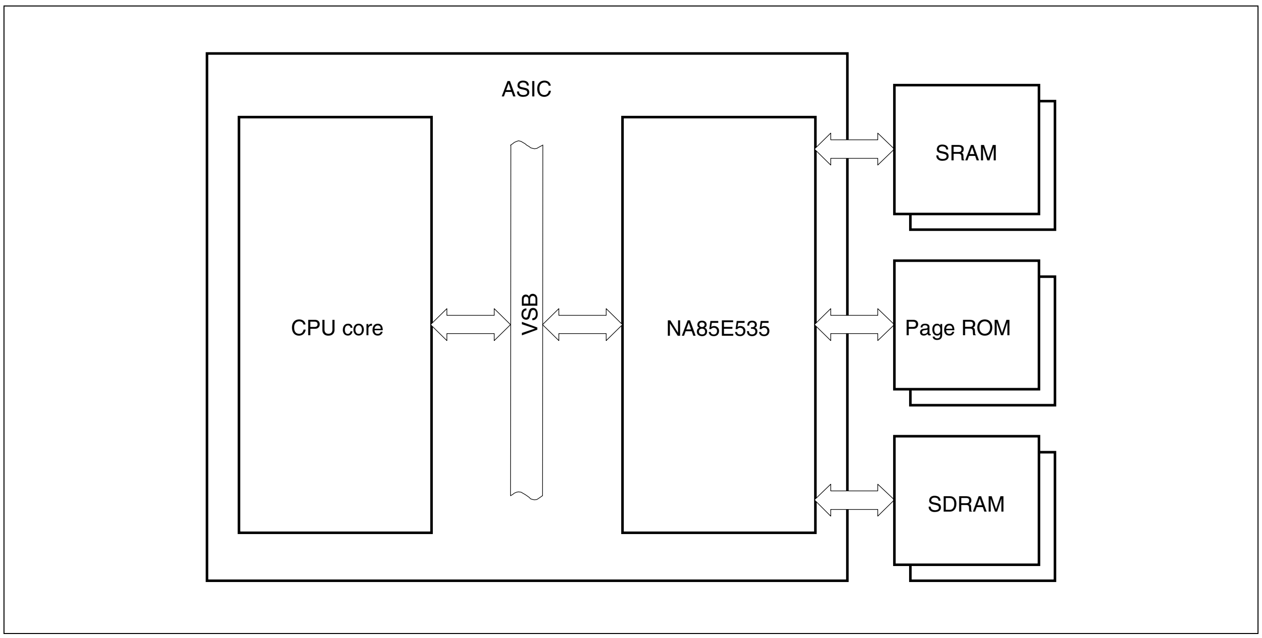
1.1 General

The NA85E535 is a macro that controls external memory and includes an SRAM/external I/O controller, a page ROM controller, and a synchronous DRAM (SDRAM) controller.

This macro can start an external bus cycle to access various memories when it is connected to a CPU core via the VSB.

When using the NA85E535, set the VSB data bus size to 32 bits regardless of the data bus width of the memory (set by using the bus size configuration register (BSC) register of the NU85EA).

Figure 1-1. Example of Connecting SRAM, Page ROM, and SDRAM



1.2 Features

(1) SRAM connection function

One SRAM/external I/O controller is provided that controls access to the SRAM (or external I/O) located in all CSn areas (n = 7 to 0). The major features of this SRAM/external I/O controller are as follows.

- Minimum 2-states access
- Insertion of up to seven data wait states by register setting
- Insertion of up to three address setting wait states by register setting
- Insertion of data wait by external pin input
- Insertion of up to three idle cycle states by register setting
- 2-cycle transfer and flyby transfer by DMA (SRAM → external I/O, external I/O → SRAM) supported

(2) Page ROM connection function

One page ROM controller is provided that controls access to the page ROM located in all CSn areas. The major features of this page ROM controller are listed below.

- Minimum 2-state access
- On-page identification function
  Change of address to be compared by register setting
  Insertion of up to seven off-page/on-page data wait states by register setting
- Read strobe signals (RDZR and RDZF) held active (low level) until a cycle in which the VSSEQ2 to VSSEQ0 signals, which indicate the end of sequential transfer, are 000, if a sequential access is requested by the CPU core.
- Insertion of data wait by external pin input
- 2-cycle transfer and flyby transfer by DMA (page ROM → external I/O) supported
- SRAM write cycle started if write cycle request is issued to CSn area where page ROM is located

Because the VSB data bus size is fixed to 32 bits, a VSB sequential access does not take place and on-page identification is not performed if a cache and an external bus master is not connected to the CPU core (however, access is executed on page if the speculative read function is used).

★ An efficient page access can be made to page ROM only when transfer is executed from page ROM to cache in a system with cache mounted, or when speculative read is set.

(3) SDRAM connection function

Four SDRAM controllers are provided that control access to the SDRAM located in the CS1, CS3, CS4, and CS6 areas. The major features of these SDRAM controllers are as follows.

- ★ Standard SDRAM (SDR SDRAM: Single data rate SDRAM) or power-saving SDRAM (MobileRAM) can be connected.
- Single-access-only can be activated (burst length = 1) (however, dummy accessing is executed by issuing a read/write command every clock if a continuous transfer is requested from a bus master, such as the CPU core, by VSSEQ2 to VSSEQ0 input).
- CAS latency = 1, 2, and 3 supported
- Insertion of up to three wait states by register setting
- Execution of register write operation each time SCRn register is accessed for write (n = 6, 4, 3, or 1).
- CBR (CAS-before-RAS) refresh command issued.
- 2-cycle transfer and flyby transfer by DMA (SRAM → external I/O, external I/O → SRAM) supported

★ **Caution** **SDR SDRAM and MobileRAM cannot be connected at the same time (must not be used together). Connect either of them.**

★ **Remark** Unless otherwise specified, both SDR SDRAM and MobileRAM are referred to as “SDRAM” in this manual.

(4) DMA flyby function

This function allows the DMA controller (DMAC) connected to the VSB to transfer data to external I/O when data is read from SRAM, page ROM, or SDRAM, and to transfer data to SRAM or SDRAM when data is read from the external I/O. Up to four external I/Os can be connected.

Up to seven data wait states and up to three idle states can be inserted by register setting.

★ **(5) DMA acknowledge, chip select, and terminal count handling functions**

After receiving an acknowledge signal, chip select signal, and terminal count signal input in synchronization with the system clock (VBCLK) and matching them with the actual DMA memory cycle (handled), each signal is output in synchronization with the bus clock (BUSCLK). (For the acknowledge signal and chip select signal, the active level is output only during flyby transfer. The inactive level is always output during 2-cycle transfer.)

(6) Speculative read/write buffer function

A read buffer and a write buffer consisting of 4 words (128 bits) are provided. If speculative read is enabled by line buffer control registers 0 and 1 (LBC0 and LBC1), data of up to 4 words can be read from addresses whose lower 4 bits are 0H to FH.

Remark In this manual, “32 bits” is defined as “1 word” and “4 words” is defined as “1 line”.

(7) Variable internal system clock function

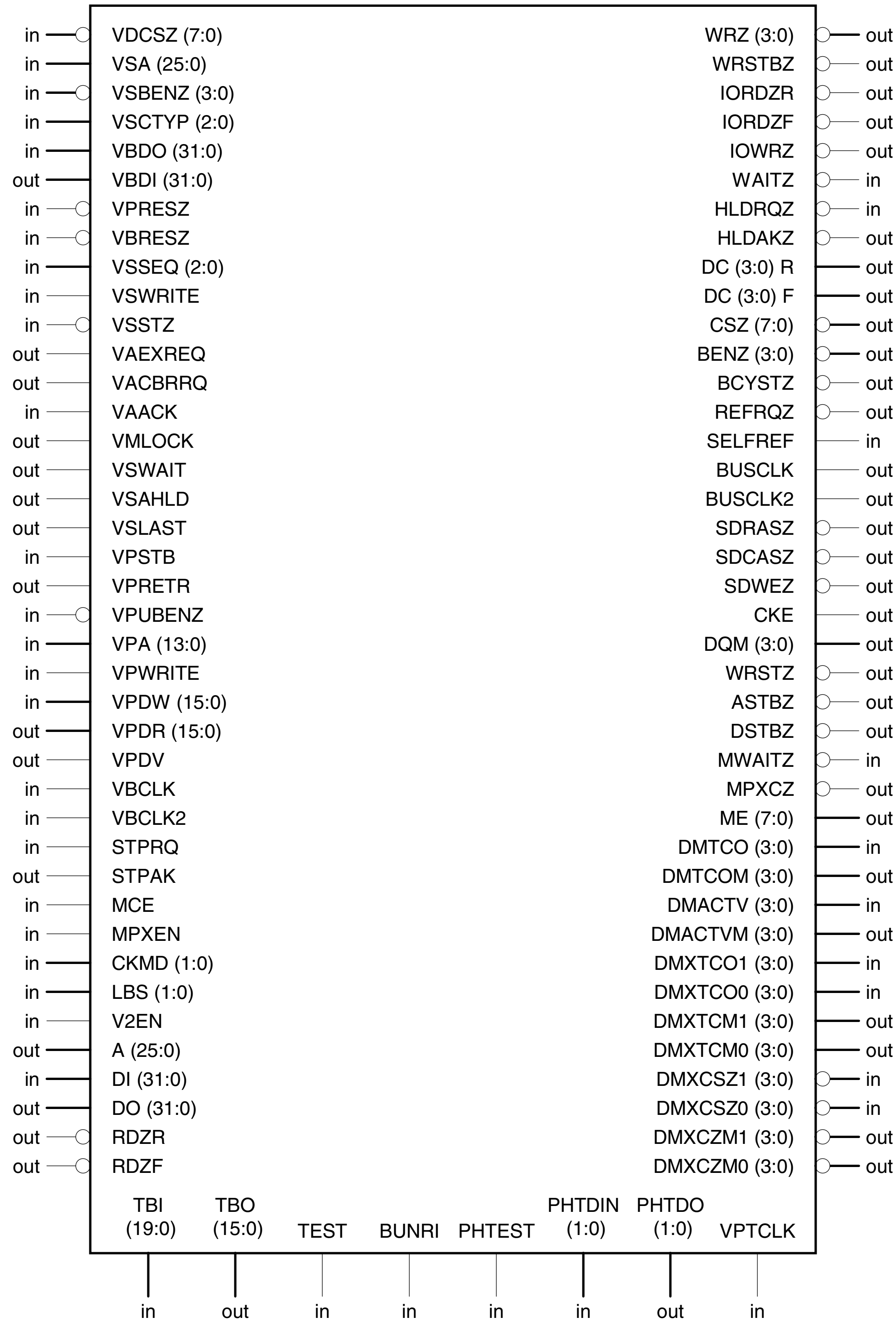
★ The memory controller can operate with a clock (internal system clock) that is divided by 1, 2, 3, or 4 for the system clock (VBCLK). The divided clock is output to an external device as bus clock by BUSCLK pin. The division ratio is determined at reset, according to the input levels of the CKMD1 and CKMD0 pins (the division ratio can be changed, after reset, by setting the BMC register).

Remark Only one internal system clock can be set for all memory controllers (it cannot be changed in each CSn area (n = 7 to 0)).

(8) Separate unit test function

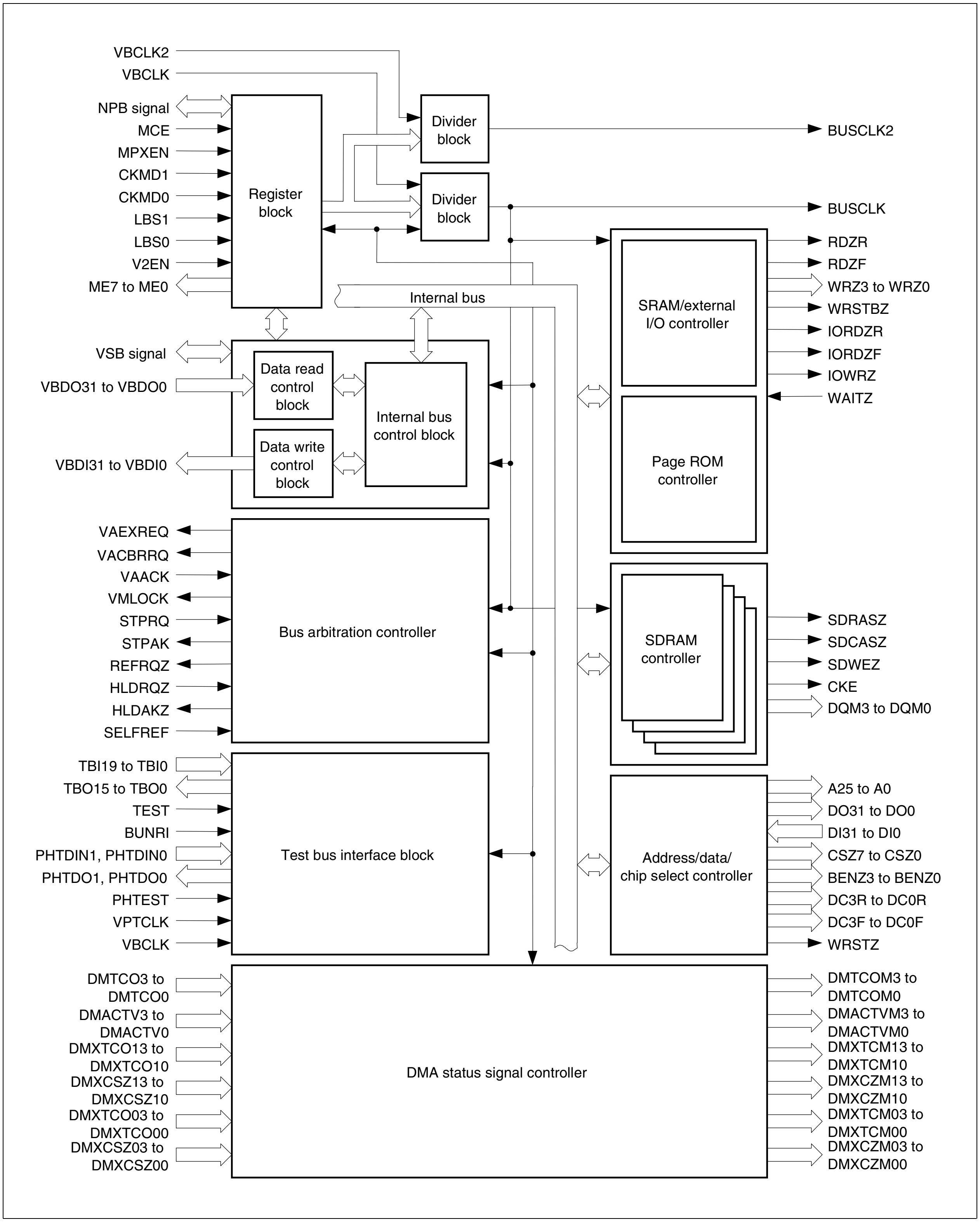
The NA85E535 can be set in separate unit test mode according to the combination of the signals of the TEST and BUNRI pins and its internal circuitry can be tested by using the test bus of the NA85E535.

★
1.3 Symbol Diagram



1.4 Block Diagram

★ 1.4.1 Internal block diagram



1.4.2 Internal units

(1) Register block

This block incorporates the registers that control the bus cycle. These registers are used to specify the operation of each controller, such as selecting an external memory type for each CSn area and setting the number of idle/wait states (n = 7 to 0).

The registers are read or written via the NPB.

(2) Divider block

★ This block divides system clocks (VBCLK, VBCLK2) input from external devices (the register that sets the division ratio is in the register block).

(3) SRAM/external I/O controller and page ROM controller

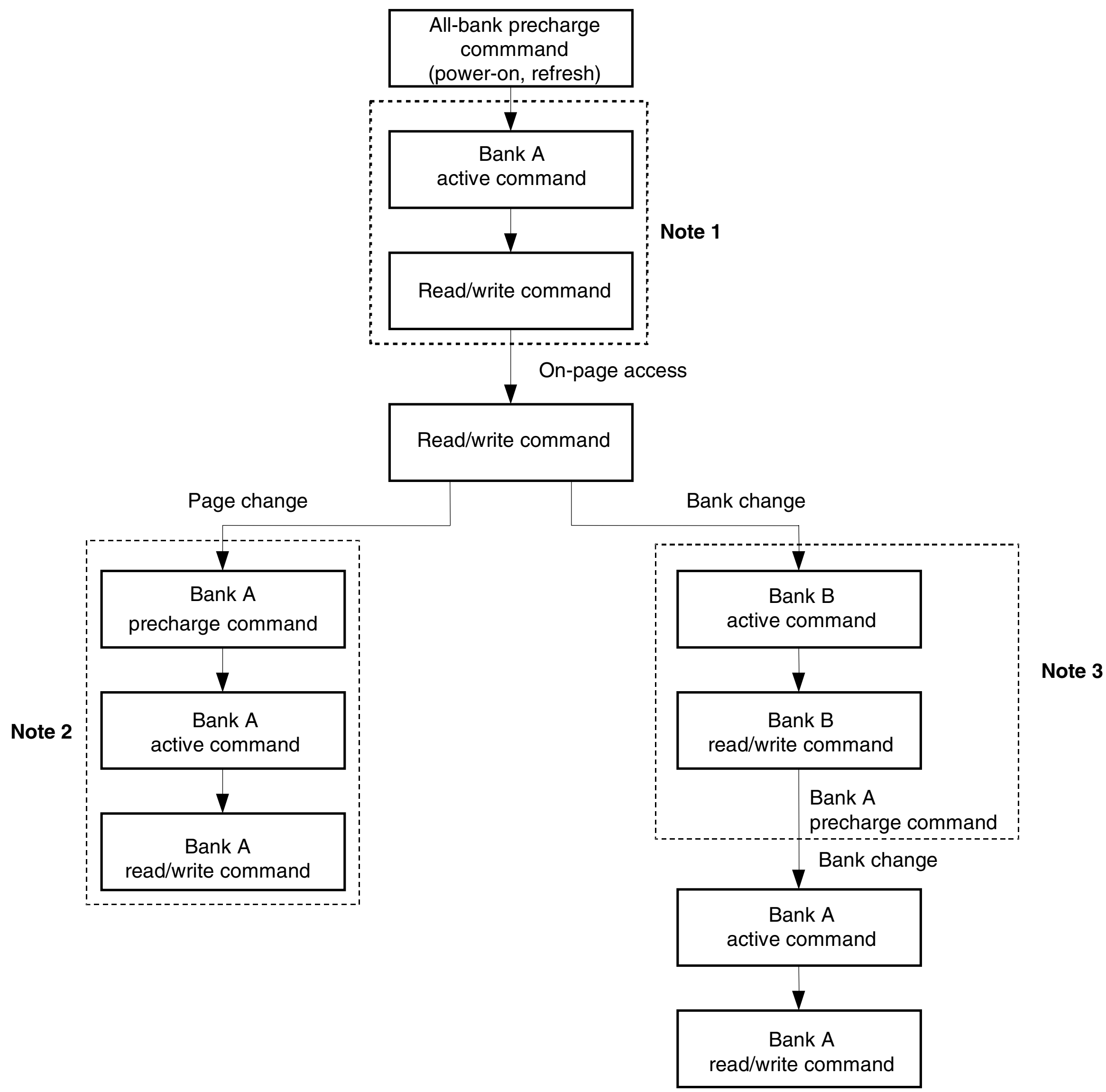
These controllers control reading and writing of SRAM, external I/O, and page ROM. They control access to all CSn areas (n = 7 to 0).

(4) SDRAM controllers

These controllers control read/write access to SDRAM, the register write cycle, and refresh. Four SDRAM controllers are available, corresponding to each of the CS1, CS3, CS4, and CS6 areas.

Commands issued to initialize SDRAM and to access memory (including commands that select pages and banks) are explained next (for the timing, refer to **Figure 4-2 Example of SDRAM Access Timing**).

Figure 1-2. Status Transition of SDRAM Access



Notes 1. An all-bank precharge command is always issued to SDRAM after power application and bus hold, or during refresh. When accessing SDRAM after this command has been issued, therefore, an active command and a read/write command are issued in that order.

2. If the page has been changed, a precharge command, active command, and read/write command are issued in that order.

3. If the bank has been changed, an active command and a read/write command are issued in that order to the bank to be accessed next. A precharge command is issued to the bank accessed immediately before the bank that is currently being accessed, immediately after the read/write command has been issued.

(5) Address/data/chip select controller

This controller controls the address and data bus signals that are output to the memory, and input/output of various control signals, in synchronization with the internal system clock (BUSCLK).

(6) Bus arbitration controller

This controller controls the bus mastership. Because the NA85E535 serves as a bus master, it asserts bus request signals (VAEXREQ and VACBRRQ) at the following timing.

- VAEXREQ signal: When a STOP mode request (STPRQ signal) is generated by the CPU core[Note]
  When a self-refresh request (SELFREF signal) is generated
  When an external bus hold request (HLDRQZ signal) is generated
- VACBRRQ signal: When a CBR refresh request is generated
  When an SDRAM mode register write command is issued

Note When the NA85E535 acknowledges the STPRQ signal, it outputs an acknowledge signal (STPAK) to the CPU core and stops operation (refer to **3.3 STOP Function** for details). When the NA85E535 acknowledges the STPRQ signal while SDRAM is connected to it, the memory controller executes a self-refresh cycle and then outputs the STPAK signal (refer to **Figure 4-23 SDRAM Self-Refresh Timing (STOP Timing)**).

(7) Data read control block

★ This block controls the local bus (bus connected from the NA85E535 to the external memory) in response to a data read access from the VSB.

It has a read buffer of one address stage and 4-word data × 32 bits and controls speculative read operations.

The speculative read condition can be specified by using the LBC0 and LBC1 registers. The read buffer discards its contents under the following conditions.

- Writing to BCT0 or BCT1 register
- Writing to LBS register
- Writing to LBC0 or LBC1 register
- Generation of bus hold
- Generation of DMA flyby cycle (not dependent on CS space)
- Memory write access to line address speculatively read

If data is written to the NPB during a speculative read operation, a retry request is generated by the VPRETR signal.

The speculative read range is the addresses (xxxxxx0H to xxxxxxFH) on the same line as the address that has been accessed (critical first access method).

For example, addresses “xxxxx00H”, “xxxxx04H”, and “xxxxx01H” are accessed in the following sequence, and data is loaded to the read buffer (when speculative read is executed with the local bus size of 32 bits).

- When accessing address “xxxxx00H”: xxxxx00H → xxxxx04H → xxxxx08H → xxxxx0CH
- When accessing address “xxxxx04H”: xxxxx04H → xxxxx08H → xxxxx0CH → xxxxx00H
- When accessing address “xxxxx01H”: xxxxx01H → xxxxx05H → xxxxx09H → xxxxx0DH

Remark Critical first access method is where the data necessary first is leaded when data of one line (4-word data equivalent to address “xxxxxx0H to xxxxxxFH”) is loaded from the external memory.

(8) Data write control block

This block controls the local bus in response to a data write access from the VSB.

It has a write buffer of four address stages, four chip select stages, and four data stages × 32 bits. This write buffer has four stages. If a write request is made when the buffer is full, a wait response continues to be output to the VSB until a vacancy is created in the buffer (until the cycle is completed once).

(9) Internal bus control block

This block controls the internal bus using the signals from the read control block and write control block.

The internal bus is connected from the internal bus control block to each of the internal controllers of the NA85E535 (the local bus is connected from the NA85E535 to the external memory).

Local bus sizing is performed in this block.

The width of the bus to which an external bus is to be connected can be set to 32, 16, or 8 bits by using the LBS register in each CSn area. When the data bus width is set to 16 or 32 bits, the lower address (A0 or A1, A0) cannot be used.

(10) DMA status signal controller

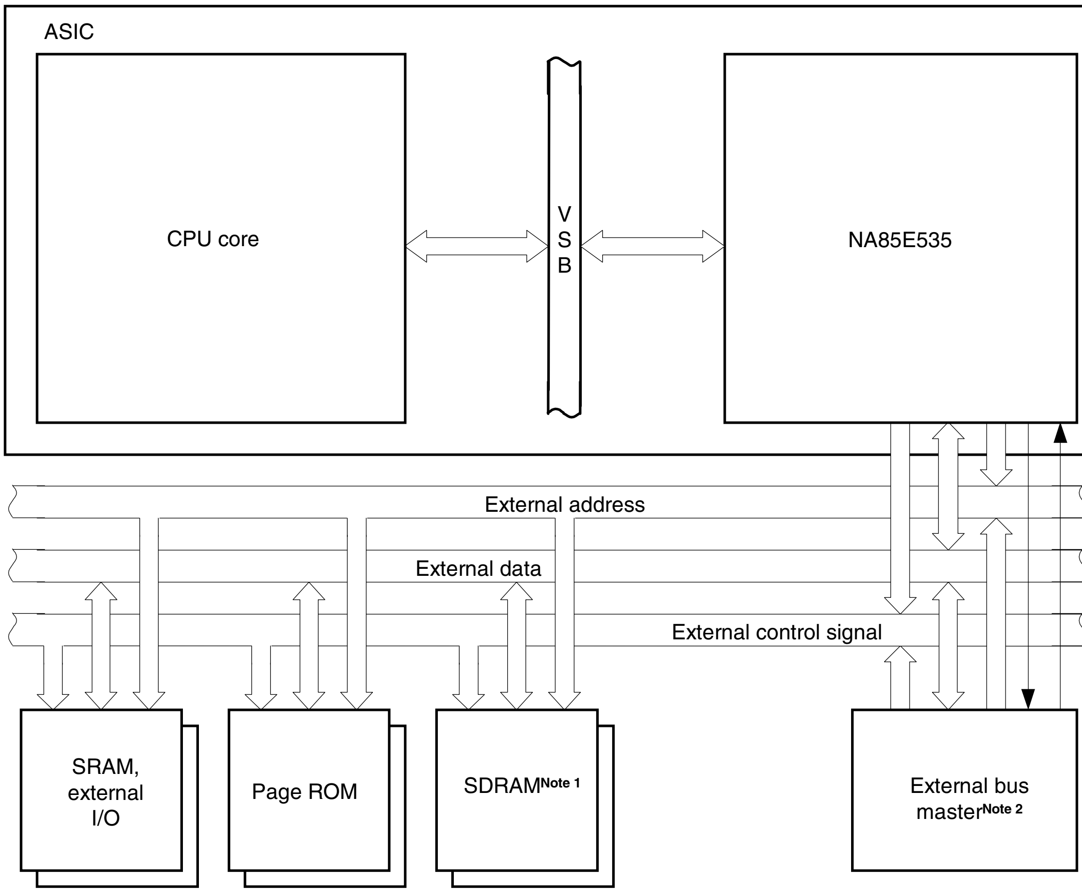
This controller outputs the status signals from the internal DMAC of the CPU core or an external DMAC connected to the CPU core (such as the NA85E300) to the external device in accordance with the bus cycle of the NA85E535.

(11) Test bus interface block

This block interfaces the signals that test the NA85E535.

1.5 System Configuration Example

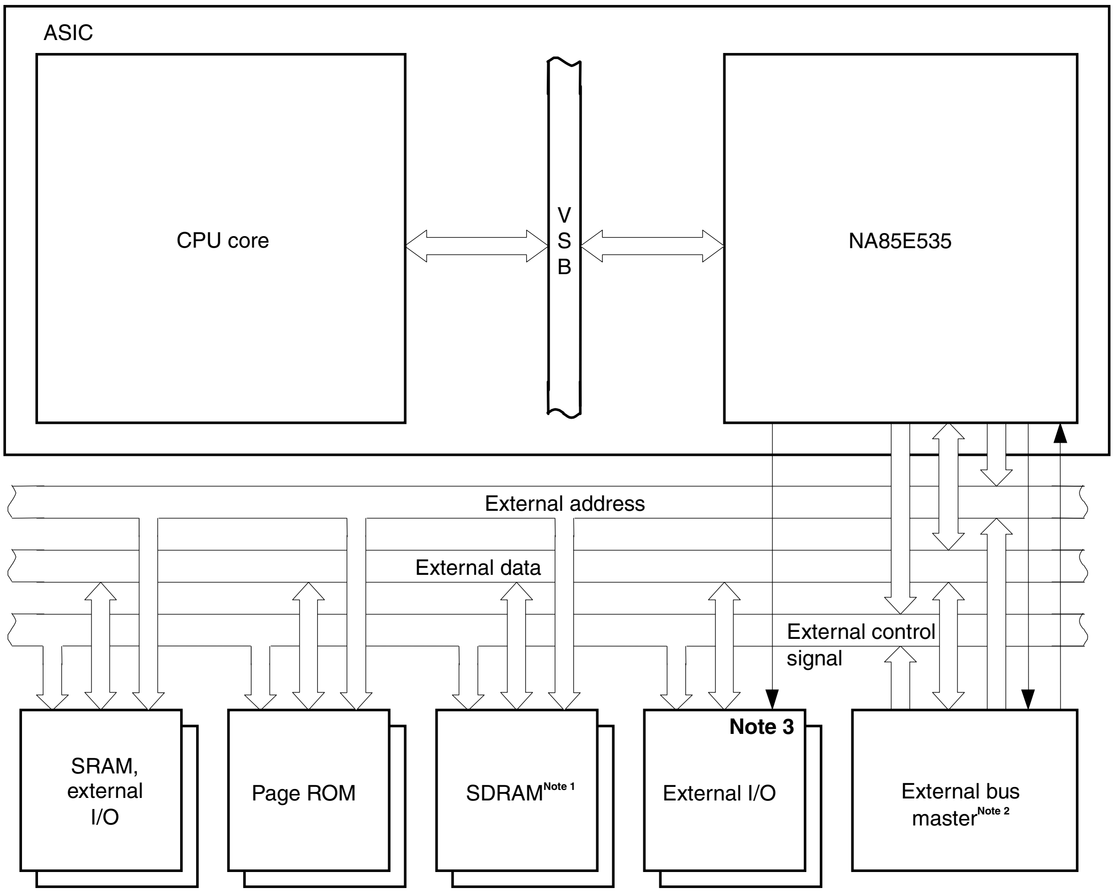
1.5.1 2-cycle transfer by DMA (without flyby transfer)



Notes 1. SDRAM with 11 to 13 row address lines, eight to 11 column address lines, and a CAS latency of 1 to 3 can be connected to the NA85E535.

2. The NA85E535 has an external bus master arbitration function that is controlled by the HLDRQZ and HLDAKZ signals.

1.5.2 Flyby transfer by DMA



Notes 1. SDRAM with 11 to 13 row address lines, eight to 11 column address lines, and a CAS latency of 1 to 3 can be connected to the NA85E535.

2. The NA85E535 has an external bus master arbitration function that is controlled by the HLDRQZ and HLDAKZ signals.

3. If the external I/O has a chip select function, the CSZn, DMACTVMx, DMXCZM1x, and DMXCZM0x pins are used (n = 7 to 0, x = 3 to 0).

1.6 Comparison with NT85E500 and NT85E502

The NA85E535 has a functionally enhanced configuration in that it is connected to four additional NT85E502 SDRAM controllers as compared with the NT85E500 external memory controller.

The differences from the NT85E500 and NT85E502, and the enhanced functions of the NT85E535 are listed below.

★ • Enables operation with the clock (internal system clock) which is divided by 1, 2, 3, or 4 for the system clock (VBCLK)
★ • Controls address bus signals and data bus signals that are output from the NA85E535 to the memory, and I/O of various control signals in synchronization with the internal system clock.
- Can connect SDRAM with 13 row address lines and 11 column address lines (the NT85E502 can connect SDRAM with 12 row address lines and 10 column address lines).
- CAS latency can be set to 1 to 3 during a read operation, by using SDRAM configuration register n (SCRn) (the latency of the NT85E502 is set to 2 or 3).
- Write access to the same page/bank of SDRAM is shorter by two clocks than that of the NT85E502.

★ • MobileRAM can be connected.
- Read buffer of 4 words is incorporated so that speculative read operations can be executed.
- Four stages (128 bits) write buffer is incorporated.
- Local bus sizing control register (LBS) is provided to change the size of the bus from VSB (32 bits) inside the NA85E535, in accordance with the data bus width of the memory to be accessed.
- Can start a DMA flyby cycle for SDRAM.
- Can set the number of data wait cycles and the number of idle wait cycles during DMA flyby transfer.

CHAPTER 2 PIN FUNCTIONS

2.1 Pin Function List

(1/3)

Pin Name		I/O	Function
CPU core connection pins	VDCSZ7 to VDCSZ0	Input	Chip select input (for VSB)
	VSA25 to VSA0	Input	Address input (for VSB)
	VSBENZ3 to VSBENZ0	Input	Byte enable input (for VSB)
	VSCTYP2 to VSCTYP0	Input	Bus cycle status input (for VSB)
	VBDO31 to VBDO0	Input	Data input (for VSB)
	VBDI31 to VBDI0	Output	Data output (for VSB)
	VPRESZ	Input	System reset input (for VSB)
	VSSEQ2 to VSSEQ0	Input	Sequential status input (for VSB)
	VSWRITE	Input	Read/write status input (for VSB)
	VSSTZ	Input	Transfer start input (for VSB)
	VAEXREQ	Output	Bus mastership request output other than CBR refresh (for VSB)
	VACBRRQ	Output	Bus mastership request output of CBR refresh (for VSB)
	VMLOCK	Output	Bus lock output
	VAACK	Input	Bus mastership acknowledge input (for VSB)
	VSWAIT	Output	Wait response output (for VSB)
	VSAHLD	Output	Address hold response output (for VSB)
	VSLAST	Output	Write response output (for VSB)
	VPSTB	Input	Data strobe input (for NPB)
	VPRETR	Output	Retry request output (for NPB)
	VPUBENZ	Input	Upper byte enable input (for NPB)
	VPA13 to VPA0	Input	Address input (for NPB)
	VPWRITE	Input	Write access strobe input (for NPB)
	VPDW15 to VPDW0	Input	Data input (for NPB)
	VPDR15 to VPDR0	Output	Data output (for NPB)
	VPDV	Output	Data output (VPDR15 to VPDR0) control output (for NPB)
★	VBCLK	Input	System clock input (for internal system clock, BUSCLK signal generation)
★	VBCLK2	Input	System clock input (for BUSCLK2 signal generation)
	STPRQ	Input	STOP mode request input
	STPAK	Output	Acknowledge output in response to STPRQ input
Initialization pins	MCE	Input	MEn bit reset value control input of BCT0 and BCT1 registers (n = 7 to 0)
	CKMD1, CKMD0	Input	Reset value control input of BMC register
	LBS1, LBS0	Input	Reset value control input of LBS register
	V2EN	Input	VSB specification selection input

(2/3)

Pin Name		I/O	Function
External memory connection pins	A25 to A0	Output	External memory address output
	DI31 to DI0	Input	External memory data input
	DO31 to DO0	Output	External memory data output
	RDZR	Output	SRAM/page ROM read strobe output (output at rising edge of BUSCLK signal)
	RDZF	Output	SRAM/page ROM read strobe output (output at falling edge of BUSCLK signal)
	WRZ3 to WRZ0	Output	SRAM/external I/O write strobe output
	WRSTBZ	Output	SRAM/external I/O write strobe output
	IORDZR	Output	External I/O read strobe output (output at rising edge of BUSCLK signal)
	IORDZF	Output	External I/O read strobe output (output at falling edge of BUSCLK signal)
	IOWRZ	Output	External I/O write strobe output
	WAITZ	Input	Wait request input
	HLDRQZ	Input	External bus hold request input
	HLDAKZ	Output	External bus hold request acknowledge output
	DC3R to DC0R, DC3F to DC0F	Output	Data bus control output
	CSZ7 to CSZ0	Output	Chip select output
	BENZ3 to BENZ0	Output	Byte enable output
	BCYSTZ	Output	Bus cycle start status output
	REFRQZ	Output	Refresh status output
	SELFREF	Input	Self-refresh request input
★	BUSCLK	Output	Bus clock output (generated from VBCLK)
★	BUSCLK2	Output	Bus clock output (generated from VBCLK2)
	SDRASZ	Output	SDRAM row address strobe output
	SDCASZ	Output	SDRAM column address strobe output
	SDWEZ	Output	SDRAM data write enable output
	CKE	Output	Clock enable output
	DQM3 to DQM0	Output	Data mask output
	WRSTZ	Output	Read/write status output of memory cycle
★	ME7 to ME0	Output	MEn bit value output of BCT0 and BCT1 registers (n = 7 to 0)
DMA pins	DMTCO3 to DMTCO0	Input	Terminal count input from internal DMAC (DMAC connected to CPU core)
	DMTCOM3 to DMTCOM0	Output	Terminal count output of internal DMAC cycle
	DMACTV3 to DMACTV0	Input	Acknowledge signal (DMAACK) input from internal DMAC
	DMACTVM3 to DMACTVM0	Output	Acknowledge signal (DMAACK) output of internal DMAC cycle

(3/3)

Pin Name		I/O	Function
DMA pins	DMXTCO13 to DMXTCO10, DMXTCO03 to DMXTCO00	Input	Terminal count input from NA85E300 (external DMAC connected to CPU core)
	DMXTCM13 to DMXTCM10, DMXTCM03 to DMXTCM00	Output	Terminal count output of NA85E300 cycle
	DMXCSZ13 to DMXCSZ10, DMXCSZ03 to DMXCSZ00	Input	Chip select signal input from NA85E300
	DMXCZM13 to DMXCZM10, DMXCZM03 to DMXCZM00	Output	Chip select signal output of NA85E300 cycle
Pins for separate unit test mode	TBI19 to TBI4	Input	Shift data input for separate unit test
	TBI3	Input	Reset input for separate unit test
	TBI2	Input	Clock input for separate unit test
	TBI1	Input	Chip select input for separate unit test
	TBI0	Input	Enable input for separate unit test
	TBO15 to TBO0	Output	Shift data output for separate unit test
	BUNRI	Input	BUNRI input for separate unit test
	TEST	Input	TEST input for separate unit test
Pins reserved by NEC	MPXEN	Input	Reserved by NEC (input a low level to this pin)
★	PHTEST	Input	
★	PHTDIN1, PHTDIN0	Input	
★	VPTCLK	Input	
★	VBRESZ	Input	Reserved by NEC (input a high level to this pin)
	MWAITZ	Input	
	ASTBZ	Output	Reserved by NEC (leave these pins open)
	DSTBZ	Output	
	MPXCZ	Output	
★	PHTDO1, PHTDO0	Output	

2.2 Pin Functions

2.2.1 CPU core connection pins

For details of each pin, refer to **NU85E Hardware User's Manual (A14874E)**.

(1) Pins for VSB

(a) VDCSZ7 to VDCSZ0 (input)

These are chip select pins. They input the VDCSZn signal for the CSn area set by the chip area select control registers (CSC0 and CSC1) of the CPU core (n = 7 to 0). For details, refer to **NU85E Hardware User's Manual (A14874E)**.

(b) VSA25 to VSA0 (input)

These pins form an address input bus for the VSB.

★ **Caution The NA85E535 does not support the VMA27 and VMA26 pins of the target CPU core and the VMA27 and VMA26 pins of the NA85E300 (nor does it support the VMA28 to VMA26 pins of the Nx85E2x (under development)). Therefore, up to 64 MB of space is supported for one CS area.**

(c) VSBENZ3 to VSBENZ0 (input)

These pins are active-low pins and indicate the valid byte data of the data bus (VBDI31 to VBDI0 and VBDO31 to VBDO0) divided into four.

Table 2-1. VSBENZ3 to VSBENZ0 Signals

Active (Low Level) Signal	Valid Byte Data
VSBENZ3	VBDI31 to VBDI24, VBDO31 to VBDO24
VSBENZ2	VBDI23 to VBDI16, VBDO23 to VBDO16
VSBENZ1	VBDI15 to VBDI8, VBDO15 to VBDO8
VSBENZ0	VBDI7 to VBDI0, VBDO7 to VBDO0

(d) VSCTYP2 to VSCTYP0 (input)

These input pins indicate the current bus cycle status.

Table 2-2. VSCTYP2 to VSCTYP0 Signals

VSCTYP2	VSCTYP1	VSCTYP0	Bus Cycle Status
0	0	0	Opcode fetch
0	0	1	Data access
0	1	0	Misalign access
0	1	1	Read-modify-write access
1	0	0	Fetching opcode of destination address of branch instruction
1	1	0	2-cycle DMA transfer
1	1	1	Flyby DMA transfer
1	0	1	(Reserved for future function expansion)

Remark 0: Low-level input, 1: High-level input

(e) VBDO31 to VBDO0 (input)

These pins form a data bus that inputs data from a macro connected to the VSB.

(f) VBDI31 to VBDI0 (output)

These pins form a data bus that outputs data to a macro connected to the VSB.

(g) VPRESZ (input)

This pin inputs the system reset signal output by the CPU core.

This signal asynchronously resets all registers (register settings are also reset).

(h) VSSEQ2 to VSSEQ0 (input)

These pins input a sequential status that indicates the transfer size during burst transfer.

They indicate “length of burst transfer” on starting burst transfer, “continuous” during burst transfer, and “single transfer” at the end of burst transfer.

Table 2-3. VSSEQ2 to VSSEQ0 Signals

VSSEQ2	VSSEQ1	VSSEQ0	Sequential Status
0	0	0	Single transfer
0	0	1	Continuous (indicates that the next transfer address is related to the current transfer address)Note
0	1	0	Continuous 4 times (length of burst transfer: 4)
0	1	1	Continuous 8 times (length of burst transfer: 8)
1	0	0	Continuous 16 times (length of burst transfer: 16)
1	0	1	Continuous 32 times (length of burst transfer: 32)
1	1	0	Continuous 64 times (length of burst transfer: 64)
1	1	1	Continuous 128 times (length of burst transfer: 128)

Note This is output in the middle of continuous transfer of 2 times, or 4, 8, 16, 32, 64, or 128 times.

Remark 0: Low-level input, 1: High-level input

During sequential transfer, start transfer from the start address shown in Table 2-4, according to the “number of transfers” value.

Table 2-4. Start Address for Sequential Transfer

VSSEQ2	VSSEQ1	VSSEQ0	Number of Transfers	Start Address
0	0	1	2	VSA25 to VSA0 = x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,0,0,0
0	1	0	4	VSA25 to VSA0 = x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,0,0,0,0
0	1	1	8	VSA25 to VSA0 = x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,0,0,0,0,0
1	0	0	16	VSA25 to VSA0 = x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,0,0,0,0,0,0
1	0	1	32	VSA25 to VSA0 = x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,0,0,0,0,0,0,0
1	1	0	64	VSA25 to VSA0 = x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,0,0,0,0,0,0,0,0
1	1	1	128	VSA25 to VSA0 = x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,x,0,0,0,0,0,0,0,0,0

Remark 0: Low-level input, 1: High-level input

When using the read buffer (when “speculative read” is specified by the LBC0 and LBC1 registers), transfer may not be executed correctly if it is started from an address other than the start addresses shown in Table 2-4. If the address sequence of the sequential transfer target is “xxxxx14H → xxxxx18H → xxxxx1CH → xxxxx20H”, for example, the address sequence in which an access is actually made is “xxxxx14H → xxxxx18H → xxxxx1CH → xxxxx10H”. This means that transfer returns to the first address (xxxxx10H) on the same line. This is because data (4 words) on the same line is always read when speculative read is executed.
When the read buffer is not used (when “no speculative read” is specified by the LBC0 and LBC1 registers), transfer is correctly executed even if it is started from an address other than those listed in Table 2-4.

(i) VSWRITE (input)

This input pin indicates the transfer direction.
A high level is input to this pin during write.

(j) VSSTZ (input)

This input pin indicates the start of transfer.

(k) VAEXREQ (output)

This pin outputs a bus mastership request signal as a result of a cause other than an SDRAM CBR refresh.
The VAEXREQ signal becomes active (high-level output) in the following cases.

- If a STOP mode request (STPRQ signal) is generated from the CPU core
- If a self-refresh request (SELFREF signal) is generated
- If an external bus hold request (HLDRQZ signal) is generated

(l) VACBRRQ (output)

This pin outputs a bus mastership request signal as a result of an SDRAM CBR refresh.
The VACBRRQ signal is also output when the SDRAM mode register write command is executed.

Remark If no other bus master except the CPU core is used, OR the VAEXREQ and VACBRRQ signals and input the result to the VAREQ pin of the CPU core.

(m) VAACK (input)

This pin inputs a signal that indicates that the bus mastership request signal (VAREQ) has been acknowledged.

(n) VMLOCK (output)

This output pin holds the bus mastership and is connected to the bus arbiter.
It is used to prohibit suspension of transfer due to an access by another bus master, between the current transfer and the next transfer.

(o) VSWAIT (output)

This pin indicates a wait response. It is connected to the VMWAIT pin of the CPU core.

The wait response is output to the bus master to request more bus cycles, because preparation for outputting data is not completed.

When this signal goes high, the bus cycle enters the wait status.

This signal is asserted when a wait response, address hold response, disconnect response, or busy response is output (the disconnect response and busy response are output when the V2EN bit of the BMC register is set to 1).

(p) VSAHLD (output)

This pin indicates an address hold response. It is connected to the VMAHLD pin of the CPU core.

The address hold response is output to the bus master to request more bus cycles when preparation for outputting data is complete.

This signal is asserted when the address hold response or busy response is output (the busy response is output when the V2EN bit of the BMC register is set to 1).

When this signal and VSWAIT signal go high, the bus cycle enters the address hold status.

In the address hold status, it is not necessary to latch an address because the address for data does not change even in the middle of the read/write cycle of that data. Consequently, the circuit can be simplified.

If 1 or more idle states are set in the NA85E535, the VSAHLD signal is asserted during the idle state at the end of the read cycle of SRAM, page ROM, or SDRAM.

(q) VSLAST (output)

This pin indicates a write response. It is connected to the VMLAST pin of the CPU core. This pin is used when the bus decoder requires a decode cycle.

This signal is asserted when the disconnect response or busy response is output (the disconnect response and busy response are output when the V2EN bit of the BMC register is set to 1).

In a system in which two or more external slave devices are connected and selected by a bus decoder, decoding to select the bus slave is usually executed during non-sequential transfer. Even if an attempt is made to change the slave device during sequential transfer such as burst transfer, therefore, a decode cycle to select the slave cannot be issued.

In this case, the slave device outputs a last response to notify the bus master that the slave select signal will change. The bus master transfers the next bus cycle by non-sequential transfer if it has received the last response from the slave device, so that a decode cycle can be issued.

Table 2-5. Transfer Response

VSWAIT	VSAHLD	VSLAST	Transfer Response
0	0	0	Ready response (status where current transfer is complete)
1	0	0	Wait response
1	1	0	Address hold response (holds address and control signal)
★ 1	0	1	Disconnect response[Note]
★ 1	1	1	Busy response[Note]

Note These responses are output when the V2EN bit of the bus mode control register (BMC) is set to 1 (the target CPU core does not have a disconnect response and a busy response).

Remarks 1. 0: Low level, 1: High level

2. The NA85E535 does not have a last response.

(2) Pins for NPB

(a) VPSTB (input)

This pin inputs the data strobe of the VPDW15 to VPDW0 signals.

(b) VPRETR (output)

This pin outputs a retry request for the NPB.

★ When a write access is made to the bus mode control register (BMC) or when a write request is issued to the NPB register of the NA85E535 while memory is being accessed, a retry request is issued.

★ **Remark** With the target CPU core, the retry request by the VPRETR signal is not valid unless a high level is input to the VPDACT pin. Therefore, connect an address decoder that outputs a high level to the VPDACT pin while all the on-chip NPB registers of the NA85E535 are being accessed to the CPU core, in the same manner as the other NPB peripheral macros (this address decoder does not have to be connected to the Nx85E2x (under development)).

(c) VPUBENZ (input)

This is the upper byte enable input pin. A low level is input to this pin when halfword data is accessed or when an odd address is accessed for byte data.

Input a high level to this pin to access an even address in byte units.

(d) VPA13 to VPA0 (input)

These pins input an address for the NPB. Specify the lower 14 bits of the address.

(e) VPWRITE (input)

This pin inputs the write access strobe of the VPDO15 to VPDO0 signals.

Input a high level to this pin during write.

(f) VPDW15 to VPDW0 (input)

These pins form a bus that inputs data from the CPU core.

(g) VPDR15 to VPDR0 (output)

These pins form a bus that outputs data to the CPU core.

(h) VPDV (output)

This pin outputs a signal that controls the data output (VPDR15 to VPDR0). It outputs a high level during read. When a bidirectional data bus is configured, this pin is connected to the enable pin of the three-state buffer connected to the data bus to control data output.

(3) System control pins

(a) VBCLK (input)

★ This pin inputs the system clock. Input a stable clock with a duty factor of 50% from the external clock generator to this pin.

★ **(b) VBCLK2 (input)**

This pin inputs a system clock that is used to generate the BUSCLK2 clock.

To improve the AC specification of the bus clock of a CBIC product, input a clock adjusting the delay value to the VBCLK signal.

Cautions 1. When the BUSCLK2 signal is not used, clock input to the VBCLK2 pin is not necessary (input a low level). However, be sure to input a clock to the VBCLK pin, regardless of whether the BUSCLK and BUSCLK2 signals are used or not.

2. Use the same clock generator for for both the VBCLK and VBCLK2 pins (use the common clock source).

3. The AC specification is defined for the delay difference between the VBCLK and VBCLK2 signals (contact NEC for details).

Remark The BUSCLK signal that uses the VBCLK signal as a source clock is output to an external device of the NA85E535 and is also used for the internal circuit. Therefore, the clock skew with the bus master of VSB must be adjusted and the delay value of the VBCLK signal input to the NA85E535 cannot be made extremely faster than other macros.

In contrast, the BUSCLK2 signal, which uses the VBCLK2 signal as a source clock, is a signal dedicated for the external output. It is therefore not necessary to adjust the clock skew of the clock input to the VBCLK2 pin with the other macros on the VSB (the output delay value of the bus clock output from a CBIC product can be improved).

(c) STPRQ (input)

This pin inputs a hardware/software STOP mode request from the CPU core.

(d) STPAK (output)

This pin inputs an acknowledge signal to the CPU core that has received the STPRQ signal.

2.2.2 Initialization pins

Caution Do not change the input level of the following pins during operation (fix the input level). Otherwise, the operation is not guaranteed.

(1) MCE (input)

This pin enables operation of the NA85E535 at reset.

Depending on the input level of this pin, the value of the MEn bits of the BCT0 and BCT1 register at reset (default value) changes as follows (n = 7 to 0).

- Low level: 0 (Operation of the NA85E535 in the CSn area is disabled (no response to the CPU core))
- High level: 1 (Operation of the NA85E535 in the CSn area is enabled)

Make sure that the input level of this pin does not change before and after reset.

(2) CKMD1 and CKMD0 (input)

★ These input pins are used to select the division ratio of the bus clock (BUSCLK/BUSCLK2) to the system clock (VBCLK/VBCLK2) input from an external source after reset (the divided VBCLK signal is also used as an internal system clock).

Depending on the input level of these pins, the value of the CKM1 and CKM0 bits of the BMC register (default value) changes as follows.

★ **Table 2-6. CKMD1 and CKMD0 Pins**

Input Level of CKMD1 and CKMD0 Pins		Value of CKM1 and CKM0 Bits After Reset (Default Value)		Division Ratio of BUSCLK/BUSCLK2 Signal for VBCLK/VBCLK2 Signal
CKMD1	CKMD0	CKM1 Bit	CKM0 Bit	
Low level	Low level	0	0	1/1 (VBCLK/VBCLK2 is divided by 1.)
Low level	High level	0	1	1/2 (VBCLK/VBCLK2 is divided by 2.)
High level	Low level	1	0	1/3 (VBCLK/VBCLK2 is divided by 3.)
High level	High level	1	1	1/4 (VBCLK/VBCLK2 is divided by 4.)

Make sure that the input levels of these pins do not change before and after reset.

(3) LBS1 and LBS0 (input)

These pins are used to set the data bus width for the memory to be accessed at reset.

Depending on the input levels of these pins, the value of the LBS register at reset (default value) changes as follows.

Table 2-7. LBS1 and LBS0 Pins

Input Level of LBS1 and LBS0 Pins		Value of LBS Register at Reset (Default Value)
LBS1	LBS0	
0	0	AAAAH (data bus width: 32 bits)
0	1	5555H (data bus width: 16 bits)
1	0	0000H (data bus width: 8 bits)
1	1	

Remark 0: Low-level input, 1: High-level input

Make sure that the input level of this pin does not change before and after reset.

(4) V2EN (input)

This pin selects the specification of the VSB that connects the NA85E535. Set this pin in accordance with the CPU core used. Input a low level to this pin if a CPU core specified in this manual is connected.

- NU85EA, NU85ET, NDU85ETVxx: 0 (low-level input)
- Nx85E2x (under development): 1 (high-level input)

Depending on the input level of this pin, the value of the V2EN bit of the BMC register at reset (default value) changes as follows.

- Low-level input: 0 (conforms to VSB specifications)
- High-level input: 1 (conforms to VSB2 specifications (support of bus reset, disconnect response, and busy response))

Make sure that the input level of this pin does not change before and after reset.

2.2.3 External memory connection pins

(1) A25 to A0 (output)

These pins form an address bus for external memory.

(2) DI31 to DI0 (input)

These pins form a data input bus for external memory.

(3) DO31 to DO0 (output)

These pins form a data output bus for external memory.

(4) RDZR and RDZF (output)

These pins output read strobe signals to make the SRAM and page ROM active.

The RDZR signal is asserted (low-level output) at the rising edge of the BUSCLK signal, and the RDZF signal is asserted (low-level output) at the falling edge of the BUSCLK signal.

When connecting a memory, AND the RDZR and RDZF signals and use the resultant signal.

(5) WRZ3 to WRZ0 (output)

These pins output write strobe signals to make the SRAM and external I/O active.

WRZ3 … For DO31 to DO24
WRZ2 … For DO23 to DO16
WRZ1 … DO15 to DO8
WRZ0 … DO7 to DO0

(6) WRSTBZ (output)

This pin outputs a write strobe signal to make the SRAM and external I/O active.

This signal is the result of ANDing WRZ3 to WRZ0.

(7) IORDZR and IORDZF (output)

These pins output read strobe signals to make the external I/O active in the DMA flyby cycle.

The IORDZR signal is asserted (low-level output) at the rising edge of the BUSCLK signal and the IORDZF signal is asserted (low-level output) at the falling edge of the BUSCLK signal.

★ The IORDZR signal and the IORDZF signals perform the same operation as the RDZR signal and RDZF signal, respectively, in a cycle other than the DMA flyby cycle, only when the IOEN bit of the flyby transfer strobe control register (BCP) is set to 1 (they do not operate when the IOEN bit is cleared to 0).

When connecting an external I/O, AND the IORDZR and IORDZF signals and use the resultant signal.

(8) IOWRZ (output)

This pin outputs a write strobe signal to make the external I/O active in the DMA flyby cycle.

It is asserted (low-level output) at the falling edge of the BUSCLK signal.

★ The IOWRZ signal performs the same operation as the WRSTB signal in a cycle other than the DMA flyby cycle only when the IOEN bit of the flyby transfer strobe control register (BCP) is set to 1 (it does not operate when the IOEN bit is cleared to 0).

(9) WAITZ (input)

This pin inputs a wait request from external memory.

(10) HLDRQZ (input)

This pin inputs a bus hold request from the external device.
It must be kept active during bus hold.

(11) HLDAKZ (output)

This pin outputs a bus hold acknowledge signal to an external device.
It indicates that bus hold is enabled.

(12) DC3R to DC0R and DC3F to DC0F (output)

These output pins control the direction of the I/O buffer of the data bus.

DC3R, DC3F … For DI31 to DI24, DO31 to DO24
DC2R, DC2F … For DI23 to DI16, DO23 to DO16
DC1R, DC1F … For DI15 to DI8, DO15 to DO8
DC0R, DC0F … For DI7 to DI0, DO7 to DO0

These pins output a high level during read and flyby transfer by DMA.
The DCnR signal is asserted (high-level output) at the rising edge of the BUSCLK signal, and the DCnF signal is asserted (high-level output) at the falling edge of the BUSCLK signal (n = 3 to 0).
When connecting an external I/O, AND the DCnR and DCnF signals and use the resultant signal.

(13) CSZ7 to CSZ0 (output)

These are chip select output pins.
They output the value input to the VDCSZ7 to VDCSZ0 pins.

CSZ7 … For CS7 area
CSZ6 … For CS6 area
CSZ5 … For CS5 area
CSZ4 … For CS4 area
CSZ3 … For CS3 area
CSZ2 … For CS2 area
CSZ1 … For CS1 area
CSZ0 … For CS0 area

(14) BENZ3 to BENZ0 (output)

These are byte enable output pins. They output the value input to the VMBENZ3 to VMBENZ0 pins of the CPU core.

(15) BCYSTZ (output)

This pin indicates the bus cycle start status.

★ **Caution A glitch is generated when SDRAM is successively accessed. Therefore, avoid circuit configuration in which an operation is performed in synchronization with an edge of the BCYSTZ signal (there is no problem when SRAM or page ROM is accessed).**

(16) REFRQZ (output)

This pin indicates the execution status of a refresh cycle to SDRAM.
It outputs a low level while the refresh cycle is being executed.
If this pin goes low during a bus hold, it indicates that a refresh request has been issued to the external bus master.

(17) SELFREF (input)

This pin inputs a self-refresh request.
The input level of this pin indicates the presence or absence of the self-refresh request.

- Low-level input: No self-refresh request has been generated.
- High-level input: Self-refresh request has been generated.

(18) BUSCLK (output)

★ This pin outputs the bus clock generated from the VBCLK signal.
It outputs a clock with the division ratio set by the CKMD1 and CKMD0 pins or the bus mode control register (BMC). The bus clock output from this pin is identical to the internal system clock.

★ **(19) BUSCLK2 (output)**

This pin outputs the bus clock generated from the VBCLK2 signal.
The theoretical operation of this pin is the same as the BUSCLK pin. However, the delay value of this pin is designed lower than that of the BUSCLK signal inside the NA85E535, use the clock output from this pin to improve the bus clock output delay.

(20) SDRASZ (output)

This pin outputs a row address strobe signal for SDRAM.
★ This pin always outputs a high level if SDRAM is not set as a memory connected (by the BCT0 and BCT1 registers).

(21) SDCASZ (output)

This pin outputs a column address strobe signal for SDRAM.
★ This pin always outputs a high level if SDRAM is not set as a memory connected (by the BCT0 and BCT1 registers).

(22) SDWEZ (output)

This pin outputs a data write enable signal for SDRAM.
★ This pin always outputs a high level if SDRAM is not set as a memory connected (by the BCT0 and BCT1 registers).

(23) CKE (output)

This pin outputs a clock enable signal for SDRAM.
It outputs an inactive level (low level) in the self-refresh cycle or during flyby transfer from SDRAM to external I/O (TF state).
★ This pin always outputs a high level if SDRAM is not set as a memory connected (by the BCT0 and BCT1 registers).

(24) DQM3 to DQM0 (output)

These pins output data mask signals for SDRAM.

They output the same value as the VMBENZ3 to VMBENZ0 signals of the CPU core while a write command is being executed. All these pins output a low level while a read command is being executed.

★ This pin always outputs a high level if SDRAM is not set as a memory connected (by the BCT0 and BCT1 registers).

(25) WRSTZ (output)

This pin outputs the read/write status signal of a memory access cycle.

It outputs a low level in the write cycle.

★ **(26) ME7 to ME0 (output)**

These pins output the value of the MEn bits of the BCT0 and BCT1 registers (n = 7 to 0).

Depending on the value of the MEn bits, the operation of the NA85E535 in each CSn area can be enabled or disabled.

2.2.4 DMA pins

(1) DMTCO3 to DMTCO0 (input)

These pins input a terminal count from the internal DMAC (of the CPU core).

(2) DMTCOM3 to DMTCOM0 (output)

These pins output the terminal count of the internal DMAC cycle.

★ If the DMA transfer cycle issued by the on-chip DMAC is transfer involving the terminal counter (DMTCOn), these pins output a high level during the first 1BUSCLK period when the NA85E535 executes that transfer as an actual memory cycle.

If terminal count is generated in DMA transfer cycle accessing the NPB area or RAM area directly connected to the CPU core, however, terminal count (DMTCOn) from the DMA controller synchronized with VBCLK is resynchronized with BUSCLK, and these pins are asserted for 1 BUSCLK period.

(3) DMACTV3 to DMACTV0 (input)

These pins input an acknowledge signal (DMAACK) from the internal DMAC.

(4) DMACTVM3 to DMACTVM0 (output)

These pins output an acknowledge signal (DMAACK) of the internal DMAC cycle.

★ These pins become active (high-level output) during DMA flyby transfer.

(5) DMXTCO13 to DMXTCO10 and DMXTCO03 to DMXTCO00 (input)

These pins input a terminal count from the NA85E300 (external DMAC connected to the CPU core).

(6) DMXTCM13 to DMXTCM10 and DMXTCM03 to DMXTCM00 (output)

These pins output the terminal count of the NA85E300 cycle.

★ If the DMA transfer cycle issued by the NA85E300 is for transfer involving the terminal count (DMXTCO1n, DMXTCO0n), these pins output a high level during the first 1BUSCLK period in which the NA85E535 executes the transfer as the first memory cycle (n = 3 to 0).

If terminal count occurs in the DMA transfer cycle accessing the NPB area or RAM area directly connected to the CPU core, these pins becomes active during 1BUSCLK period immediately after the terminal count has been acknowledged, regardless of the memory cycle.

(7) DMXCSZ13 to DMXCSZ10 and DMXCSZ03 to DMXCSZ00 (input)

These pins input a chip select signal from the NA85E300.

(8) DMXCZM13 to DMXCZM10 and DMXCZM03 to DMXCZM00 (output)

These pins output the chip select signal of the NA85E300 cycle.

★ These pins becomes active (low-level output) during DMA flyby transfer.

2.2.5 Separate unit test mode pins

(1) TBI9 to TBI4 (input)
These pins input shift data for the separate unit test.

(2) TBI3 (input)
This pin inputs a reset signal for the separate unit test.

(3) TBI2 (input)
This pin inputs a clock for the separate unit test.

(4) TBI1 (input)
This pin inputs a chip select signal for the separate unit test.

(5) TBI0 (input)
This pin inputs an enable signal for the separate unit test.

(6) TBO15 to TBO0 (output)
These pins output shift data for the separate unit test.

(7) BUNRI (input)
This pin inputs the BUNRI signal for the separate unit test.

(8) TEST (input)
This pin inputs the TEST signal for the separate unit test.

2.2.6 Pins reserved by NEC

★ **(1) MPXEN, PHTEST, PHTDIN1, PHTDIN0, and VPTCLK (input)**
This pin is reserved by NEC. Always input a low level to this pin.

★ **(2) VBRESZ and MWAITZ (input)**
This pin is reserved by NEC. Always input a high level to this pin.

★ **(3) ASTBZ, DSTBZ, MPXCZ, PHTDO1, and PHTDO0 (output)**
These pins are reserved by NEC. Leave these pins open.

2.3 Connection of Unused Pins

	Pin Name		I/O	Recommended Connection
★	CPU core connection pins	VDCSZ7 to VDCSZ0, VSA25 to VSA0, VSBENZ3 to VSBENZ0, VSCTYP2 to VSCTYP0, VBDO31 to VBDO0, VPRESZ, VSSEQ2 to VSSEQ0, VSWRITE, VSSTZ, VAACK, VPSTB, VPUBENZ, VPA13 to VPA0, VPWRITE, VPDW15 to VPDW0, VBCLK	Input	– (Be sure to use these pins.)
★		VBDI31 to VBDI0, VAEXREQ, VACBRRQ, VSWAIT, VSAHLD, VSLAST, VPRETR, VPDR15 to VPDR0	Output	
★		VPDV, VMLOCK, STPAK	Output	Leave these pins open.
★		VBCLK2, STPRQ	Input	Input a high level to this pin.
	Initialization pins	MCE	Input	Input a high level to this pin.
		CKMD1, CKMD0, V2EN	Input	Input a low level to these pins.
		LBS1, LBS0	Input	Input a signal to these pins in accordance with the external bus setting.
★ ★	External memory connection pins	A25 to A0, DO31 to DO0, RDZR, RDZF, WRZ3 to WRZ0, WRSTBZ, IORDZR, IORDZF, IOWRZ, HLDAKZ, DC3R to DC0R, DC3F to DC0F, CSZ7 to CSZ0, BENZ3 to BENZ0, BCYSTZ, REFRQZ, BUSCLK, BUSCLK2, SDRASZ, SDCASZ, SDWEZ, CKE, DQM3 to DQM0, WRSTZ, ME7 to ME0	Output	Leave these pins open.
		DI31 to DI0, SELFREF	Input	Input a low level to these pins.
		WAITZ, HLDRQZ	Input	Input a high level to these pins.
	DMA pins	DMTCO3 to DMTCO0, DMACTV3 to DMACTV0, DMXTCO13 to DMXTCO10, DMXTCO03 to DMXTCO00	Input	Input a low level to these pins.
		DMXCSZ13 to DMXCSZ10, DMXCSZ03 to DMXCSZ00	Input	Input a high level to these pins.
		DMTCOM3 to DMTCOM0, DMACTVM3 to DMACTVM0, DMXTCM13 to DMXTCM10, DMXTCM03 to DMXTCM00, DMXCZM13 to DMXCZM10, DMXCZM03 to DMXCZM00	Output	Leave these pins open.
	Separate unit test mode pins	TBI19 to TBI2	Input	Input a low or high level to these pins.
		TBI1, TBI0	Input	Input a high level to these pins.
		TBO15 to TBO0	Output	Leave these pins open.
		BUNRI, TEST	Input	Input a low level to these pins.
★	Pins reserved by NEC	MPXEN, PHTEST, PHTDIN1, PHTDIN0, VPTCLK	Input	Input a low level to this pin.
★		VBRESZ, MWAITZ	Input	Input a high level to this pin.
★		ASTBZ, DSTBZ, MPXCZ, PHTDO1, PHTDO0	Output	Leave these pins open.

2.4 Pin Status

The following table shows the status of pins with an output function in each operation mode.

Table 2-8. Pin Status in Each Operation Mode (1/2)

	Pin Name		Pin Status					
			Normal Mode				Test Mode	
★			Reset	STOP Mode	HALT Mode	Bus Hold	Standby Test Mode[Note 1]	Unit Test Mode[Note 1]
	CPU core connection pins	VBDI31 to VBDI0	0	0	Operates[Note 2]	0	Undefined	Operates
		VAEXREQ	0	1	Operates[Note 2]	1	Undefined	Operates
		VACBRRQ	0	0	Operates	0	Undefined	Operates
		VMLOCK	0	1	Operates	1	Undefined	Operates
		VSWAIT	0	0	Operates[Note 2]	0	Undefined	Operates
		VSAHLD	0	0	Operates[Note 2]	0	Undefined	Operates
		VSLAST	0	0	Operates[Note 2]	0	Undefined	Operates
		VPRETR	0	0	0	0	Undefined	Operates
		VPDR15 to VPDR0	0	0	Operates[Note 2]	0	Undefined	Operates
		VPDV	0	0	Operates[Note 2]	0	Undefined	Operates
		STPAK	0	1	Operates	0	Undefined	Operates
★	External memory connection pins	A25 to A0	0	0	Operates	0	Undefined	Operates
		DO31 to DO0	0	Held	Operates	Held	Undefined	Operates
		RDZR	1	1	Operates	1	Undefined	Operates
		RDZF	1	1	Operates	1	Undefined	Operates
		WRZ3 to WRZ0	1	1	Operates	1	Undefined	Operates
		WRSTBZ	1	1	Operates	1	Undefined	Operates
		IORDZR	1	1	Operates	1	Undefined	Operates
		IORDZF	1	1	Operates	1	Undefined	Operates
		IOWRZ	1	1	Operates	1	Undefined	Operates
		HLDAKZ	1	1	Operates	0	Undefined	Operates
		DC3R to DC0R	1	1	Operates	1	Undefined	Operates
★		DC3F to DC0F	1	0	Operates	0	Undefined	Operates
		CSZ7 to CSZ0	1	1	Operates	1	Undefined	Operates
		BENZ3 to BENZ0	1	1	Operates	1	Undefined	Operates
		BCYSTZ	1	1	Operates	1	Undefined	Operates
		REFRQZ	1	0	Operates	Operates	Undefined	Operates
★		BUSCLK	**Note 3**	0	Operates	Operates	Undefined	Operates
★		BUSCLK2	**Note 4**	0	Operates	Operates	Undefined	Operates
		SDRASZ	1	1	Operates	1	Undefined	Operates
		SDCASZ	1	1	Operates	1	Undefined	Operates
		SDWEZ	1	1	Operates	1	Undefined	Operates

Table 2-8. Pin Status in Each Operation Mode (2/2)

★ ★

Pin Name			Pin Status					
			Normal Mode				Test Mode	
			Reset	STOP Mode	HALT Mode	Bus Hold	Standby Test Mode Note 1	Unit Test Mode Note 1
External memory connection pins	CKE		1	0	Operates	1	Undefined	Operates
	DQM3 to DQM0		1	1	Operates	1	Undefined	Operates
	WRSTZ		0	0	Operates	0	Undefined	Operates
	ME7 to ME0		**Note 5**	Held	Operates	Held	Undefined	Operates
DMA pins	DMTCOM3 to DMTCOM0		0	0	Operates	0	Undefined	Operates
	DMACTVM3 to DMACTVM0		0	0	Operates	0	Undefined	Operates
	DMXTCM13 to DMXTCM10, DMXTCM03 to DMXTCM00		0	0	Operates	0	Undefined	Operates
	DMXCZM13 to DMXCZM10, DMXCZM03 to DMXCZM00		1	1	Operates	1	Undefined	Operates
Separate unit test mode pins	TBO15 to TBO0	CB-10VX	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Operates
		CB-12M	0	0	0	0	0	Operates

Notes 1. The standby test mode or unit test mode can be selected by the input levels of the BUNRI and TEST pins.

Test Mode	BUNRI Pin Input Level	TEST Pin Input Level
Standby test mode	High level	Low level
Unit test mode	High level	High level

2. If a refresh occurs in the HALT mode and the NA85E535 is the bus master, the same value as in the STOP mode is output.

3. If a low level (divided by one setting) is input to the CKMD1 and CKMD0 pins, the level input to the VBCLK pin is output. In other cases, the operation is undefined until a VBCLK signal of 1 clock or longer is input during the reset period (in which a low level is input to the VPRESZ pin). A low level is output when a VBCLK signal of 1 clock or longer is input.

4. If a low level (divided by one setting) is input to the CKMD1 and CKMD0 pins, the level input to the VBCLK2 pin is output. In other cases, the operation is undefined until a VBCLK2 signal of 1 clock or longer is input during the reset period (in which a low level is input to the VPRESZ pin). A low level is output when a VBCLK2 signal of 1 clock or longer is input.

5. When a low level is input to the MCE pin: 0
When a high level is input to the MCE pin: 1

Remark 0: Low-level output, 1: High-level output, Hi-Z: High impedance, Operates: Outputs valid signal

3.1 Control Registers

The bus cycle function of the NA85E535 is specified by the operation mode setting pins and the control registers listed below.

Each control register is allocated to the peripheral I/O area of the CPU core.

Remark The setting of the control registers is invalid for ROM connected to VFB (V850E fetch bus) of the CPU core or RAM connected to VDB (V850E data bus).

Table 3-1. Control Register List (1/2)

Address	Register Name	Symbol	R/W	Bit Unit for Manipulation			Default Value
				1 Bit	8 Bits	16 Bits	
FFFFF480H	Bus cycle type configuration register 0	BCT0	R/W	–	–	√	8888H/ 0000H
FFFFF482H	Bus cycle type configuration register 1	BCT1	R/W	–	–	√	8888H/ 0000H
FFFFF484H	Data wait control register 0	DWC0	R/W	–	–	√	7777H
FFFFF486H	Data wait control register 1	DWC1	R/W	–	–	√	7777H
FFFFF488H	Bus cycle control register	BCC	R/W	–	–	√	FFFFH
FFFFF48AH	Address setting wait control register	ASC	R/W	–	–	√	FFFFH
★ FFFFF48CH	Flyby transfer strobe control register	BCP	R/W	–	√	–	00H
FFFFF48EH	Local bus sizing control register	LBS	R/W	–	–	√	0000H/ 5555H/ AAAAH
FFFFF490H	Line buffer control register 0	LBC0	R/W	–	–	√	0000H
FFFFF492H	Line buffer control register 1	LBC1	R/W	–	–	√	0000H
FFFFF494H	DMA flyby transfer wait control register	FWC	R/W	–	–	√	7777H
FFFFF496H	DMA flyby transfer idle control register	FIC	R/W	–	–	√	3333H
FFFFF498H	Bus mode control register	BMC	R/W	–	√	–	00H/01H/ 02H/03H/ 80H/81H/ 82H/83H
FFFFF49AH	Page ROM configuration register	PRC	R/W	–	–	√	7000H
FFFFF4A4H	SDRAM configuration register 1	SCR1	R/W	–	–	√	30C0H
FFFFF4A6H	SDRAM refresh control register 1	RFS1	R/W	–	–	√	0000H
FFFFF4ACH	SDRAM configuration register 3	SCR3	R/W	–	–	√	30C0H
FFFFF4AEH	SDRAM refresh control register 3	RFS3	R/W	–	–	√	0000H
FFFFF4B0H	SDRAM configuration register 4	SCR4	R/W	–	–	√	30C0H
FFFFF4B2H	SDRAM refresh control register 4	RFS4	R/W	–	–	√	0000H
FFFFF4B8H	SDRAM configuration register 6	SCR6	R/W	–	–	√	30C0H

Table 3-1. Control Register List (2/2)

	Address	Register Name	Symbol	R/W	Bit Unit for Manipulation			Default Value
					1 Bit	8 Bits	16 Bits	
	FFFFF4BAH	SDRAM refresh control register 6	RFS6	R/W	–	–	√	0000H
★	FFFFF4C4H	Setting register for MobileRAM expansion mode register 1	ESC1	R/W	–	–	√	0000H
★	FFFFF4CCH	Setting register for MobileRAM expansion mode register 3	ESC3	R/W	–	–	√	0000H
★	FFFFF4D0H	Setting register for MobileRAM expansion mode register 4	ESC4	R/W	–	–	√	0000H
★	FFFFF4D8H	Setting register for MobileRAM expansion mode register 6	ESC6	R/W	–	–	√	0000H

3.1.1 Bus cycle type configuration registers 0 and 1 (BCT0 and BCT1)

The BCT0 and BCT1 registers enable operation of the NA85E535 in each CSn area and specify the type of memory to be connected (n = 7 to 0).

These registers can be read or written in 16-bit units.

Figure 3-1. Bus Cycle Type Configuration Registers 0 and 1 (BCT0 and BCT1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Default value
BCT0	ME3	0	BT31	BT30	ME2	0	BT21	BT20	ME1	0	BT11	BT10	ME0	0	BT01	BT00	FFFFF480H	**Note**
BCT1	ME7	0	BT71	BT70	ME6	0	BT61	BT60	ME5	0	BT51	BT50	ME4	0	BT41	BT40	FFFFF482H	**Note**

Bit position	Bit name	Meaning
15, 11, 7, 3	MEn	Enables or disables operation of NA85E535 in each CSn area. 0: Disabled (no response to CPU core) 1: Enabled
13, 12, 9, 8, 5, 4, 1, 0	BTn1, BTn0	Sets the type of memory to be connected for each CSn area

BTn1	BTn0	Connected memory
0	0	SRAM (or external I/O)
0	1	Page ROM
1	0	Setting prohibited
1	1	When n = 6, 4, 3, or 1: SDRAM When n = 7, 5, 2, or 0: Setting prohibited

Note The default value differs as follows depending on the input level of the MCE pin at reset.

MCE pin input level	MPXEN pin input level	Default value
High level	Low level	8888H
Low level	Low level	0000H

Cautions 1. Be sure to input a low level to the MPXEN pin.

2. Be sure to clear bits 14, 10, 6, and 2 to 0 (otherwise, the operation is not guaranteed).

3. Set the BCT0 and BCT1 registers immediately after reset. Do not change the set values of these registers (however, the MEn bit may be changed).

Remark n = 7 to 0

3.1.2 Address setting wait control register (ASC)

The ASC register specifies the number of address setting wait states to be inserted at the beginning of the SRAM read/write cycle or page ROM read cycle, for each CSn area (n = 7 to 0).

This register can be read or written in 16-bit units.

Remarks 1. The setting of this register is invalid when SDRAM is accessed.

2. The external wait function by the WAITZ pin is invalid during the address setting wait period.

Figure 3-2. Address Setting Wait Control Register (ASC)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Default value
ASC	AC71	AC70	AC61	AC60	AC51	AC50	AC41	AC40	AC31	AC30	AC21	AC20	AC11	AC10	AC01	AC00	FFFFF48AH	FFFFH

Bit position	Bit name	Meaning
15 to 0	ACn1, ACn0	Sets the number of address setting wait states for each CSn area.

ACn1	ACn0	Number of address setting wait states
0	0	0
0	1	1
1	0	2
1	1	3 (default value)

Remark n = 7 to 0

3.1.3 Bus cycle control register (BCC)

The BCC register specifies the number of idle states to be inserted at the end of the SRAM read/write cycle, page ROM read cycle, or SDRAM read cycle, for each CSn area (n = 7 to 0).

This register is used to make sure that the time required for the memory to release the external data bus elapses. The next bus cycle starts in the state following the idle states.

The chip select signal (CSZn) is not asserted in the idle states.

This register can be read or written in 16-bit units.

Figure 3-3. Bus Cycle Control Register (BCC)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Default value
BCC	BC71	BC70	BC61	BC60	BC51	BC50	BC41	BC40	BC31	BC30	BC21	BC20	BC11	BC10	BC01	BC00	FFFFF488H	FFFFH

Bit position	Bit name	Meaning
15 to 0	BCn1, BCn0	Sets the number of idle states for each CSn area.

BCn1	BCn0	Number of idle states
0	0	0
0	1	1
1	0	2
1	1	3 (default value)

Remark n = 7 to 0

★ ### 3.1.4 Flyby transfer strobe control register (BCP)

The BCP register is used to specify the operations of the IORDZR, IORDZF, and IOWRZ signals during the read/write cycle when DMA flyby transfer is not executed.

When the IOEN bit of this register is cleared to 0, the IORDZR, IORDZF, and IOWRZ signals do not operate during the read/write cycle when DMA flyby transfer is not executed.

When the IOEN bit is set to 1, the IORDZR, IORDZF, and IOWRZ signals perform the same operations as the RDZR, RDZF, and WRSTB signals, respectively, during the read/write cycle when DMA flyby transfer is not executed.

These signals operate, regardless of the value of the IOEN bit, when DMA flyby transfer is executed (the operation is the same).

This register can be read or written in 8-bit units.

Figure 3-4. Flyby Transfer Strobe Control Register (BCP)

	7	6	5	4	3	2	1	0	Address	Default value
BCP	0	0	0	0	IOEN	0	0	0	FFFFF48CH	00H

Bit position	Bit name	Meaning
3	IOEN	Specifies operations of the IORDZR, IORDZF, and IOWRZ signals during the read/write cycle when DMA flyby transfer is not executed. 0: Does not operate. 1: Operates.

Remark Bits 7 to 4 and 2 to 0 are fixed to 0 (setting these bits to 1 is ignored).

3.1.5 Data wait control registers 0 and 1 (DWC0 and DWC1)

The DWC0 and DWC1 registers specify the number of data wait cycle states to be inserted in the SRAM read/write cycle or page ROM read cycle (off-page) for each CSn area (n = 7 to 0).

These registers can be read or written in 16-bit units.

Caution The number of wait states for the on-page cycle of page ROM is set by the Page ROM configuration register (PRC).

Figure 3-5. Data Wait Control Registers 0 and 1 (DWC0 and DWC1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Default value
DWC0	0	DW32	DW31	DW30	0	DW22	DW21	DW20	0	DW12	DW11	DW10	0	DW02	DW01	DW00	FFFFF484H	7777H
DWC1	0	DW72	DW71	DW70	0	DW62	DW61	DW60	0	DW52	DW51	DW50	0	DW42	DW41	DW40	FFFFF486H	7777H

Bit position	Bit name	Meaning
14 to 12, 10 to 8, 6 to 4, 2 to 0	DWn2 to DWn0	Sets the number of wait states for each CSn area.

DWn2	DWn1	DWn0	Number of wait states
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7 (default value)

Remarks 1. n = 7 to 0

2. Bits 15, 11, 7, and 3 are fixed to 0 (setting these bits to 1 is ignored).

(1) External wait function

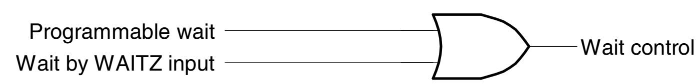
When the NA85E535 is connected to a low-speed macro or an asynchronous system, wait states (external wait states) can be inserted in the bus cycle by using the external wait pin (WAITZ).

The external wait states are inserted only in the data wait cycle.

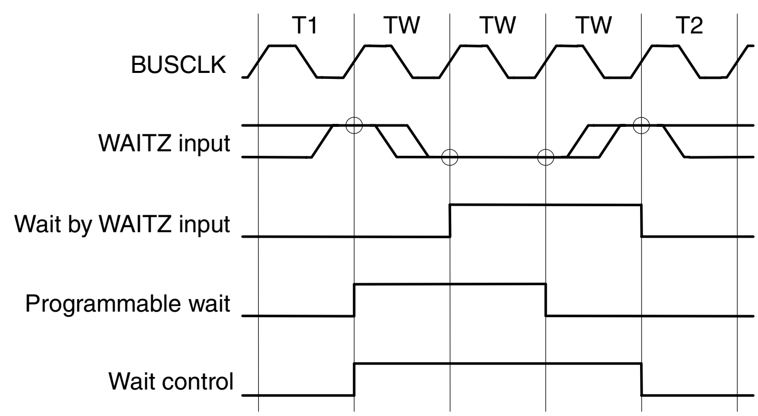
The external wait pin (WAITZ) is sampled at the rising edge of the BUSCLK signal.

(2) Data wait control registers and external wait

The number of wait states set by data wait control registers 0 and 1 (DWC0 and DWC1) is ORed with the number of external wait states set by WAITZ input, and the resultant number of wait states is inserted. This means that the greater of the two values is inserted.



For example, three wait states are inserted in the bus cycle if the programmable wait and input to WAITZ pin occur at the following timing.



3.1.6 Page ROM configuration register (PRC)

If a page ROM sequential bus cycle is generated, the NA85E535 compares the current address with the address immediately after the generated page ROM cycle to identify whether the access is on-page access.

The PRC register sets a width for address comparison and the number of wait states to be inserted in the on-page cycle.

This register can be read or written in 16-bit units.

Caution The number of wait states to be inserted in the off-page cycle is set by the data wait control registers 0 and 1 (DWC0 and DWC1).

Figure 3-6. Page ROM Configuration Register (PRC)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Default value
PRC	0	PRW2	PRW1	PRW0	0	0	0	0	0	0	0	0	MA6	MA5	MA4	MA3	FFFFF49AH	7000H

Bit position	Bit name	Meaning
14 to 12	PRW2 to PRW0	Sets the number of data wait states for on-page cycle of page ROM.

PRW2	PRW1	PRW0	Number of data wait states
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7 (default value)

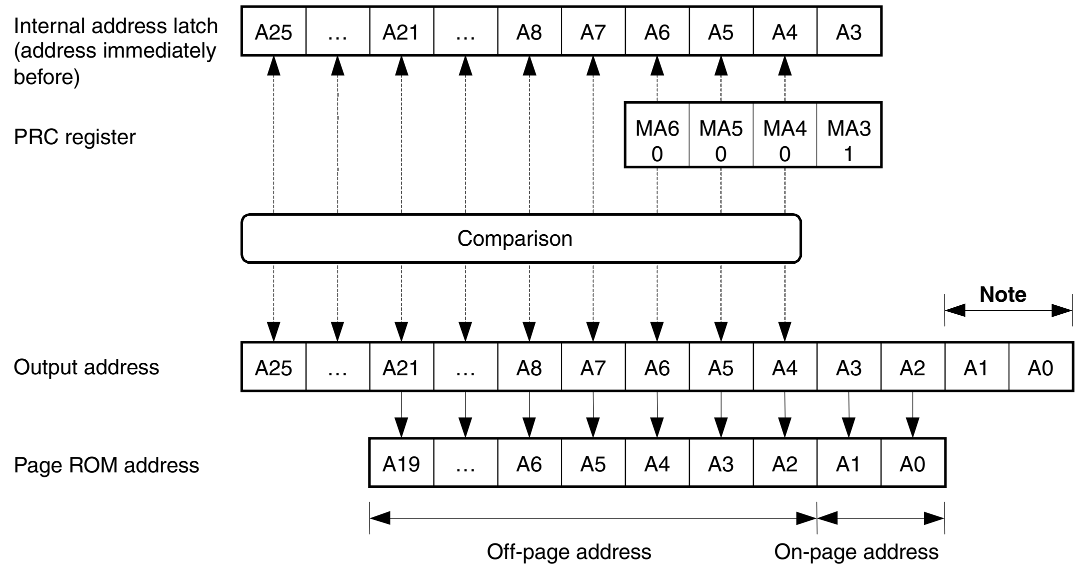
Bit position	Bit name	Meaning
3 to 0	MA6 to MA3	Sets mask bits for address comparison.

MA6	MA5	MA4	MA3	Number of bits successively read
0	0	0	0	32 bits × 2, 16 bits × 4, 8 bits × 8 (default value)
0	0	0	1	32 bits × 4, 16 bits × 8, 8 bits × 16
0	0	1	1	32 bits × 8, 16 bits × 16, 8 bits × 32
0	1	1	1	32 bits × 16, 16 bits × 32, 8 bits × 64
1	1	1	1	32 bits × 32, 16 bits × 64, 8 bits × 128
Other than above				Setting prohibited (Operation is not guaranteed if this setting is made.)

Remark Bits 15 and 11 to 4 are fixed to 0 (setting these bits is ignored).

An example of address mask control if four page ROMs of 1 Mwords × 8 bits are connected is illustrated below.

Figure 3-7. Example of Control by MA6 to MA3 Bits



Note These bits are not used if the data bus width is 32 bits.

3.1.7 SDRAM configuration register n (SCRn)

The SCRn register sets the number of wait states for accessing SDRAM and an address multiplex width for each CSn area (n = 6, 4, 3, or 1). If data is written to this register, the NA85E535 starts a register write operation. This register can be read or written in 16-bit units.

Cautions 1. The SDRAM read/write cycle is not generated before execution of the register write operation. Read the value of the SCRn register to check if the WCF bit is set to 1, before accessing SDRAM.

2. Before writing data to the SCRn register again after accessing SDRAM, be sure to clear the ME bit of the BCT0 and BCT1 registers to 0 and then re-set to 1.

3. Do not consecutively execute instructions that write data to the SCRn registers. Be sure to insert another instruction between the instructions that write data to the SCRn register.

4. Before accessing SDRAM, make sure that all settings of the SCRn register are complete.

Remarks 1. n of the register name corresponds to a CSn area number (n = 6, 4, 3, or 1).

2. Be sure to clear bit 15 to 0. Otherwise, the operation is not guaranteed.

3. Bits 11 to 9 are fixed to 0 (setting these bits is ignored).

Figure 3-8. SDRAM Configuration Register n (SCRn) (1/3)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Default value
SCRn	0	LTM2	LTM1	LTM0	0	0	0	WCF	BCW1	BCW0	SSO1	SSO0	RAW1	RAW0	SAW1	SAW0	FFFFF4A0H +4n	30C0H

Bit position	Bit name	Meaning
14 to 12	LTM2 to LTM0	Sets the value of CAS latency during read. LTM2 / LTM1 / LTM0 : CAS latency 0 / 0 / 0 : Setting prohibited 0 / 0 / 1 : 1 (setting prohibited during DMA flyby transfer) 0 / 1 / 0 : 2 0 / 1 / 1 : 3 (default value) 1 / Any / Any : Setting prohibited
8	WCF	Indicates that a register write command was completely executed to SDRAM after the SCRn register was set. If the register write command is generated, this bit is set to 1. This bit can only be read. 0: Setting not completed (default value) 1: Setting completed

LTM2	LTM1	LTM0	CAS latency
0	0	0	Setting prohibited
0	0	1	1 (setting prohibited during DMA flyby transfer)
0	1	0	2
0	1	1	3 (default value)
1	Any	Any	Setting prohibited

Remark n = 6, 4, 3, or 1

Figure 3-8. SDRAM Configuration Register n (SCRn) (2/3)

<table>
<tr><th>Bit position</th><th>Bit name</th><th>Meaning</th></tr>
<tr><td>7, 6</td><td>BCW1,
BCW0</td><td>Sets the number of wait states from a bank active command to a read/write command, or from a precharge command to a bank active command.
<table>
<tr><th>BCW1</th><th>BCW0</th><th>Number of wait states</th></tr>
<tr><td>0</td><td>0</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>2</td></tr>
<tr><td>1</td><td>1</td><td>3 (default value)</td></tr>
</table></td></tr>
<tr><td>5, 4</td><td>SSO1,
SSO0</td><td>Sets the shift width of an address for identifying on-page access.
If the data bus width is set to 16 or 32 bits, the system does not use the lower address (A0 or A1, A0). Set these bits in accordance with the contents of the LBS register corresponding to the chip select area.
<table>
<tr><th>SSO1</th><th>SSO0</th><th>Address shift width</th></tr>
<tr><td>0</td><td>0</td><td>0 bit (data bus width: 8 bits) (default value)</td></tr>
<tr><td>0</td><td>1</td><td>1 bit (data bus width: 16 bits)[Note]</td></tr>
<tr><td>1</td><td>0</td><td>2 bits (data bus width: 32 bits)[Note]</td></tr>
<tr><td>1</td><td>1</td><td>Setting prohibited</td></tr>
</table></td></tr>
<tr><td>3, 2</td><td>RAW1,
RAW0</td><td>Sets a row address width.
<table>
<tr><th>RAW1</th><th>RAW0</th><th>Row address width</th></tr>
<tr><td>0</td><td>0</td><td>11 bits (default value)</td></tr>
<tr><td>0</td><td>1</td><td>12 bits[Note]</td></tr>
<tr><td>1</td><td>0</td><td>13 bits[Note]</td></tr>
<tr><td>1</td><td>1</td><td>Setting prohibited</td></tr>
</table></td></tr>
<tr><td>1, 0</td><td>SAW1,
SAW0</td><td>Sets an address multiplex width (column address width) for accessing SDRAM.
<table>
<tr><th>SAW1</th><th>SAW0</th><th>Address multiplex width (column address width)</th></tr>
<tr><td>0</td><td>0</td><td>8 bits (default value)</td></tr>
<tr><td>0</td><td>1</td><td>9 bits</td></tr>
<tr><td>1</td><td>0</td><td>10 bits[Note]</td></tr>
<tr><td>1</td><td>1</td><td>11 bits[Note]</td></tr>
</table></td></tr>
</table>

Note Refer to the next page for explanation.

Figure 3-8. SDRAM Configuration Register n (SCRn) (3/3)

Note The following setting is prohibited because the upper limit of the address is exceeded.

SSO1	SSO0	RAW1	RAW0	SAW1	SAW0	Setting
0	1	1	0	1	1	Data bus width: 16 bits Row address width: 13 bits Column address width: 11 bits
1	0	0	1	1	1	Data bus width: 32 bits Row address width: 12 bits Column address width: 11 bits
1	0	1	0	1	0	Data bus width: 32 bits Row address width: 13 bits Column address width: 10 bits
					1	Data bus width: 32 bits Row address width: 13 bits Column address width: 11 bits

Table 3-2. Row Address Output

Bit Setting		Address Pin																		
SAW1	SAW0	A25 to A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	a25 to a18	a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a13	a12	a11	a10	a9	a8
0	1	a25 to a18	a17	a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a13	a12	a11	a10	a9
1	0	a25 to a18	a17	a16	a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a13	a12	a11	a10
1	1	a25 to a18	a17	a16	a15	a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a13	a12	a11

Table 3-3. Column Address Output

(a) For all bank precharge commands

Bit Setting		Address Pin																		
SSO1	SSO0	A25 to A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	a25 to a18	a17	a16	a15	a14	a13	a12	a11	1	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0
0	1	a25 to a18	a17	a16	a15	a14	a13	a12	1	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0
1	0	a25 to a18	a17	a16	a15	a14	a13	1	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0

(b) For register write command

Bit Setting		Address Pin																		
SSO1	SSO0	A25 to A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	LTM2	LTM1	LTM0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	LTM2	LTM1	LTM0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	LTM2	LTM1	LTM0	0	0	0	0	0	0

(c) For read/write command

Bit Setting		Address Pin																		
SSO1	SSO0	A25 to A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	a25 to a18	a17	a16	a15	a14	a12	a11	a10	0	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0
0	1	a25 to a18	a17	a16	a15	a14	a12	a11	0	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0
1	0	a25 to a18	a17	a16	a15	a14	a12	0	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0

3.1.8 SDRAM refresh control register n (RFSn)

The NA85E535 can generate the SDRAM CBR refresh and self-refresh cycles.

The RFSn register enables refresh and sets the refresh interval for each CSn area (n = 6, 4, 3, or 1).

This register can be read or written in 16-bit units.

Remark n of the register name corresponds to a CSn area number (n = 6, 4, 3, or 1).

Figure 3-9. SDRAM Refresh Control Register n (RFSn) (1/2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Default value
RFSn	REN	0	0	0	0	0	RCC1	RCC0	0	0	RIN5	RIN4	RIN3	RIN2	RIN1	RIN0	FFFFF4A2H +4n	0000H

<table>
<tr><th>Bit position</th><th>Bit name</th><th>Meaning</th></tr>
<tr><td>15</td><td>REN</td><td>Enables refresh.
<table><tr><th>REN</th><th>Refresh setting</th></tr><tr><td>0</td><td>Disables refresh (default value).</td></tr><tr><td>1</td><td>Enables refresh.</td></tr></table></td></tr>
<tr><td>9, 8</td><td>RCC1, RCC0</td><td>Sets a source clock factor for the refresh interval counter.
<table><tr><th>RCC1</th><th>RCC0</th><th>Count source clock factor (Cfac)</th></tr><tr><td>0</td><td>0</td><td>32 (default value)</td></tr><tr><td>0</td><td>1</td><td>128</td></tr><tr><td>1</td><td>0</td><td>256</td></tr><tr><td>1</td><td>1</td><td>Setting prohibited</td></tr></table>Remark Refresh count clock (Trcy) = Cfac/ϕ
ϕ: Operating clock (BUSCLK)</td></tr>
</table>

Remarks 1. n = 6, 4, 3, or 1

2. Bits 14 to 10, 7, and 6 are fixed to 0 (setting these bits is ignored).

Figure 3-9. SDRAM Refresh Control Register n (RFSn) (2/2)

Bit position	Bit name	Meaning
5 to 0	RIN5 to RIN0	Sets a refresh interval factor.

RIN5	RIN4	RIN3	RIN2	RIN1	RIN0	Interval factor (Ifac)
0	0	0	0	0	0	1 (default value)
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
:	:	:	:	:	:	:
1	1	1	1	1	1	64

Caution To change the setting of the RFSn register, follow these steps (n = 6, 4, 3, or 1).

<1> Clear the MEn bit of the BCT register to 0.
<2> Clear the REN bit to 0.
<3> Set the MEn bit of the BCT register to 1.
<4> Set a new value to the RCC1, RCC0, and RIN5 to RIN0 bits, and set the REN bit to 1.

To change the refresh interval, set a value that allows refresh to be performed in time even when the interval is changed.

Table 3-4. Example of SDRAM Refresh Interval

Default Refresh Interval (μs)	Refresh Count Clock (Trcy)	Interval Factor (Ifac)Note			
		ϕ = 20 MHz	ϕ = 33 MHz	ϕ = 50 MHz	ϕ = 66 MHz
15.6	32/ϕ	9 (14.4)	16 (15.5)	24 (15.4)	32 (15.5)
	128/ϕ	2 (12.8)	4 (15.5)	6 (15.4)	8 (15.5)
	256/ϕ	1 (12.8)	2 (15.5)	3 (15.4)	4 (15.5)

Note ( ): Calculated refresh interval (μs)
Refresh interval (μs) = Trcy $\times$ Ifac

Remark ϕ: Operating clock (BUSCLK)

★ 3.1.9 Setting register for MobileRAM expansion mode register n (ESCn)

The ESCn register sets the MobileRAM operation for each CSn area (n = 6, 4, 3, or 1).
This register can be read or written in 16-bit units.

Cautions 1. The ESCn register does not have to be set when MobileRAM is not connected.
2. Be sure to set the ESCn register before setting the SCRn register.
3. Be sure to re-set the ESCn and SCRn registers and start a register write operation after the deep power down mode has been released.

Remark n of the register name corresponds to a CSn area number (n = 6, 4, 3, or 1).

Figure 3-10. Setting Register for MobileRAM Expansion Mode Register n (ESCn) (1/2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Default value
ESCn	ERS	DPD	0	EMB 12	EMB 11	EMB 10	EMB 9	EMB 8	EMB 7	EMB 6	EMB 5	EMB 4	EMB 3	EMB 2	EMB 1	EMB 0	FFFFF4C0H +4n	0000H

Bit position	Bit name	Meaning
15	ERS	Specifies a write operation to the expansion mode register of MobileRAM during a register write operation. 0: Does not write to the expansion mode register (default value). 1: Writes to the expansion mode register.
14	DPD	Specifies the operation mode of MobileRAM when the CPU core enters the STOP mode or when a high level is input to the SELFREF pin. 0: Self-refresh cycle mode (default value)[Note] 1: Deep power down mode
12 to 7	EMB12 to EMB7	Specifies the expansion mode register (bits 12 to 7) of MobileRAM (default value: 0). Set these bits in accordance with the specifications of the MobileRAM connected.

Note When the DPD bits of any of the ESCn registers is set to 1, even if the DPD bit of other registers is cleared to 0, the operation is changed to the deep power down mode. To operate MobileRAM in the self-refresh mode, therefore, clear the DPD bit of all the ESCn registers to 0.

Remarks 1. n = 6, 4, 3, or 1
2. Bit 13 is fixed to 0 (setting this bit is ignored).

Figure 3-10. Setting Register for MobileRAM Expansion Mode Register n (ESCn) (2/2)

Bit position	Bit name	Meaning
6, 5	EMB6, EMB5	Sets bits 6 and 5 of the expansion mode register of MobileRAM. Set these bits in accordance with the specifications of MobileRAM connected. Set these bits as follows when MobileRAM of Elpida Memory.

EMB6	EMB5	Drive strength
0	0	Normal (default value)
0	1	1/2 strength
1	0	1/4 strength
1	1	Reserved

Bit position	Bit name	Meaning
4, 3	EMB4, EMB3	Sets bits 4 and 3 of the expansion mode register of MobileRAM. Set these bits in accordance with the specifications of MobileRAM connected. Set these bits as follows when MobileRAM of Elpida Memory.

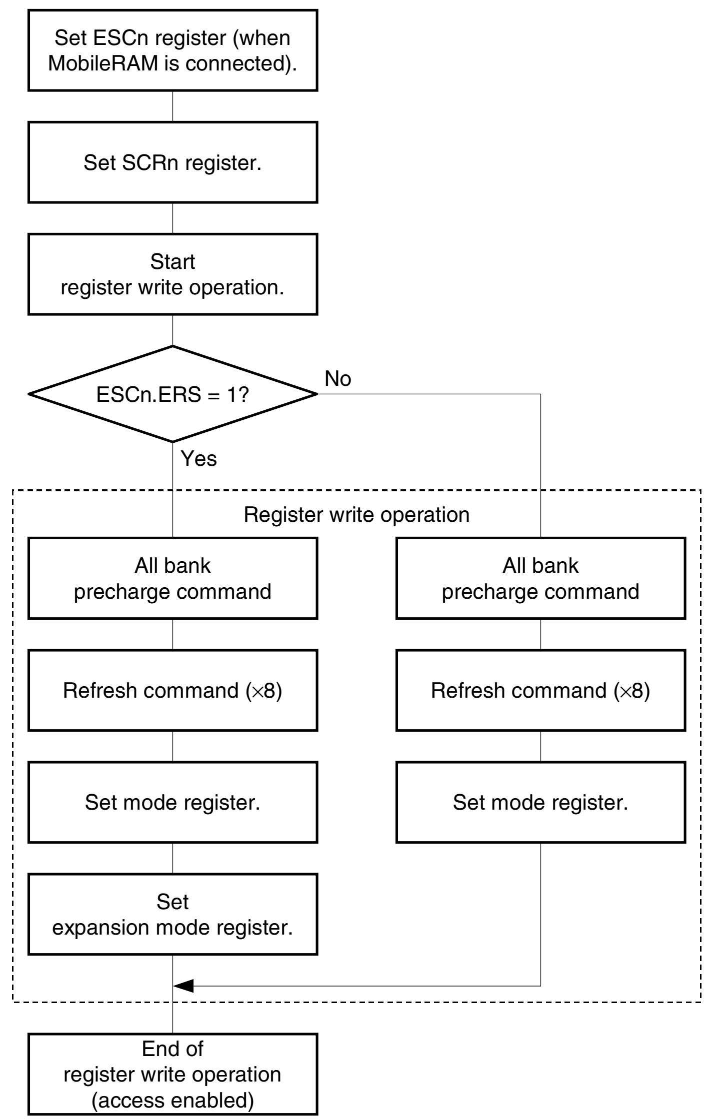
EMB4	EMB3	Self-refresh guarantee temperature
0	0	70°C (default value)
0	1	45°C
1	0	15°C
1	1	85°C

Bit position	Bit name	Meaning
2 to 0	EMB2 to EMB0	Sets bits 2 to 0 of the expansion mode register of MobileRAM. Set these bits in accordance with the specifications of MobileRAM connected. Set these bits as follows when MobileRAM of Elpida Memory.

EMB2	EMB1	EMB0	Self-refresh operation area
0	0	0	All Banks (default value)
0	0	1	Bank A & Bank B
0	1	0	Bank A
0	1	1	Reserved
1	0	0	Reserved
1	0	1	1/2 of Bank A
1	1	0	1/4 of Bank B
1	1	1	Reserved

The following figure shows a flow from setting the ESCn and SCRn registers to completion of a register write operation.

Figure 3-11. Flow from Setting ESCn and SCRn Register to Register Write Operation



Remark n = 6, 4, 3, or 1

3.1.10 Line buffer control registers 0 and 1 (LBC0 and LBC1)

The NA85E535 includes a read buffer.

The LBC0 and LBC1 registers set the operation conditions of the read buffer included in the NA85E535 for each CSn area (n = 7 to 0).

These registers can be read or written in 16-bit units.

Figure 3-12. Line Buffer Control Registers 0 and 1 (LBC0 and LBC1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Default value
LBC0	0	0	RB31	RB30	0	0	RB21	RB20	0	0	RB11	RB10	0	0	RB01	RB00	FFFFF490H	0000H
LBC1	0	0	RB71	RB70	0	0	RB61	RB60	0	0	RB51	RB50	0	0	RB41	RB40	FFFFF492H	0000H

Bit position	Bit name	Meaning
13, 12, 9, 8, 5, 4, 1, 0	RBn1, RBn0	Sets the operating conditions (timing to execute speculative read) of the read buffer for each CSn area.

RBn1	RBn0	Timing of speculative read
0	0	No speculative read (operation of read buffer prohibited) (default value)
0	1	No speculative read (operation of read buffer prohibited)
1	0	In DMA/fetch cycle
1	1	In all cycles

Remarks 1. n = 7 to 0

2. Be sure to clear bits 15, 11, 7, and 3 to 0. Otherwise, the operation is not guaranteed.

3. Bits 14, 10, 6, and 2 are fixed to 0 (setting these bits is ignored).

4. If the setting of the RBn1 and RBn0 bits is changed, the data retained in the read buffer becomes invalid immediately after changing.

The read buffer has a capacity of 4 words (128 bits) and enables execution of speculative read operations. The speculative read range is the addresses (xxxxxx0H to xxxxxxFH) on the same line as the address that has been accessed (critical first access method). For example, addresses “xxxxx00H”, “xxxxx04H”, and “xxxxx01H” are accessed in the following sequence, and data is loaded to the read buffer (when speculative read is executed with the local bus size of 32 bits).

- When accessing address “xxxxx00H”: xxxxx00H → xxxxx04H → xxxxx08H → xxxxx0CH
- When accessing address “xxxxx04H”: xxxxx04H → xxxxx08H → xxxxx0CH → xxxxx00H
- When accessing address “xxxxx01H”: xxxxx01H → xxxxx05H → xxxxx09H → xxxxx0DH

The NA85E535 has an internal buffer of four stages (128 bits) and, if a write request is generated while the buffer is full, outputs a wait response until a vacancy is available in the buffer.

★ **(1) Recommended setting of speculative read function**

The following explanation shows the cases indicating whether or not speculative read should be set for an individual memory type. Note, however, that the following explanation only indicates whether the probability that speculative read improves the performance is high or low, and does not guarantee that the performance is improved. Whether speculative read is actually executed or not must be determined based on the access condition of the system and the set value of each wait cycle.

(a) SRAM

- Case where speculative read should be set
  - 2-cycle transfer by using the DMA controller with on-chip CPU core[Note]
  - DMA 2-cycle transfer when using the NA85E300
- Case where speculative read should not be set
  - Random data access by CPU
  - Fetch access
  - Transfer involving sequential status (cache refill)

Note Especially when performing line transfer and setting wait, setting speculative read is advantageous.

(b) Page ROM/SDRAM

- Case where speculative read should be set
  - 2-cycle transfer by using the DMA controller with on-chip CPU core[Note 1]
  - DMA 2-cycle transfer when using the NA85E300
  - Fetch access[Note 2]
    (When setting address setup wait/idle wait)
- Case where speculative read should not be set
  - Random data access by CPU
  - Transfer involving sequential status[Note 3] (cache refill)

Notes 1. Especially when performing line transfer and setting wait, setting speculative read is advantageous.

2. Depending on the branch rate of the program to be fetched, speculative read should not be set.

3. If a sequential access occurs from VSB, there is no problem if speculative read is set because the NA85E535 gives priority to the request from VSB.

★ **3.1.11 Bus mode control register (BMC)**

The BMC register is used to select the VSB specifications and set the rate by which the VBCLK/VBCLK2 signal is to be divided. The divided VBCLK/VBCLK2 signal is output from the BUSCLK/BUSCLK2 pin as the bus clock. The divided BUSCLK signal is also used as an internal system clock.

When the BMC register is written, an NPB write retry cycle is always generated, and the BUSCLK/BUSCLK2 signal stops once for the duration of 12 clocks of the VBCLK/VBCLK2 signal. The BUSCLK/BUSCLK2 signal resumes its operation with the divided clock set after it had stopped. While the BUSCLK/BUSCLK2 signal is stopped, the SDRAM refresh control register (RFSn) of SDRAM also stops operating. Therefore, re-set the refresh cycle before setting the BMC register so that refresh occurs correctly within the refresh interval required by the SDRAM to be connected (n = 6, 4, 3, or 1).

If the power-saving mode is selected by setting the PDWN bit to 1, the internal system clock is stopped, and all the internal registers are initialized.

This register can be read or written in 8-bit units.

Cautions 1. Immediately before setting the PDWN bit to 1, be sure to clear (0) all the MEn bits of bus cycle type configuration registers 0 and 1 (BCT1 and BCT0) to 0 (clear the MEn bits to 0 and set the PDWN bit to 1 successively) (n = 7 to 0).

The operation is not guaranteed if another bus cycle occurs between clearing the MEn bits to 0 and setting the PDWN bit to 1.

For the setting procedure, refer to Figure 3-14 (the operation is not guaranteed if the setting is made in a way other than the procedure shown in Figure 3-14).

2. When the PDWN bit is set to 1, all the internal settings of the NA85E535 are initialized. To change the division ratio of the internal system clock set by the CKMD1 and CKMD0 pins by using the CKm1 and CKM0 bits, set the normal operation mode (by clearing the PDWN bit to 0) and then set the CKM1 and CKM0 bits again.

For the setting procedure, refer to Figure 3-15 (the operation is not guaranteed if the setting is made in a way other than the procedure shown in Figure 3-15).

When using the division ratio of the internal system clock by changing the setting of the CKM1 and CKM0 bits, a clock whose frequency is different from the set division ratio is output if the PWDN bit is set to 1 (a glitch is generated on the BUSCLK/BUSCLK2 signal). Therefore, the external circuit using the BUSCLK/BUSCLK2 signal must be initialized, depending on whether the PDWN bit is set to 1.

3. Change the division ratio by changing the setting of the CKM1 and CKM0 bits in the procedure shown in Figure 3-16 (the operation is not guaranteed if the setting is made in a way other than the procedure shown in Figure 3-16).

In this case, an NPB write retry cycle may be repeatedly issued until the phase relationship of the clock is stabilized.

Figure 3-13. Bus Mode Control Register (BMC)

	7	6	5	4	3	2	1	0	Address	Default value
BMC	V2EN	0	0	0	0	PDWN	CKM1	CKM0	FFFFF498H	**Note**

Bit position	Bit name	Meaning
7	V2EN	Selects the specification of the VSB that connects the NA85E535. Set this bit in accordance with the CPU core to be used. If a CPU core covered by this manual is used, input a low level to this bit. 0: Conforms to VSB specifications. 1: Conforms to VSB2 specifications (support of bus reset, disconnect response, and busy response).
★ 2	PDWN	Selects an operation mode of the NA85E535. When this bit is set to 1, the internal system clock stops. 0: Normal operation mode (default value) 1: Power-saving mode (Operation stops.)
★ 1, 0	CKM1, CKM0	Sets the division ratio by which the VBCLK/VBCLK2 signal is to be divided to generate the bus clock (BUSCLK/BUSCLK2). Divided BUSCLK signal is used as an internal system clock.

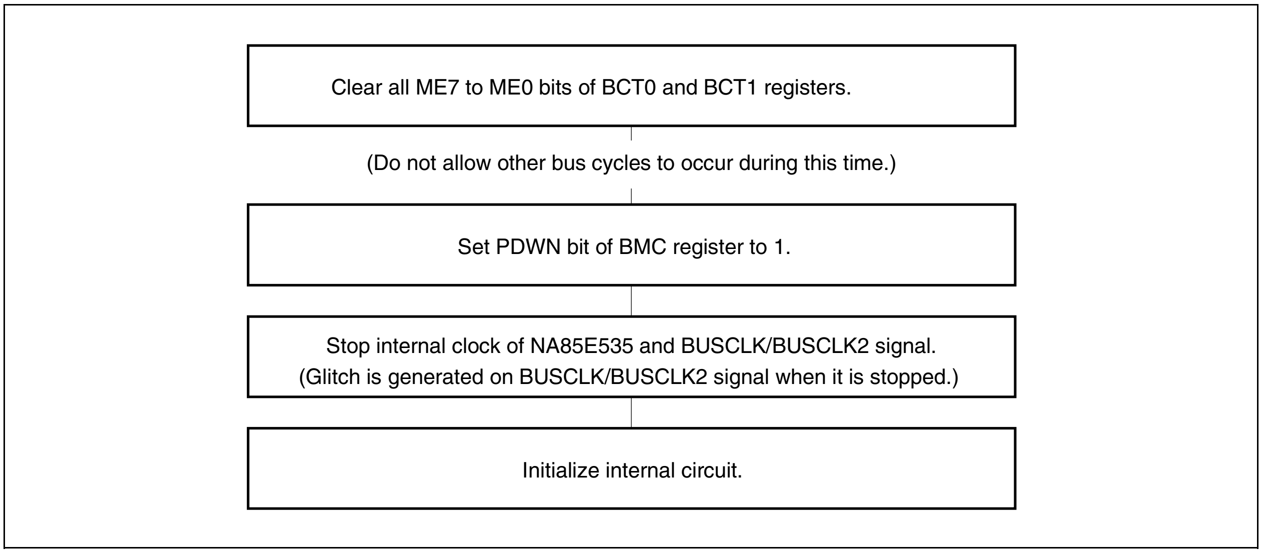
CKM1	CKM0	Division ratio of VBCLK/VBCLK2 signal to generate BUSCLK/BUSCLK2 signal
0	0	1/1 (VBCLK/VBCLK2 is divided by 1.)
0	1	1/2 (VBCLK/VBCLK2 is divided by 2.)
1	0	1/3 (VBCLK/VBCLK2 is divided by 3.)
1	1	1/4 (VBCLK/VBCLK2 is divided by 4.)

Note The default value differs as follows, depending on the input levels of the V2EN, CKMD1, and CKMD0 pins at reset.

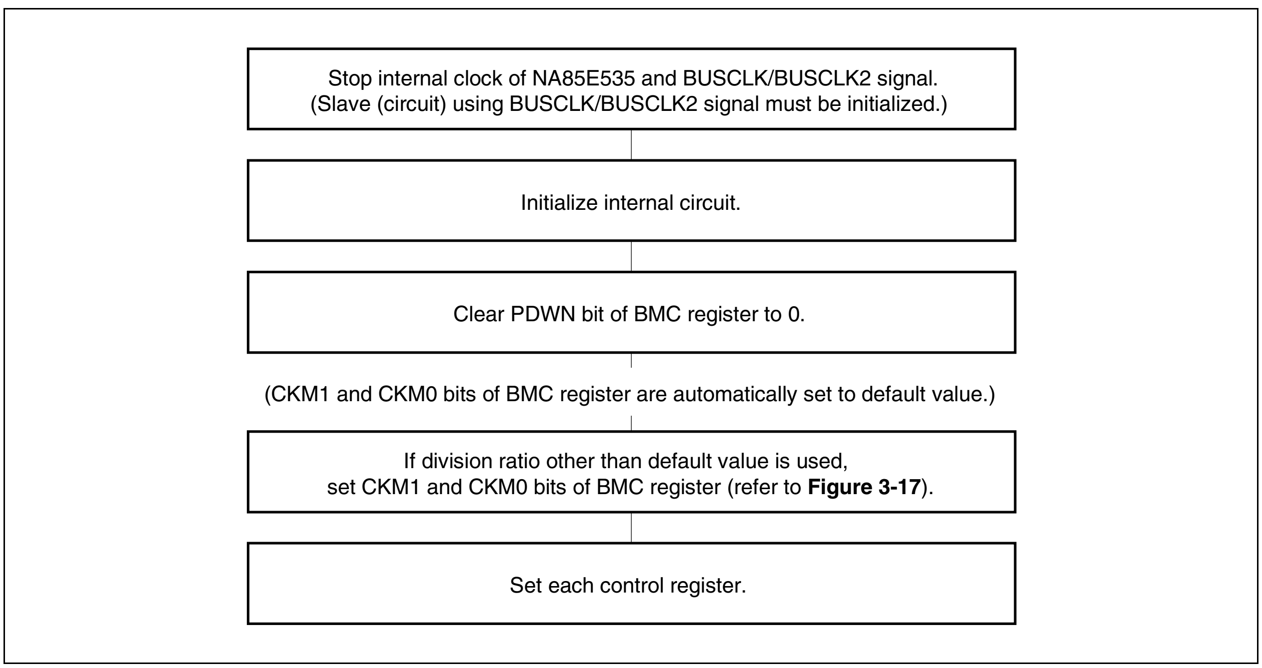
V2EN pin input level	CKMD1 pin input level	CKMD0 pin input level	Default value
High level	High level	High level	83H
		Low level	82H
	Low level	High level	81H
		Low level	80H
Low level	High level	High level	03H
		Low level	02H
	Low level	High level	01H
		Low level	00H

Remark Bits 6 to 3 are fixed to 0 (setting these bits is ignored).

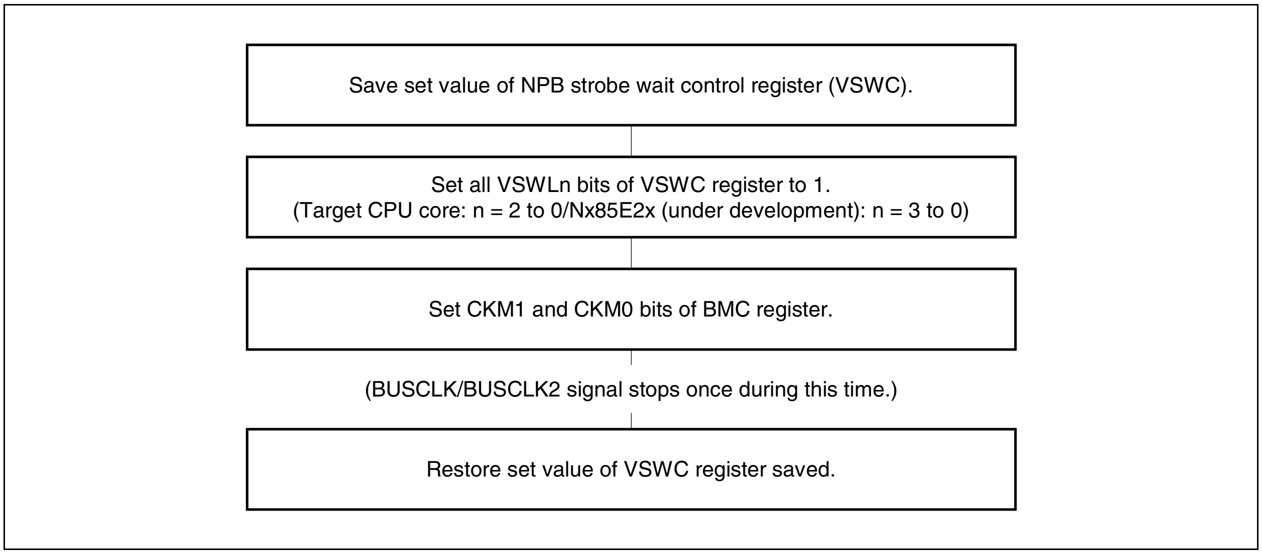
★ **Figure 3-14. Procedure of Setting PDWN Bit (1)**



★ **Figure 3-15. Procedure of Clearing PDWN Bit (0)**



★ **Figure 3-16. Procedure of Setting CKM1 and CKM0 Bits**



3.1.12 Local bus sizing control register (LBS)

The LBS register sets the data bus width of the memory to be accessed, for each CSn area (n = 7 to 0).

This register can be read or written in 16-bit units.

Figure 3-17. Local Bus Sizing Control Register (LBS)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Default value
LBS	LB71	LB70	LB61	LB60	LB51	LB50	LB41	LB40	LB31	LB30	LB21	LB20	LB11	LB10	LB01	LB00	FFFFF48EH	**Note 1**

Bit position	Bit name	Meaning
15 to 0	LBn1, LBn0	Sets the data bus width of the connected memory for each CSn area.

LBn1	LBn0	Data bus width	Maximum number of times of successive transfer[Note 2]
0	0	8 bits	32 times (VSSEQ2 to VSSEQ0 = 1, 0, 1)
0	1	16 bits	64 times (VSSEQ2 to VSSEQ0 = 1, 1, 0)
1	Any	32 bits	128 times (VSSEQ2 to VSSEQ0 = 1, 1, 1)

Notes 1. The default value differs as follows depending on the input levels of the LBS1 and LBS0 pins reset.

LBS1 pin input level	LBS0 pin input level	Default value
Low level	Low level	AAAAH
Low level	High level	5555H
High level	Any	0000H

2. The maximum number of times of successive transfer VSB can request from the NA85E535 differs depending on the data bus width setting (specify the maximum number of times of successive transfer by using VSSEQ2 to VSSEQ0, and do not input a value other than the above).
Successive transfers exceeding a page of SDRAM are prohibited.

Remark n = 7 to 0

3.1.13 DMA flyby transfer wait control register (FWC)

The FWC register sets the number of data wait states for channel n (n = 3 to 0) during DMA flyby transfer.

The set value of this register is valid during DMA flyby transfer, and the set values of the DWC0, DWC1, and PRC registers are invalid.

This register can be read or written in 16-bit units.

Figure 3-18. DMA Flyby Transfer Wait Control Register (FWC)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Default value
FWC	0	FW32	FW31	FW30	0	FW22	FW21	FW20	0	FW12	FW11	FW10	0	FW02	FW01	FW00	FFFFF494H	7777H

Bit position	Bit name	Meaning
14 to 12, 10 to 8, 6 to 4, 2 to 0	FWn2 to FWn0	Sets the number of data wait states for DMA flyby transfer for channel n.

FWn2	FWn1	FWn0	Number of data wait states
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7 (default value)

Remarks 1. n = 3 to 0

2. Bits 15, 11, 7, and 3 are fixed to 0 (setting these bits is ignored).

3.1.14 DMA flyby transfer idle control register (FIC)

The FIC register sets the number of idle states for channel n (n = 3 to 0) during DMA flyby transfer.

The set value of this register is valid during DMA flyby transfer, and the set value of the BCC register is invalid.

This register can be read or written in 16-bit units.

Figure 3-19. DMA Flyby Transfer Idle Control Register (FIC)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Default value
FIC	0	0	FI31	FI30	0	0	FI21	FI20	0	0	FI11	FI10	0	0	FI01	FI00	FFFFF496H	3333H

Bit position	Bit name	Meaning
13, 12, 9, 8, 5, 4, 1, 0	FIn1, FIn0	Sets the number of idle states for DMA flyby transfer for channel n.

FIn1	FIn0	Number of idle states
0	0	0
0	1	1
1	0	2
1	1	3 (default value)

Remarks 1. n = 3 to 0

2. Bits 15, 14, 11, 10, 7, 6, 3, and 2 are fixed to 0 (setting these bits is ignored).

3.2 Examples of Memory Connection

3.2.1 Example of SRAM connection

Figure 3-20. SRAM Connection Example 1

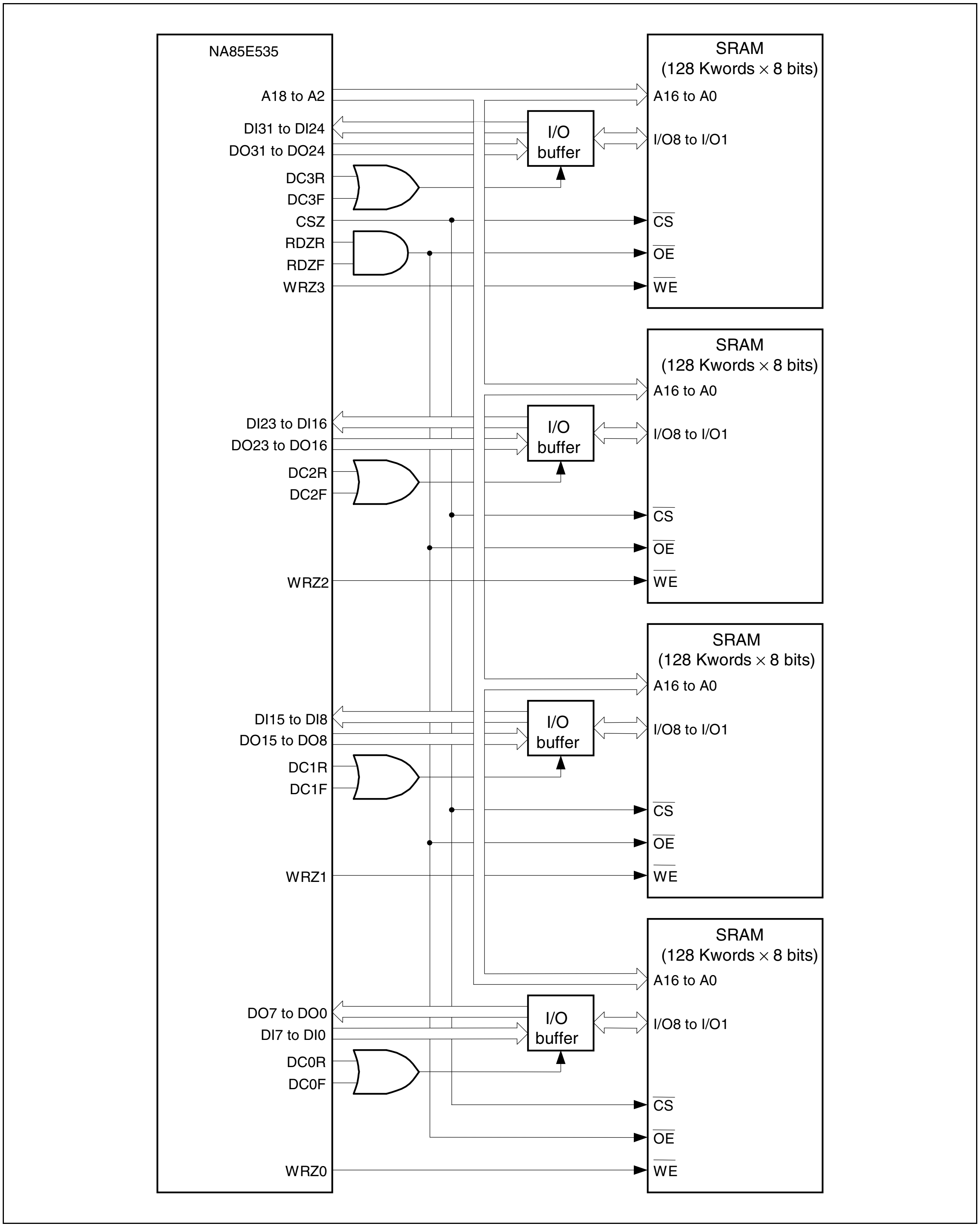
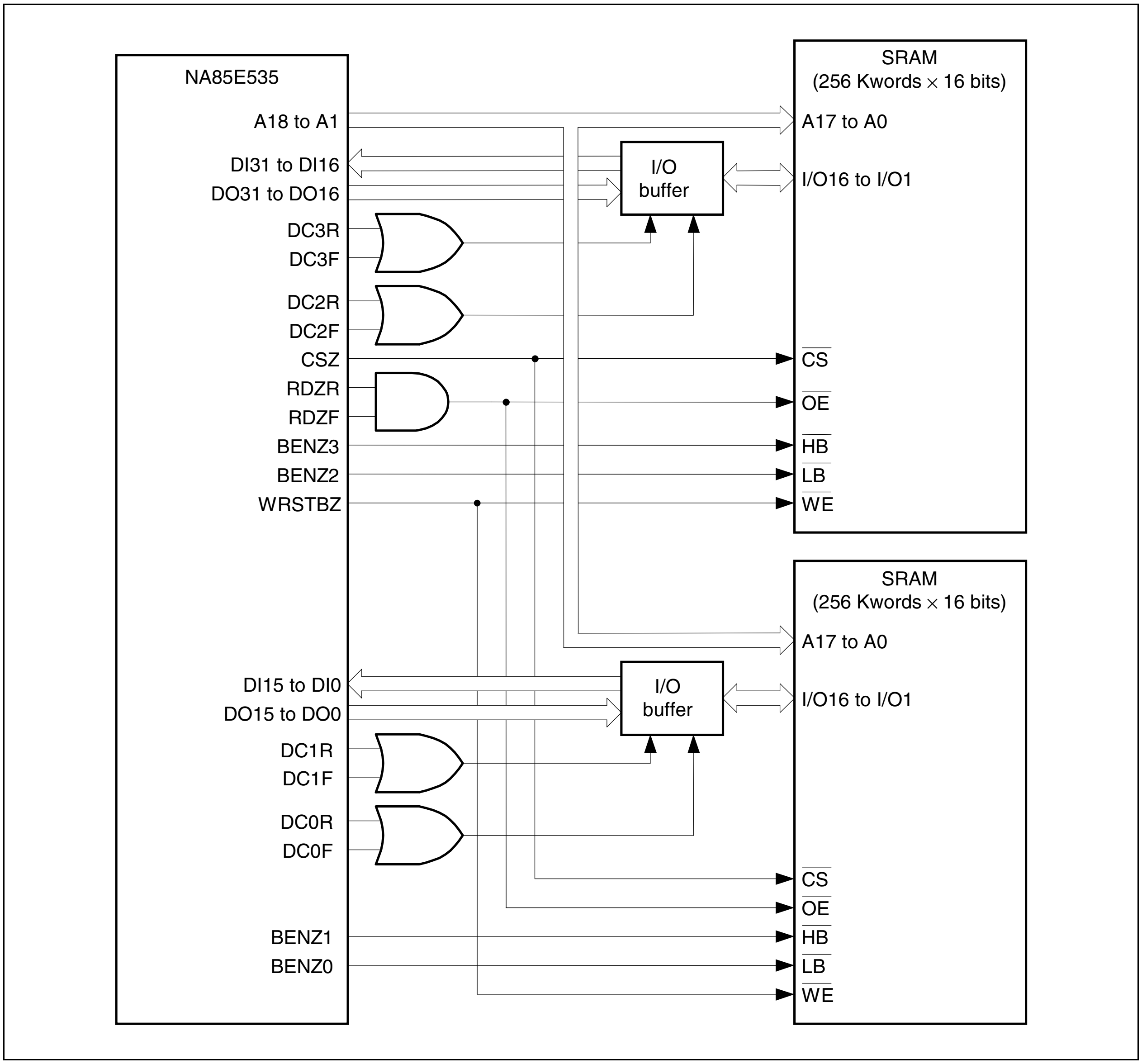


Figure 3-21. SRAM Connection Example 2



3.2.2 Example of page ROM connection

Figure 3-22. Page ROM Connection Example 1 (Data Bus Width: 16 Bits)

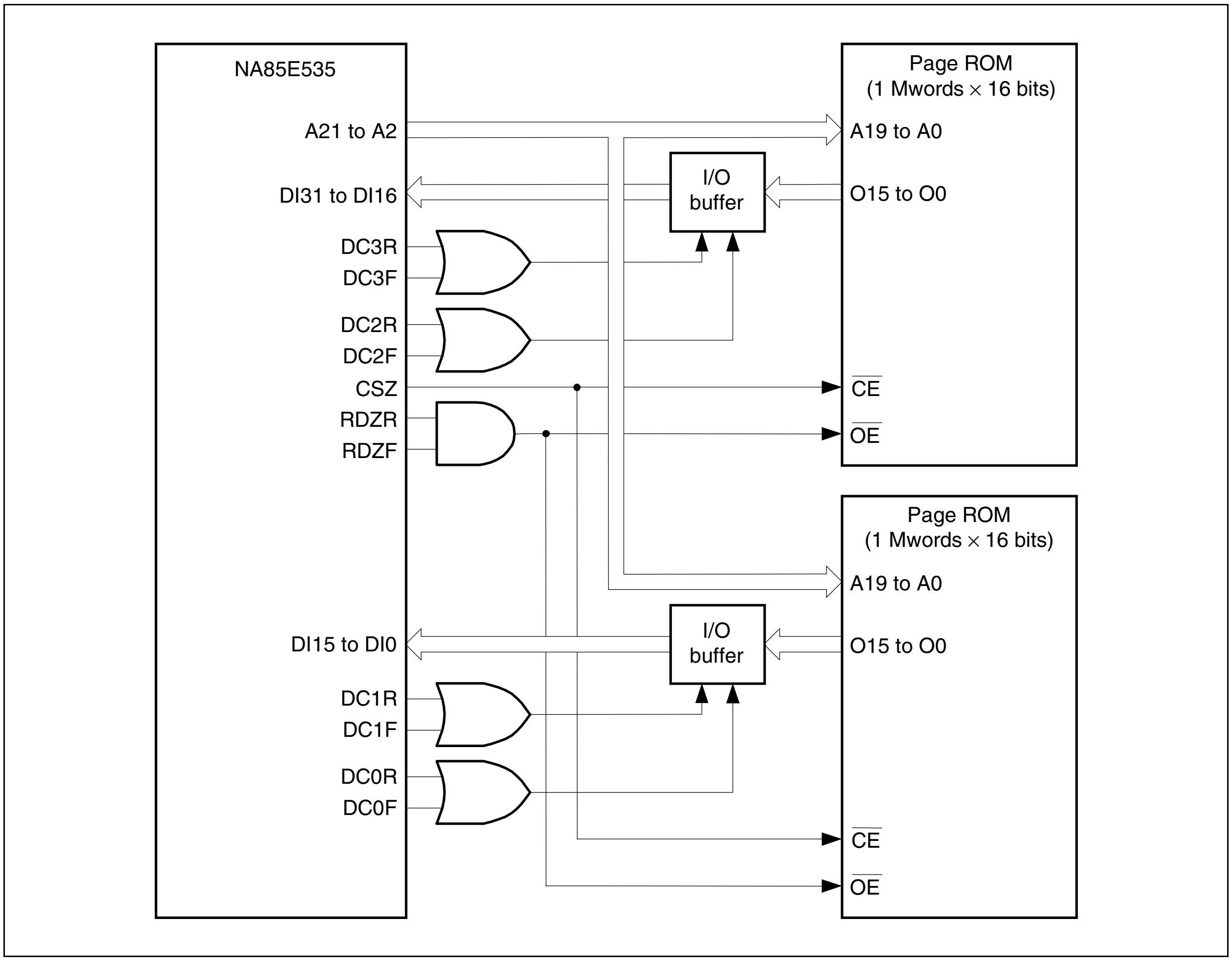
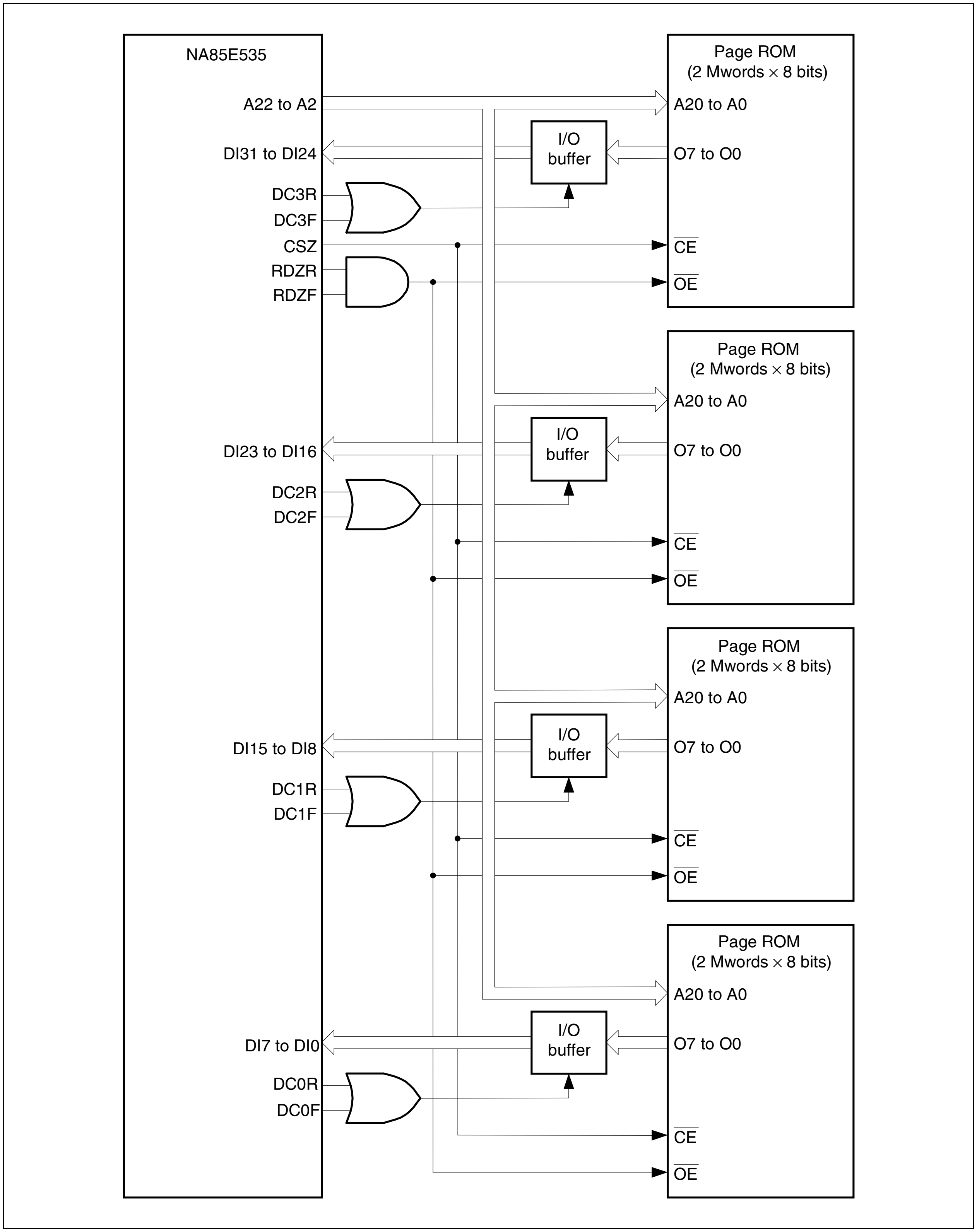
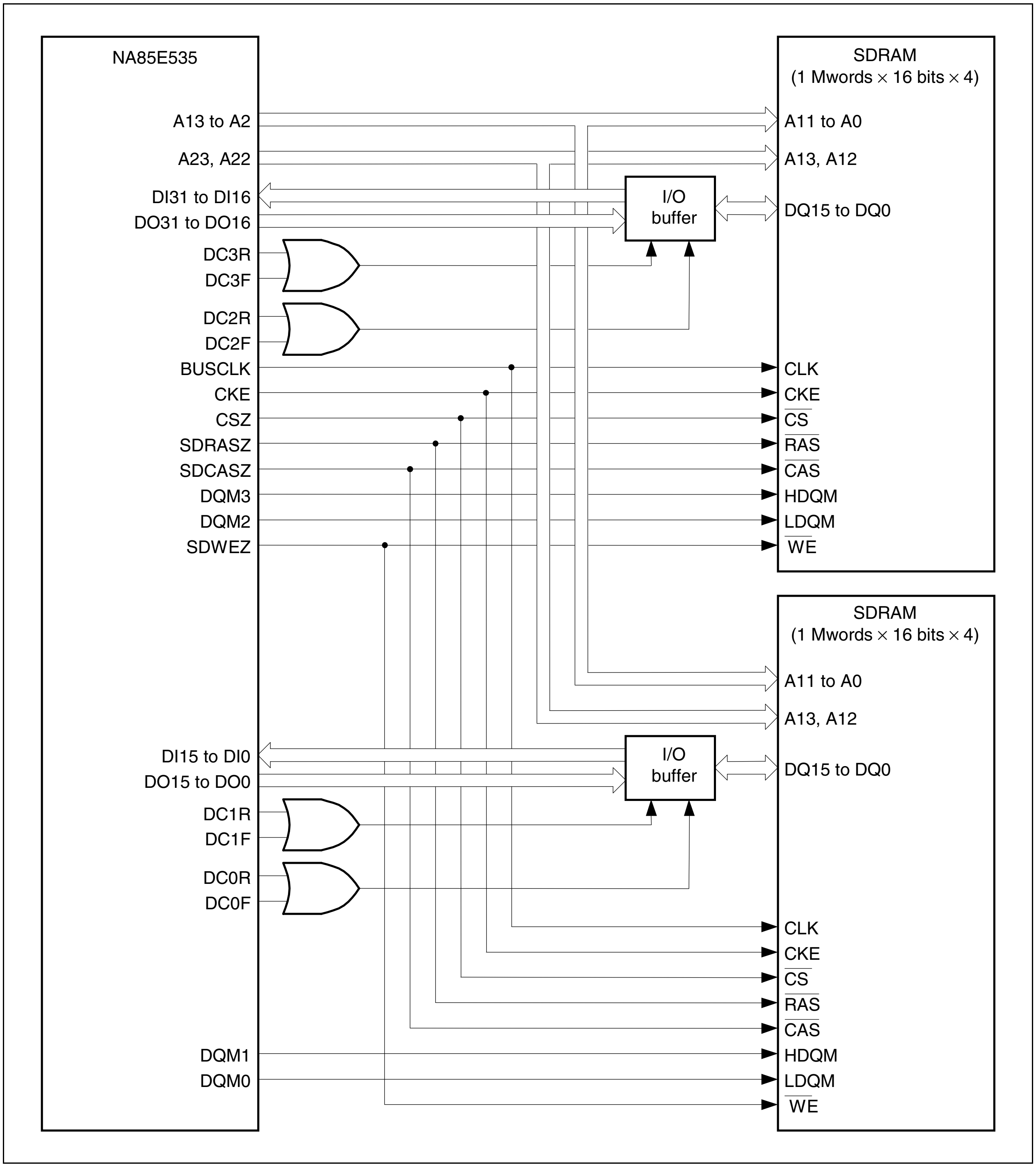


Figure 3-23. Page ROM Connection Example 2 (Data Bus Width: 8 Bits)



3.2.3 Example of SDRAM connection

Figure 3-24. Example of 64Mb SDRAM Connection



(1) Output of each address and connection of SDRAM

The setting of SDRAM configuration register n (SCRn) for each data bus width (8 bits, 16 bits, and 32 bits), physical address, address output from the NA85E535, and connection of SDRAM to the NA85E535 are explained below.

(a) With data bus width of 8 bits

Here is an example of connecting 64 Mb SDRAM (2 Mwords × 8 bits × 4 banks) when the data bus width is 8 bits:

- Setting of SCRn register
  SSO1, SSO0 = 00: Data bus width = 8 bits
  RAW1, RAW0 = 01: Row address width = 12 bits
  SAW1, SAW0 = 01: Column address width = 9 bits

- Physical address
  A22, A21: Bank address
  A20 to A9: Row address
  A8 to A0: Column address

- Address output from NA85E535
  A22, A21: Bank address
  A11 to A0: Row address (12 bits), column address (9 bits)

Row address and bank address output with active command

A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
a25	a24	a23	a22	a21	a20	a19	a18	a17	a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a13	a12	a11	a10	a9

Bank address (A22, A21) Row address (A11 to A0)

Column address output with read/write command

A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a12	a11	a10	0	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0

Column address (A8 to A0)

- Connection of SDRAM to NA85E535
  A22, A1 (NA85E535) → BA0 (A13), BA1 (A12) (SDRAM)
  A11 to A0 (NA85E535) → A11 to A0 (SDRAM)

(b) With data bus width of 16 bits

Here is an example of connecting 512 Mb SDRAM (8 Mwords × 16 bits × 4 banks) when the data bus width is 16 bits:

- Setting of SCRn register
  SSO1, SSO0 = 01: Data bus width = 16 bits
  RAW1, RAW0 = 10: Row address width = 13 bits
  SAW1, SAW0 = 10: Column address width = 10 bits

- Physical address
  A25, A24: Bank address
  A23 to A11: Row address
  A10 to A1: Column address

- Address output from NA85E535
  A25, A24: Bank address
  A13 to A1: Row address (13 bits), column address (10 bits)

Row address and bank address output with active command

A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a13	a12	a11	a10

Bank address (A25, A24) — Row address (A13 to A1)

Column address output with active command

A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a12	a11	0	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0

Column address (A10 to A1)

- Connection of SDRAM to NA85E535
  A25, A24 (NA85E535) → BA0 (A14), BA1 (A13) (SDRAM)
  A13 to A1 (NA85E535) →A12 to A0 (SDRAM)

(c) With data bus width of 32 bits

Here is an example of connecting 512 Mb SDRAM (256 Mb SDRAM (4 Mwords × 16 bits × 4 banks) × 2) when the data bus width is 32 bits:

- Setting of SCRn register
  SSO1, SSO0 = 10: Data bus width = 32 bits
  RAW1, RAW0 = 10: Row address width = 13 bits
  SAW1, SAW0 = 01: Column address width = 9 bits

- Physical address
  A25, A24: Bank address
  A23 to A11: Row address
  A10 to A2: Column address

- Address output from NA85E535
  A25, A24: Bank address
  A14 to A2: Row address (13 bits), column address (9 bits)

Row address and bank address output with active command

A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
a25	a24	a23	a22	a21	a20	a19	a18	a17	a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a13	a12	a11	a10	a9

Bank address (A25, A24) — Row address (A14 to A2)

Column address output with active command

A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a12	0	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0

Column address (A10 to A2)

- Connection of SDRAM to NA85E535
  A25, A4 (NA85E535) → BA0 (A14), BA1 (A13) (SDRAM)
  A14 to A2 (NA85E535) → A12 to A0 (SDRAM)

(2) Bank address output

The NA85E535 precharges the bank it is about to access when it outputs a row address immediately after page change as a bank precharge command. After bank change, the NA85E535 also precharges the bank previously accessed when it outputs a column address. Therefore, the bank is precharged both when a row address is output and when a column address is output. For this reason, always connect the pins of NA85E535 that output a bank address (A22 and A21) to the bank address pins (A13 and A12) of SDRAM when SDRAM is connected as explained in **3.2.3 (1) (a) With data bus width of 8 bits**.

An example of address output when the bank precharge command is executed to change the page and bank with the connection introduced in **3.2.3 (1) (a) With data bus width of 8 bits** is shown below.

(a) To change page (with data bus width of 8 bits)

Because the bank to be accessed is precharged, the physical addresses (A25 to A9) are output from the A25 to A0 pins of the NA85E535.

A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
a25	a24	a23	a22	a21	a20	a19	a18	a17	a25	a24	a23	a22	a21	a20	0	a18	a17	a16	a15	a14	a13	a12	a11	a10	a9

Bank address to be accessed (A22–A21)

Row address (A11–A0)

(b) To change bank (with data bus width of 8 bits)

Because the bank previously accessed is precharged, the physical addresses previously accessed (A25 to A9) are output from the A25 to A9 pins of the NA85E535.

A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
a25	a24	a23	a22	a21	a20	a19	a18	a17	a16	a15	a14	a12	a11	a10	0	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0

Bank address previously accessed (A22–A21)

Column address (A8–A0)

The bits that determine the precharge mode (A10: 8-bit data bus width, A11: 16-bit data bus width, A12: 32-bit data bus width) output a high level when the all-bank precharge command is executed, and a low level when any other precharge command is executed.

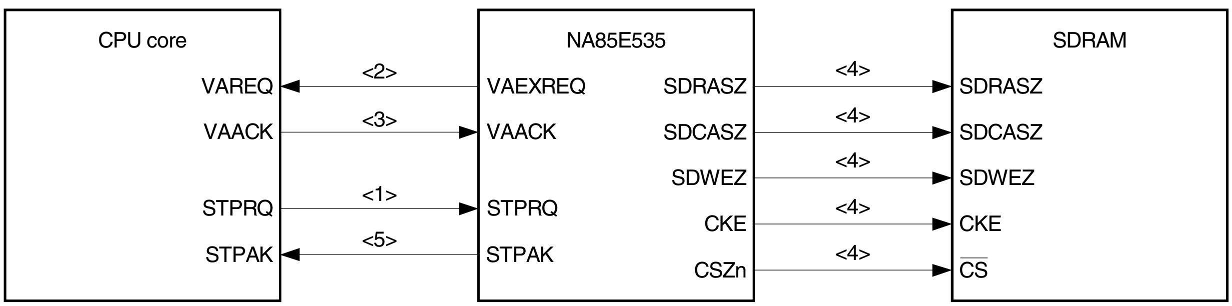
3.3 STOP Function

When the CPU core enters the STOP mode, the NA85E535 operates in the following sequence (refer to **Figure 3-25**).

<1> When hardware STOP or software STOP instruction is executed, the CPU core inputs the STOP mode request signal (STPRQ) to the NA85E535.
<2> The NA85E535 outputs the VSB mastership request signal (VAEXREQ) to the CPU core.
<3> The CPU core inputs an acknowledge signal (VAACK) to the NA85E535 in response to the VAREQ signal.
★ <4> If there is a CSn area set as SDRAM, the all bank precharge command, NOP command, and self-refresh command are output.
<5> The NA85E535 returns an acknowledge signal (STPAK) to the CPU core in response to the STPRQ signal.

The NA85E535 returns the STPAK signal two clocks, at the earliest, after it has received the STPRQ signal.
★ If SDRAM is connected, the NA85E535 enters the STOP status when the REFRQZ signal and CKE signal go low.

Figure 3-25. Operation of NA85E535 in STOP Mode



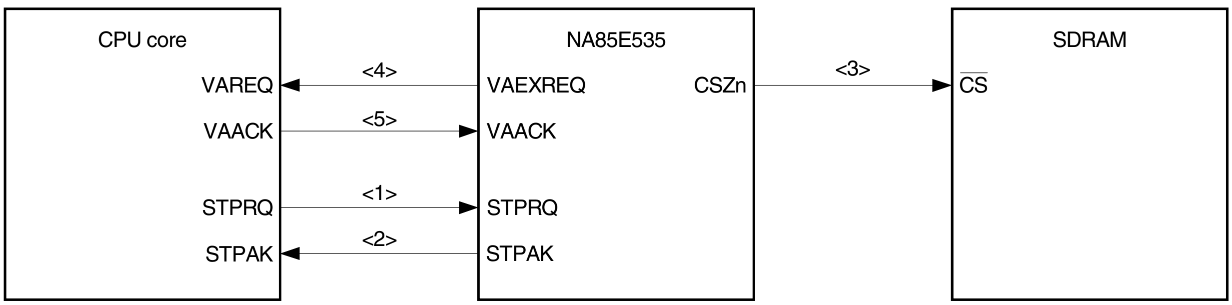
Remark n = 6, 4, 3, or 1

When releasing the STOP mode, the NA85E535 operates in the following sequence (refer to **Figure 3-26**).

<1> The STOP mode request signal (STPRQ) from the CPU core is cleared.
<2> After the STPRQ has been cleared, the NA85E535 clears its acknowledge signal (STPAK) in response to the STPRQ signal at the next rising edge of VBCLK.
<3> If there is a CSn area that is set as SDRAM, a NOP command is output and an idle state (BCW wait × 4 BUSCLK clocks) is inserted (n = 6, 4, 3, or 1).
<4> The VSB mastership request signal (VAEXREQ) is cleared.
<5> The acknowledge signal (VAACK) from the CPU core in response to the VAEXREQ signal is cleared.

If SDRAM is not set, <3> is not executed (for details, refer to **Figure 4-23 SDRAM Self-Refresh Timing (STOP Timing)**).

Figure 3-26. Operation of NA85E535 When STOP Mode Is Released



Remark n = 6, 4, 3, or 1

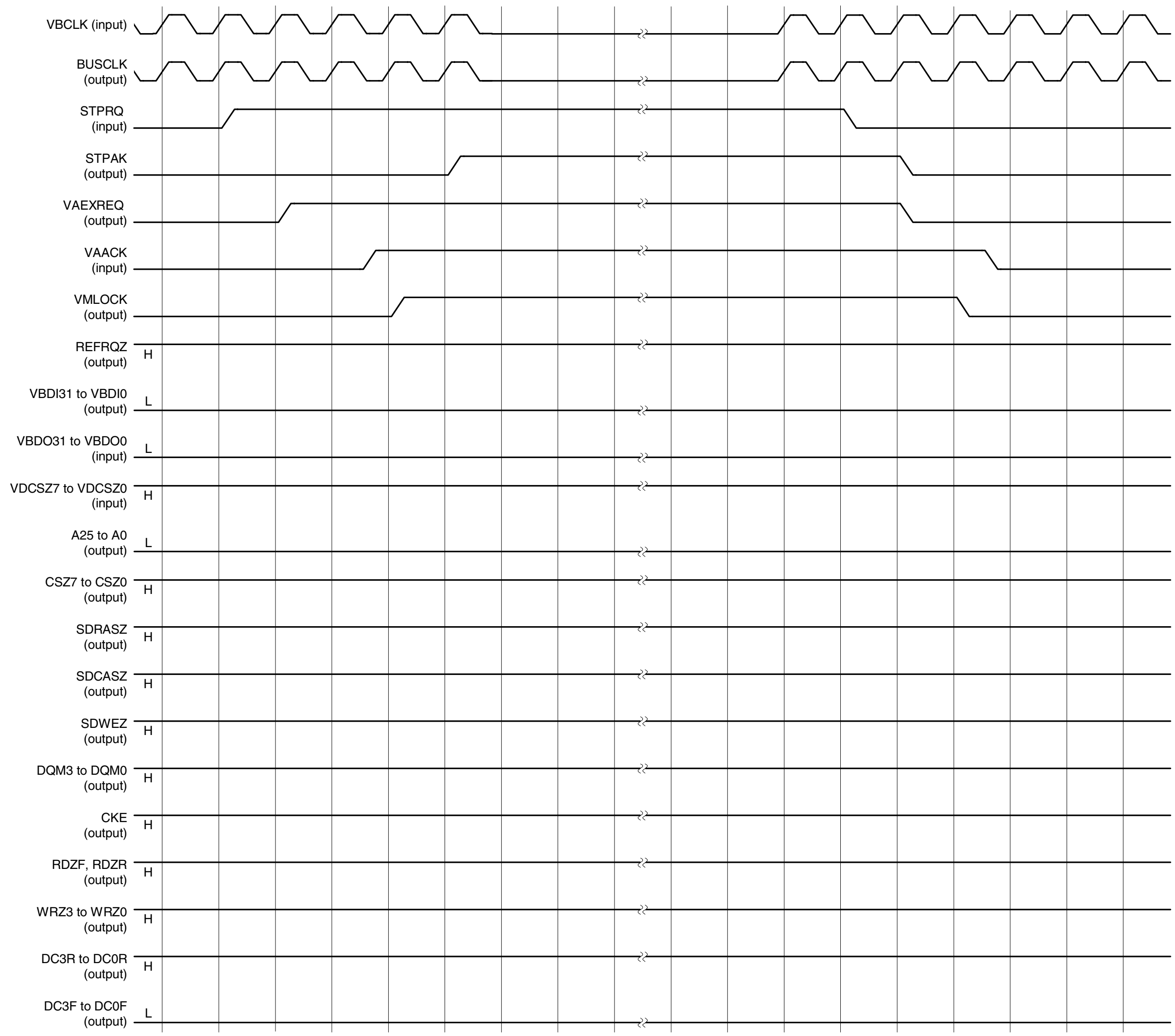
★ **(2) Timing of setting/releasing STOP mode**

Figure 3-27 shows the timing of setting and releasing the STOP mode.

Remark For details of the VSB signals, refer to **NU85E Hardware User's Manual (A14874E)**.

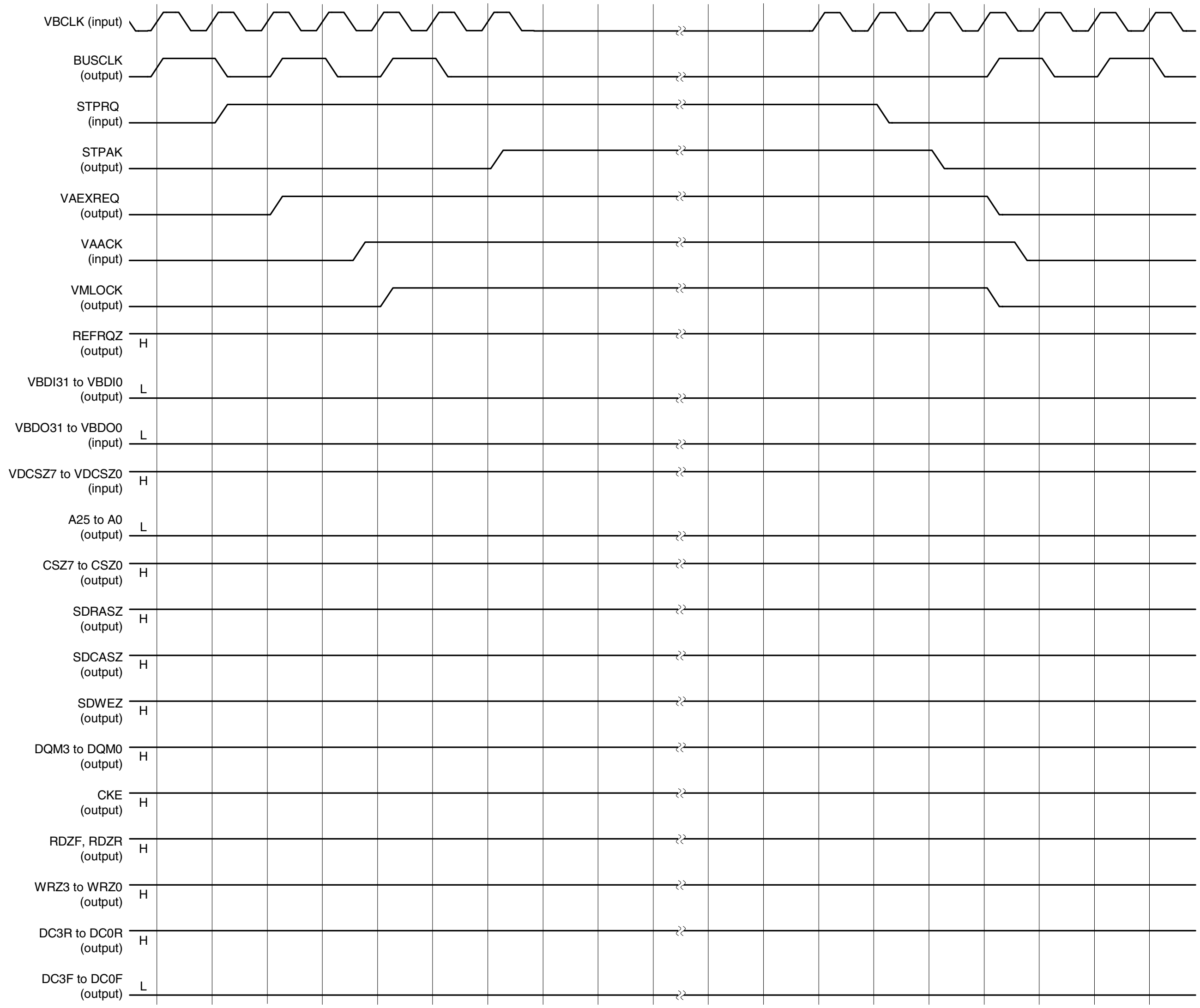
★Figure 3-27. Timing of Setting/Releasing STOP Mode (Without SDRAM Setting) (1/4)

(a) Division by 1



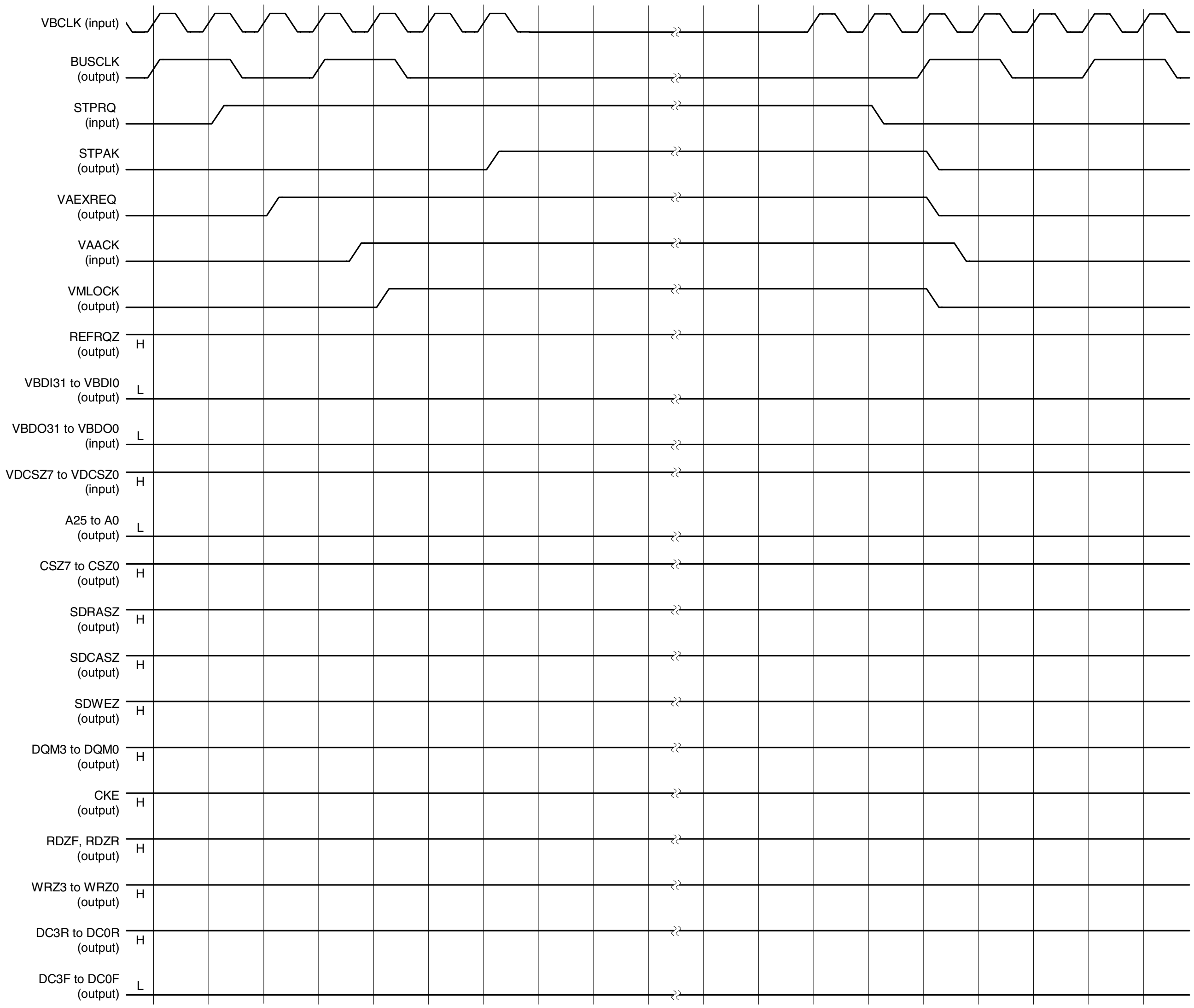
★Figure 3-27. Timing of Setting/Releasing STOP Mode (Without SDRAM Setting) (2/4)

(b) Division by 2



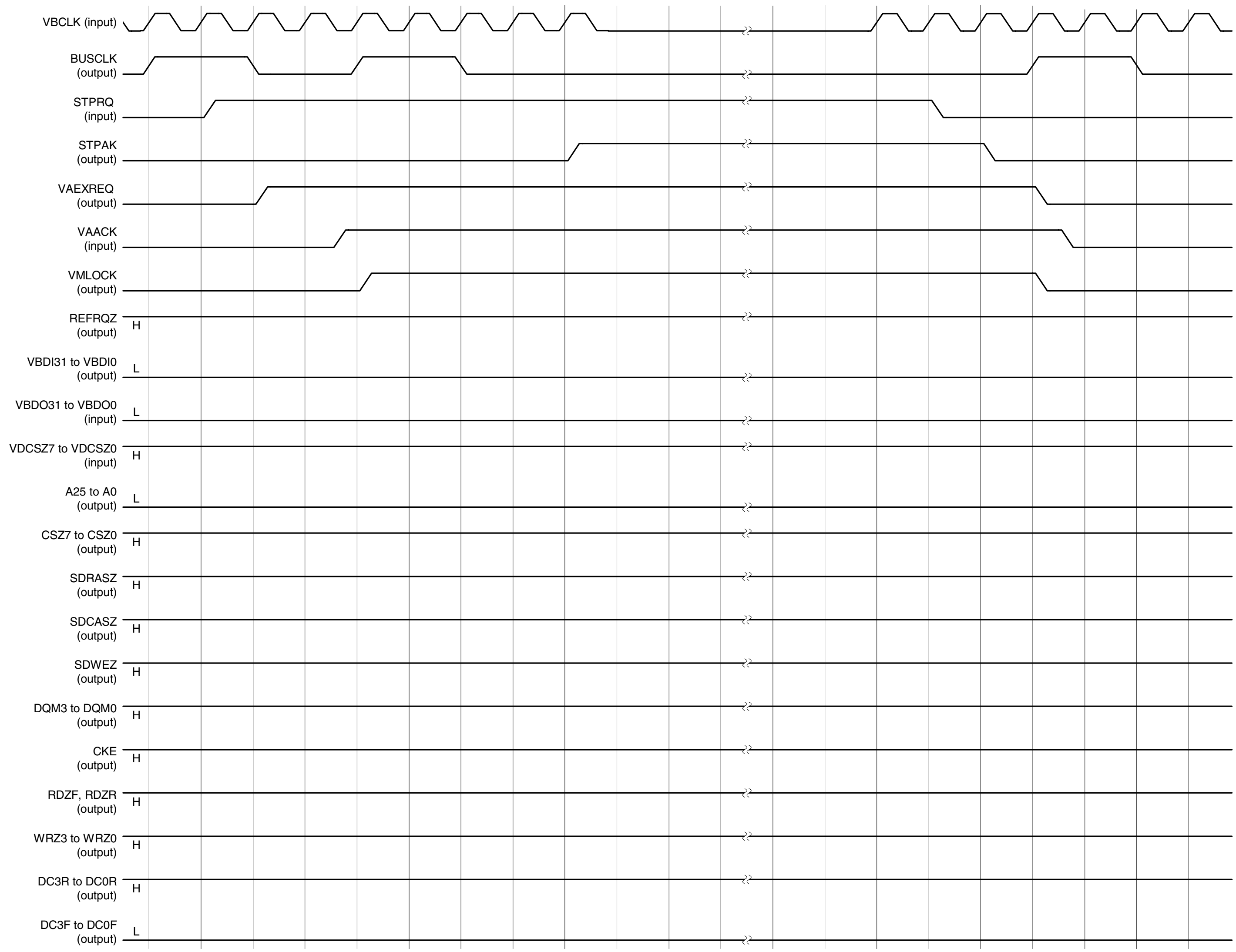
★**Figure 3-27. Timing of Setting/Releasing STOP Mode (Without SDRAM Setting) (3/4)**

(c) Division by 3



★**Figure 3-27. Timing of Setting/Releasing STOP Mode (Without SDRAM Setting) (4/4)**

(d) Division by 4



3.4 Bus Hold Function

When the HLDRQZ signal is asserted, the NA85E535 enters the bus hold status. When the NA85E535 has completely entered the bus hold status, the HLDAKZ signal is asserted. While the NA85E535 is in the bus hold status, the HLDAKZ signal stays active.

In the bus hold status, the NA85E535 is the bus master of the VSB. The external memory connection pins of the NA85E535 must be designed on the user logic side so that the signals do not conflict in the bus hold status. For the details of the pin statuses in the bus hold status, refer to **Table 2-8 Pin Status in Each Operation Mode**.

When the HLDRQZ signal is inactive, the NA85E535 enters the normal status.

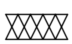
★ **Caution Make sure that the external bus master accesses SDRAM during bus hold after the bank precharge command has been executed.**

(1) Bus hold procedure

<1> The external memory inputs an external bus hold request signal (HLDRQZ) to the NA85E535.
<2> The NA85E535 outputs the VSB mastership request signal (VAEXREQ) to the CPU core.
<3> The current bus cycle is completed.
<4> The CPU core inputs an acknowledge signal (VAACK) to the NA85E535 in response to the VAEXREQ signal.
<5> The NA85E535 returns an acknowledge signal (HLDAKZ) to the external memory in response to the HLDRQZ signal.
:
Bus hold status
:
<6> The HLDRQZ signal is deasserted.
<7> Because the bus hold request from the external memory has been cleared, the HLDAKZ signal is inactive.
<8> When the bus cycle in the bus hold status is complete, the VAEXREQ signal is inactive.
<9> The VAACK signal from the CPU core is deasserted, and the bus hold status ends.
<10> The CPU core is now the master and starts a VSB bus cycle.

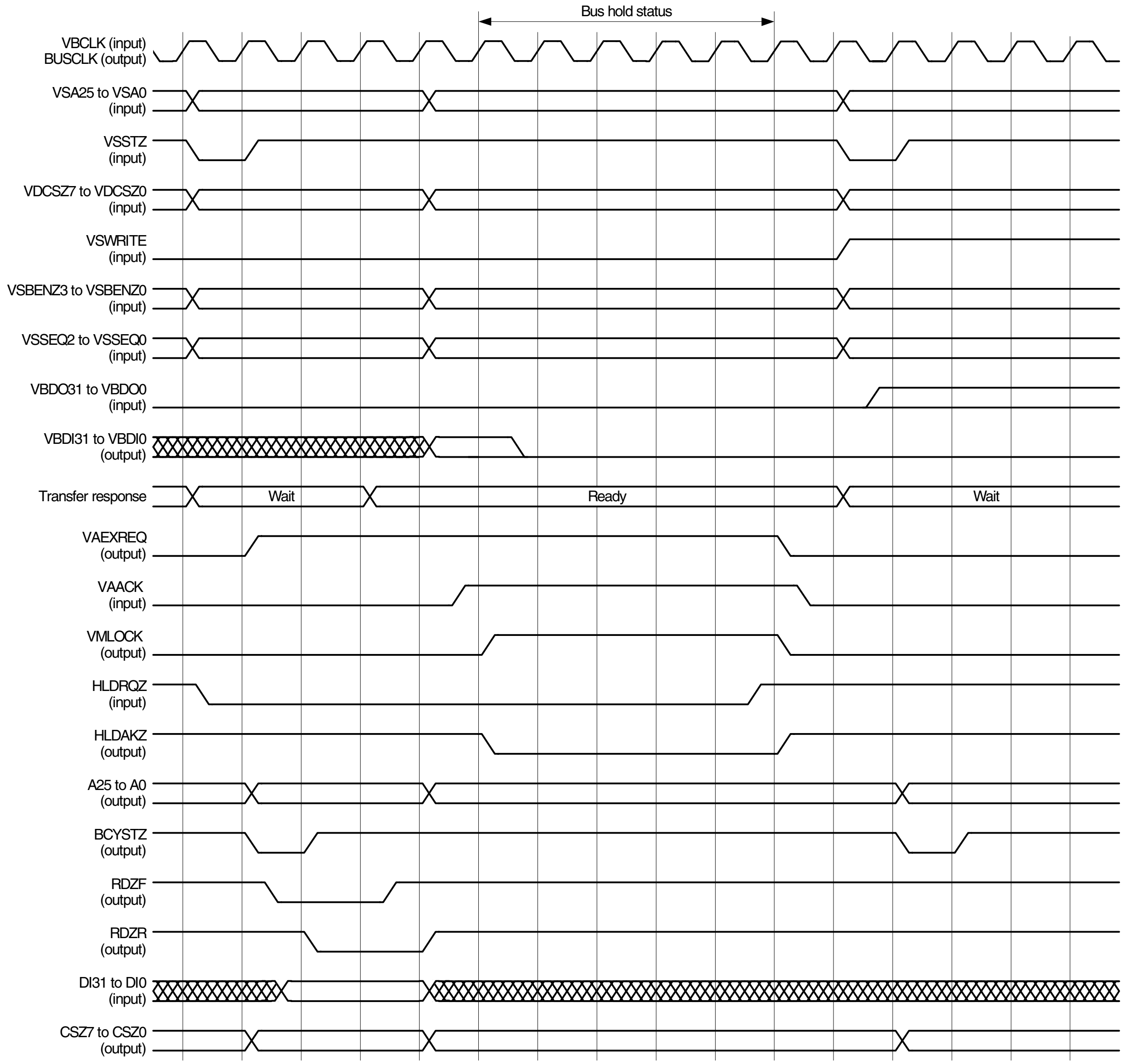
(2) Bus hold timing

An example of the bus hold timing is illustrated on the next page.

Remarks 1.  : Undetermined status (output), or any level (input)

2. For details of the VSB signals, refer to **NU85E Hardware User's Manual (A14874E)**.

★Figure 3-28. Bus Hold Timing

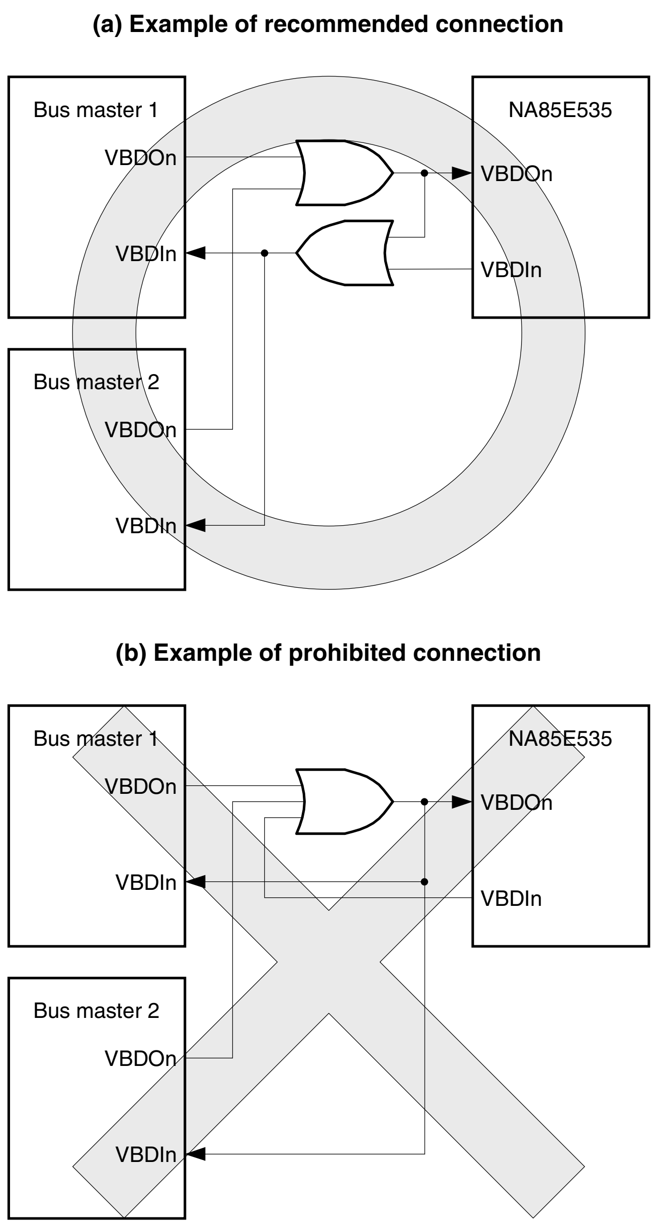


★ 3.5 Cautions

3.5.1 Connection to VSB

In a system where two or more bus masters exist on the VSB (VSB multi-master configuration), make sure that the logical sum (OR) of each bus master output data (VBDOn) and the NA85E535 output data (VBDIn) is not input to the input pin (VBDOn) of the NA85E535.

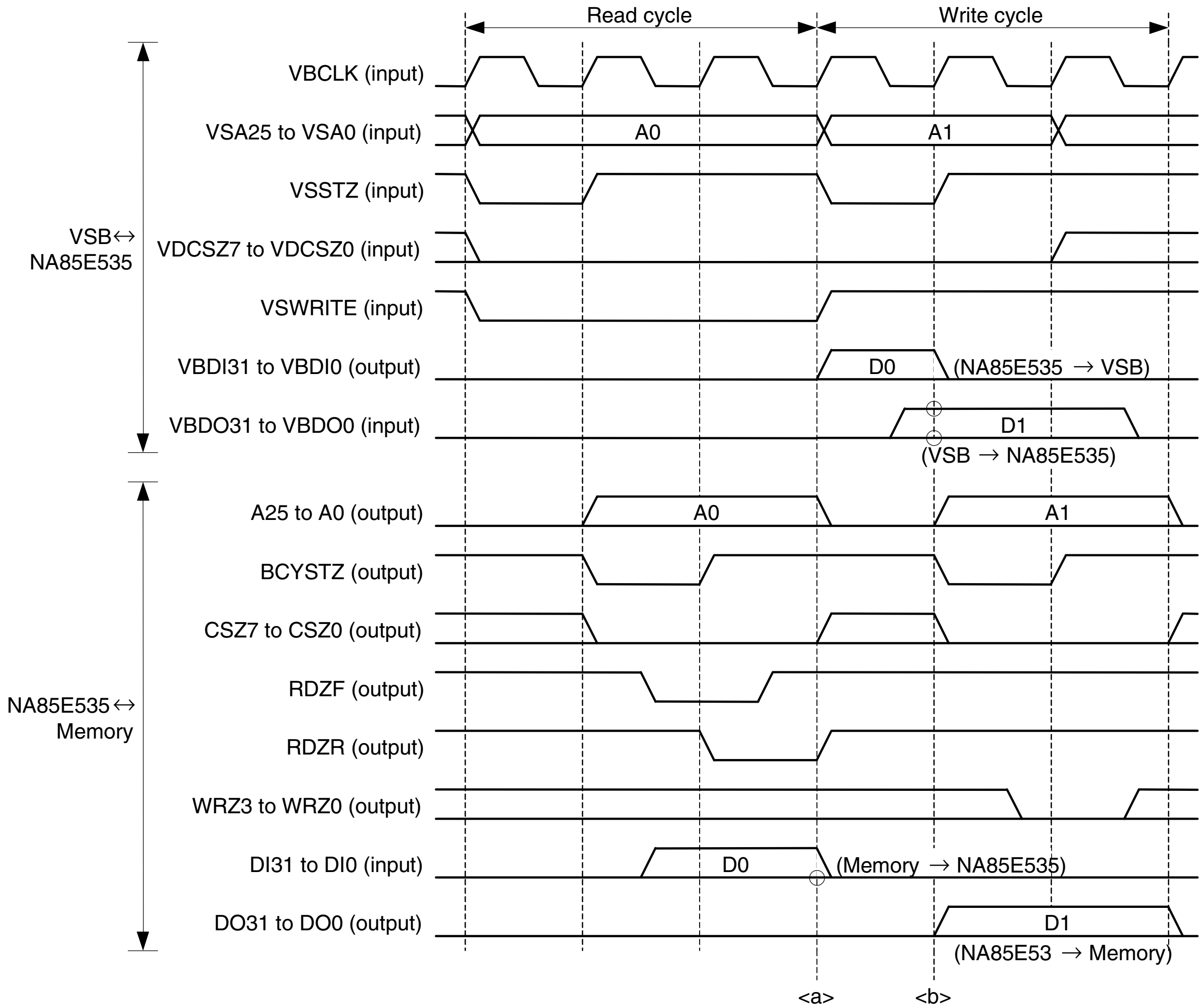
Figure 3-29. Example of Connection of MEMC and Bus Master in VSB Multi-Master Configuration



Remark n = 31 to 0

In the following memory access timing, for example, correct data is not input to the NA85E535 in a system with the prohibited connection shown in Figure 3-29 (b), because the logical sum (OR) of the input data ‘D0’ from the memory and the input data ‘D1’ from the VSB is latched at the timing <b> in Figure 3-30.

Figure 3-30. Example of Memory Access Timing



Remark <a>: Data from memory is latched and output to the VSB.
<b>: Data from the VSB is latched and output to memory.
○: Sampling timing

3.5.2 Designing high-speed circuit

When designing an interface with high-speed clocked external memory (especially SDRAM) by using the NA85E535, the external read data setup time is very critical. This data setup time can be relaxed in the following ways.

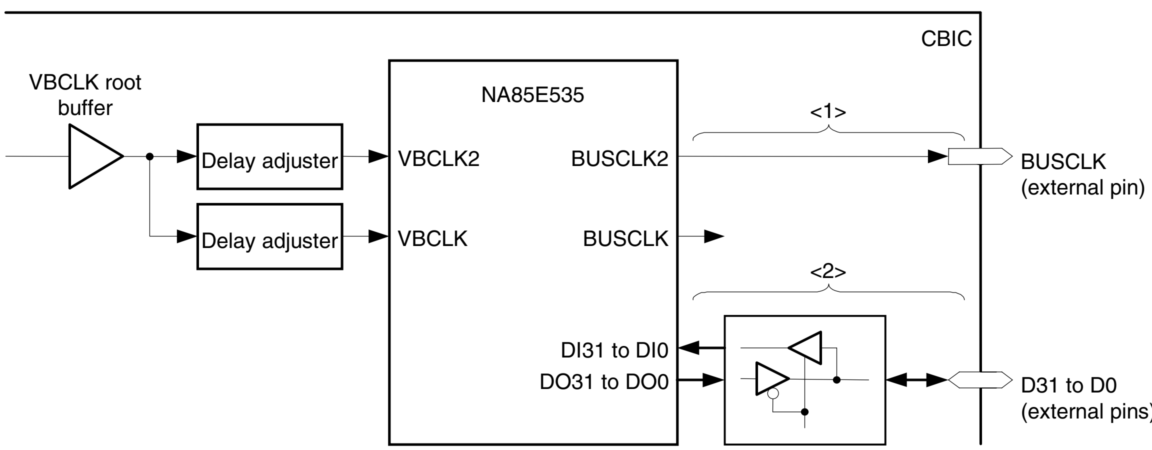
- Output the bus clock as quickly as possible (minimize the delay value with respect to the system clock).
- Locate the BUSCLK2 and DI31 to DI0 pins of the NA85E535 and the external pins of the CBIC product as closely as possible (as shown in <1> and <2> in Figure 3-31), to minimize the delay value.

The NA85E535 has a system clock input pin (VBCLK2) and a bus clock output pin (BUSCLK2) to support a high-speed memory interface, in addition to the normal system clock input pin (VBCLK) and bus clock output pin (BUSCLK). The VBCLK2 pin is a clock input pin dedicated to generation of the bus clock output by the BUSCLK2 pin (the logical operations of the BUSCLK2 and BUSCLK signals are the same).

The delay time from input of the VBCLK2 signal to output of the BUSCLK2 signal is designed to be shorter than the delay time from input of the VBCLK signal to output of the BUSCLK signal. To improve the bus clock output delay value of a CBIC product, therefore, use the BUSCLK2 signal as the bus clock.

Figure 3-31. Example of Measures to Relax Data Setup Time (1/2)

(a) Configuration



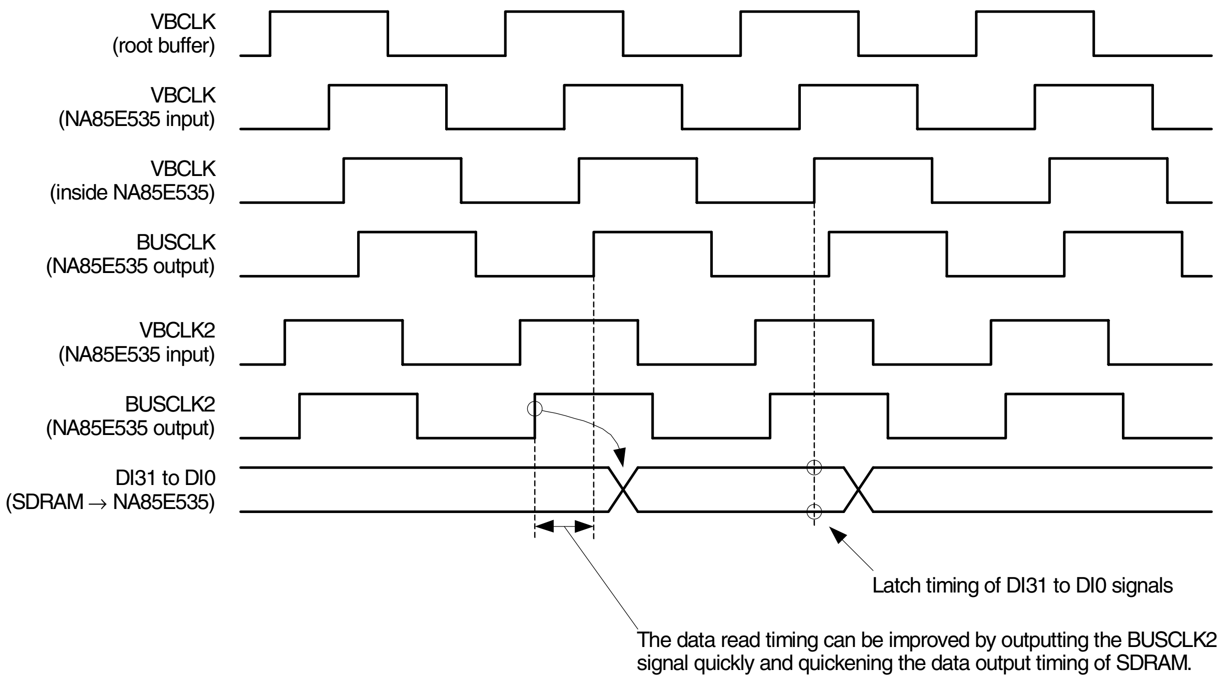
Remarks 1. The specification of the BUSCLK signal of a CBIC product can be adjusted by the delay adjuster.

2. Shorten the distances between the BUSCLK2 pin of the NA85E535 and external BUSCLK pin (<1>) and between the DI31 to DI0 pins of the NA85E535 and external D31 to D0 pins (<2>) as much as possible.

3. Be sure to input the clock to the VBCLK pin.

Figure 3-31. Example of Measures to Relax Data Setup Time (2/2)

(b) Timing chart



Remark The AC specifications are defined for the delay difference between the VBCLK signal output by the root buffer and the VBCLK and VBCLK2 signals input to the NA85E535 (for details, contact NEC).

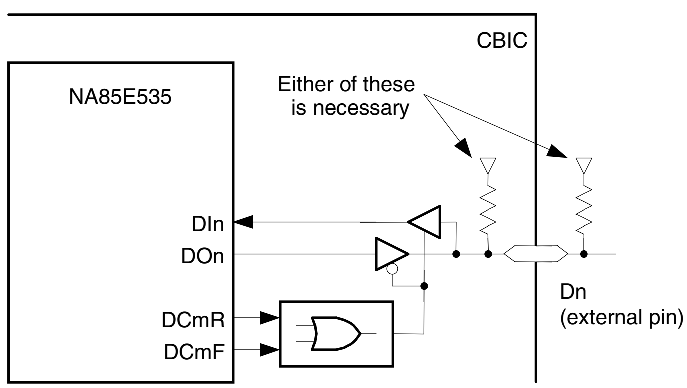
3.5.3 Processing of data bus

The NA85E535 has the DC3R to DC0R and DC3F to DC0F pins to control the data output pins, and the logical sum (OR) of these signals can be used to control output of the data I/O pins of the CBIC product.

However, because these control signals are always high level, except when the external memory is written (the output buffer goes into a high-impedance state), when the internal peripheral I/O is accessed or internal ROM is fetched, for example, the data bus goes into a high-impedance state. This means that the DC3R to DC0R and DC3F to DC0F pins can be used to select an output buffer but not to enable an input buffer.

To prevent through-current and malfunction of the memory, therefore, externally connect (on the user set board) a buffer with a pull-up function to the I/O buffer for the data bus to pull up the buffer.

Figure 3-32. Processing of Data Bus



Remark n = 31 to 0, m = 3 to 0

3.5.4 DMA acknowledge/chip select handling function

Memory access using the NA85E535 does not execute the VSB cycle and external memory access cycle simultaneously. Therefore, the acknowledge/chip select signal output by the DMA controller is input to the NA85E535, matched with the actual DMA memory cycle, and output in synchronization with the bus clock (BUSCLK). (For details, refer to Figures 4-4 to 4-13.) However, the active level of the acknowledge/chip select signal is output only during flyby transfer, and is not output during 2-cycle transfer. For this reason, a selector circuit with the following specifications must be externally connected when 2-cycle transfer and flyby transfer by DMA are used together.

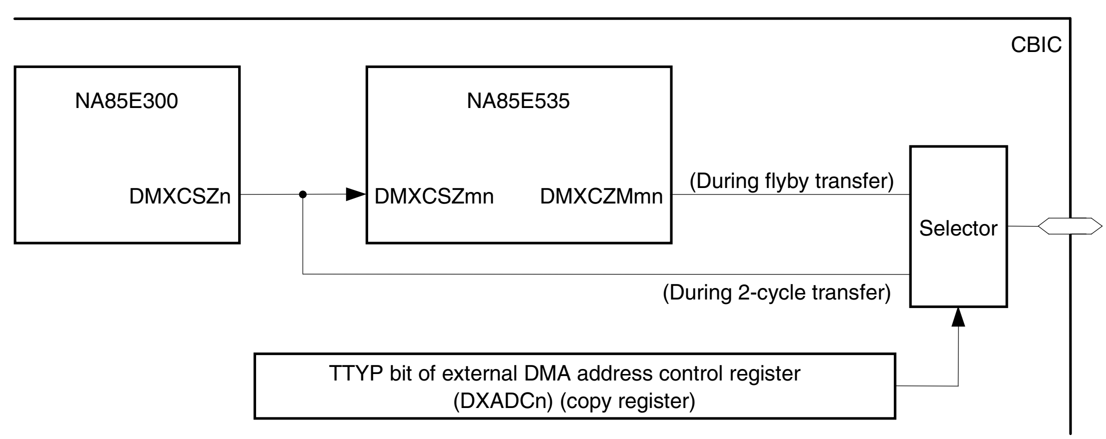
- During 2-cycle transfer: Outputs the acknowledge/chip select signal output by the DMA controller.
- During flyby transfer: Outputs the acknowledge/chip select signal output by the NA85E535.

This selector circuit must be of a configuration that it has a copy bit of the bit that sets the transfer type of each transfer channel of the DMA controller[Note] and selects the corresponding acknowledge/chip select signal.

Note Internal DMA controller of CPU core: TTYP bit of DADC0 to DADC3 registers
NA85E300: TTYP bit of DXADC0 to DXADC3 registers

An example of a circuit that selects the acknowledge/chip select signal when the NA85E300 is used is shown below.

Figure 3-33. Example of Circuit Selecting Acknowledge/Chip Select Signal (with NA85E300)



Remark n = 3 to 0, m = 1, 0

In the following cases, handling cannot be performed because the internal system clock is stopped (do not execute DMA transfer).

- While the division ratio set by the bus mode control register (BMC) is being switched
- When the PDWN bit of the BMC register is set to 1

CHAPTER 4 MEMORY ACCESS TIMING EXAMPLES

The following pages show examples of memory access timing.

★ **Table 4-1. Examples of Memory Access Timing (1/4)**

(a) Example of SRAM access timing

Figure No.		Read/Write Cycle	Access Condition	Page
4-1	a	Read cycle	–	104
	b	Write cycle	–	105
	c	Read cycle	Without wait/sequential transfer	106
	d		Without wait/with speculative read	107
	e		Without wait/single transfer/with speculative read/read access to line	108
	f		Without wait/single transfer/with speculative read/read access to another line	109
	g		Without wait/single transfer/with speculative read/write access to line	110
	h		Without wait/single transfer/with speculative read/write access to another line	111
	i		Without wait/single transfer/with speculative read/write access to NA85E535 register	112
	j		Without wait/eight sequential transfers from speculative read hit address/local bus size: 32 bits	113
	k	Write cycle	Without wait/sequential transfer	114
	l		Data wait = 1/sequential transfer	115
	m		Without wait/non-sequential transfer	116
	n		Data wait = 1/non-sequential transfer	117
	o		Without wait/sequential transfer/local bus size: 16 bits	118

★ **Table 4-1. Examples of Memory Access Timing (2/4)**

(b) Example of SDRAM access timing

Figure No.		Read/Write Cycle	Access Condition	Page
4-2	a	Read cycle	CL = 2/BCW = 2/single transfer	119
	b		Without wait/CL = 2/sequential transfer/without page and bank change	120
	c	Write cycle	CL = 2/BCW = 2/single transfer/with page and bank change	121
	d		Without wait/sequential transfer/without page and bank change	122
	e		Without wait/sequential transfer/with bank change	123
	f		Without wait/non-sequential transfer/without page and bank change	124
	g	Write cycle → read cycle	CL = 2/BCW = 2/single transfer	125
	h	Read cycle → write cycle	Without wait/CL = 2/single transfer/without page and bank change/with speculative read	126
	i	Read cycle	Without wait/CL = 2/non-sequential transfer/without page and bank change/without speculative read/local bus size: 16 bits	127
	j		Without wait/CL = 2/non-sequential transfer/without page and bank change/with speculative read/local bus size: 8 bits	128
	k		Without wait/CL = 3/sequential transfer/without page and bank change/without speculative read/local bus size: 16 bits	129
	l		Without wait/CL = 3/sequential transfer/without page and bank change/without speculative read/local bus size: 8 bits	130
	m		Without wait/CL = 2/16 sequential transfers from speculative read hit address/local bus size: 32 bits	131
	n	Write cycle	Without wait/sequential transfer/without page and bank change/local bus size: 8 bits	132

(c) Example of page ROM access timing

Figure No.		Access Condition	Page
4-3	a	Without speculative read/non-sequential transfer	133
	b	Without speculative read/sequential transfer	134
	c	With speculative read/non-sequential transfer	135
	d	With speculative read/sequential transfer	136
	e	With speculative read/off-page wait = 1/without on-page wait/local bus size: 32 bits (1)	137
	f	With speculative read/off-page wait = 1/without on-page wait/local bus size: 32 bits (2)	138

★

Table 4-1. Examples of Memory Access Timing (3/4)

(d) Example of DMA transfer timing (1/2)

Figure No.		Transfer Type	DMAC	Transfer Direction	Transfer Condition	Page
4-4	a	Flyby transfer[Note 1]	DMAC with on-chip CPU core	SRAM → external I/O	Single transfer	139
	b				Single transfer/transfer request during speculative read	140
	c				Single transfer/division by 2 (1)	141
	d				Single transfer/division by 2 (2)	142
4-5	a			External I/O → SRAM	Single transfer	143
	b				Single transfer/flyby transfer request during write	144
4-6				Page ROM → external I/O	Single transfer	145
4-7				SDRAM → external I/O	Single transfer	146
4-8				External I/O → SDRAM	Single transfer	147
4-9	a		NA85E300	SRAM → external I/O	Single transfer	148
	b				Single transfer (4 words)	149
4-10	a			External I/O → SRAM	Single transfer	150
	b				Single transfer (4 words)	151
4-11				Page ROM → external I/O	Single transfer (4 words)	152
4-12				SDRAM → external I/O	Single transfer (4 words)	153
4-13				External I/O → SDRAM	Single transfer (4 words)	154
4-14	a	2-cycle transfer[Note 2]	DMAC with on-chip CPU core	SRAM → SRAM	Single transfer/without wait/without speculative read	155
	b				Block transfer/with speculative read	156
	c				Block transfer/without speculative read	157
	d				Line transfer/with speculative read	158
	e				Line transfer/without speculative read	159
4-15	a			SDRAM → SDRAM	Single transfer/without wait/CL = 2/ without speculative read	160
	b				Block transfer/with speculative read	161
	c				Block transfer/without speculative read	162
	d				Line transfer/with speculative read	163
	e				Line transfer/without speculative read	164
4-16				SRAM → NPB	Single transfer/with speculative read	165
4-17				NPB → SRAM	Single transfer	166
4-18				NPB → NPB	Single transfer/during speculative read	167

Notes 1. The same cycle is generated in the VSB and local bus regardless of whether speculative read is set.

2. Local bus size: 32 bits

★ **Table 4-1. Examples of Memory Access Timing (4/4)**

(d) Example of DMA transfer timing (2/2)

Figure No.		Transfer Type	DMAC	Transfer Direction	Transfer Condition	Page
4-19		2-cycle transfer[Note 1]	DMAC with on-chip CPU core	NPB → RAM	Single transfer/during speculative read	168
4-20	a		NA85E300	SRAM → SRAM	Single transfer/without wait/without speculative read	169
	b				Block transfer/with speculative read	170
	c				Block transfer/without speculative read	171
	d				Single transfer (4 words)/with speculative read	172
	e				Single transfer (4 words)/without speculative read	173
4-21	a			SDRAM → SDRAM	Single transfer/without wait/CL = 2/without speculative read	174
	b				Block transfer/with speculative read	175
	c				Block transfer/without speculative read	176
	d				Single transfer (4 words)/with speculative read[Note 2]	177
	e				Single transfer (4 words)/without speculative read[Note 2]	178

Notes 1. Local bus size: 32 bits

2. The timing is the same regardless of whether speculative read is set.

(e) Other

Figure No.	Title	Page
4-22	SDRAM CBR refresh timing	179
4-23	SDRAM self-refresh timing (STOP timing)	180
4-24	MobileRAM deep power down timing (STOP timing)	181
4-25	SDRAM mode register write operation timing	182
4-26	MobileRAM expansion mode register write operation timing	183
4-27	BMC register change timing (setting of division by 1 → division by 2)	184
4-28	SRAM write access timing example (if division ratio of BUSCLK for VBCLK signal is 1/2)	185

Each timing chart consists of the following states.

- T0 state: VSB start state from CPU core
- T1 and T2 states: Basic states
- TA state: Address setting wait state
- TW state: Wait state
- TACT state: State of bank active command
- TBCW state: Wait state inserted if BCW = 2 or 3
- TREAD state: State of read command
- TLATE state: Wait state of latency
- TPREC state: State of bank precharge command
- TWR state: State indicating write command
- WPRE state: Precharge state after write command
- WEND state: State indicating end of write cycle
- TF state: State during DMA flyby transfer between SDRAM and external I/O
- TRPW state: State inserted while NA85E535 waits for cycle generation

Remarks 1. : Undetermined status (output), or any level (input)
2. O: Sampling timing
3. For details of the VSB signals, refer to **NU85E Hardware User's Manual (A14874E)**.
4. The shaded part in the VSB figure is the same shading of the memory cycle of the corresponding VSB cycle.

The transfer response is changed by the VSWAIT, VSAHLD, and VSLAST signals as shown in Table 4-2.

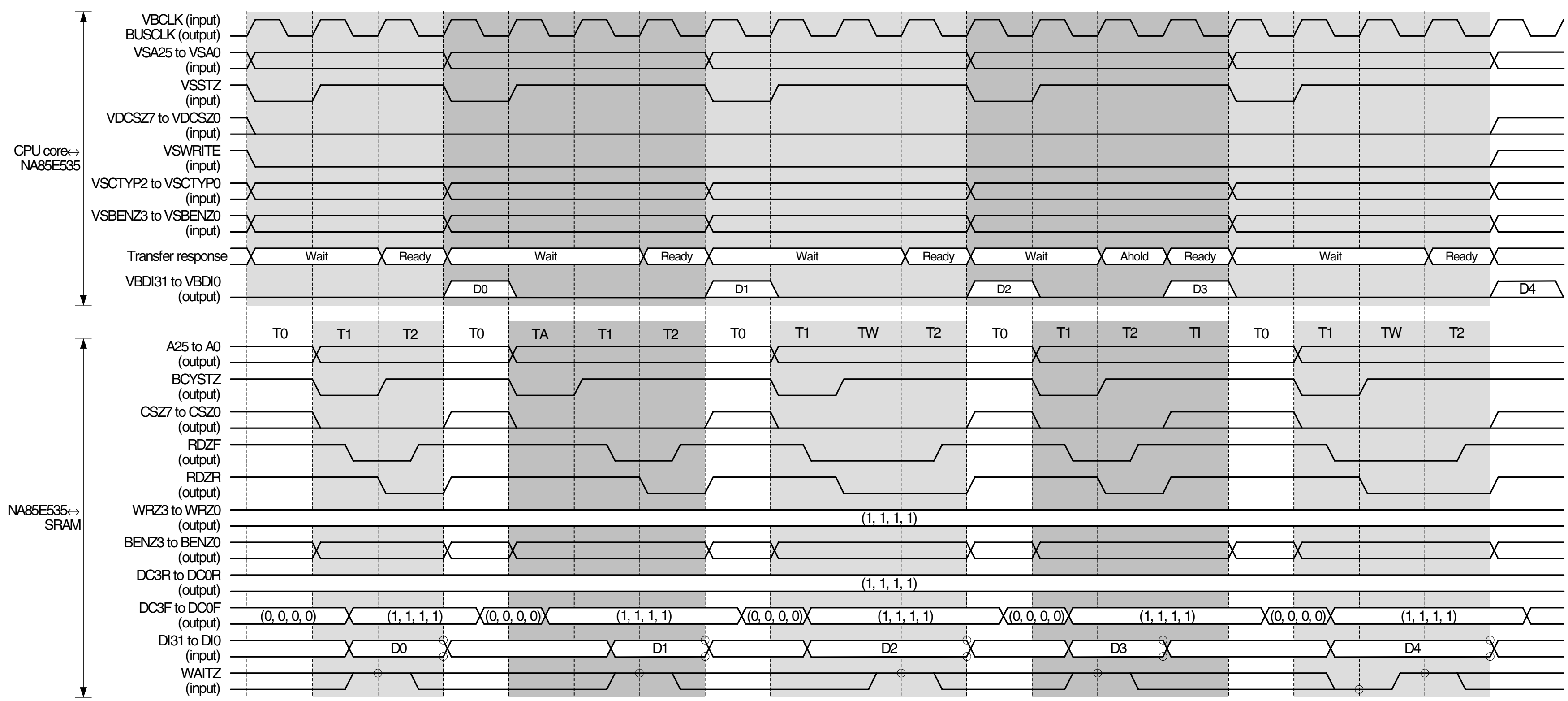
Table 4-2. Transfer Response

VSWAIT	VSAHLD	VSLAST	Transfer Response
0	0	0	Ready (ready response: Current transfer is completed)
1	0	0	Wait (wait response)
1	1	0	Ahold (Address hold response: Holds address and control signal)

Remarks 1. 0: Low level, 1: High level
2. The NA85E535 does not have Last (last response).
3. If a cache or external bus master is not connected to the CPU core, the VSB data bus size is fixed to 32 bits. As a result, sequential transfer does not take place.

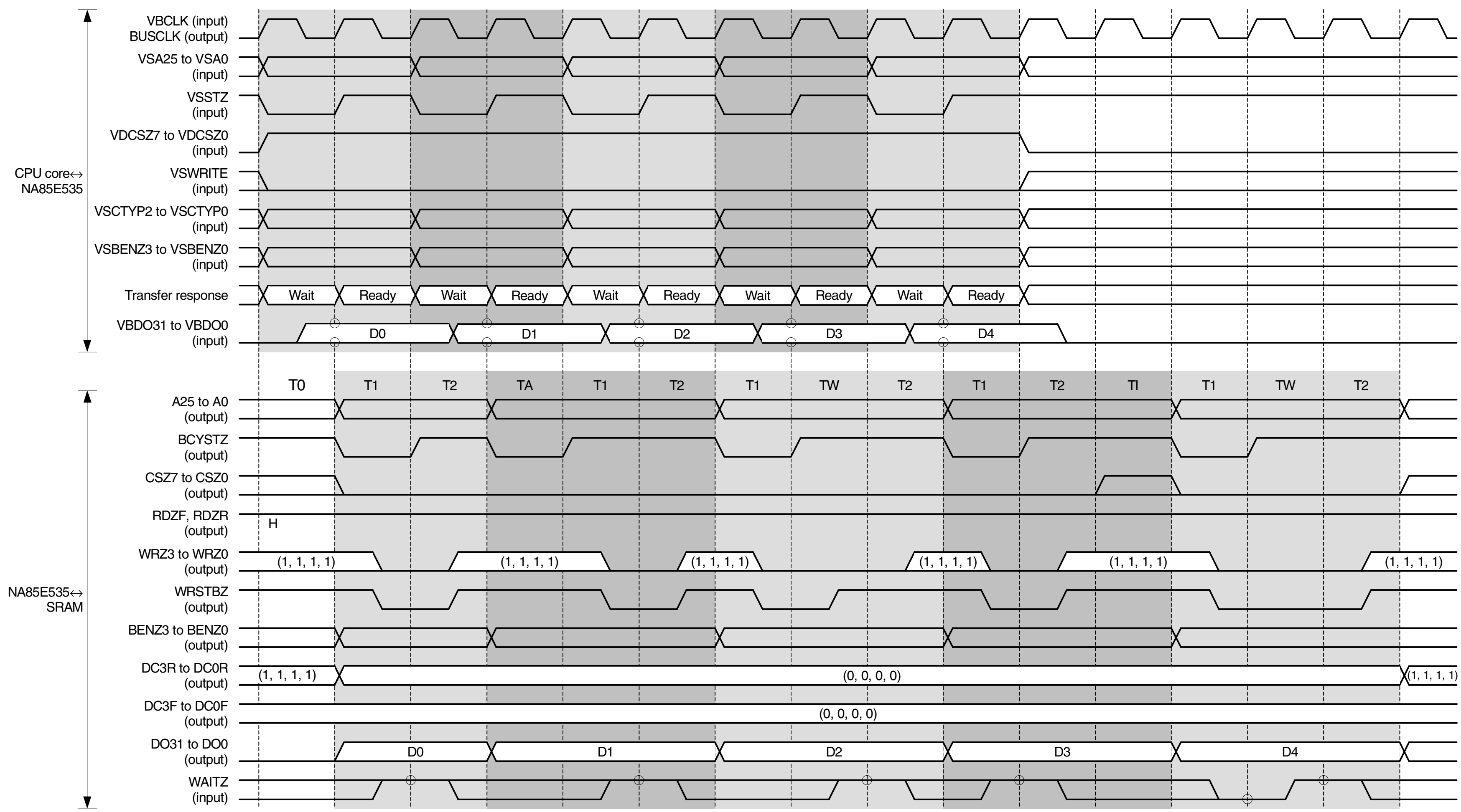
★Figure 4-1. Example of SRAM Access Timing (1/15)

(a) Read cycle



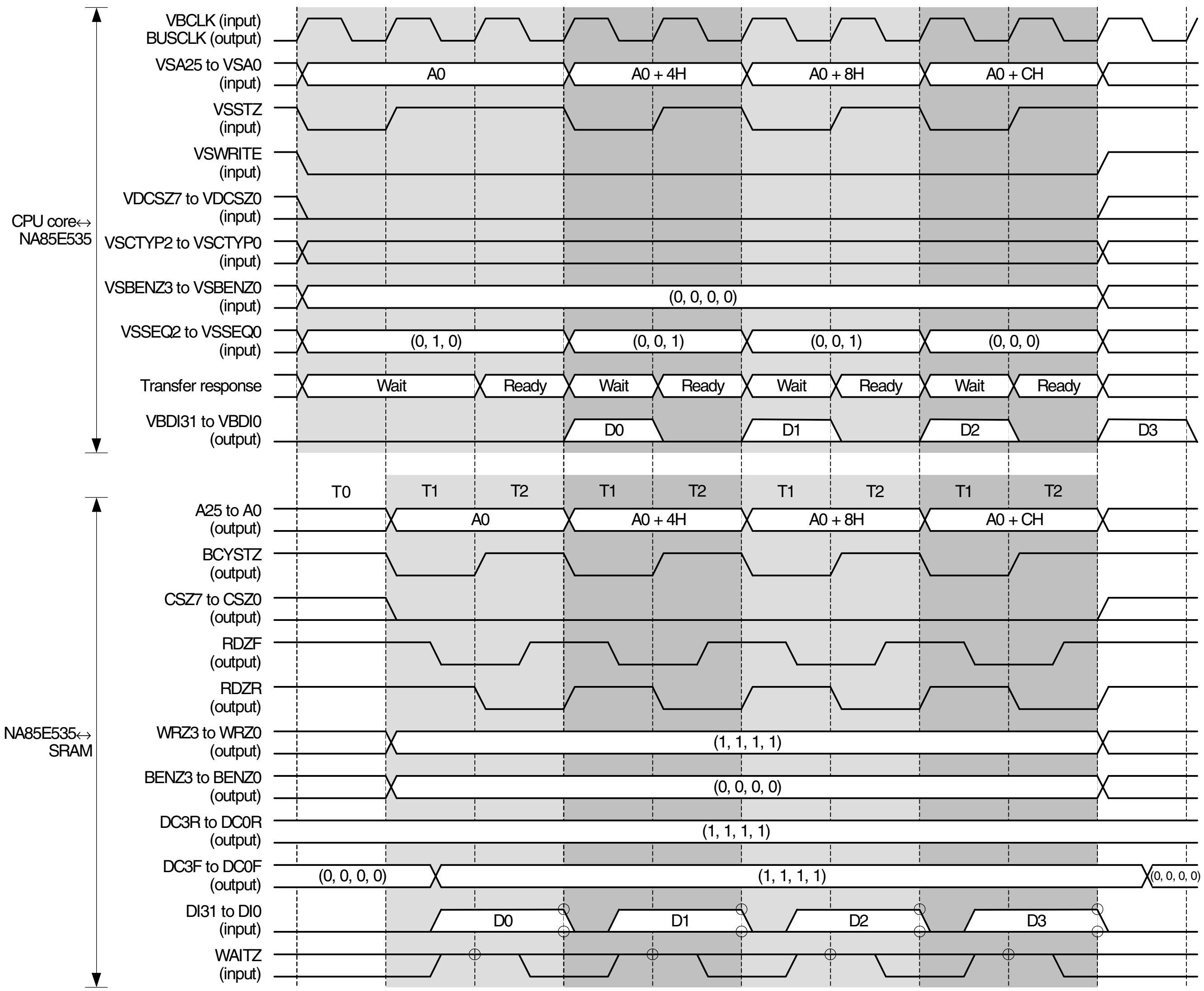
★Figure 4-1. Example of SRAM Access Timing (2/15)

(b) Write cycle



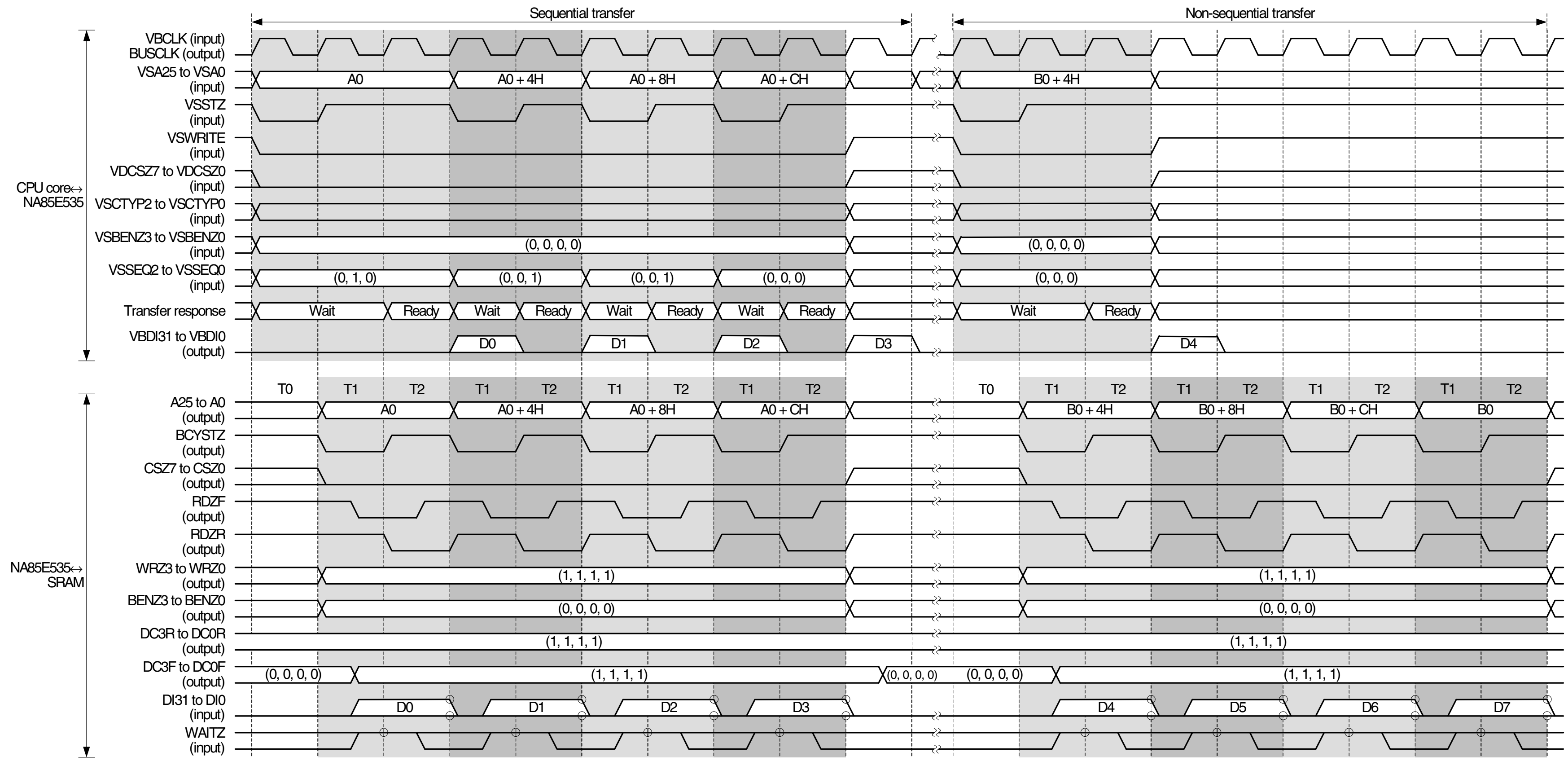
★Figure 4-1. Example of SRAM Access Timing (3/15)

(c) Read cycle/without wait/sequential transfer



★Figure 4-1. Example of SRAM Access Timing (4/15)

(d) Read cycle/without wait/with speculative read



★Figure 4-1. Example of SRAM Access Timing (5/15)

(e) Read cycle/without wait/single transfer/with speculative read/read access to line

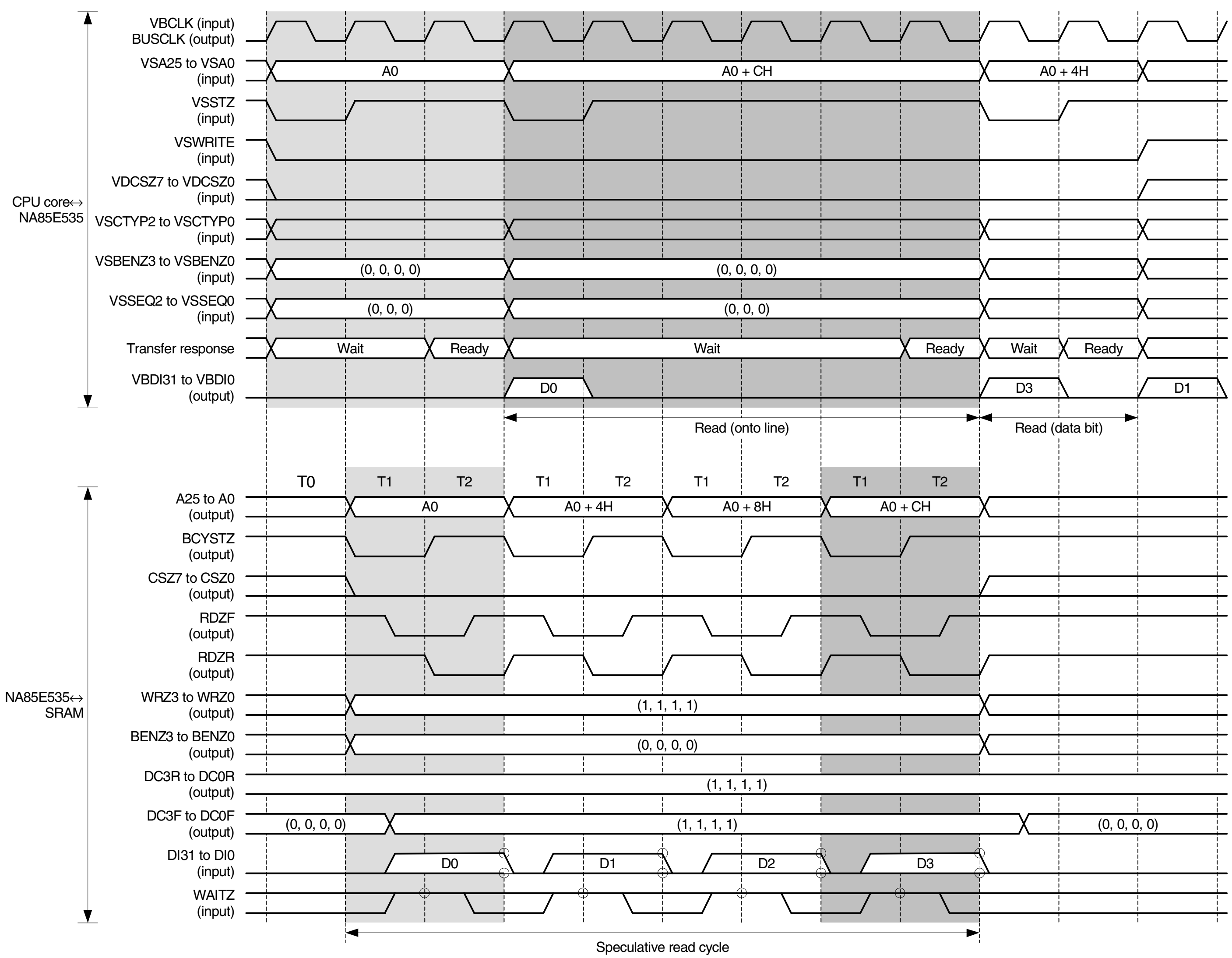
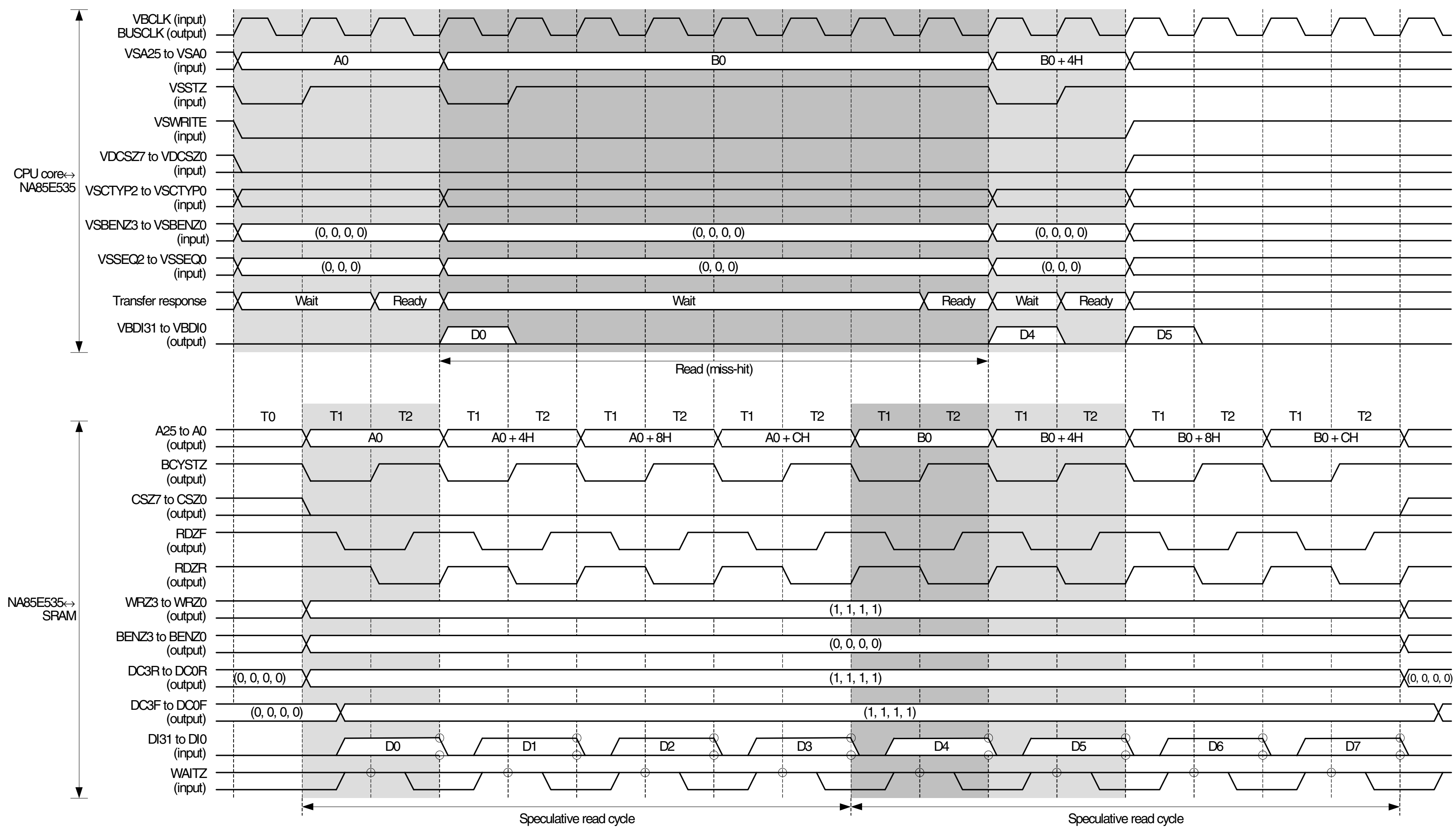


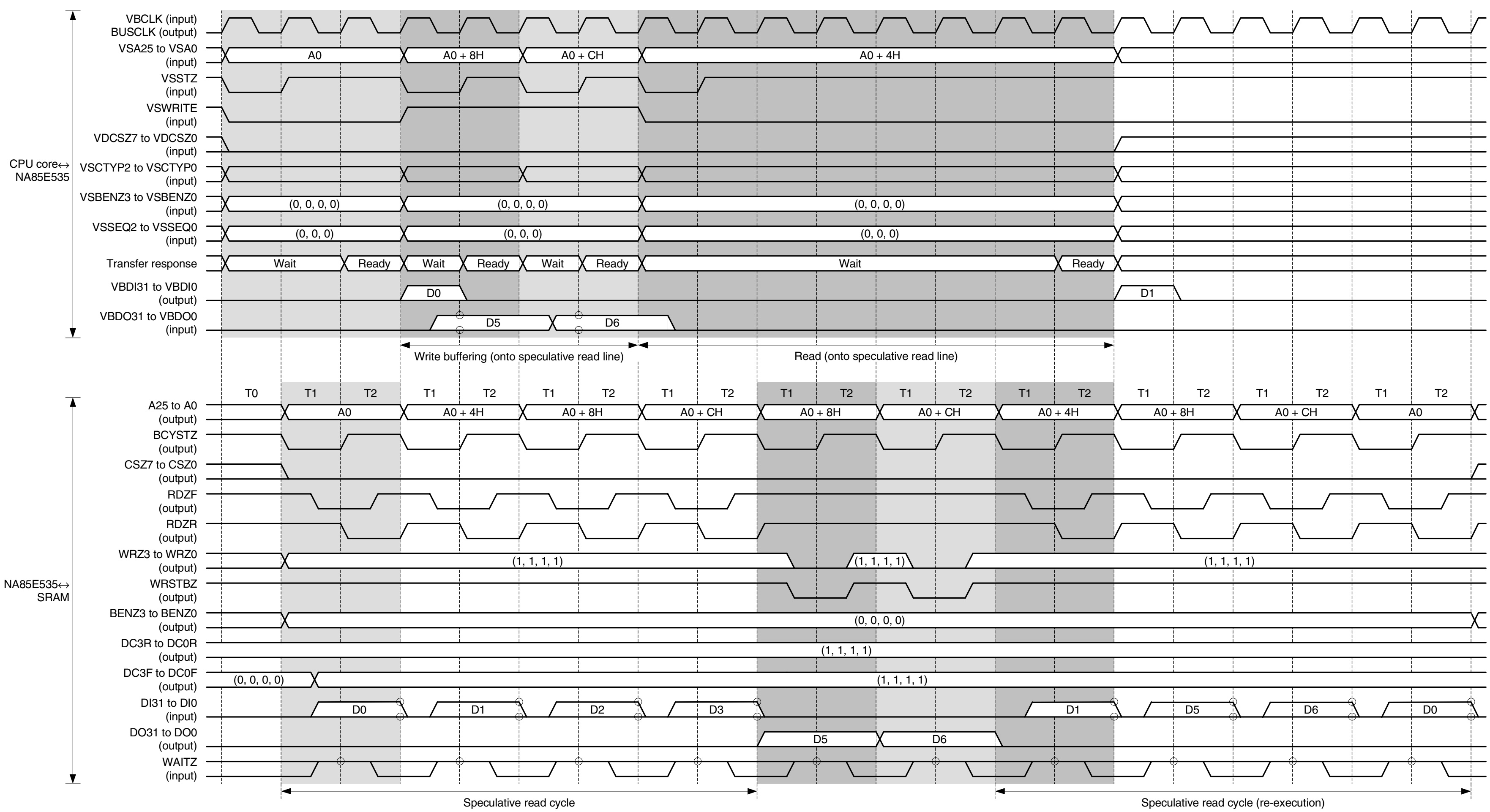
Figure 4-1. Example of SRAM Access Timing (6/15)

(f) Read cycle/without wait/single transfer/with speculative read/read access to another line



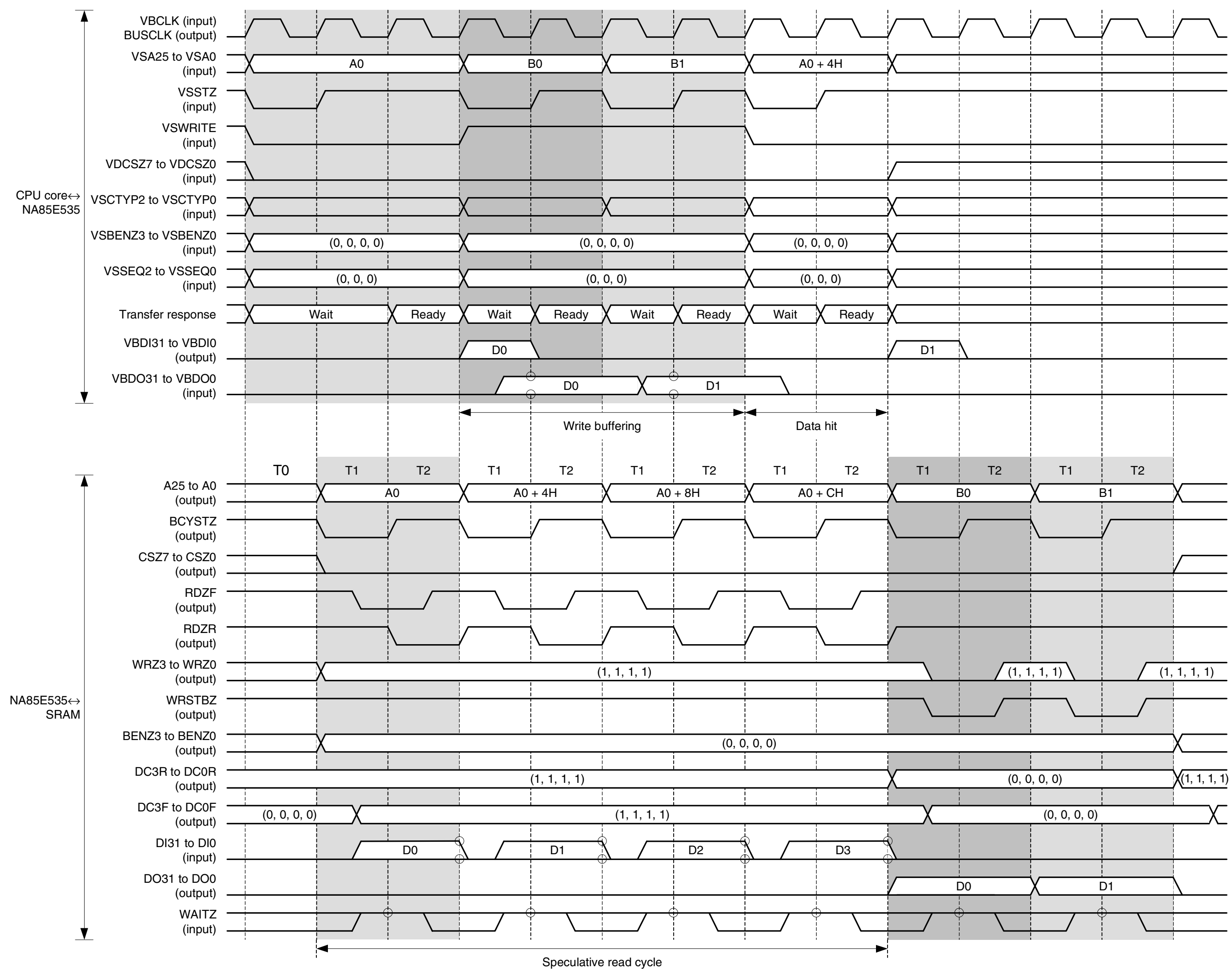
★Figure 4-1. Example of SRAM Access Timing (7/15)

(g) Read cycle/without wait/single transfer/with speculative read/write access to line



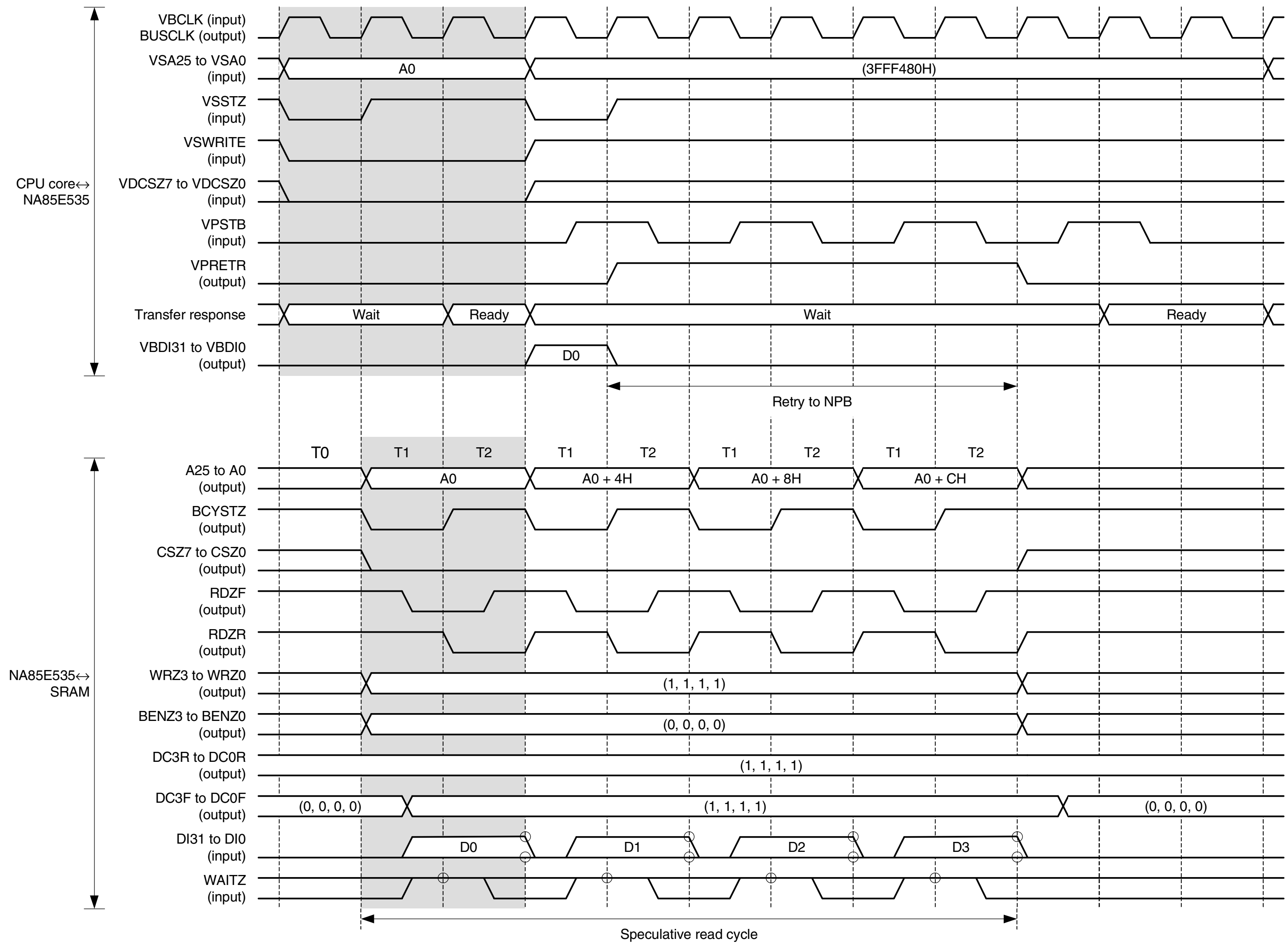
★Figure 4-1. Example of SRAM Access Timing (8/15)

(h) Read cycle/without wait/single transfer/with speculative read/write access to another line



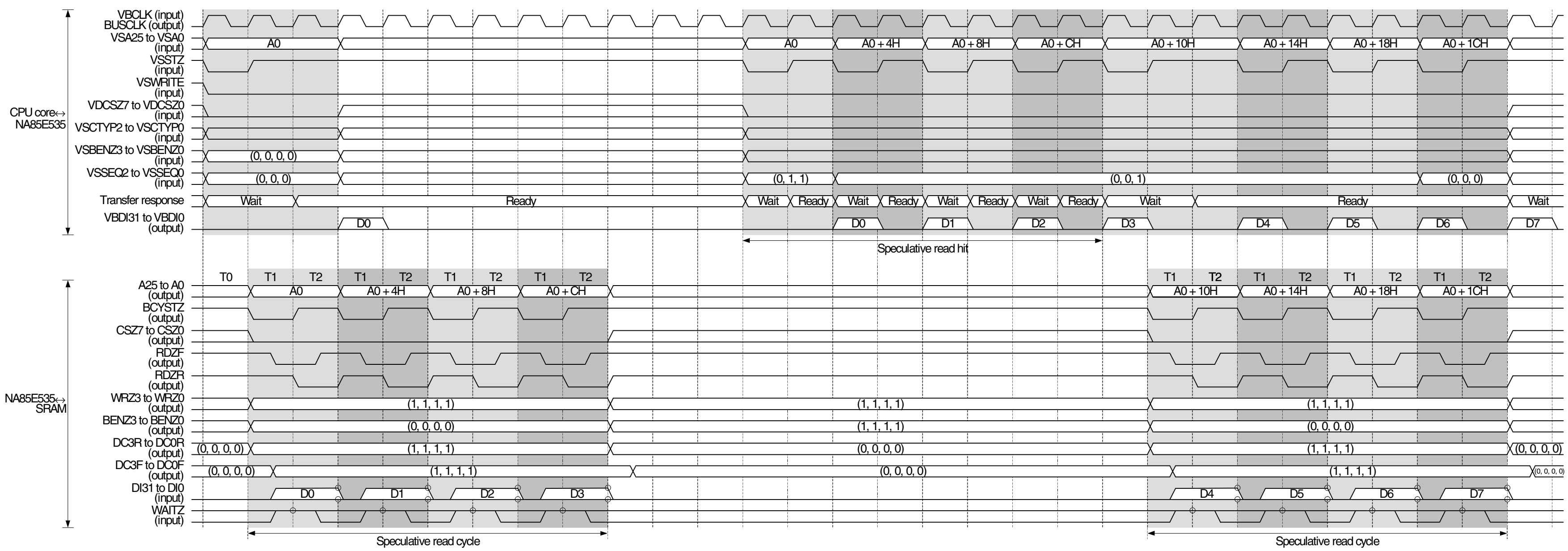
★Figure 4-1. Example of SRAM Access Timing (9/15)

(i) Read cycle/without wait/single transfer/with speculative read/write access to NA85E535 register



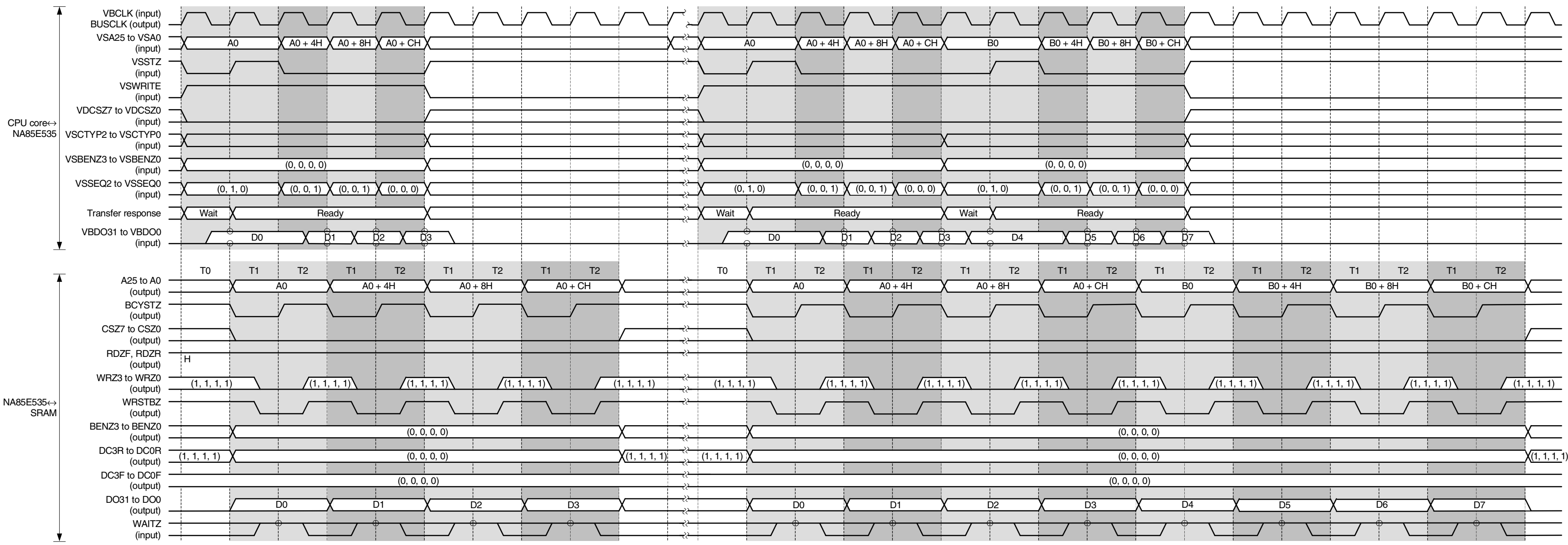
★Figure 4-1. Example of SRAM Access Timing (10/15)

(j) Read cycle/without wait/8 times of sequential transfer from speculative read hit address/local bus size: 32 bits



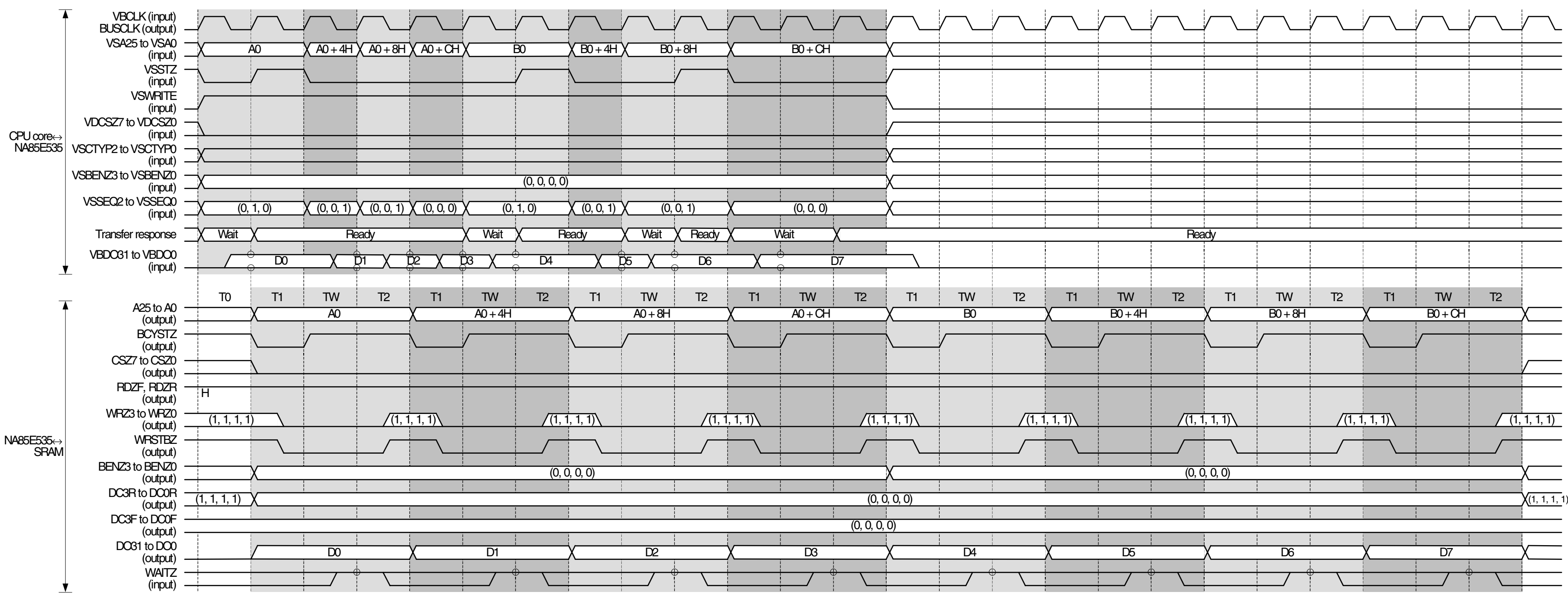
★Figure 4-1. Example of SRAM Access Timing (11/15)

(k) Write cycle/without wait/sequential transfer



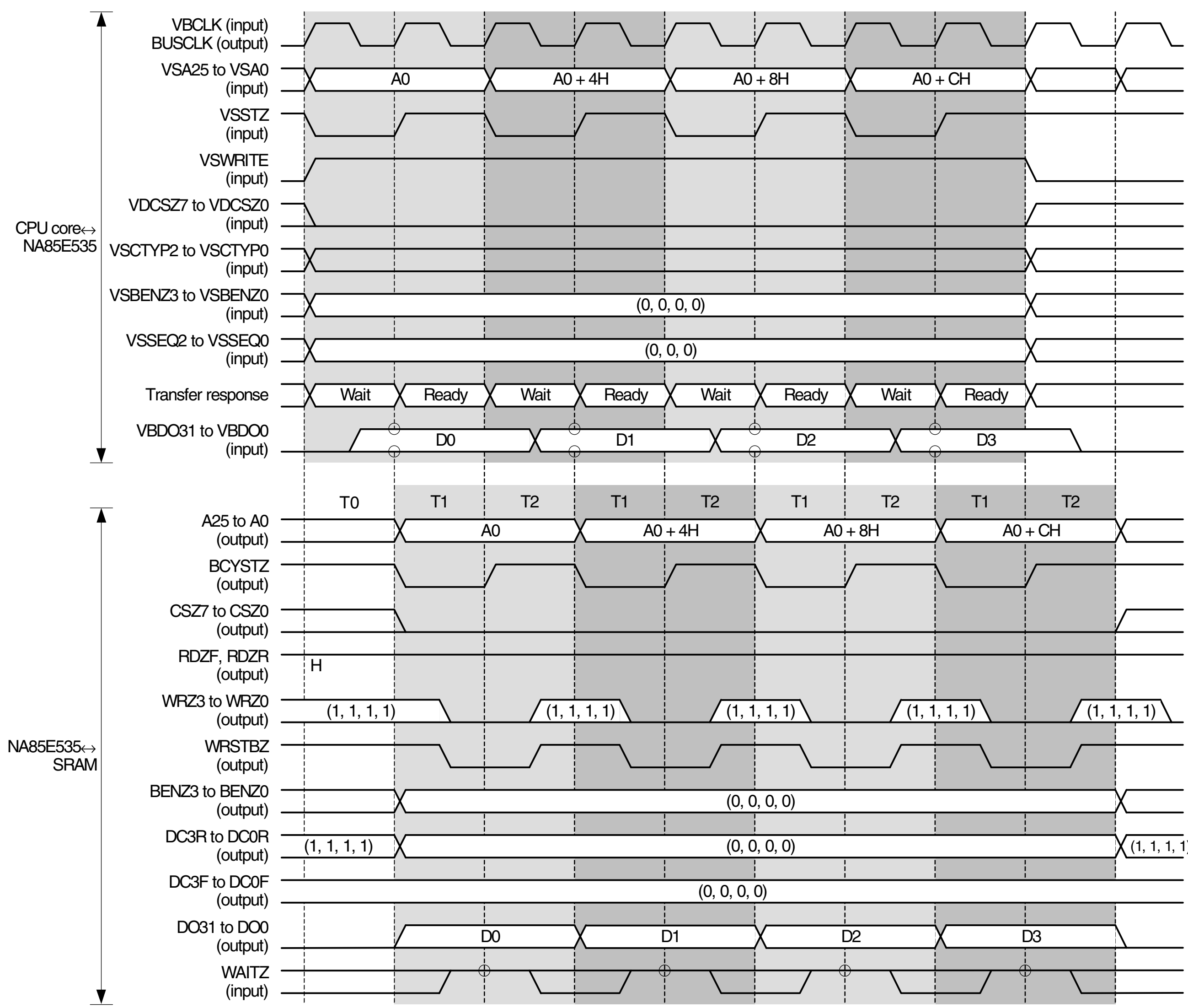
★Figure 4-1. Example of SRAM Access Timing (12/15)

(l) Write cycle/data wait = 1/sequential transfer



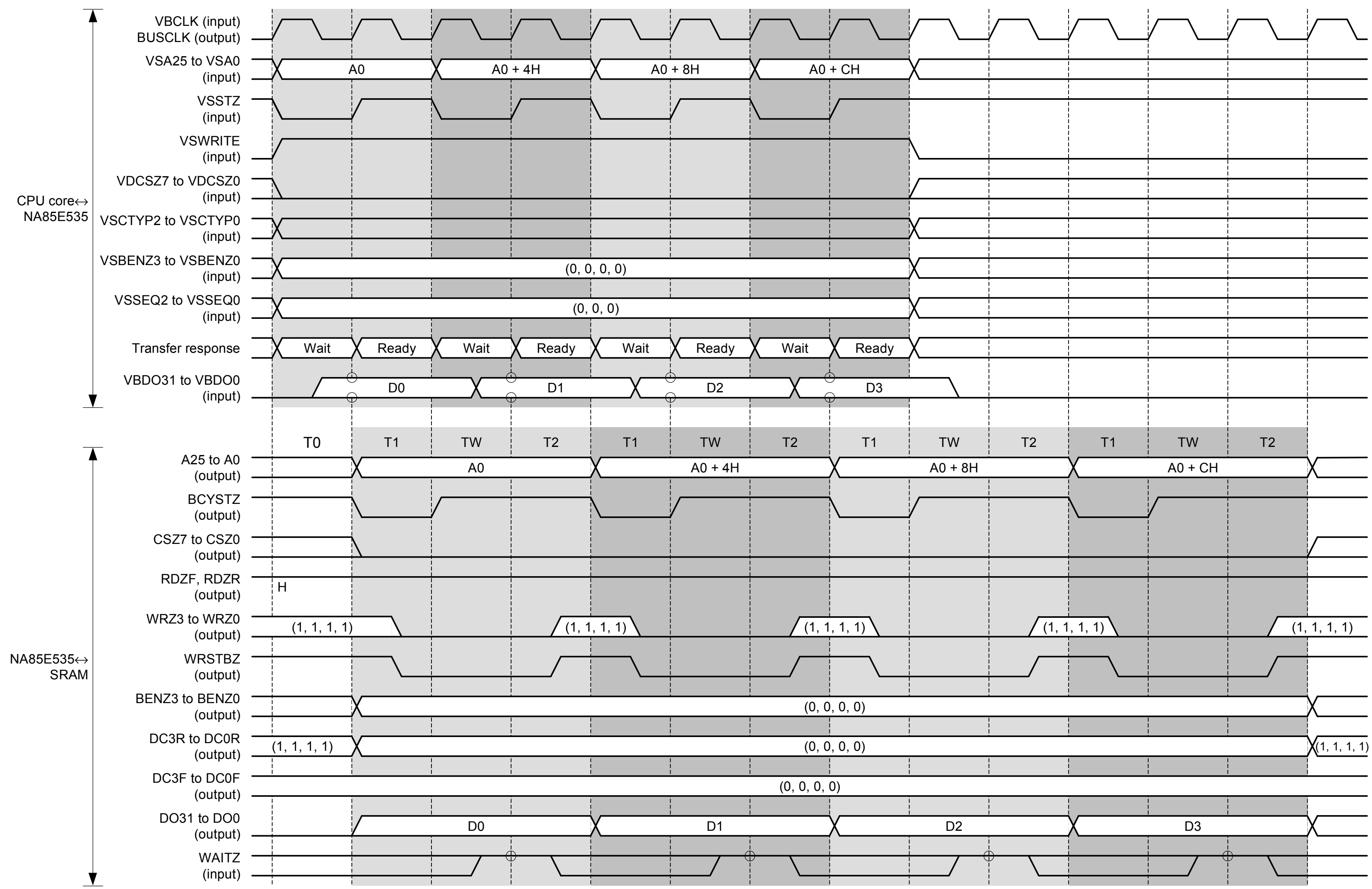
★Figure 4-1. Example of SRAM Access Timing (13/15)

(m) Write cycle/without wait/non-sequential transfer



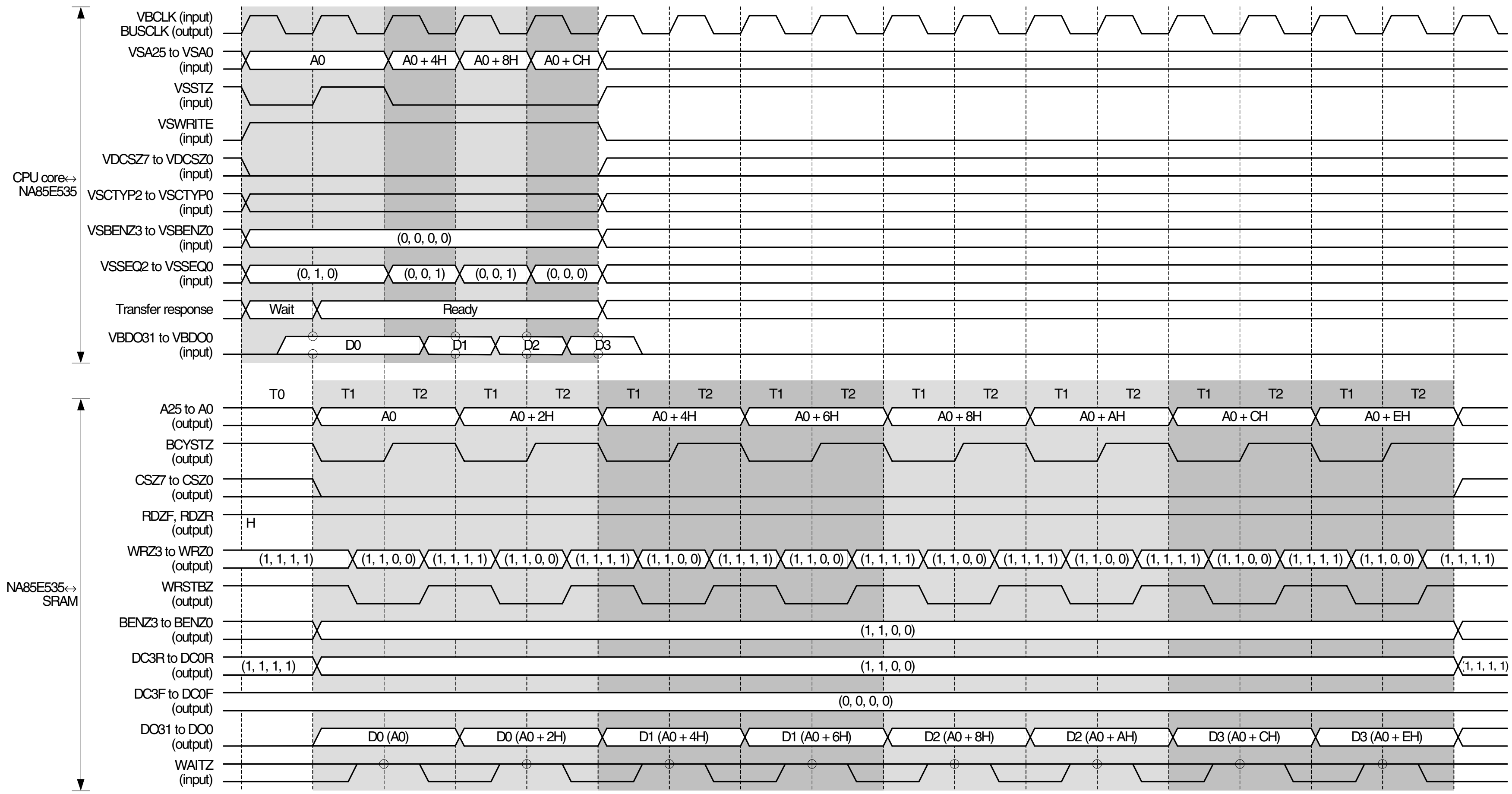
★Figure 4-1. Example of SRAM Access Timing (14/15)

(n) Write cycle/data wait = 1/non-sequential transfer



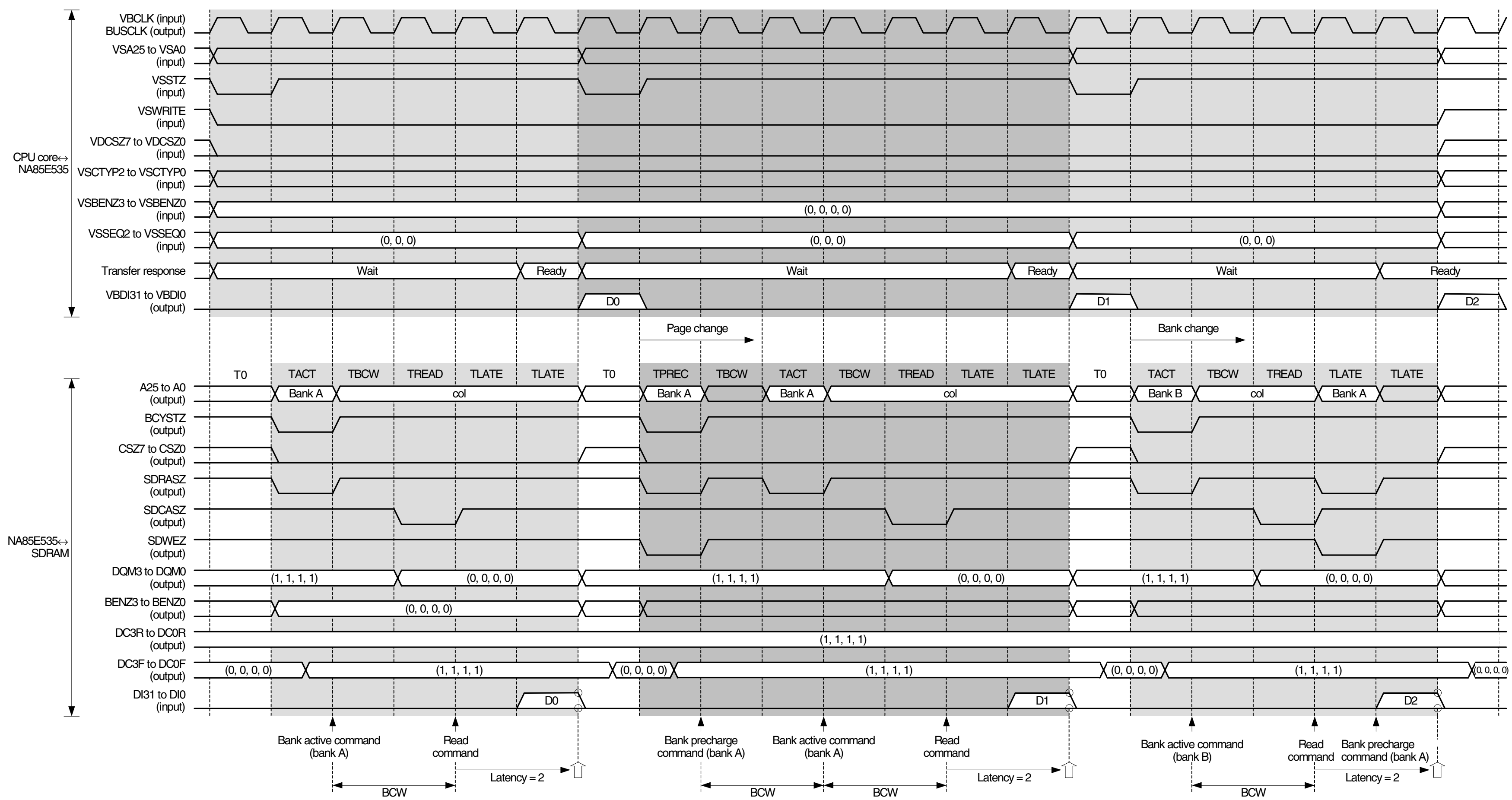
★Figure 4-1. Example of SRAM Access Timing (15/15)

(o) Write cycle/without wait/sequential transfer/local bus size: 16 bits



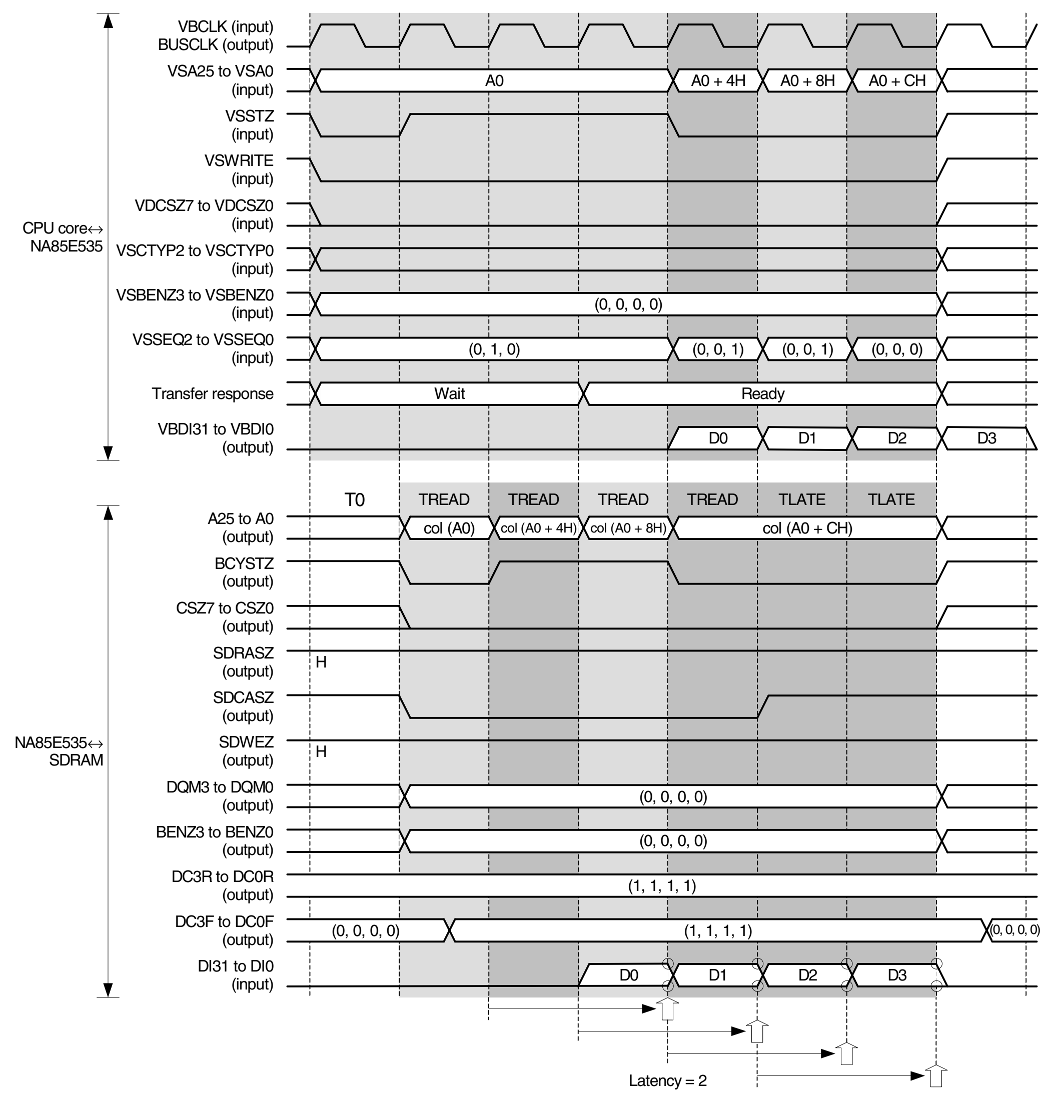
★ **Figure 4-2. Example of SDRAM Access Timing (1/14)**

(a) Read cycle/CL = 2/BCW = 2/single transfer



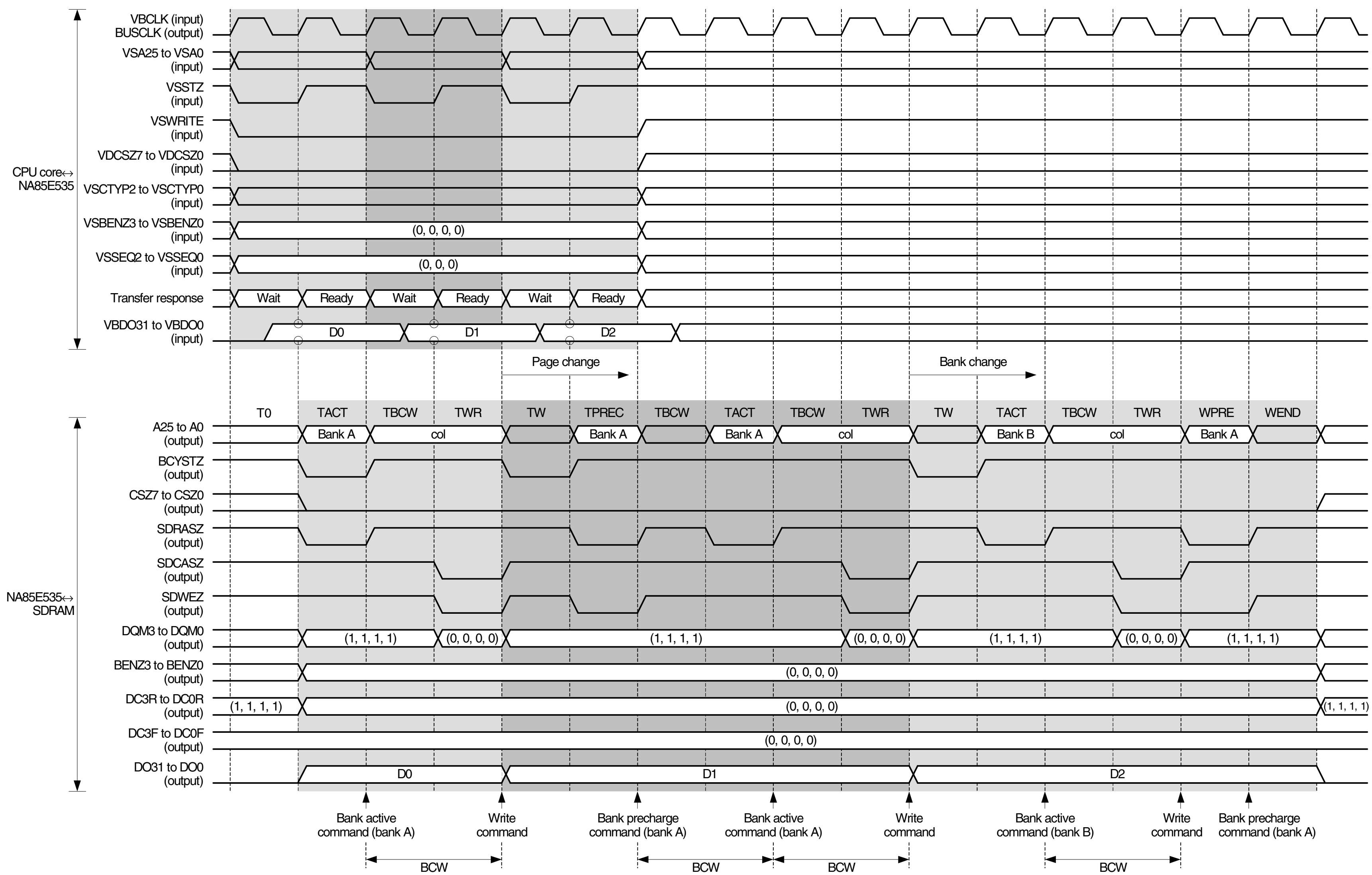
★Figure 4-2. Example of SDRAM Access Timing (2/14)

(b) Read cycle/without wait/CL = 2/sequential transfer/without page and bank change



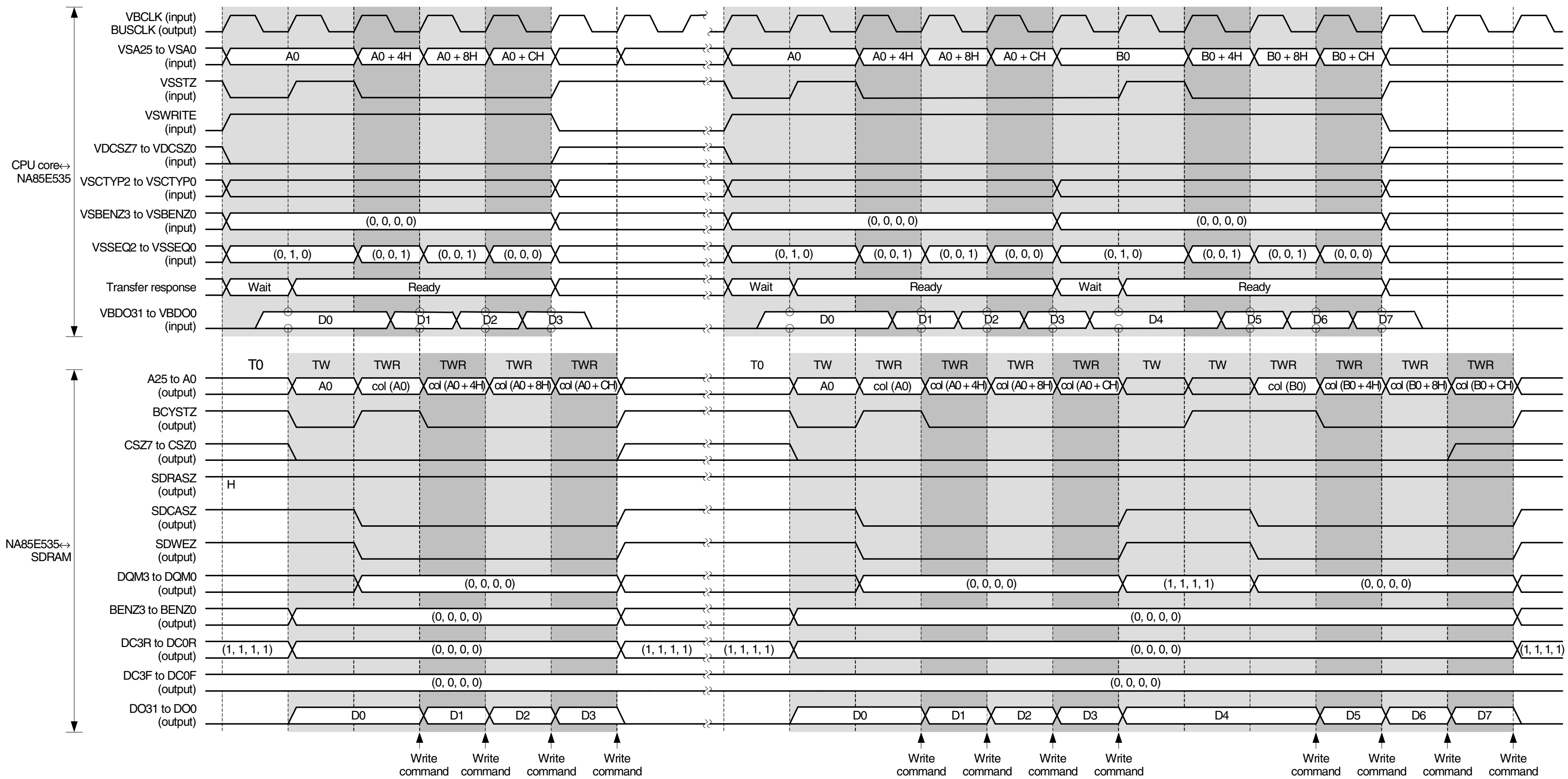
★Figure 4-2. Example of SDRAM Access Timing (3/14)

(c) Write cycle/CL = 2/BCW = 2/single transfer/with page and bank change



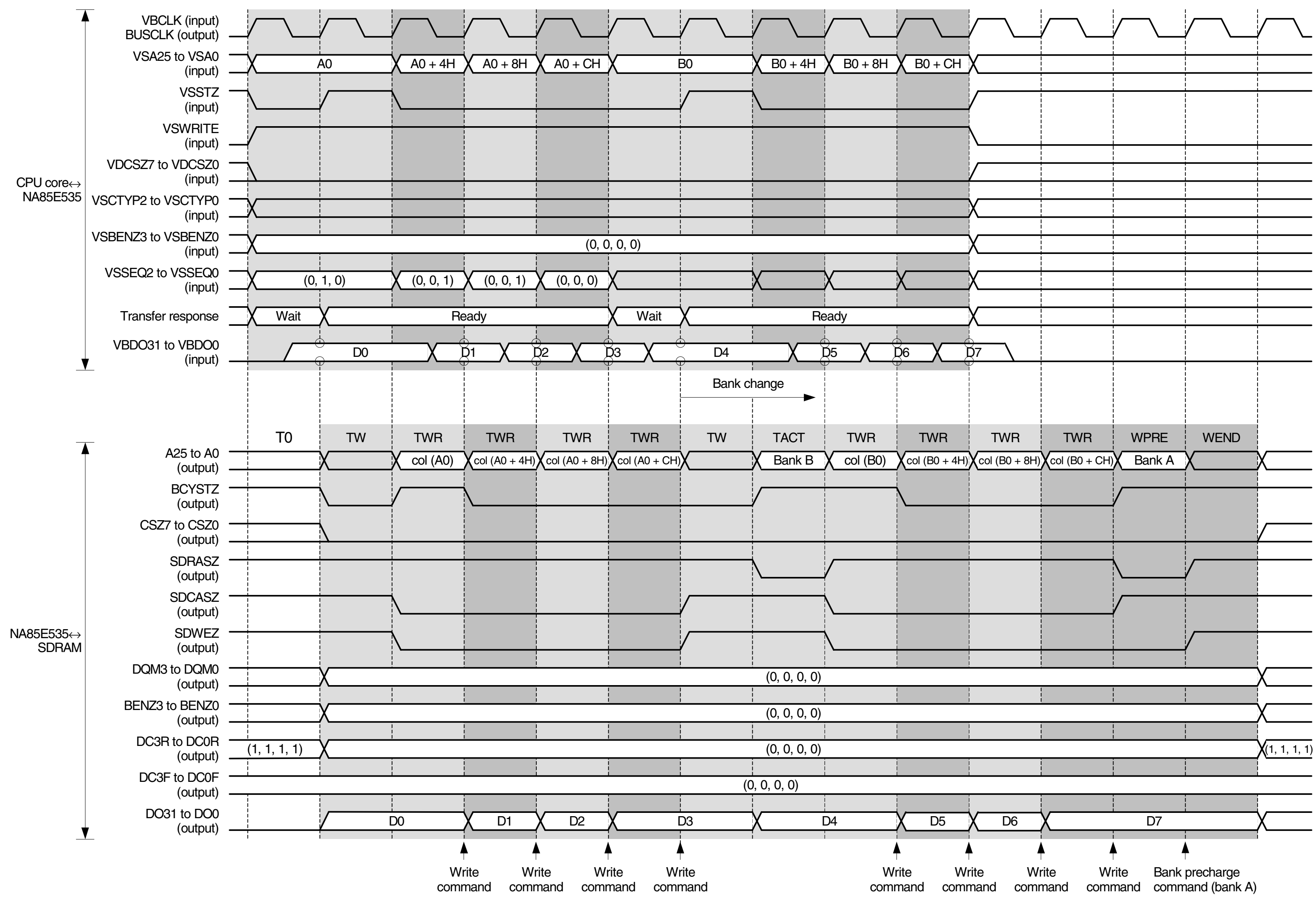
★Figure 4-2. Example of SDRAM Access Timing (4/14)

(d) Write cycle/without wait/sequential transfer/without page and bank change



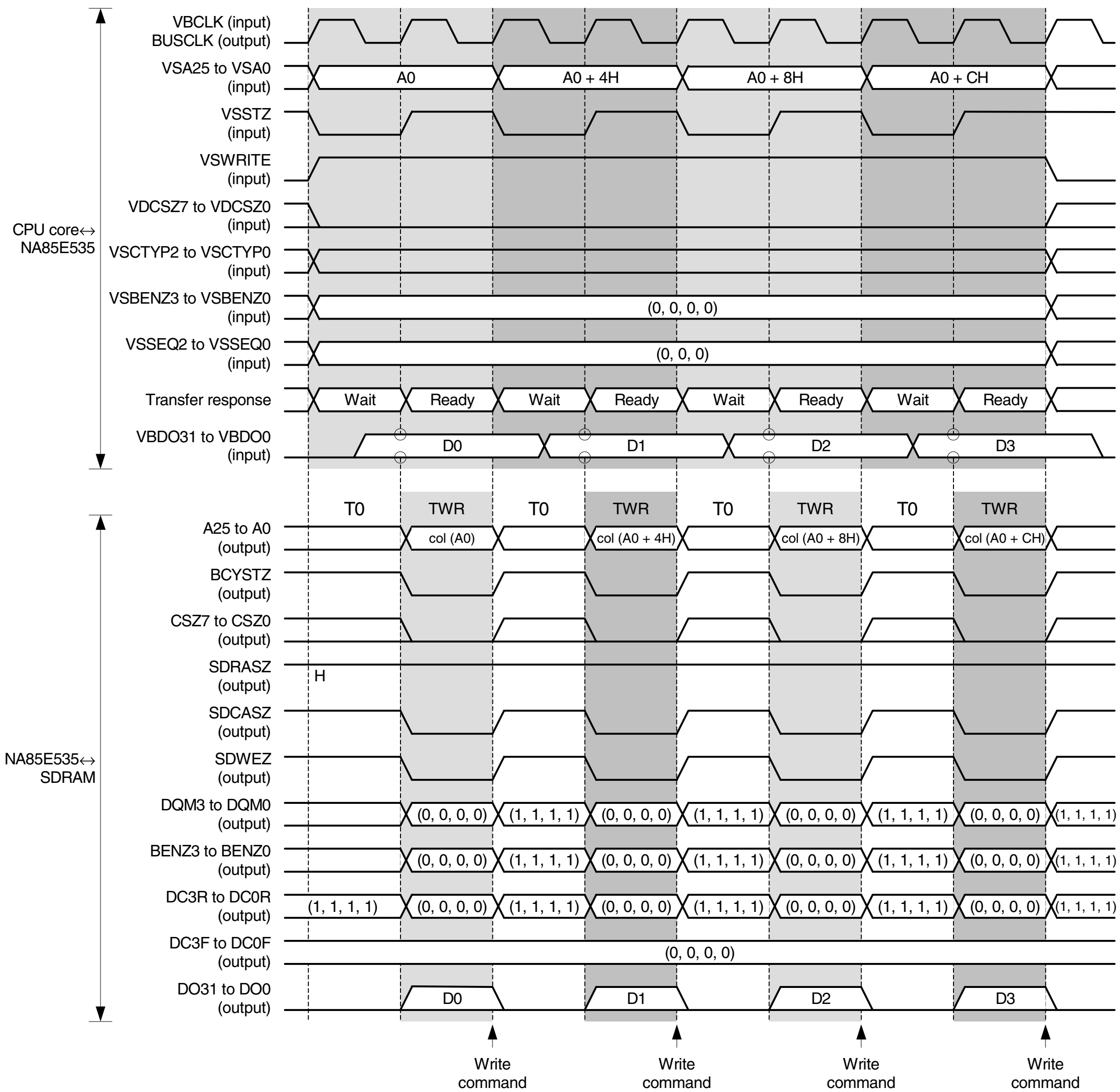
★Figure 4-2. Example of SDRAM Access Timing (5/14)

(e) Write cycle/without wait/sequential transfer/with bank change



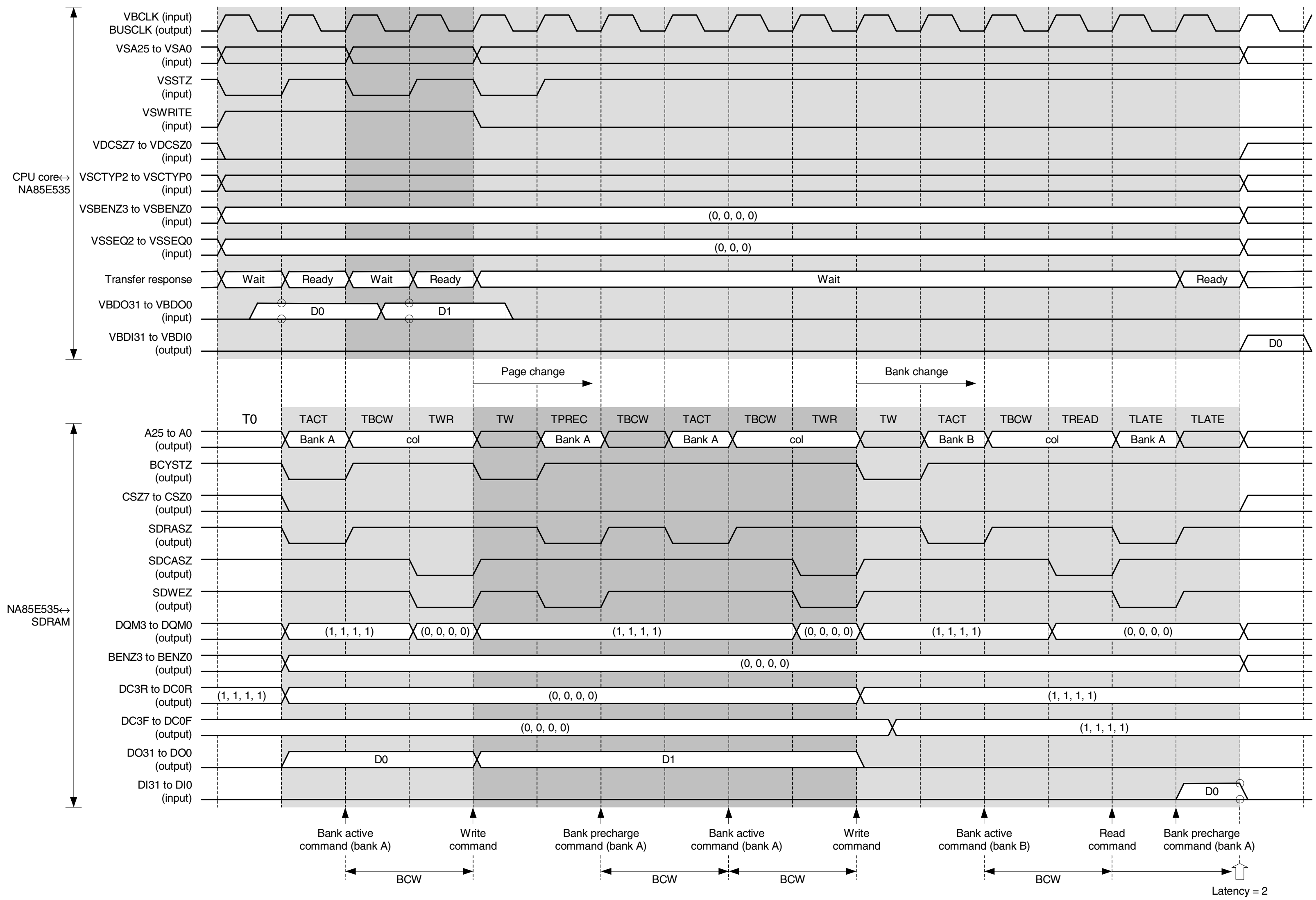
★**Figure 4-2. Example of SDRAM Access Timing (6/14)**

(f) Write cycle/without wait/non-sequential transfer/without page and bank change



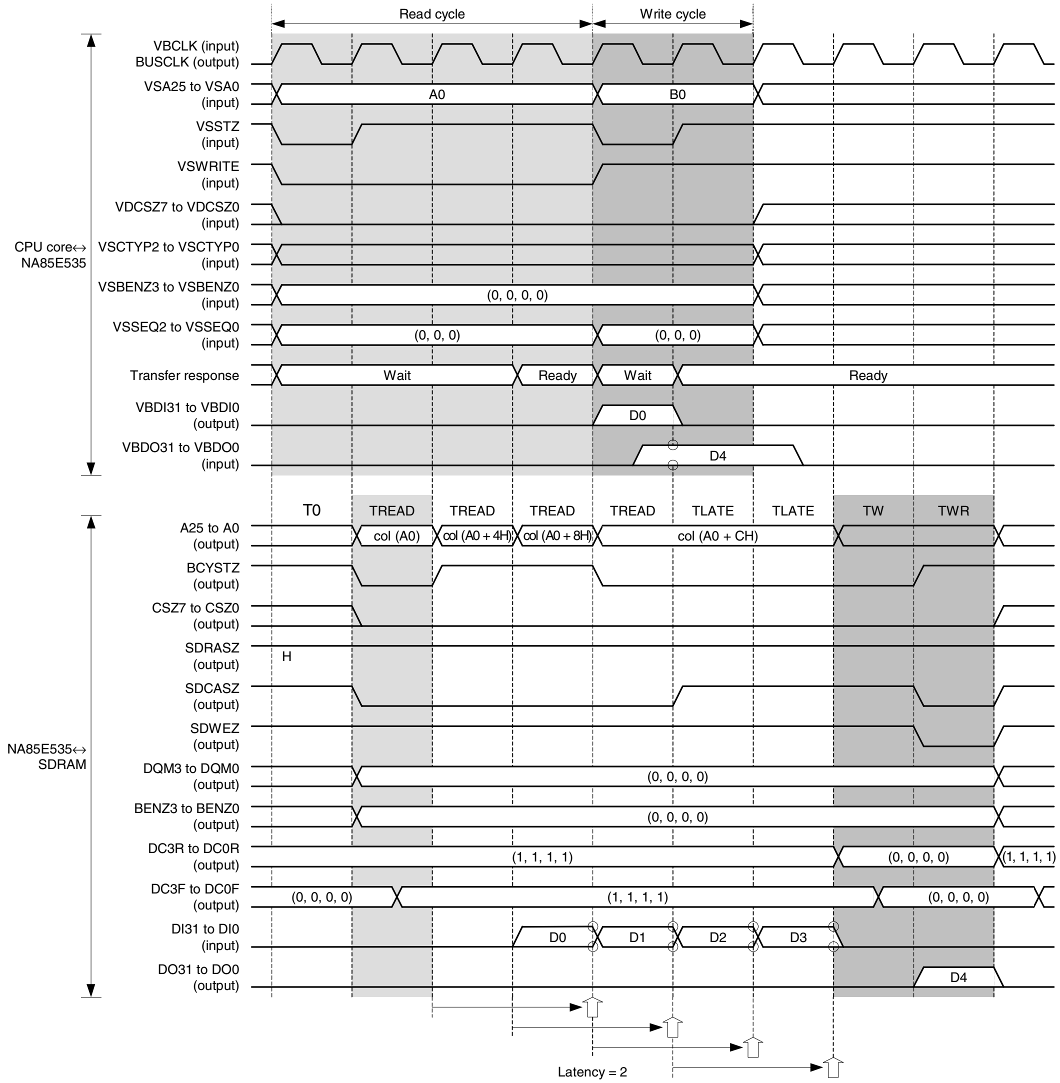
★Figure 4-2. Example of SDRAM Access Timing (7/14)

(g) Write cycle → read cycle/CL = 2/BCW = 2/single transfer



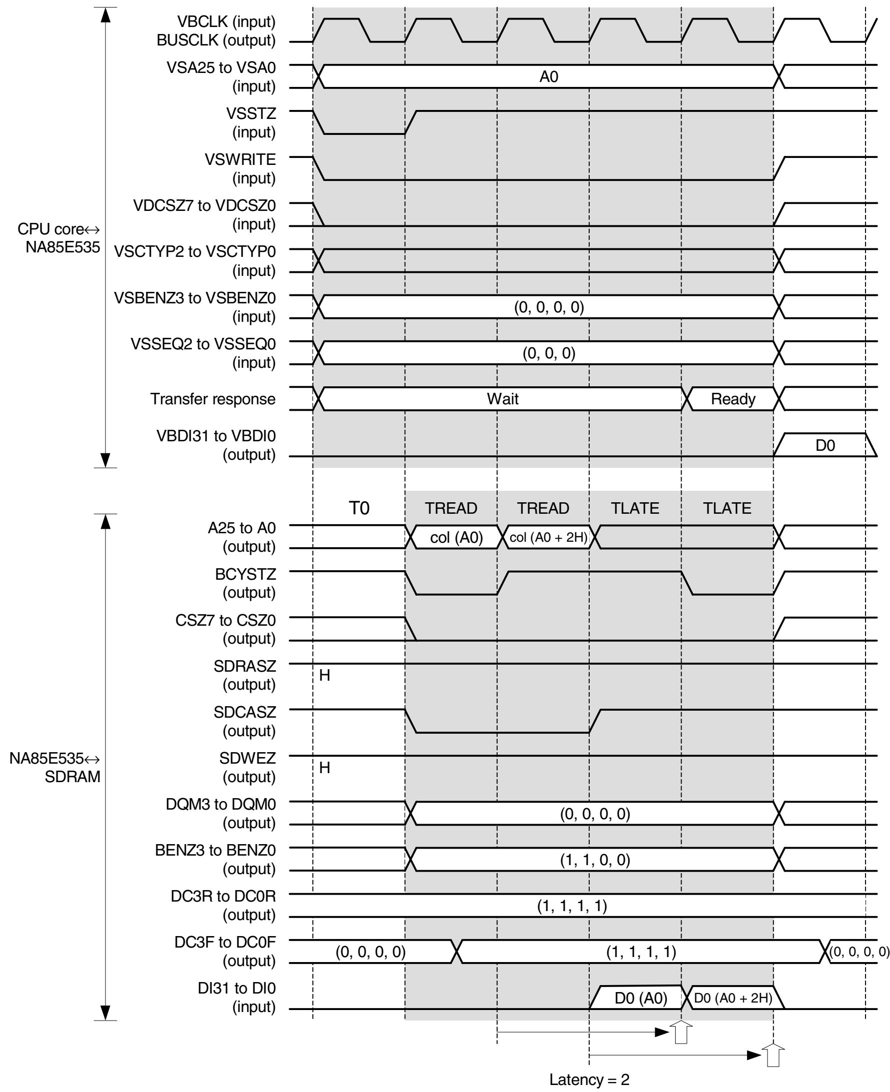
★Figure 4-2. Example of SDRAM Access Timing (8/14)

(h) Read cycle → write cycle/without wait/CL = 2/single transfer/without page and bank change/with speculative read



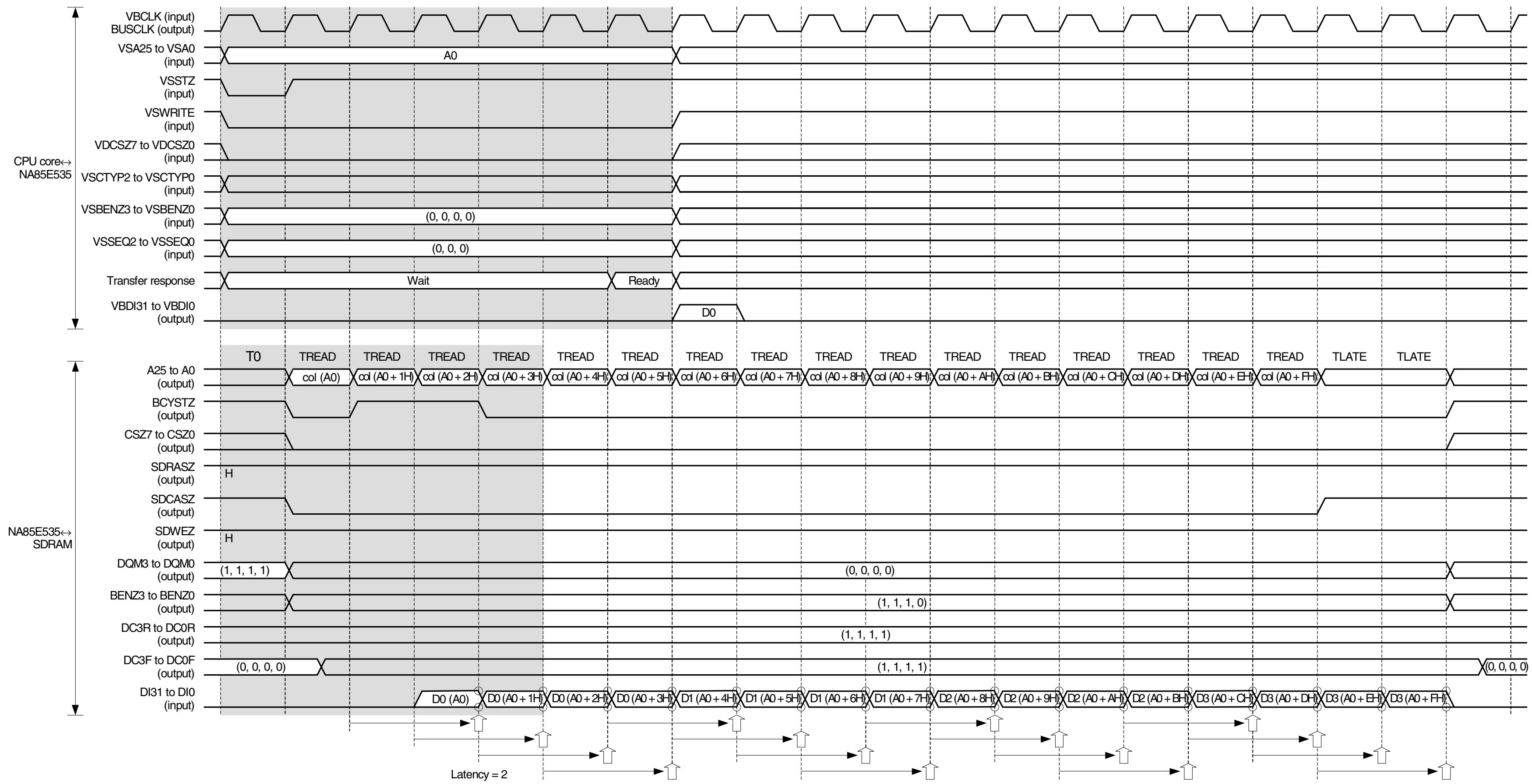
★Figure 4-2. Example of SDRAM Access Timing (9/14)

(i) Read cycle/without wait/CL = 2/non-sequential transfer/without page and bank change/without speculative read/local bus size: 16 bits



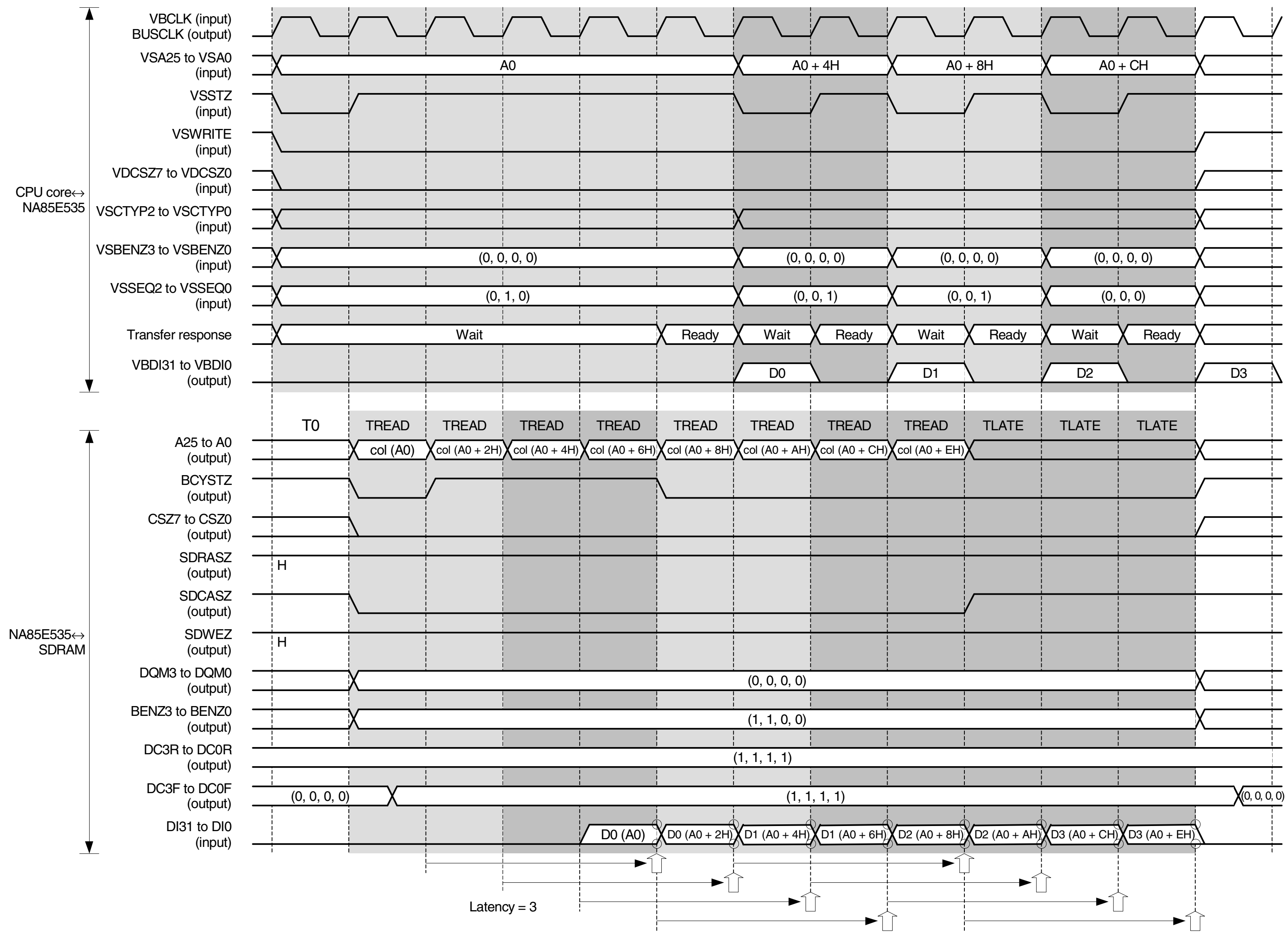
★Figure 4-2. Example of SDRAM Access Timing (10/14)

(j) Read cycle/without wait/CL = 2/non-sequential transfer/without page and bank change/with speculative read/local bus size: 8 bits



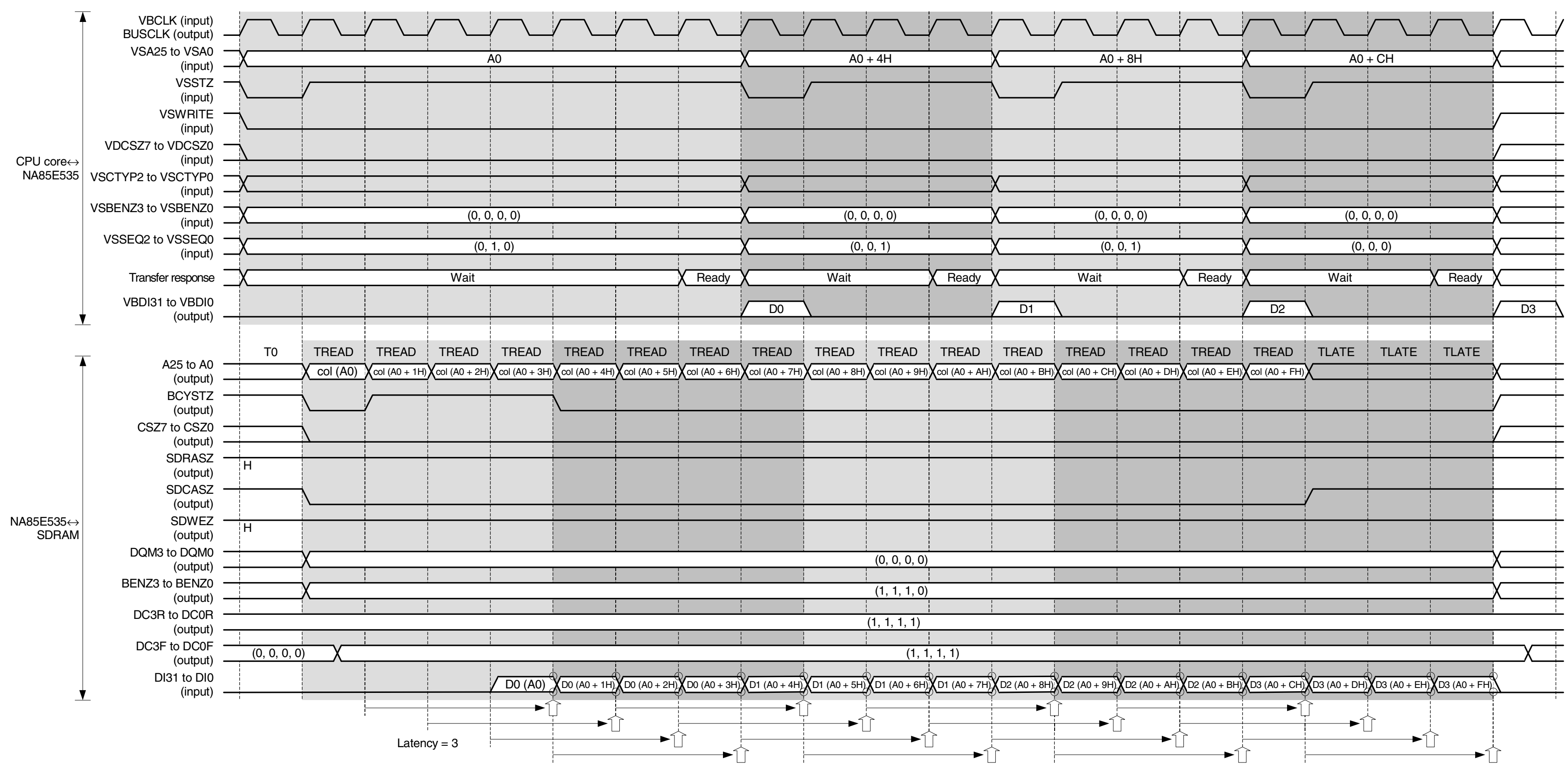
★Figure 4-2. Example of SDRAM Access Timing (11/14)

(k) Read cycle/without wait/CL = 3/sequential transfer/without page and bank change/without speculative read/local bus size: 16 bits



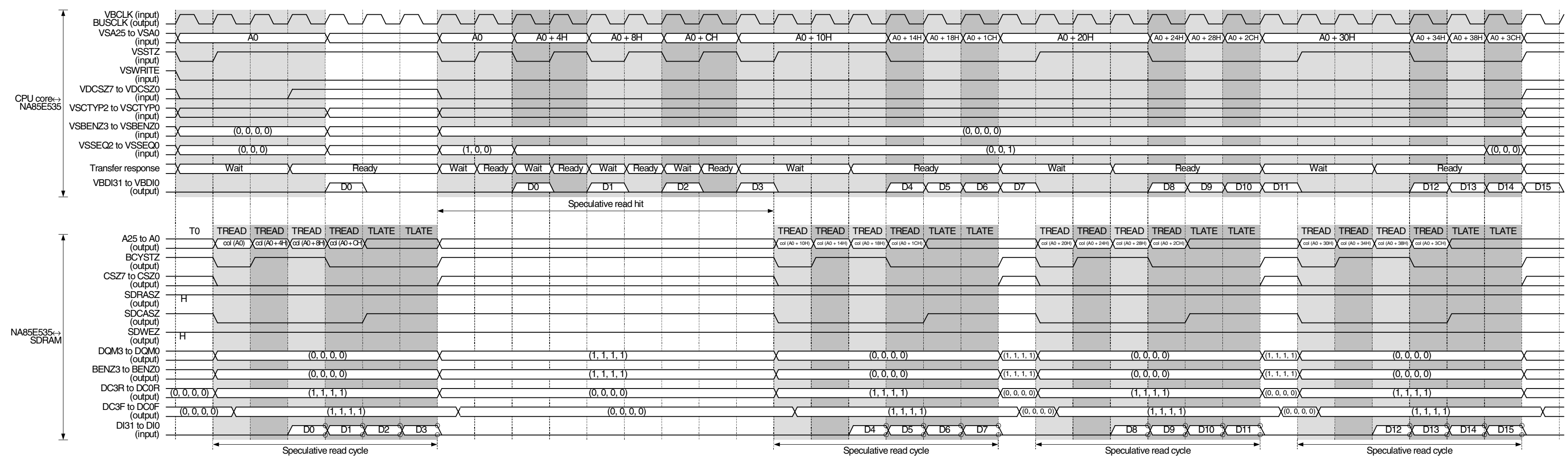
★Figure 4-2. Example of SDRAM Access Timing (12/14)

(l) Read cycle/without wait/CL = 3/sequential transfer/without page and bank change/without speculative read/local bus size: 8 bits



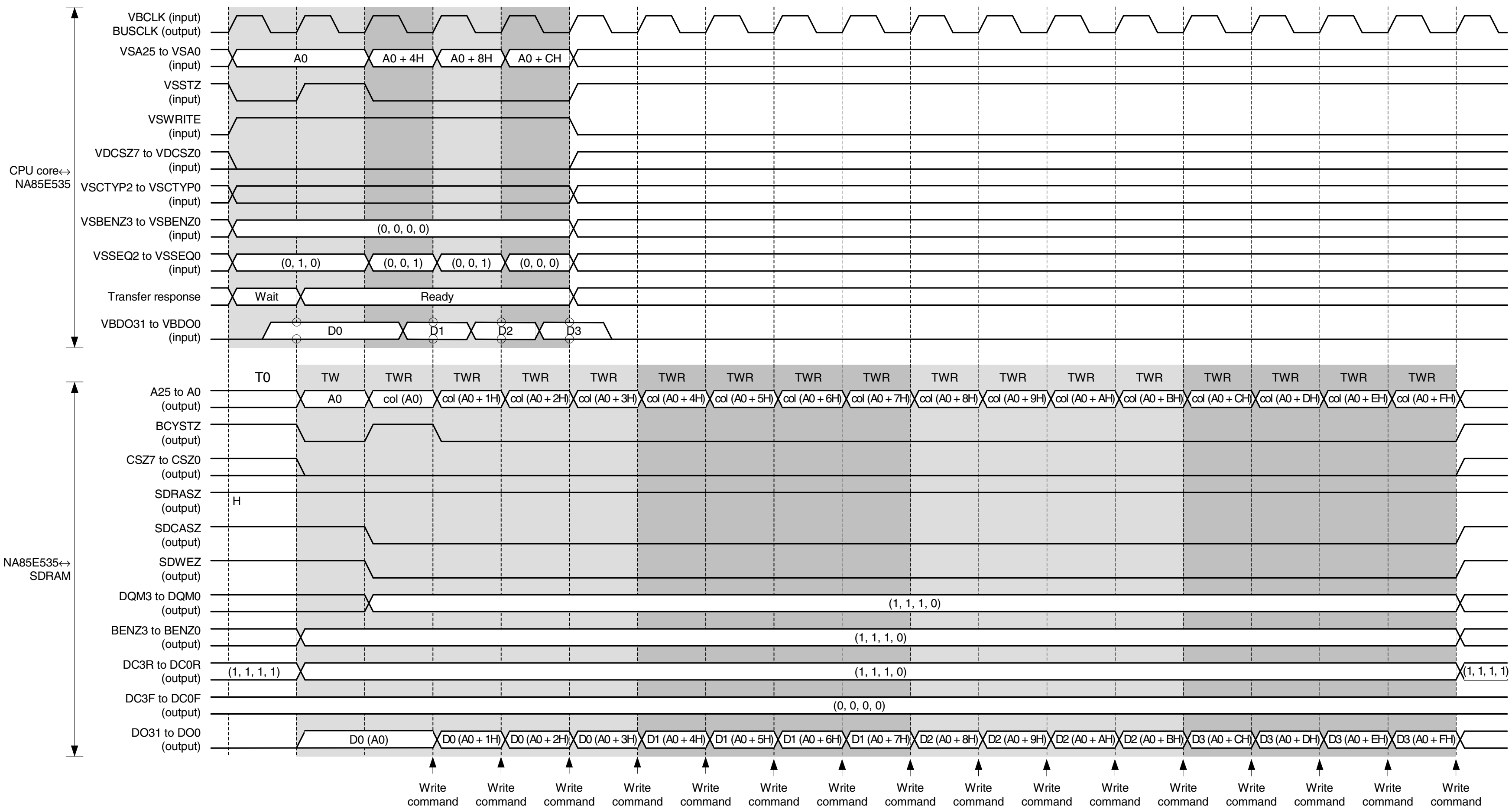
★Figure 4-2. Example of SDRAM Access Timing (13/14)

(m) Read cycle/without wait/CL = 2/16 times of sequential transfer from speculative read hit address/local bus size: 32 bits



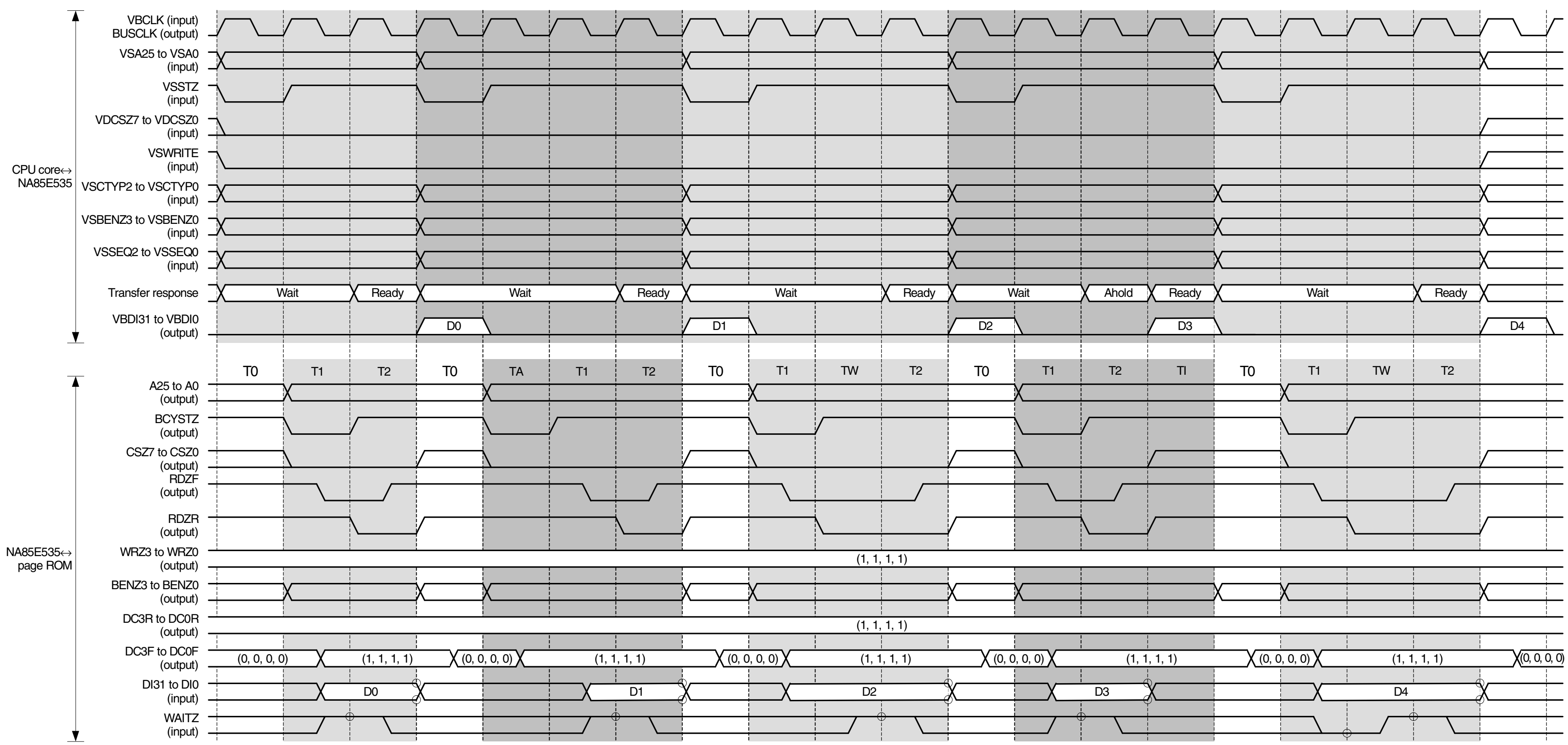
★Figure 4-2. Example of SDRAM Access Timing (14/14)

(n) Write cycle/without wait/sequential transfer/without page and bank change/local bus size: 8 bits



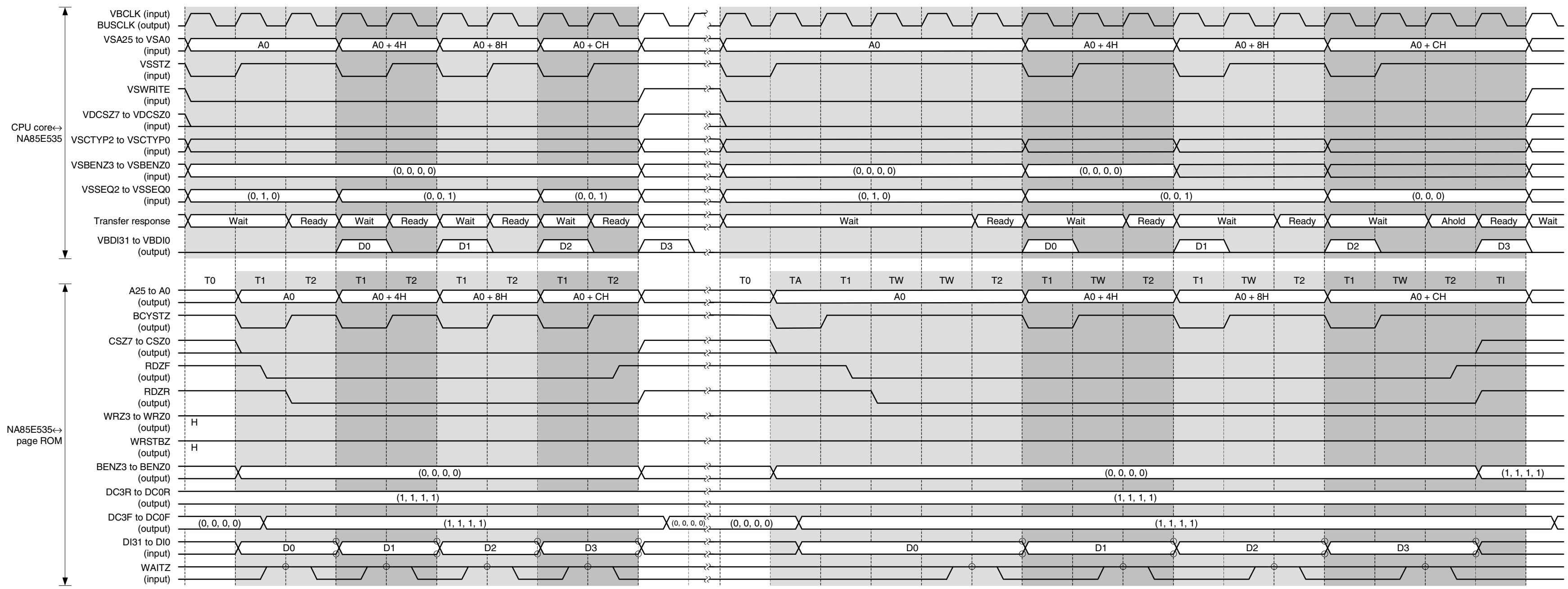
★**Figure 4-3. Example of Page ROM Access Timing (1/6)**

(a) Without speculative read/non-sequential transfer



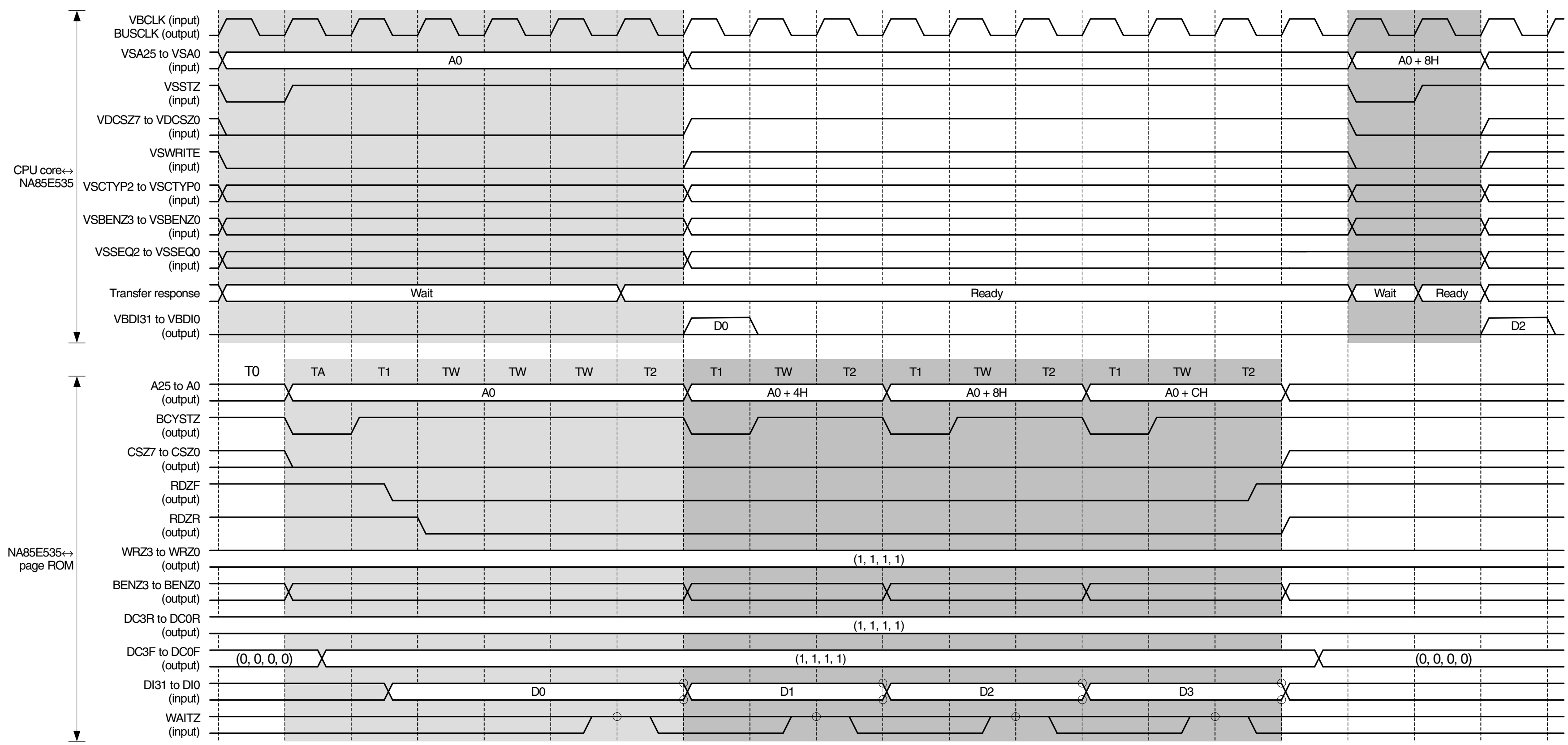
★Figure 4-3. Example of Page ROM Access Timing (2/6)

(b) Without speculative read/sequential transfer



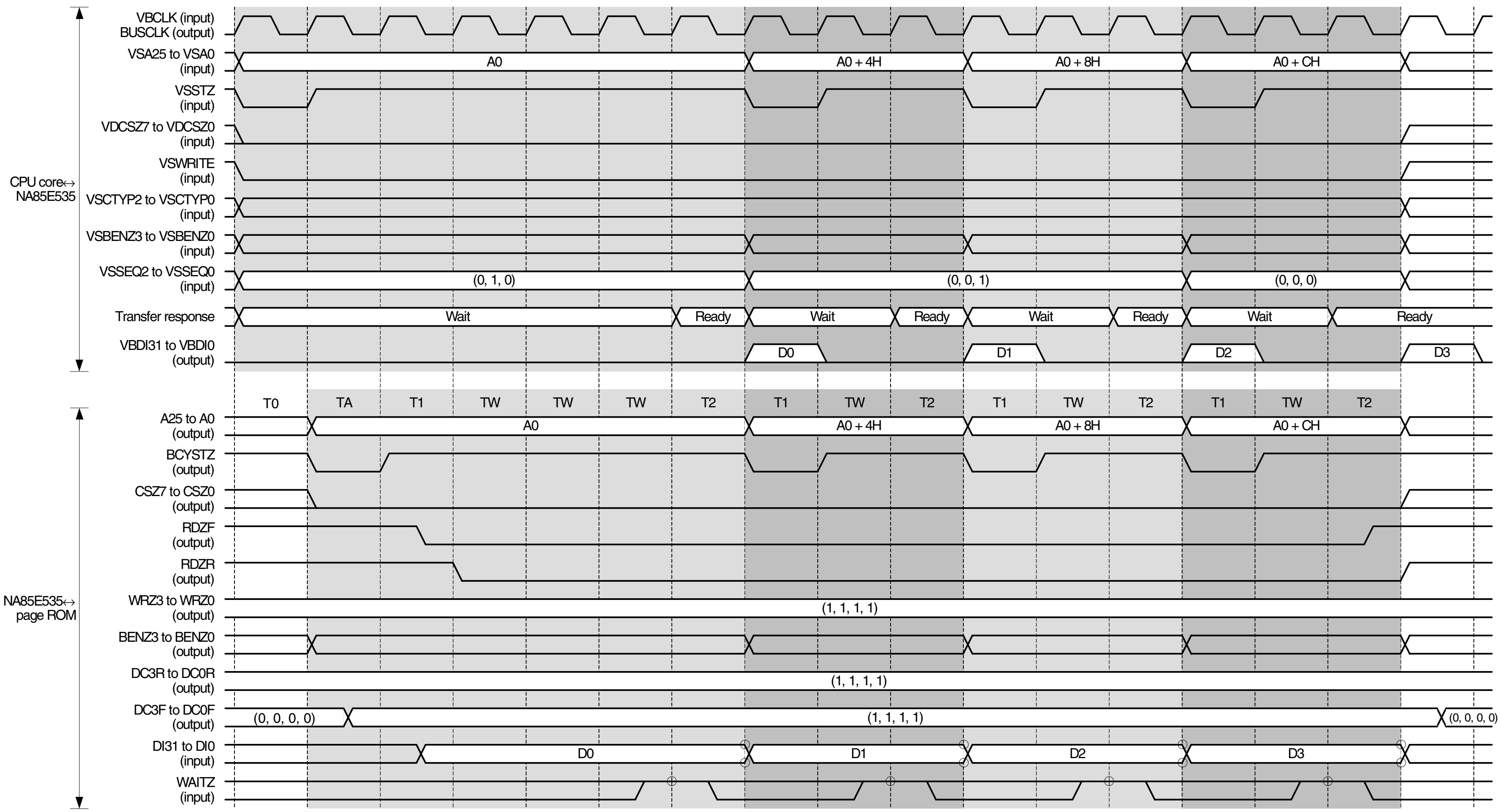
★Figure 4-3. Example of Page ROM Access Timing (3/6)

(c) With speculative read/non-sequential transfer



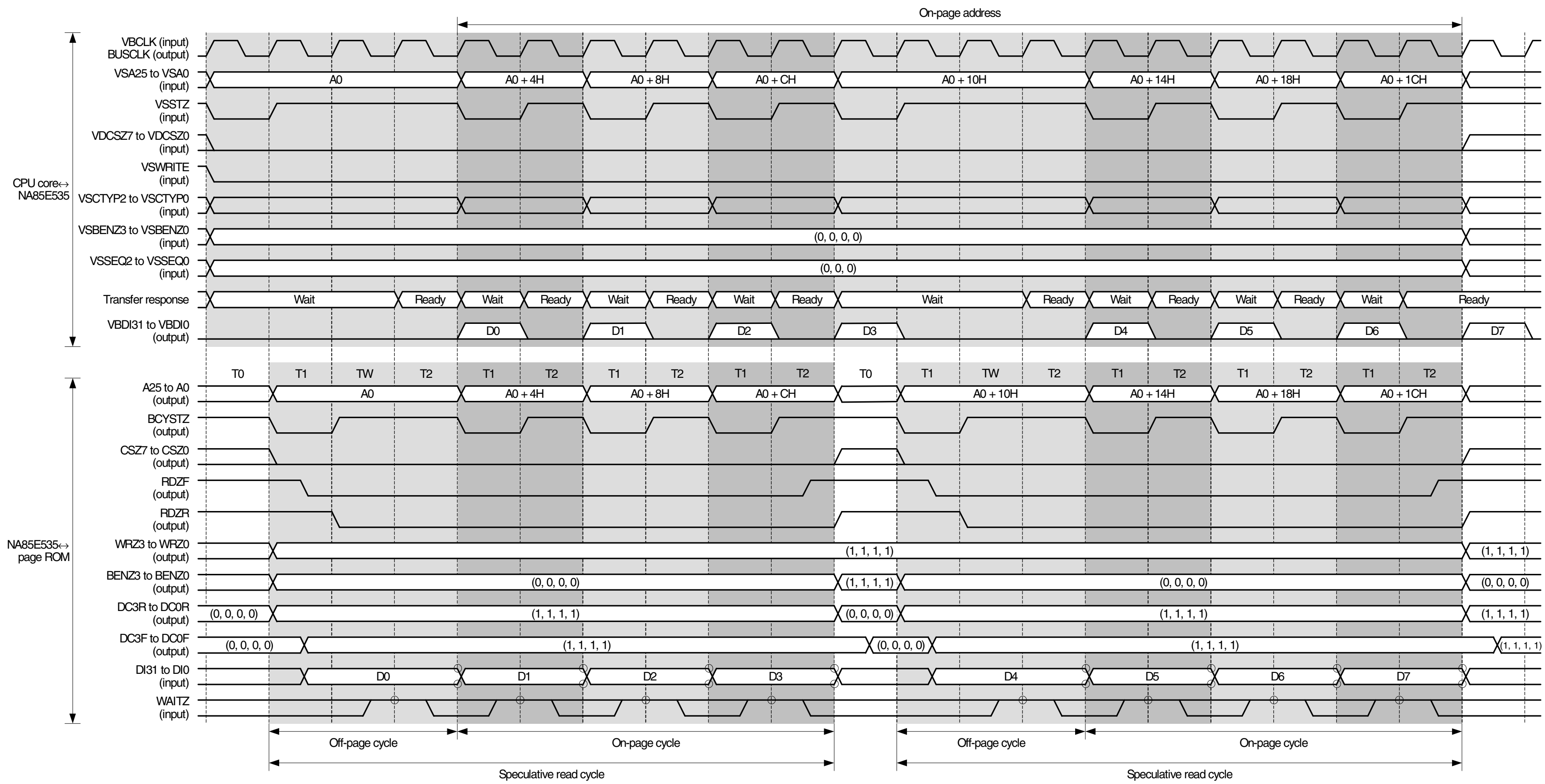
★Figure 4-3. Example of Page ROM Access Timing (4/6)

(d) With speculative read/sequential transfer



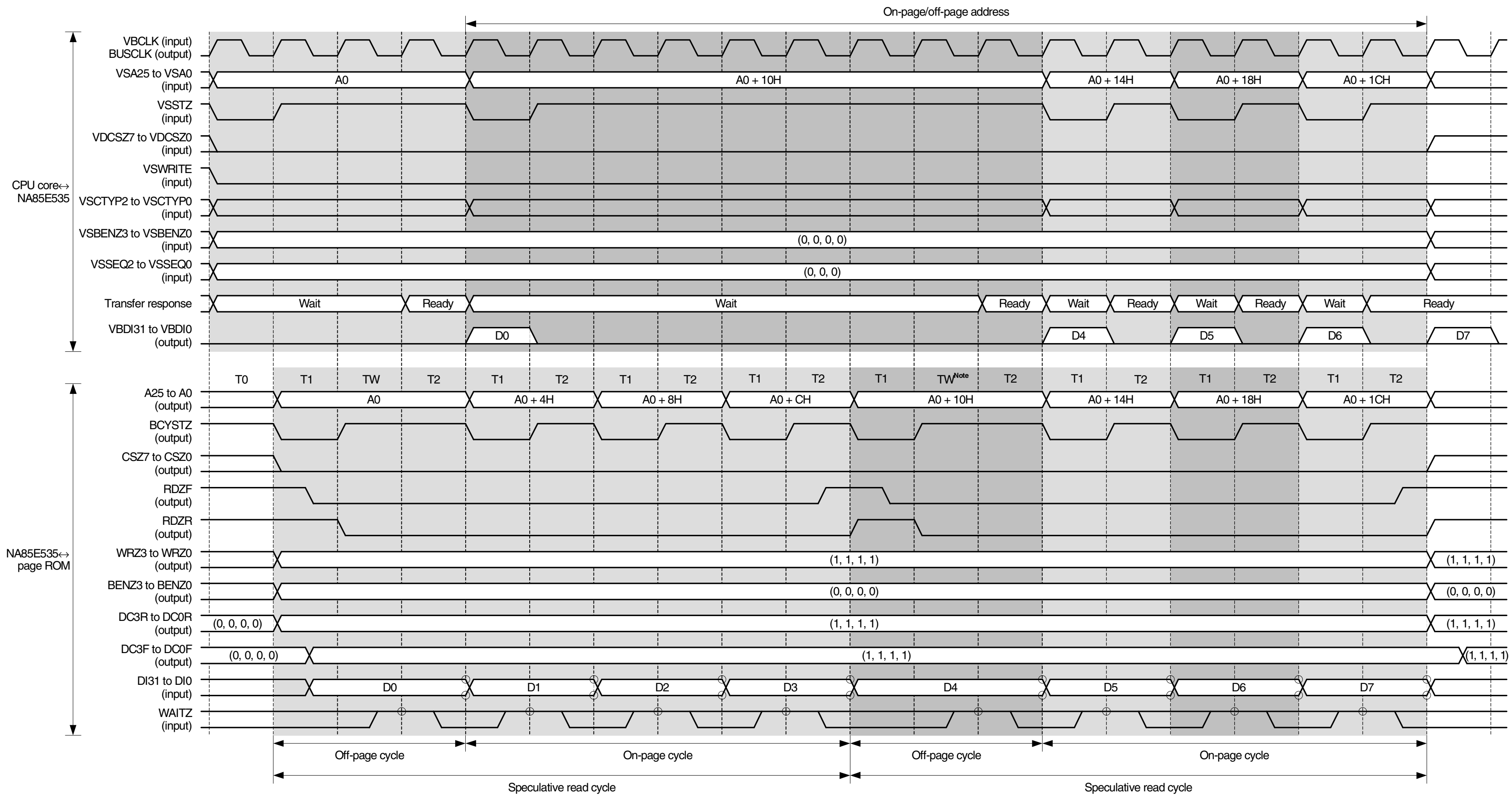
★Figure 4-3. Example of Page ROM Access Timing (5/6)

(e) With speculative read/off-page wait = 1/without on-page/local bus size: 32 bits (1)



★Figure 4-3. Example of Page ROM Access Timing (6/6)

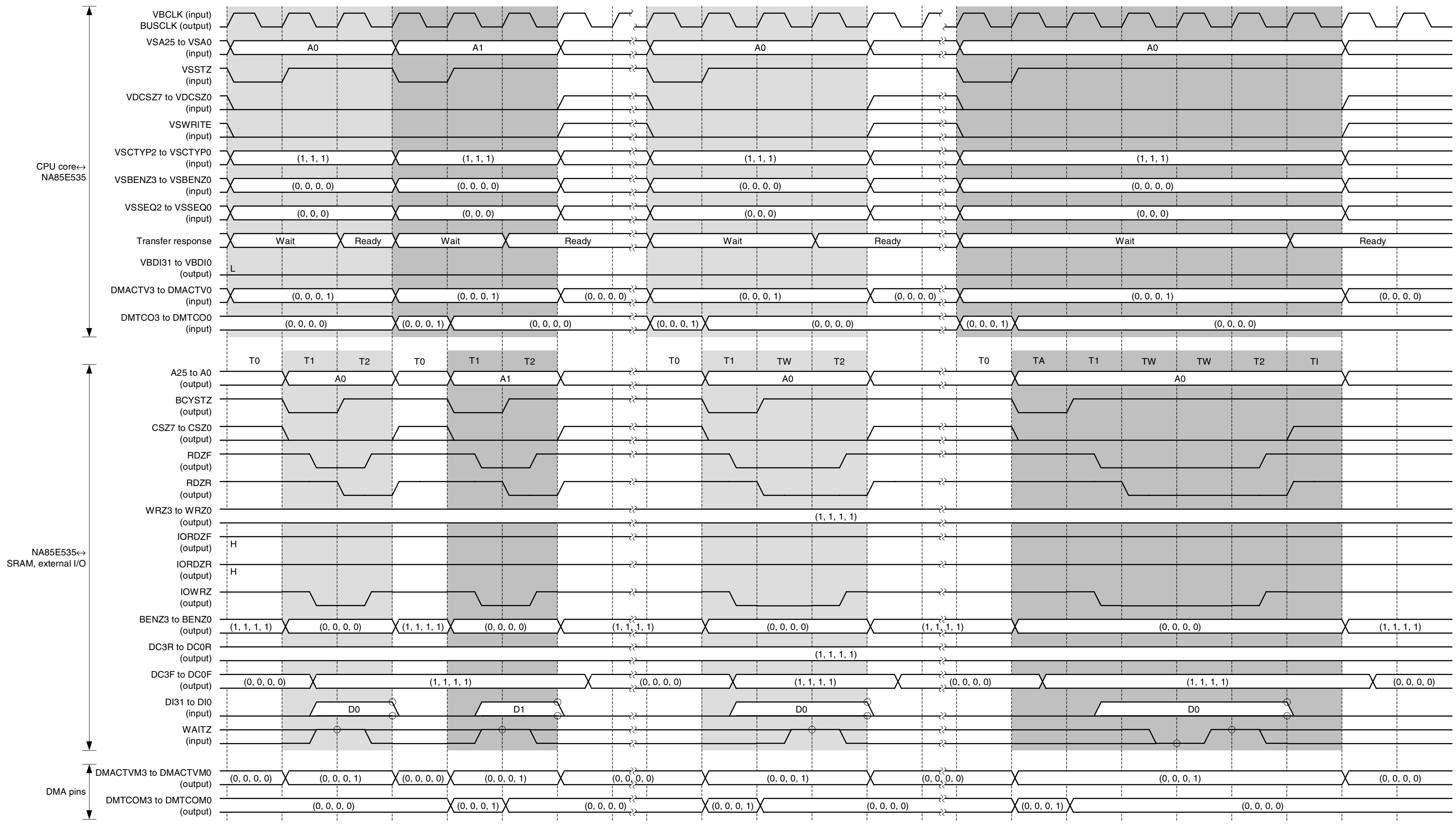
(f) With speculative read/off-page wait = 1/without on-page/local bus size: 32 bits (2)



Note If successive cycles have been completed, the wait cycles set as off-page cycles are inserted regardless of whether the address to be accessed next is within or outside the page range.

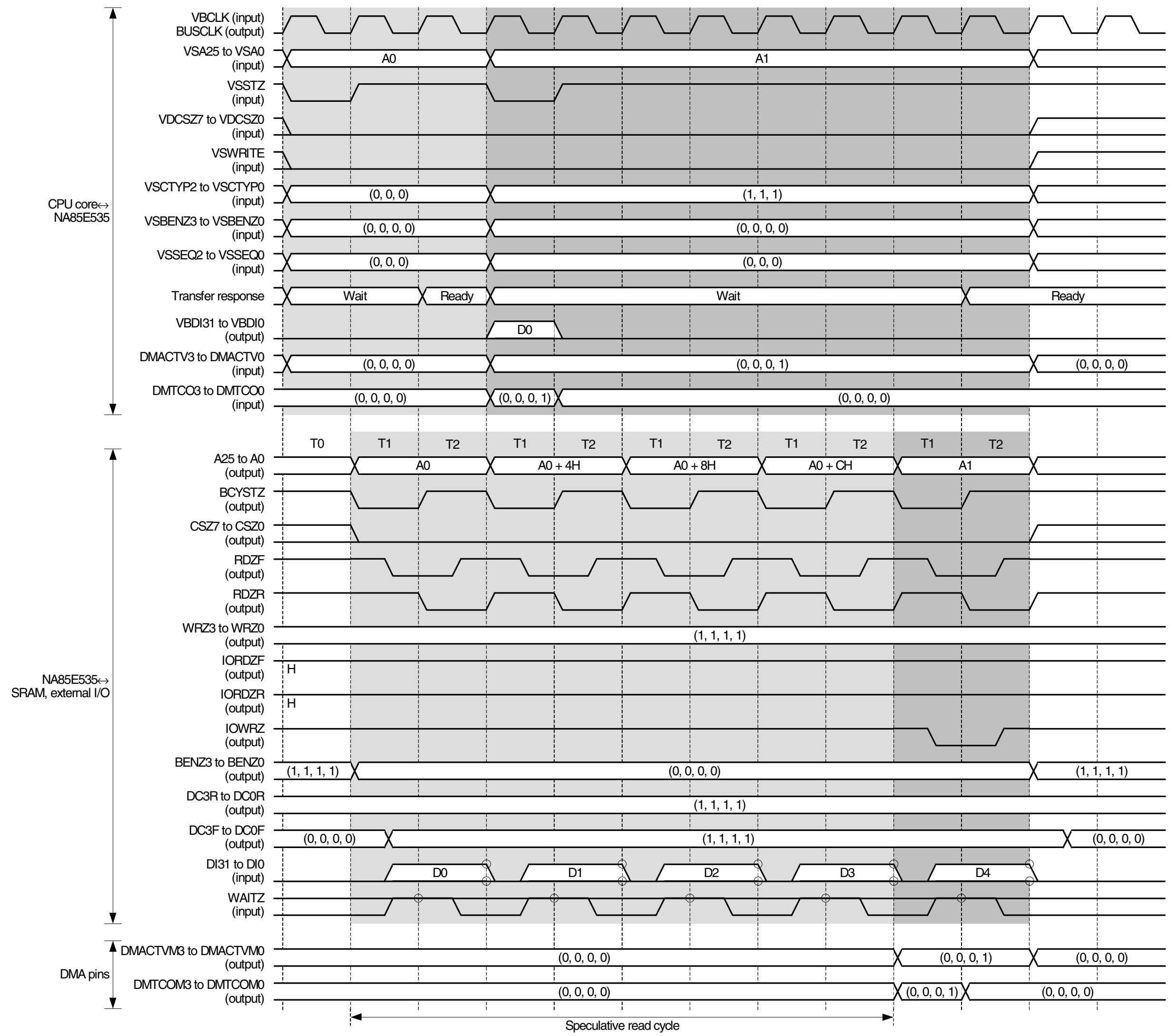
★Figure 4-4. Example of DMA Transfer Timing (Flyby Transfer (Using DMAC with On-Chip CPU Core): SRAM → External I/O) (1/4)

(a) Single transfer



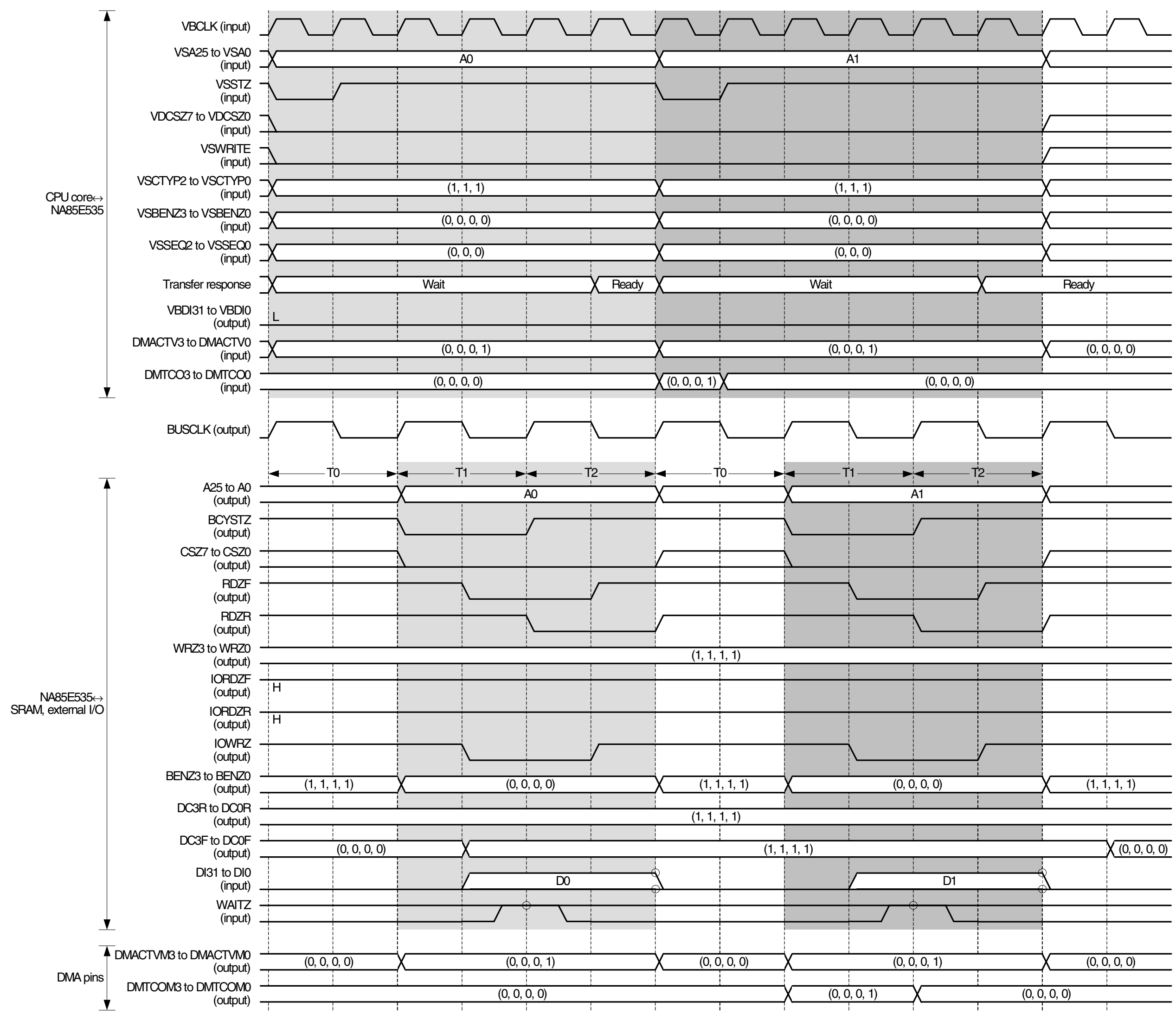
★Figure 4-4. Example of DMA Transfer Timing (Flyby Transfer (Using DMAC with On-Chip CPU Core): SRAM → External I/O) (2/4)

(b) Single transfer/transfer request during speculative read



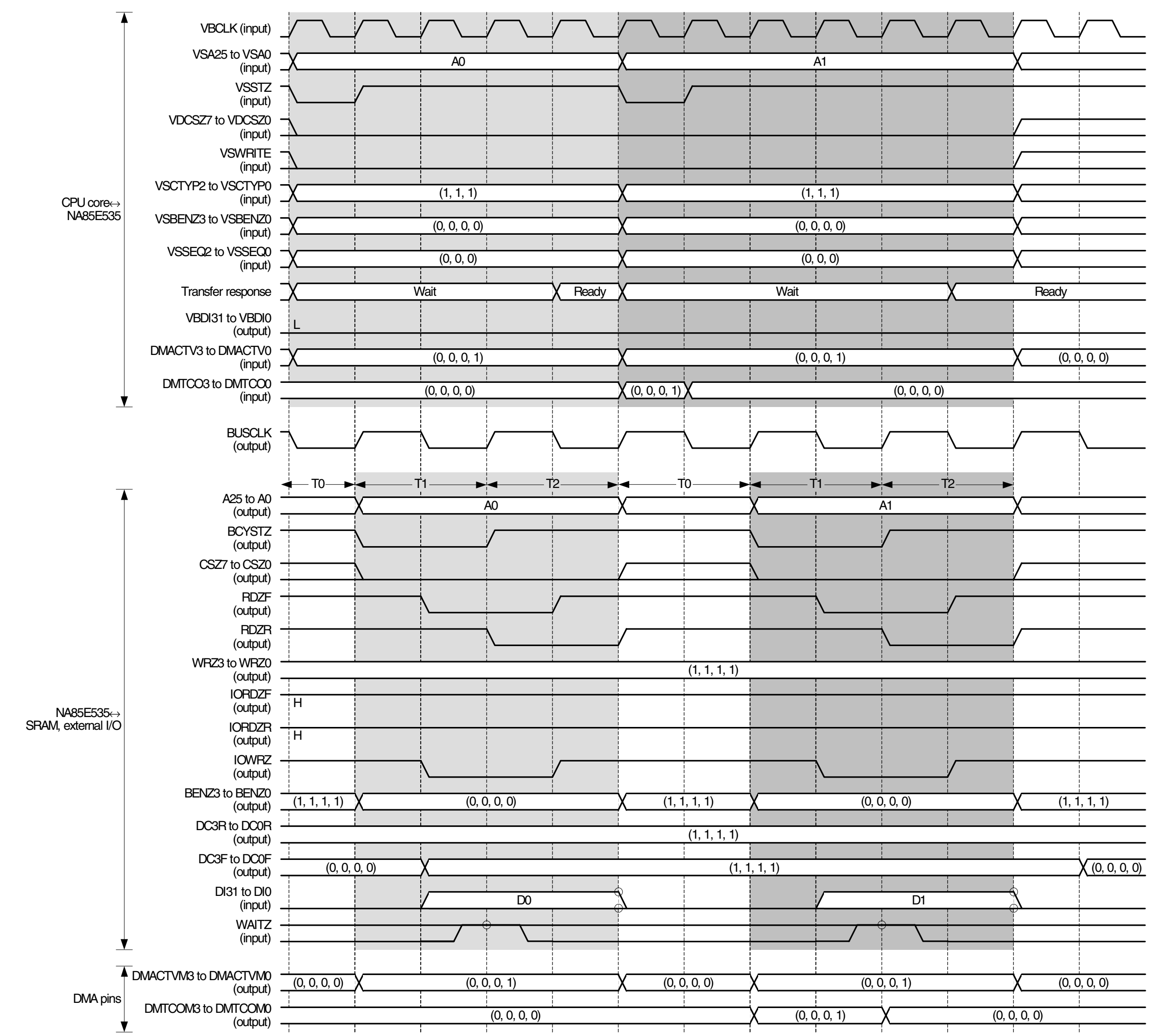
★Figure 4-4. Example of DMA Transfer Timing (Flyby Transfer (Using DMAC with On-Chip CPU Core): SRAM → External I/O) (3/4)

(c) Single transfer/division by 2 (1)



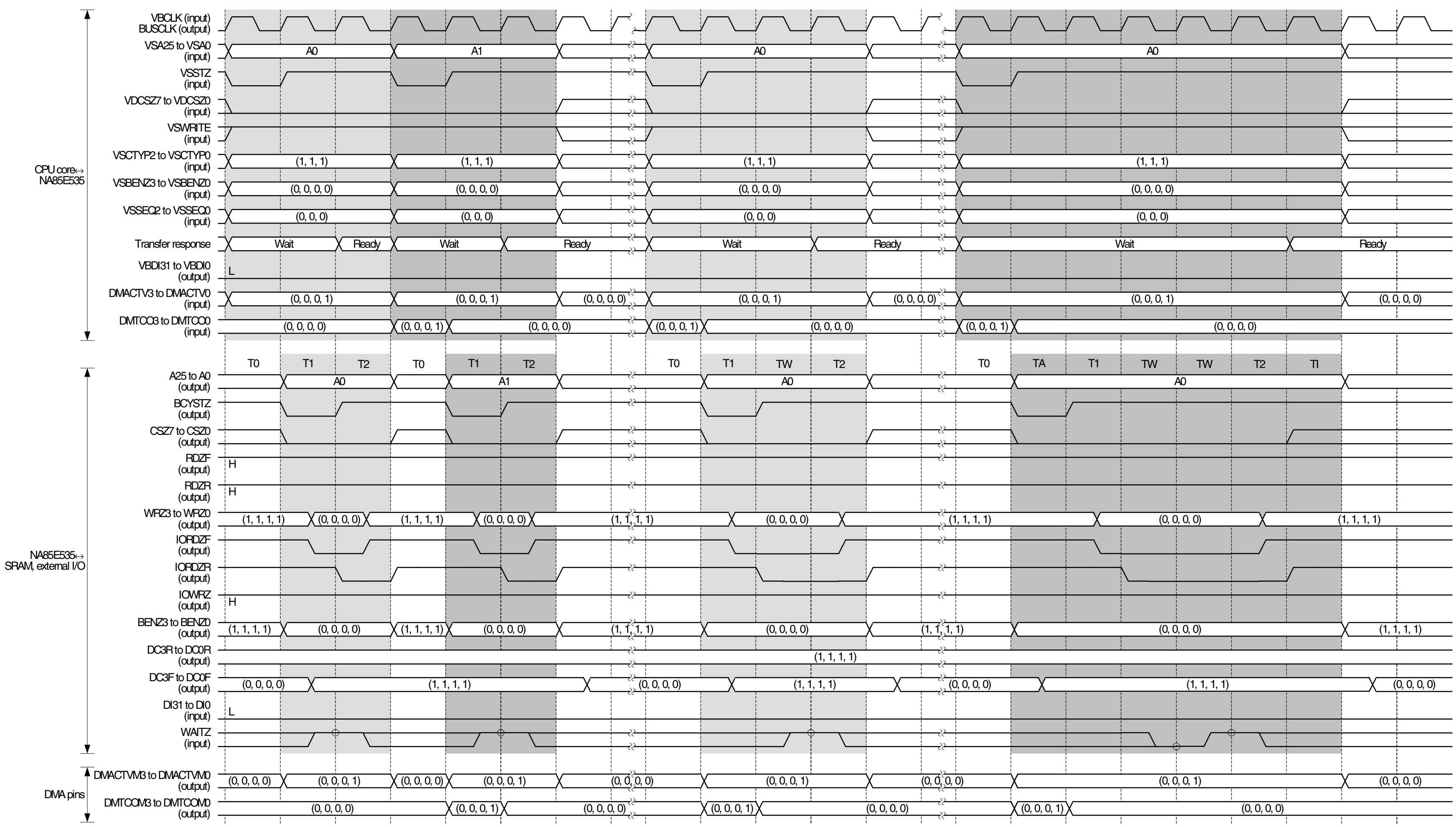
★Figure 4-4. Example of DMA Transfer Timing (Flyby Transfer (Using DMAC with On-Chip CPU Core): SRAM → External I/O) (4/4)

(d) Single transfer/division by 2 (2)



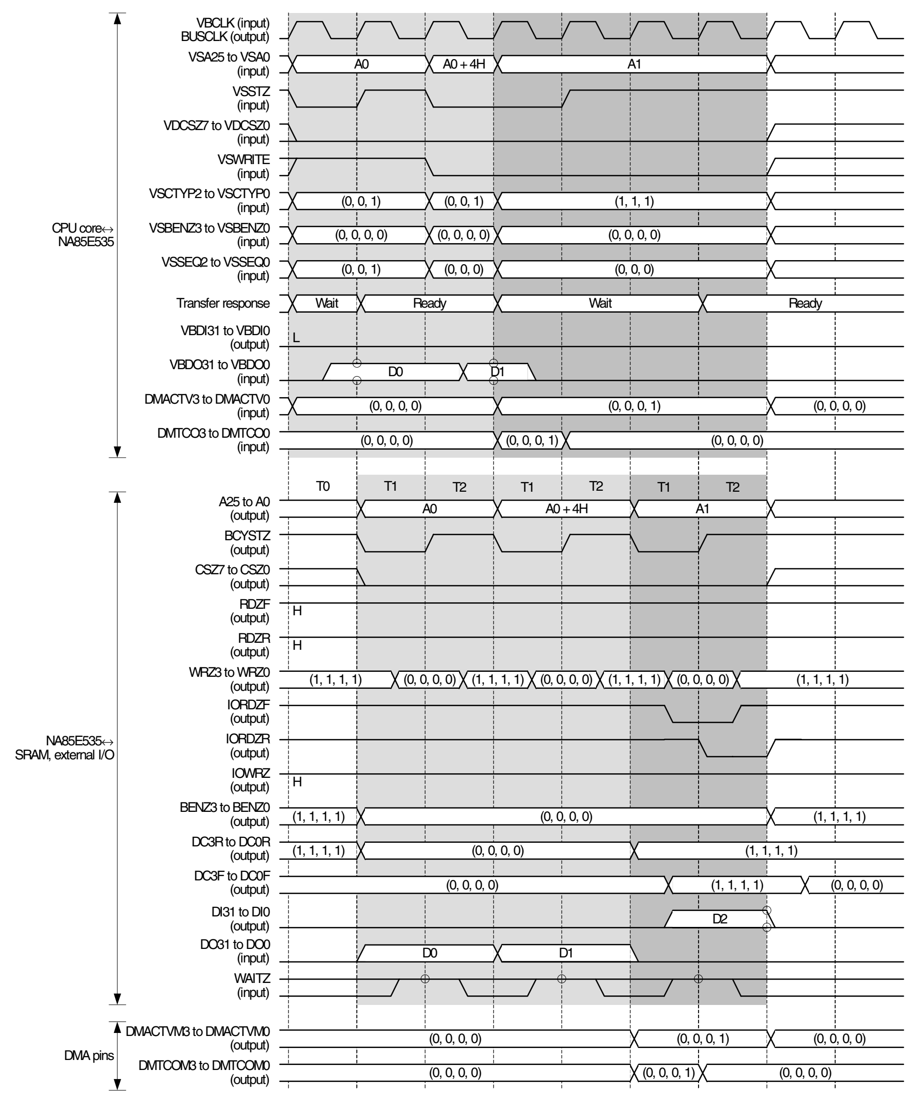
★Figure 4-5. Example of DMA Transfer Timing (Flyby Transfer (Using DMAC with On-Chip CPU Core): External I/O → SRAM) (1/2)

(a) Single transfer

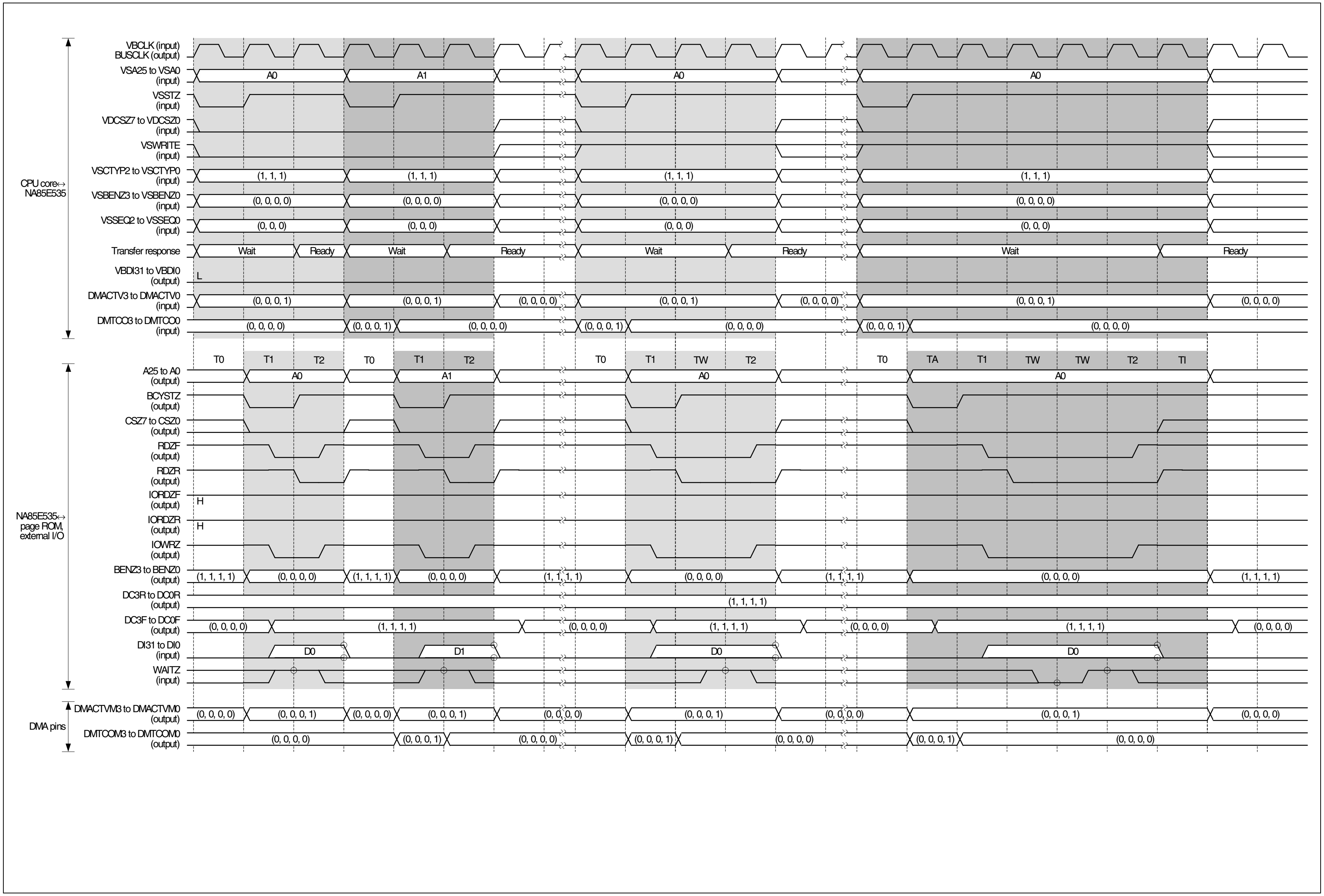


★Figure 4-5. Example of DMA Transfer Timing (Flyby Transfer (Using DMAC with On-Chip CPU Core): External I/O → SRAM) (2/2)

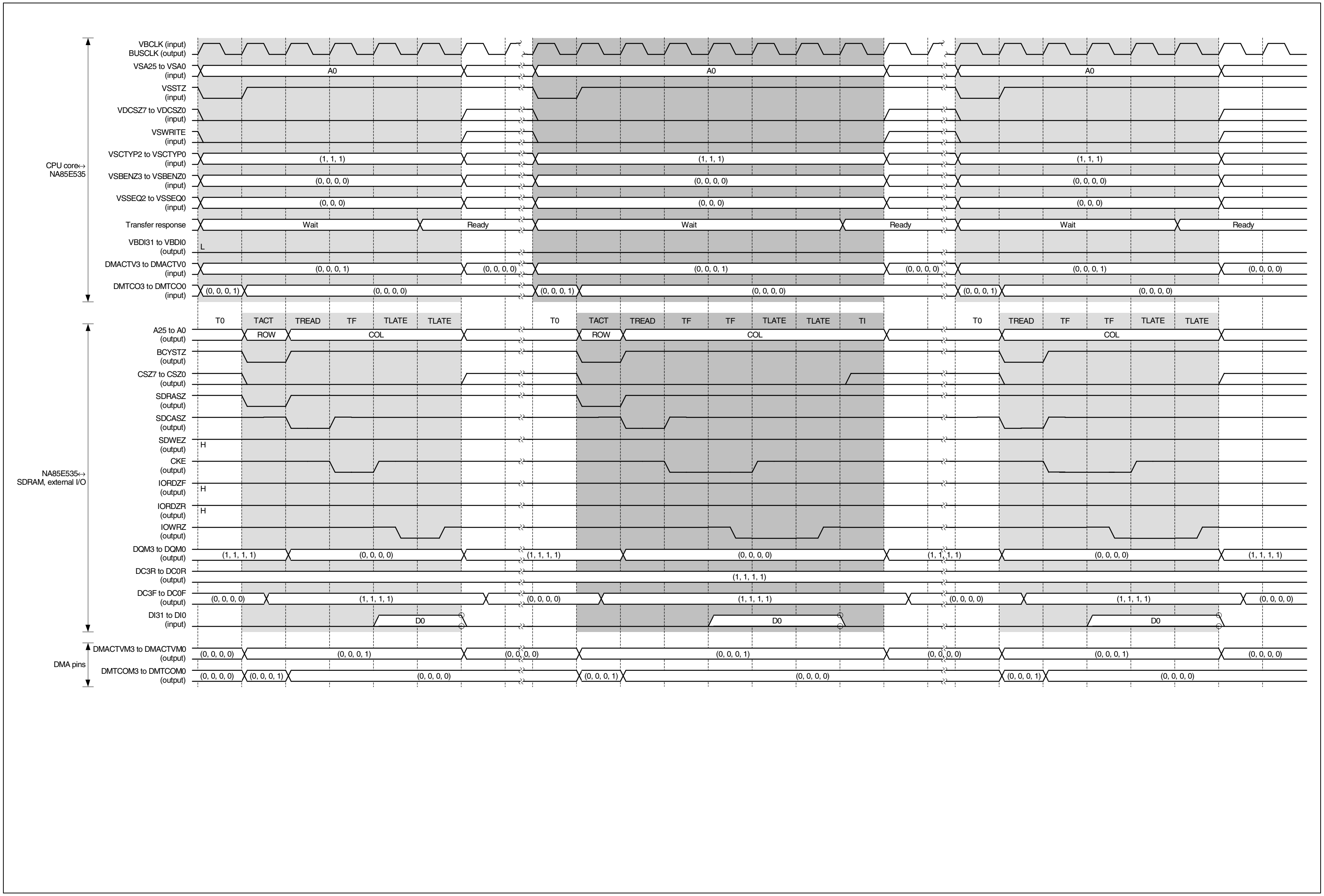
(b) Single transfer/flyby transfer request during write



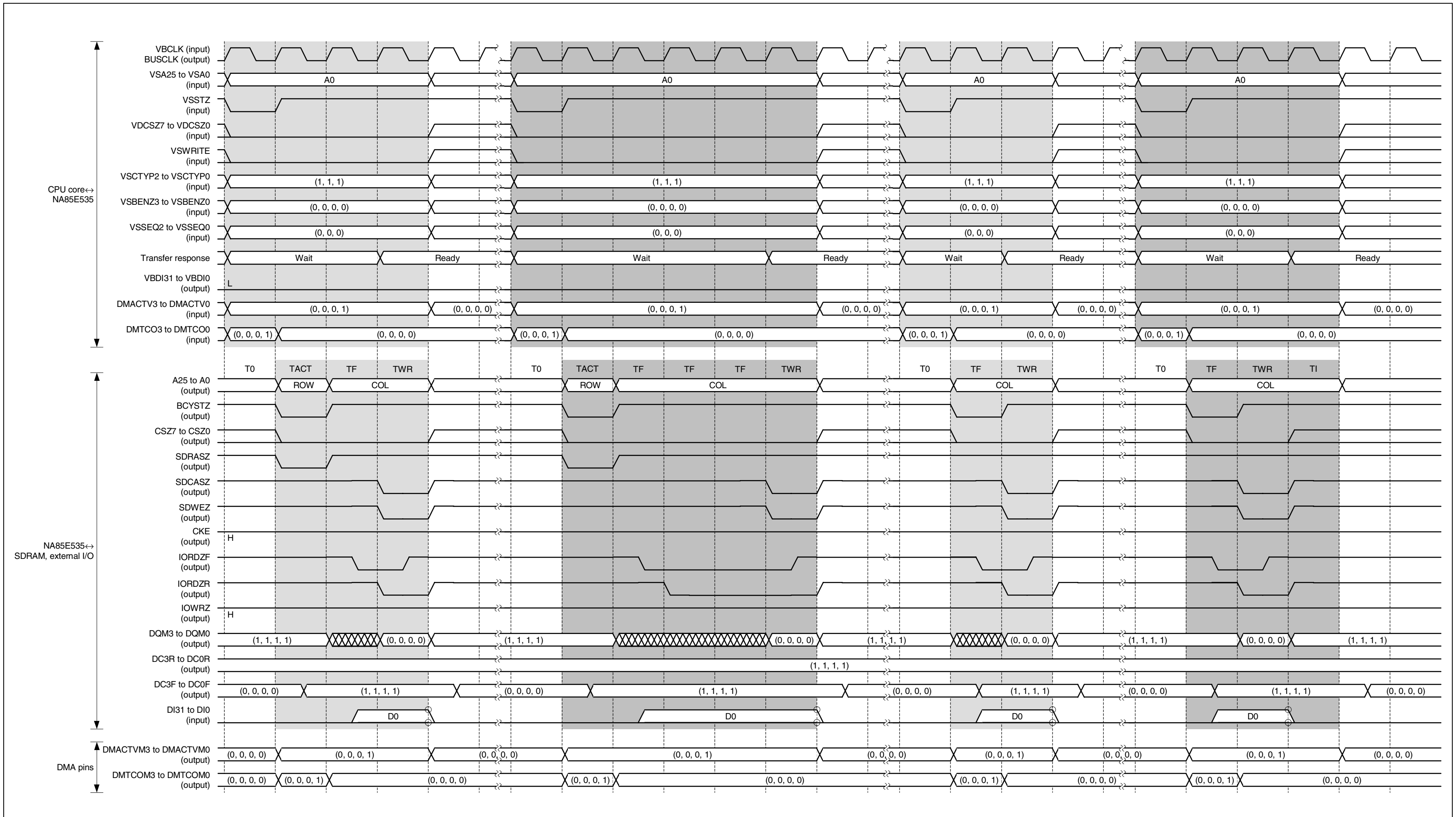
★Figure 4-6. Example of DMA Transfer Timing (Flyby Transfer (Using DMAC with On-Chip CPU Core): Page ROM→ External I/O (Single Transfer)



★**Figure 4-7. Example of DMA Transfer Timing (Flyby Transfer (Using DMAC with On-Chip CPU Core): SDRAM→ External I/O (Single Transfer)**

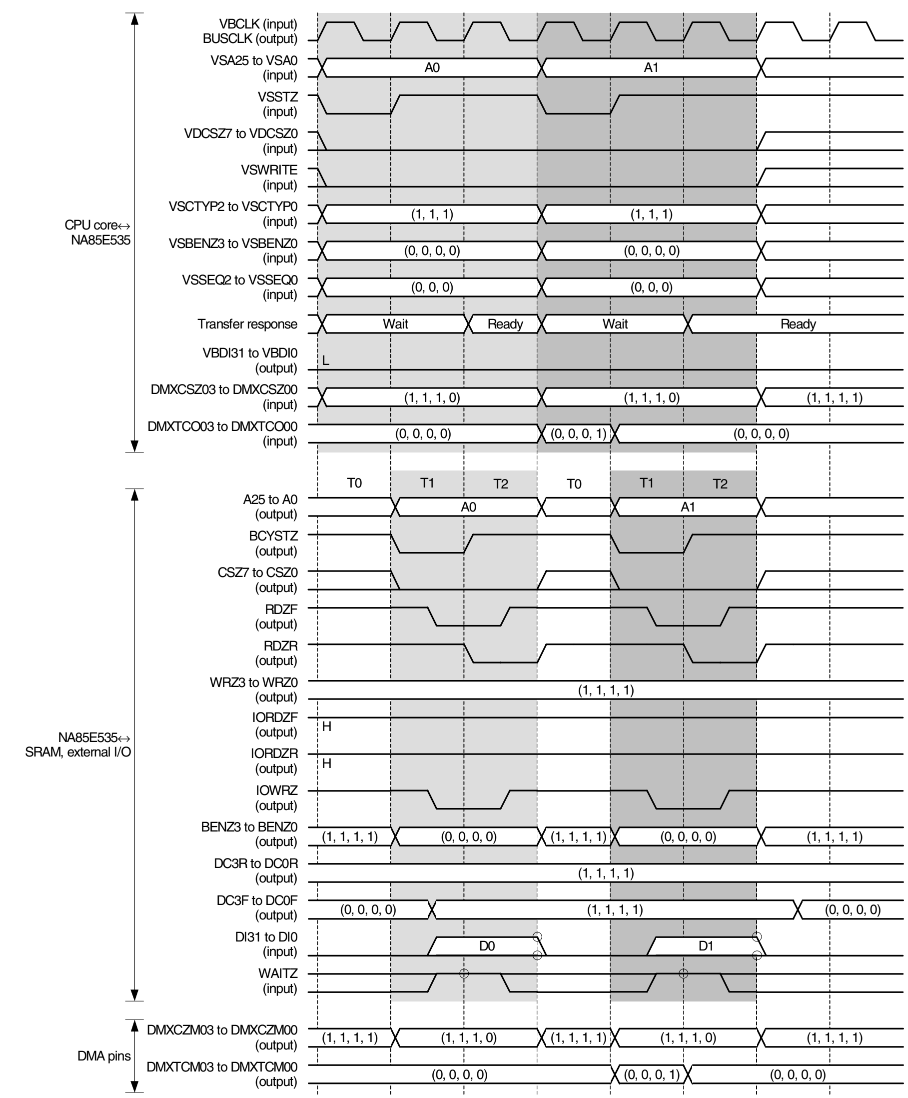


★Figure 4-8. Example of DMA Transfer Timing (Flyby Transfer (Using DMAC with On-Chip CPU Core): External I/O → SDRAM (Single Transfer)



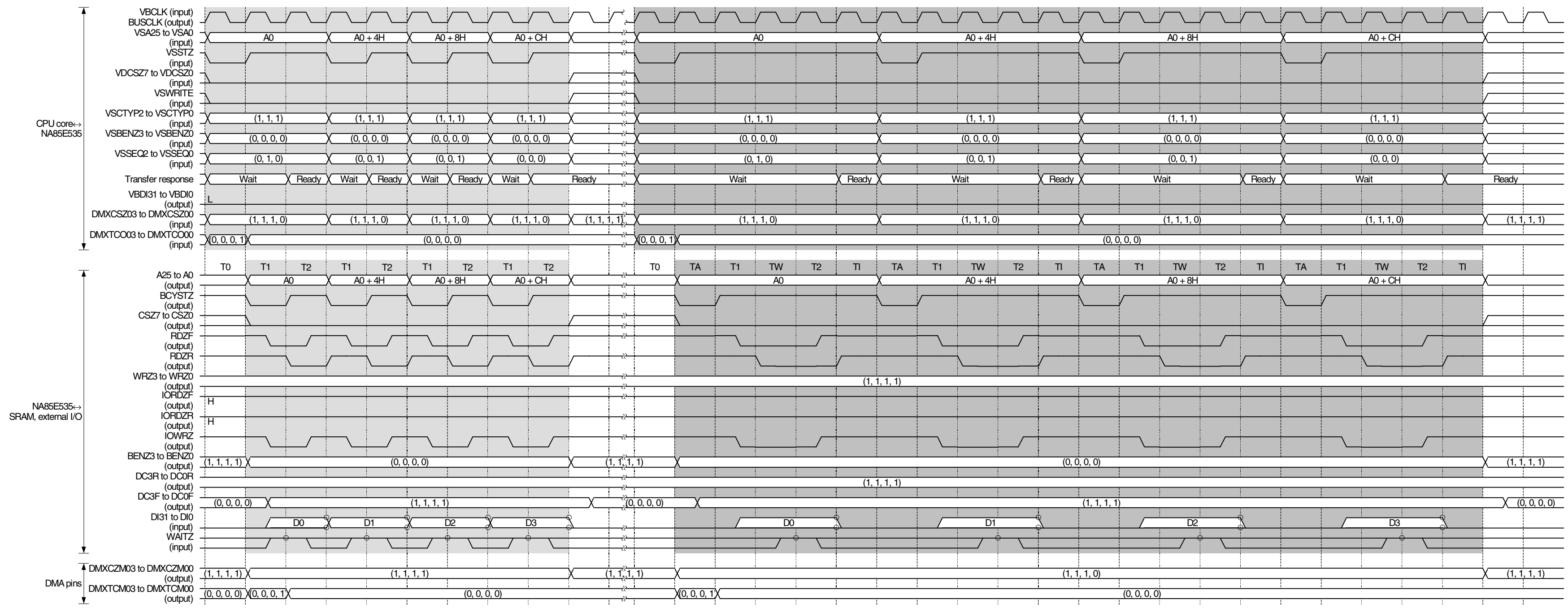
★Figure 4-9. Example of DMA Transfer Timing (Flyby Transfer (with NA85E300): SRAM → External I/O) (1/2)

(a) Single transfer



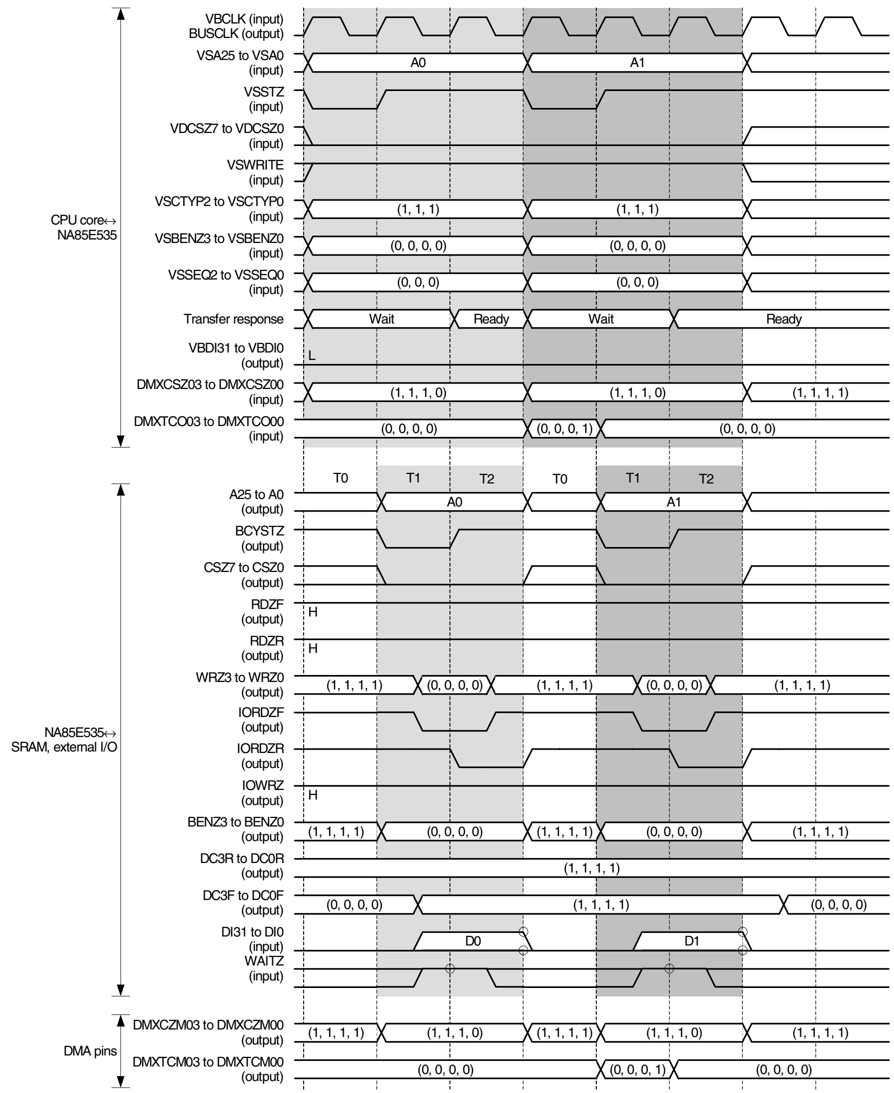
★**Figure 4-9. Example of DMA Transfer Timing (Flyby Transfer (with NA85E300): SRAM → External I/O) (2/2)**

(b) Single transfer (4 words)



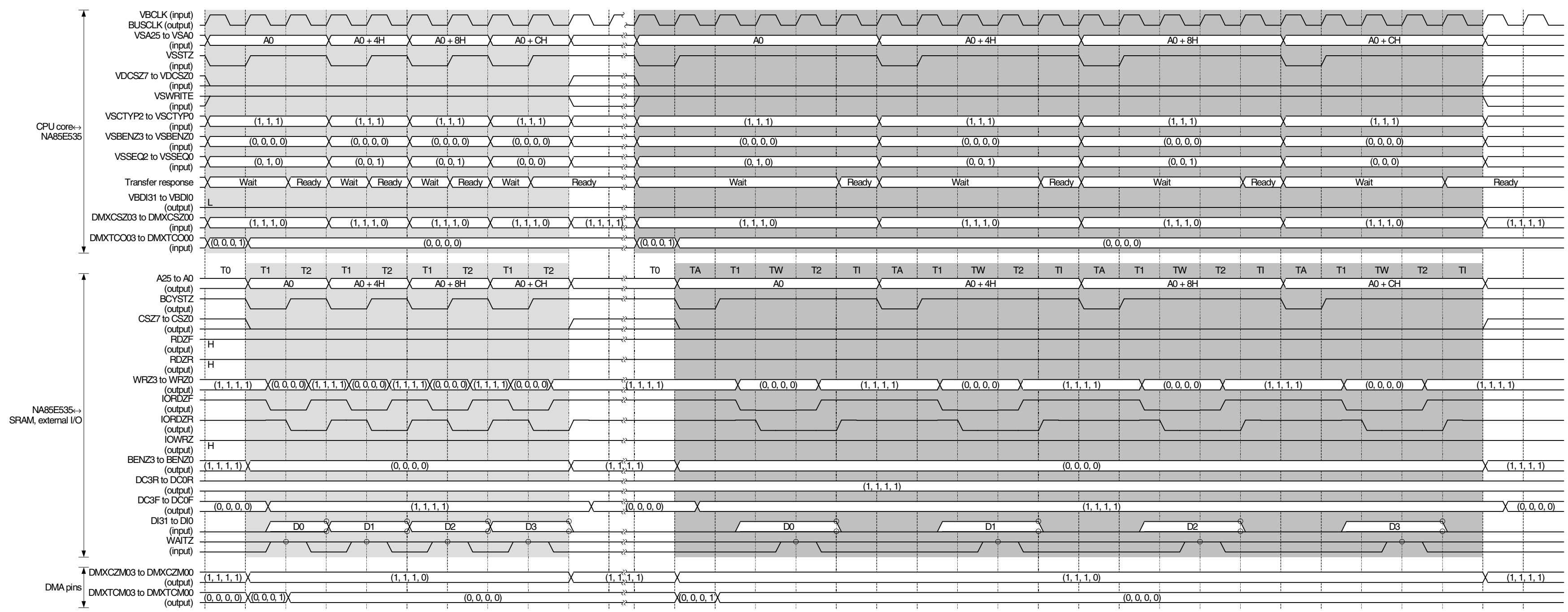
★Figure 4-10. Example of DMA Transfer Timing (Flyby Transfer (with NA85E300): External I/O → SRAM) (1/2)

(a) Single transfer

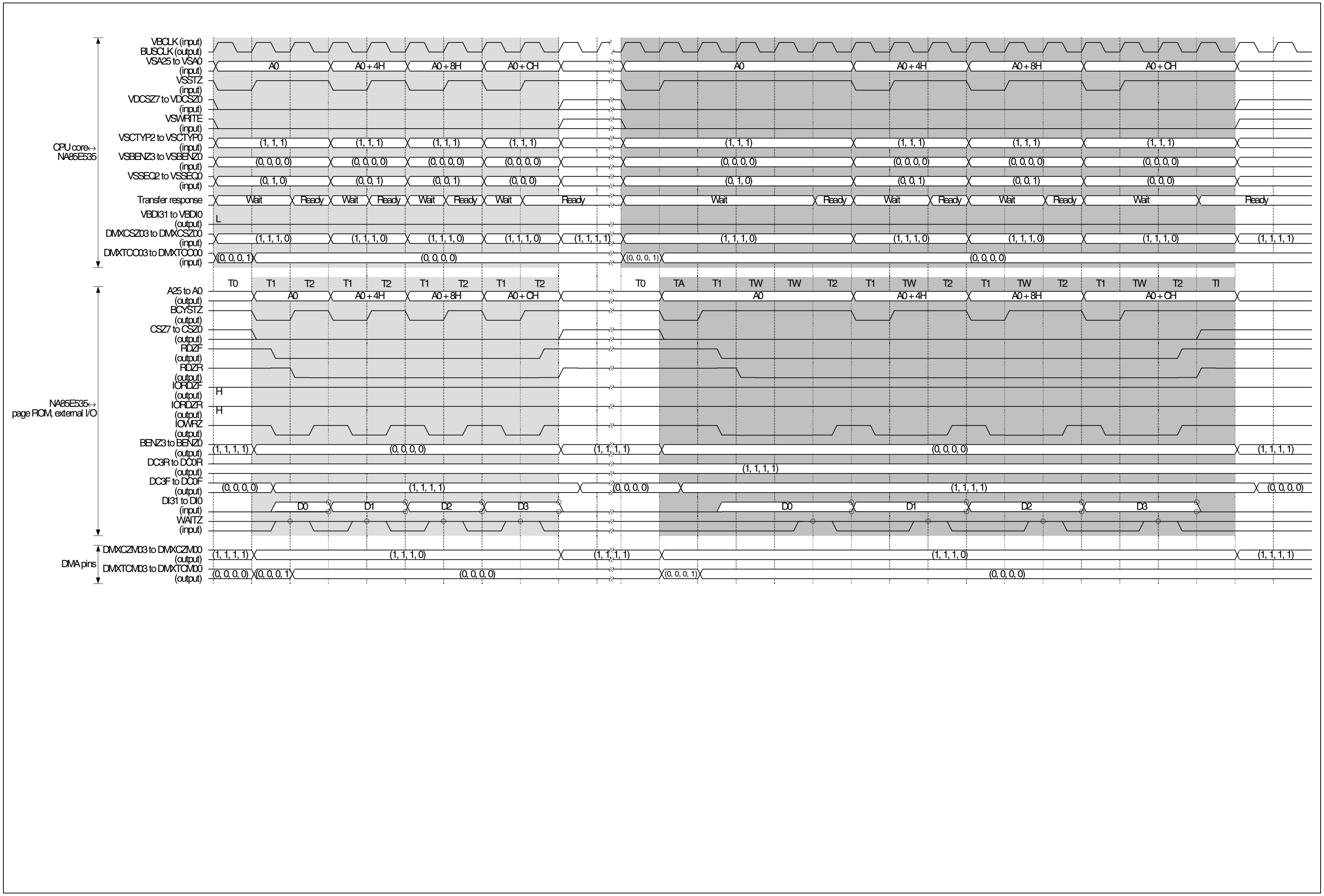


★Figure 4-10. Example of DMA Transfer Timing (Flyby Transfer (with NA85E300): External I/O → SRAM) (2/2)

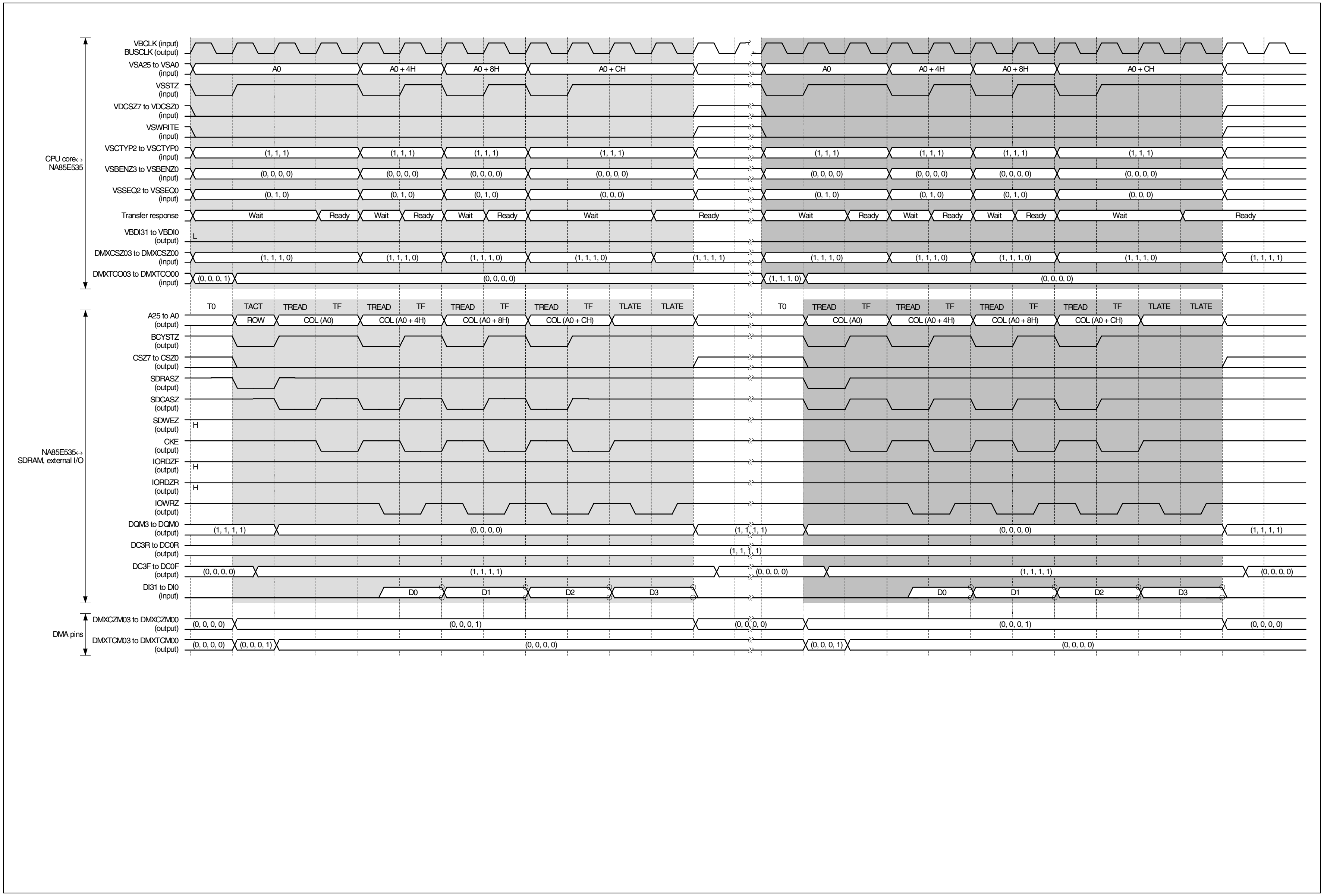
(b) Single transfer (4 words)



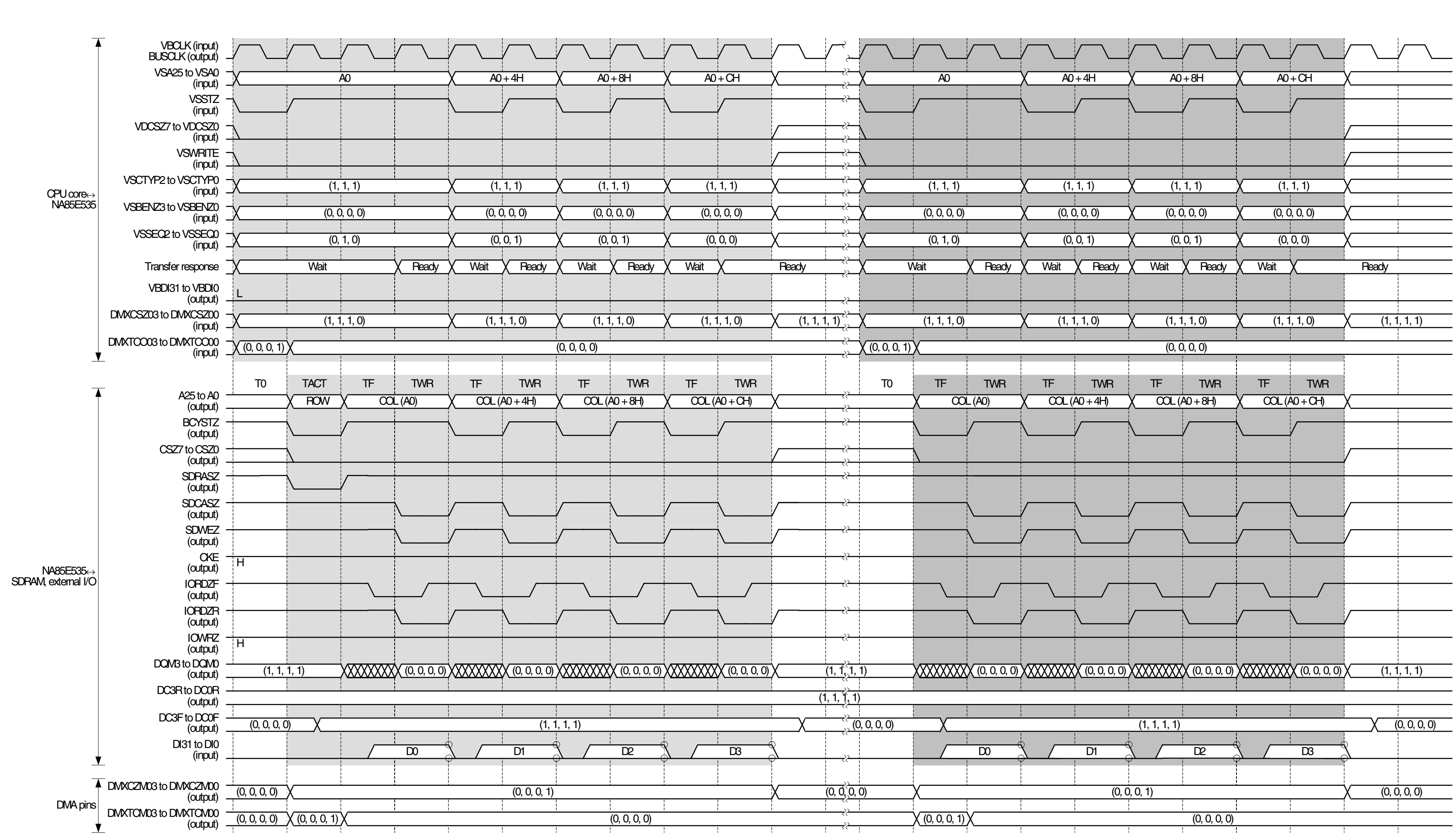
★**Figure 4-11. Example of DMA Transfer Timing (Flyby Transfer (with NA85E300): Page ROM → External I/O) (Single Transfer (4 Words)))**



★**Figure 4-12. Example of DMA Transfer Timing (Flyby Transfer (with NA85E300): SDRAM → External I/O) (Single Transfer (4 Words)))**

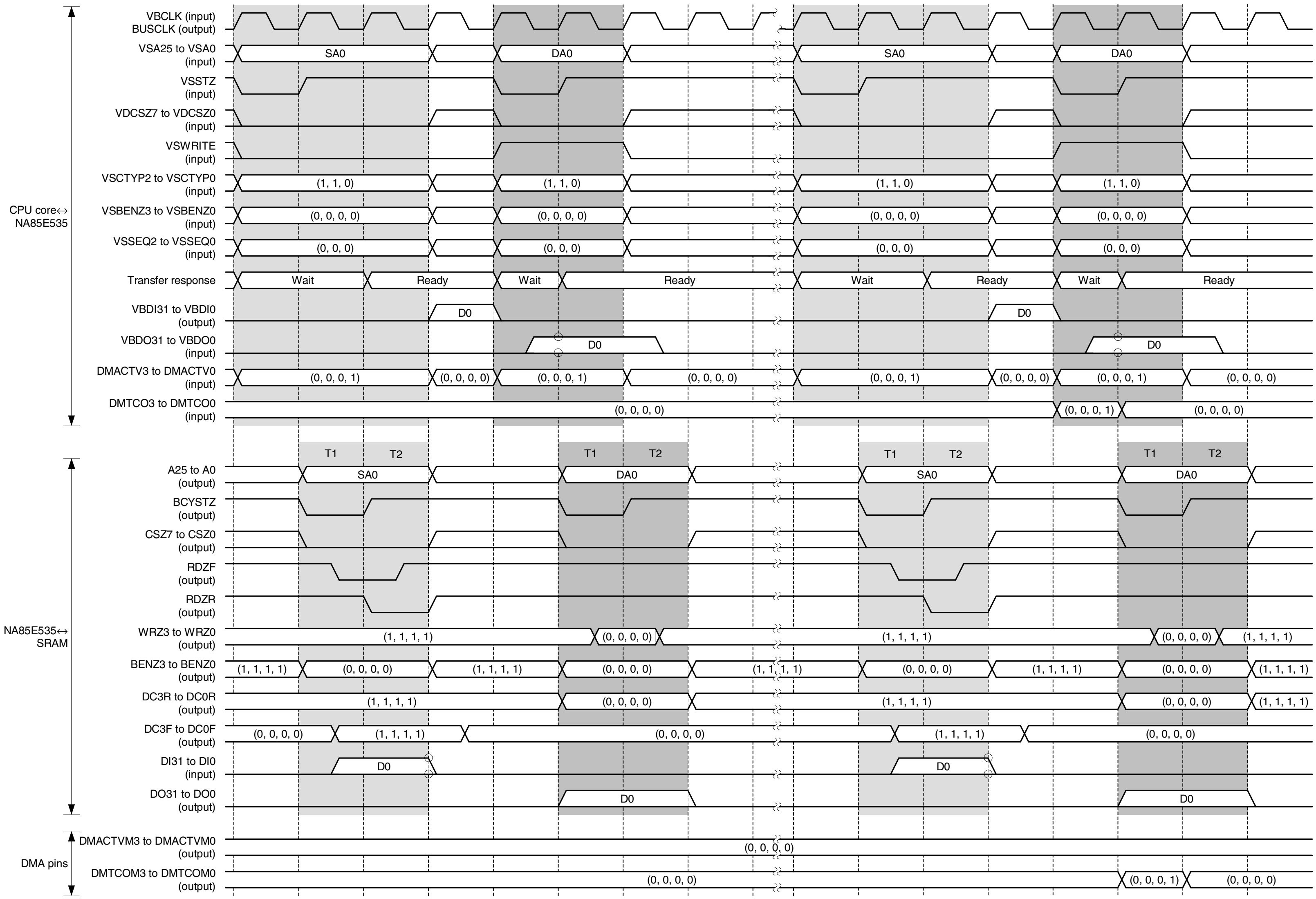


★Figure 4-13. Example of DMA Transfer Timing (Flyby Transfer (with NA85E300): External I/O → SDRAM) (Single Transfer (4 Words)))



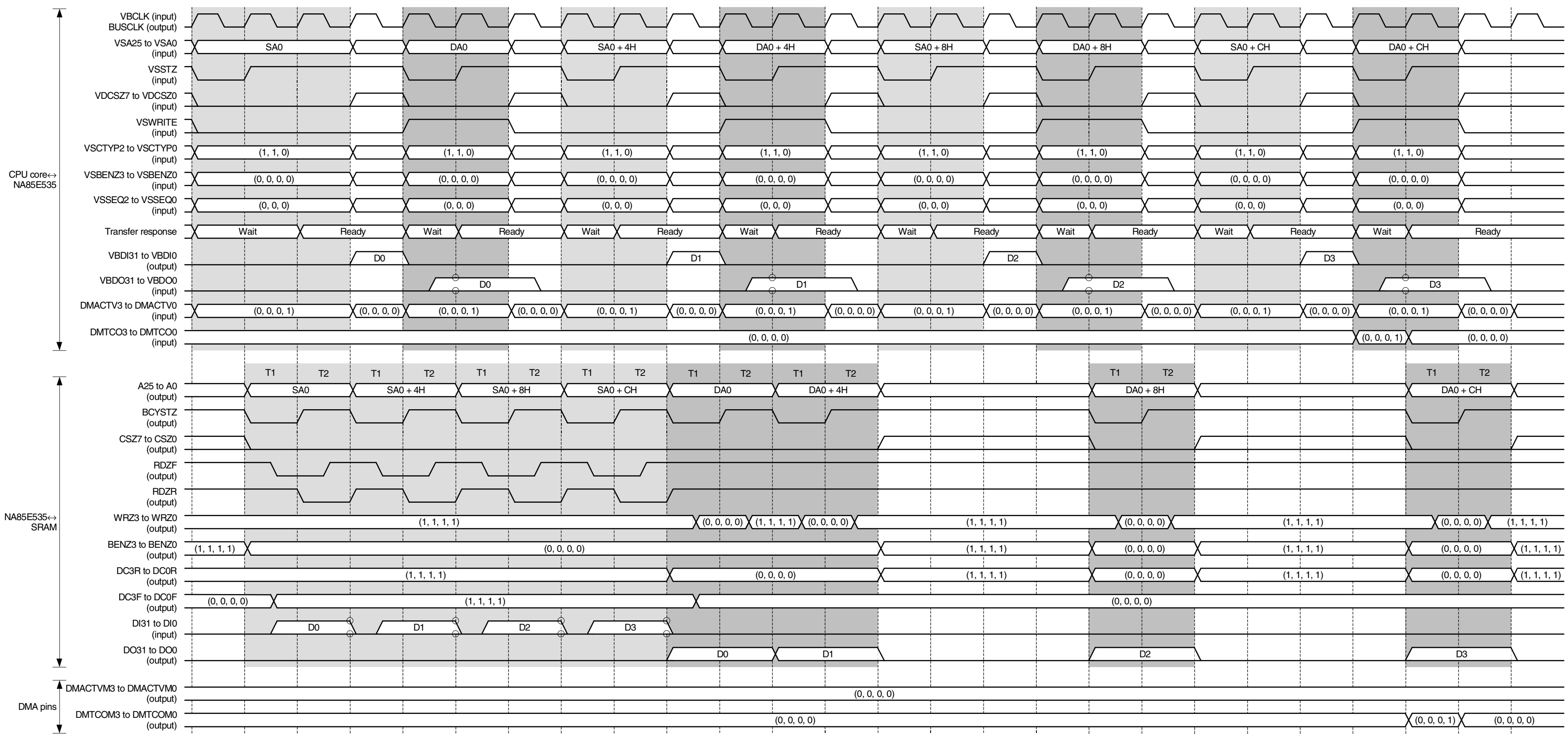
★Figure 4-14. Example of DMA Transfer Timing (2-Cycle Transfer (Using DMAC with On-Chip CPU Core): SRAM → SRAM) (1/5)

(a) Single transfer/without wait/without speculative read/local bus size: 32 bits



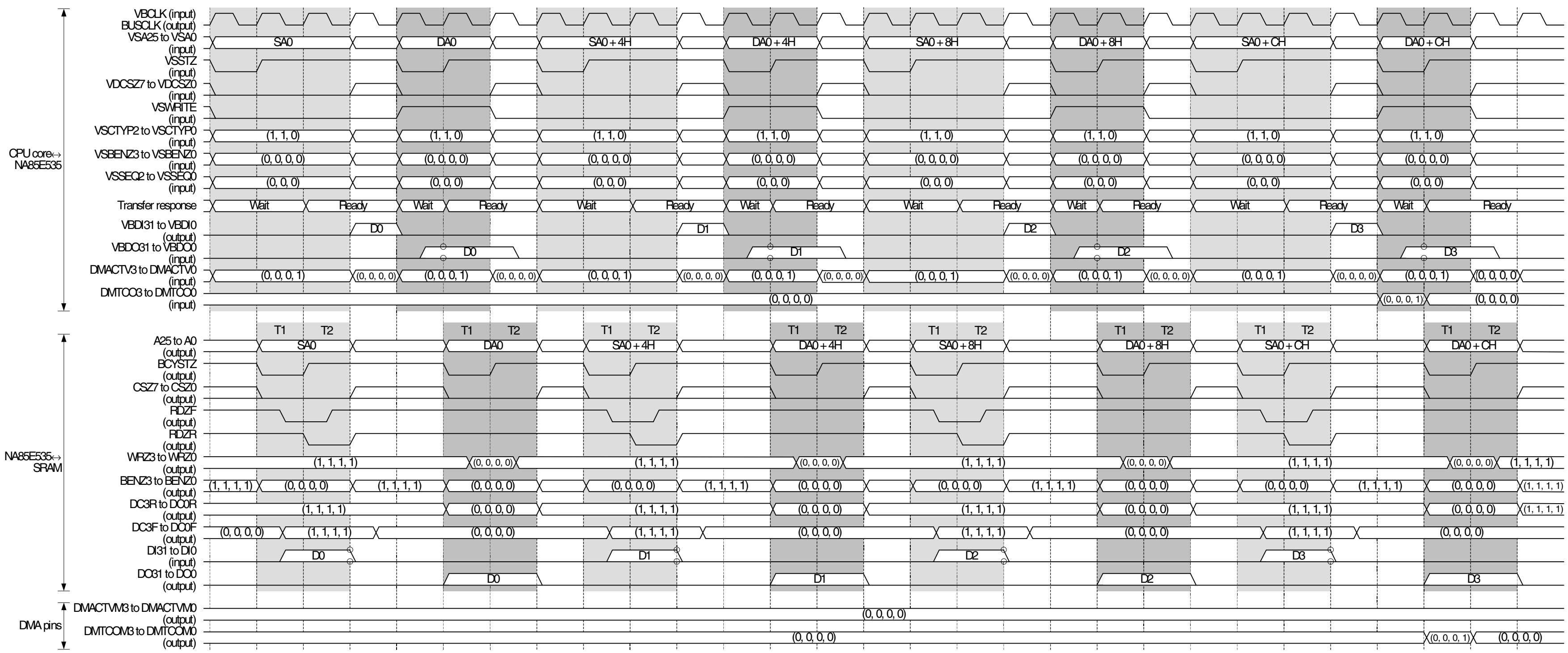
★Figure 4-14. Example of DMA Transfer Timing (2-Cycle Transfer (Using DMAC with On-Chip CPU Core): SRAM → SRAM) (2/5)

(b) Block transfer/with speculative read/local bus size: 32 bits



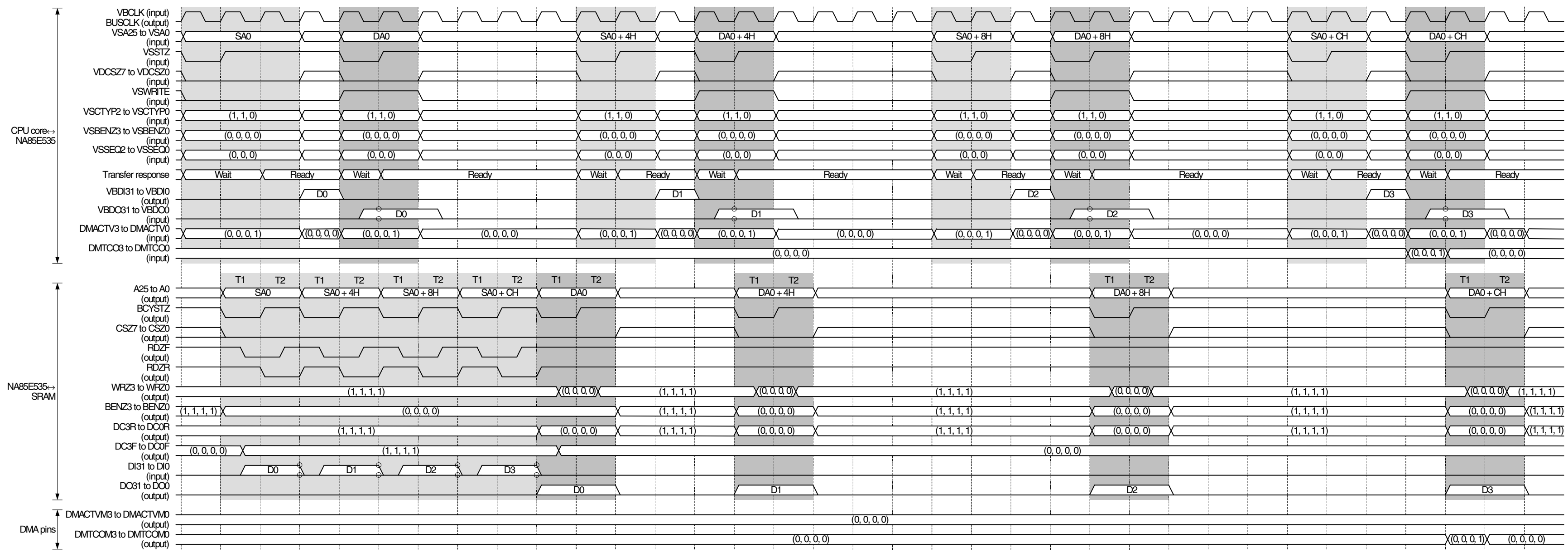
★**Figure 4-14. Example of DMA Transfer Timing (2-Cycle Transfer (Using DMAC with On-Chip CPU Core): SRAM → SRAM) (3/5)**

(c) Block transfer/without speculative read/local bus size: 32 bits



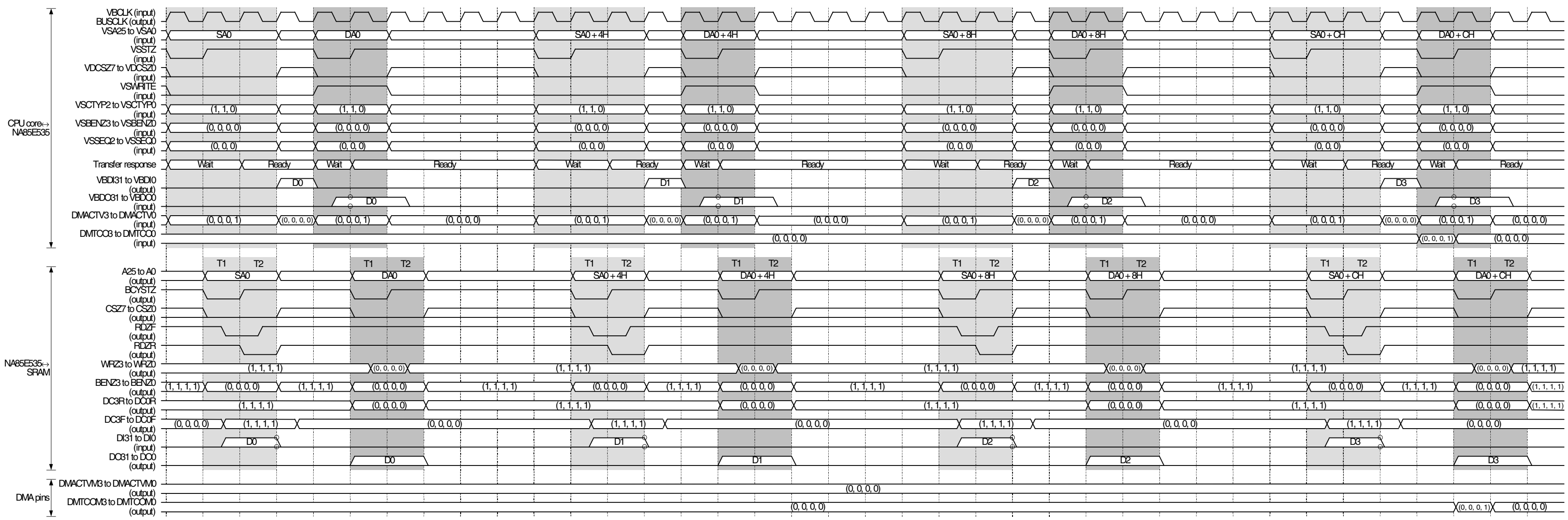
★Figure 4-14. Example of DMA Transfer Timing (2-Cycle Transfer (Using DMAC with On-Chip CPU Core): SRAM → SRAM) (4/5)

(d) Line transfer/with speculative read/local bus size: 32 bits



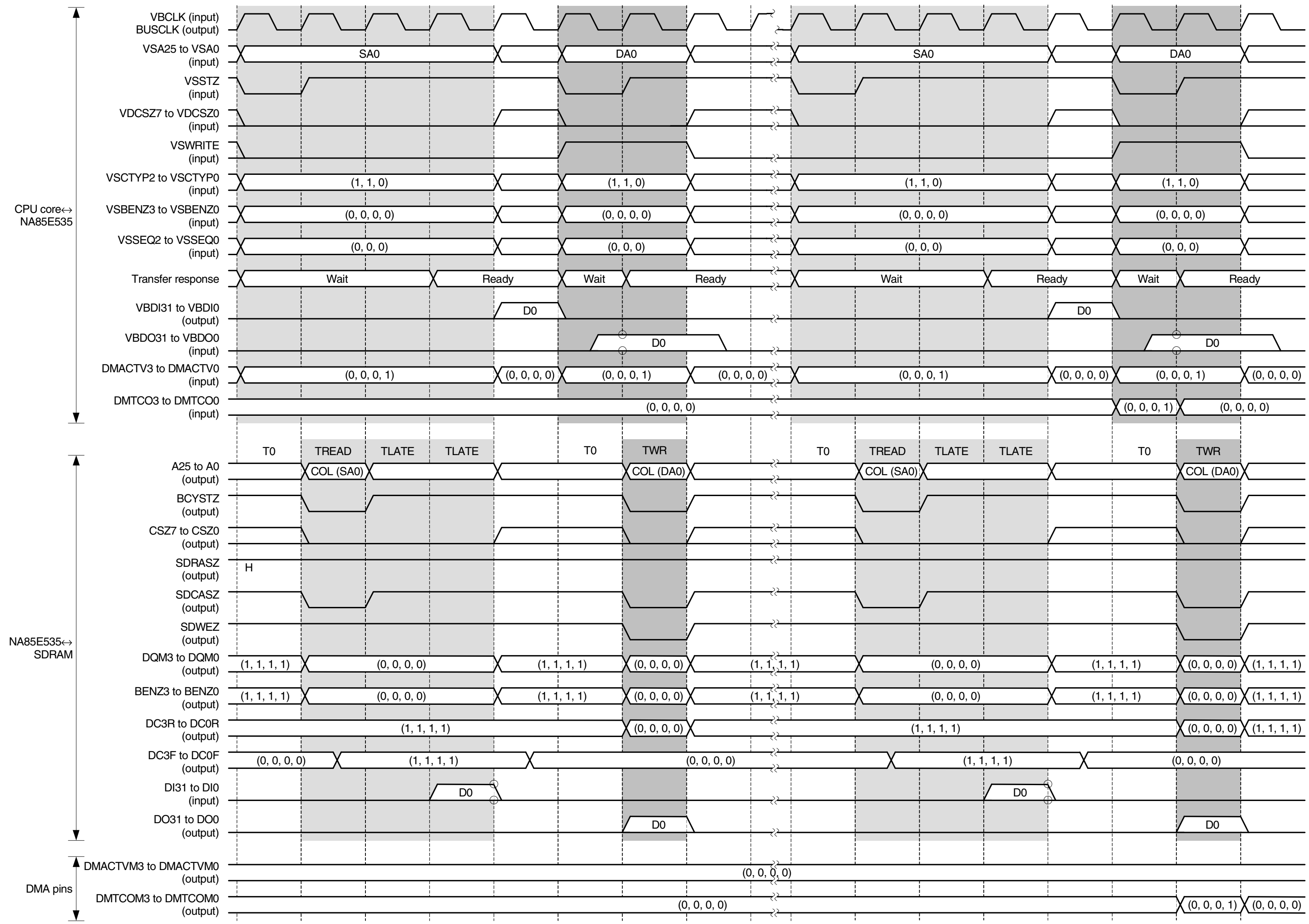
★Figure 4-14. Example of DMA Transfer Timing (2-Cycle Transfer (Using DMAC with On-Chip CPU Core): SRAM → SRAM) (5/5)

(e) Line transfer/without speculative read/local bus size: 32 bits



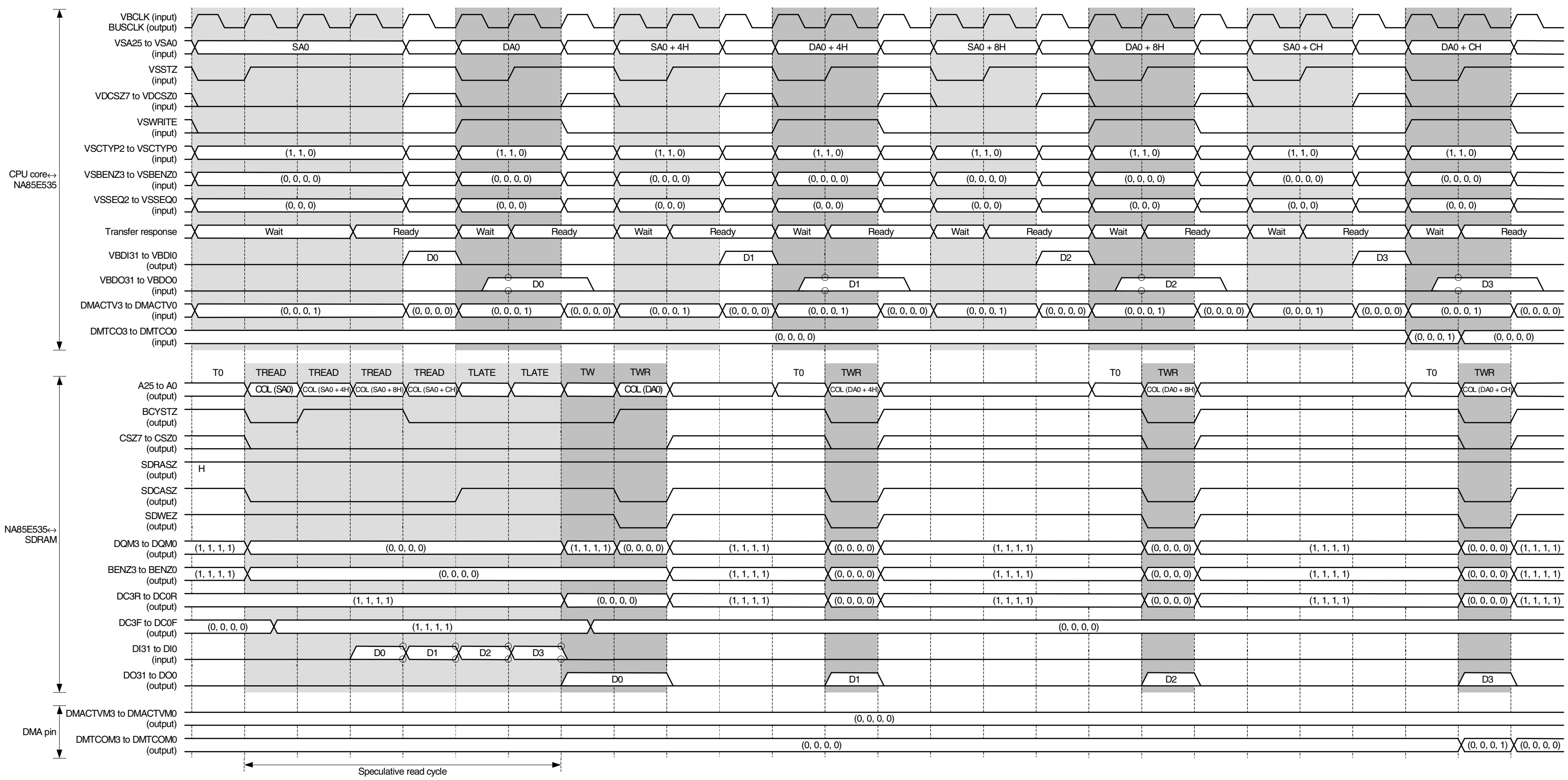
★Figure 4-15. Example of DMA Transfer Timing (2-Cycle Transfer (Using DMAC with On-Chip CPU Core): SDRAM → SDRAM) (1/5)

(a) Single transfer/without wait/CL = 2/without speculative read/local bus size: 32 bits



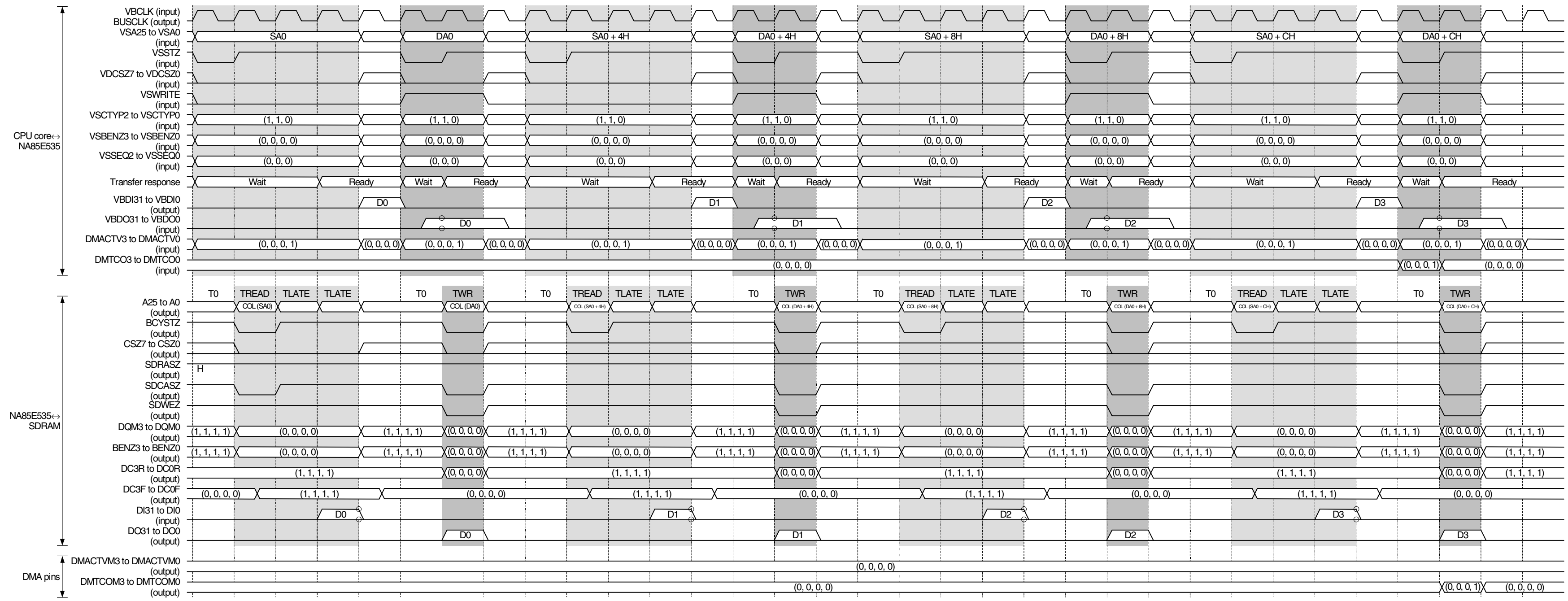
★Figure 4-15. Example of DMA Transfer Timing (2-Cycle Transfer (Using DMAC with On-Chip CPU Core): SDRAM → SDRAM) (2/5)

(b) Block transfer/with speculative read/local bus size: 32 bits



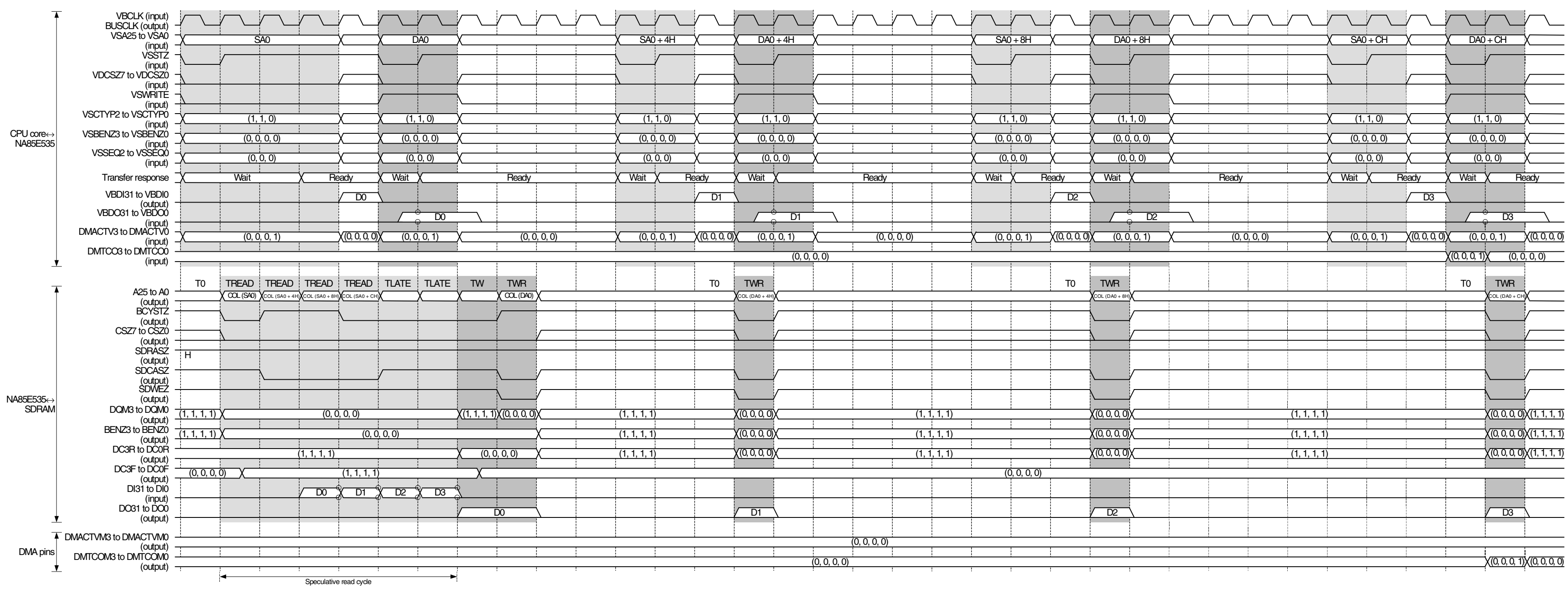
★Figure 4-15. Example of DMA Transfer Timing (2-Cycle Transfer (Using DMAC with On-Chip CPU Core): SDRAM → SDRAM) (3/5)

(c) Block transfer/without speculative read/local bus size: 32 bits



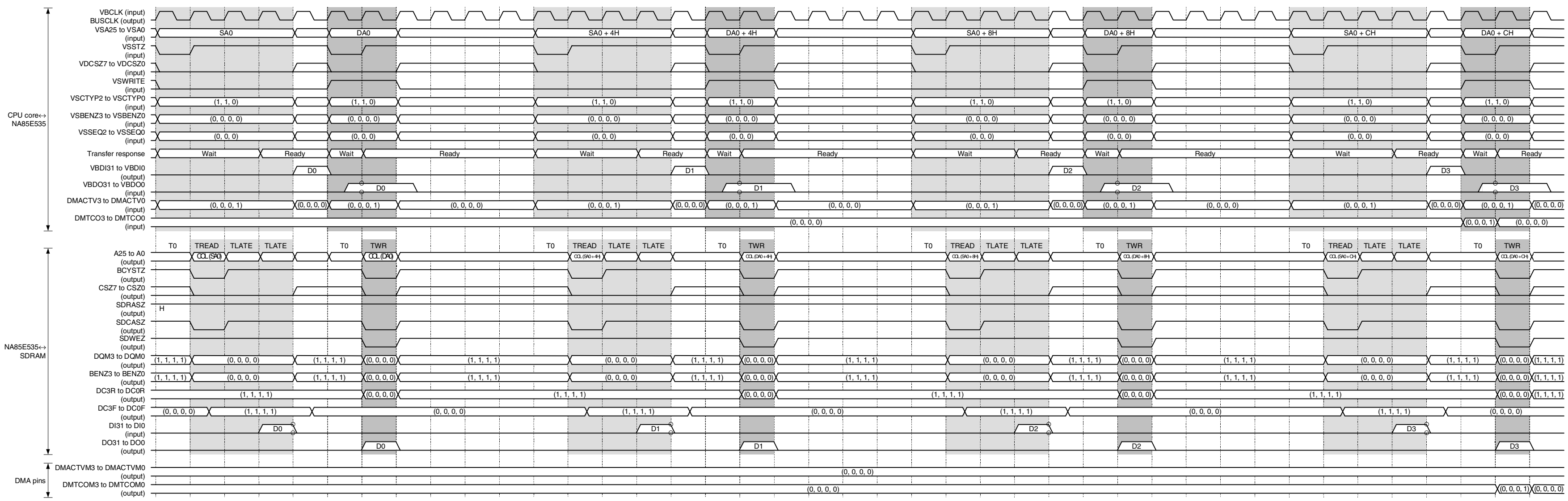
★Figure 4-15. Example of DMA Transfer Timing (2-Cycle Transfer (Using DMAC with On-Chip CPU Core): SDRAM → SDRAM) (4/5)

(d) Line transfer/with speculative read/local bus size: 32 bits

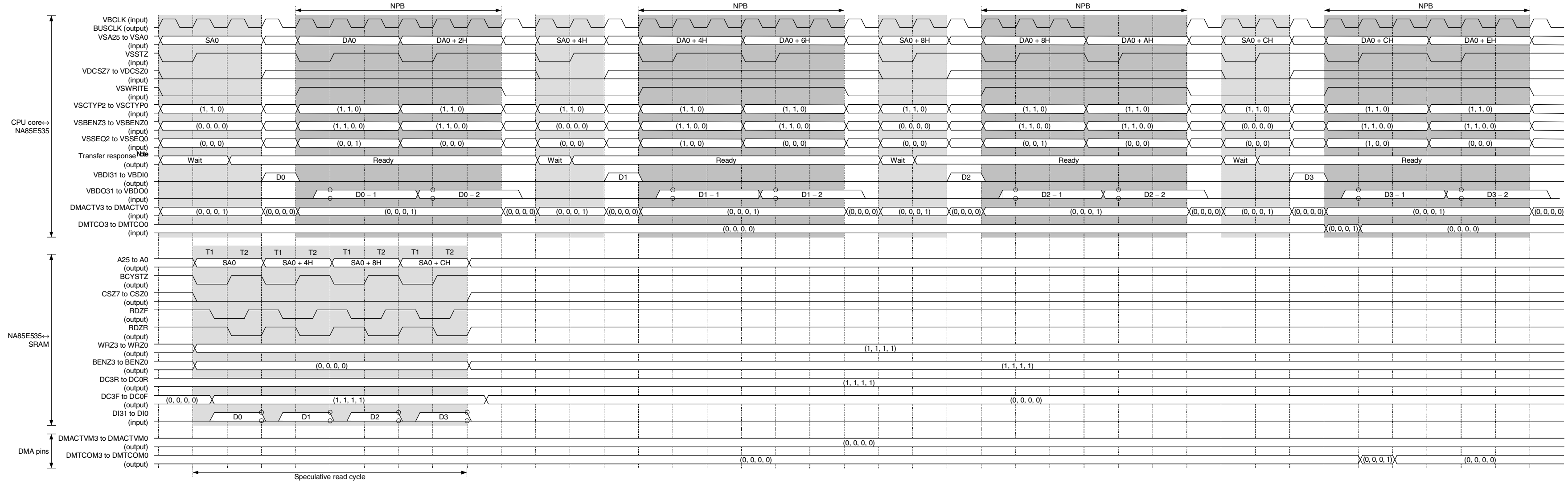


★Figure 4-15. Example of DMA Transfer Timing (2-Cycle Transfer (Using DMAC with On-Chip CPU Core): SDRAM → SDRAM) (5/5)

(e) Line transfer/without speculative read/local bus size: 32 bits

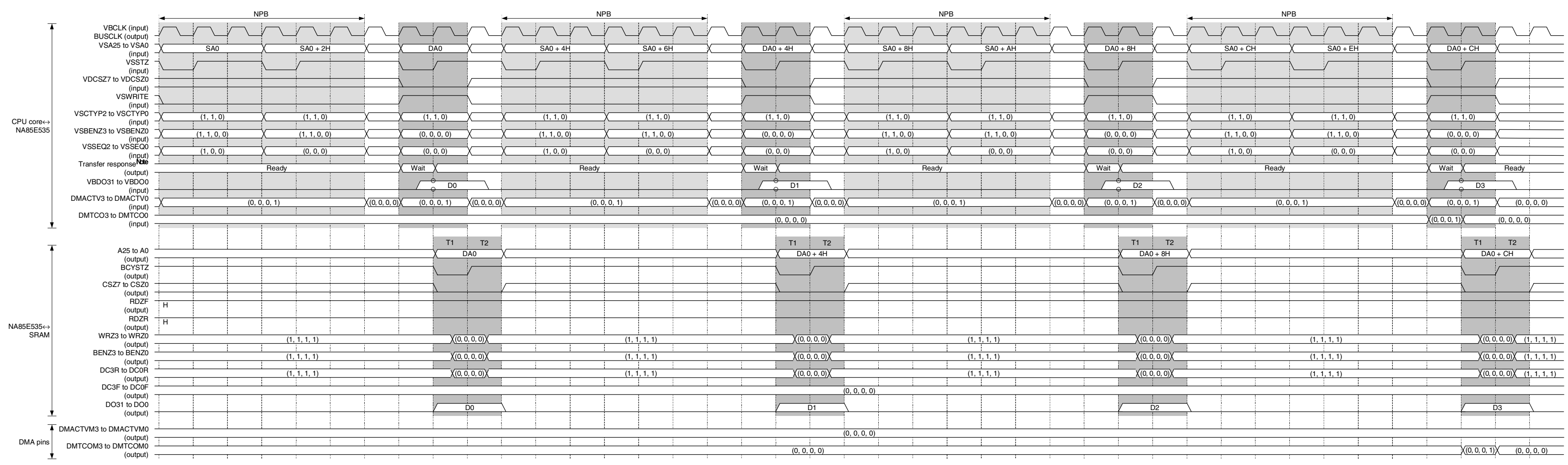


★**Figure 4-16. Example of DMA Transfer Timing (2-Cycle Transfer (Using DMAC with On-Chip CPU Core): SRAM → NPB (Single Transfer/with Speculative Read/Local Bus Size: 32 Bits))**



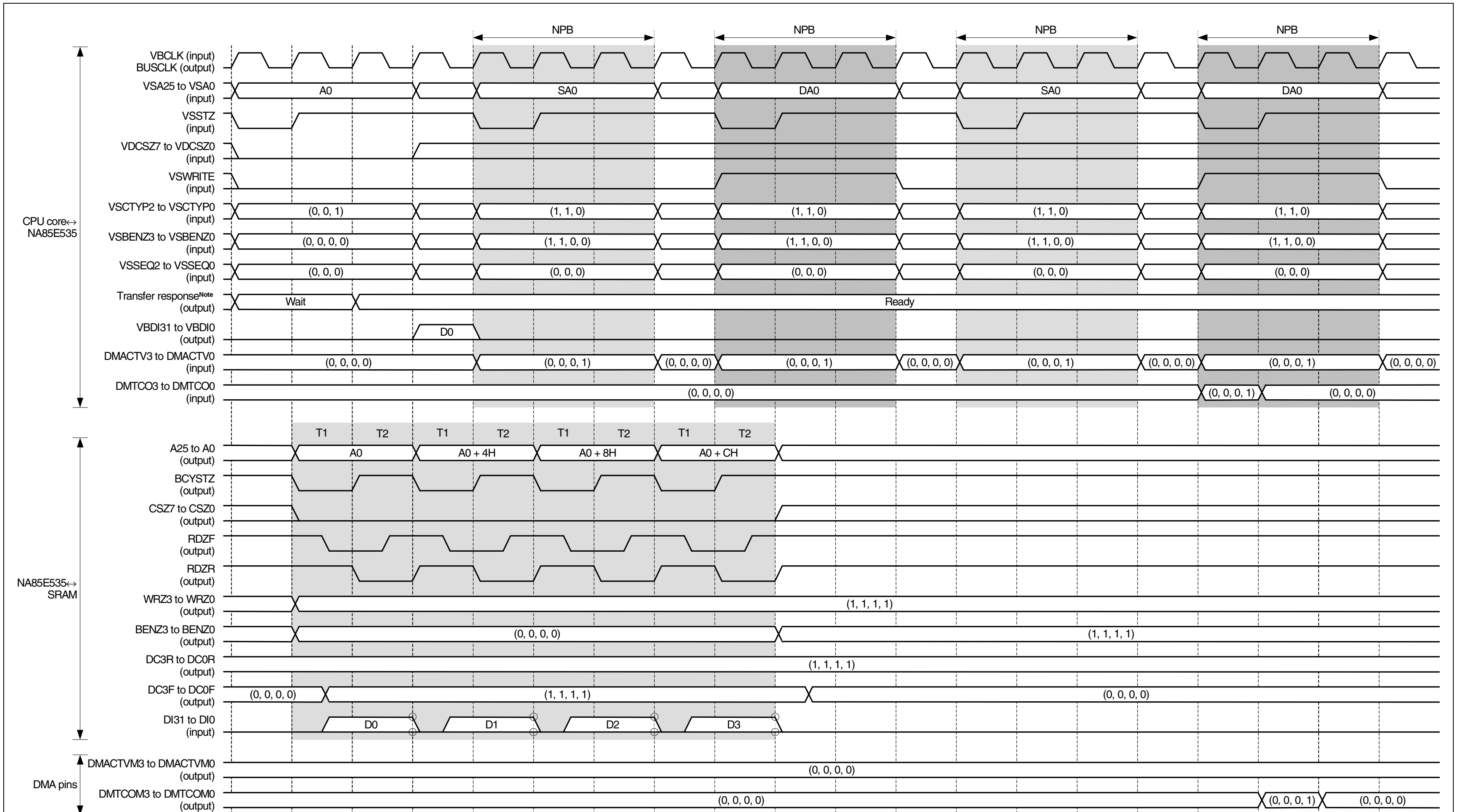
Note Transfer response output by NA85E535

★Figure 4-17. Example of DMA Transfer Timing (2-Cycle Transfer (Using DMAC with On-Chip CPU Core): NPB → SRAM (Single Transfer/Local Bus Size: 32 Bits))



Note Transfer response output by NA85E535

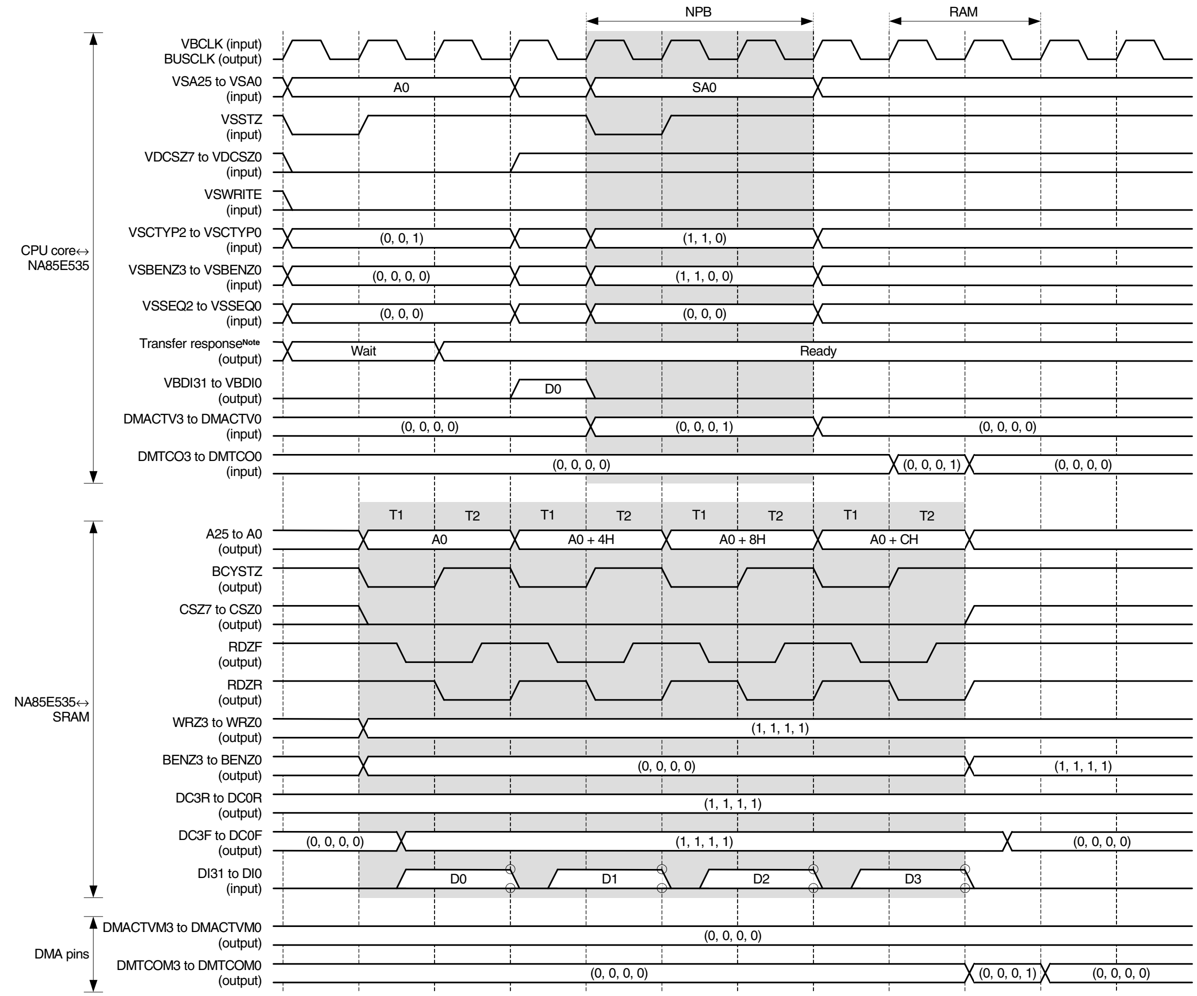
★Figure 4-18. Example of DMA Transfer Timing (2-Cycle Transfer (Using DMAC with On-Chip CPU Core): NPB → NPB (Single Transfer/During Speculative Read/Local Bus Size: 32 Bits))



Note Transfer response output by NA85E535

Remark The 2-cycle transfer of NPB → NPB is executed regardless of an external memory access by the NA85E535.

★Figure 4-19. Example of DMA Transfer Timing (2-Cycle Transfer (Using DMAC with On-Chip CPU Core): NPB → RAM (Single Transfer/During Speculative Read/Local Bus Size: 32 Bits))

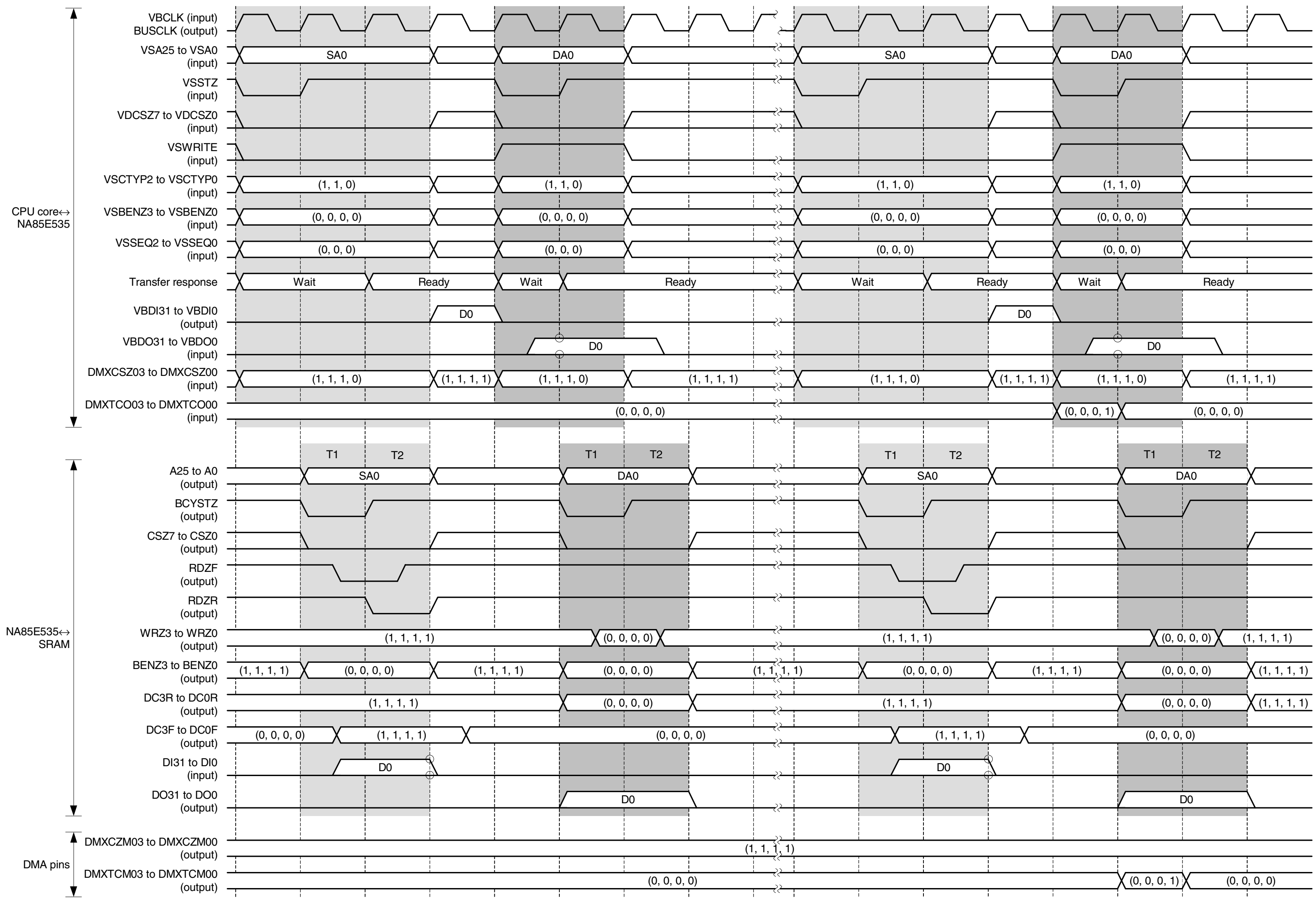


Note Transfer response output by NA85E535

Remark The 2-cycle transfer of NPB → RAM is executed regardless of an external memory access by the NA85E535.

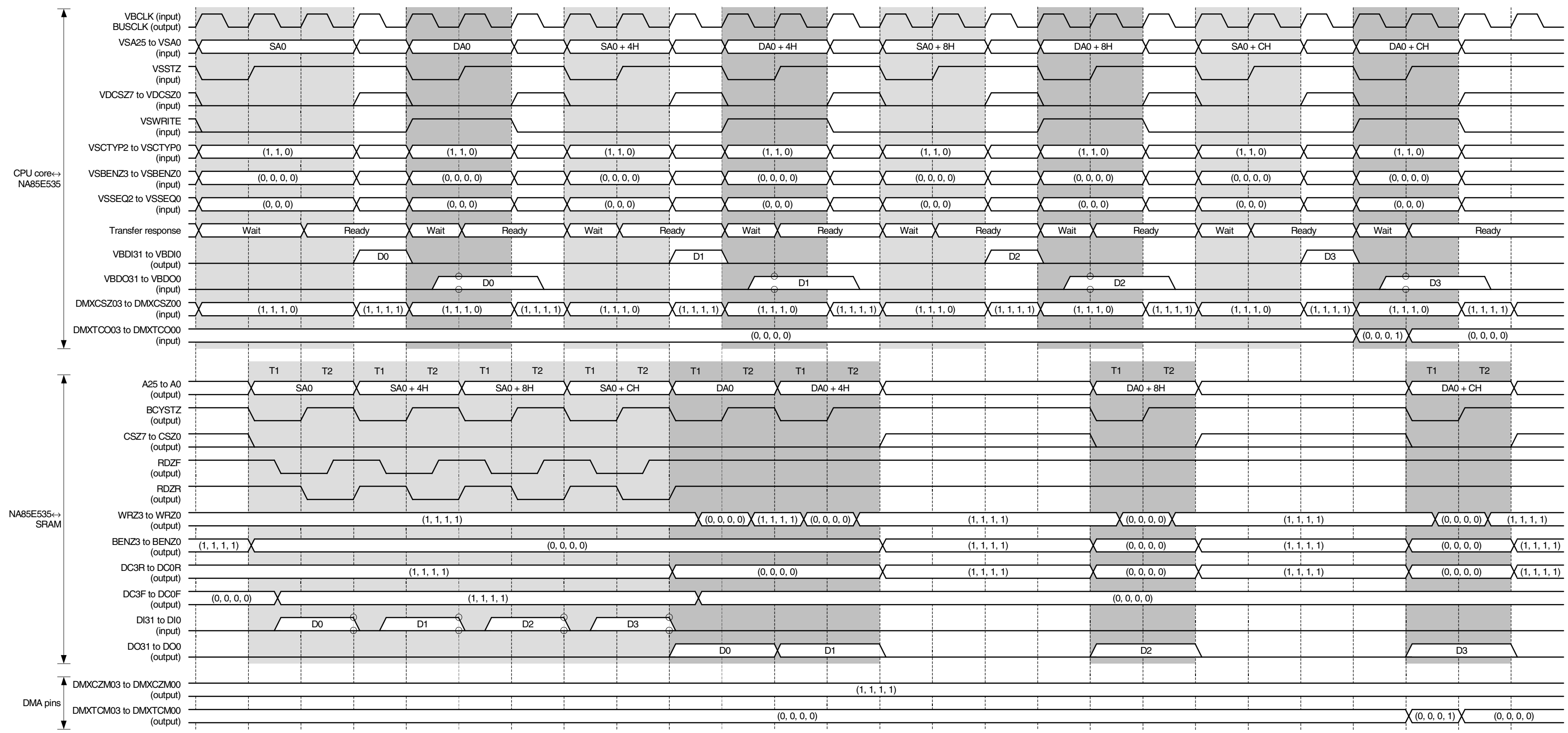
★Figure 4-20. Example of DMA Transfer Timing (2-Cycle Transfer (with NA85E300): SRAM → SRAM) (1/5)

(a) Single transfer/without wait/without speculative read/local bus size: 32 bits



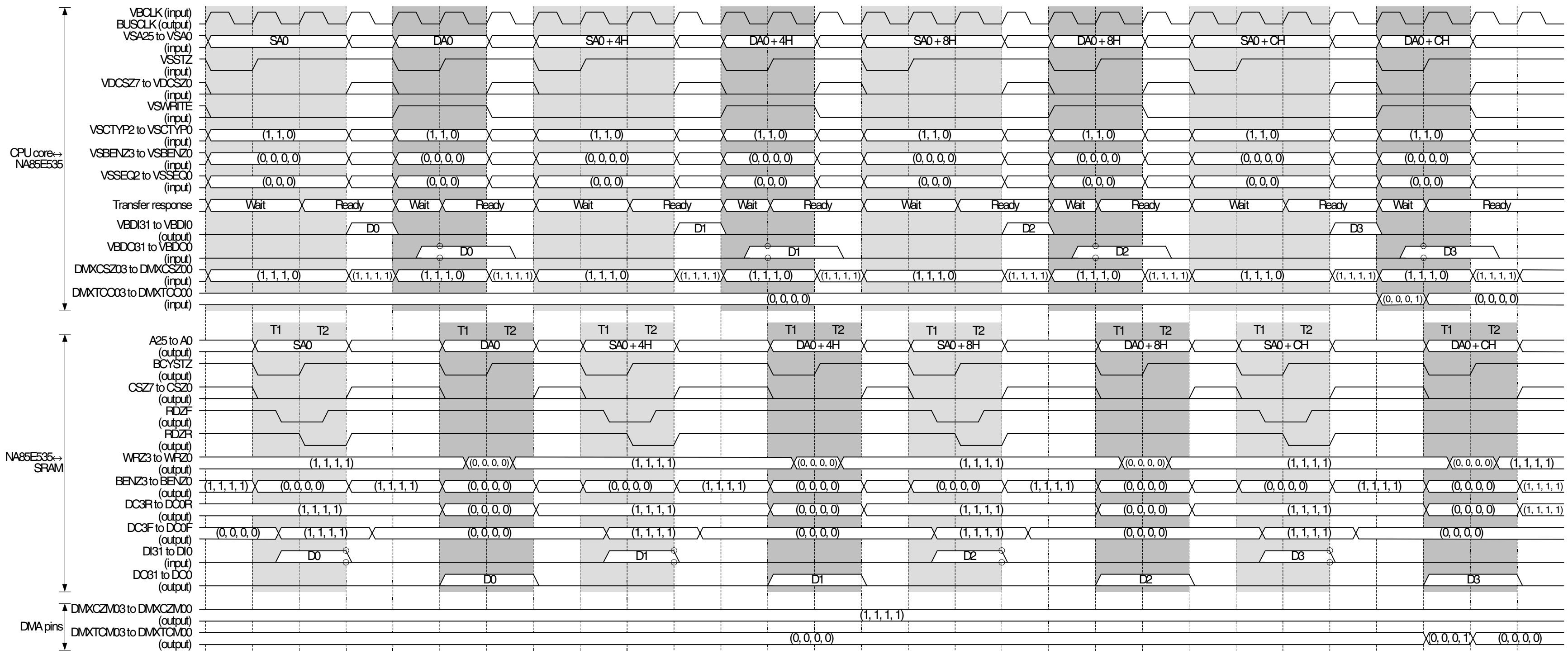
★Figure 4-20. Example of DMA Transfer Timing (2-Cycle Transfer (with NA85E300): SRAM → SRAM) (2/5)

(b) Block transfer/with speculative read/local bus size: 32 bits



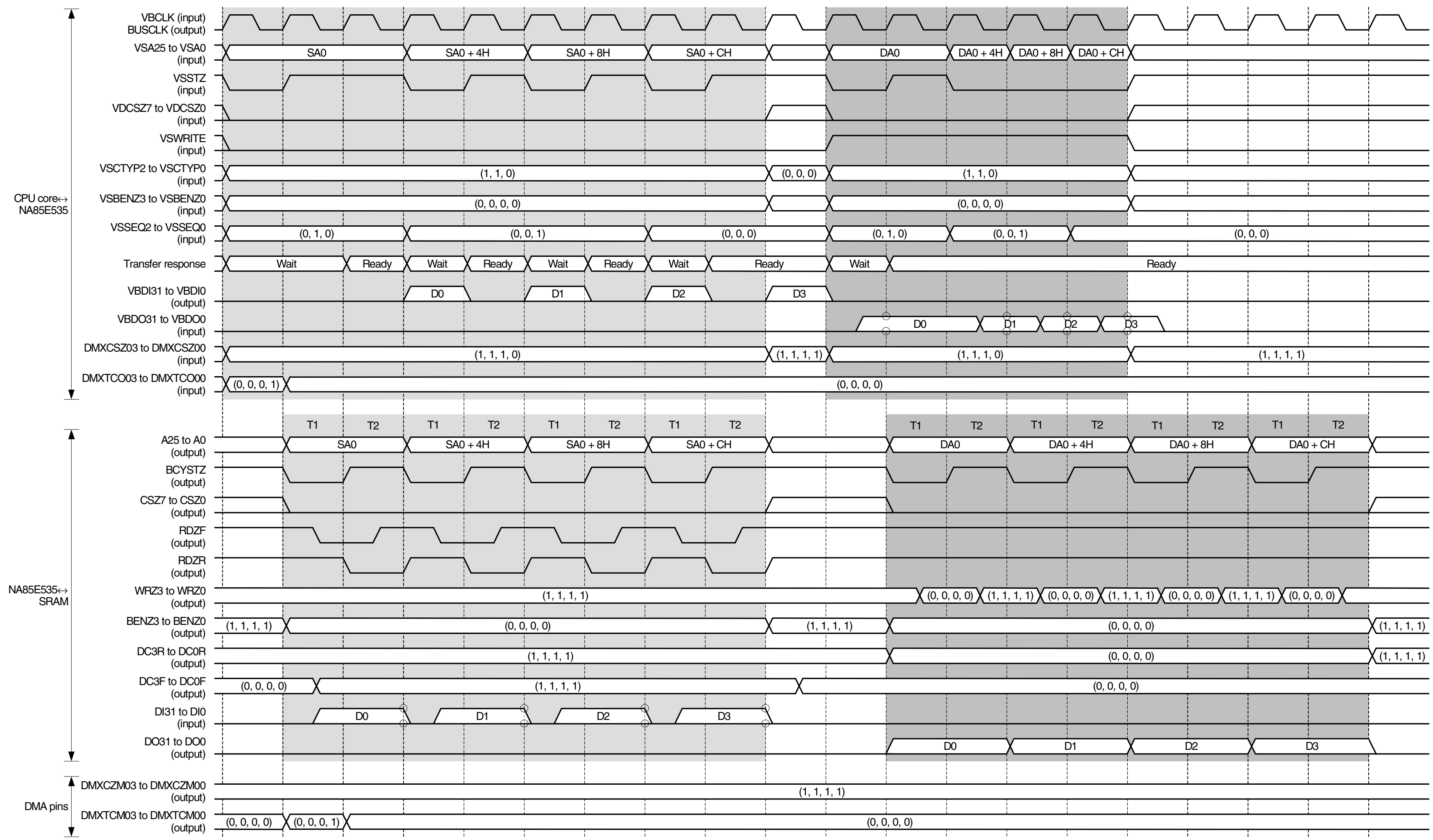
★Figure 4-20. Example of DMA Transfer Timing (2-Cycle Transfer (with NA85E300): SRAM → SRAM) (3/5)

(c) Block transfer/without speculative read/local bus size: 32 bits



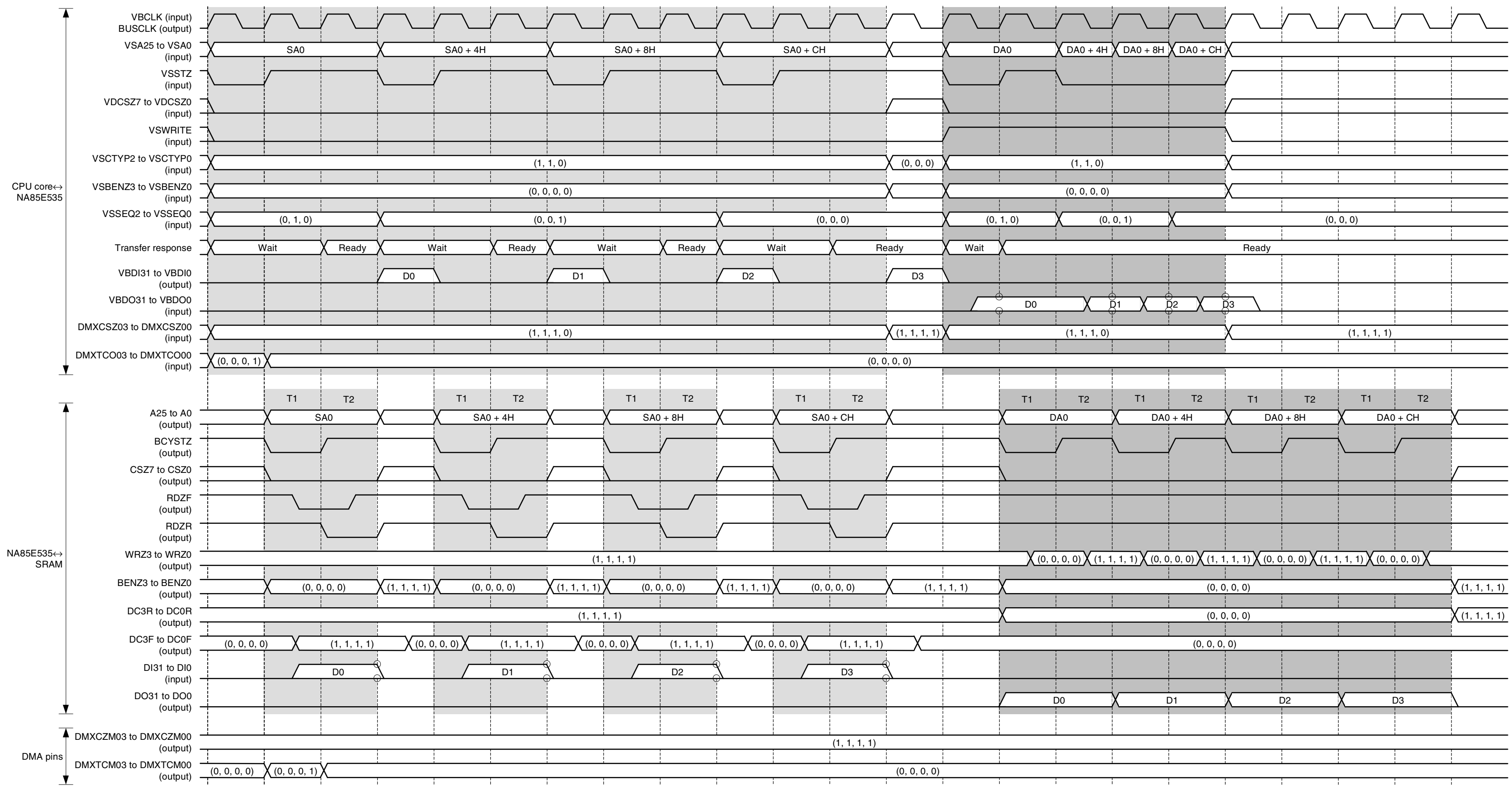
★Figure 4-20. Example of DMA Transfer Timing (2-Cycle Transfer (with NA85E300): SRAM → SRAM) (4/5)

(d) Single transfer (4 word)/with speculative read/local bus size: 32 bits



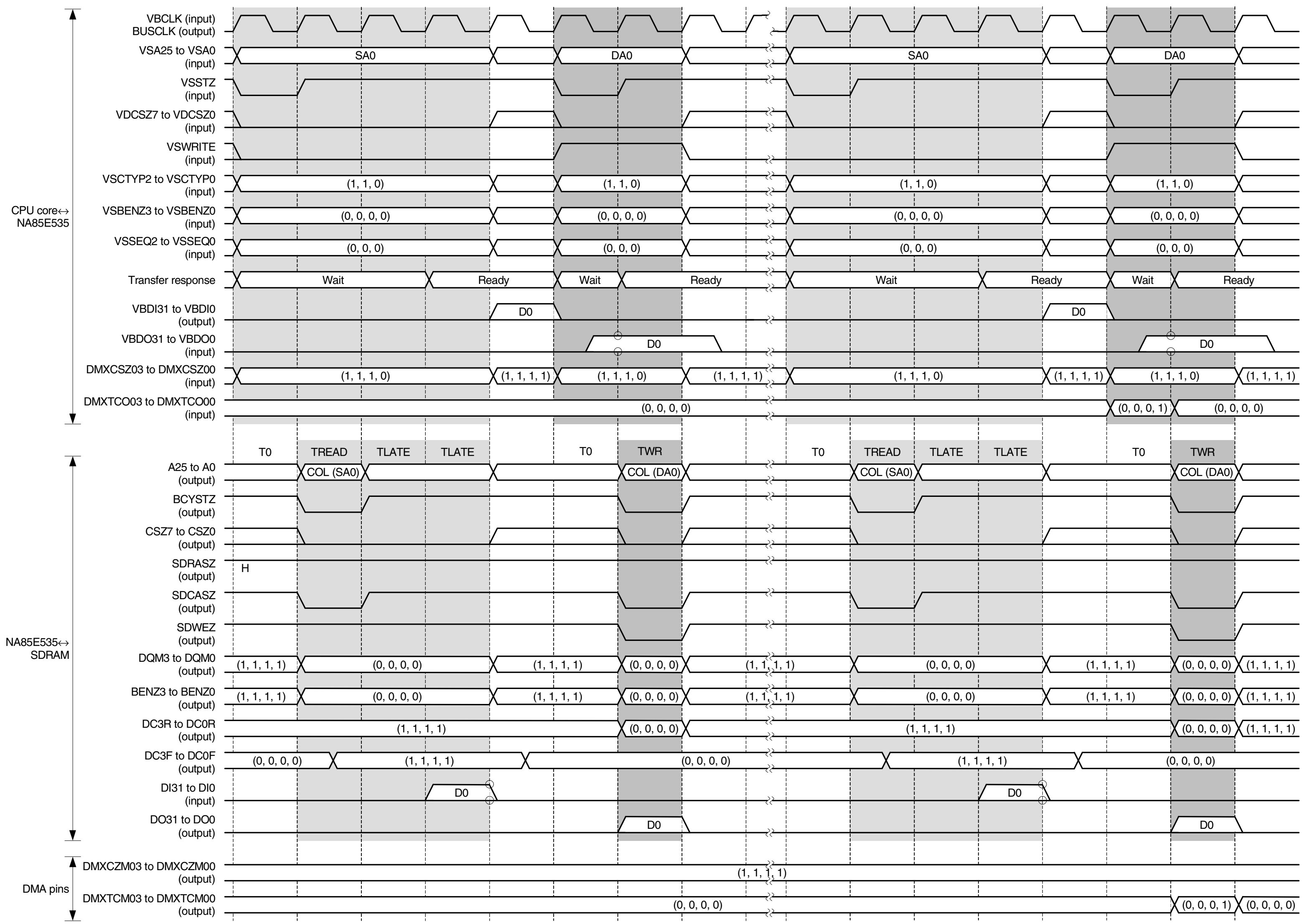
★Figure 4-20. Example of DMA Transfer Timing (2-Cycle Transfer (with NA85E300): SRAM → SRAM) (5/5)

(e) Single transfer (4 word)/without speculative read/local bus size: 32 bits



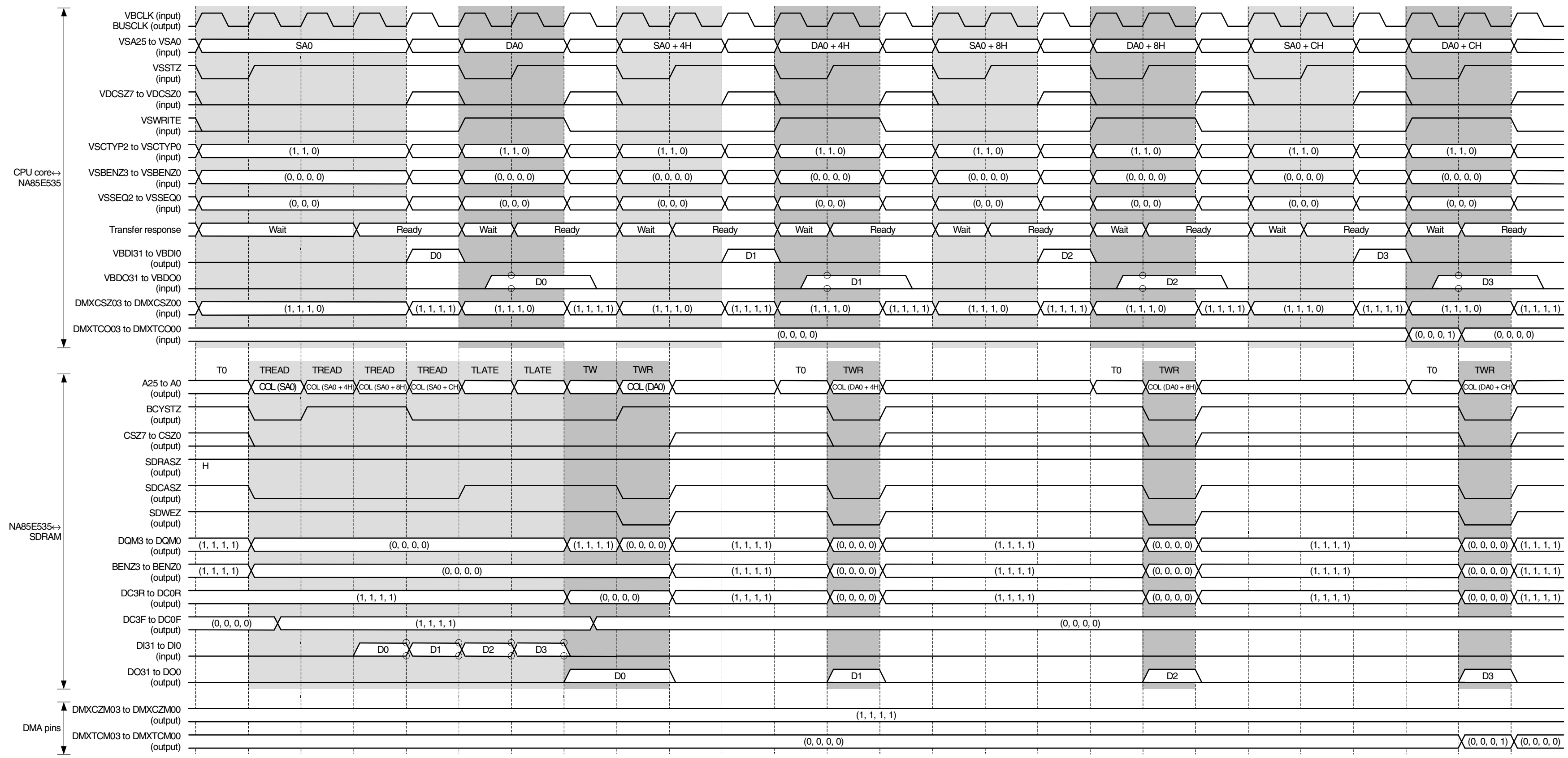
★Figure 4-21. Example of DMA Transfer Timing (2-Cycle Transfer (with NA85E300): SDRAM → SDRAM) (1/5)

(a) Single transfer/without wait/CL = 2/without speculative read/local bus size: 32 bits



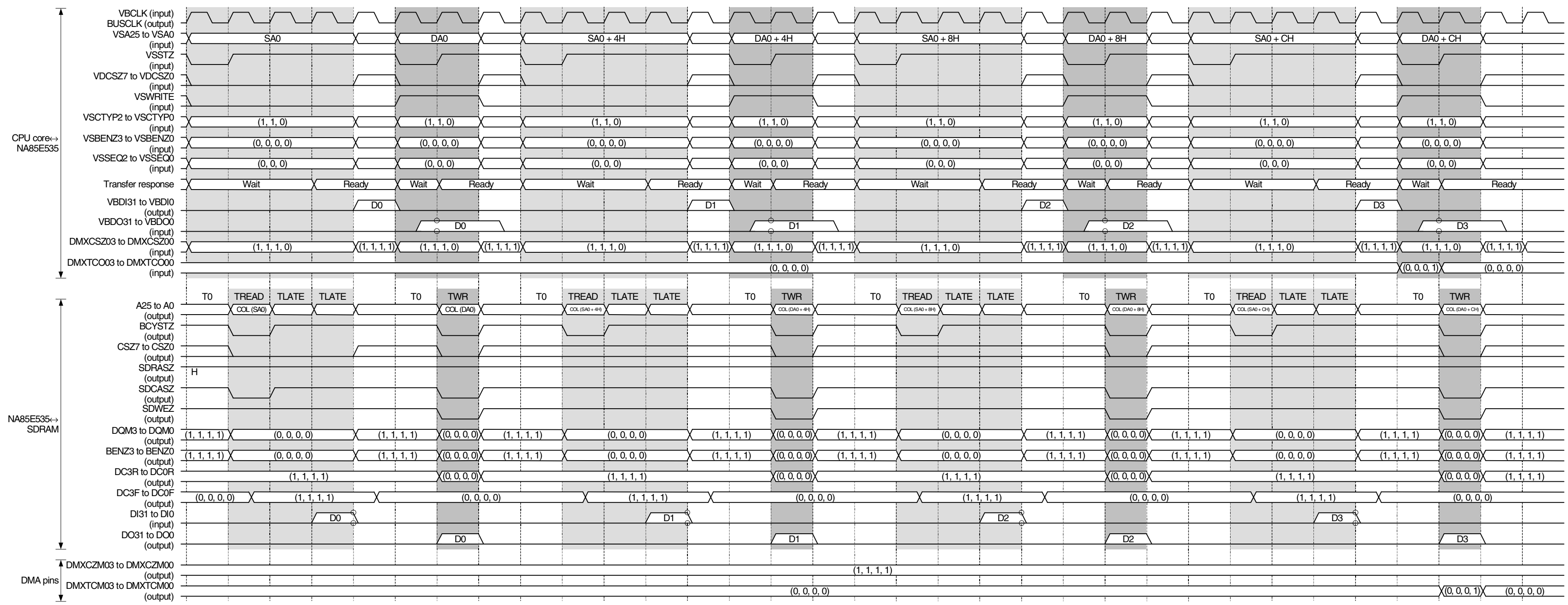
★**Figure 4-21. Example of DMA Transfer Timing (2-Cycle Transfer (with NA85E300): SDRAM → SDRAM) (2/5)**

(b) Block transfer/with speculative read/local bus size: 32 bits



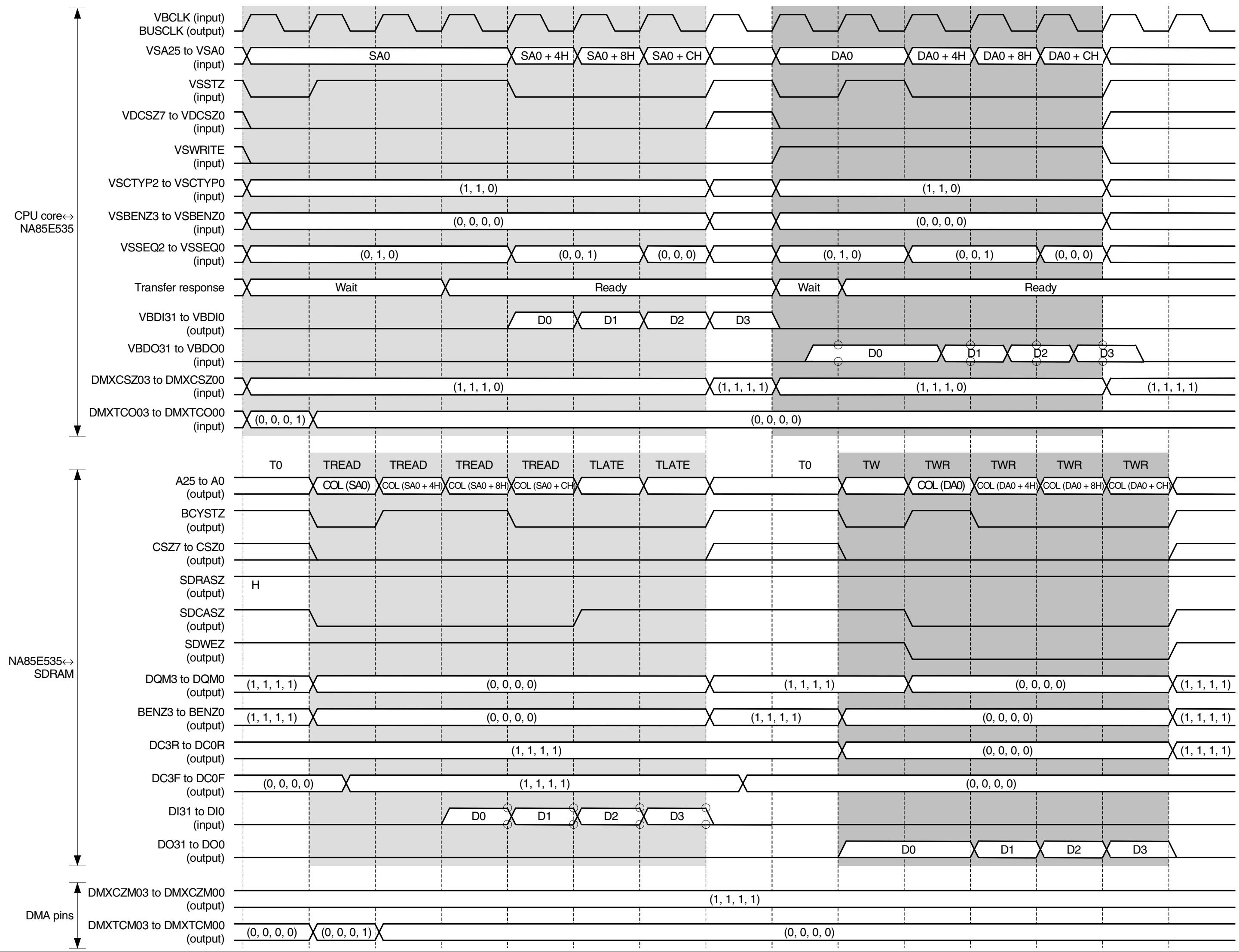
★Figure 4-21. Example of DMA Transfer Timing (2-Cycle Transfer (with NA85E300): SDRAM → SDRAM) (3/5)

(c) Block transfer/without speculative read/local bus size: 32 bits



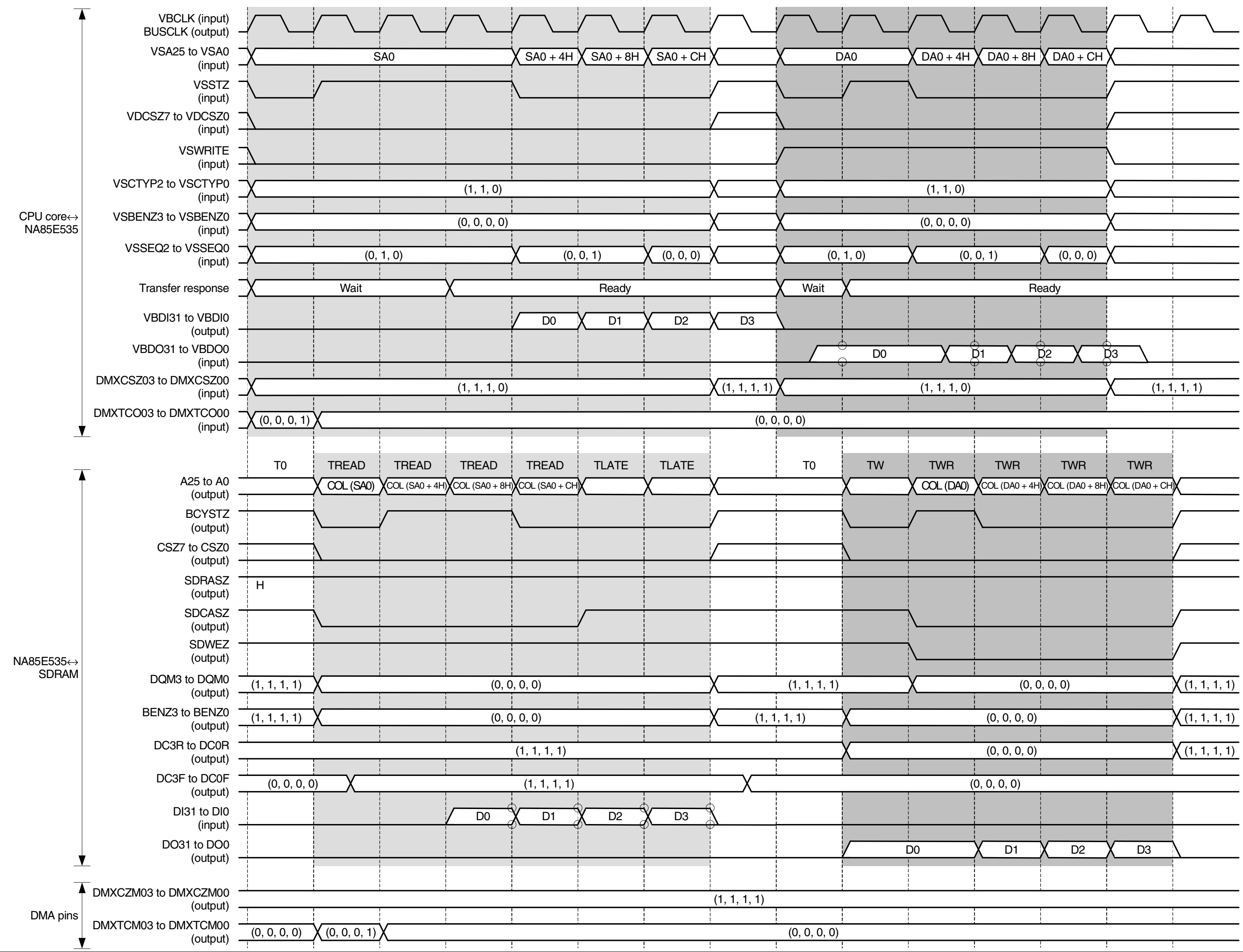
★Figure 4-21. Example of DMA Transfer Timing (2-Cycle Transfer (with NA85E300): SDRAM → SDRAM) (4/5)

(d) Single transfer (4 words)/with speculative read/local bus size: 32 bits

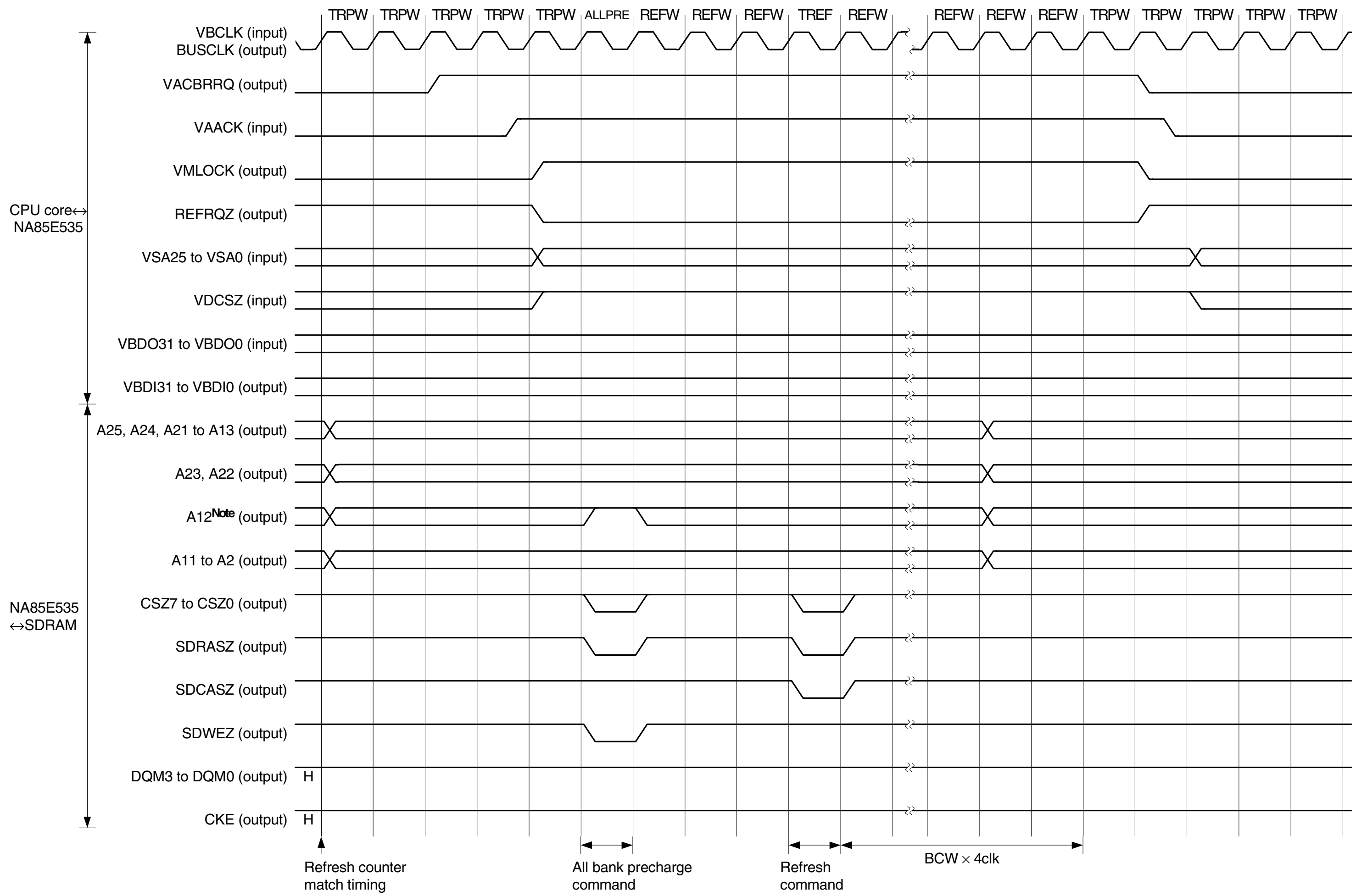


★Figure 4-21. Example of DMA Transfer Timing (2-Cycle Transfer (with NA85E300): SDRAM → SDRAM) (5/5)

(e) Single transfer (4 words)/without speculative read/local bus size: 32 bits



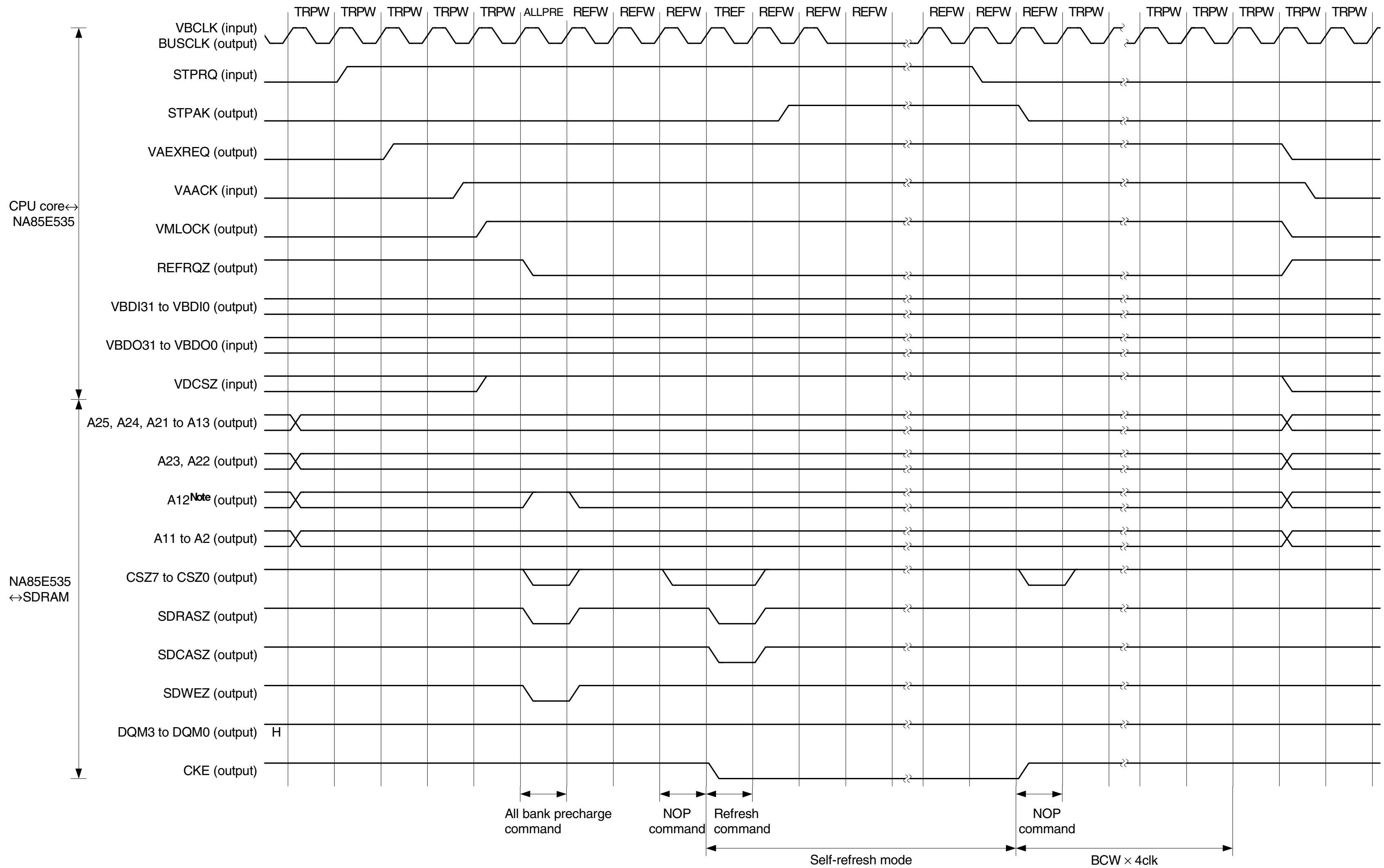
★Figure 4-22. SDRAM CBR Refresh Timing



Note This is the case where the local bus size is 32 bits. Read the local bus size of 16 bits or 8 bits as "A11" or "A10", respectively.

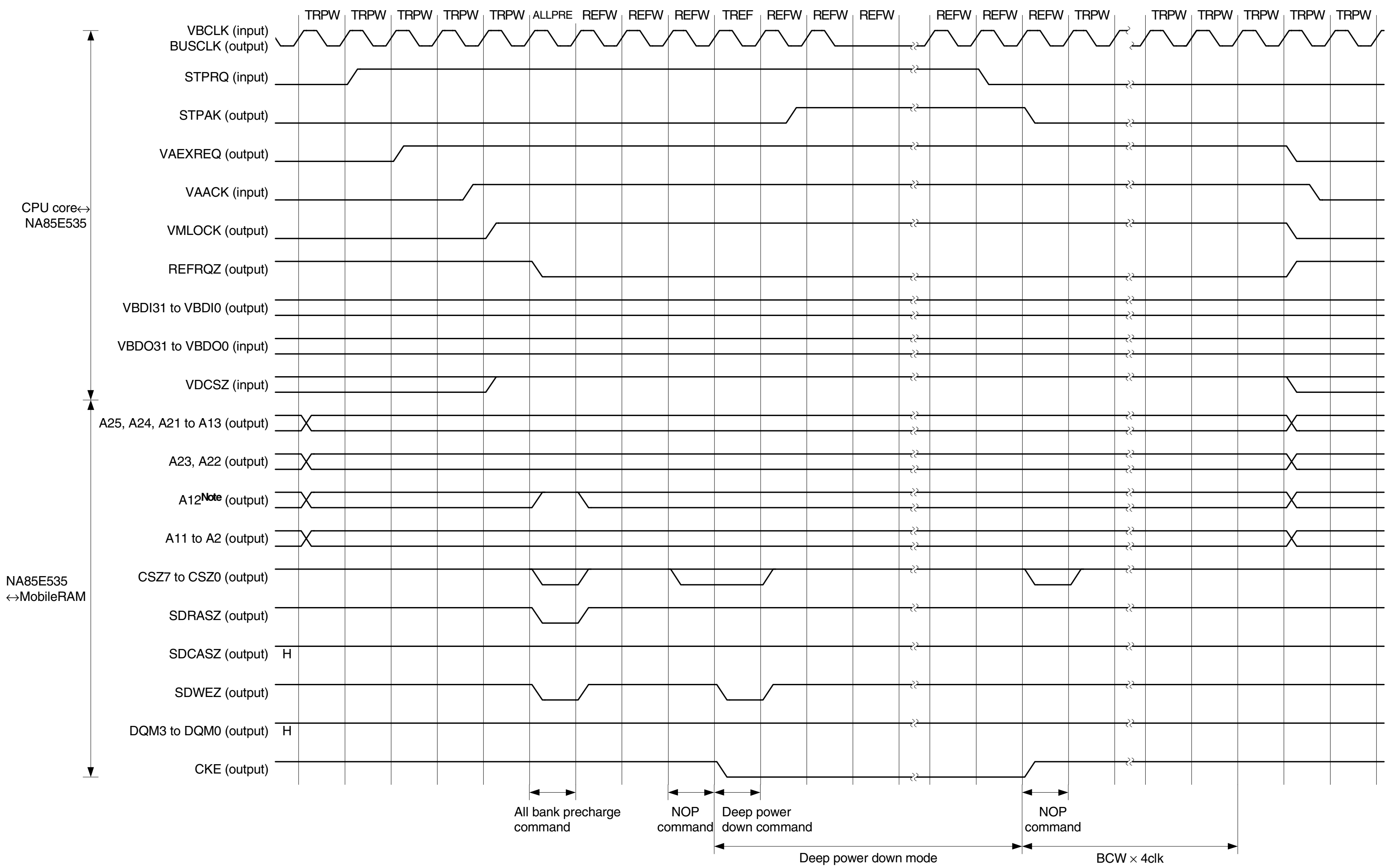
Remark A TRPW state is inserted while the NA85E535 is waiting for generation of a cycle. If no cycle is generated, the NA85E535 is always in the TRPW state. In Figures 4-22 and 4-23, it is in TRPW state while it is arbitrating the VSB.

★Figure 4-23. SDRAM Self-Refresh Timing (STOP Timing)



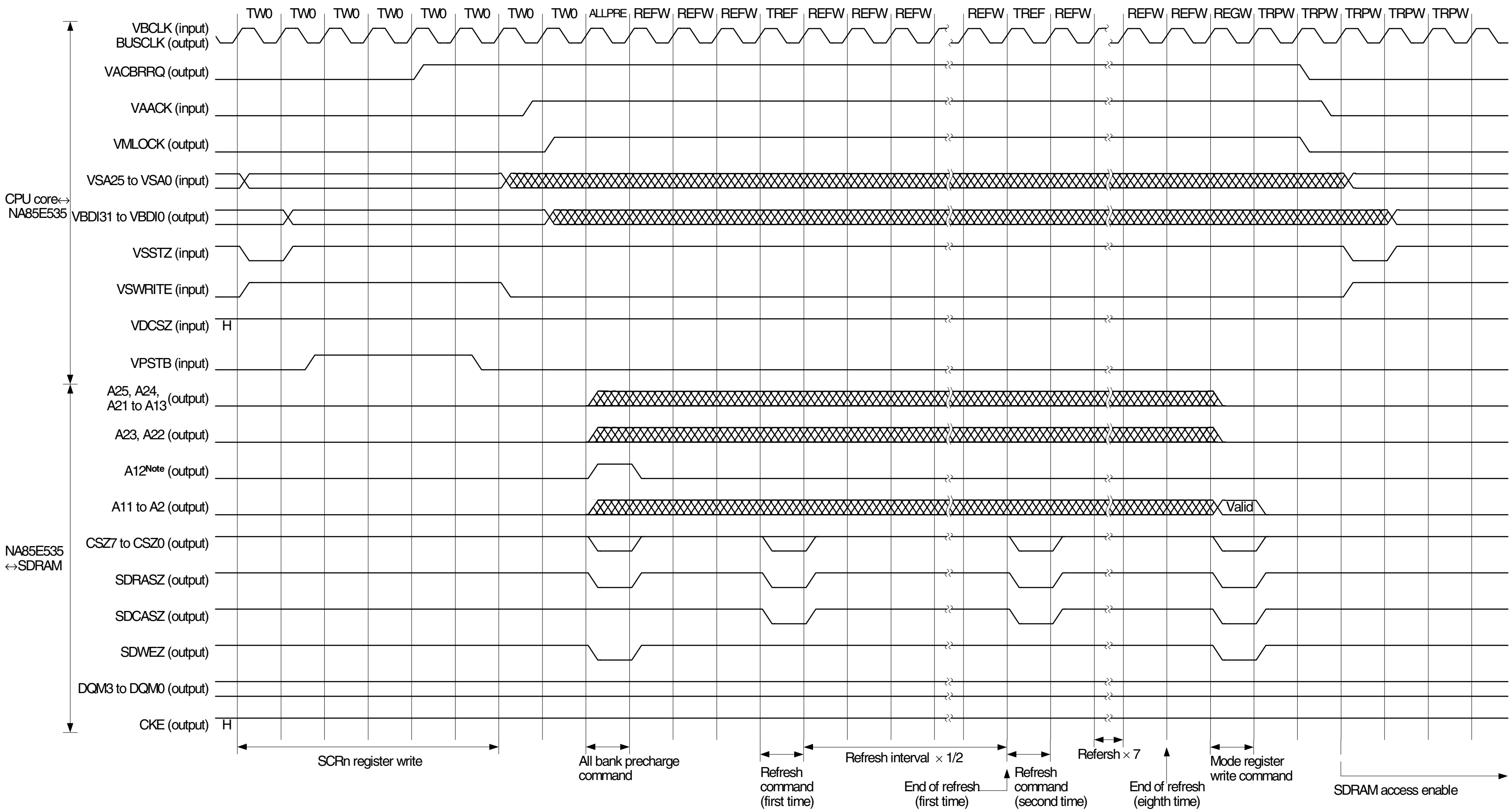
Note This is the case where the local bus size is 32 bits. Read the local bus size of 16 bits or 8 bits as “A11” or “A10”, respectively.

★Figure 4-24. MobileRAM Deep Power Down Timing (STOP Timing)



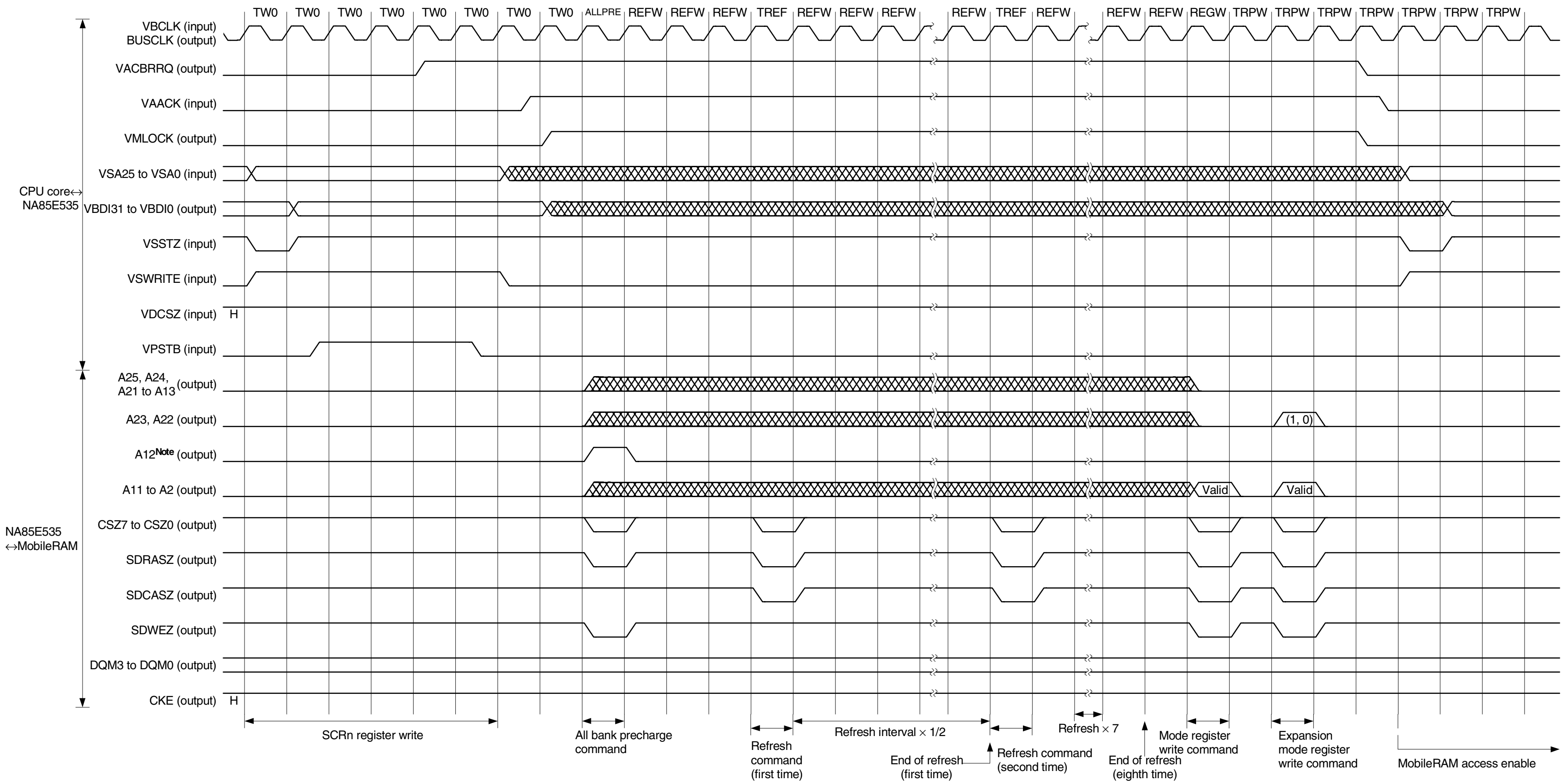
Note This is the case where the local bus size is 32 bits. Read the local bus size of 16 bits or 8 bits as “A11” or “A10”, respectively.

★Figure 4-25. SDRAM Mode Register Write Operation Timing



Note This is the case where the local bus size is 32 bits. Read the local bus size of 16 bits or 8 bits as “A11” or “A10”, respectively.

★Figure 4-26. MobileRAM Expansion Mode Register Write Timing



Note This is the case where the local bus size is 32 bits. Read the local bus size of 16 bits or 8 bits as “A11” or “A10”, respectively.

Figure 4-27. BMC Register Change Timing (Divided by 1 → Divided by 2)

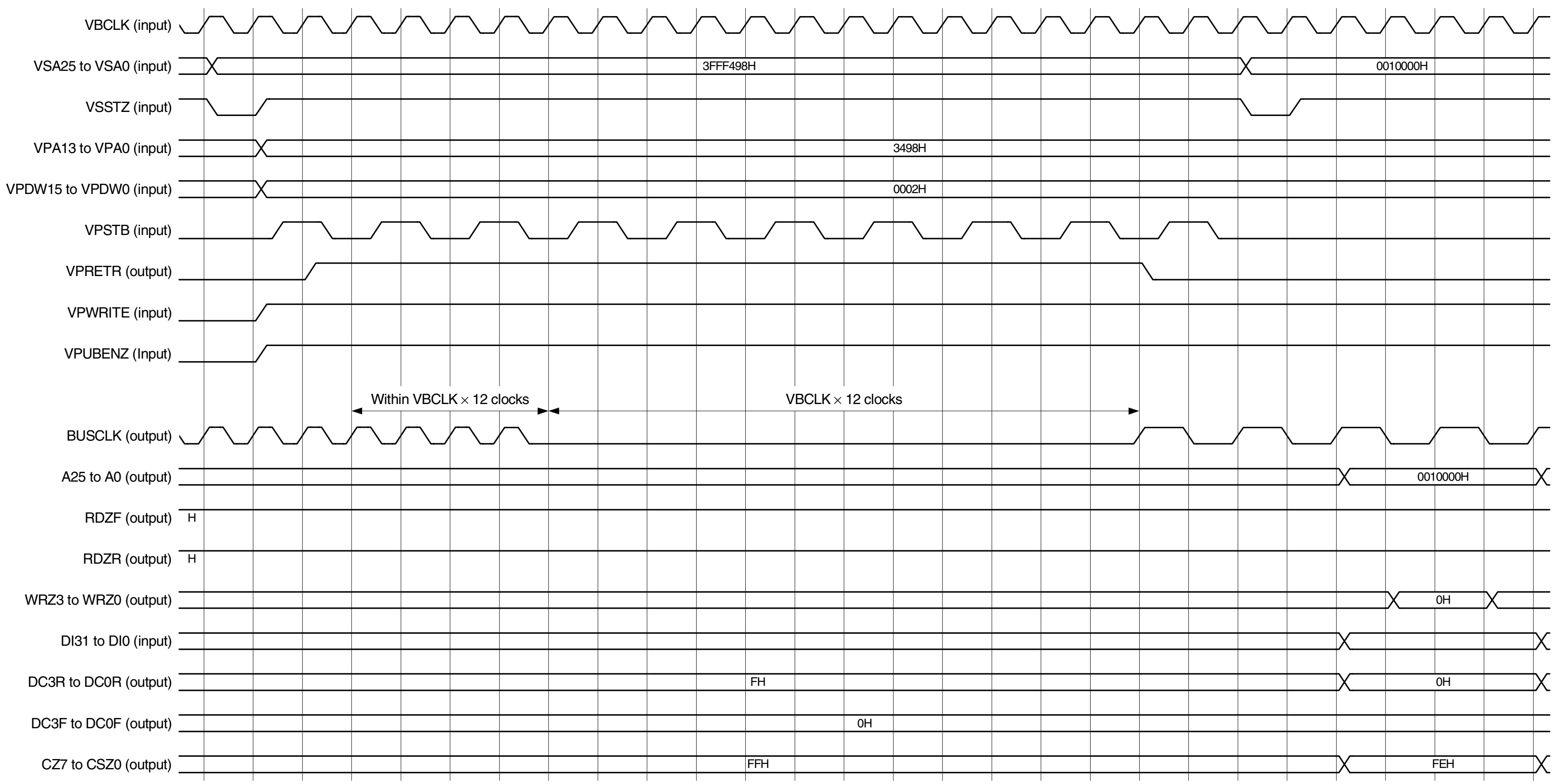
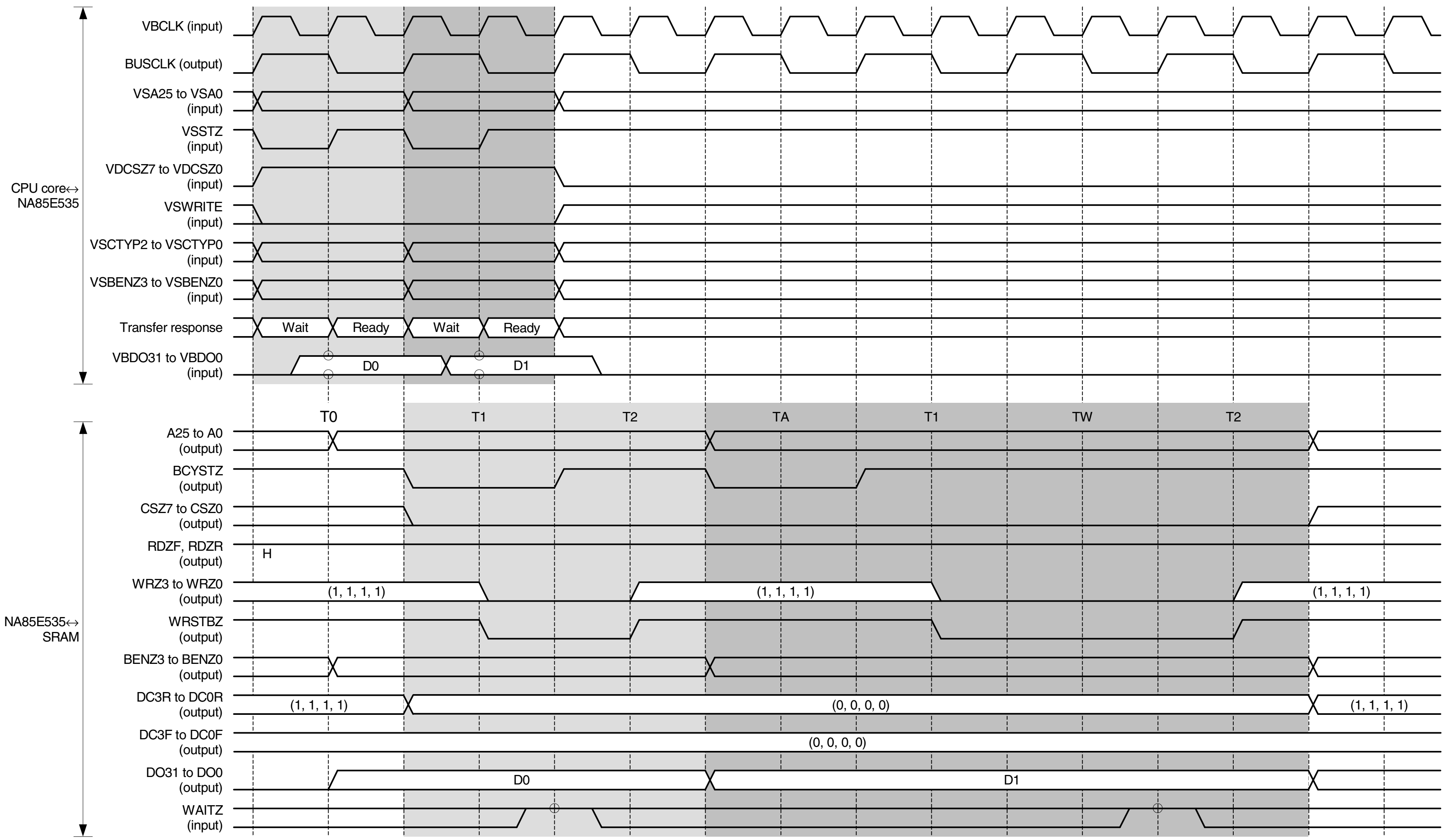


Figure 4-28. Example of SRAM Write Access Timing (If VBCLK Is Divided by Two to Generate BUSCLK)



Remark The output timing of the DO31 to DO0 signals differs compared with when the VBCLK signal is divided by one to generate BUSCLK.

5.1 Separate Unit Test

To test the internal circuitry of the NA85E535, set the separate unit test mode by inputting a high level to the TEST and BUNRI pins, and conduct the test by using the test input pins (TBI19 to TBI0) and test output pins (TBO15 to TBO0).

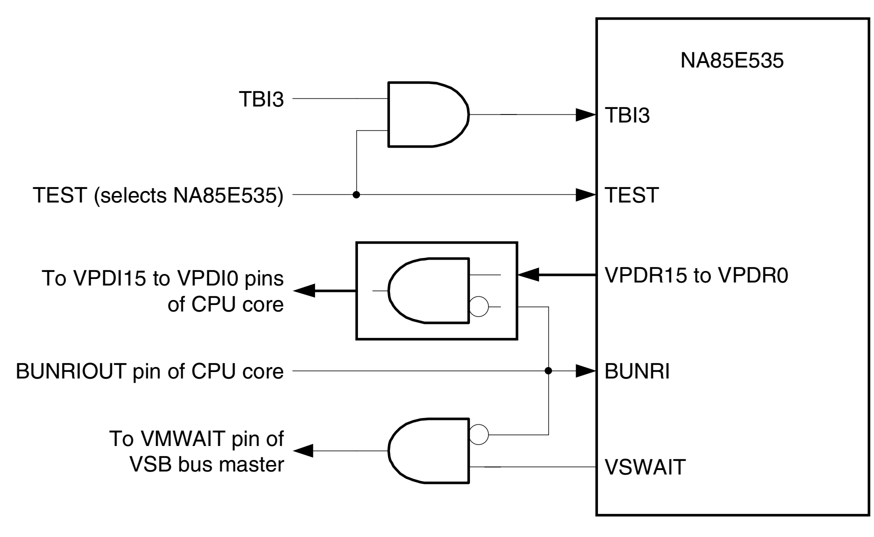
★ 5.2 Notes on Wiring Test Bus

The NA85E535 does not initialize the normally connected pins in the separation test mode of other macros (BUNRI = 1, TEST = 0). If the VDCSZn signal is active at this time, an active level is output to the VSWAIT pin (n = 7 to 0).

The CPU core has a peripheral test mode that tests the macro connected to its VSB (NPB) via the test bus. In this peripheral test mode, the VSB pin is valid even in the test bus mode. Therefore, the test pattern of the VSB peripheral macro may not pass because of the output pin level of the NA85E535 in the VSB peripheral test mode using the test bus of the CPU core. To avoid this, wire the TBI3 and TEST signals of the test bus of the NA85E535 as shown in Figure 5-1 after wiring the test bus with TESTACT.

Note that this wiring is not necessary if there is no macro to be tested in the peripheral test mode using the test bus of the CPU core.

Figure 5-1. Wiring of Test Bus

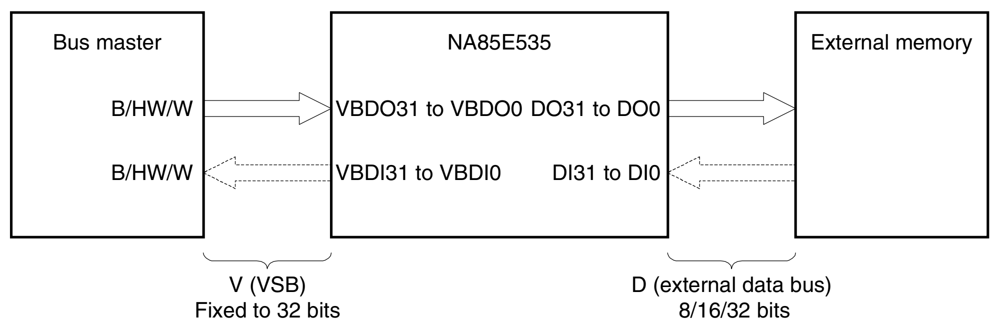


Remark The TBI19 to TBI4, TBI2 to TBI0, and TBO15 to TBO0 pins require no special processing.

CHAPTER 6 DATA FLOW

The flow to transfer data to the external memory differs depending on the set values of the registers, start address, and data width.

Figure 6-1. Data, VSB, External Data Bus

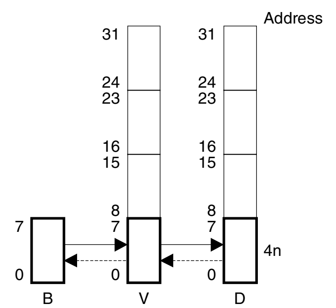
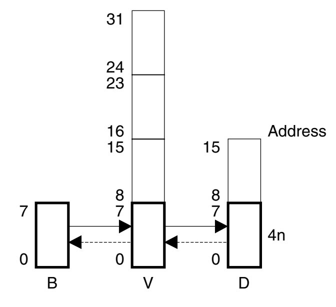
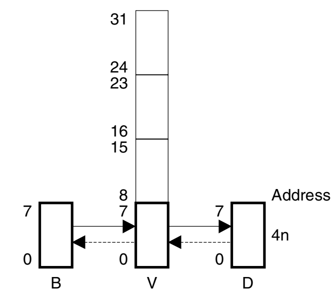
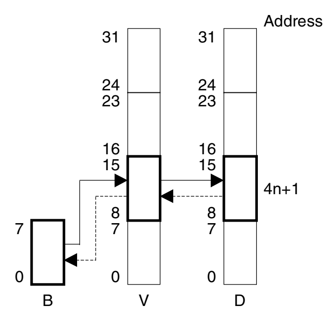
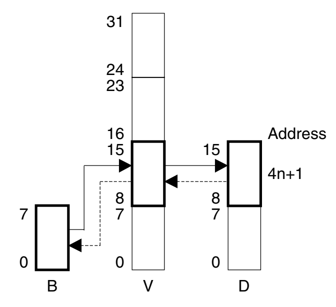
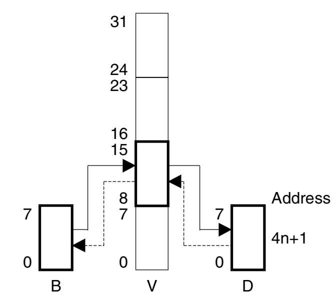
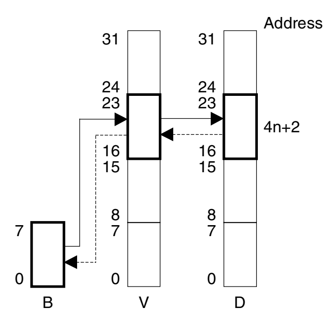
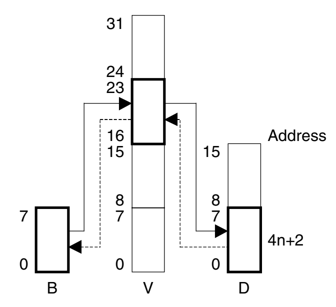
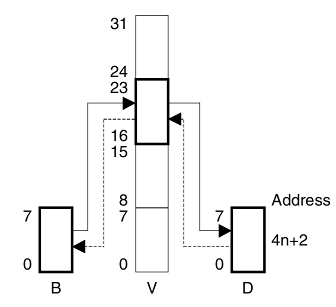
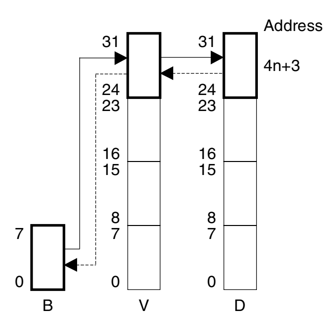
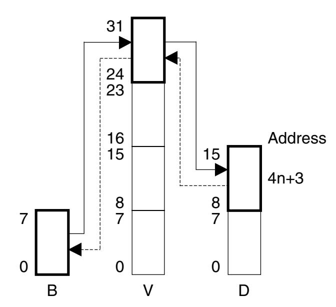
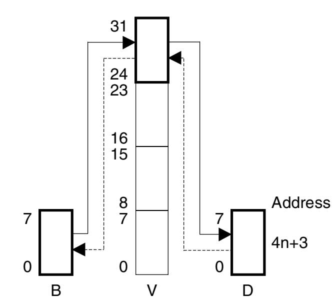


Remark B: Byte data
HW: Halfword data
W: Word data

The data flow in each condition is shown on the following pages.

6.1 Data Flow for Byte Access (8 Bits)

Figure 6-2. Data Flow for Byte Access (Little Endian)

Address to be accessed	Data transfer flow		
	External data bus: 32 bits	External data bus: 16 bits	External data bus: 8 bits
4n			
4n+1			
4n+2			
4n+3			

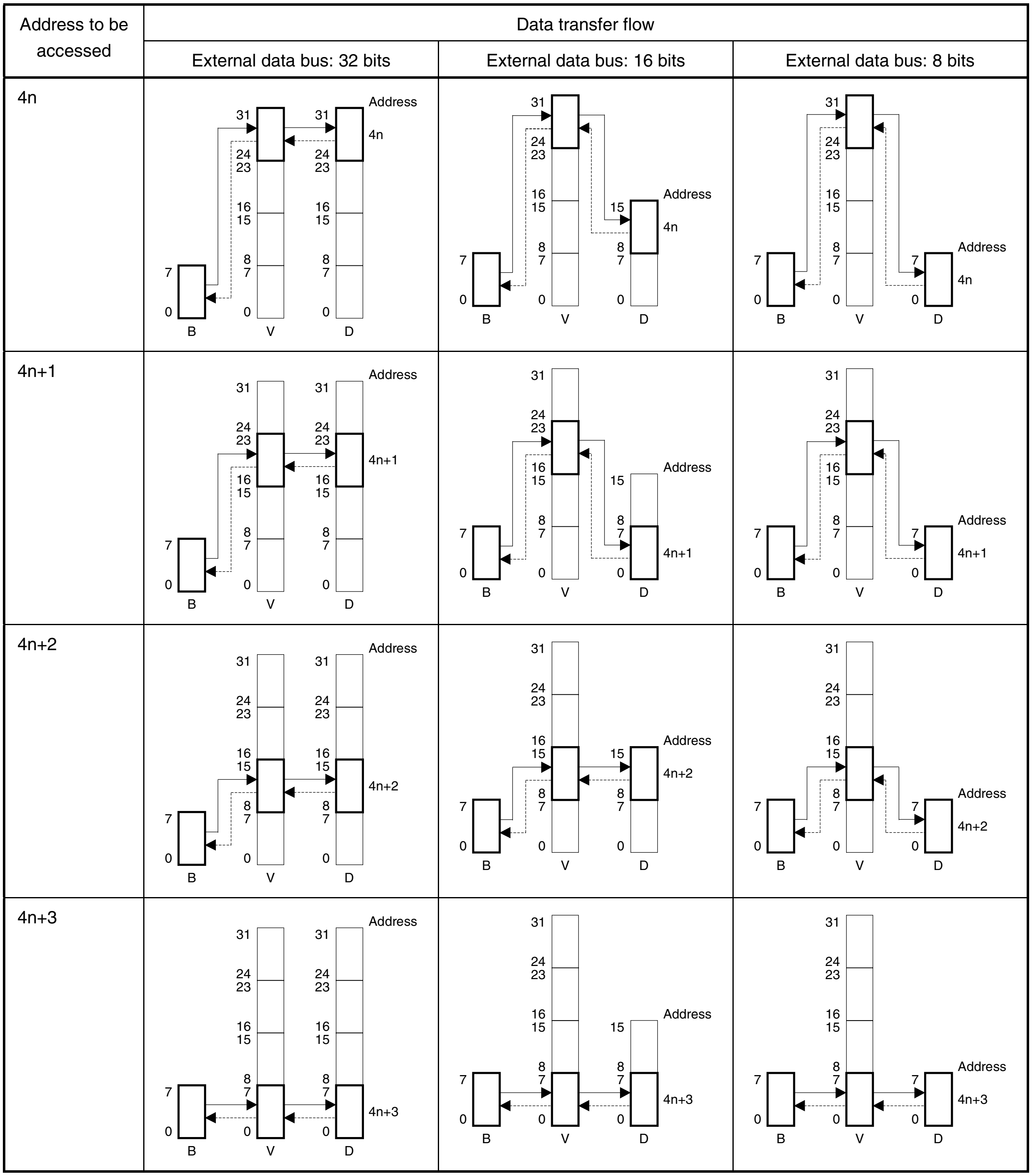
Remarks **1.** B: Byte data, V: VSB (fixed to 32 bits), D: External data bus

2. Solid line (——▶): Write

Dotted line (◀----): Read

3. n = 0, 1, 2, 3, …

Figure 6-3. Data Flow for Byte Access (Big Endian)



Remarks 1. B: Byte data, V: VSB (fixed to 32 bits), D: External data bus

2. Solid line (——►): Write

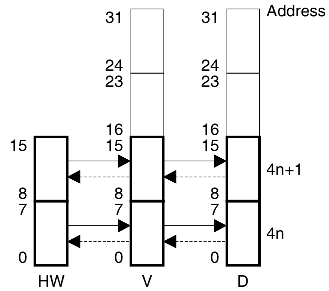
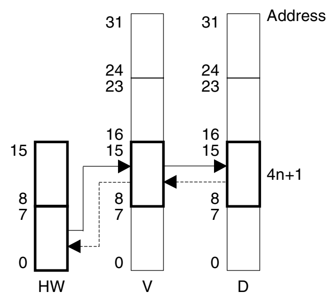
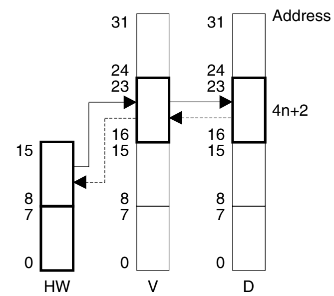
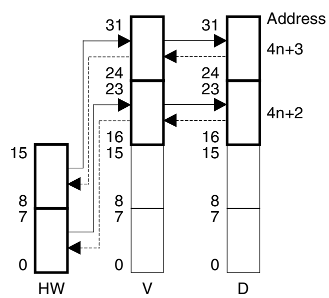
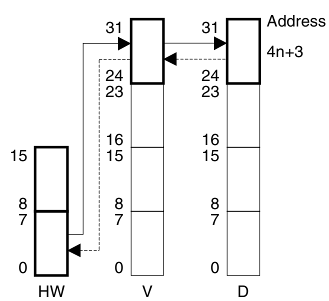
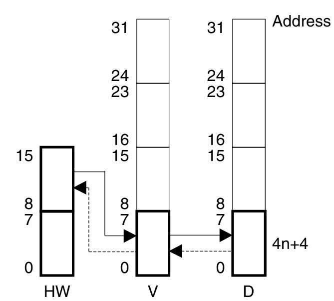
Dotted line (◄----): Read

3. n = 0, 1, 2, 3, …

6.2 Data Flow for Halfword Access (16 Bits)

Figure 6-4. Data Flow for Halfword Access (Little Endian) (1/3)

(a) External data bus: 32 bits

Address to be accessed	Data transfer flow (number of transfers when viewed from external bus)	
	First time	Second time
4n		–
4n+1		
4n+2		–
4n+3		

Remarks 1. B: Byte data, V: VSB (fixed to 32 bits), D: External data bus

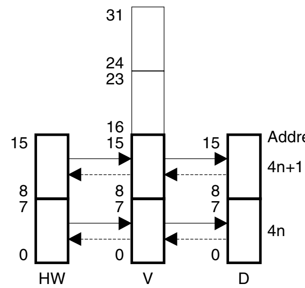
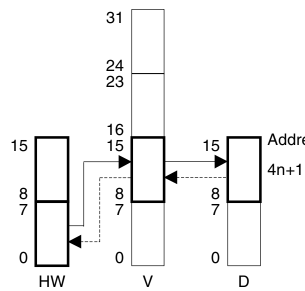
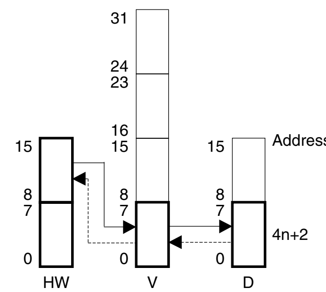
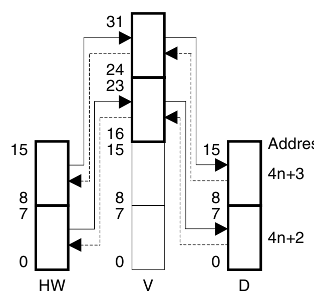
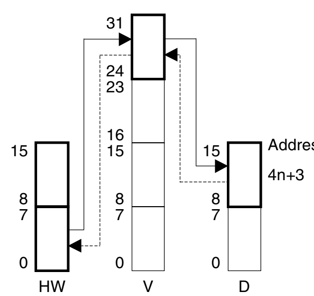
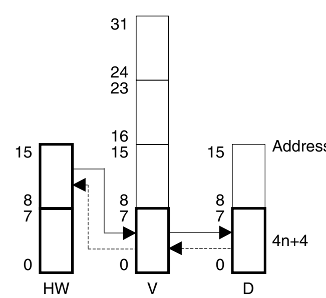
2. Solid line (——►): Write

Dotted line (◄----): Read

3. n = 0, 1, 2, 3, …

Figure 6-4. Data Flow for Halfword Access (Little Endian) (2/3)

(b) External data bus: 16 bits

Address to be accessed	Data transfer flow (number of transfers when viewed from external bus)	
	First time	Second time
4n		–
4n+1		
4n+2		–
4n+3		

Remarks 1. B: Byte data, V: VSB (fixed to 32 bits), D: External data bus

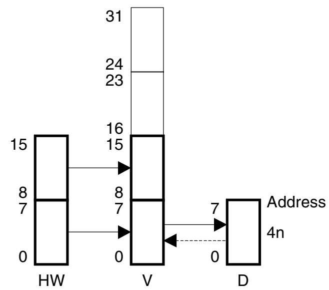
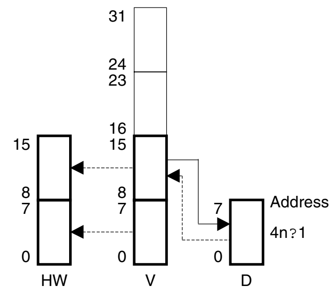
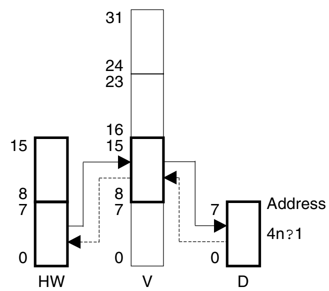
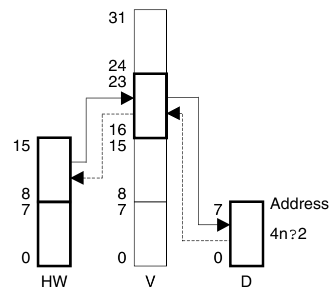
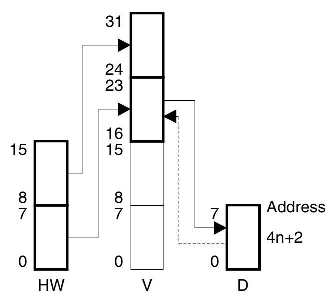
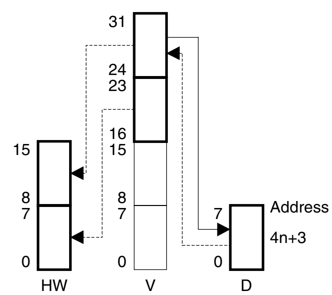
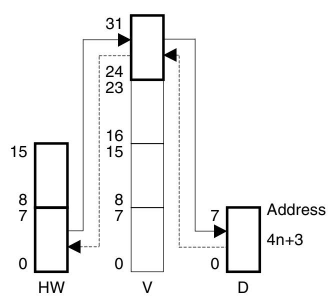
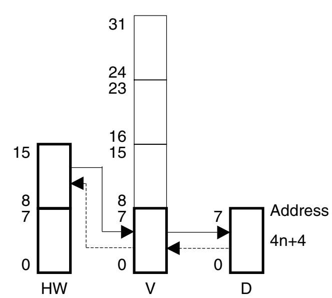
2. Solid line (⟶): Write

Dotted line (◀----): Read

3. n = 0, 1, 2, 3, …

Figure 6-4. Data Flow for Halfword Access (Little Endian) (3/3)

(c) External Data bus: 8 bits

Address to be accessed	Data transfer flow (number of transfers when viewed from external bus)	
	First time	Second time
4n		
4n+1		
4n+2		
4n+3		

Remarks 1. B: Byte data, V: VSB (fixed to 32 bits), D: External data bus

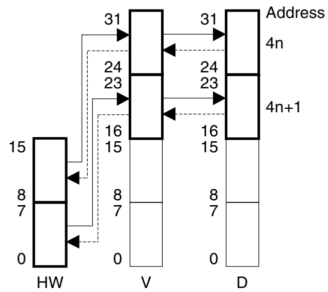
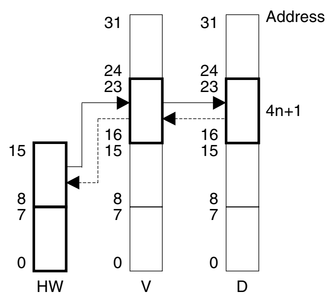
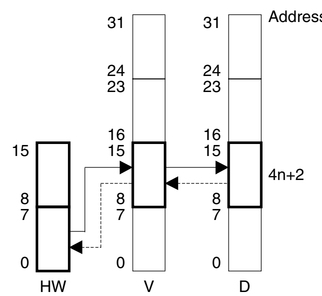
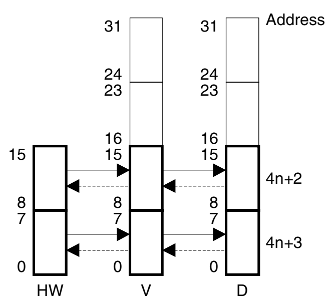
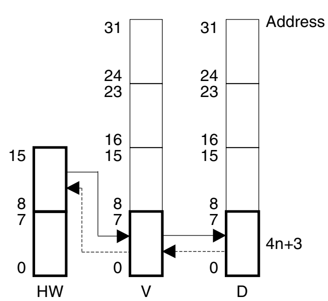
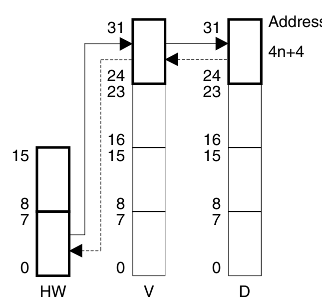
2. Solid line (⟶): Write

Dotted line (◄----): Read

3. n = 0, 1, 2, 3, …

Figure 6-5. Data Flow for Halfword Access (Big Endian) (1/3)

(a) External data bus: 32 bits

Address to be accessed	Data transfer flow (number of transfers when viewed from external bus)	
	First time	Second time
4n		–
4n+1		
4n+2		–
4n+3		

Remarks **1.** B: Byte data, V: VSB (fixed to 32 bits), D: External data bus

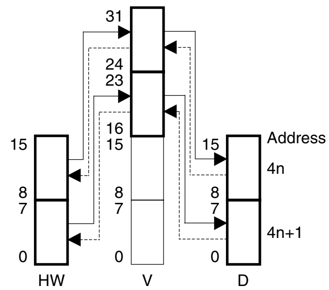
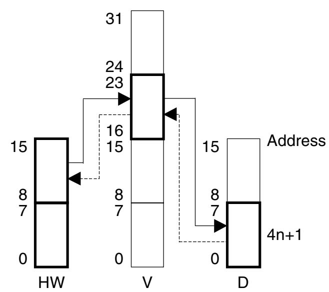
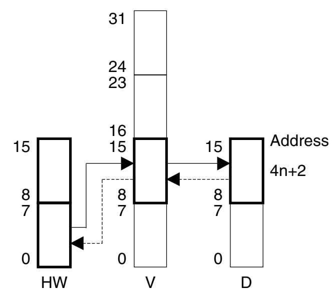
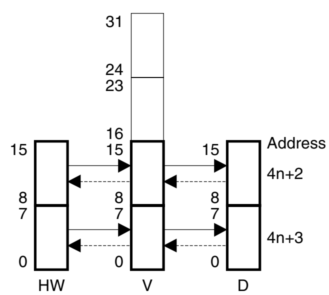
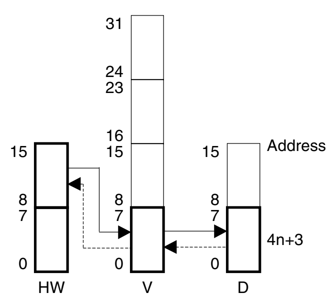
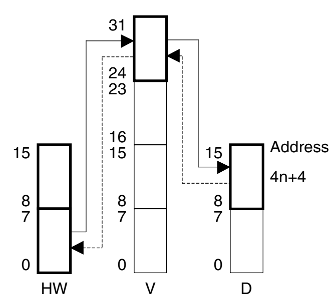
2. Solid line (⟶): Write

Dotted line (◀----): Read

3. n = 0, 1, 2, 3, …

Figure 6-5. Data Flow for Halfword Access (Big Endian) (2/3)

(b) External data bus: 16 bits

Address to be accessed	Data transfer flow (number of transfers when viewed from external bus)	
	First time	Second time
4n		–
4n+1		
4n+2		–
4n+3		

Remarks 1. B: Byte data, V: VSB (fixed to 32 bits), D: External data bus

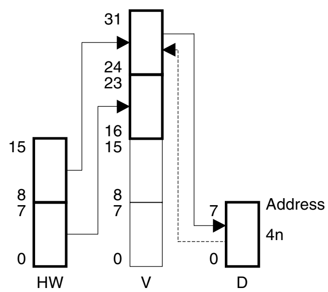
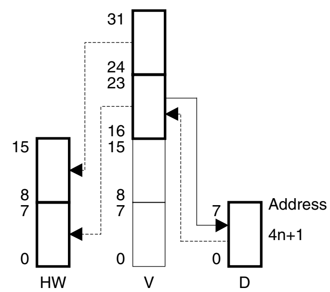
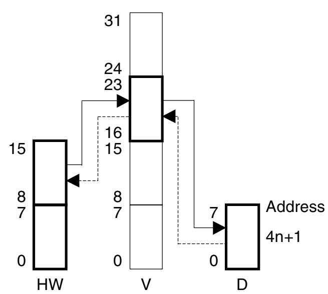
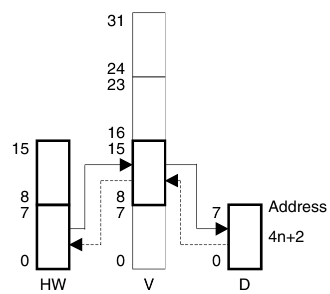
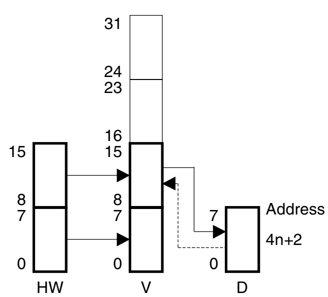
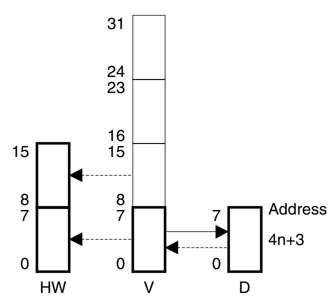
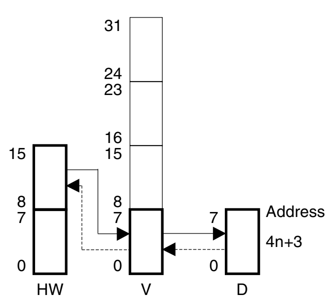
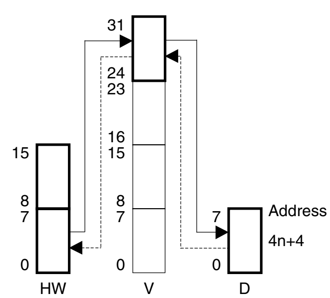
2. Solid line (⟶): Write

Dotted line (◄----): Read

3. n = 0, 1, 2, 3, …

Figure 6-5. Data Flow for Halfword Access (Big Endian) (3/3)

(c) External Data bus: 8 bits

Address to be accessed	Data transfer flow (number of transfers when viewed from external bus)	
	First time	Second time
4n		
4n+1		
4n+2		
4n+3		

Remarks 1. B: Byte data, V: VSB (fixed to 32 bits), D: External data bus

2. Solid line (⟶): Write

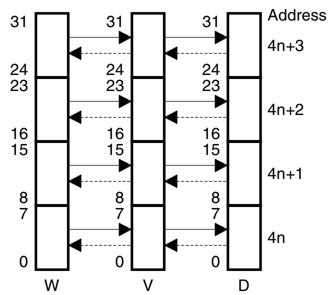
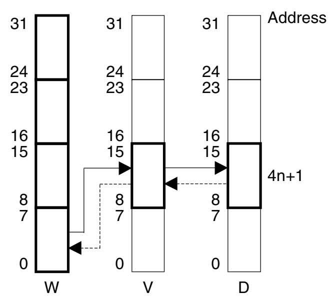
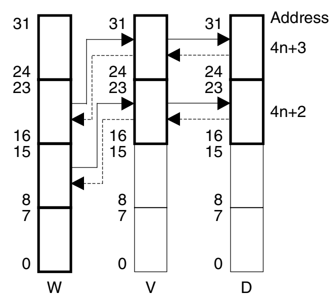
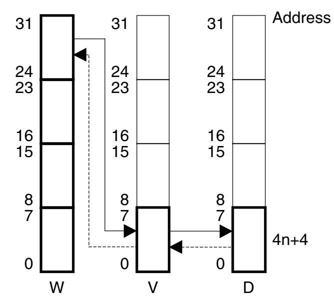
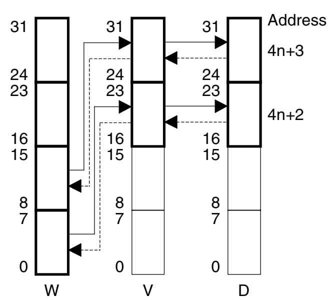
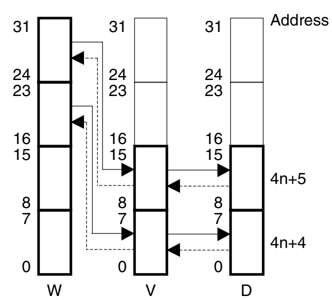
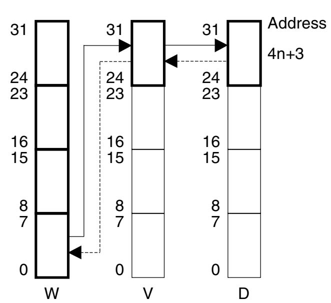
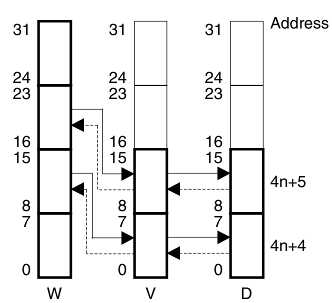
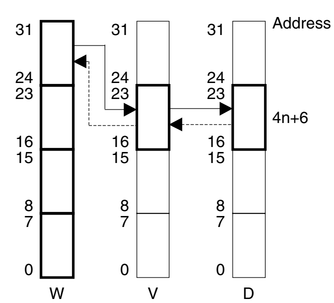
Dotted line (◄----): Read

3. n = 0, 1, 2, 3, …

6.3 Data Flow for Word Access (32 Bits)

Figure 6-6. Data Flow for Word Access (Little Endian) (1/3)

(a) External data bus: 32 bits

Address to be accessed	Data transfer flow (number of transfers when viewed from external bus)		
	First time	Second time	Third time
4n		–	–
4n+1			
4n+2			–
4n+3			

Remarks 1. B: Byte data, V: VSB (fixed to 32 bits), D: External data bus

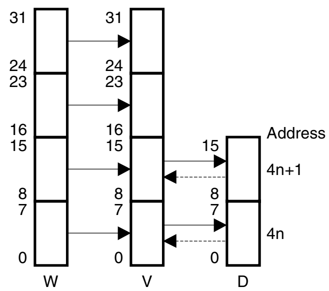
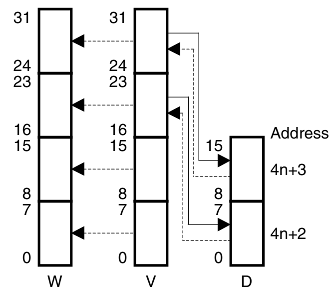
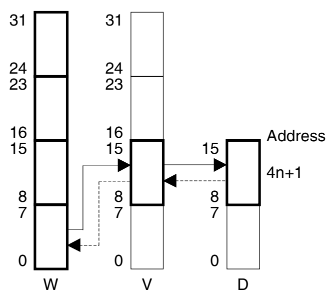
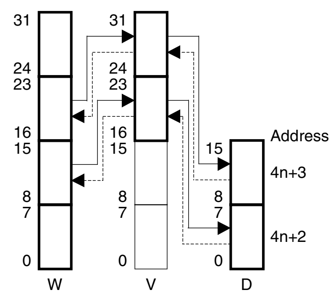
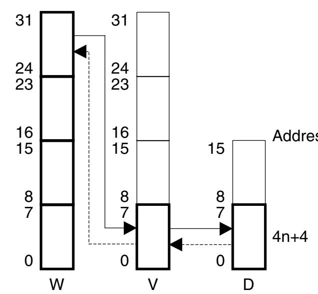
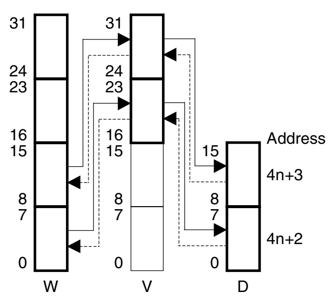
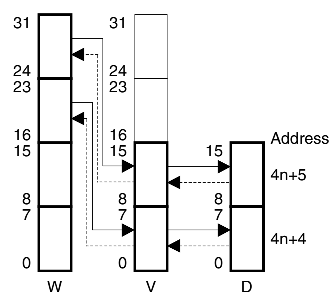
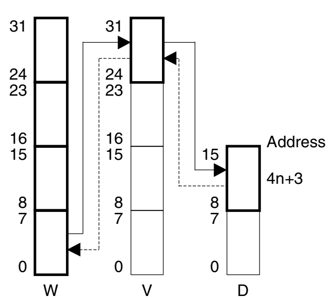
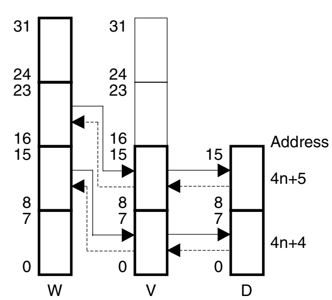
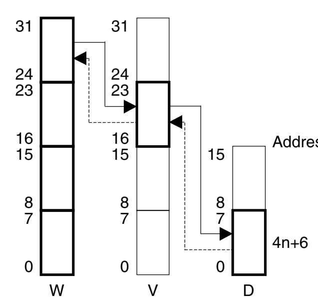
2. Solid line (⟶): Write

Dotted line (◄----): Read

3. n = 0, 1, 2, 3, …

Figure 6-6. Data Flow for Word Access (Little Endian) (2/3)

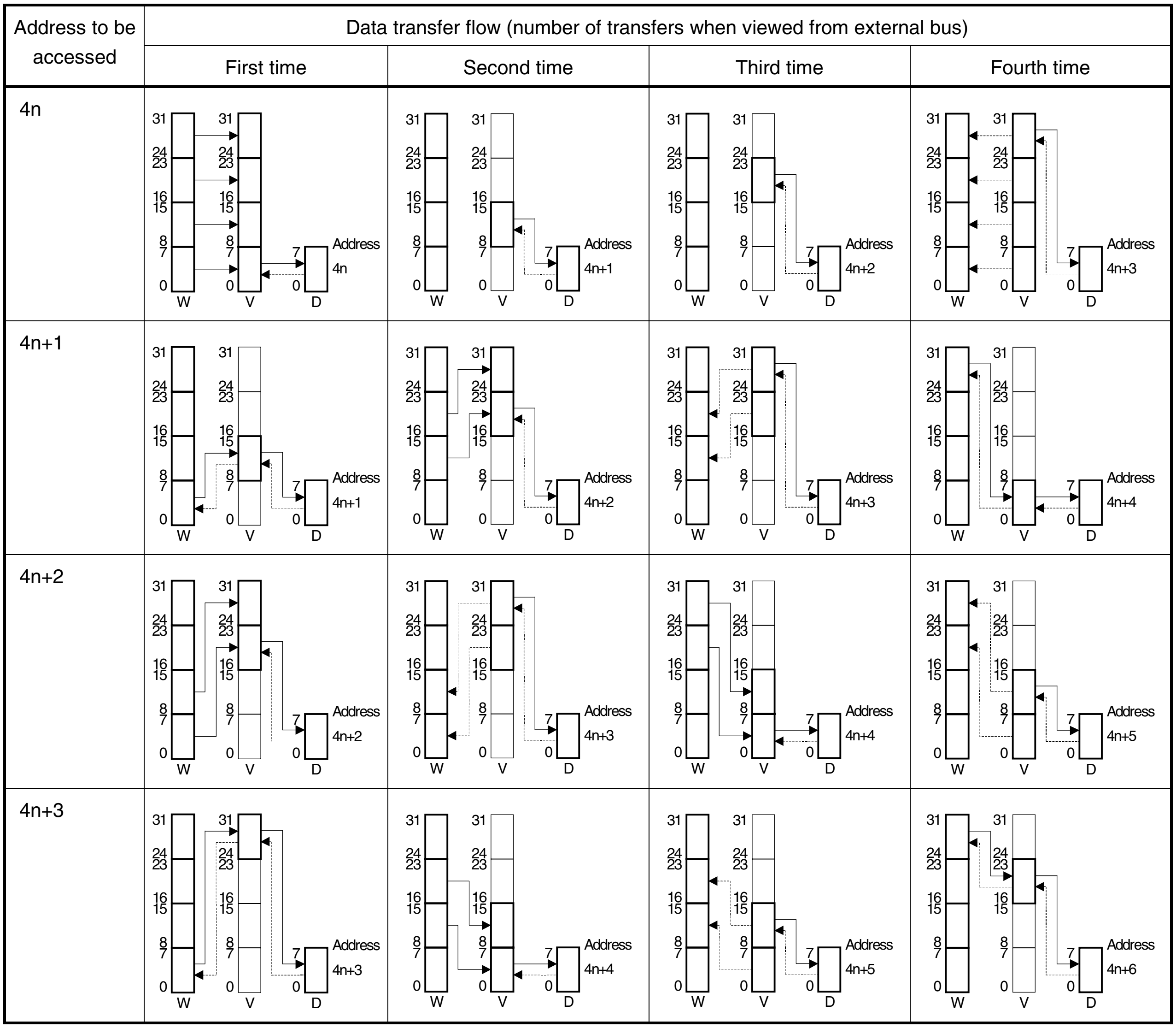
(b) External data bus: 16 bits

Address to be accessed	Data transfer flow (number of transfers when viewed from external bus)		
	First time	Second time	Third time
4n			–
4n+1			
4n+2			–
4n+3			

Remarks
1. B: Byte data, V: VSB (fixed to 32 bits), D: External data bus
2. Solid line (⟶): Write
Dotted line (◀----): Read
3. n = 0, 1, 2, 3, …

Figure 6-6. Data Flow for Word Access (Little Endian) (3/3)

(c) External data bus: 8 bits



Remarks **1.** B: Byte data, V: VSB (fixed to 32 bits), D: External data bus

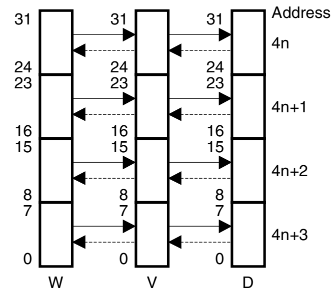
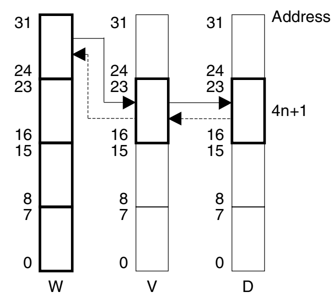
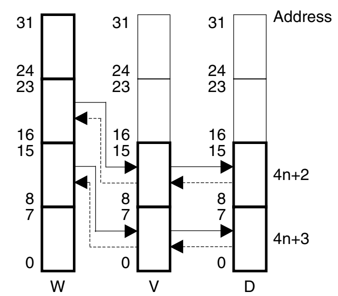
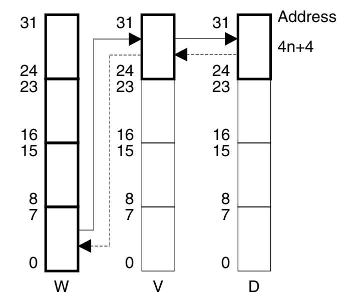
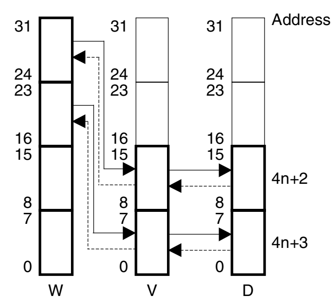
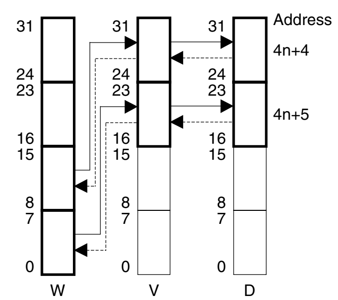
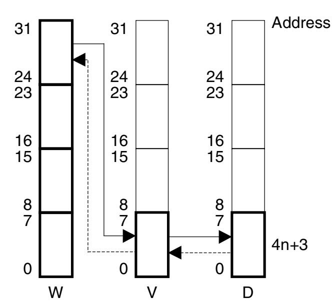
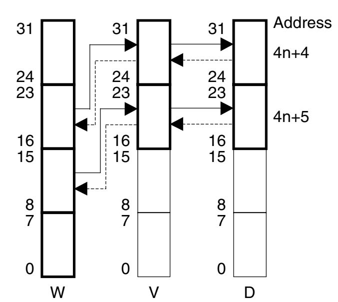
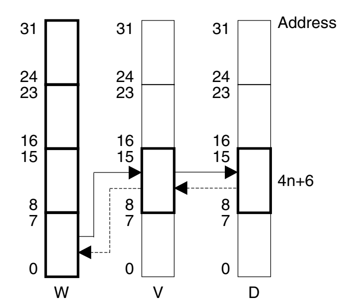
2. Solid line (——►): Write

Dotted line (◄----): Read

3. n = 0, 1, 2, 3, …

Figure 6-7. Data Flow for Word Access (Big Endian) (1/3)

(a) External data bus: 32 bits

Address to be accessed	Data transfer flow (number of transfers when viewed from external bus)		
	First time	Second time	Third time
4n		–	–
4n+1			
4n+2			–
4n+3			

Remarks 1. B: Byte data, V: VSB (fixed to 32 bits), D: External data bus

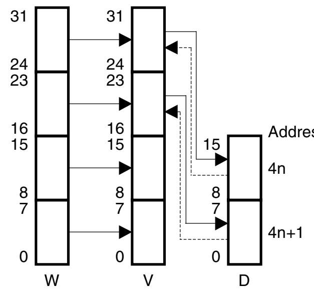
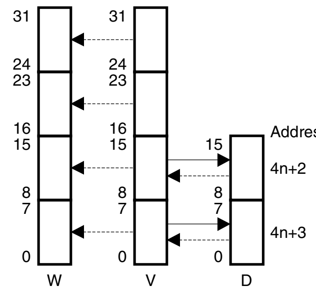
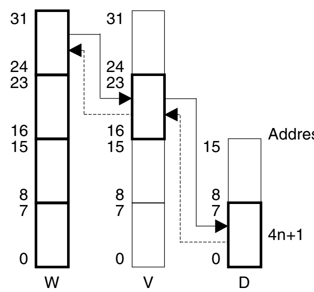
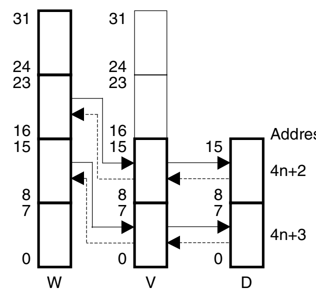
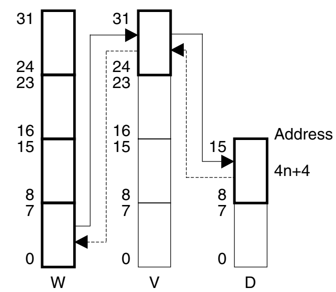
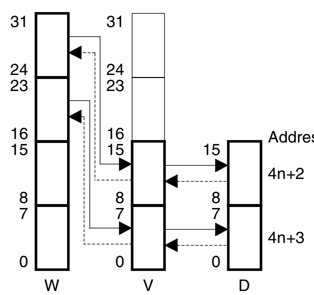
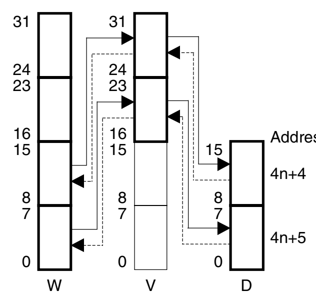
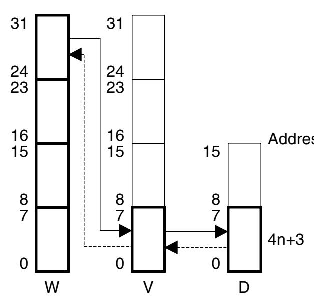
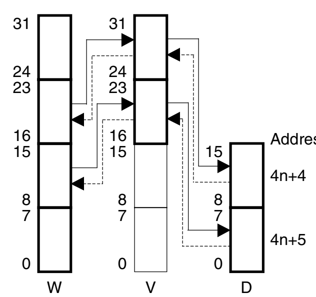
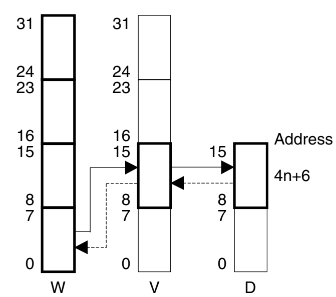
2. Solid line (⟶): Write

Dotted line (◄----): Read

3. n = 0, 1, 2, 3, …

Figure 6-7. Data Flow for Word Access (Big Endian) (2/3)

(b) External data bus: 16 bits

Address to be accessed	Data transfer flow (number of transfers when viewed from external bus)		
	First time	Second time	Third time
4n			–
4n+1			
4n+2			–
4n+3			

Remarks 1. B: Byte data, V: VSB (fixed to 32 bits), D: External data bus

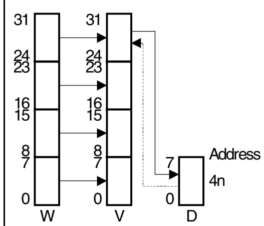
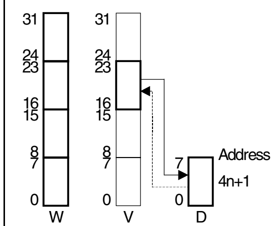
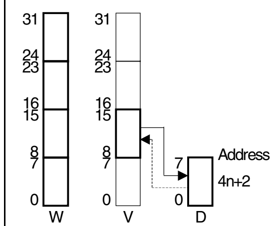
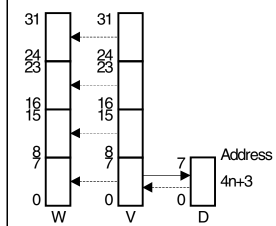
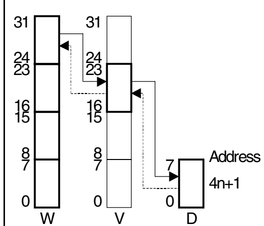
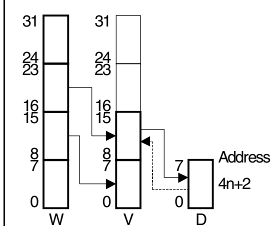
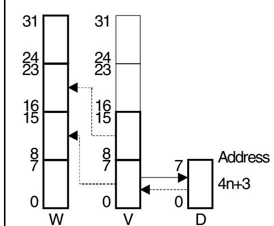
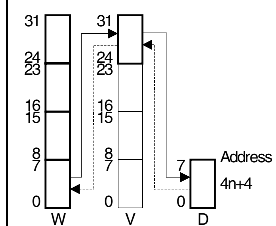
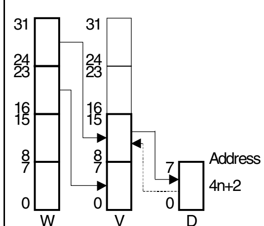
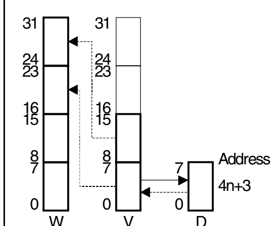
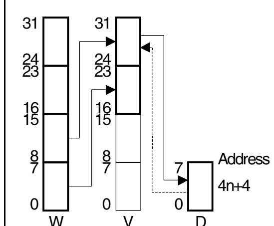
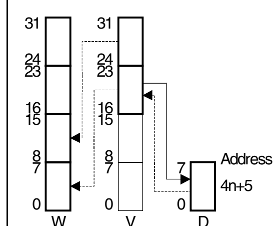
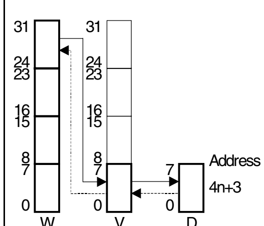
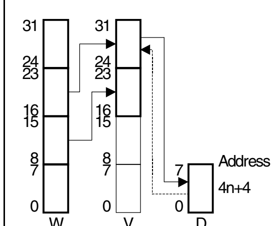
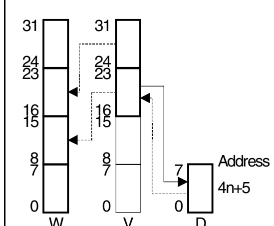
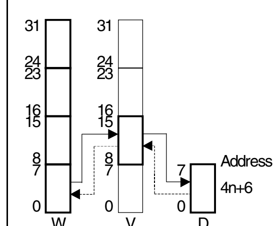
2. Solid line (⟶): Write

Dotted line (◄----): Read

3. n = 0, 1, 2, 3, …

Figure 6-7. Data Flow for Word Access (Big Endian) (3/3)

(c) External data bus: 8 bits

Address to be accessed	Data transfer flow (number of transfers when viewed from external bus)			
	First time	Second time	Third time	Fourth time
4n				
4n+1				
4n+2				
4n+3				

Remarks **1.** B: Byte data, V: VSB (fixed to 32 bits), D: External data bus

2. Solid line (——►): Write

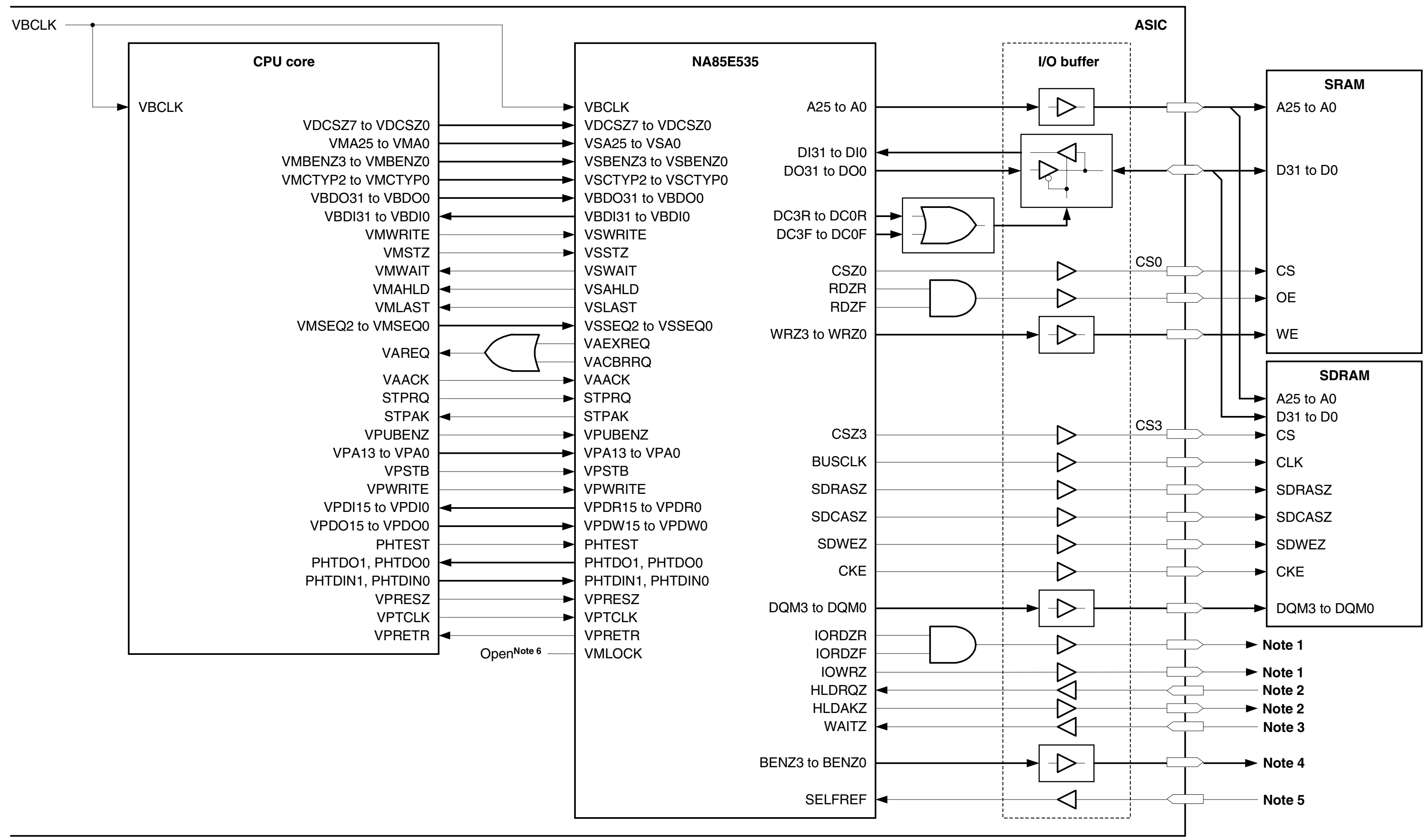
Dotted line (◄----): Read

3. n = 0, 1, 2, 3, …

APPENDIX A CONNECTION EXAMPLE

An example of the connection (when a bus master other than the CPU core is not used) of the CPU core, NA85E535, and external memory (SRAM or SDRAM) is shown below.

★Figure A-1. Example of Connecting CPU Core, NA85E535, and External Memory (SRAM or SDRAM) (When Bus Master Other than CPU Core Is Not Used)



Notes
1. Used during DMA flyby transfer
2. Used in bus hold status
3. Used for external wait control
4. Used when memory with byte enable control function is connected
5. Used for self-refresh
6. This may be opened when a bus master other than the CPU core is not used.

APPENDIX B GENERAL INDEX

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