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RENESAS

User's Manual

How to Use Low Latency DRAM

Document No. M19202EJ1V0UM00 (1st Edition)
Date Published July 2008 NS

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

QDR RAMs and Quad Data Rate RAMs comprise a new series of products developed by Cypress Semiconductor, Renesas, IDT, NEC Electronics, and Samsung.

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M8E 02. 11-1

INTRODUCTION

Target Readers This manual is intended for users who design application systems which use low latency DRAM.

Purpose The purpose of this manual is to help users understand the basic functions of low latency DRAM, and how to use them. For the detailed values of each product, see the corresponding data sheets.

How to Read This Manual It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and memory products. For details of the functions of each product, see the corresponding data sheets. Note that the operation examples described in this user's manual are presented for reference and that the described data are not guaranteed values but values to be used for reference.

Conventions

Data significance: Higher digits on the left and lower digits on the right

xxx# (sharp symbol appended to a pin or signal name) :
Active low representation

Note: Footnote for item marked with Note in the text.

Caution: Information requiring particular attention

Remark: Supplementary information

Configuration This manual is configured of the following contents.

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CHAPTER 2 COMMANDS
CHAPTER 3 REFRESH OPERATIONS
CHAPTER 4 POWER APPLICATION
CHAPTER 5 PLL CIRCUIT
CHAPTER 6 OUTPUT IMPEDANCE MATCHING
CHAPTER 7 TERMINAL RESISTORS
CHAPTER 8 ON DIE TERMINATION (ODT)

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CHAPTER 1 OVERVIEW

NEC Electronics develops QDR™ SRAMs, DDR SRAMs, and low latency DRAM as memories for network devices. QDR SRAMs and DDR SRAMs are suitable for network devices which require high-speed random access performance, and low latency DRAM is suitable for network devices which require memory capacity and random access performance. Furthermore, the application of low latency DRAM is increasing not only for network devices, but also for digital home appliances. This manual describes how to use low latency DRAM.

1.1 Features

Low latency DRAM is memory which is suited to be used as buffer memories of highly functional network switches, network routers, and digital home appliances. The random access performance is improved by configuring the memory cell array in eight banks.

Low latency DRAM is classified into four major product groups according to the I/O configuration and I/O voltage, as shown in Table 1-1. The part numbers of products differ for I/O voltages of 1.5 V and 1.8 V, so select the I/O voltage product to be used accordingly.

Table 1–1. 288 Mb Low Latency DRAM Product Classification

Part Number	I/O Configuration	I/O Voltage	Absolute Maximum I/O Voltage Rating
μPD482882xxFF-EFxx	Common (CIO)	1.5 V	1.975 V
μPD482881xxFF-EFxx	Separated (SIO)	1.5 V	1.975 V
μPD482882xxFF-Exx	Common (CIO)	1.8 V	2.1 V
μPD482881xxFF-Exx	Separated (SIO)	1.8 V	2.1 V

With low latency DRAM, the product functions shown in Table 1-2 can be set according to the application. See **2.3 MRS Command** for setting descriptions and setting methods, because some functional combinations are restricted.

Table 1–2. Selectable Product Functions

Selectable Product Functions
Configuration • Random cycle time (t_{RC}) • READ latency (t_{RL}) • WRITE latency (t_{WL})
Burst length
Address multiplex function
PLL function
Output impedance mode function
ODT function[Note]

Note ODT: On Die Termination

1.2 CIO and SIO Product Characteristics

CIO (Common I/O) and SIO (Separate I/O) products have different pin counts and command input timings.

With CIO products, data ports are shared for input and output. The number of I/O pins used can therefore be halved in contrast to SIO products. With CIO products, insertion of NOP cycles, however, is required when switching from WRITE command input to READ command input, as shown in Figure 1-1.

With SIO products, data ports are separately provided for input and output. The data transfer rate (band width) can therefore be improved in contrast to CIO products. Furthermore, unlike with CIO products, insertion of NOP cycles when switching from WRITE command input to READ command input is not required, as shown in Figure 1-2.

Figure 1–1. CIO Product Timing Chart (Non-Multiplexed Address Mode, BL = 2, Configuration 1)

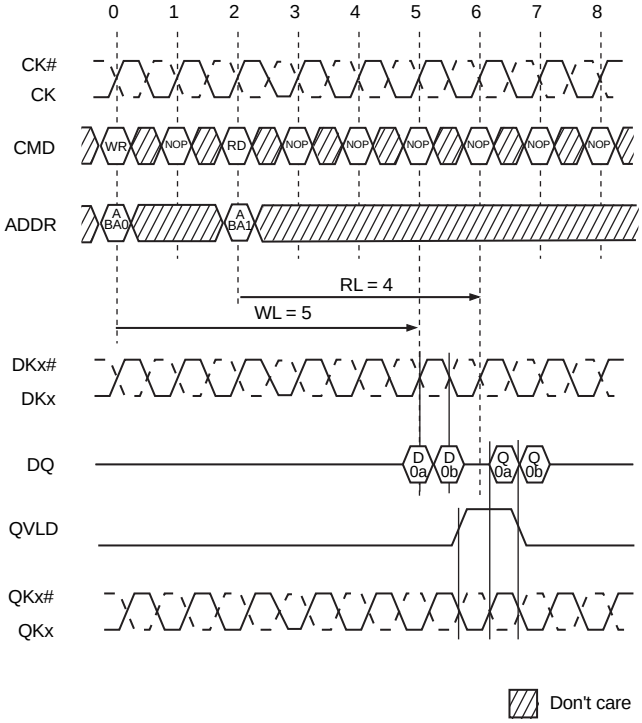
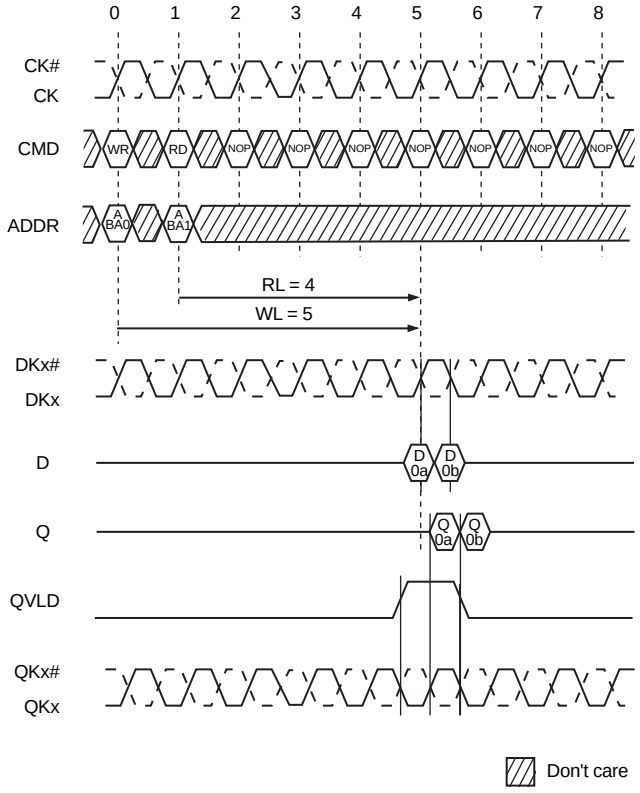


Figure 1–2. SIO Product Timing Chart (Non-Multiplexed Address Mode, BL = 2, Configuration 1)



1.3 Bank Operation

The memory cell array is configured in eight banks, each of which can be controlled separately. By freely selecting the bank, banks can be operated normally, even if a refresh operation is performed on another bank.

The selection of banks can be set according to the bank address [BA2:0] input level. Table 1-3 shows the correspondence between the selected addresses of each bank.

Table 1–3. Bank Correspondence

Selected Bank	BA2	BA1	BA0
Bank 0	0	0	0
Bank 1	0	0	1
Bank 2	0	1	0
Bank 3	0	1	1
Bank 4	1	0	0
Bank 5	1	0	1
Bank 6	1	1	0
Bank 7	1	1	1

Figures 1-3, 1-4, 1-5, and 1-6 show examples of the representative timing charts of bank operations.

Figure 1–3. CIO Product Timing Chart (Non-Multiplexed Address Mode, BL = 2, Configuration 1)

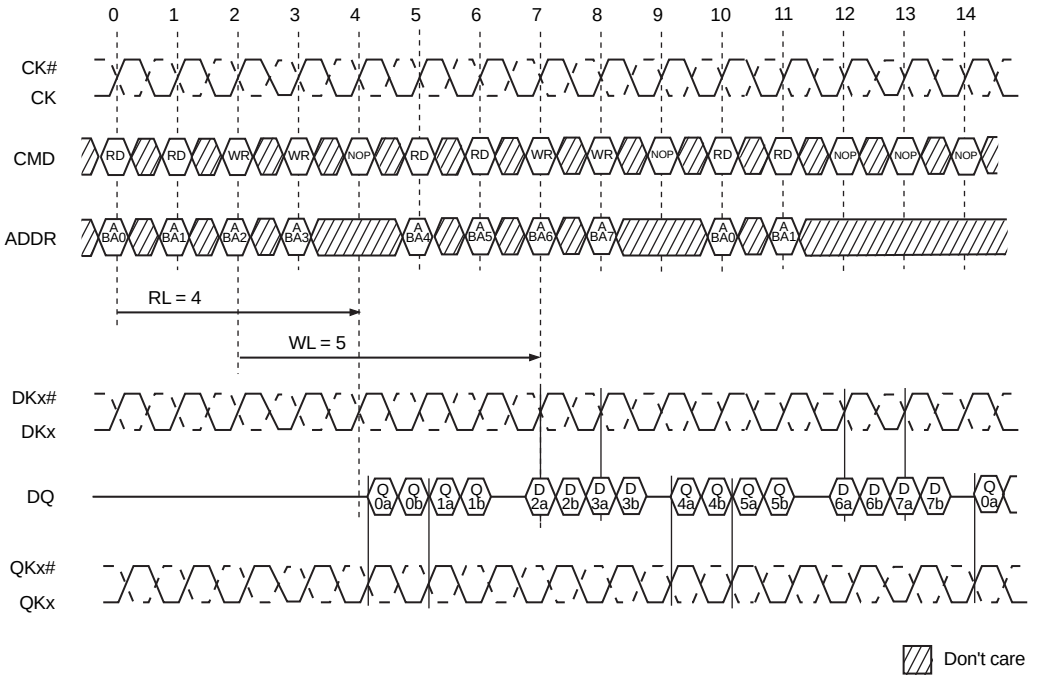


Figure 1–4. SIO Product Timing Chart (Non-Multiplexed Address Mode, BL = 2, Configuration 1)

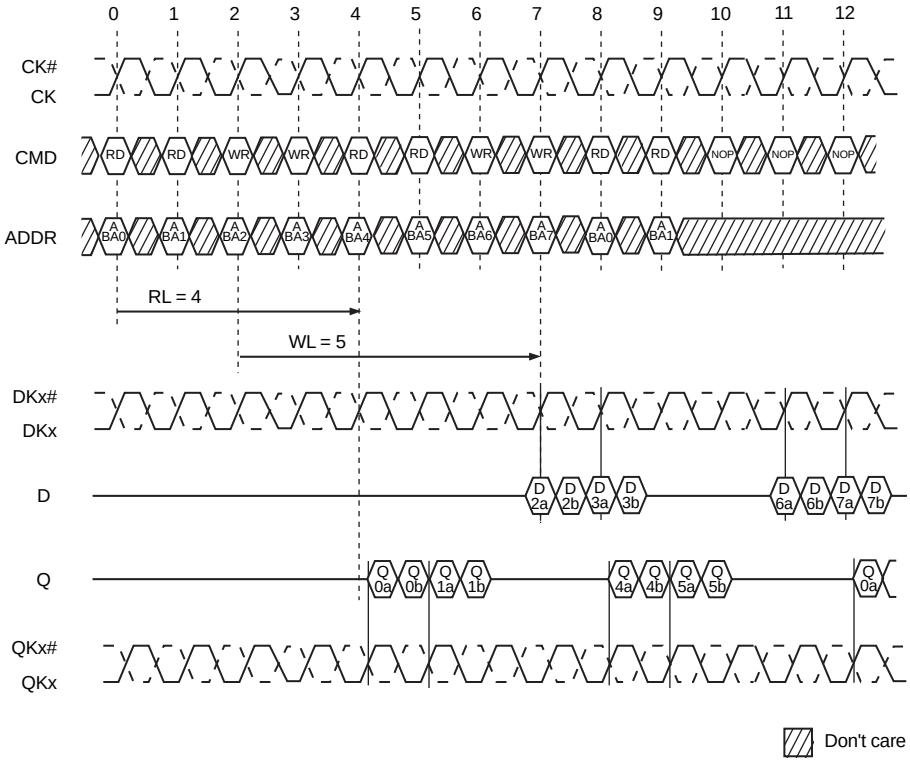


Figure 1–5. CIO Product Timing Chart Including Refresh Operation (Non-Multiplexed Address Mode, BL = 2, Configuration 1)

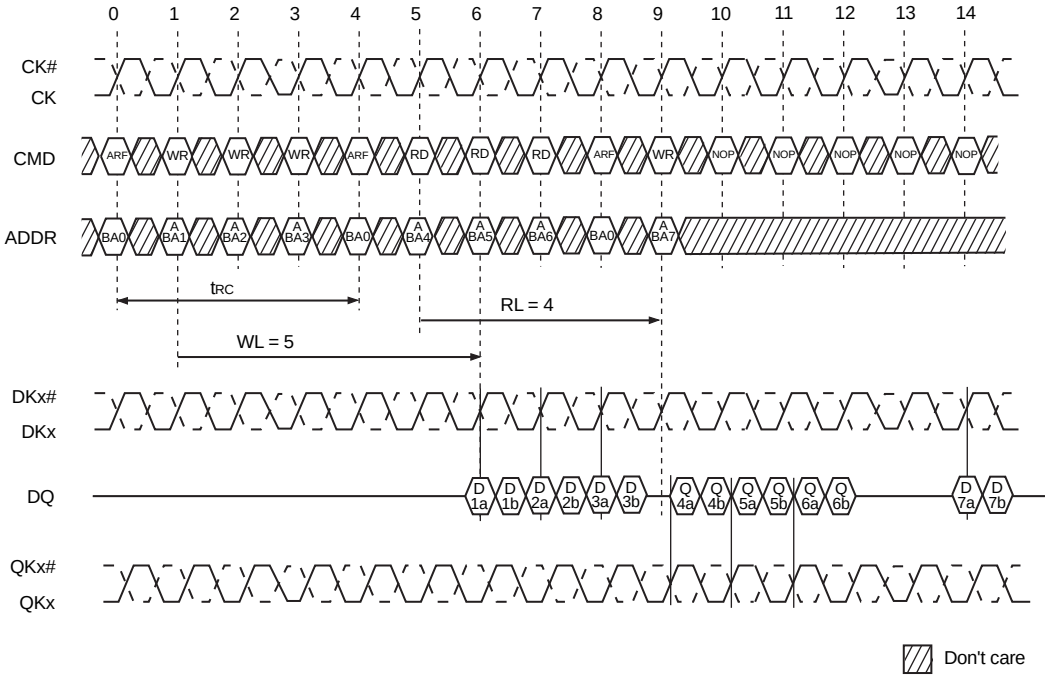
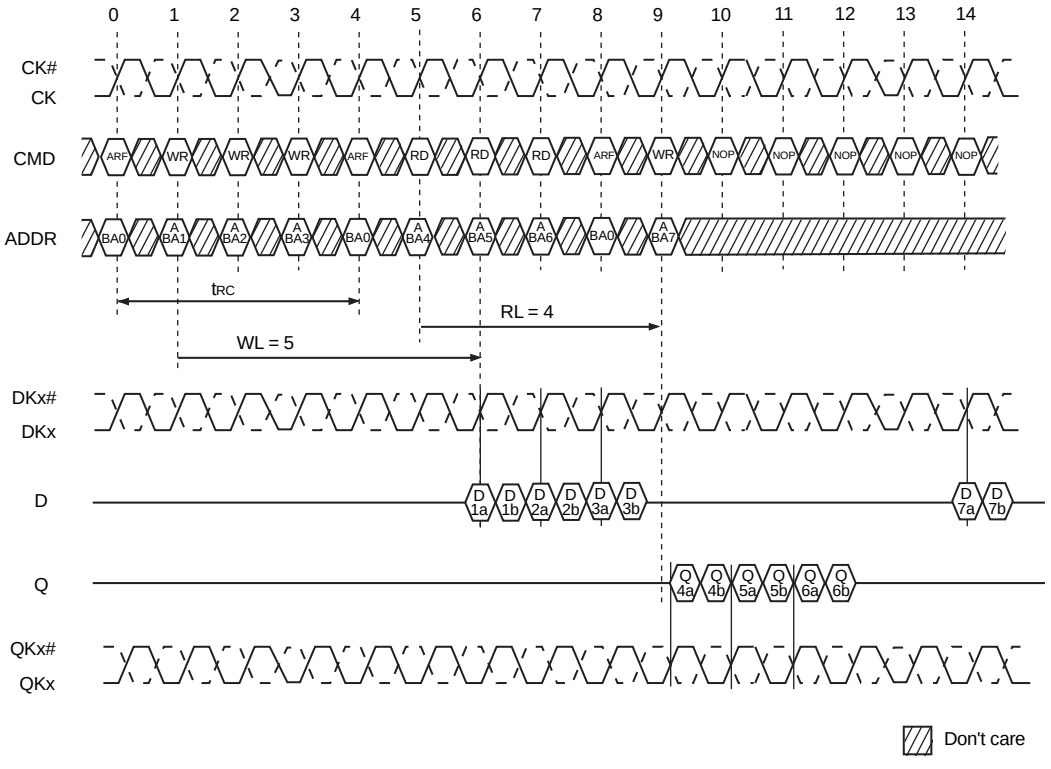


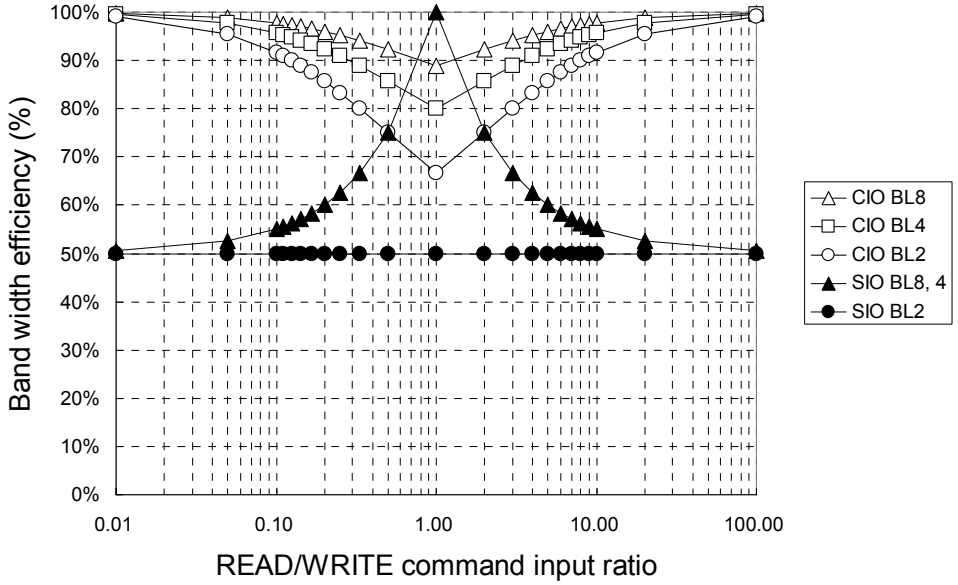
Figure 1–6. SIO Product Timing Chart Including Refresh Operation (Non-Multiplexed Address Mode, BL = 2, Configuration 1)



1.4 Data Transfer Rate (Band Width) Comparison

A data transfer rate (band width) represents the data transfer performance at a data port (D pin, Q pin, or DQ pin). The band width varies, depending on the product (CIO or SIO product), bit configuration (×9, ×18, or ×36), burst length (BL = 2, 4, or 8), operation frequency, and operation ratio between READ and WRITE operations. Figure 1-7 shows the relationship between the READ and WRITE command input ratio and the band width efficiency for each product and burst length. Comparisons are made assuming the same operation frequencies and bit configurations.

Figure 1–7. Band Width Efficiency READ and WRITE Command Input Ratio Dependence



1.5 Explanation of pin functions

This section explains the product pin functions. Table 1-4 describes pins that are common to CIO and SIO products, Table 1-5 describes pins unique to CIO products, and Table 1-6 describes pins unique to SIO products.

Table 1–4. Pins Common to CIO and SIO Products (1/3)

Pin	Type	Pin Function
CK, CK#	Input	Input clock This is a clock signal input pin which becomes the standard for the input timing of command and address signals. Command and address signals must be input in synchronization with the rising edge of CK. The inputs of CK and CK# are differential clock inputs. Input CK and CK#, being at a phase difference of 180 degrees against each other.
CS#	Input	Chip selection This pin is used to control command input. When CS# = LOW at the rising edge of CK at a CK/CK# cross point, command input becomes valid. When CS# = HIGH, command input becomes invalid.
WE#	Input	WRITE command input This pin is used to control WRITE and READ command input. When WE# = LOW, CS# = LOW, and REF# = HIGH at the rising edge of CK at a CK/CK# cross point, a WRITE command results. A READ command results when WE# = HIGH, CS# = LOW, and REF# = HIGH.
REF#	Input	Refresh command input This pin is used to control refresh command input. When REF# = LOW, CS# = LOW, and WE# = HIGH at the rising edge of CK at a CK/CK# cross point, an automatic refresh command results.
A[xx:0]	Input	Address input These are address signal input pins. Input write and read addresses at the rising edge of CK at a CK/CK# cross point. The address input pins are used to set the mode register. See **2.3 MRS Command** for details.
BA[2:0]	Input	Bank address input These pins are used to select the banks which perform “READ” and “WRITE”. This product has eight banks. Input the addresses of the banks which will perform “WRITE” and “READ” at the rising edge of CK at a CK/CK# cross point.
QKx, QKx#	Output	Output data clock These are the output pins of the clock signals output by the IC. QKx and QKx# are clock signals for referencing output data signals and are output at the same timing as output data signals. QKx and QKx# are constantly output at a phase difference of 180 degrees against each other. x9 product: QK0 and QK0# are output from output data Q0 (DQ0) at the same timing as Q8 (DQ8). x18 product: QK0 and QK0#, and Q8 (DQ8), QK1, and QK1# are output from Q0 (DQ0) and Q9 (DQ9), respectively, at the same timing as Q17 (DQ17). x36 product: QK0 and QK0#, and Q17 (DQ17), QK1, and QK1# are output from Q0 (DQ0) and Q18 (DQ18), respectively, at the same timing as Q35 (DQ35).

Table 1–4. Pins Common to CIO and SIO Products (2/3)

Pin	Type	Pin Function
DKx, DKx#	Input	Input data clock These are the clock signal input pins which become the standard for the data input timing. The data to be written must be input in synchronization with the cross point of DKx/DKx#. The inputs of DKx and DKx# are differential clock inputs. Input DKx and DKx#, being at a phase difference of 180 degrees against each other. x9 and x18 products: Input data Dxx (DQxx) is captured at the same timing as DK and DK#. x36 products: D0 (DQ0) to D17 (DQ17), and D18 (DQ18) to D35 (DQ35) are captured at the same timing as DK0 and DK0#, and DK1 and DK1#, respectively.
DM	Input	Data mask input This pin is used to control the operation that writing is not executed for any data when writing the data. DM is captured in synchronization with the rising edges of DKx and DKx#. Data is not written if DM = HIGH is set while data is being input. Data is written while DM = LOW.
QVLD	Output	Valid-data output period This is an output signal pin that indicates the period during which valid data is output. The QVLD signal is switched at the same timing as QKx and QKx#. QVLD goes to HIGH half a cycle before valid data is output. QVLD goes to LOW half a cycle before output of valid data is completed.
ZQ	Input/Output	Output impedance matching input This pin is used to adjust the output impedance. Connect RQ, with a resistance five times the output impedance value to be set, between the ZQ pin and V_{SS}. The output impedance values of the data output pins (Q, DQ), output data clocks (QKx, QKx#), and valid-data output period signal (QVLD) are automatically adjusted to $0.2 \times$ RQ in the IC. Minimum impedance mode is set when ZQ = V_{SS}, and maximum impedance mode is set when ZQ = $V_{DD}Q$. Do not connect ZQ to V_{DD}.
TMS	Input	IEEE1149.1 test input This pin is used to select the JTAG test mode when using the JTAG function. Input a command to be input to the TAP controller. Input TMS according to the rising edge of TCK. This pin may be left open when not using the JTAG function.
TDI	Input	IEEE1149.1 test input This pin is used to input JTAG test data when using the JTAG function. It is used to input serial data to be input to the JTAG instruction register and data register. Input TDI according to the rising edge of TCK. This pin may be left open when not using the JTAG function.
TCK	Input	IEEE1149.1 clock input This is the clock input pin for the JTAG test when using the JTAG function. The input signals of the TMS and TDI pins are captured at the rising edge of TCK and data output to the TDO pin is started at the falling edge of TCK. Be sure to connect the pin to V_{SS} when not using the JTAG function.
TDO	Output	IEEE1149.1 test output This pin is used to output JTAG test data when using the JTAG function. This pin must be left open when not using the JTAG function.

Table 1–4. Pins Common to CIO and SIO Products (3/3)

Pin	Type	Pin Function
V_{REF}	Input	Input reference voltage This is a voltage application pin used to reference the input.
V_{EXT}	Supply	Power supply voltage This pin is used to apply the power supply voltage to the product.
V_{DD}	Supply	Power supply voltage This pin is used to apply the power supply voltage to the product.
$V_{DD}Q$	Supply	Power supply voltage This pin is used to apply the power supply voltage to I/O buffers.
V_{SS}	Supply	Ground This pin is used to ground V_{SS}.
$V_{SS}Q$	Supply	DQ ground This is an I/O buffer ground pin.
V_{TT}	Supply	Power supply voltage This is a power supply voltage application pin that applies the terminal potential.
DNU		Unused pin This is an I/O pin that is not to be used. Connect it to V_{SS}.
NF		No function This is an input pin that is not to be used. Connect it to V_{SS}.

Table 1–5. Pins Unique to CIO Products

Pin	Type	Pin Function
DQ[xx:0]	Input/Output	Data I/O These pins are alternatively used for data input and output. READ operation: Output the data to be read to the DQxx to DQ0 pins. Input a READ command and output the first data at the rising edge of QKx after the set RL (READ latency). Data is output for as much as the burst length at successive rising edges of QKx and QKx#. WRITE operation: Input the data to be written to the DQxx to DQ0 pins. Input a WRITE command and input the data at the rising edge of DKx after the set WL (WRITE latency). Data is captured for as much as the burst length at successive rising edges of DKx and DKx#.

Table 1–6. Pins Unique to SIO Products

Pin	Type	Pin Function
D[17:0]	Input	Data input These are data input pins. Input the data to be written to the D17 to D0 pins. Input a WRITE command and input the data at the rising edge of DK after the set WL (WRITE latency). Data is captured for as much as the burst length at successive rising edges of DK and DK#.
Q[17:0]	Output	Data output These are data output pins. Output the data to be read to the Q17 to Q0 pins. Input a READ command and output the first data at the rising edge of QK0/QK1 after the set RL (READ latency). Data is output for as much as the burst length at successive rising edges of QK0/QK1 and QK0#/QK1#.

1.6 Output Data and Output Data Clock

Low latency DRAM output data signals are Q and DQ, valid-data output period signal QVLD, and output data clocks QKx and QKx#. Q, DQ, and QVLD are output at the same timing as the rising edge of QKx or QK#.

1.6.1 READ latency (t_{RL})

A READ latency (t_{RL}) is the period from when a READ command is input until data is output and is specified by the number of clock cycles. With low latency DRAM, the t_{RL} to be used can be set by setting the configuration when setting the mode register. The t_{RL} that can be set, however, varies according to the operation frequency and the address multiplex function setting. Table 1-7 shows the t_{RL} configuration in non-multiplexed address mode and Table 1-8 shows the t_{RL} configuration in multiplexed address mode. See **2.3 MRS Command** for how to set the configuration.

Table 1–7. t_{RL} Configuration in Non-Multiplexed Address Mode (Common to CIO and SIO Products)

Operation Frequency	BL	Configuration			Unit
		1	2	3	
400 MHz	BL = 2	NA	NA	8	cycles
	BL = 4				
	BL = 8				
300 MHz	BL = 2	NA	6	8	
	BL = 4				
	BL = 8				
200 MHz	BL = 2	4	6	8	
	BL = 4				
	BL = 8	NA			

Remark NA (Not Available) : No setting is available.

Table 1–8. t_{RL} Configuration in Multiplexed Address Mode (Common to CIO and SIO Products)

Operation Frequency	BL	Configuration			Unit
		1	2	3	
400 MHz	BL = 2	NA	NA	9	cycles
	BL = 4				
	BL = 8				
300 MHz	BL = 2	NA	7	9	
	BL = 4				
	BL = 8				
200 MHz	BL = 2	5	7	9	
	BL = 4				
	BL = 8	NA			

Remark NA (Not Available) : No setting is available.

1.6.2 Output data and output data clock timing

Figures 1-8 and 1-9 show representative timing charts of Q, DQ, QVLD, QKx, and QKx# output by low latency DRAM.

Figure 1–8. READ Timing Chart (Non-Multiplexed Address Mode, BL = 2, Configurations 1, 2, 3)

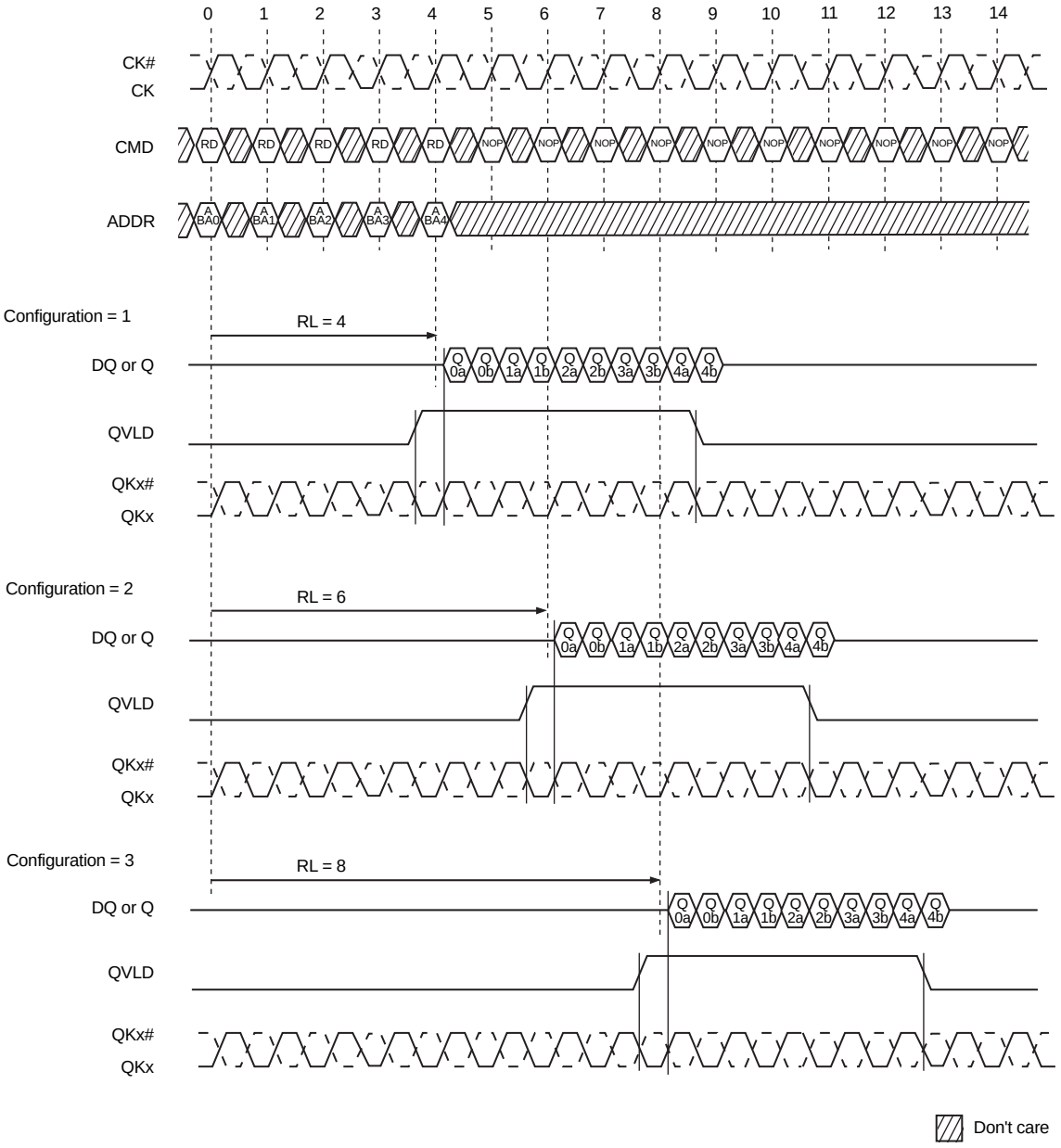
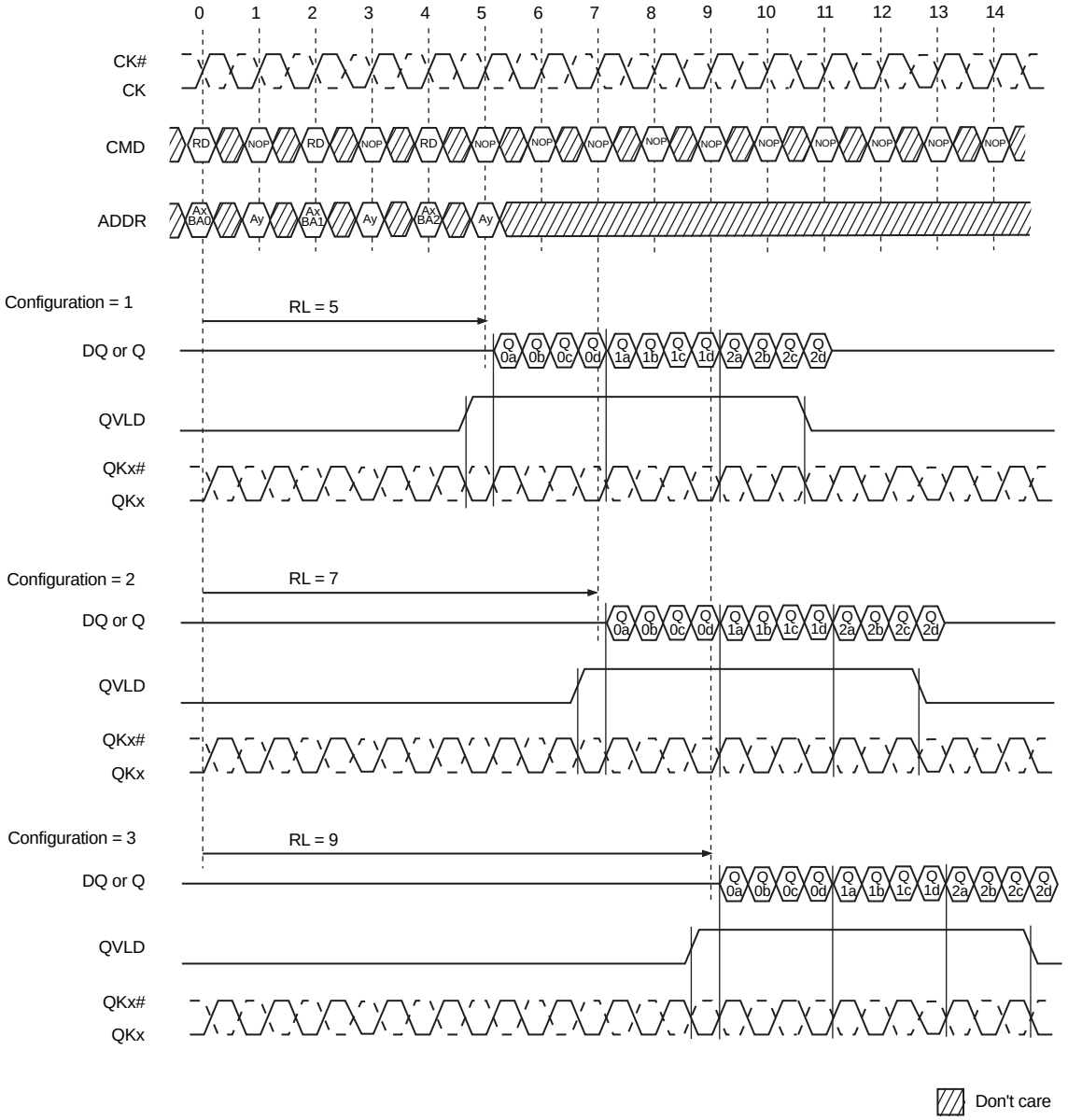


Figure 1–9. READ Timing Chart (Multiplexed Address Mode, BL = 4, Configurations 1, 2, 3)



1.7 HSTL interface and V_{REF}

Low latency DRAM uses an HSTL (high-speed transceiver logic) interface as the I/O interface. An HSTL interface distinguishes between HIGH and LOW, based on the differential potential for the reference voltage (V_{REF}). A V_{REF} power supply must therefore be supplied to the HSTL interface and, normally, the HSTL interface should be used around $V_{REF} = V_{DD}Q/2$.

When the V_{REF} voltage fluctuates during an operation, the input level of an input signal cannot be identified correctly, and malfunctioning may result; therefore, supply a stable voltage to V_{REF}.

CHAPTER 2 COMMANDS

2.1 Command Operation

Low latency DRAM is provided with five commands, which are determined by the input of CS#, WE#, REF#, Ax, or BAx.

Table 2-1 shows the types and descriptions of the commands. Table 2-2 shows the input level of each pin when a command is determined. Input each signal in synchronization with the rising edge of CK at a CK/CK# cross point. Table 2-3 shows the differences in the number of addresses used according to the burst length and bit configuration

Table 2–1. Command Types and Descriptions

Code	Command Name	Command Description
DESEL / NOP	No operation command (NOP command)	This command sets a device to no-operation and to a non-selected state.
MRS	Mode register set command	This command sets the value of the mode register, which determines the product function.
READ	READ command	This command is used to read data.
WRITE	WRITE command	This command is used to write data.
AREF	Automatic refresh command	This command is used to perform a refresh operation to retain memory cell data.

Table 2–2. Determined Commands

Code	CS#	WE#	REF#	Ax	BAx	Note
DESEL / NOP	H	X	X	X	X	
MRS	L	L	L	OPCODE[Note1]	X	3
READ	L	H	H	A	BA	4
WRITE	L	L	H	A	BA	4
AREF	L	H	L	X	BA[Note2]	

Notes 1. The address (A) input during MRS setting is used to select the MRS setting contents.

2. The bank address (BA) input during AREF is used to set the bank that performs a refresh operation.

3. Only address pins A0 to A17 are used for MRS.

4. See Table 2-3 for the number of addresses used.

Table 2–3. Number of Addresses Used

Burst Length	CIO Product			SIO Product
	x36	x18	x9	x18
BL = 2	A [18 : 0]	A [19 : 0]	A [20 : 0]	A [19 : 0]
BL = 4	A [17 : 0]	A [18 : 0]	A [19 : 0]	A [18 : 0]
BL = 8	NA	A [17 : 0]	A [18 : 0]	A [17 : 0]

2.2 DESEL/NOP Command

The internal state of a device will be set to non-selectable by inputting a no operation command at the rise timing of CK. Unnecessary commands can be prevented from being input to the device internal state during an idle period by using this command.

2.3 MRS Command

This command is used to set the value of the mode register, which determines the product function of a device. The following six functions can be set by selecting the register value.

- Configuration
- Burst length
- Address multiplex function
- PLL function
- Output impedance mode function
- ODT function

2.3.1 How to set MRS command

How to the set the MRS command differs depending on whether the address multiplex function is in non-multiplexed address mode or multiplexed address mode.

(1) How to set MRS command in non-multiplexed address mode

Input CS# = LOW, WE# = LOW, and REF# = LOW at the rising edge of CK at a CK/CK# cross point. At the same time, input the expected value, which set the function to be used, to address pins A0 to A17. The period from inputting the MRS command until the function settings are completed is specified by t_{MRSC}. Figure 2-1 shows the MRS command input timing chart, Figure 2-2 shows the pin input states during MRS command input, and Table 2-4 shows the address pin allocation.

Figure 2–1. MRS Command Input Timing Chart (Non-Multiplexed Address Mode)

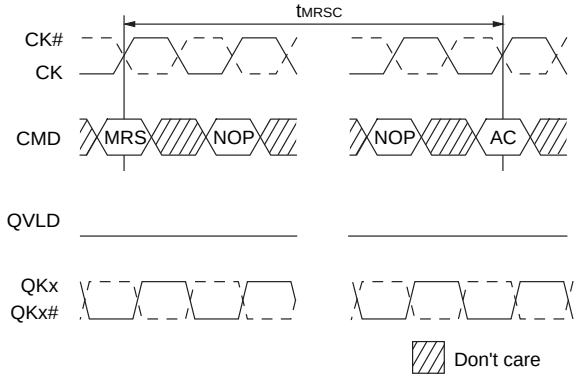


Figure 2–2. Pin Input States During MRS Command Input (Non-Multiplexed Address Mode)

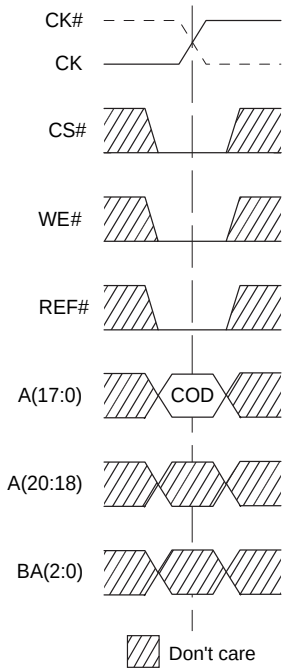


Table 2–4. Address Pin Allocation with Respect to Function Setting (Non-Multiplexed Address Mode)

Address Pin	MRS Allocation	Remark
A0, A1, A2	Configuration setting	
A3, A4	Burst length setting	
A5	Address multiplex function setting	
A6	Unused	
A7	PLL function setting	
A8	Output impedance mode function setting	
A9	ODT function setting	
A [xx:10]	For future function expansion	All fixed to LOW

(2) How to set MRS in multiplexed address mode

Input CS# = LOW, WE# = LOW, and REF# = LOW at the rising edge of CK at a CK/CK# cross point. Input the expected value, which set the function to be used, to address pins A0, A3 to A5, A8 to A10, A13, A14, A17, and A18, in two separate cycles. The period from inputting the MRS command until the function settings are completed is specified by t_{MRSC}. Figure 2-3 shows the MRS command input timing chart, Figure 2-4 shows the pin input states during MRS command input, and Table 2-5 shows the address pin allocation.

Figure 2–3. MRS Setting Timing Chart (Multiplexed Address Mode)

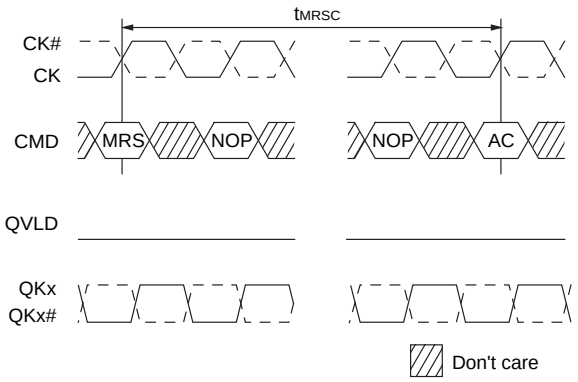


Figure 2–4. How to Input to Pins During MRS Command Input (Multiplexed Address Mode)

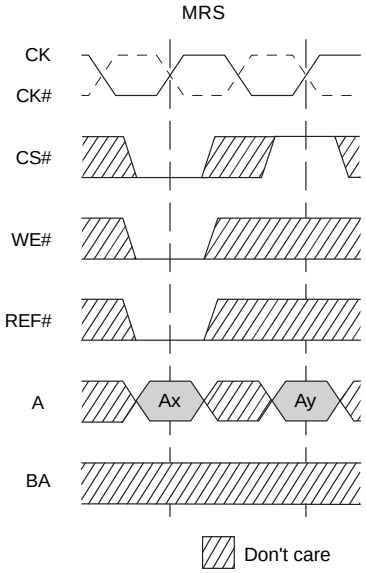


Table 2–5. Address Pin Allocation of MRS Setting (Multiplexed Address Mode)

Address Pin		MRS Allocation	Remark
Ax	Ay		
A0	A3, A4	Configuration setting	
A3, A4	-	Burst length setting	
A5	-	Address multiplex function setting	
-	A8	Unused	
-	A9	PLL function setting	
A8	-	Output impedance mode function setting	
A9	-	ODT function setting	
A[xx:10]		For future function expansion	All fixed to LOW

2.3.2 Configuration setting

Low latency DRAM has three predetermined combinations (configurations) of random cycle time t_{RC}, READ latency t_{RL}, and WRITE latency t_{WL}. t_{RC}, t_{RL}, and t_{WL} vary between non-multiplexed address mode and multiplexed address mode. The configuration settings in non-multiplexed address mode and multiplexed address mode are described below.

(1) Configuration settings in non-multiplexed address mode

The configuration is set according to the expected values of address pins A0, A1, and A2. Input to the address pins is performed according to the MRS command input timing. Table 2-6 shows the configuration setting contents and Table 2-7 shows the address pin expected values related to the configuration settings.

Table 2–6. Configuration Setting Contents (Non-Multiplexed Address Mode)

Frequency	Symbol	Configuration			Unit
		1 Note	2	3	
	t_{RC}	4	6	8	cycles
	t_{RL}	4	6	8	
	t_{WL}	5	7	9	
400 MHz	t_{RC}	NA	NA	20.0	ns
	t_{RL}	NA	NA	20.0	
	t_{WL}	NA	NA	22.5	
300 MHz	t_{RC}	NA	20.0	26.7	
	t_{RL}	NA	20.0	26.7	
	t_{WL}	NA	23.3	30.0	
200 MHz	t_{RC}	20.0	30.0	40.0	
	t_{RL}	20.0	30.0	40.0	
	t_{WL}	25.0	35.0	45.0	

Note Configuration 1 cannot be set when BL = 8.

Remark NA (Not Available) : No setting is available.

Table 2–7. Configuration Settings (Non-Multiplexed Address Mode)

A2	A1	A0	Configuration
0	0	0	1 Note (default)
0	0	1	1 Note
0	1	0	2
0	1	1	3
1	0	0	For future expansion
1	0	1	For future expansion
1	1	0	For future expansion
1	1	1	For future expansion

Note Configuration 1 cannot be set when BL = 8.

(2) Configuration settings in multiplexed address mode setting

The configuration is set according to the expected values of address pins A0, A3, and A4. Input to the address pins is performed separately in two successive cycles following the MRS command input timing. Table 2-8 shows the configuration setting contents and Table 2-9 shows the address pin expected values related to the configuration settings.

Table 2–8. Configuration Setting Contents (Multiplexed Address Mode)

Frequency	Symbol	Configuration			Unit
		1 Note	2	3	
	t_{RC}	4	6	8	cycles
	t_{RL}	5	7	9	
	t_{WL}	6	8	10	
400 MHz	t_{RC}	NA	NA	20.0	ns
	t_{RL}	NA	NA	22.5	
	t_{WL}	NA	NA	25.0	
300 MHz	t_{RC}	NA	20.0	26.7	
	t_{RL}	NA	23.3	30.0	
	t_{WL}	NA	26.7	33.3	
200 MHz	t_{RC}	20.0	30.0	40.0	
	t_{RL}	25.0	35.0	45.0	
	t_{WL}	30.0	40.0	50.0	

Note Configuration 1 cannot be set when BL = 8.

Remark NA (Not Available) : No setting is available.

Table 2–9. Configuration Settings (Multiplexed Address Mode)

A4y	A3y	A0x	Configuration
0	0	0	1 Note (default)
0	0	1	1 Note
0	1	0	2
0	1	1	3
1	0	0	For future expansion
1	0	1	For future expansion
1	1	0	For future expansion
1	1	1	For future expansion

Note Configuration 1 cannot be set when BL = 8.

2.3.3 Burst length (BL) setting

The burst length of low latency DRAM can be set to BL = 2, 4, or 8. BL = 8, however, cannot be set for CIO x36 products. The BL settings for non-multiplexed address mode and multiplexed address mode differ and are therefore separately described below.

(1) BL setting in non-multiplexed address mode

The burst length is set according to the expected values of address pins A3 and A4. Table 2-10 shows the address pin inputs of the BL settings. Input to A3 and A4 when inputting the MRS command.

Table 2–10. BL Settings (Non-Multiplexed Address Mode)

A4	A3	BL
0	0	2 (default)
0	1	4
1	0	8[Note]
1	1	Invalid

Note BL = 8 cannot be set for CIO x36 products.

(2) BL setting in multiplexed address mode

The burst length is set according to the expected values of address pins A3 and A4. Table 2-11 shows the address pin inputs of the BL settings. Input to A3x and A4x when inputting the MRS command.

Table 2–11. BL Settings (Multiplexed Address Mode)

A4x	A3x	BL
0	0	2 (default)
0	1	4
1	0	8[Note]
1	1	Invalid

Note BL = 8 cannot be set for CIO x36 products.

2.3.4 Non-multiplexed address mode and multiplexed address mode settings

With low latency DRAM, non-multiplexed address mode, in which all address inputs are captured in one cycle in a batch, or multiplexed address mode, in which address inputs as X-address inputs and Y-address inputs are captured in two separate cycles, can be set.

(1) Address multiplex function setting in non-multiplexed address mode

Non-multiplexed address mode or multiplexed address mode is set according to the expected value of address pin A5. Table 2-12 shows the address pin input in non-multiplexed address mode. Input to A5 when inputting the MRS command.

Table 2–12. Address Multiplex Function Setting (Non-Multiplexed Address Mode)

A5	Address Multiplex Function
0	Non-multiplexed address mode (default)
1	Multiplexed address mode

(2) Address multiplex function setting in multiplexed address mode

Non-multiplexed address mode or multiplexed address mode can be set according to the expected value of address pin A5. Table 2-13 shows the address pin input in multiplexed address mode. Input to A5x when inputting the MRS command.

Table 2–13. Address Multiplex Function Setting (Multiplexed Address Mode)

A5x	Address Multiplex Function
0	Non-multiplexed address mode (default)
1	Multiplexed address mode

2.3.5 PLL setting

Low latency DRAM is provided with a PLL circuit which is used to adjust the output timing and which can be enabled or disabled. Enable the PLL circuit for a normal operation. On the other hand, when performing a system operation check at a low speed, the system can be operated at a clock cycle speed slower than that restricted by t_{CK} (MAX.) and t_{DK} (MAX.) by disabling the PLL circuit. In this case, however, the AC/DC characteristics will not be guaranteed.

The PLL settings differ in non-multiplexed address mode and multiplexed address mode and are therefore separately described below.

(1) PLL setting in non-multiplexed address mode

The PLL circuit is enabled or disabled according to the expected value of address pin A7. Table 2-14 shows the address pin input during the PLL setting. Input to A7 when inputting the MRS command.

Table 2–14. PLL Setting (Non-Multiplexed Address Mode)

A7	PLL Function
0	Disables PLL circuit (default)
1	Enables PLL circuit

(2) PLL setting in multiplexed address mode

The PLL circuit is enabled or disabled according to the expected value of address pin A9. Table 2-15 shows the address pin input during the PLL setting. Input to A9y at the rising edge of CK following the CK when the MRS command was input.

Table 2–15. PLL Setting (Multiplexed Address Mode)

A9y	PLL Function
0	Disables PLL circuit (default)
1	Enables PLL circuit

2.3.6 Output impedance mode setting

A function to adjust the output impedance of output pins is provided for which the following two settings can be selected.

(1) Referencing the resistance preset in the device and setting the impedance to that value

(2) Referencing the value of resistor RQ to be externally connected to the ZQ pin and setting the impedance to RQ/5 Ω

The output impedance mode settings differ in non-multiplexed address mode and multiplexed address mode and are therefore separately described below. See **CHAPTER 6 OUTPUT IMPEDANCE MATCHING** for details.

(1) Output impedance mode setting in non-multiplexed address mode

The setting to adjust the output impedance according to the expected value of address pin A8 can be switched. Table 2-16 shows the address pin input during the mode setting. Input to A8 when inputting the MRS command.

Table 2–16. Output Impedance Mode Setting (Non-Multiplexed Address Mode)

A8	Impedance Mode
0	Sets impedance to device-internal 50 Ω (default)
1	Sets impedance to value of externally connected resistor RQ/5 Ω

(2) Output impedance mode setting in multiplexed address mode

The setting to adjust the output impedance according to the expected value of address pin A8 can be switched. Table 2-17 shows the address pin input during the mode setting. Input to A8x when inputting the MRS command.

Table 2–17. Output Impedance Mode Setting (Multiplexed Address Mode)

A8x	Impedance Mode
0	Sets impedance to device-internal 50 Ω (default)
1	Sets impedance to value of externally connected resistor RQ/5 Ω

2.3.7 ODT (On Die Termination) function setting

The ODT function can be switched to be enabled or disabled. The ODT settings differ in non-multiplexed address mode and multiplexed address mode and are therefore separately described below.

(1) ODT setting in non-multiplexed address mode

The ODT function can be switched to be enabled or disabled according to the expected value of address pin A9. Table 2-18 shows the address pin input during the setting. Input to A9 when inputting the MRS command.

Table 2–18. ODT Function Setting (Non-Multiplexed Address Mode)

A9	ODT Function
0	Disabled (default)
1	Enabled

(2) ODT setting in multiplexed address mode

The ODT function can be switched to be enabled or disabled according to the expected value of address pin A9. Table 2-19 shows the address pin input during the setting. Input to A9x when inputting the MRS command.

Table 2–19. ODT Function Setting (Multiplexed Address Mode)

A9x	ODT Function
0	Disabled (default)
1	Enabled

2.4 READ and WRITE Commands

READ or WRITE operation can be performed by inputting READ command or WRITE command at the rise timing of CK at a CK/CK# cross point, at the same as inputting an address or bank address. READ and WRITE timings differ according to differences in the I/O setup, configuration, burst length, and address multiplex mode.

(1) CIO and SIO products

With both CIO and SIO products, commands are input in the same manner when processing successive data read or successive WRITE operations. With CIO products, however, when WRITE operation is switched to READ operation, a NOP cycle is required between the WRITE command input and READ command input in order to prevent a bus conflict. With SIO products, no NOP cycle is required to be inserted, because data ports are separately provided for input and output.

Figure 2-5 shows an example of a CIO product timing chart and Figure 2-6 shows an example of an SIO product timing chart.

Figure 2–5. CIO Product Timing Chart (Non-Multiplexed Address Mode, BL = 2, Configuration 1)

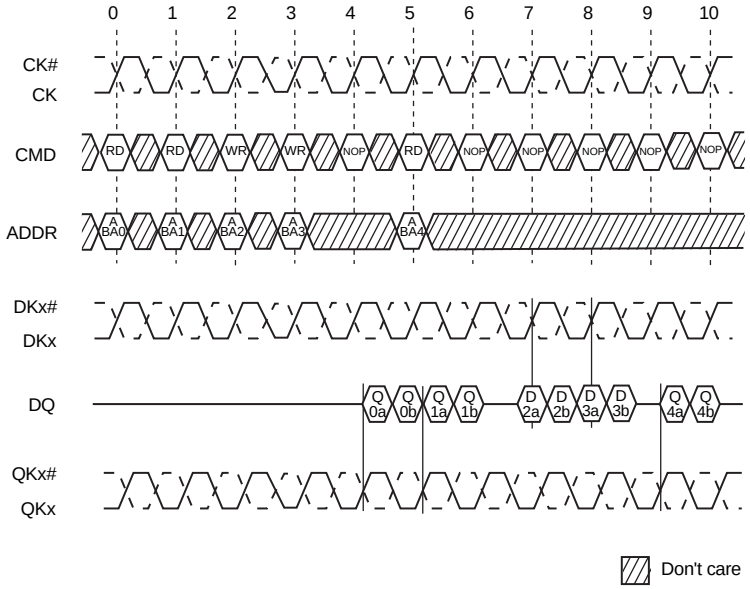
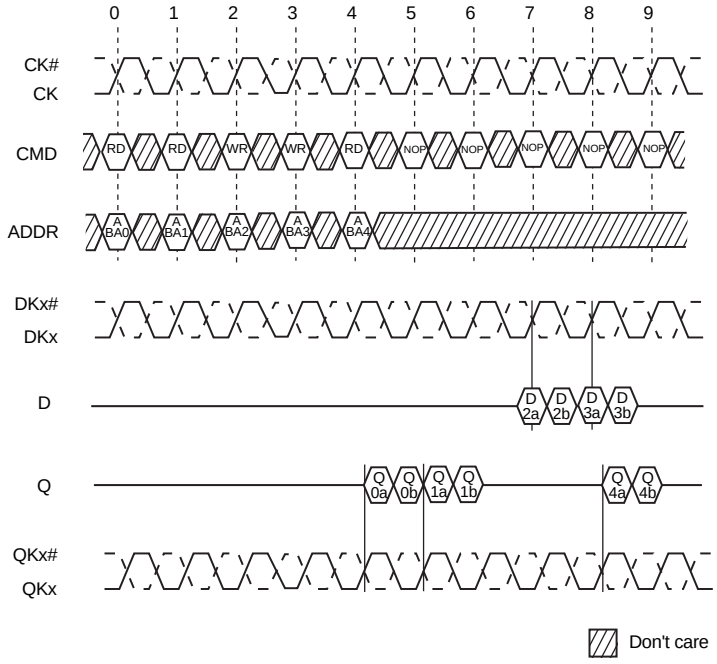


Figure 2–6. SIO Product Timing Chart (Non-Multiplexed Address Mode, BL = 2, Configuration 1)



(2) Configuration setting

t_{RC}, t_{RL}, and t_{WL} differ depending on the configuration. The differences in READ and WRITE timings according to differences in the configuration are described below.

Figure 2-7. Timing Charts for Configuration When Processing Successive READ Commands

Figure 2-8. Timing Charts for Configuration When Processing Successive WRITE Commands

Figure 2-9. Timing Charts for Configuration When READ Commands Are Switched to WRITE Commands

Figure 2-10. Timing Charts for Configuration When WRITE Commands Are Switched to READ Commands

Figure 2–7. Timing Charts of Successive READ Commands (CIO Products, Non-Multiplexed Address Mode, BL = 2, for Each Configuration)

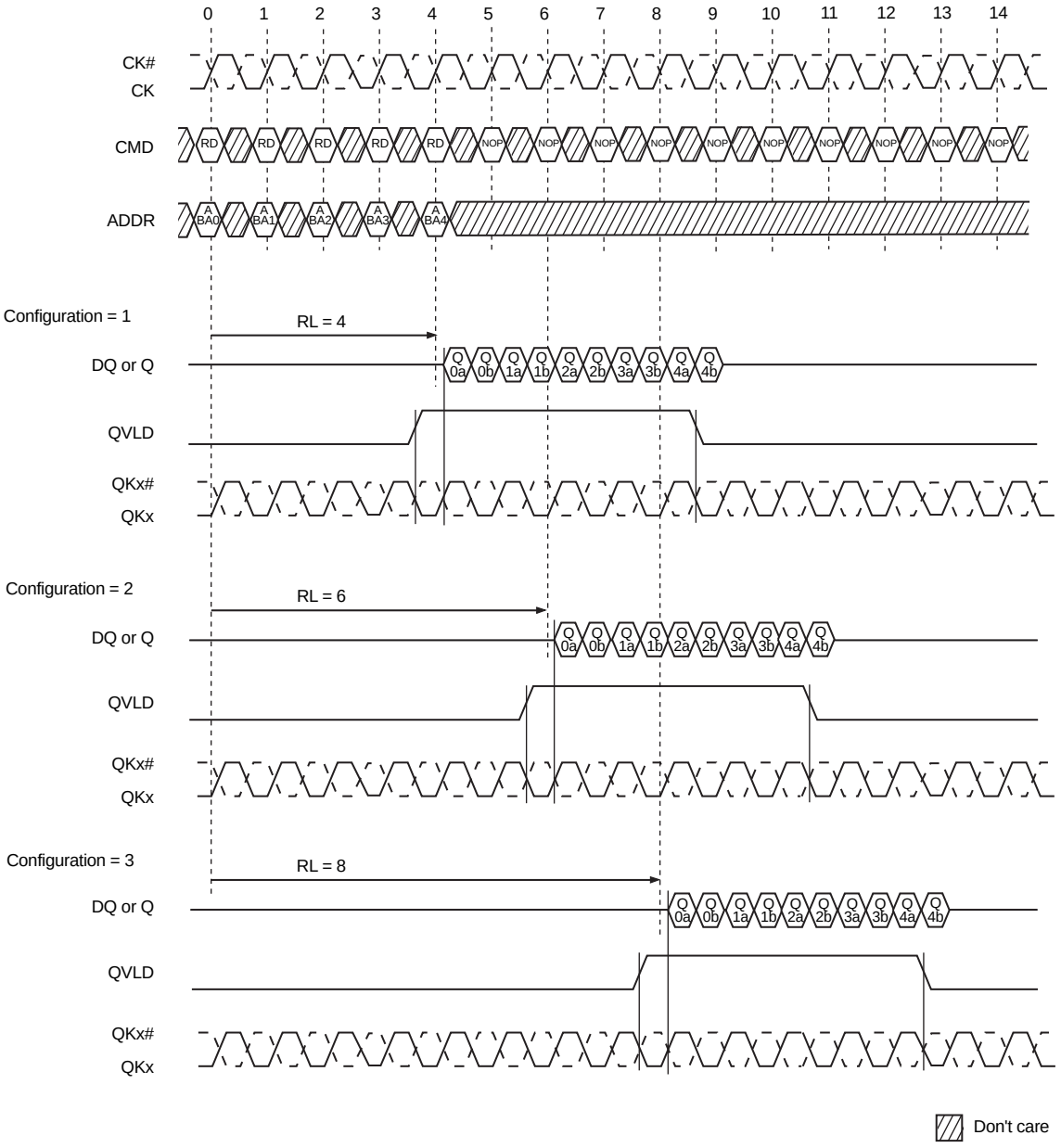


Figure 2–8. Timing Charts of Successive WRITE Commands (CIO Products, Non-Multiplexed Address Mode, BL = 2, for Each Configuration)

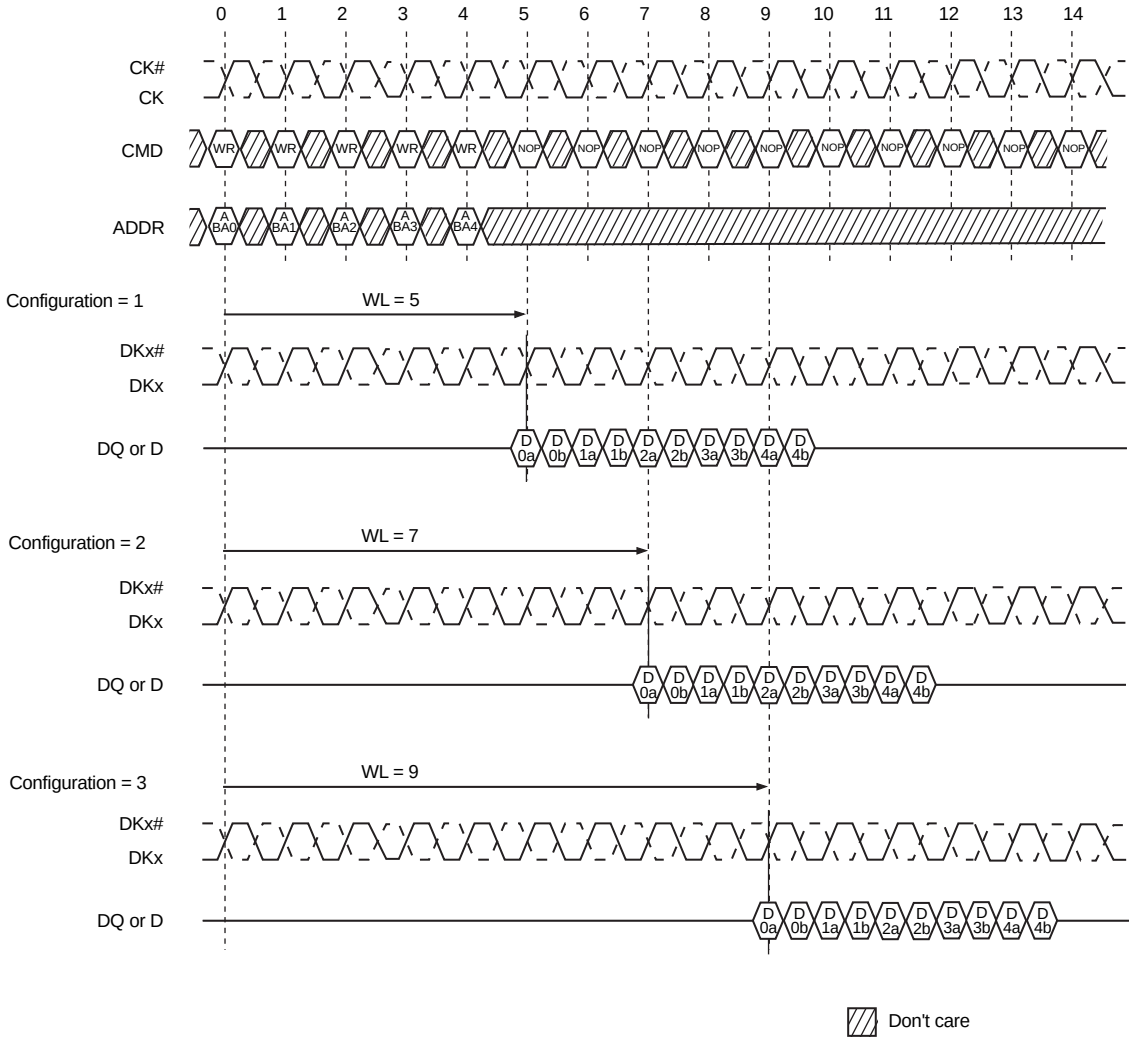


Figure 2–9. Timing Charts When READ Commands Are Switched to WRITE Commands (CIO Products, Non-Multiplexed Address Mode, BL = 2, for Each Configuration)

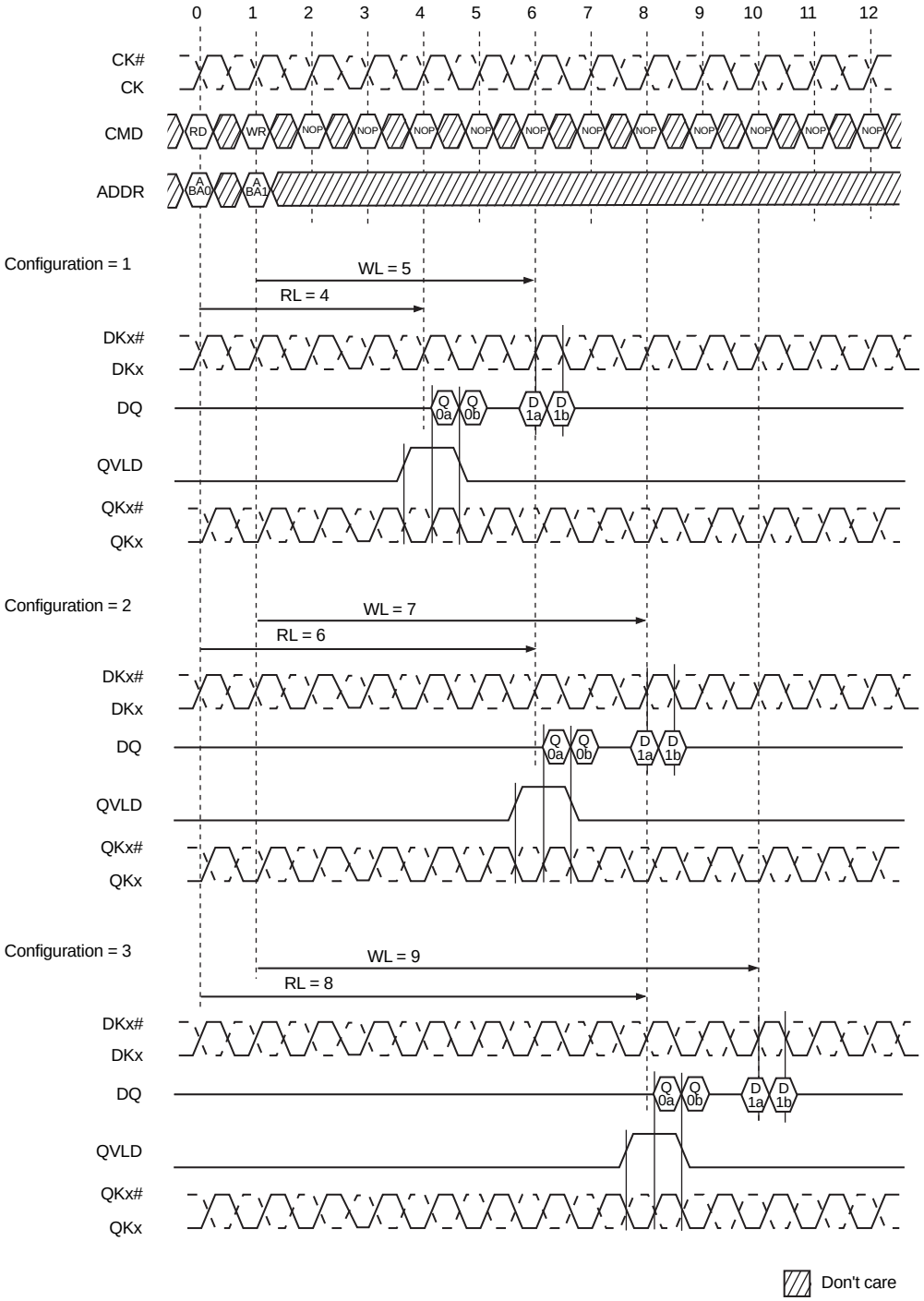
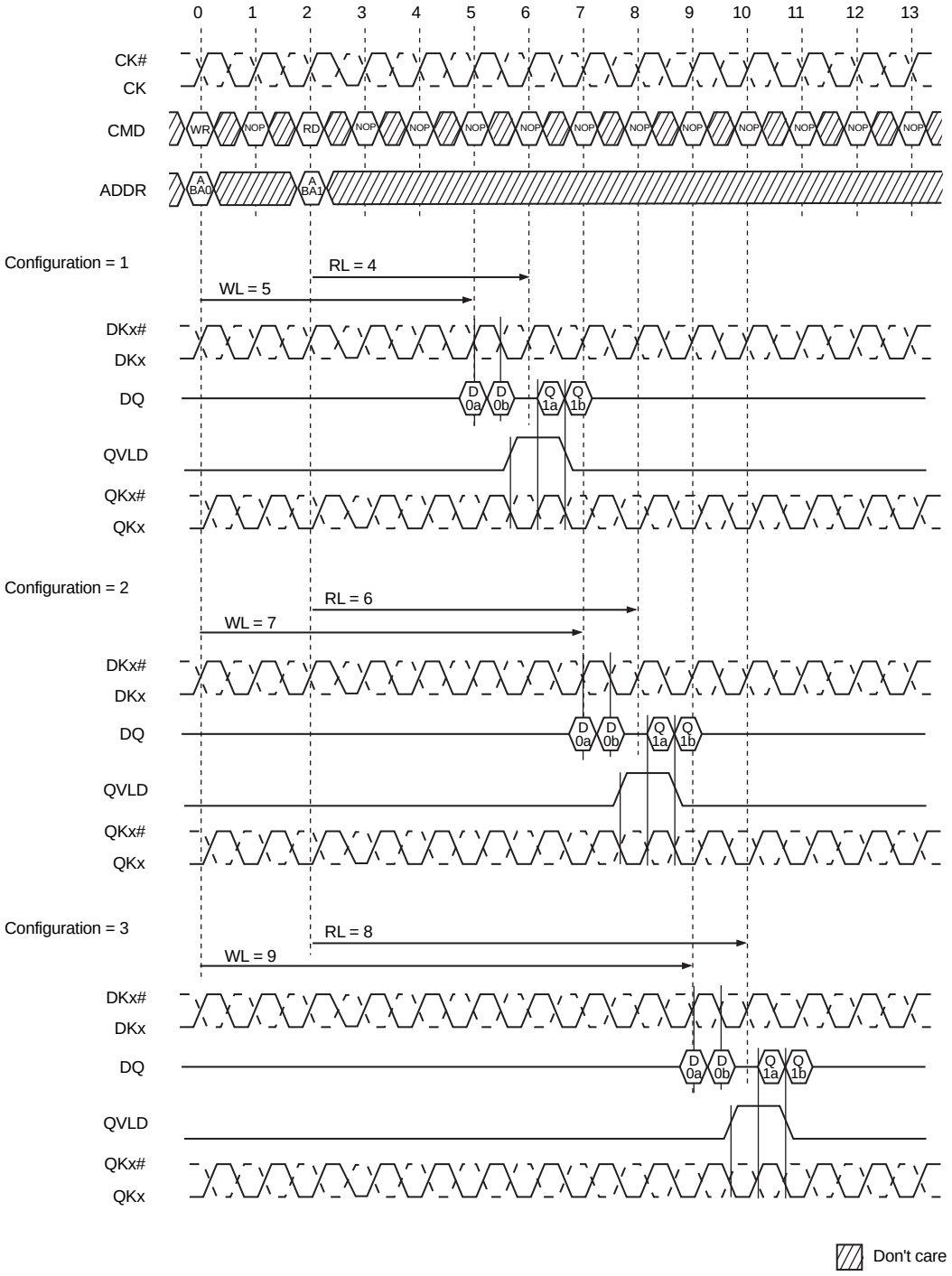


Figure 2–10. Timing Chart When WRITE Commands Are Switched to READ Commands (CIO Products, Non-Multiplexed Address Mode, BL = 2, for Each Configuration)



(3) Burst length (BL)

The command input timings differ depending on the burst length to be set (BL = 2, 4, 8). The differences in READ and WRITE timings according to differences in the burst length are described below.

Figure 2-11. Timing Charts for BL Settings When Processing Successive READ Commands

Figure 2-12. Timing Charts for BL Settings When Processing Successive WRITE Commands

Figure 2-13. Timing Charts for BL Settings When READ Commands Are Switched to WRITE Commands

Figure 2-14. Timing Charts for BL Settings When WRITE Commands Are Switched to READ Commands

Figure 2–11. Timing Charts of Successive READ Commands (CIO Products, Non-Multiplexed Address Mode, Configuration 2, for each BL)

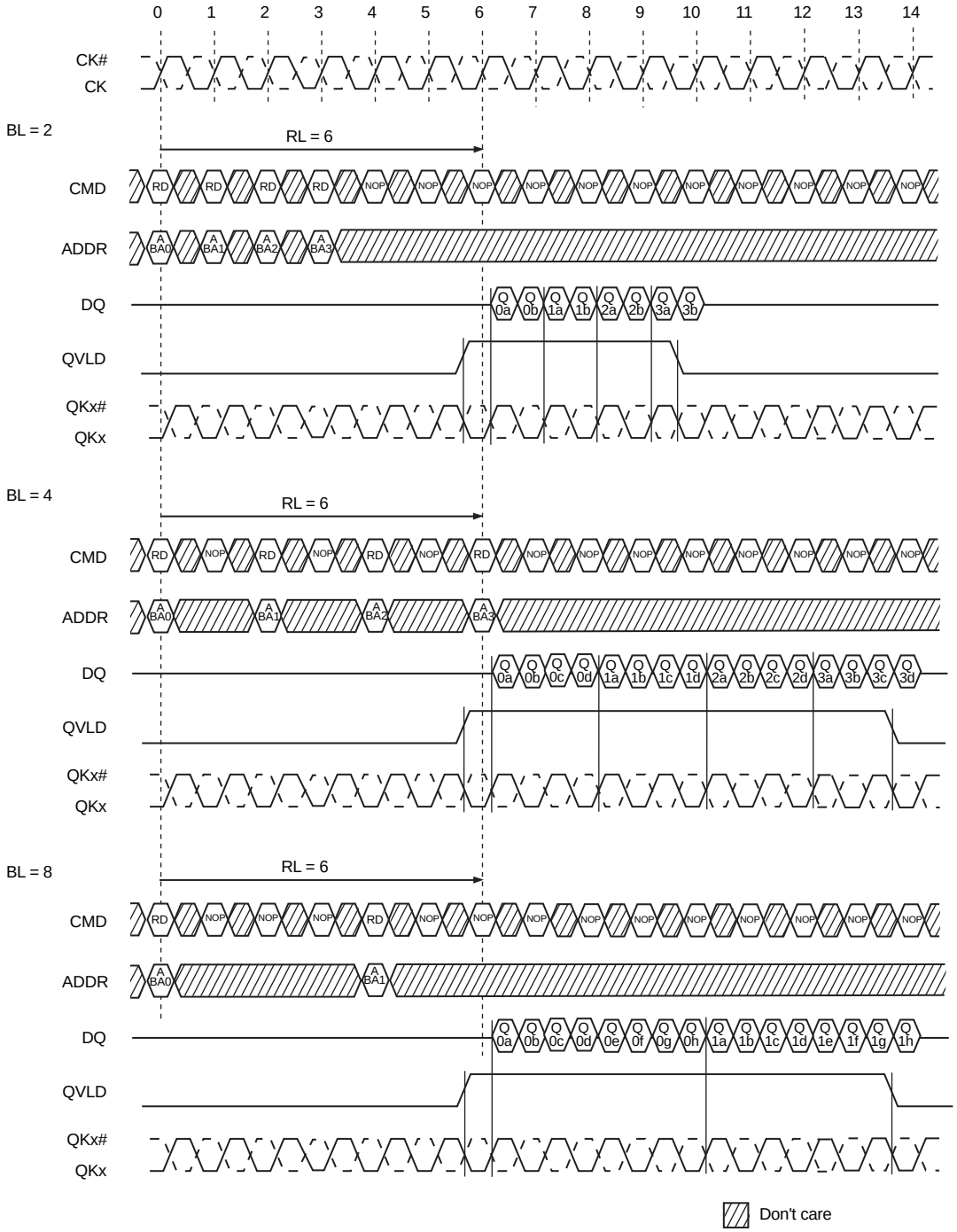


Figure 2–12. Timing Charts of Successive WRITE Commands (CIO Products, Non-Multiplexed Address Mode, Configuration 2, for each BL)

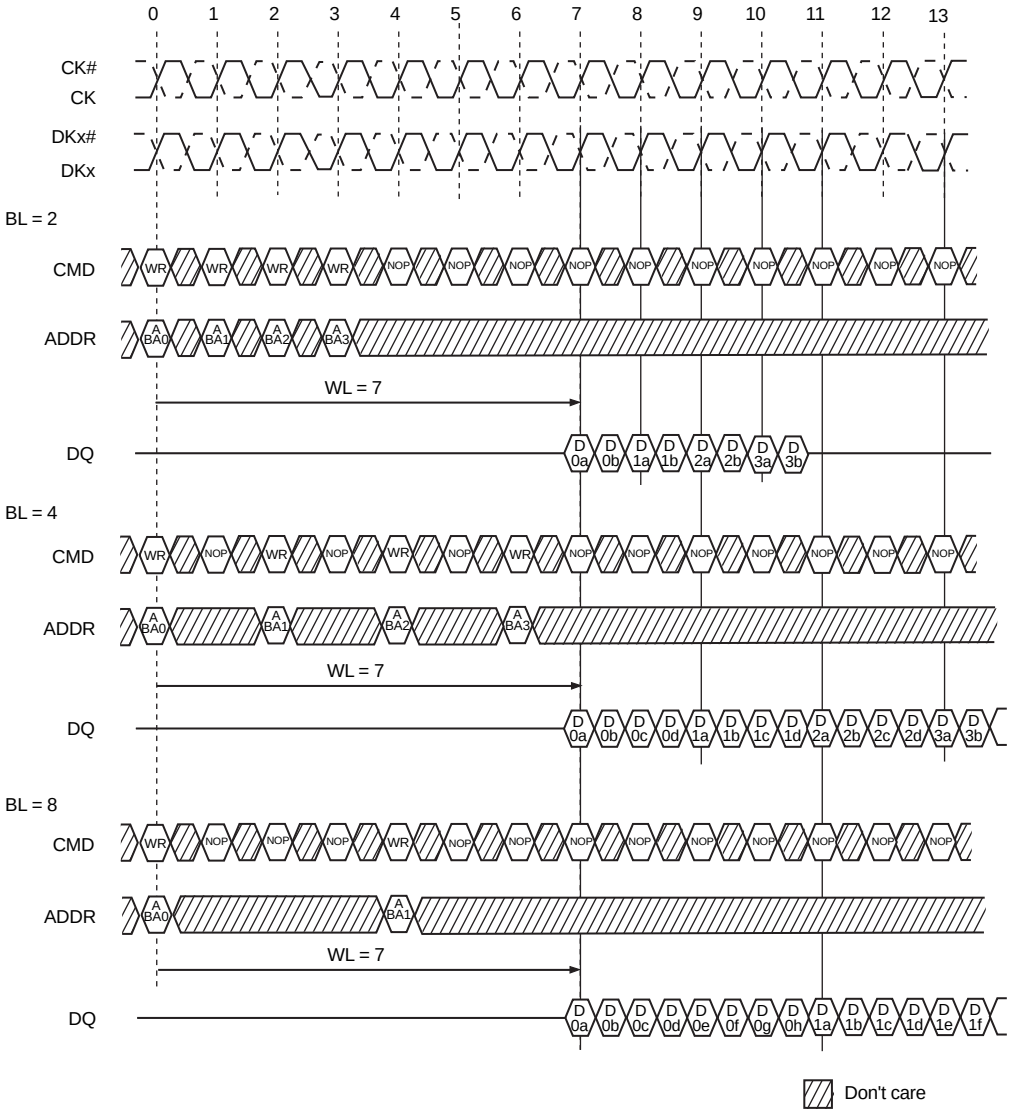


Figure 2–13. Timing Charts When READ Commands Are Switched to WRITE Commands (CIO Products, Non-Multiplexed Address Mode, Configuration 2, for each BL)

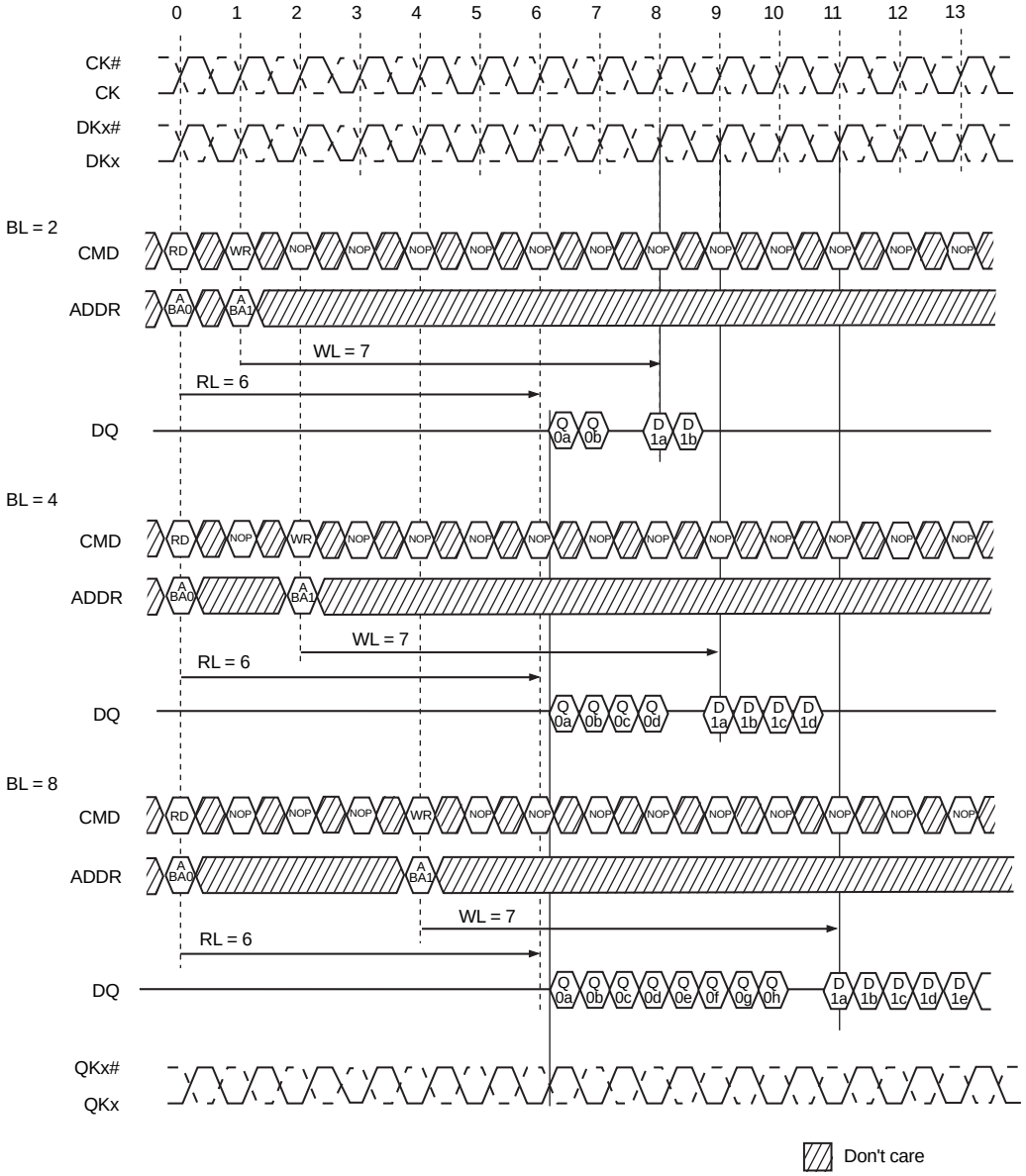
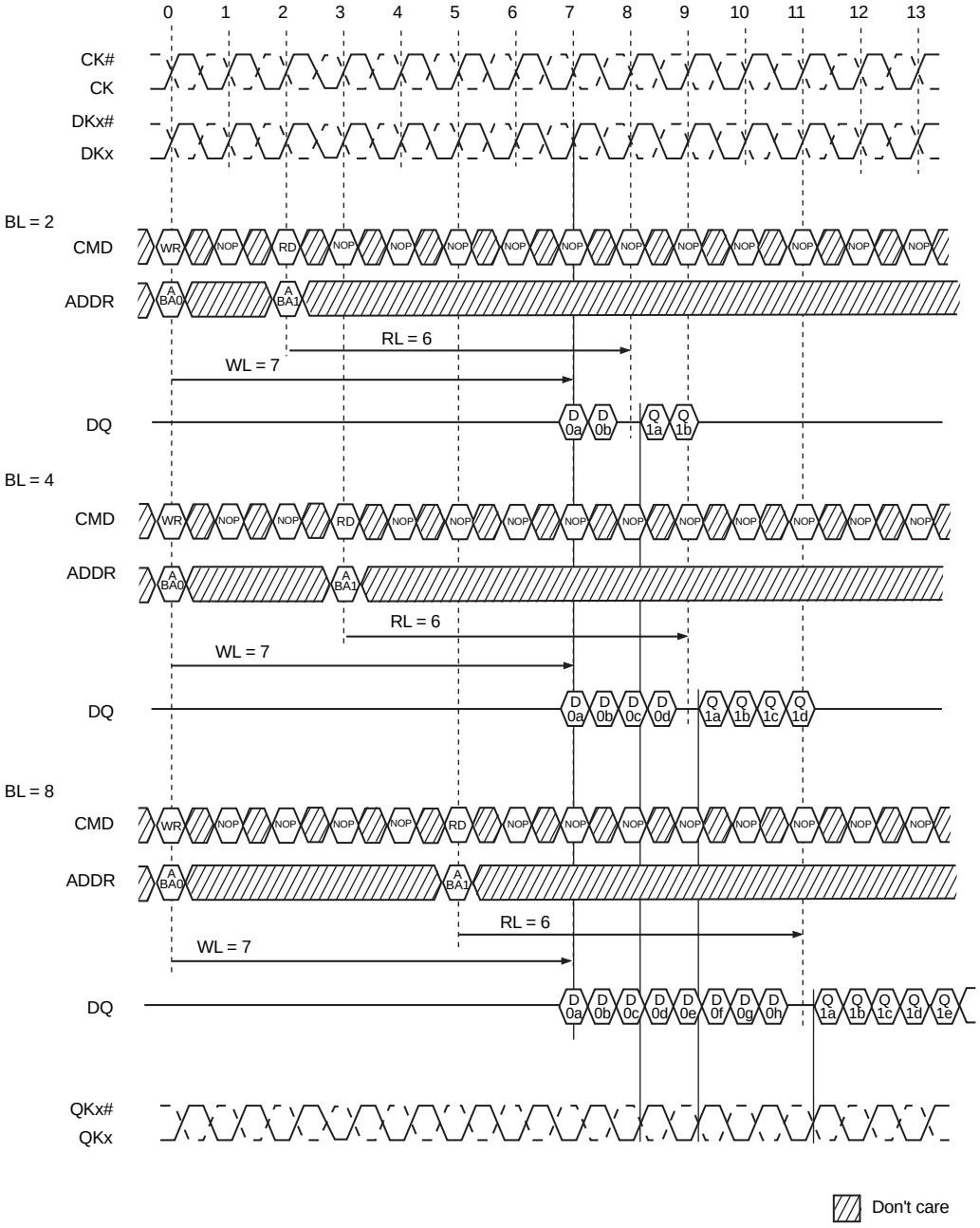


Figure 2–14. Timing Charts When WRITE Commands Are Switched to READ Commands (CIO Products, Non-Multiplexed Address Mode, Configuration 2, for each BL)



(4) Multiplexed address mode

t_{RL} and t_{WL} differ in non-multiplexed address mode and multiplexed address mode. The differences in READ and WRITE timings according to differences between non-multiplexed address mode and multiplexed address mode are described below.

Figure 2-15. Timing Chart of CIO Products in Non-Multiplexed Address Mode

Figure 2-16. Timing Chart of CIO Products in Multiplexed Address Mode

Figure 2-17. Timing Chart of SIO Products in Non-Multiplexed Address Mode

Figure 2-18. Timing Chart of SIO Products in Multiplexed Address Mode

Figure 2–15. Timing Chart of CIO Products in Non-Multiplexed Address Mode (BL = 4, Configuration 1)

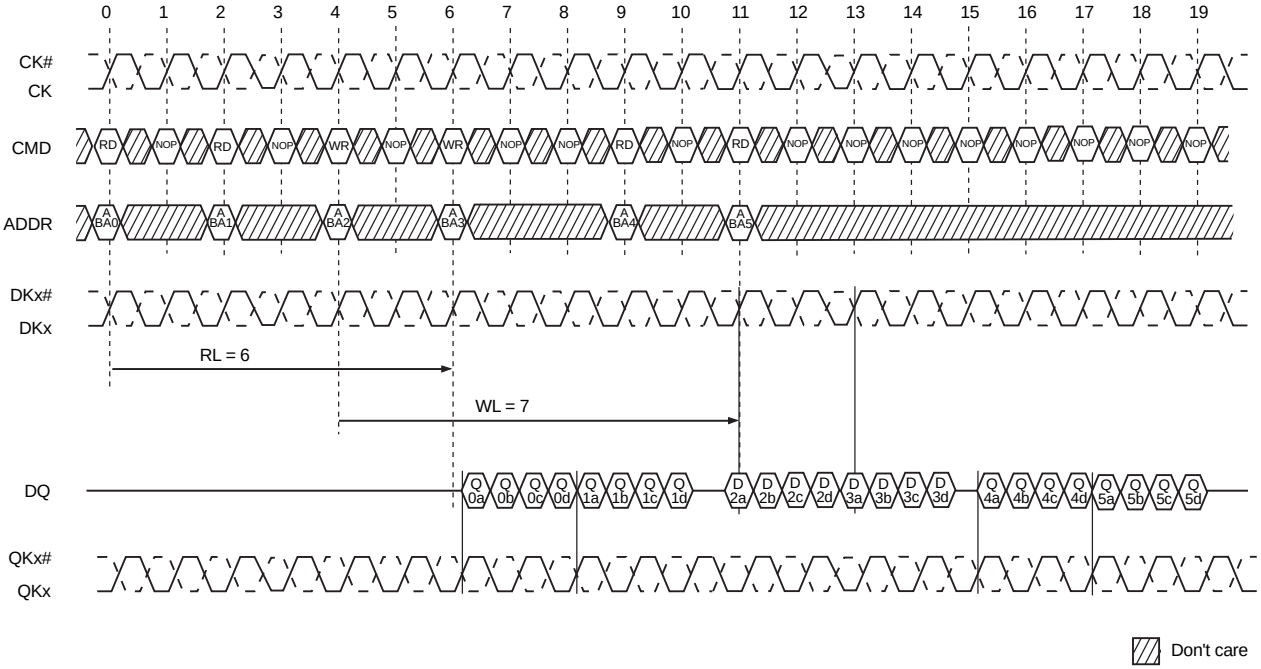


Figure 2–16. Timing Chart of CIO Products in Multiplexed Address Mode (BL = 4, Configuration 1)

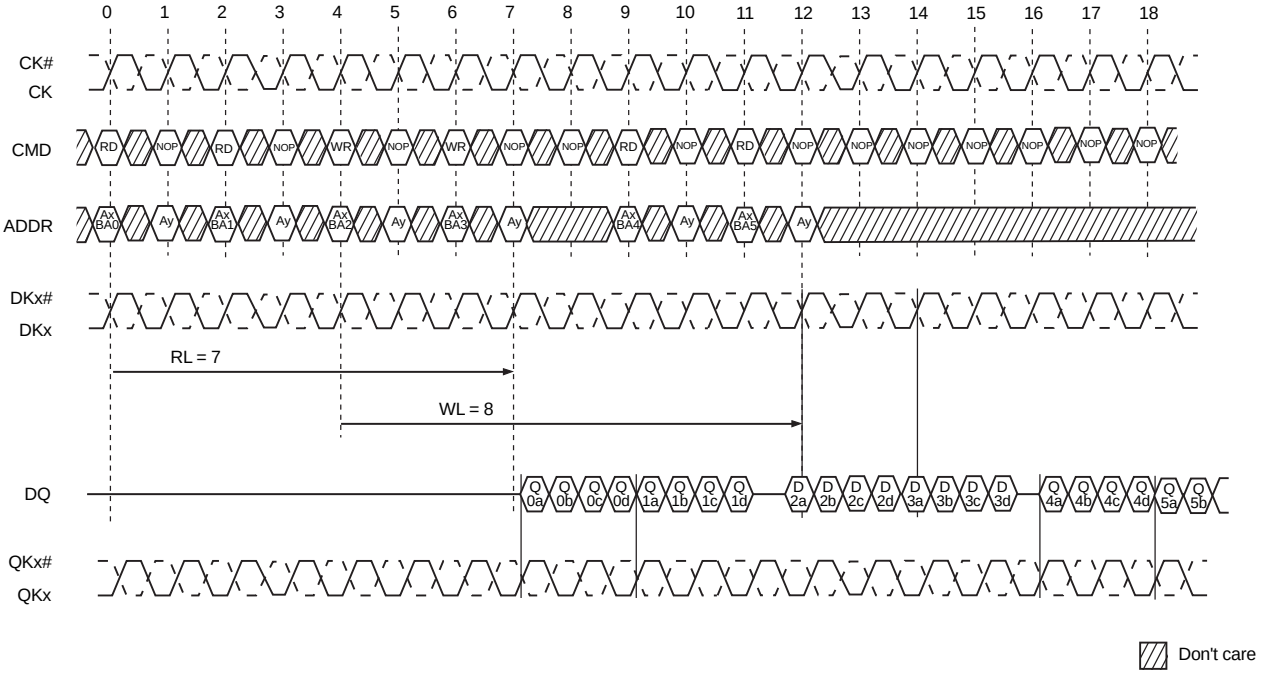


Figure 2–17. Timing Chart of SIO Products in Non-Multiplexed Address Mode (BL = 4, Configuration 1)

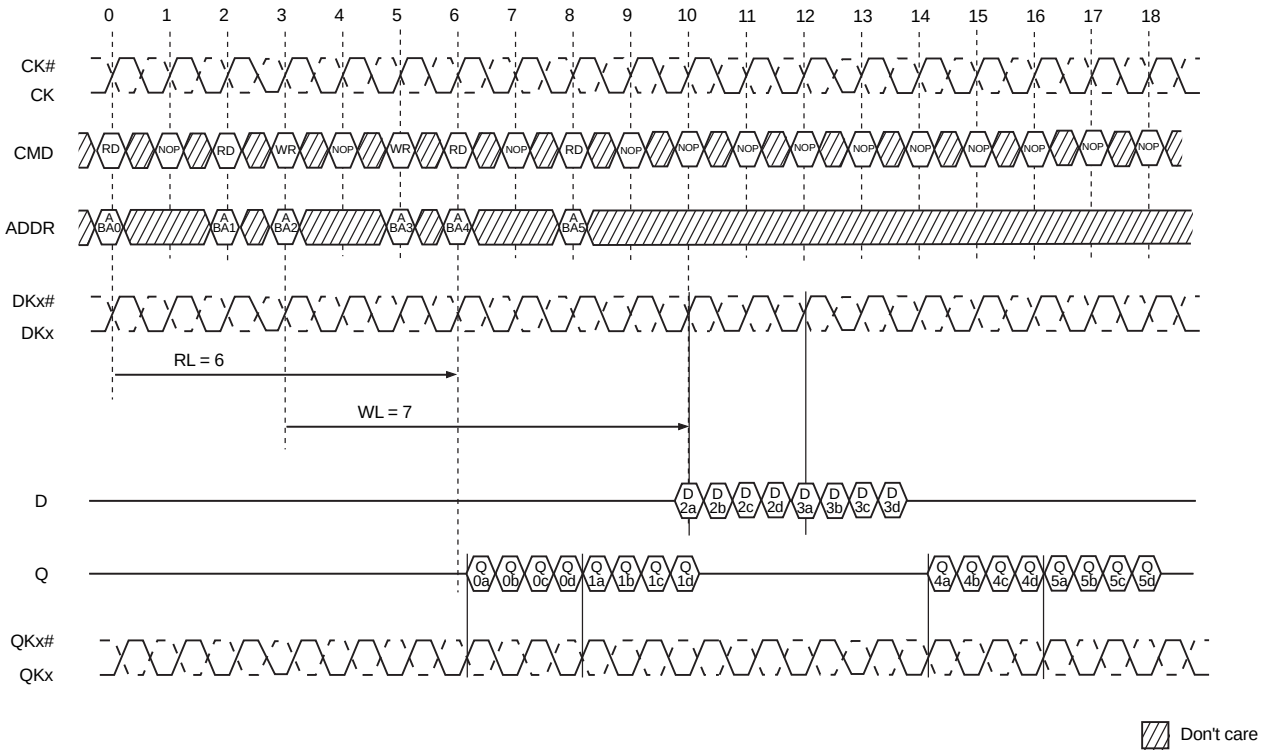
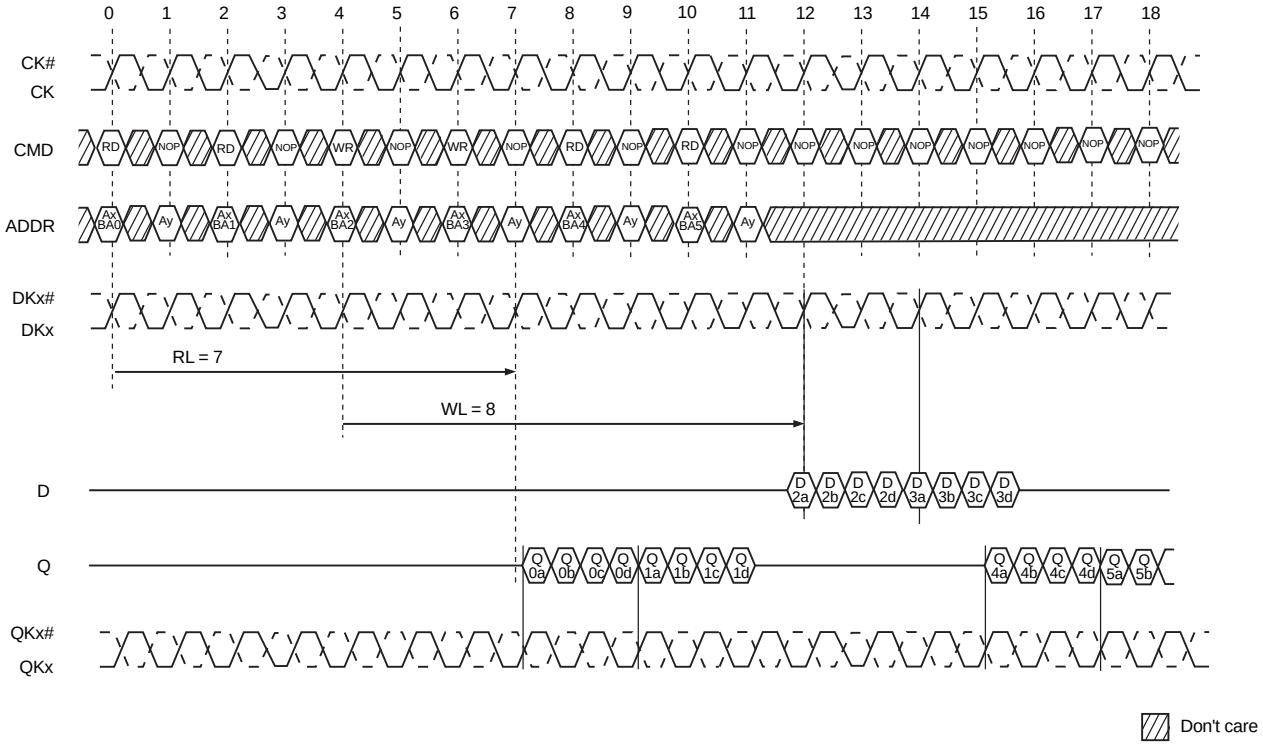


Figure 2–18. Timing Chart of SIO Products in Multiplexed Address Mode (BL = 4, Configuration 1)



(5) Timing charts

Timing charts for various operations are shown below. Figures 2-19 to 2-30 show the timing charts of the settings shown in Table 2-20. Figures 2-31 and 2-32 show the timing charts of READ and WRITE interleave operations, which enable maximized band widths.

Table 2–20. Timing Charts of READ and WRITE Operations

I/O	Multiplexed Address Mode	BL	Configuration	See
CIO	Non-MUX	2	1	Figure 2-19
		4	1	Figure 2-20
		8	2	Figure 2-21
	MUX	2	1	Figure 2-22
		4	1	Figure 2-23
		8	2	Figure 2-24
SIO	Non-MUX	2	1	Figure 2-25
		4	1	Figure 2-26
		8	2	Figure 2-27
	MUX	2	1	Figure 2-28
		4	1	Figure 2-29
		8	2	Figure 2-30

Figure 2–19. Timing Chart (CIO Products, Non-Multiplexed Address Mode, BL = 2, Configuration = 1)

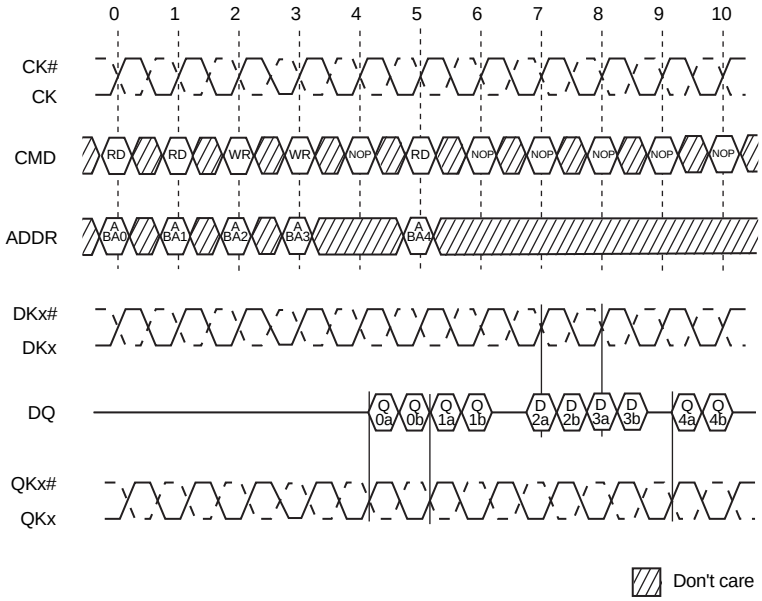


Figure 2–20. Timing Chart (CIO Products, Non-Multiplexed Address Mode, BL = 4, Configuration = 1)

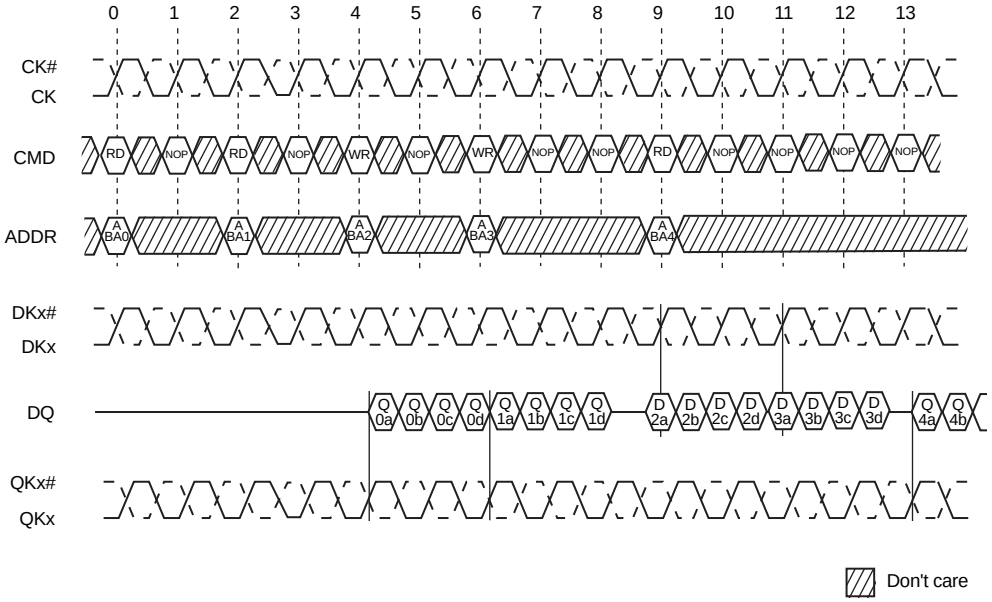


Figure 2–21. Timing Chart (CIO Products, Non-Multiplexed Address Mode, BL = 8, Configuration = 2)

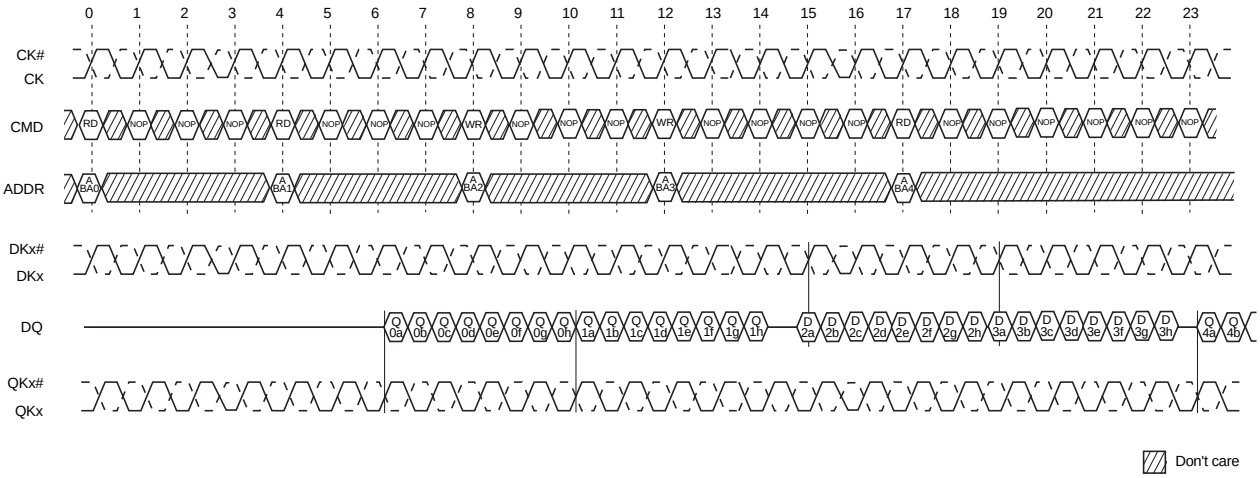


Figure 2–22. Timing Chart (CIO Products, Multiplexed Address Mode, BL = 2, Configuration = 1)

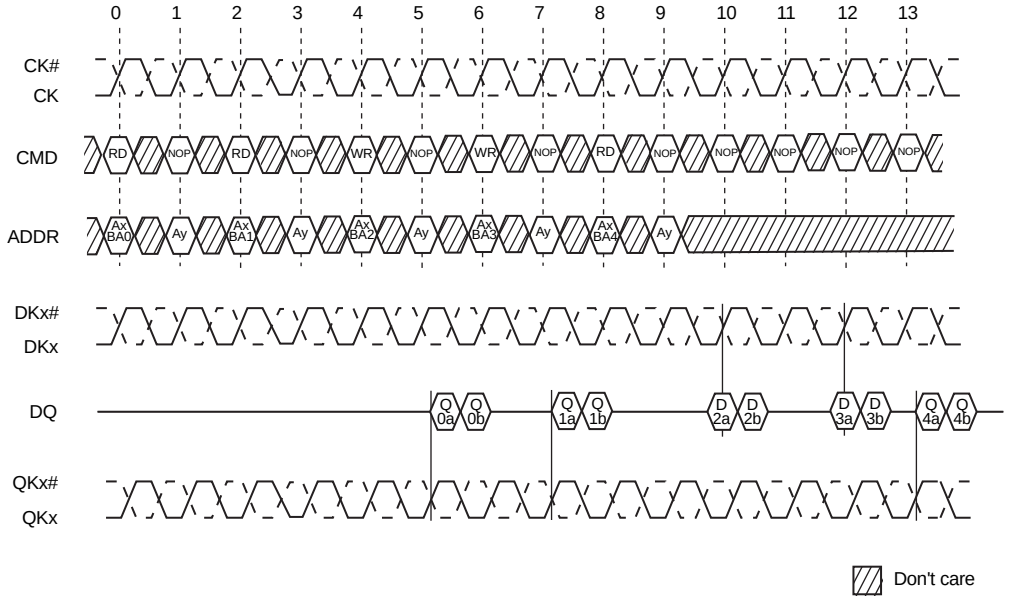


Figure 2–23. Timing Chart (CIO Products, Multiplexed Address Mode, BL = 4, Configuration = 1)

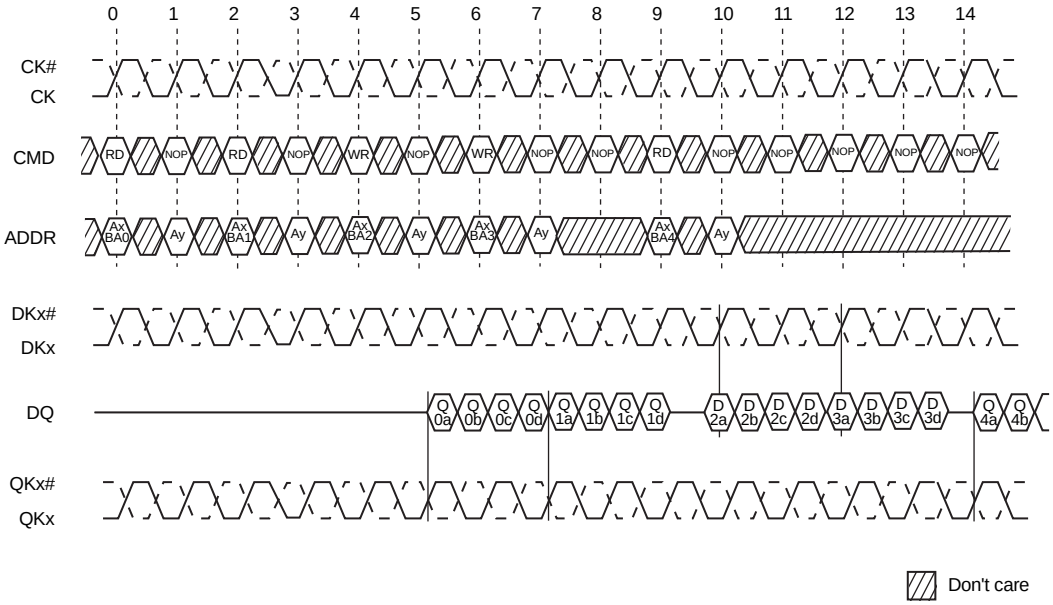


Figure 2–24. Timing Chart (CIO Products, Multiplexed Address Mode, BL = 8, Configuration = 2)

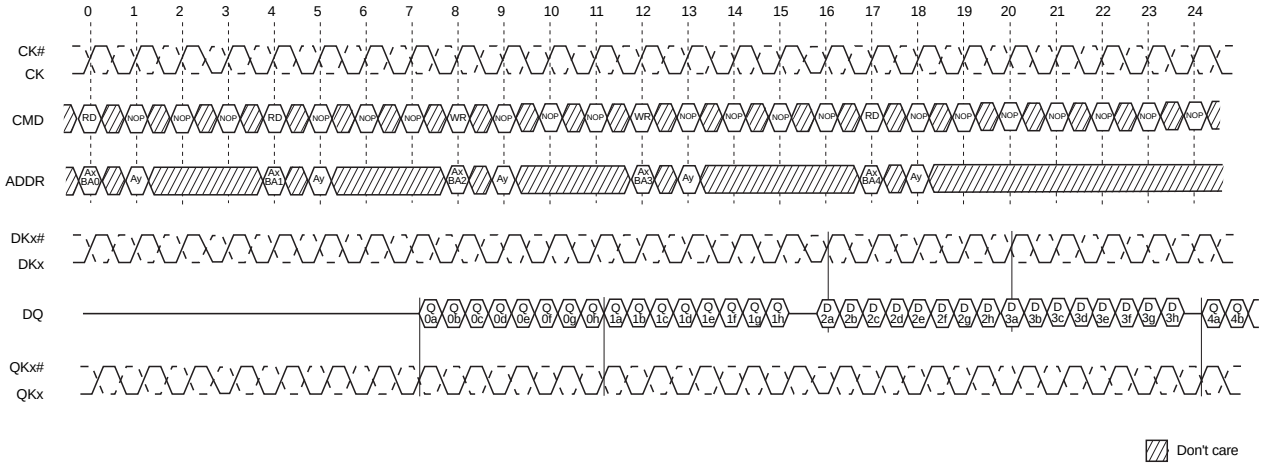


Figure 2–25. Timing Chart (SIO Products, Non-Multiplexed Address Mode, BL = 2, Configuration = 1)

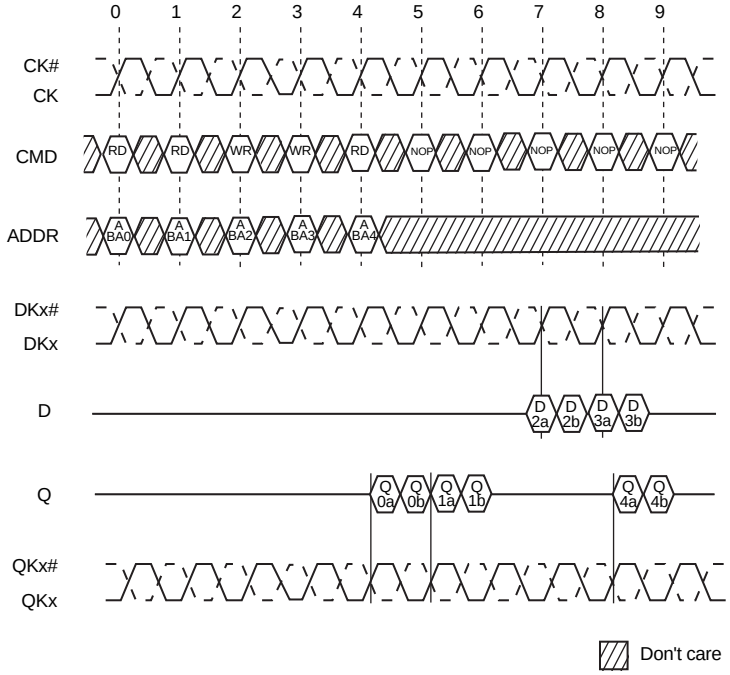


Figure 2–26. Timing Chart (SIO Products, Non-Multiplexed Address Mode, BL = 4, Configuration = 1)

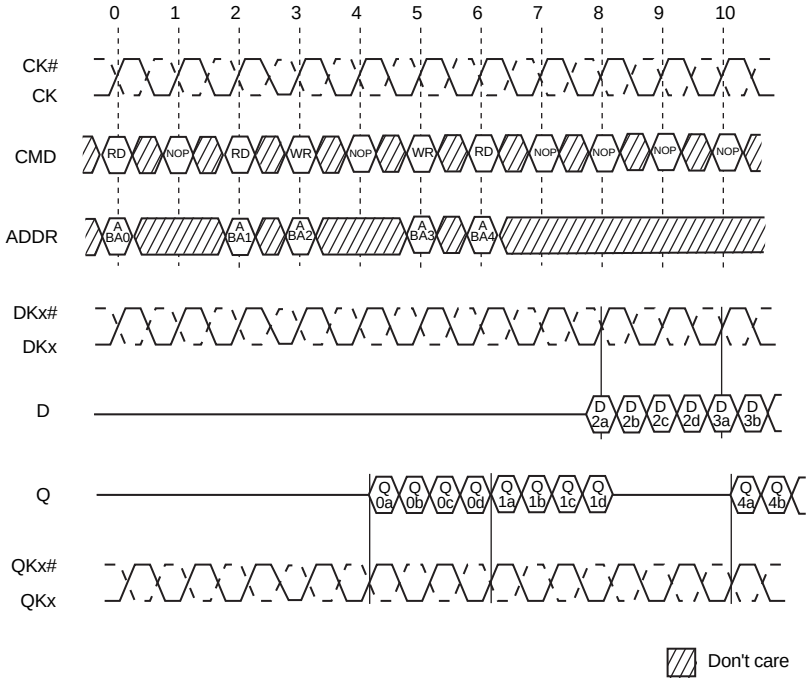


Figure 2–27. Timing Chart (SIO Products, Non-Multiplexed Address Mode, BL = 8, Configuration = 2)

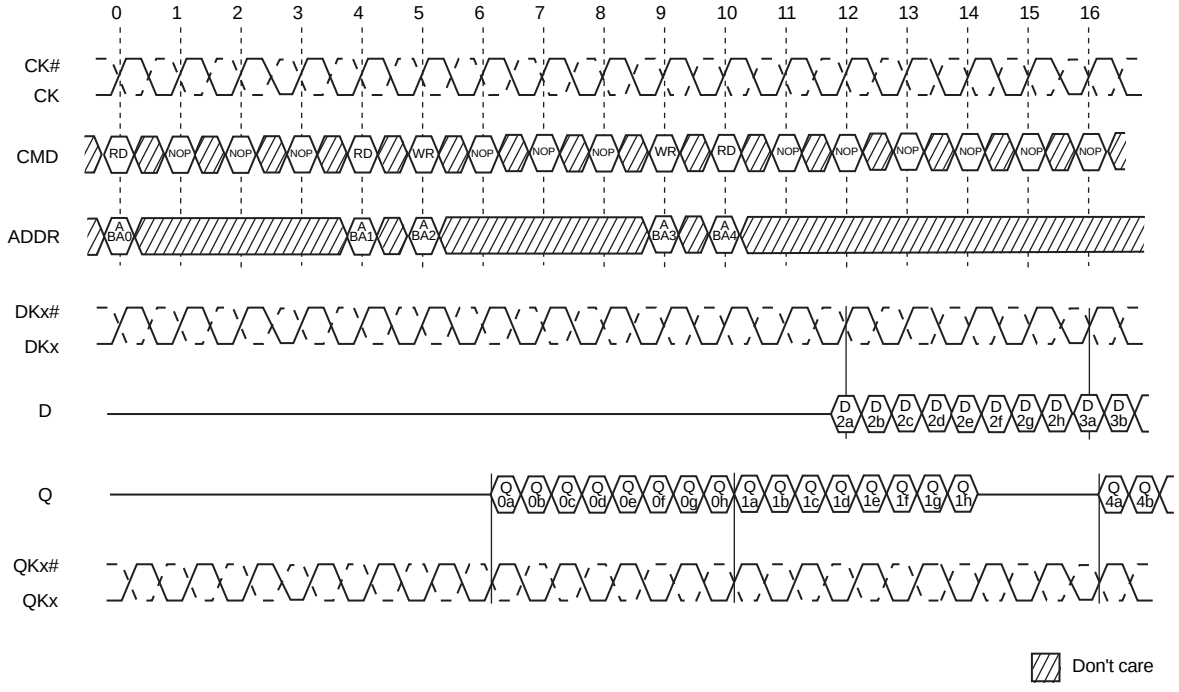


Figure 2–28. Timing Chart (SIO Products, Multiplexed Address Mode, BL = 2, Configuration = 1)

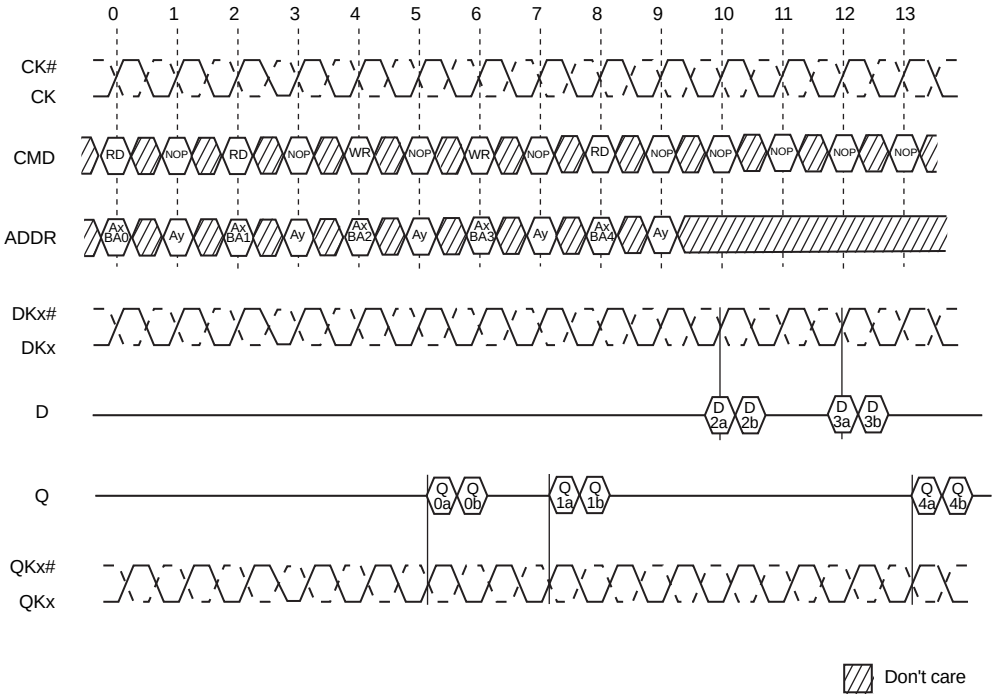


Figure 2–29. Timing Chart (SIO Products, Multiplexed Address Mode, BL = 4, Configuration = 1)

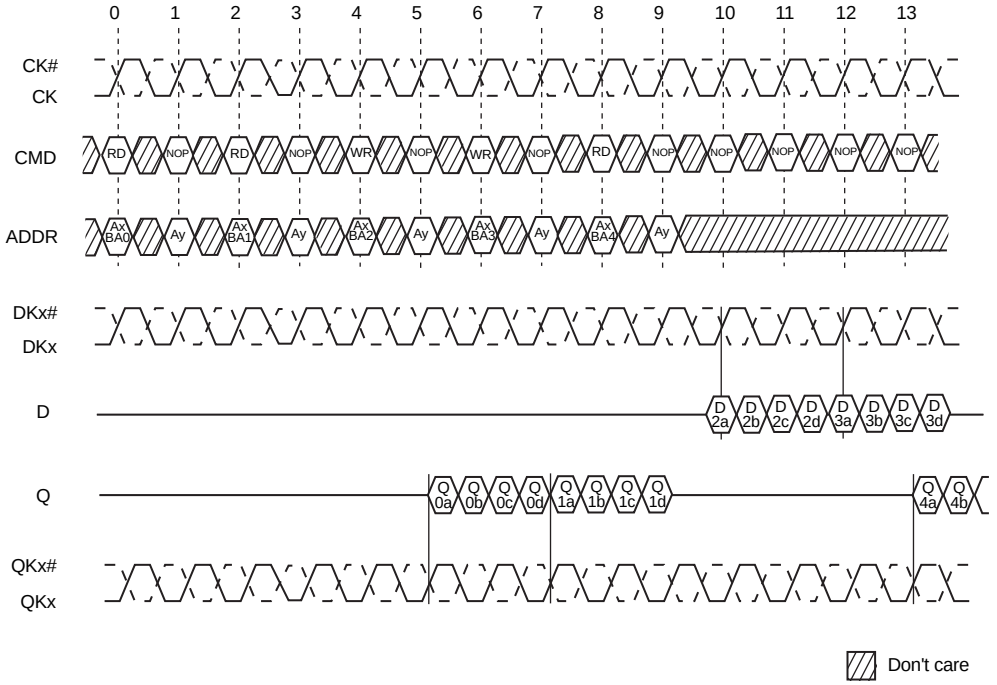


Figure 2–30. Timing Chart (SIO Products, Multiplexed Address Mode, BL = 8, Configuration = 2)

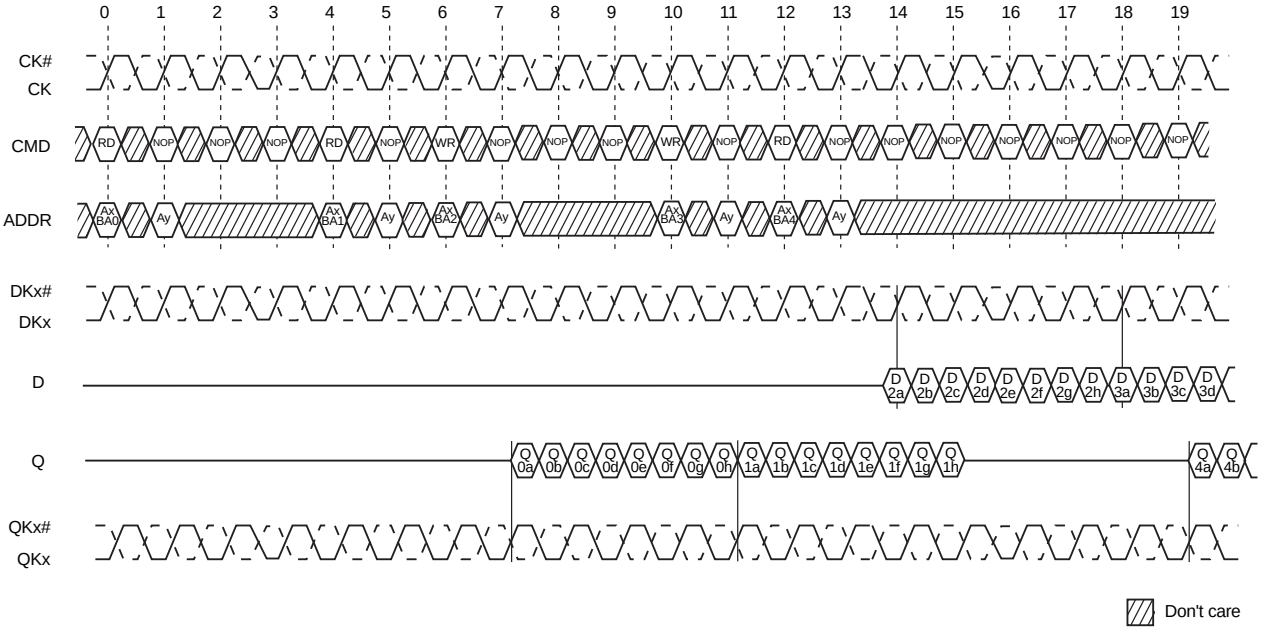


Figure 2–31. READ/WRITE Interleave Operation Timing Chart (SIO Products, Non-Multiplexed Address Mode, BL = 4, Configuration = 1)

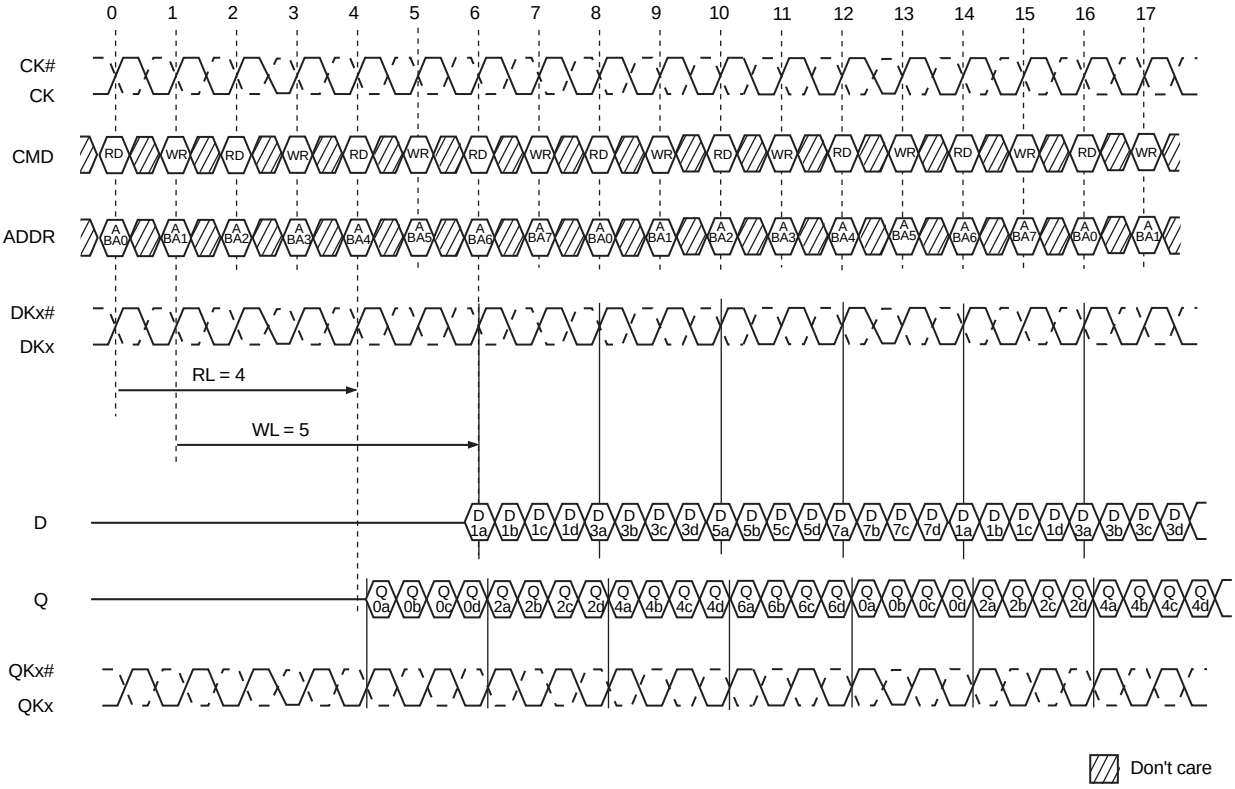
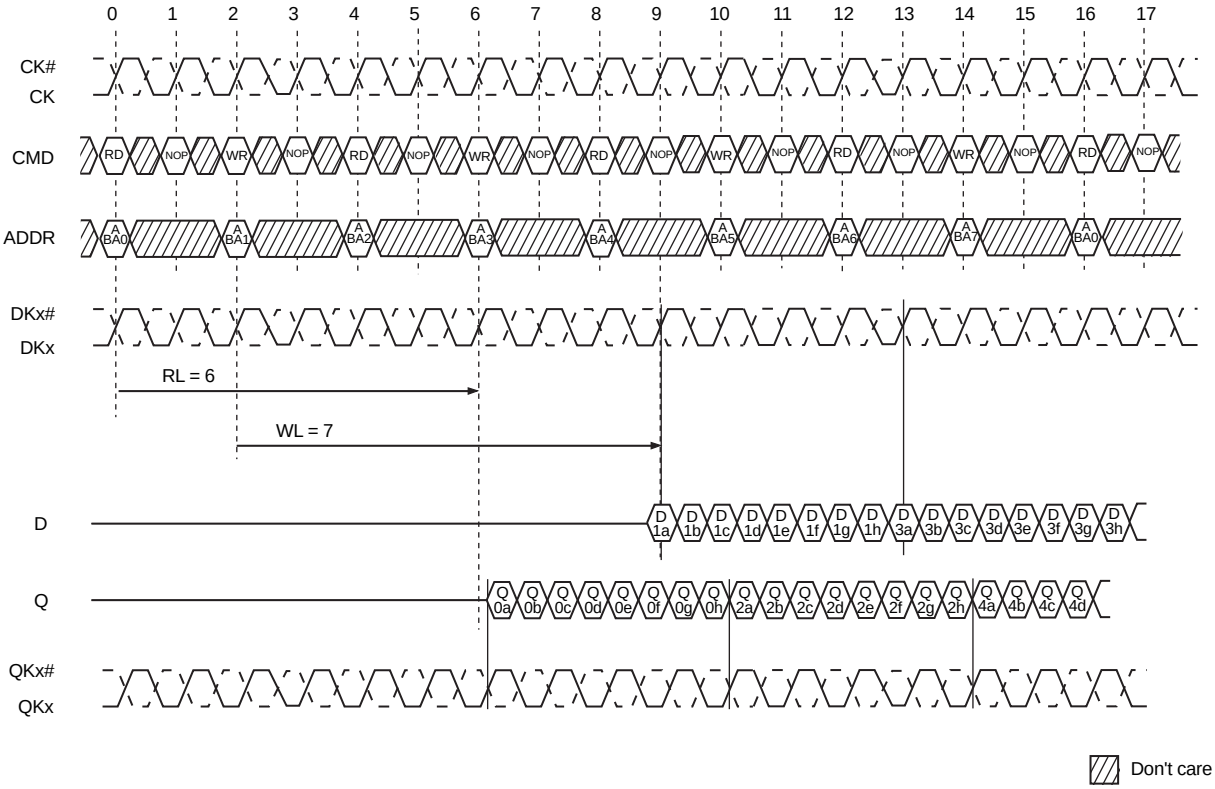


Figure 2–32. READ/WRITE Interleave Operation Timing Chart (SIO Products, Non-Multiplexed Address Mode, BL = 8, Configuration = 2)



2.5 AREF

Banks can be separately refreshed by inputting an automatic refresh command simultaneously with a bank address at the rise timing of CK. Input to address pins will not have any effect.

See **CHAPTER 3 REFRESH OPERATIONS** for details.

Figure 2–33. Automatic Refresh Command

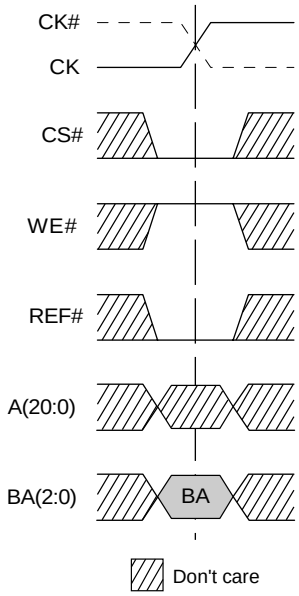
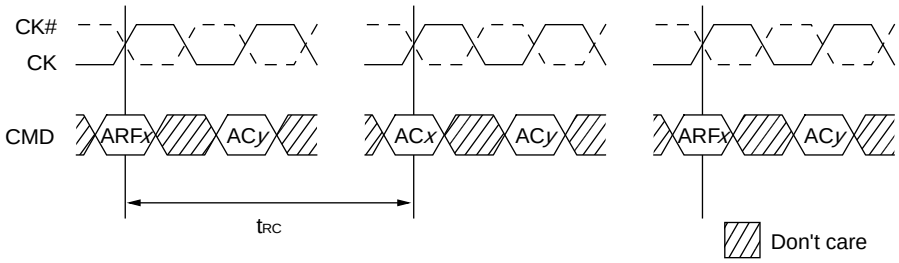


Figure 2–34. Automatic Refresh Cycle



CHAPTER 3 REFRESH OPERATIONS

Low latency DRAM requires refresh operations. Refresh operations must be performed for all memory cells within a refresh time of 32 ms.

3.1 Refresh Operations

The AREF command is used to refresh memory cell contents. Input the bank address that specifies the bank to be refreshed, together with the AREF command. The addresses to be refreshed are not required to be input, because they will be efficiently and automatically generated by an internal refresh controller provided with the device. To input a command to the same bank, the t_{RC} (MIN.) specifications must be satisfied. Distributed refresh and burst refresh operations are available as refresh methods.

3.1.1 Distributed refresh operation

A distributed refresh operation is a method by which the refresh command is input in multiple batches within the low latency DRAM refresh time of 32 ms.

(1) Distributed bank/word refresh operation

A distributed bank/word refresh operation is a method by which all banks and words are refreshed at equal timings within a refresh time of 32 ms. The average refresh interval time is 0.488 μs for a 288 Mb low latency DRAM.

Average refresh interval time = Refresh time/Number of words per bank/Number of banks
= 32 ms / 8,192 words / 8 banks = 0.488 μs

Figure 3–1. Image of Distributed Bank/Word Refresh Timing

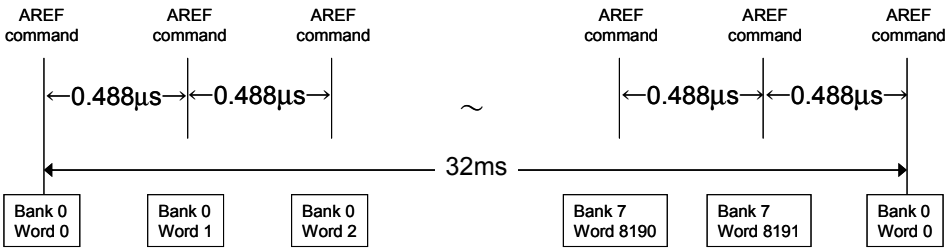
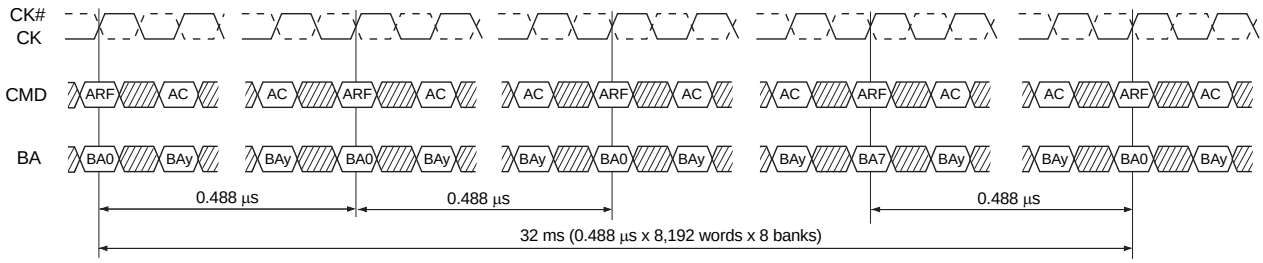


Figure 3–2. Distributed Bank/Word Refresh Timing Chart



(2) Distributed word refresh operation

A distributed word refresh operation is a method by which a refresh operation is performed by issuing successive AREF commands for eight banks in a batch. Consequently, a data write/read period that is successive and longer than that of a distributed bank/work refresh operation can be secured without interruption by refresh operations.

The refresh interval time is 3.90 μs for a 288 Mb low latency DRAM.

Refresh interval time = Refresh time/Number of words per bank
= 32 ms /8,192 words = 3.90 μs

Figure 3–3. Image of Distributed Word Refresh Timings

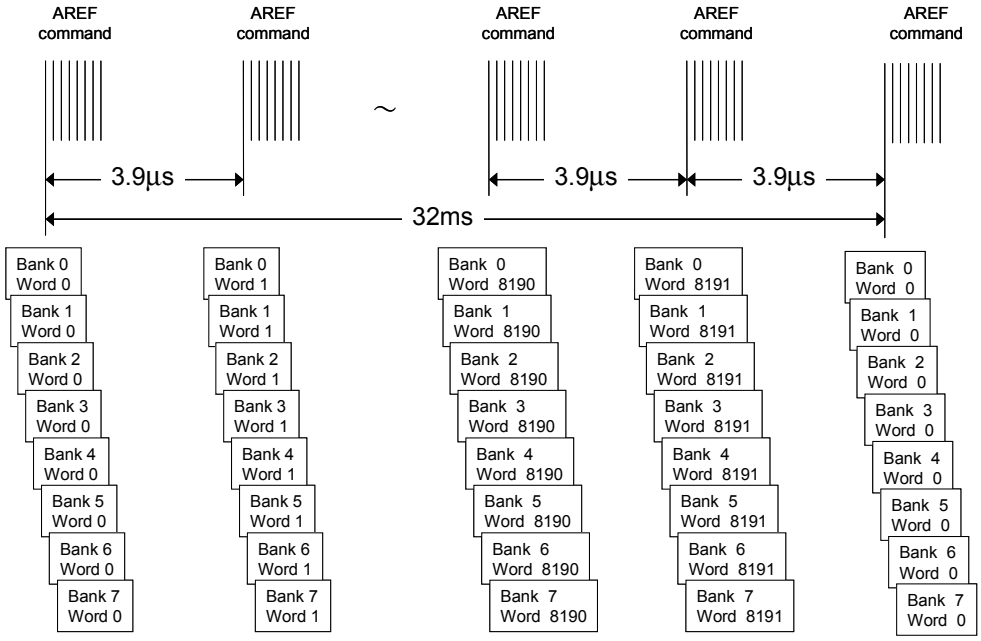
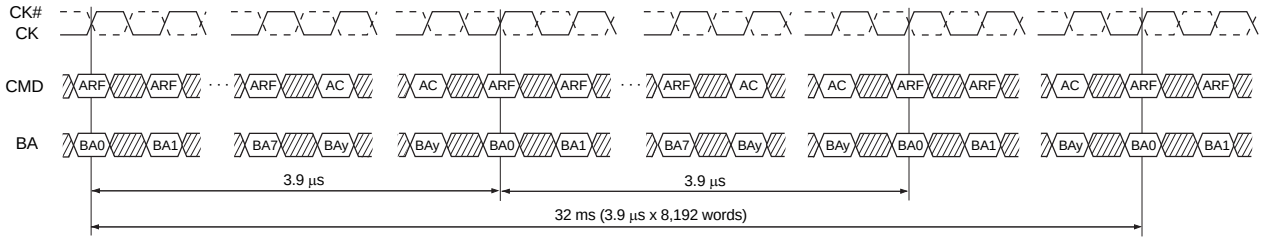


Figure 3–4. Distributed Word Refresh Timing Chart



3.1.2 Burst refresh operation

A burst refresh operation is a method by which refresh commands are input intensively within the low latency DRAM refresh time of 32 ms.

(1) Burst refresh operation

A burst refresh operation is a method by which all banks and words are refreshed in a batch within a refresh time of 32 ms. Consequently, the period that equals the time required for the refresh operation subtracted from the refresh time of 32 ms can be secured as a data write/read period without interruption by refresh operations.

The burst refresh time is 0.164 ms, and the period during which data writing/reading without interruption by refresh operations can be performed is 31.836 ms for a 288 Mb low latency DRAM (400 MHz).

Burst refresh time = Number of words per bank × Number of banks × Cycle time
= 8,192 words × 8 banks × 2.5 ns = 0.164 ms

Period during which data writing/reading without interruption by refresh operations can be performed
= Refresh time − Burst refresh time
= 32 ms − 0.164 ms = 31.836 ms

Figure 3–5. Image of Burst Refresh Timing (400 MHz Operation)

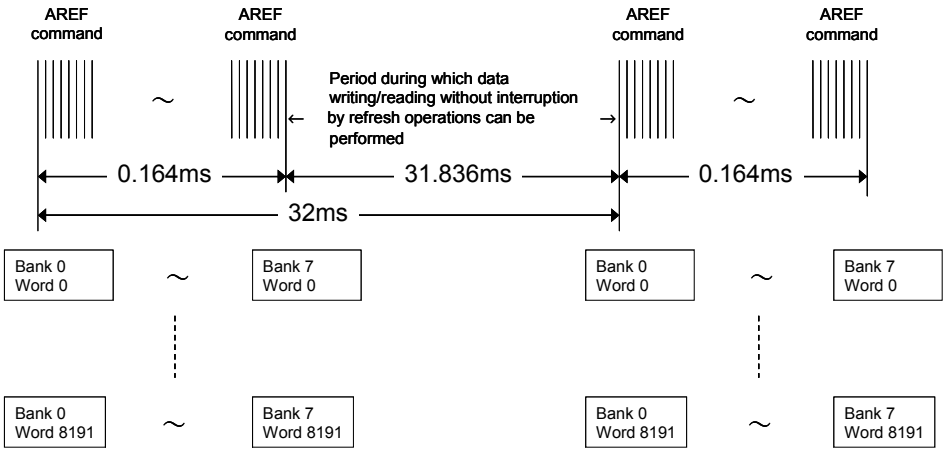
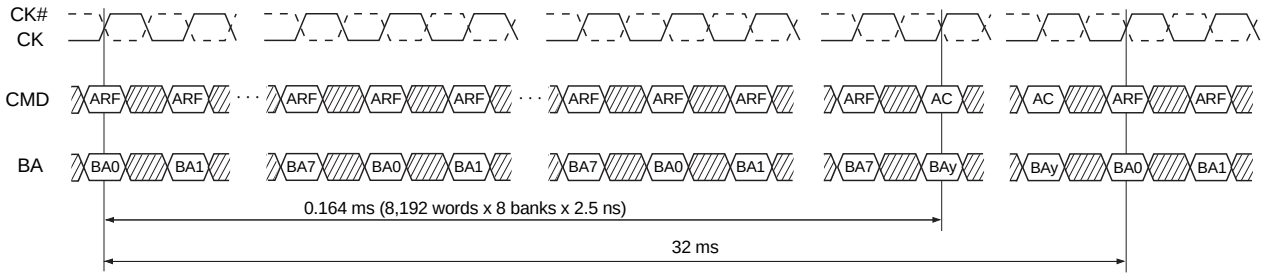


Figure 3–6. Burst Refresh Timing Chart (400 MHz Operation)



CHAPTER 4 POWER APPLICATION

The internal state of a low latency DRAM is undefined immediately after the power is applied. To start normal operation, the specified power application procedure and initialization procedure must be followed. The procedures differ for non-multiplexed address mode and multiplexed address mode and are therefore separately described below. Operate the device according to the given procedures in order to prevent unexpected operations and permanent damage.

4.1 Non-Multiplexed Address Mode

Apply power according to (1) to (5) below.

(1) Apply V_{EXT}, V_{DD}, $V_{DD}Q$, V_{REF}, and V_{TT}, and start clock operation after all voltages have stabilized.
Apply V_{DD} and V_{EXT} at the same time as $V_{DD}Q$ or before $V_{DD}Q$.
Apply $V_{DD}Q$ at the same time as V_{REF} and V_{TT}, or before V_{REF} and V_{TT}.
There are no restrictions related to the application order or the time until the normal operation level is reached between applying V_{DD} and V_{EXT}, but the following device power application procedure must be continued after both levels have reached normal operation levels **Note 1**.
VID (DC) must be satisfied until clock operations of CK and CK# start.
Meanwhile, continuously execute NOP commands and maintain a NOP state.

(2) Maintain a stable state **Note 2** for at least 200 μs.

(3) Successively input MRS commands for at least three cycles.
These cycles consist of at least two cycles of dummy MRS commands and one cycle of a valid MRS command. It is recommended to make the mode register codes when inputting dummy MRS commands the same values as those of the mode register codes when a valid MRS command is input.

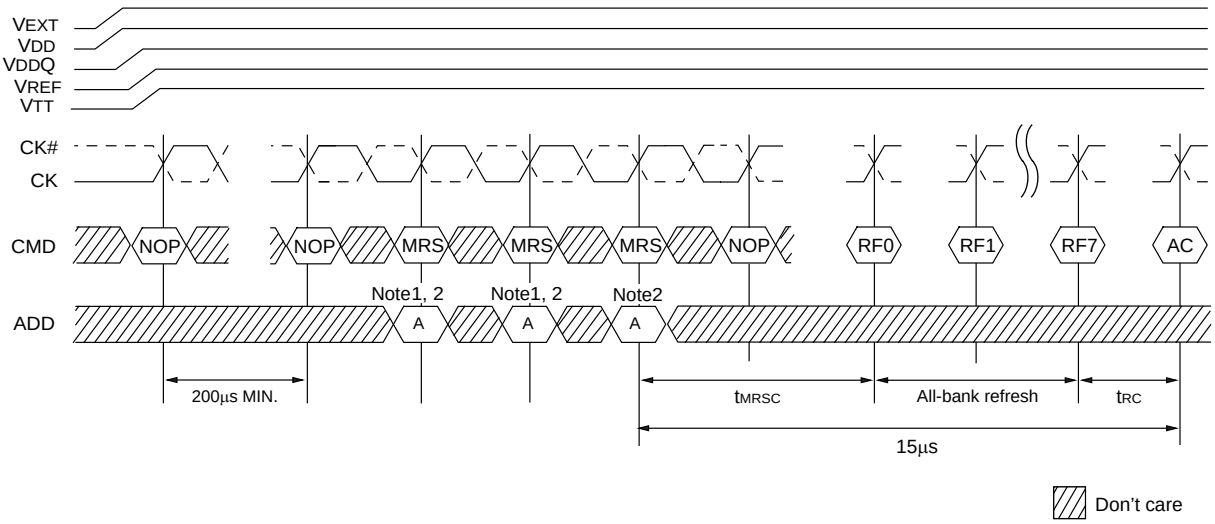
(4) Input refresh commands to all eight banks after t_{MRSC} after having set the MRS to be used. Furthermore, clock input will be required during the 15 μs specified by PLL circuit lock time t_{CK} Lock (MIN.) until normal operation starts.

(5) Normal operation can be performed after t_{RC} has elapsed from the last AREF command.

Notes 1. There are no restrictions regarding the design targets of the power application procedure and initialization procedure, but be sure to follow the above-mentioned procedure.

2. A stable level is a level whose voltage fluctuation is less than ±0.1 V DC/50 ns.

Figure 4–1. Power Application Sequence in Non-Multiplexed Address Mode



Notes 1. Set all address pins to LOW while inputting dummy MRS commands.

2. Set A10 to A17 to LOW.

Remark MRS: MRS command
RFx: Refresh command (bank x)
AC: Any command

4.2 Multiplexed Address Mode

Apply power according to (1) to (5) below.

(1) Apply V_{EXT}, V_{DD}, $V_{DD}Q$, V_{REF}, and V_{TT}, and start clock operation after all voltages have stabilized.
Apply V_{DD} and V_{EXT} at the same time as $V_{DD}Q$ or before $V_{DD}Q$.
Apply $V_{DD}Q$ at the same time as V_{REF} and V_{TT}, or before V_{REF} and V_{TT}.
There are no restrictions related to the application order or the time until the normal operation level is reached between applying V_{DD} and V_{EXT}, but the following device power application procedure must be continued after both levels have reached normal operation levels **Note 1**.
V_{ID} (DC) must be satisfied until clock operations of CK and CK# start.
Meanwhile, continuously execute NOP commands and maintain a NOP state.

(2) Maintain a stable state **Note 2** for at least 200 μs.

(3) Successively input MRS commands for at least three cycles.
These cycles consist of at least two cycles of dummy MRS commands and one cycle of a valid MRS command to set multiple-address mode. At this time, input HIGH to the address pin A5. It is recommended to make the mode register codes when inputting dummy MRS commands the same values as those of the mode register codes when a valid MRS command is input.

(4) Start inputting the mode register codes together with MRS commands which are valid in multiple-address mode after t_{MRSC} has elapsed from the previous valid MRS command.

(5) Start inputting eight AREF commands, each of which correspond to a bank, after t_{MRSC} has elapsed from the last valid MRS command. Leave an interval of 2,048 cycles between all AREF commands **Note 3**. There are no particular restrictions regarding the order of banks when the commands are input.

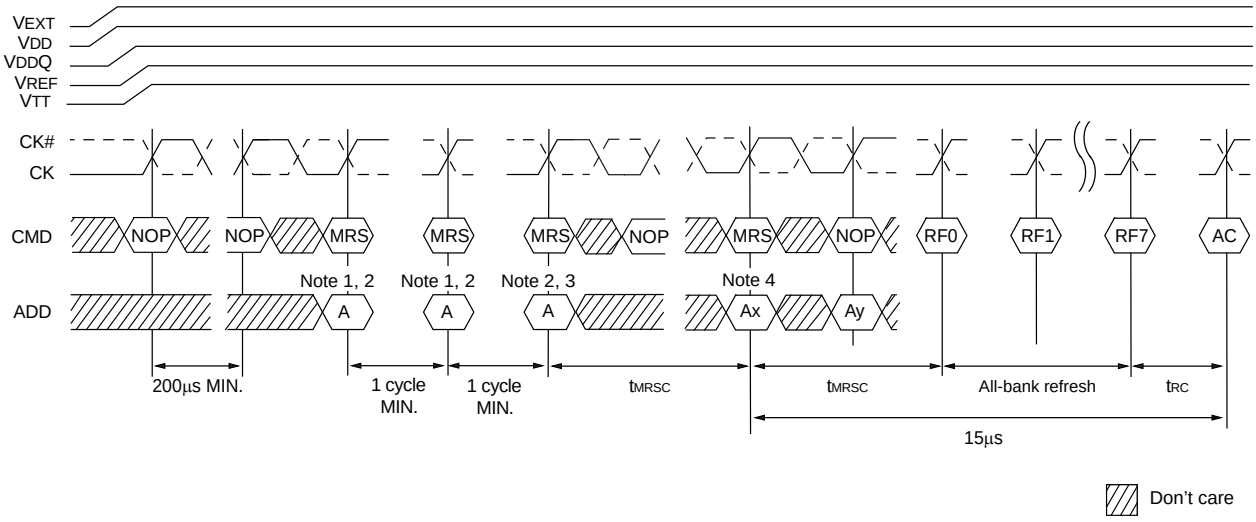
(6) Normal operation can be performed after t_{RC} has elapsed from the last AREF command.

Notes 1. There are no restrictions regarding the design targets of the power application procedure and initialization procedure, but be sure to follow the above-mentioned procedure.

2. A stable level is a level whose voltage fluctuation is less than ±0.1 V DC/50 ns.

3. AREF commands must be input to eight banks. There is no problem as long as a time of at least 15 μs, which is specified by t_{CK} Lock (MIN.), is secured until input of AREF commands to all banks is completed. The PLL circuit will be locked during this period.

Figure 4–2. Power Application Sequence in Multiplexed Address Mode



Notes 1. Set all address pins to LOW while inputting dummy MRS commands.

2. Set A10 to A17 to LOW.

3. Set address pin A5 to HIGH (multiple-address mode is set in non-multiplexed address mode).

4. Set address pin A5 to HIGH (multiple-address mode is set in multiplexed address mode).

Remark MRS: MRS command

RFx: Refresh command (bank x)

AC: Any command

CHAPTER 5 PLL CIRCUIT

5.1 Mounting PLL Circuit

NEC Electronics' low latency DRAM is mounted with a PLL circuit. The PLL circuit can be used to generate clock signals for internal device control, which are used to improve the output timing accuracy of data outputs Q and DQ, and output data clocks QK and QK#. By mounting a PLL circuit, however, the minimum operation frequency will be restricted to t_{CK} (MAX.).

The PLL circuit is enabled or disabled by using the mode register codes that set the PLL function when inputting MRS commands.

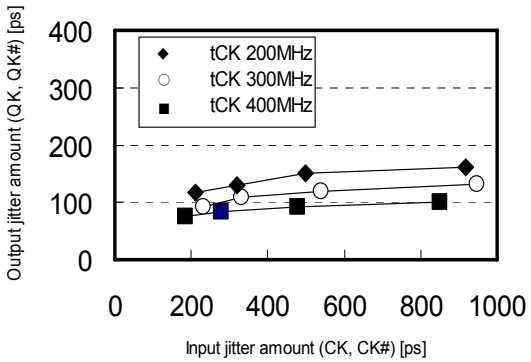
Table 5–1. Mode Register Codes

PLL Function	Address Multiplex Function	
	Non-Multiplexed Address Mode	Multiplexed Address Mode
PLL circuit disabled (default)	A7 = 0	A9y = 0
PLL circuit enabled	A7 = 1	A9y = 1

5.1.1 Advantages of PLL circuit

A PLL circuit can suppress the effect of input jitter and can minimize output jitter. Consequently, valid data windows for output data can be expanded in products that use a PLL circuit. Figure 5-1 shows the dependence of the output jitter amount against the input jitter amount of a product using a PLL circuit. The output jitter amount of the product using a PLL circuit hardly depends on the input jitter amount and is constant. A PLL circuit is therefore used for low latency DRAM.

Figure 5–1. Dependence of Output Jitter Amount on Input Jitter Amount for PLL Circuit



5.1.2 Disabling PLL circuit

When performing a system operation check at a low speed, the PLL circuit can be disabled and the system can be operated at a clock frequency slower than that restricted by t_{CK} (MAX.), by setting the mode register codes during MRS command input. At this time, the READ latency t_{RL} is the same as the value set in **2.3.2 Configuration setting**, but the AC/DC characteristics will not be guaranteed.

During normal operation, enable the PLL circuit for use.

Table 5–2. Minimum Operation Frequency

PLL Function	t_{CK} (MAX.)	Frequency
PLL circuit disabled (default)	488 ns	2.05 MHz
PLL circuit enabled	5.7 ns	175 MHz

5.1.3 Clock stop

Power consumption can be suppressed by stopping operation of input clock CK/CK#. At this time, the clock operations of output data clocks QK and QK# will be similarly stopped and a level of QK/QK# = HIGH/LOW or QK/QK# = LOW/HIGH will be continuously output.

When returning from a clock stop, input stable input clock CK/CK# for the period specified by PLL circuit lock time t_{CK} Lock (MIN.) before starting a normal operation. Data that was written before the clock was stopped will not be retained.

5.1.4 Operation frequency change

The operation frequency of a low latency DRAM can be changed without re-setting the mode register codes by using MRS commands. After the operation frequency has been changed, however, input stable input clock CK/CK# for the period specified by PLL circuit lock time t_{CK} Lock (MIN.) before starting a normal operation. Note that data that was written before the operation frequency was changed will not be retained.

CHAPTER 6 OUTPUT IMPEDANCE MATCHING

Low latency DRAM is mounted with a programmable impedance output buffer which is provided with a function to adjust the output impedance. Consequently, the output pin impedance and transmission line impedance can be matched. The distortion of output signal waveforms can be suppressed through this matching of impedances.

6.1 Output Impedance Adjustment

With this function, the following two settings can be selected.

(1) Referencing the resistance preset in the device and setting the impedance to that value

(2) Referencing the value of resistor RQ to be externally connected to the ZQ pin and setting the impedance to RQ/5 Ω

The resistance setting is selected by using the mode registers codes that define impedance matching.

Table 6–1. Mode Register Codes

Output Impedance Mode Function	Address Multiplex Function	
	Non-Multiplexed Address Mode	Multiplexed Address Mode
Sets impedance to device-internal 50 Ω (default)	A8 = 0	A8x = 0
Sets impedance to value of externally connected resistor RQ/5 Ω	A8 = 1	A8x = 1

(1) The output impedance to be set to the referenced resistance preset in the device is the preset resistance of 50 Ω.

(2) Referencing the value of resistor RQ to be externally connected to the ZQ pin of external device and setting the impedance to RQ/5 Ω

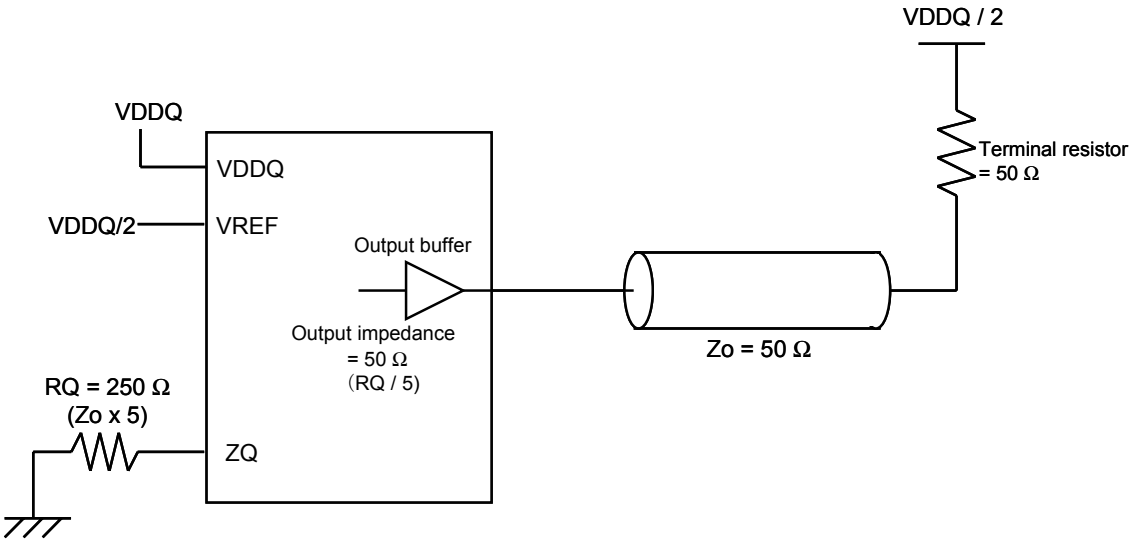
The output impedance can be adjusted by altering the value of the resistor connected between the ZQ pin and V_{SS}. Connect RQ, whose resistance is five times the output impedance value to be set, between the ZQ pin and V_{SS}. For example, when the impedance (Z_O) of the transmission line is 50 Ω, the output impedance of the low latency DRAM is set to 50 Ω by setting the value of the resistor RQ to be connected to the ZQ pin to 250 Ω. At this time, the output impedance can be set within a range of 25 to 60 Ω.

Remarks1. In the case of the mode register code setting of (2), the minimum impedance can be set by connecting the ZQ pin to V_{SS}, and the maximum impedance can be set by connecting the ZQ pin to $V_{DD}Q$.

2. To change the output impedance that has been set, turn off the power and turn on the power again after having changed the value of the resistor to be connected to the ZQ pin.

3. With this device, the output impedance is appropriately corrected according to voltage and temperature fluctuations. This correction is automatically performed and cannot be externally detected, but it does not affect the operation of the device. All AC/DC characteristics are satisfied.

Figure 6–1. Output Impedance Setting Example



CHAPTER 7 TERMINAL RESISTORS

7.1 Effects of Terminal Resistor

Terminating the signal line has an effect of distorting signal waveforms being suppressed. The reflection of waves to the signal waveforms to be input to the controller can be suppressed by terminating the far end of the signal line that is connected to the output pin of the low latency DRAM. The quality of signal waves can be improved by using the programmable impedance output buffer to adjust the output impedance, as described in **CHAPTER 6 OUTPUT IMPEDANCE MATCHING**, and using this terminal resistor in combination.

Caution The AC characteristics of a low latency DRAM are specified under the condition that the synchronous data output pin (Q or DQ), data valid pin (QVLD), and the output data clocks (QK and QK#) are terminated.

Figure 7-1 shows an image of signal wave transmission when the transmission line has been terminated. The reflected waves of signal waves can be suppressed by terminating the transmission line that connects the low latency DRAM and the memory controller.

Figure 7–1. Image of Signal Wave Transmission When Transmission Line Has Been Terminated

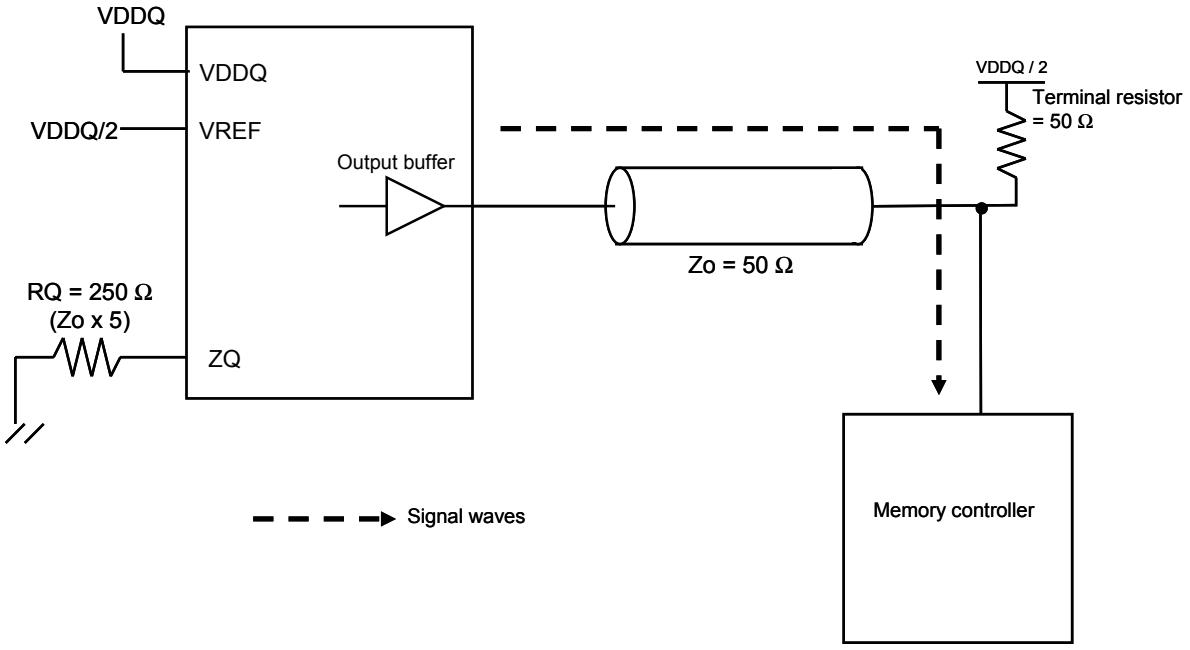
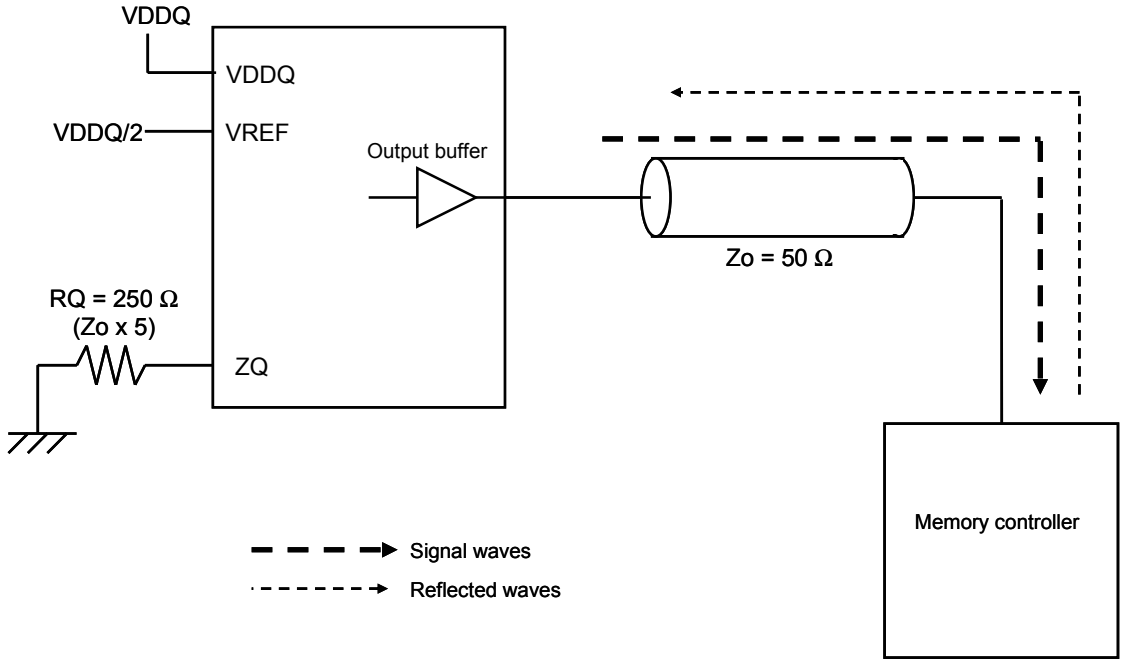


Figure 7-2 shows an image of signal wave transmission when the transmission line has not been terminated. The reflected waves of signal waves cannot be suppressed and the quality of signal waves may deteriorate, because the transmission line is not terminated.

Figure 7–2. Image of Signal Wave Transmission When Transmission Line Has Not Been Terminated



CHAPTER 8 ON DIE TERMINATION (ODT)

Low latency DRAM is provided with an ODT function. Distortion of signal waveforms can be suppressed and degradation of the quality of signal waveforms can be prevented by using the ODT function and terminating the signal line. Furthermore, costs can be reduced, because the number of components of the terminal resistor, which was formerly externally mounted on the system board, can be reduced.

8.1 ODT Function Setting

Data I/O pin DQ, data input pin D, data output pin Q, and data mask input pin DM are provided with an ODT function. The ODT function is set to be enabled or disabled by using the mode register codes which define the ODT function.

Table 8–1. Mode Register Codes

ODT Function	Address Multiplex Function	
	Non-Multiplexed Address Mode	Multiplexed Address Mode
Disabled (default)	A9 = 0	A9x = 0
Enabled	A9 = 1	A9x = 1

8.2 ODT-On Timing of Each Pin

The ODT-on timing differs depending on the I/O setup and pins when the ODT function is enabled.

Table 8–2. Mode Register Codes

I/O Setup	Pin	ODT-On Timing
CIO products	DM	Always
	DQ	Except when reading data
SIO products	D, DM	Always
	Q	Except when reading data

Remark The ODT function is disabled and ODT-off is always set for the DNU pins (DQ, D, and Q pins not used with x9 and x18 products), even if the ODT function is set to be enabled.

Figures 8-1 and 8-2 show the timing charts of CIO products and SIO products, respectively.

Figure 8–1. CIO Product Timing Chart When ODT Is Used (Non-Multiplexed Address Mode, BL = 2, Configuration 1)

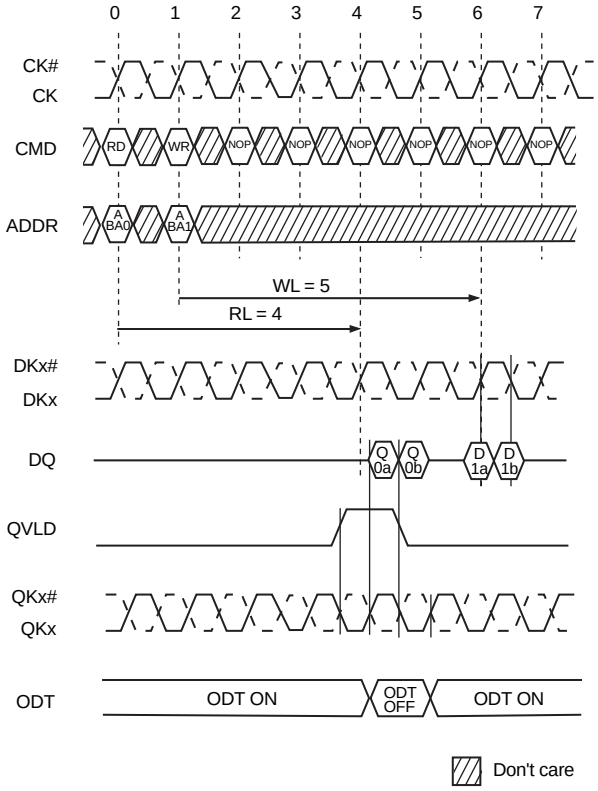
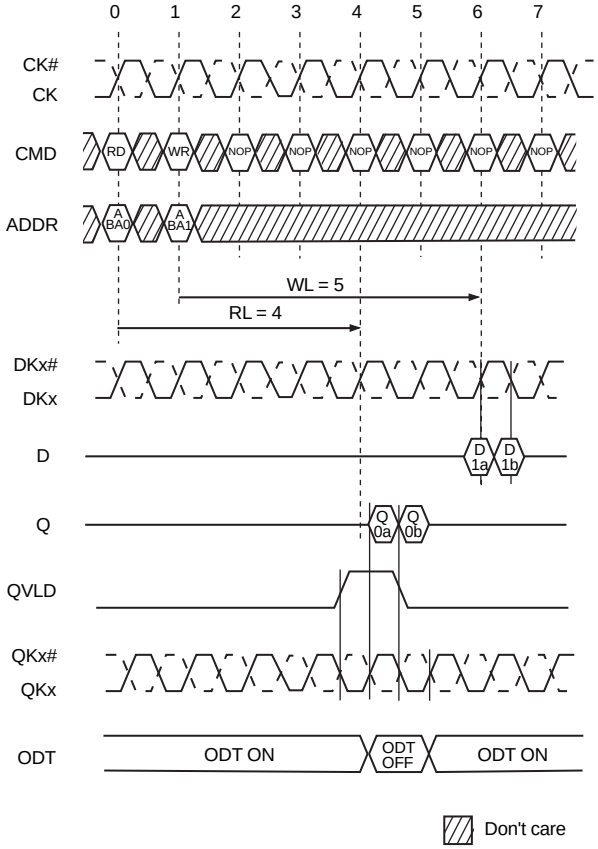


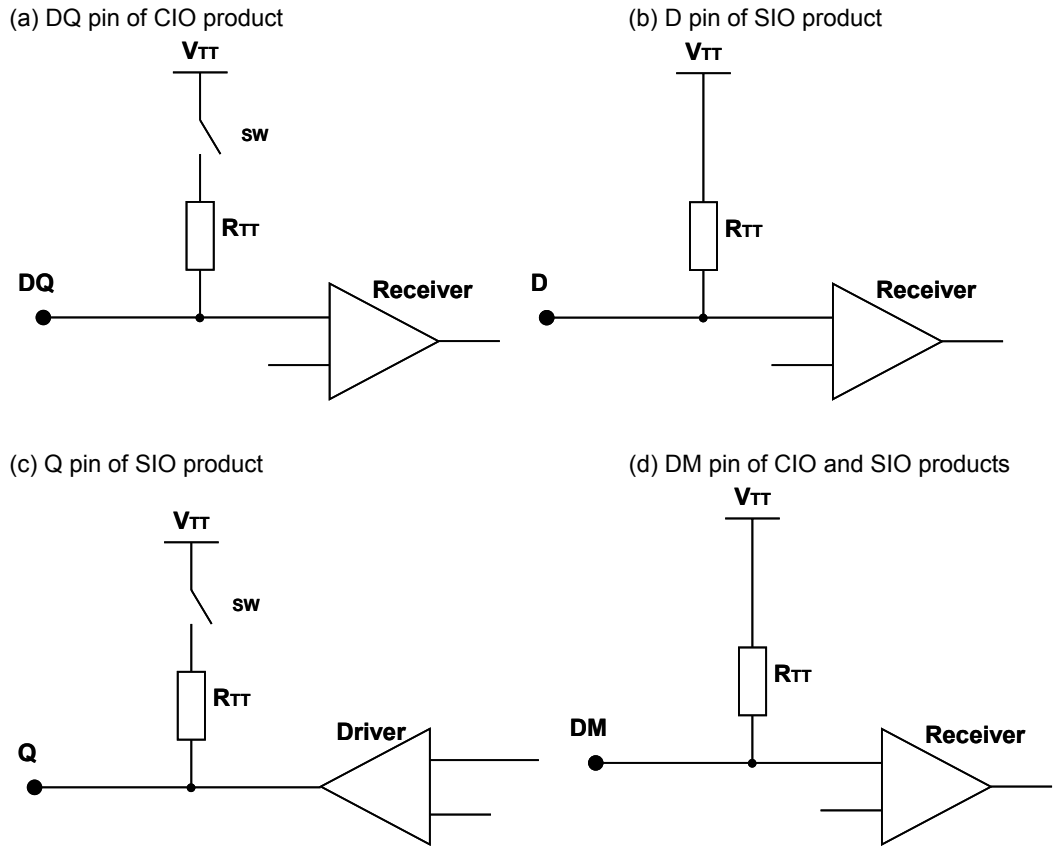
Figure 8–2. SIO Product Timing Chart When ODT Is Used (Non-Multiplexed Address Mode, BL = 2, Configuration 1)



8.3 ODT Structure

When ODT is on, the DQ, D, Q, and DM pins are terminated at V_{TT} via resistor R_{TT} within the device. Figure 8-3 shows the equivalent circuits of ODT.

Figure 8–3. Equivalent Circuits of ODT



8.4 ODT DC Parameters

Set the voltage of V_{TT} to V_{REF}. R_{TT} is set to 135 to 165 Ω at T_C = 95°C.

Table 8–3. ODT DC Specifications

ODT Function	Symbol	MIN.	MAX.	Unit
Terminal voltage	V_{TT}	0.95 x V_{REF}	1.05 x V_{REF}	V
Terminal resistance	R_{TT}	135	165	Ω

[MEMO]

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