ForgeFPGA Socket Adapter #1

User Manual

ForgeFPGA™

Socket Adapter #1

Contents

Figures

The "ForgeFPGA™ Socket Adapter #1" implements a connection between the pins of an ForgeFPGA and Development Board. This board can be used for design prototyping with diferent boot modes. Socket Adapter supports PMOD standards which gives ability to connect different PMOD adapters.

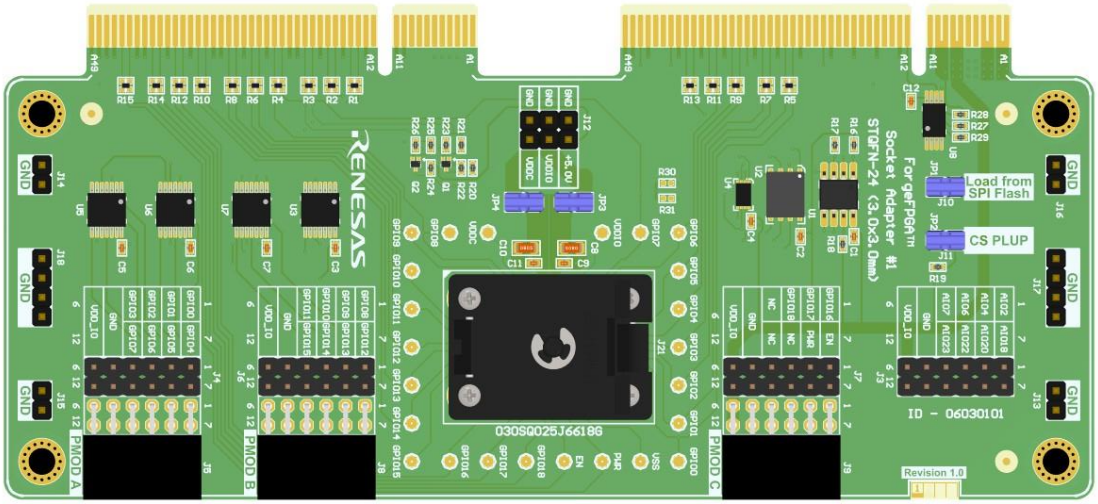


Figure 1. ForgeFPGA Socket Adapter #1

Features

Working Stand-alone or in pair with ForgeFPGA Advanced Development Board, Socket Adapter can be configured to work with different FPGA designs by providing a list of useful features:

- Programming and Emulation
- Stand-alone Boot Options
- Onboard 4 Mbit SPI flash
- PMOD Connectors
- Stand-alone Power Connectors

1. Functional Description

The figure below shows the board view and identifies the main components. This board can be used together with ForgeFPGA™ Advanced Development Board using Dual Interaction Connector to transmit and process signals. Also, the board can be used as an independent unit. The chip can be powered by Development Board or through the EXT PWR connector. The signals on GPIO are accessible through the 12-pin GPIO connectors or PMOD connectors.

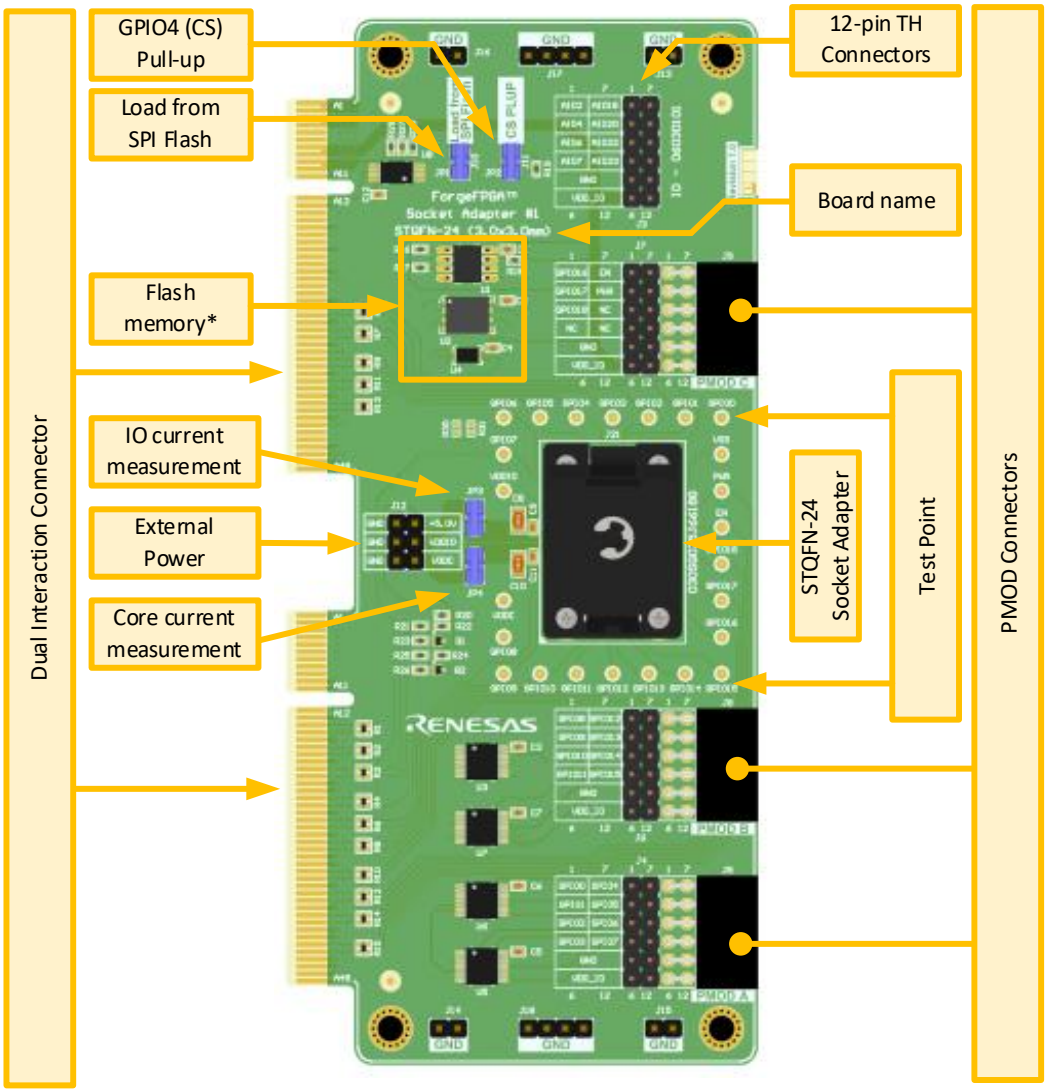
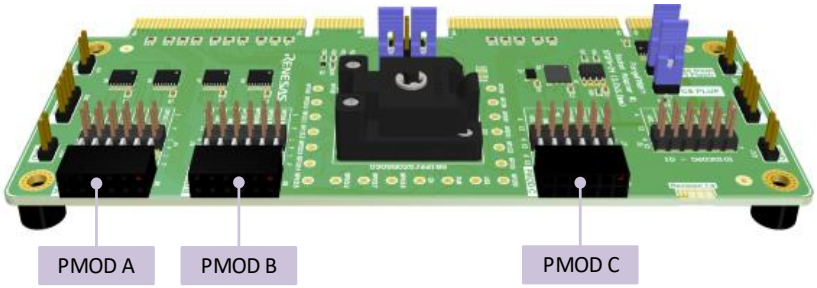


Figure 2. ForgeFPGA Socket Adapter #1 Components

*Only one flash memory chip can be installed on board.

1.1 GPIO and PMOD Connectors

Access to socket pins is provided by GPIO and PMOD connectors. Both GPIO and PMOD connectors have the same pinout. Note that programming signals from interaction connector to GPIO/PMOD are gated while programming and emulation have entry sequences.



6	5	4	3	2	1
12	11	10	9	8	7

Figure 3. PMOD Connector Position

Table 1. PMOD and External connectors pinout

GPIO/PMOD A	
PMOD Pin #	**GPIO #**
1	GPIO0
2	GPIO1
3	GPIO2
4	GPIO3
5	GND
6	VDD IO
7	GPIO4
8	GPIO5
9	GPIO6
10	GPIO7
11	GND
12	VDD IO

GPIO/PMOD B	
PMOD Pin #	**GPIO #**
1	GPIO8
2	GPIO9
3	GPIO10
4	GPIO11
5	GND
6	VDD IO
7	GPIO12
8	GPIO13
9	GPIO14
10	GPIO15
11	GND
12	VDD IO

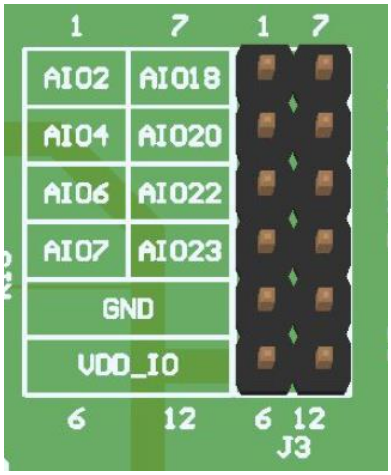
GPIO/PMOD C	
PMOD Pin #	**GPIO #**
1	GPIO16
2	GPIO17
3	GPIO18
4	NC
5	GND
6	VDD IO
7	EN
8	PWR
9	NC
10	NC
11	GND
12	VDD IO

Table 2. GPIO and PMOD Connector characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I_L	Input leakage current	-	-	2	-	µA
C_{IO}	Input-Output Pin Capacitance	-	-	7	-	pF
R_{ON}	Series Resistance	-	-	25	52	Ω
V_{IN}	Input Voltage	-	-0.5	-	V_{DDIO}	V

1.2 Analog I/O

Analog I/O pins can be used to transfer or read analog signals. Analog pins work only in combination with the ForgeFPGA™ Advanced Development Board.



GPIO/PMOD C	
"J3" Pin #	AIO #
1	AIO2
2	AIO4
3	AIO6
4	AIO7
9	GND
11	VDD IO
7	AIO18
8	AIO20
9	AIO22
10	AIO23
10	GND
12	VDD IO

Figure 4. AIO Connector Pinout

1.3 FPGA Current Measuring

"ForgeFPGA™ Socket Adapter #1" has an IC power consumption measurement option. To measure power consumption, remove jumpers JP3, JP4 and plug a current meter instead (typical load should not exceed 200 mA). Normally, these jumpers must be installed on the board (if current consumption measurement is not required).

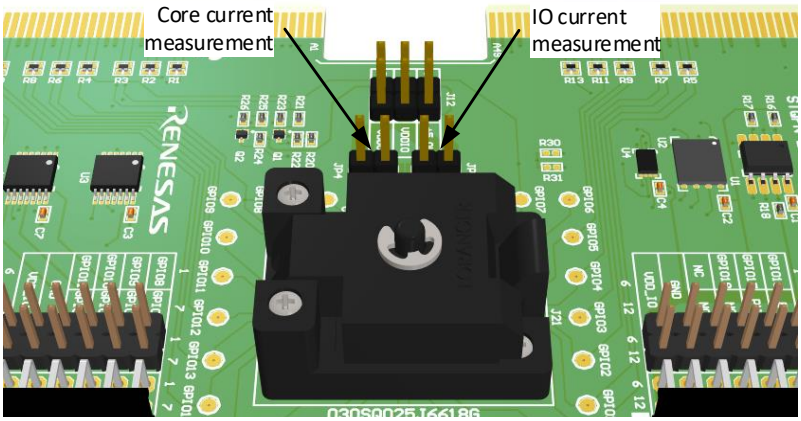


Figure 5. FPGA Current Measurement Setup

1.4 SPI Interface between FPGA, Flash Memory, Interaction and PMOD Connectors

Figure 6 shows the SPI flash interface connection across Output connectors, ForgeFPGA IC and Interaction connectors.

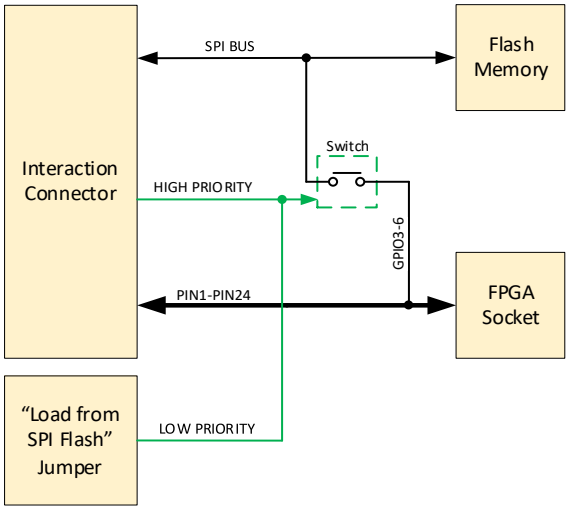
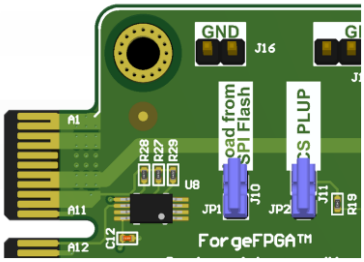


Figure 6. SPI interface Connection

"JP1" and "JP2" jumpers should be installed while working with Development Board. Jumper remove/set events are overridden and controlled by the Development Board. Table on Figure 7 shows jumper setup for Stand-alone work mode.



Mode	JP1	JP2
Internal OTP Memory	0	X
SPI FLASH Memory	1	1

Figure 7. Memory Selection Table for Boot Configuration

1.5 "EXT PWR" Connector

"ForgeFPGA™ Socket Adapter #1" can work with an external power supply – in this case three different power supply channels should be applied to the "EXT PWR" (J12) connector (shown in Figure 8). Voltage and current ranges for V_{DDIO} and V_{DDC} should match the ForgeFPGA IC specifications. "5.0 V" Terminal should be powered with 5.0V power supply to match GPIO characteristics on PMOD and 12-pin connector. External power supply option can be used only in case when Socket Adapter is not attached to the "ForgeFPGA Advanced Development Board.

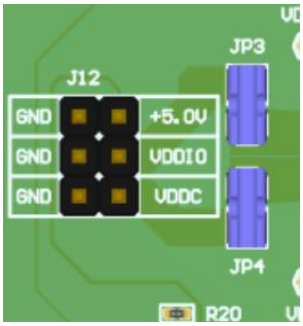


Figure 8. External Power Connector Pinout

2. Working with ForgeFPGA Products

To start working with ForgeFPGA products which using the Socket Adapter, user can choose two different methodologies: with ForgeFPGA Dev. Board or in stand alone mode, where FPGA config will be downloaded from onboard SPI flash.

2.1 Stand-alone Working Mode

As previously described, ForgeFPGA can boot from onboard flash as an SPI host. There are two ways of programming onboard flash: program with Development Board or program flash IC manually. Pins for programming flash chip are accessible through the PMOD A connector. For doing that, user needs to power the Socket Adapter from “EXT Power” connector as mentioned before.

If V_{DDIO} voltage is equal or greater than 3.0V - “5V” then the “V_{DDIO}” pins can be powered from the same source. For these operations, users also need to disable ForgeFPGA by applying logic 0 to “PWR” and “EN” pins. While doing these operation “JP1” and “JP2” jumpers must be installed. If SPI flash is programmed in a correct way by setting logic 1 to PWR and EN, ForgeFPGA will then boot from SPI Flash.

2.2 Configuration with ForgeFPGA Advanced Development Board

To start working with the ForgeFPGA products, connect the platform to the PC via a USB Type-C cable and connect the power supply. Important note, that USB cable should be connected directly to PC without any USB hubs and Docking stations. Make sure that socket adapter board is connected to the ForgeFPGA Dev. Board as shown in Figure 9.

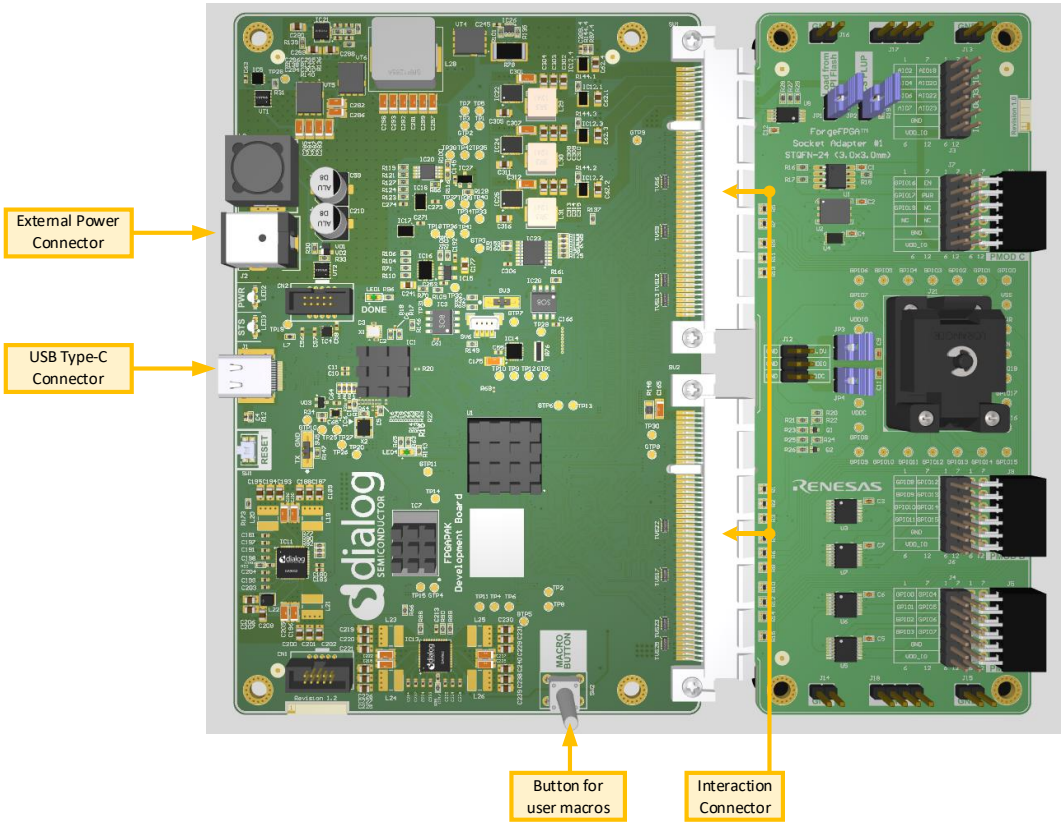


Figure 9. Development Kit

If all the connections are correct, then the red LED (PWR) will automatically be enabled. After selecting "ForgeFPGA Advanced Development Board" in Go Configure "Debug" tab , blue LED will blink several times and "HW-FW" version will be visible in left bottom corner of debugging control window (Figure 10).

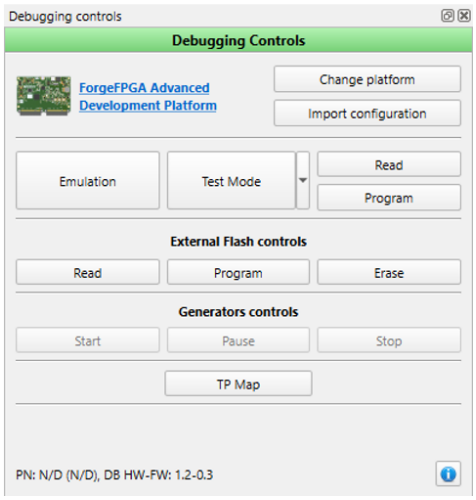
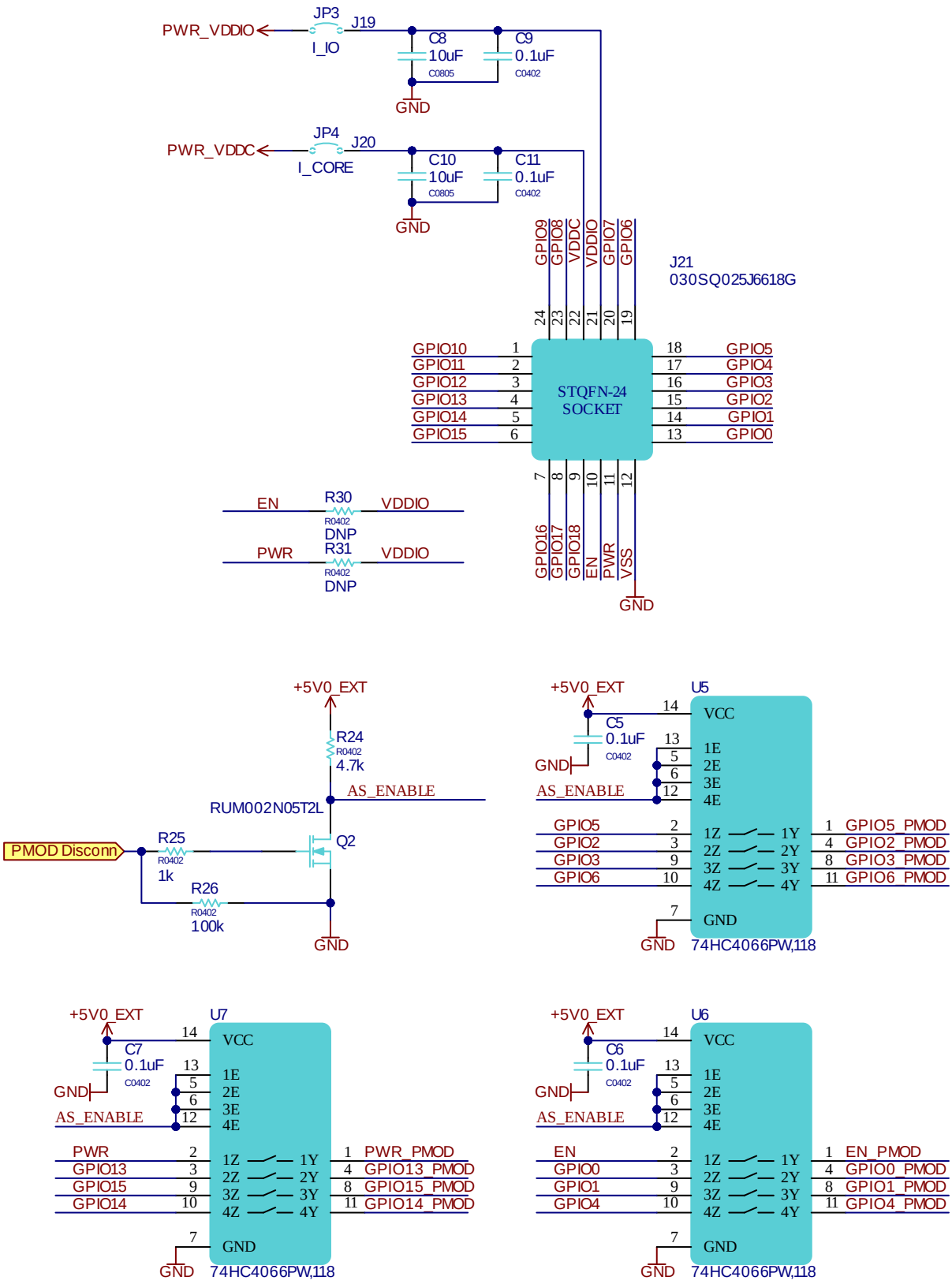


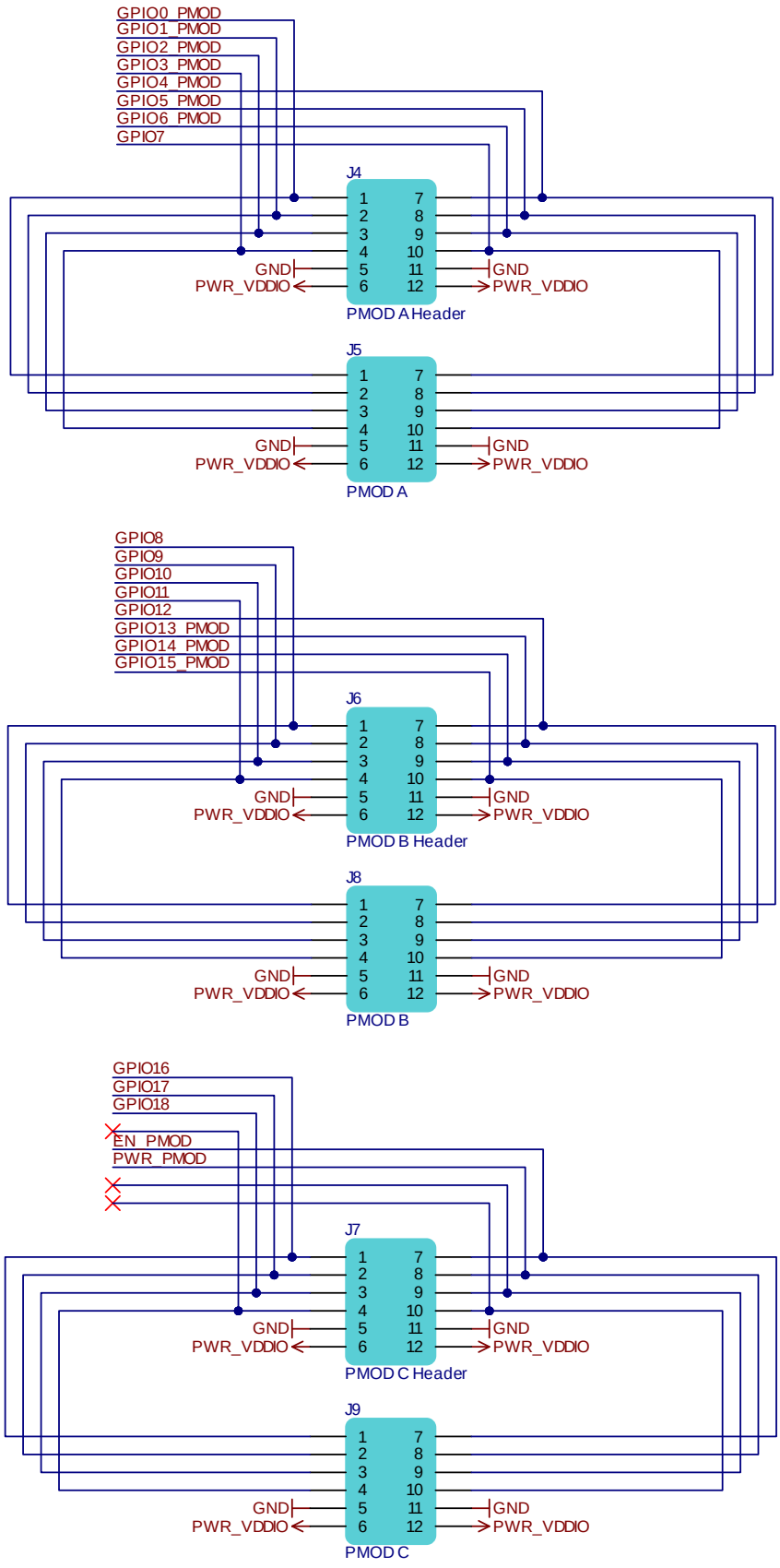
Figure 10. Debugging Controls

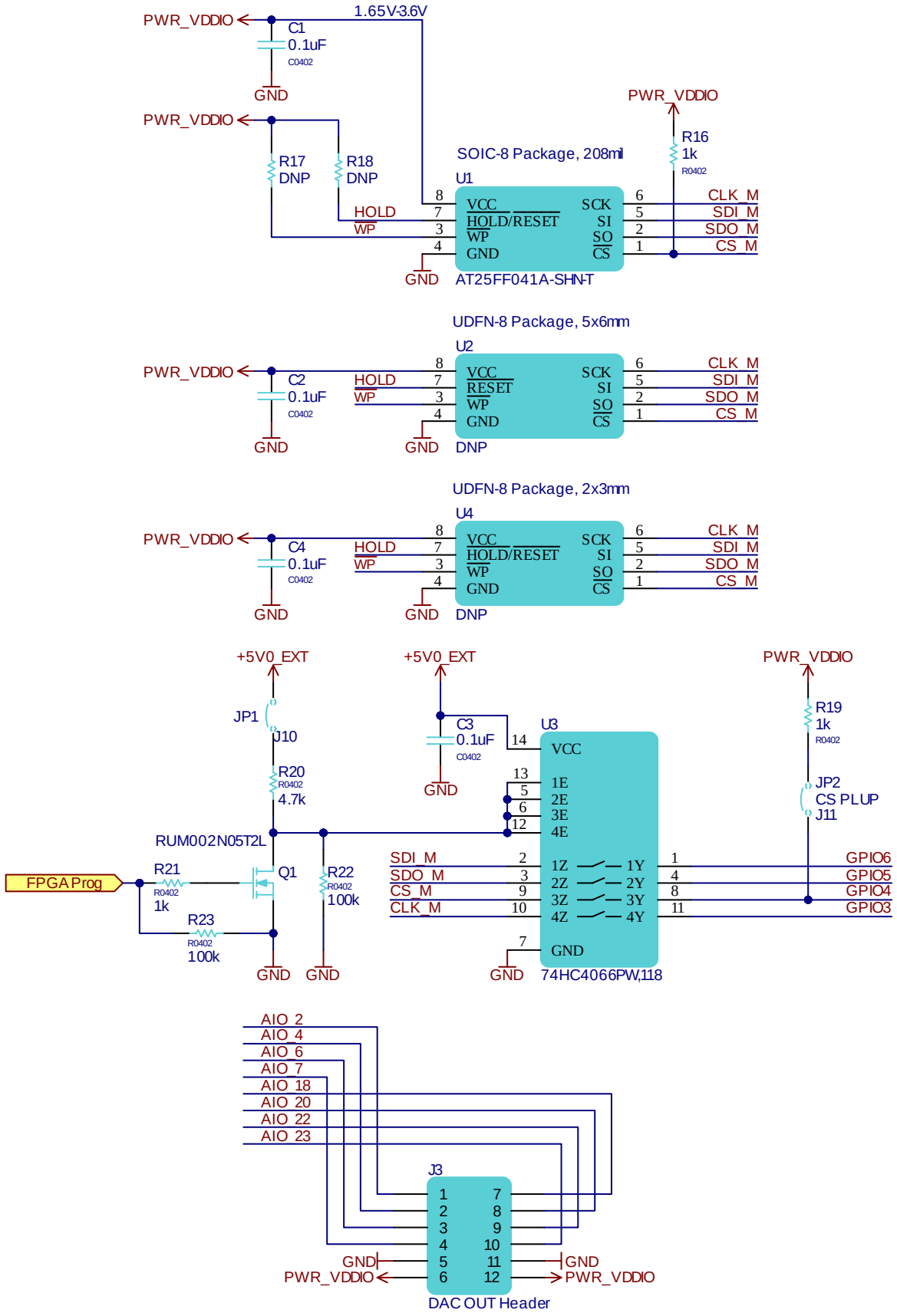
"Emulation" allows to debug the current project, it will only work after performing synthesis in FPGA Editor, "Test Mode" allows the users to debug the programmed project. "Read" button reads the programmed chip configuration and opens the project in the new software instance or in the "Project data" window of the current instance. "Program" button programs the chip with the current project. "TP Map" shows the test point map on the work area, reflecting the physical Test Points on the development platform.

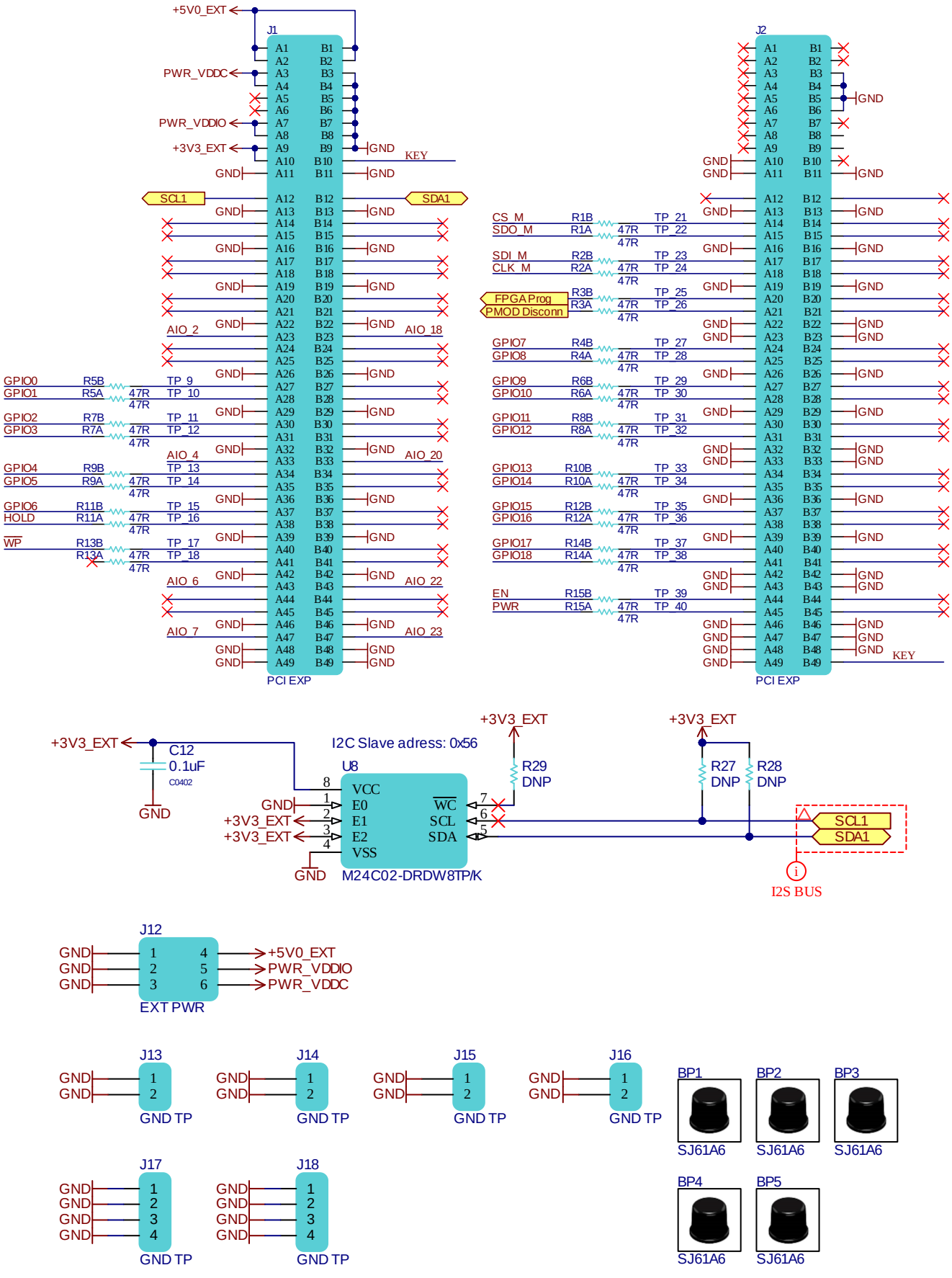
The more detailed information about Go Configure software can be found in ForgeFPGA Software User Guide

3. Schematic Diagram




GPIO0_PMOD
GPIO1_PMOD
GPIO2_PMOD
GPIO3_PMOD
GPIO4_PMOD
GPIO5_PMOD
GPIO6_PMOD
GPIO7
J4
1 7
2 8
3 9
4 10
GND 5 11 GND
PWR_VDDIO 6 12 PWR_VDDIO
PMOD A Header
J5
1 7
2 8
3 9
4 10
GND 5 11 GND
PWR_VDDIO 6 12 PWR_VDDIO
PMOD A
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13_PMOD
GPIO14_PMOD
GPIO15_PMOD
J6
1 7
2 8
3 9
4 10
GND 5 11 GND
PWR_VDDIO 6 12 PWR_VDDIO
PMOD B Header
J8
1 7
2 8
3 9
4 10
GND 5 11 GND
PWR_VDDIO 6 12 PWR_VDDIO
PMOD B
GPIO16
GPIO17
GPIO18
EN_PMOD
PWR_PMOD
J7
1 7
2 8
3 9
4 10
GND 5 11 GND
PWR_VDDIO 6 12 PWR_VDDIO
PMOD C Header
J9
1 7
2 8
3 9
4 10
GND 5 11 GND
PWR_VDDIO 6 12 PWR_VDDIO
PMOD C


PWR_VDDIO
1.65V-3.6V
C1
0.1uF
C0402
GND
R17
DNP
R18
DNP
SOIC-8 Package, 208mil
U1
HOLD
WP
VCC
HOLD/RESET
WP
GND
SCK
SI
SO
CS
AT25FF041A-SHN-T
R16
1k
R0402
CLK_M
SDI_M
SDO_M
CS_M
UDFN-8 Package, 5x6mm
U2
C2
0.1uF
DNP
UDFN-8 Package, 2x3mm
U4
C4
0.1uF
DNP
+5V0_EXT
JP1
J10
R20
4.7k
RUM002N05T2L
FPGAProg
R21
1k
Q1
R22
100k
R23
100k
C3
0.1uF
U3
VCC
1E
2E
3E
4E
1Z
2Z
3Z
4Z
1Y
2Y
3Y
4Y
GND
74HC4066PW,118
R19
1k
JP2
CS PLUP
J11
GPIO6
GPIO5
GPIO4
GPIO3
AIO_2
AIO_4
AIO_6
AIO_7
AIO_18
AIO_20
AIO_22
AIO_23
J3
DAC OUT Header


+5V0_EXT
J1
PWR_VDDC
PWR_VDDIO
+3V3_EXT
KEY
SCL1
SDA1
AIO_2
AIO_18
AIO_4
AIO_20
AIO_6
AIO_22
AIO_7
AIO_23
PCI EXP
J2
CS_M
SDO_M
SDI_M
CLK_M
FPGA Prog
PMOD Disconn
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
EN
PWR
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
HOLD
WP
47R
I2C Slave adress: 0x56
C12
0.1uF
C0402
U8
VCC
E0
E1
E2
VSS
WC
SCL
SDA
M24C02-DRDW8TP/K
R29
DNP
R27
R28
I2S BUS
J12
EXT PWR
J13
J14
J15
J16
GND TP
BP1
BP2
BP3
BP4
BP5
SJ61A6

4. Bill Of Materials

#	Designator	Manufacturer Part Number	Manufacturer	Quantity
1	BP1, BP2, BP3, BP4, BP5	SJ61A6	3M	5
2	C1-C7, C9, C11, C12	GCM155R71C104KA55D	Murata	10
3	C8, C10	GRM21BR61C106KE15L	Murata	2
4	J3, J4, J6, J7	67996-212HLF	Amphenol ICC / FCI	4
5	J5, J8, J9	PPPC062LJBN-RC	Sullins	3
6	J10, J11, J19, J20	68000-102HLF	Amphenol ICC / FCI	4
7	J12	10129381-906002BLF	Amphenol	1
8	J13, J14, J15, J16	68000-102HLF	Amphenol ICC / FCI	4
9	J17, J18	77311-101-04LF	Amphenol ICC / FCI	2
10	J21	030SQ025J6618G	Dialog Semiconductor	1
11	JP1, JP2, JP3, JP4	NPC02SXON-RC	Sullins	4
12	Q1, Q2	RUM002N05T2L	Rohm	2
13	R1-R15	S41X043470JP	CTS	15
14	R16, R19, R21, R25	RC0402JR-071KL	Yageo	4
15	R17, R18, R27, R28-R31	DNI		7
16	R20, R24	RC0402JR-074K7L	Yageo	2
17	R22, R23, R26	RC0402JR-07100KL	Yageo	3
18	U1	AT25FF041A-SHN-T	Adesto Technologies	1
19	U2	DNI		1
20	U3, U5, U6, U7	74HC4066PW,118	Nexperia	4
21	U4	DNI		1
22	U8	M24C02-DRDW8TP/K	STMicroelectronics	1

5. Ordering Information

Part Number	Description
SLG47910V-SKT	ForgeFPGA Socket Adapter #1

6. Revision History

Revision	Date	Description
1.00	May 10, 2024	Initial release.