ForgeFPGA Advanced Development Board R1.2 Manual

User Manual

ForgeFPGA™

Advanced Development Board R1.2

R12UT0023EU0100

Contents

Figures

The ForgeFPGA Advanced Development Board R1.2 is a multi-functional tool that allows you to develop FPGA designs by providing onboard multichannel power source, digital signal generator, and logic analyser features. This development tool is a precision platform, which can replace a stack of lab equipment for digital circuit debug.

PC Requirements

- Windows 7/8.1/10/11, macOS (v10.15 or higher), Ubuntu 18.04/20.04/22.04, Debian 11/Testing
- USB 3.0 (primary), USB 2.0 interface.

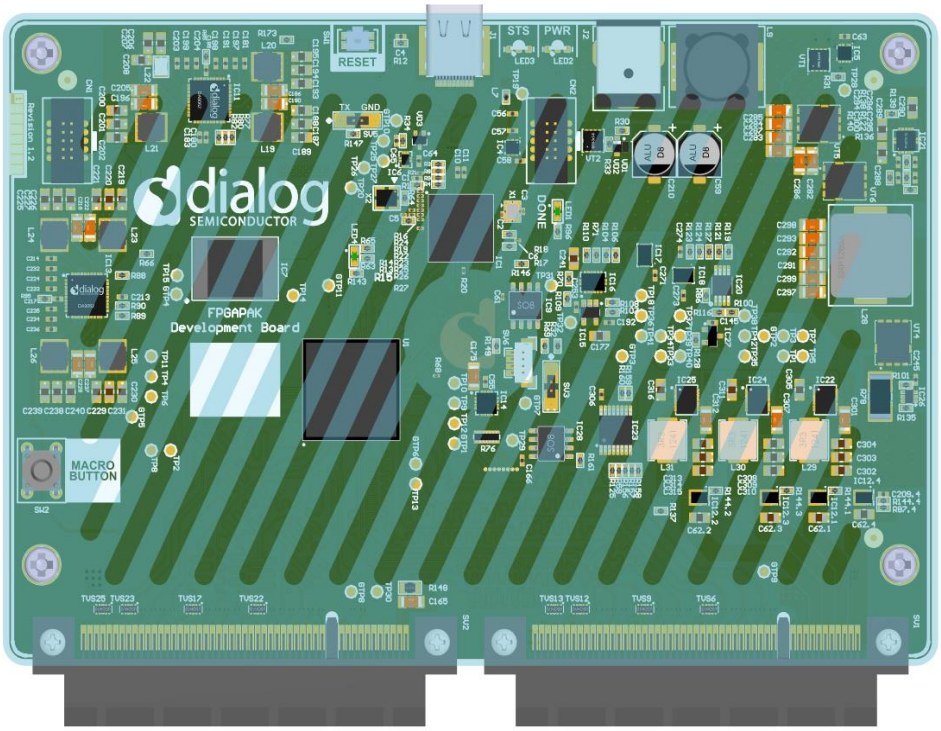


Figure 1: ForgeFPGA Advanced Dev. Board R1.2

Features

Driven by the Go Configure Software Hub, the ForgeFPGA Dev. Board can be configured to work as several digital circuit debug instruments, which include:

- Logic analyzer (LA) up to 800MS/s
- Digital pattern generator (PG) up to 200MS/s
- 80 Test Points (TP) shared with LA and PG
- Real-time Test Point control.
- Three Programmable Power Supplies
- Eight Configurable Voltage Reference Sources

1. Functional Description

The main components are shown in Figure 2.

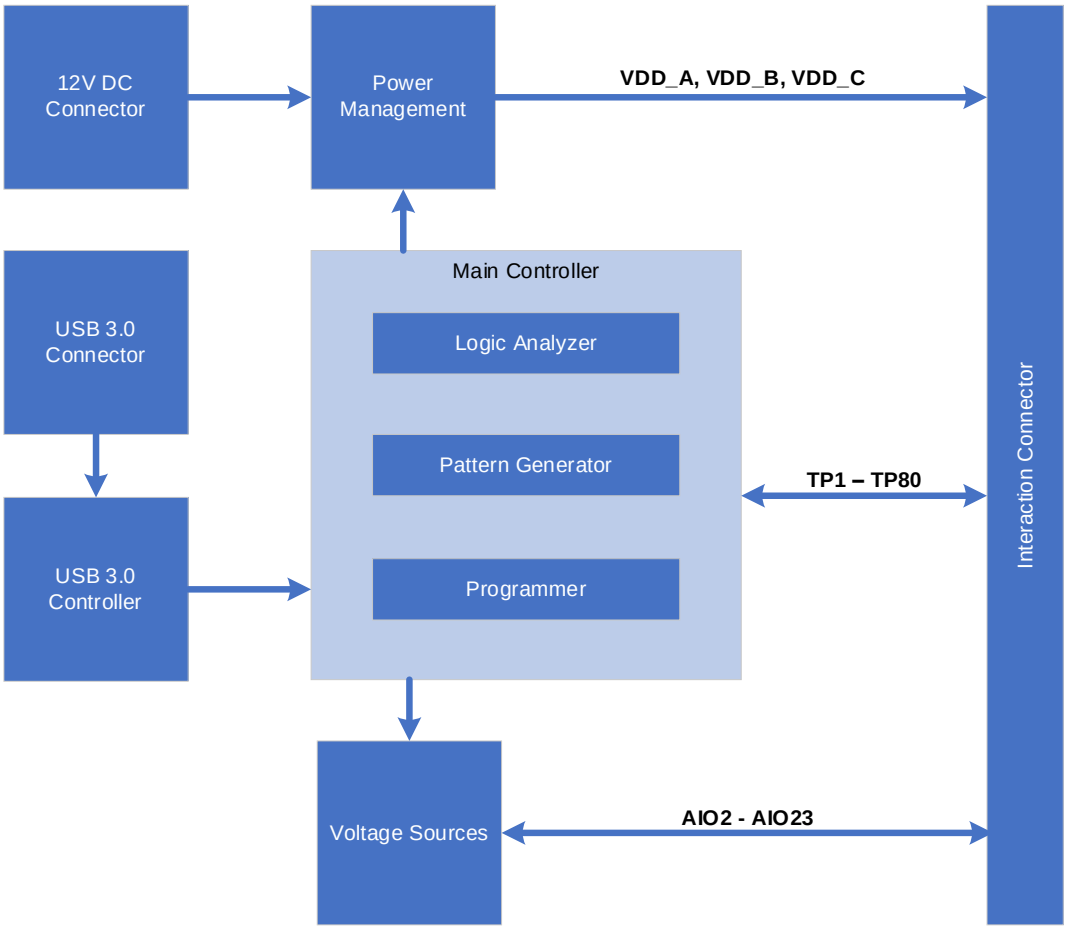


Figure 2: ForgeFPGA Dev. Board Structure

A set of 80 Test Points provides all interactions between ForgeFPGA Development Board and ForgeFPGA IC. Test Points and power supplies are configurable by the software depending on the actual IC's manufactured part number. There are two main options for Test Points – programming interface and real-time control interface. Programming interface works only during programming and emulation entry. When programming or emulation entry is done – programming interface Test Points move their functionality to real-time control depending on FPGA chip part number.

ForgeFPGA Advanced Development Board has following connectors:

- External power supply connector
- USB 3.0 Type-C connector
- 2 Interaction connectors

Development Board has two LEDs – Power LED and Status LED, and two buttons – reset and user "Macro" buttons. Their operation logic is described in subsection 4.2.

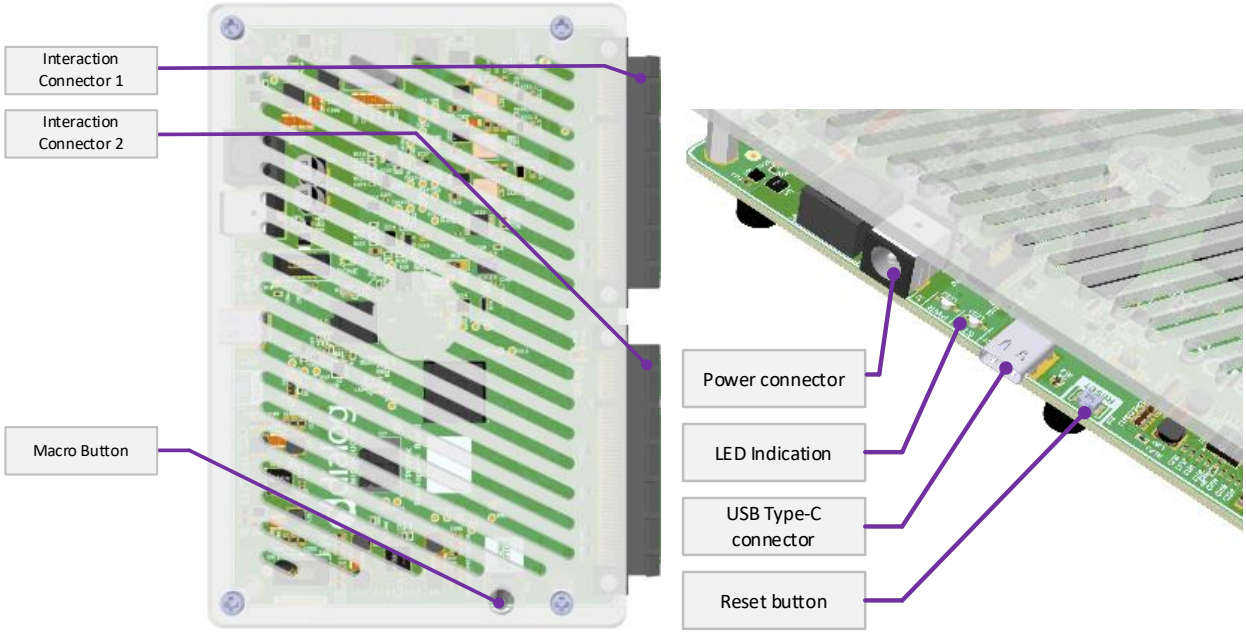


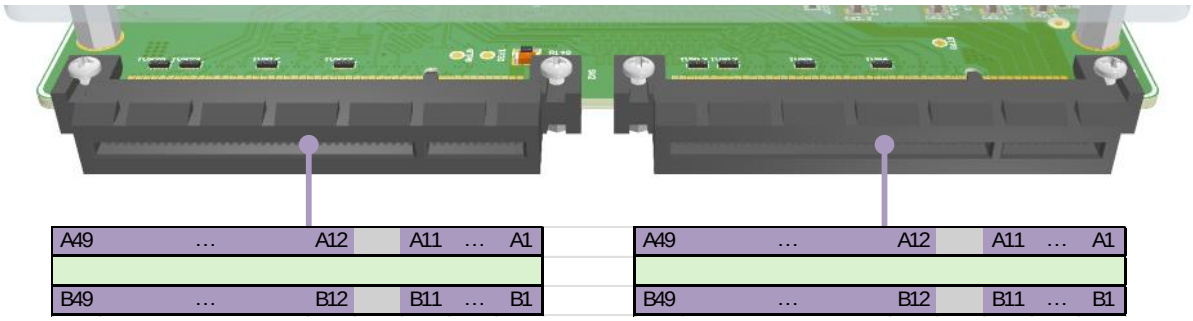
Figure 3: ForgeFPGA Dev. Board Overview

Table 1 shows general USB and Power supply characteristics that are required for Development Board stable functionality.

Table 1. General Specifications

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{PSU}	Power Supply Voltage	-	-	12	-	V
I_{PSU}	Power Supply Rated Current	-	5	-	-	A
V_{USB}	USB Input Voltage	-	-	5	-	V
I_{USB}	USB Input Current	-	-	-	100	mA
T_A	Operating Ambient Temperature	-	15	-	45	^{0}C
	Board Dimensions	-	150 X 144			mm
	Weight	-	146			g

All TPs and three Programmable Power Sources are shared between two Interaction Connectors. Figure 4 demonstrates Interaction Connector map. TP1-TP40 are referred to VDD_A Power Source, TP41-TP80 are referred to VDD_B. Basically, the board supports dual V_{DDIO} devices. V_{DDC} is used for FPGA core power. AIO signals are used as constant voltage sources. All pins that marked as “RSRV” are used for internal configuration and power purposes.



CONNECTOR 2			
Pin name	Pin number	Pin number	Pin name
RSRV	A1	B1	RSRV
	A2	B2	
	A3	B3	GND
	A4	B4	
	A5	B5	
	A6	B6	
	A7	B7	RSRV
	A8	B8	
	A9	B9	
	A10	B10	
GND	A11	B11	GND
RSRV	A12	B12	RSRV
GND	A13	B13	GND
TP21	A14	B14	TP61
TP22	A15	B15	TP62
GND	A16	B16	GND
TP23	A17	B17	TP63
TP24	A18	B18	TP64
GND	A19	B19	GND
TP25	A20	B20	TP65
TP26	A21	B21	TP66
GND	A22	B22	GND
AIO2	A23	B23	AIO18
TP27	A24	B24	TP67
TP28	A25	B25	TP68
GND	A26	B26	GND
TP29	A27	B27	TP69
TP30	A28	B28	TP70
GND	A29	B29	GND
TP31	A30	B30	TP71
TP32	A31	B31	TP72
GND	A32	B32	GND
AIO4	A33	B33	AIO20
TP33	A34	B34	TP73
TP34	A35	B35	TP74
GND	A36	B36	GND
TP35	A37	B37	TP75
TP36	A38	B38	TP76
GND	A39	B39	GND
TP37	A40	B40	TP77
TP38	A41	B41	TP78
GND	A42	B42	GND
AIO6	A43	B43	AIO22
TP39	A44	B44	TP79
TP40	A45	B45	TP80
GND	A46	B46	GND
AIO7	A47	B47	AIO23
GND	A48	B48	GND
GND	A49	B49	GND

PCB

CONNECTOR 1			
Pin name	Pin number	Pin number	Pin name
RSRV	A1	B1	RSRV
	A2	B2	
VDD _C	A3	B3	GND
	A4	B4	
VDD _B	A5	B5	
	A6	B6	
VDD _A	A7	B7	
	A8	B8	
RSRV	A9	B9	
	A10	B10	RSRV
GND	A11	B11	GND
RSRV	A12	B12	RSRV
GND	A13	B13	GND
TP1	A14	B14	TP41
TP2	A15	B15	TP42
GND	A16	B16	GND
TP3	A17	B17	TP43
TP4	A18	B18	TP44
GND	A19	B19	GND
TP5	A20	B20	TP45
TP6	A21	B21	TP46
GND	A22	B22	GND
GND	A23	B23	GND
TP7	A24	B24	TP47
TP8	A25	B25	TP48
GND	A26	B26	GND
TP9	A27	B27	TP49
TP10	A28	B28	TP50
GND	A29	B29	GND
TP11	A30	B30	TP51
TP12	A31	B31	TP52
GND	A32	B32	GND
GND	A33	B33	GND
TP13	A34	B34	TP53
TP14	A35	B35	TP54
GND	A36	B36	GND
TP15	A37	B37	TP55
TP16	A38	B38	TP56
GND	A39	B39	GND
TP7	A40	B40	TP57
TP18	A41	B41	TP58
GND	A42	B42	GND
GND	A43	B43	GND
TP19	A44	B44	TP59
TP20	A45	B45	TP60
GND	A46	B46	GND
GND	A47	B47	GND
GND	A48	B48	GND
GND	A49	B49	GND

PCB

Figure 4: Interaction Connector Pinout

2. Specifications

2.1 Configurable Test Points

ForgeFPGA Dev. Board has 80 configurable Test Points (TP). Each TP can work as a channel in the logic analyzer (LA) and the pattern generator (PG). In addition to PG and LA function, TPs can be controlled manually by setting to VDD, GND and Hi-Z states, or programmable software button.

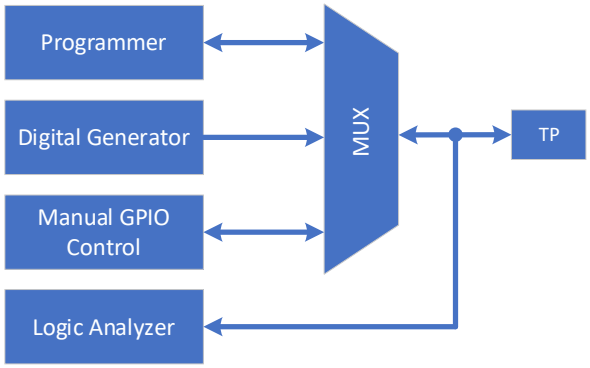


Figure 5: TP Interconnect Structure

Output Interaction connectors are optimized for high-speed digital applications. Each TP matches to 50-ohm impedance (Z0).

Note: The development board has 80 TP, but access to them depends on actual ForgeFPGA part number.

Table 2. TP1-TP80 Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IH}	High input voltage		65% V_{DD}	-	V_{DD}+0.3	V
V_{IL}	Low input voltage		-0.3	-	35% V_{DD}	V
I_{OH}	High-level output current	V_{DD}=3.3V	-	16	-	mA
I_{OL}	Low-level output current		-	16	-	mA
V_{OH}	Low-level output voltage		-	-	0.4	V
V_{OL}	High-level output voltage		75% V_{DD}	-	-	V
t_R	Output rise time	R_L = 10k; C_L= 10pF	-	2.4	-	ns
t_F	Output fall time	R_L = 10k; C_L= 10pF	-	1.7	-	ns
V_{CLAMP}	Input diode clamp voltage	I_{PP} =1A, from TP to GND	-	6.6	-	V
I_L	Input leakage current	V_{DD}=3.3V	-	15	-	µA
C_{IO}	Input-Output Pin Capacitance		-	8	-	pF

Table 2 shows GPIO characteristics. VDD value depends on TP group and matches voltage corresponding to VDD_A or VDD_B (see Figure 4).

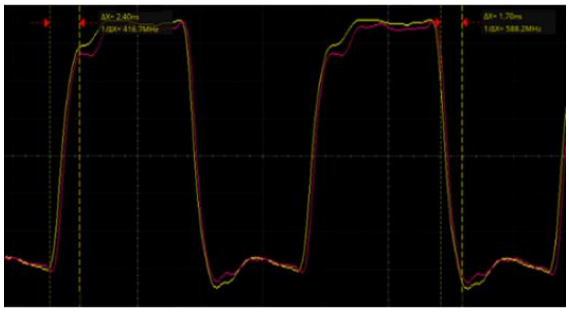


Figure 6: GPIO output signal waveform RL = 10k, CL = 10pF. 5ns/div, 500mv/div

Figure 6 shows 50MHz clock signal, where t_R and t_F are measured between 10% and 90% of V_{OL} to V_{OH}.

2.2 Power Supplies

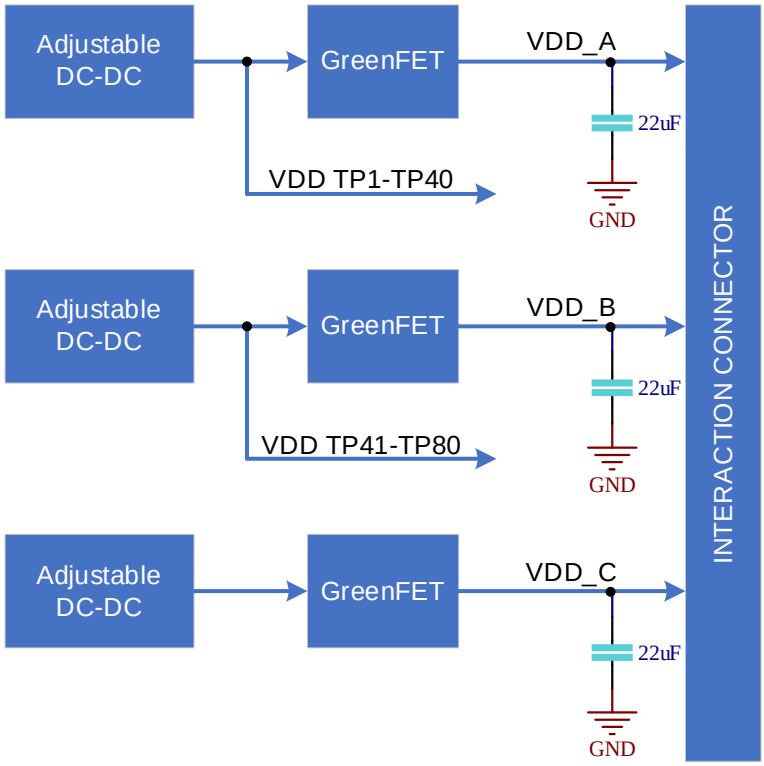


Figure 7: Power Structure

The board has three programmable power supplies. The maximum available output current is 3.4A for each source. The same voltage is supplied to the TPs, for keeping the logic level compatibility with externally connected circuit. As mentioned before, VDD_A works as logic level reference for TP1-TP40, VDD_B for TP41-TP80. If Load current value exceeds $I_{OUT(MAX),\ VDD}$ output will go into OCP mode. Output voltage range for all power sources may vary. Limits will be set according to selected target device in Go Configure software.

Table 3. Voltage Sources Characteristics (VDD_A, VDD_B, VDD_C)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OUT}	Output Voltage	$I_{OUT(MIN)} \le I_{OUT} \le I_{OUT(MAX)}$	0.8	-	3.3	V
V_{STEP}	Output Voltage Regulation Step	$V_{OUT(MIN)} \le V_{OUT} \le V_{OUT(MAX)}$	-	25	-	mV
ΔV_{OUT}	Output Voltage DC Error	$I_{OUT(MIN)} \le I_{OUT} \le I_{OUT(MAX)}$	-2	-	2	%
I_{OUT}	Output Load Current	$V_{OUT(MIN)} \le V_{OUT} \le V_{OUT(MAX)}$	0	-	3.4	A
$V_{OUT(SR)}$	V_{OUT} Slew Rate	$I_{OUT(MIN)} \le I_{OUT} \le I_{OUT(MAX)}$	2.24	2.8	4	V/ms
DC_{LOAD}	Load Regulation	$I_{OUT(MIN)} \le I_{OUT} \le I_{OUT(MAX)}$	-	5	-	mV
AC_{LOAD}	Transient Load Response	$t_r = t_f$ = 100 ns; Step 1.5 A	-20	-	20	mV
C_L	Load Capacitance	--	0	-	150	µF
$R_{DISCHRG}$	Output Discharge Resistance	$V_{OUT(MIN)} \le V_{OUT} \le V_{OUT(MAX)}$	168	210	252	Ω
V_{RIPPLE}	Output Ripple	I_{OUT} = 1A		12		mV

2.3 Logic Analyzer

ForgeFPGA Dev. Board Includes 64 channel Logic Analyzer with sampling rate up to 800MS/s and memory depth up to 65k points. Number of channels, sample rate and memory depth are inter-depended. Characteristics in Table 4 describe parameters in three different modes based on selected sample rate. Logic Analyzer supports a wide range of sampling rates which are shared between three sampling modes. The number of available channels and number of points (memory depth) are defined depending on sampling mode. These dependencies are shown in Table 4.

Table 4. Logic Analyzer Specifications

Sample rate (MS/s)	Sample Mode	Number of available channels	Memory depth (total number of points)
800 (max)	MODE 3	16	65536
400	MODE 2	32	32768
200	MODE 1	64	16384
100			
50			
40			
…			
190,7 S/s (min)			

Logic Analyzer works in two trigger modes: internal (invoked by configured triggering conditions on the target channels) and external (invoked by pressing onboard macro button). Internal triggering is configured by two setting types: group of per-channel conditions (edge, level triggering) and single global condition (AND/OR triggering), which are both described in Table 5.

Table 5 . Logic Analyzer trigger settings

Trigger mode	Trigger setting type	Available conditions	Description
External	-	Macro button pressed	Triggering occurs when onboard macro button pressed.
Internal	Per-channel	Rising, falling or both edges and high or low logic states (1)	One condition can be selected per each channel.
	Global	AND / OR	Collection type of per-channel conditions: AND – trigger occurs when all selected per-channel conditions are satisfied at current sampling time. OR – triggering occurs when at least one per-channel condition is satisfied at sampled period.

(1) For proper detection, electrical parameters of input signal should match GPIO Specifications (see Table 2).

The number of points to be written after trigger occurred is configurable, that allows to set desired position of trigger point in Logic Analyzer data waveform. This feature is shown in figure below.

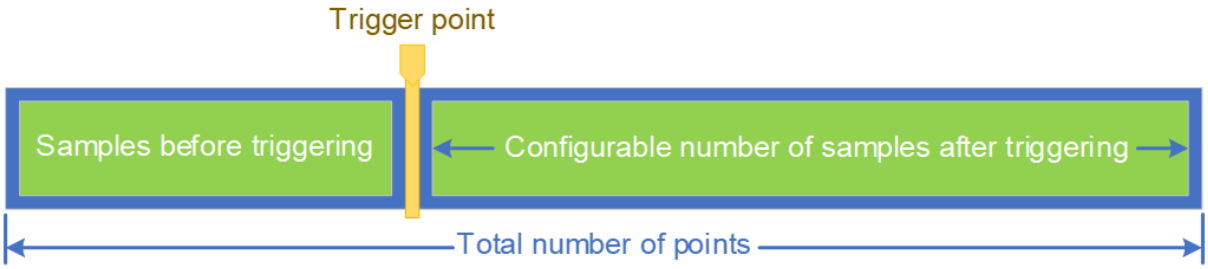


Figure 8: Configurable Position of Trigger Point in Data Buffer

The block schematic of Logic Analyzer workflow is shown below.

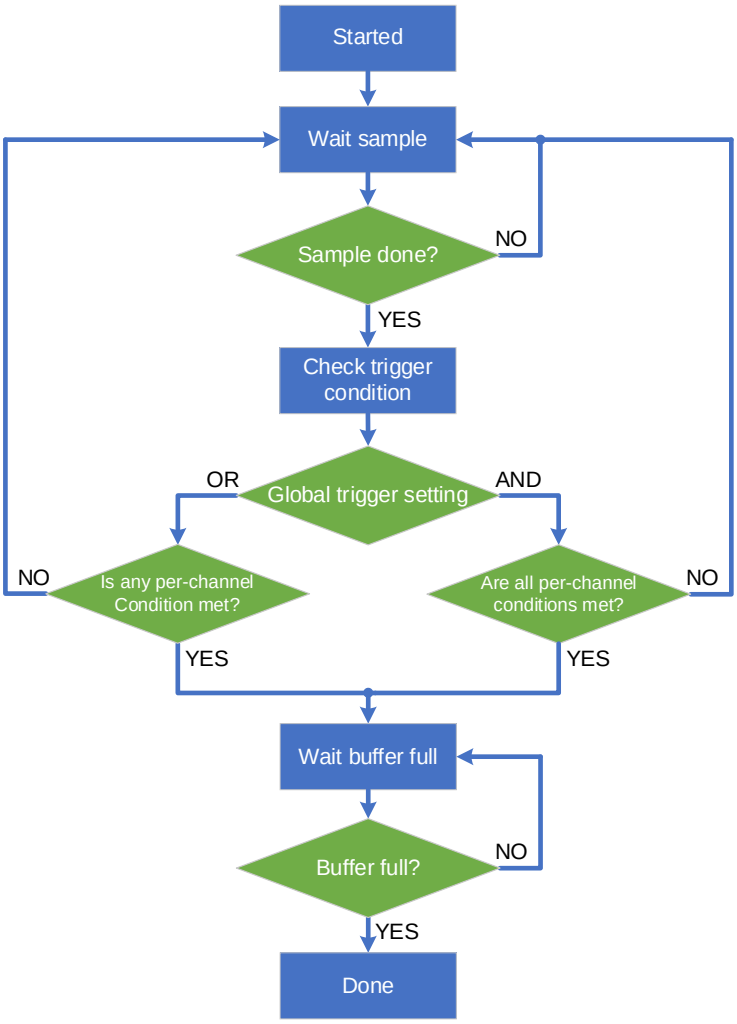


Figure 9: Logic Analyzer Workflow

2.4 Pattern Generator

Pattern generator has 64 digital channels that are connected to each TP that is currently used in Go Configure emulation or testing modes. Sample rate is up to 200MS/s. Output signal is defined as a set of “points”. Each point contains the output state and duration value for all 64 channels. Minimum duration value is 5ns. When the number of points with minimal duration in a row exceeds 512 – sample rate decreases to 40MS/s. Total number of available points is dynamic and depends on pattern configurations. All 64 channels are synchronized in time and the generator has a global start option for all channels at the same time.

Table 6. Digital Pattern Generator Specifications

Sample Rate (1)	Up to 200 MS/s
Number of channels:	64
Parametric Generator Features	PWM, CLK, UART, Raw
Repeat Functions	Cyclic, One-Shot, Custom
Repeat Count	2-255
Output Type	Push-Pull, OD HI, OD LO
Prestart/Pause/End Type	Low, High, Hi-Z
Waveform Type	Square

(1) Sample rate will be decreased depending on created waveform complexity

2.5 Configurable Voltage Sources

ForgeFPGA Dev. Board has eight built in voltage source channels. Figure 3 demonstrated voltage source locations as AIO (Analog Input-Output). All eight sources are working independently and can be set either to Hi-Z or constant voltage output. Voltage source characteristics are described in Table 6.

Table 7. Configurable Voltage Source (AIO2-AIO23) Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OUT}	Output voltage Range	-	0	-	4096	mV
ΔV_{OUT}	Output voltage Accuracy	$10mV \leq V_{OUT} \leq 4000mV$	-1	-	1	mV
-	Zero Code Error	-	-	0.65	2	mV
t_{sett}	Settling Time	-	-	6	-	µS
Z_O	DC Output impedance	-	-	33	-	Ω
-	Short-Circuit Current	-	-	-	25	mA
I_L	Off State Leakage Current	-	-	1	-	µA

3. Working with ForgeFPGA Products

To start working with the ForgeFPGA products, connect the platform to the PC via a USB Type-C cable and connect the power supply. Important note, that USB cable should be connected directly to PC without any USB hubs and Docking stations. Make sure that socket adapter board is connected to the ForgeFPGA Dev. Board as shown in Figure 10.

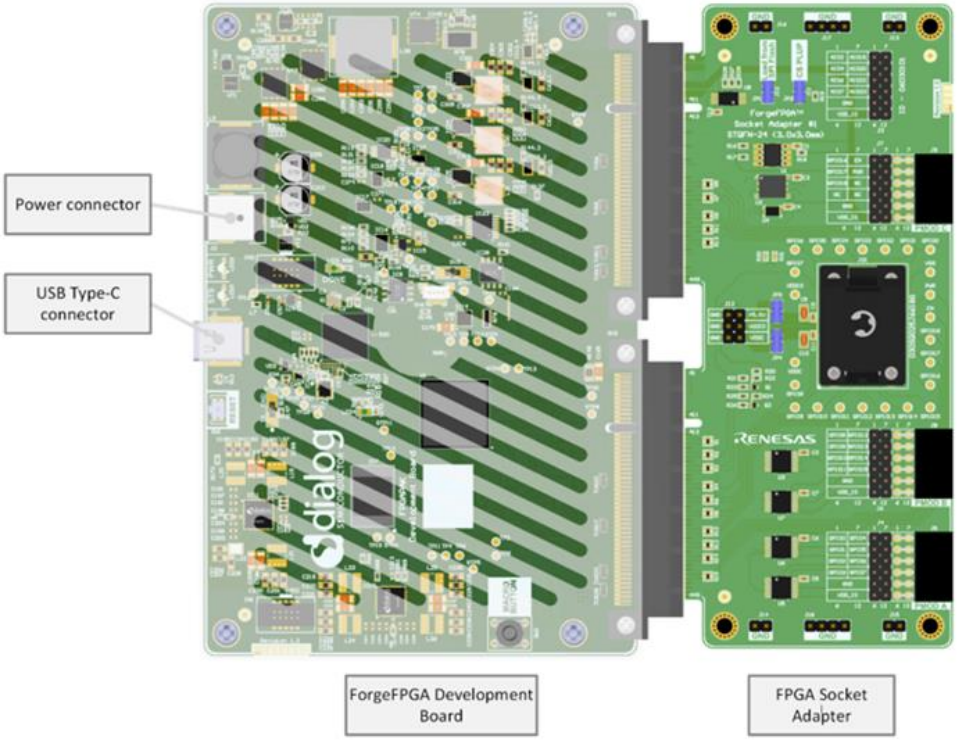


Figure 10: Development Kit

If all the connections are correct, then the red LED (PWR) will be automatically enabled. After Selecting "ForgeFPGA Advanced Development Board" in Go Configure "Debug" tab – blue LED will blink several times and "HW-FW" version will be available in left bottom corner of debugging control window (Figure 11).

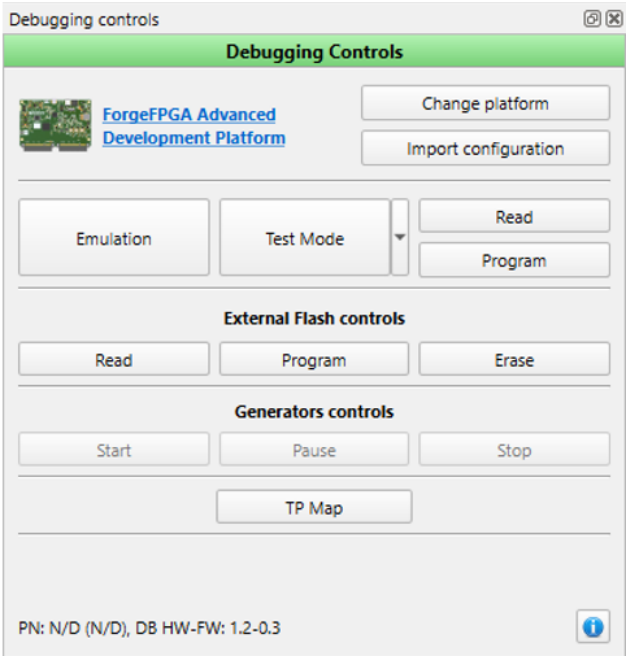


Figure 11: Debugging Setup for Socket Adapters

“Emulation” allows to debug the current project, it will only work after performing synthesis in FPGA Editor, “Test Mode” is used to debug the programmed project. “Read” button helps in reading the programmed chip configuration and opens the project in the new software instance or in the “Project data” window of the current instance. “Program” button is used to program the chip with the current project. “TP Map” shows the test point map on the work area, reflecting the physical Test Points on the development platform.

The more detailed information about Go Configure software can be found in

3.1 Socket Adapter Board

The ForgeFPGA Development Board can be used with additional external boards called a Socket Adapter. The function of the socket adapter board is to implement a connection between the target device and the ForgeFPGA Dev. Board. To implement this, the ForgeFPGA Dev. Board uses Dual Interaction connector.

ForgeFPGA Software User Guide

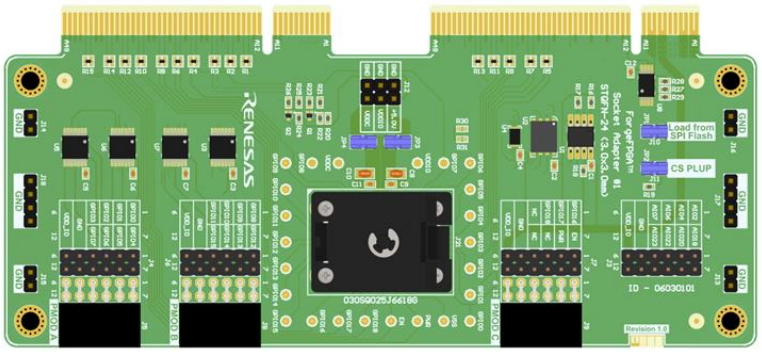


Figure 12: Example of a Socket Adapter Board

The socket adapter is shown in Figure 12. There is a plastic socket on the adapter board. The FPGA chip should be inserted into this plastic socket, with appropriate “pin1” position.

4. Additional Features

4.1 Kit Contents

- ForgeFPGA Advanced Dev. Board R1.2
- Socket Adapter
- USB 3.0 to USB Type-C cable
- AC/DC 12V Power Supply
- AC Power Cable
- PMOD LED Adapter Board
- ForgeFPGA Samples

Figure 13: Kit Content

4.2 Status Display and Controls

The ForgeFPGA Dev. Board has two buttons and two status LEDs. Their operating logic is described below:

LEDs:

Table 8. LED Indication

PWR (RED)	STS (BLUE)	
OFF	OFF	USB or power supply is not connected
ON	OFF	Standby mode
ON	BLINK	USB data transfer
BLINK	OFF	Power fail

Buttons:

- "RESET" – resets the board.
- "MACRO BUTTON" – user button. Its functionality is defined by the software.

4.3 Firmware Update

Firmware update occurs automatically when ForgeFPGA Dev. Board is connected to the computer with Go Configure Software Hub open. It is enough to connect 2 cables; power and USB, then launch Go Configure software. There are no additional requirements or restrictions.

5. Ordering Information

Part Number	Description
SLG7DVKFORGE-KIT	ForgeFPGA SLG47910 KIT

6. Revision History

Revision	Date	Description
1.00	May 10, 2024	Initial release.