

EU096-3 - Flexible 6-Ch Power Sequencer

Hardware Guide

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1. Overview

This document deals with a Flexible 6-Channel Power Sequencer Design based on a Renesas general purpose RL78/G12 microcontroller and 6 discrete DC/DC regulators with integrated power MOSFETs. For the ease of use, a Low-Iq LDO is utilized to supply the microcontroller out of 12V supply voltage rail.

The proprietary power sequencing solution based on a Standard Renesas Microcontroller offers great flexibility and it is ultimately scalable to a very broad range of FPGA and SoC applications (due to unrestrained programmable delays, sensing of main input voltage via ADC of the microcontroller, monitoring of each single power rail via MCU-integrated ADC, reading the Power good-signals of each DC/DC Converter etc.).

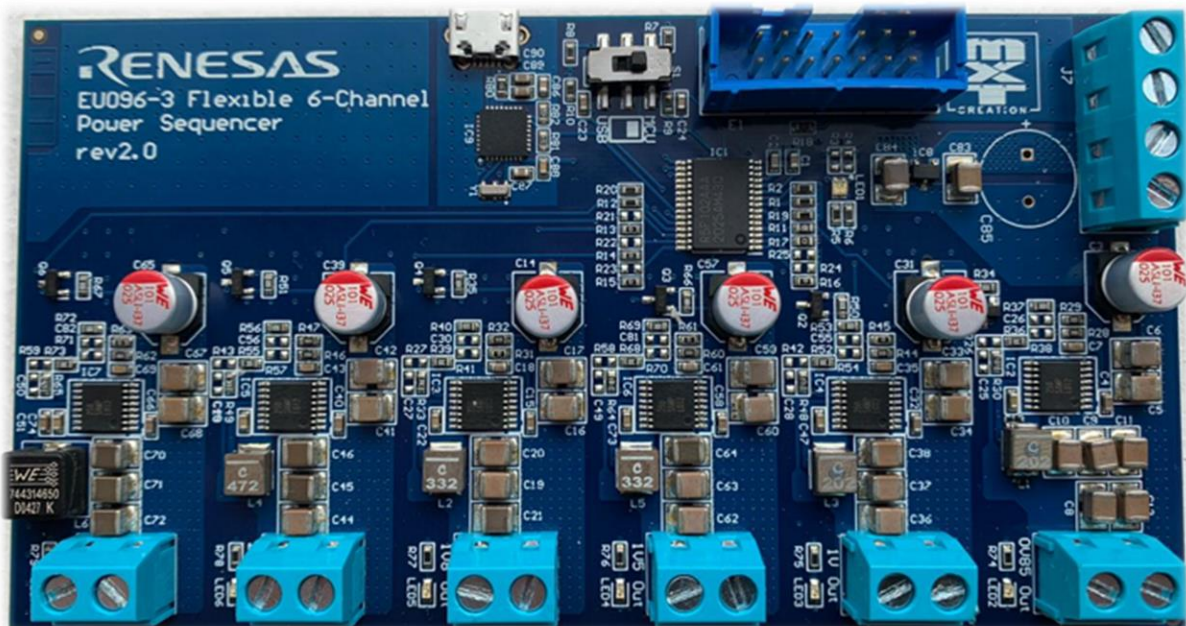


Figure 1. EU096-3 Power Sequencer Board

1.1 Features

The main components of the Power sequencer application are:

- *Board Power Supply*, the default power source is 12V, supplied from an external connector: 12V Input.
- Six independent *DC-DC Converters* supplied by 12V input:
 - 0.85V 5A RAA211250, asynchronous buck regulators with integrated low-side and high-side FETs, 4.5V to 30V Input. This device provides up to 5A of continuous output current with adjustable output voltage, adjustable soft-start time, internal or external compensation options, programmable switching frequency with 400kHz as default, and output Power-Good (PG) indicator.
 - 1V 5A RAA211250,
 - 1.5V 5A RAA211250,
 - 1.8V 5A RAA211250,
 - 2.5V 5A RAA211250,
 - 3.3V 5A RAA211250.
- *RL78/G12* microcontroller, main controller.
- *RL78/G1C* microcontroller with integrated USB Controller for USB2Serial converter.

- Individual *PG* and *output voltage monitoring*. *PG* transitions high about 1ms after the switching regulator's output voltage reaches the regulation threshold, which is typically 85% of the regulated output voltage.
- Debug feature via *E1 connector*.
- *RAA214401*, 150mA Wide Input Range Ultralow Quiescent Current (3uA) *Linear Regulator* with 3V3 fixed output.
- Possibility of individual adjusting *Soft-Start* and *Compensation* of each regulator by populating the required passive components
- Possibility of modifying the output voltage of each regulator by replacing the *feedback resistors*.

1.2 EU069-3 Power Sequencer Block Diagram

Below the block diagram of the power sequencer is depicted.

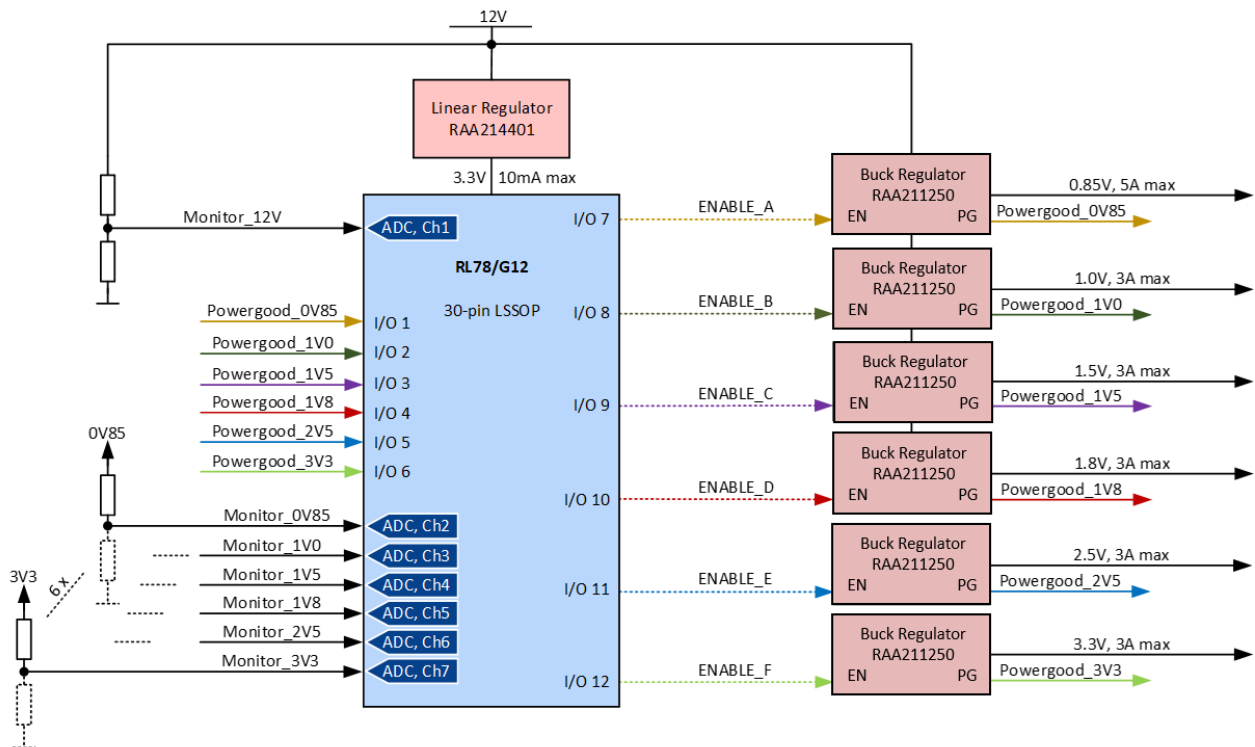


Figure 2. EU096-3 Flexible 6-Ch Power Sequencer for PLCs Block Diagram

2. Schematic components

2.1 Buck Regulator

RAA211250 is a DC/DC synchronous step-down buck regulator. It includes a programmable PWM switching frequency capable of providing a good compromise between transient response and efficiency, and an internal loop compensation circuit to reduce external components count and bill of materials cost. It also offers internal soft-start, power good response, protection features such as cycle-by-cycle peak and valley current limit, thermal shutdown and undervoltage protection on input and output pins.

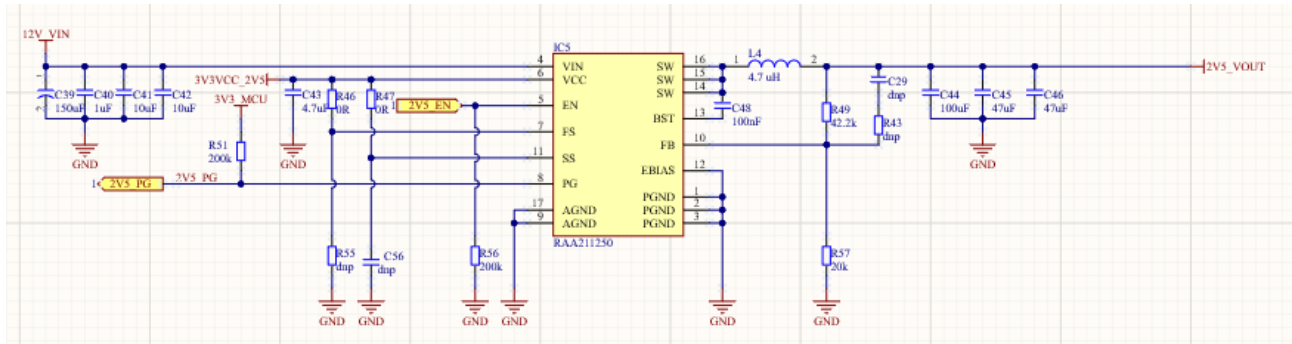


Figure 3. RAA211250 schematic

The small package, a wide range of adjustable output voltage (0.8V to 90% of the V_{IN} output voltage), the possibility to use up to 5A of continuous output current, adjustable frequency and internal compensation makes this IC a good choice for industrial power systems, telecommunication base station power supplies, high-voltage single-board systems or distributed power supplies.

Pins description:

- **EN (Enable input)** regulator is held off when the pin is pulled to ground. The device is enabled when the voltage on this pin rises above 1.3V.
- **FS (Frequency switching)** is used to program the switching frequency from 200kHz to 800kHz when is connected to AGNG through a resistor. The default switching frequency of 400kHz is selected by shorting the pin to power supply input (VCC).
- **SS (Soft Start)** selects the soft-start timing by placing a capacitor from the SS pin to ground. The default 500us soft-start time is available only when the SS pin is shorted to VCC.
- **PG (Power-good, open-drain output)** is asserted when the feedback voltage is within the regulation window and the SS voltage reaches 1.2V. It's recommended the connect it to a voltage source using a pull-up resistor.
- **BST (Bootstrap input)**, a floating bootstrap supply pin for the upper power MOSFET gate driver.
- **FB (Feedback input)**, synchronous buck regulator employs a current mode control loop. FB is the negative input to the voltage loop error amplifier. The output voltage is set by an external resistor divider connected to FB. The output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.8V reference.
- **EBIAS** allows an external bias source connections to the auxiliary internal linear regulator.
- The **AGND** terminal provides the return path for the core analog control circuitry within the device. AGND and **PGND** are connected internally within the device.
- Voltage supply input (**VIN**) represents the main power input for the IC. It is connected to the 12V input.
- **SW** (Phase switch output node) are the main outputs of the device.

- **VCC** (Low dropout linear regulator decoupling pin) is the internally generated 5V supply voltage and is derived from VIN. VIN is between 3V to 5.5V, then VDD is directly connected to VIN to improve efficiency.

Note. The EU096-3 board does not include external discharge circuits for the regulators.

2.2 3.3V Power Regulator

For the 3V3 line used by the RL78 MCU, the RAA214401 150mA Linear Regulator is used.

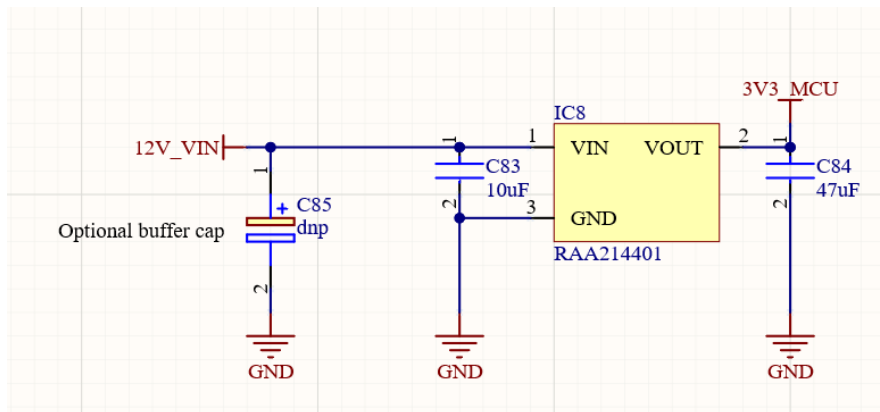


Figure 4. 12V Power supply to 3V3

2.3 Optional input buffer capacitor

The EU096-3 boards also feature an optional, not populated by default, THT buffer capacitor, in case the user requires longer buffer times for the power-down sequence.

2.4 Power timing diagram

The following figure illustrates the common use case for the Power Sequencer.

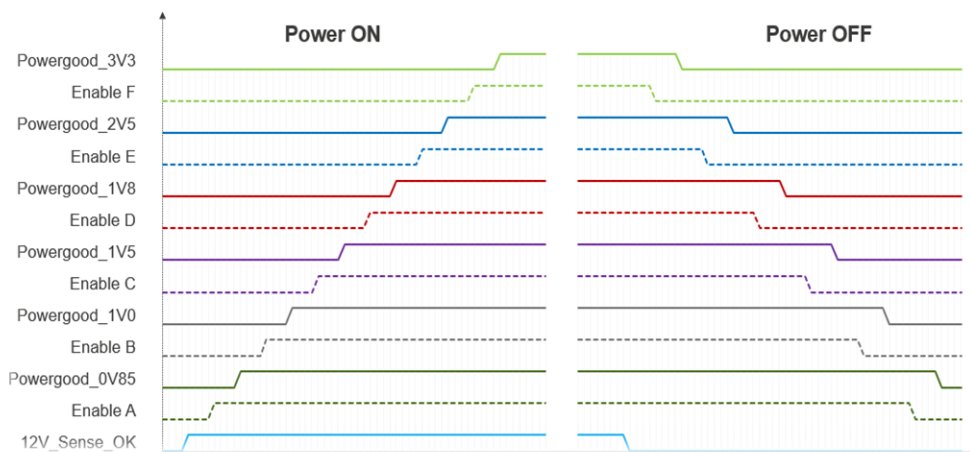


Figure 5. Timing Diagram

2.5 RL78/G1C Microcontroller

The RL78/G1C (part no. R5F10JBCANA) controller has an integrated USB Controller, True Low Power Platform (as low as 112.5 μ A/MHz, and 0.61 μ A for RTC + LVD), 2.4 V to 5.5 V Operation, 32 Kbyte Flash, 31 DMIPS at 24 MHz, for All USB Based Applications.

The RL78/G12 uC represents a true low-power platform (63 μ A/MHz) for the general-purpose applications, with 1.8-V to 5.5-V operation, 2- to 16-Kbyte code flash memory, and 31 DMIPS at 24 MHz.

- Ultra-low power consumption technology,
- RL78 CPU core,
- Code flash memory,
- Data flash memory,
- High-speed on-chip oscillator,
- Power management and reset function,
- DMA (Direct Memory Access) controller,

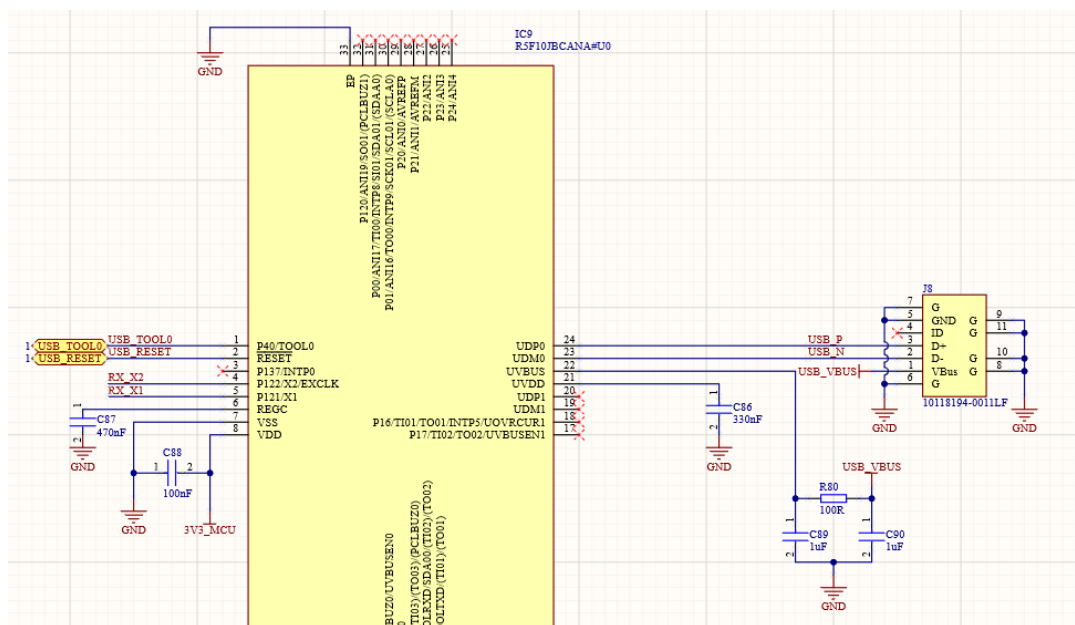


Figure 6. R5F10JBCANA – schematic part 1

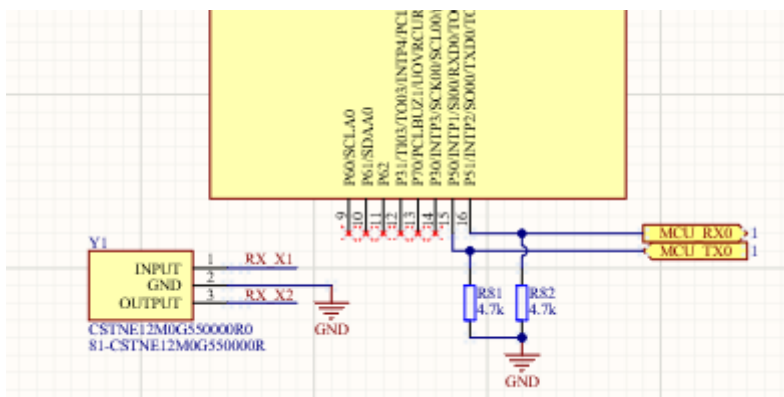


Figure 7. R5F10JBCANA - schematic part 2

3. RL78/G12 Microcontroller

The RL78/G12 uC represents a true low-power platform (63 μ A/MHz) for the general-purpose applications, with 1.8-V to 5.5-V operation, 2- to 16-Kbyte code flash memory, and 31 DMIPS at 24 MHz.

The main features of the uC are:

- Ultra-low power consumption technology,
- RL78 CPU core,
- Code flash memory,
- Data flash memory,
- High-speed on-chip oscillator,
- Power management and reset function,
- DMA (Direct Memory Access) controller,

- Multiplier and divider/multiply-accumulator,
- Serial interface,
- Timer,
- A/D converter,
- I/O port.

The G12 is used to control and monitor each voltage regulator, by reading the input voltage, regulator output voltages, regulator power-good signals and controlling the regulator enable pins.

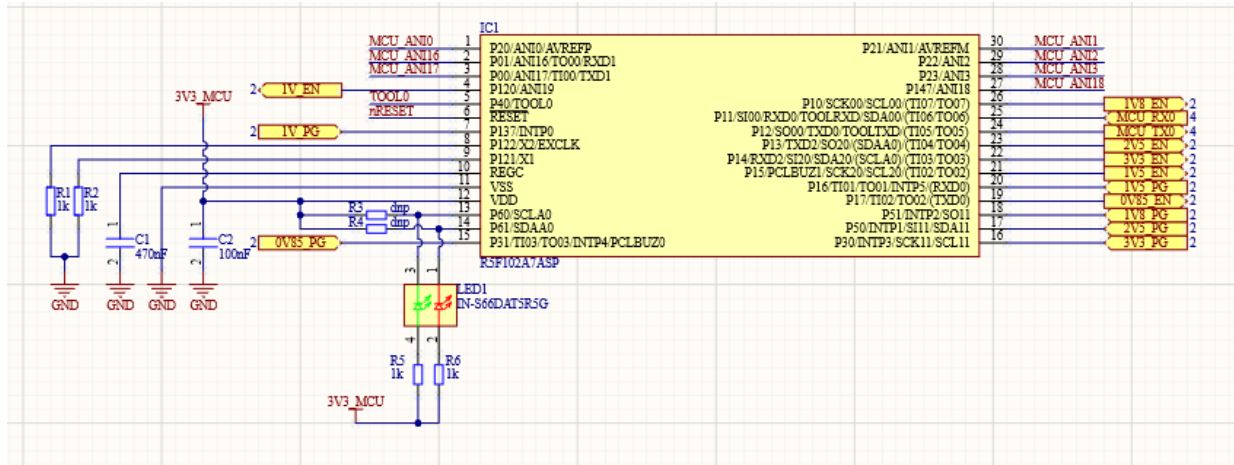


Figure 8. RL78/G12 R5F102A7ASP schematic

3.1 Voltage Monitoring schematic

The regulator output voltages are read through a voltage divider* for the 12V and 3.3V lines (please see the figure below), but the voltage dividers can be adjusted for the rest of the lines in case the output voltage of the regulators is changed.

In the current configuration, the ADC references are uC power supply and ground plane, that means $\pm 7\text{LSB}$ overall error. Translated in voltage, a maximum error between the real voltage and the GUI voltage displayed may be $\pm 25\text{ mV}$ for each ADC channel.

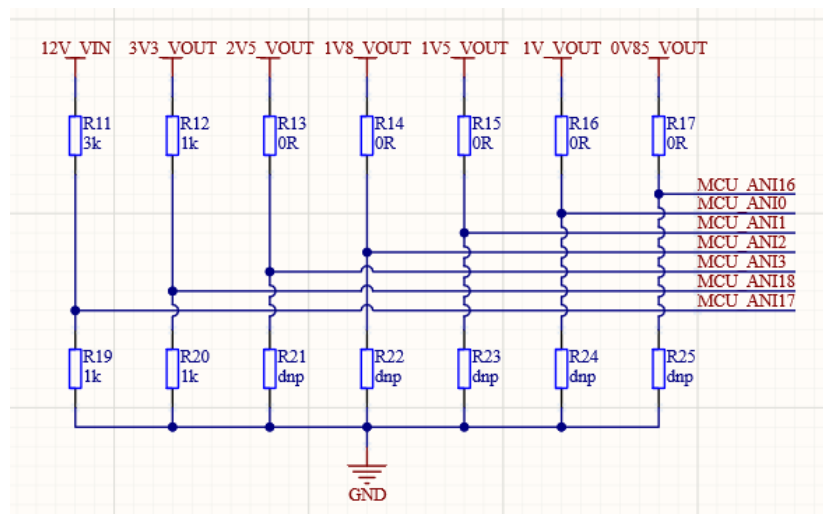


Figure 9. Voltage monitoring schematic

* The resistive tolerance is 5%, that can influence the voltage value from the ADC input channel.

3.2 Microcontroller Pinout

Table 1. Microcontroller Pin Out

Pin	Port	Function
1	P20	ANI0 – (Default)1V Regulator Monitor
2	P01	ANI16 – (Default)0.85V Regulator Monitor
3	P00	ANI17 – (Default)12V Monitor
4	P120	P120 – (Default)1V Regulator Enable
5	P40	TOOL0
6	RESET	RESET
7	P137	INTP0
8	P122	Externally pulled down to GND
9	P121	Externally pulled down to GND
10	REGC	
11	VSS	GND
12	VDD	VDD – Connected to 3.3V Source
13	P60	User LED (Green)
14	P61	User LED (Red)
15	P31	INTP4 – (Default)0V85 Regulator Power Good
16	P30	INTP3 – (Default)3V3 Regulator Power Good
17	P50	INTP1 – (Default)2V5 Regulator Power Good
18	P51	INTP2 – (Default)1V8 Regulator Power Good
19	P17	P17 – (Default)0V85 Regulator Enable
20	P16	INTP5 – (Default)1V5 Regulator Power Good
21	P15	P15 – (Default)1V5 Regulator Enable
22	P14	P14 – (Default)3V3 Regulator Enable
23	P13	P13 – (Default)2V5 Regulator Enable
24	P12	UART TX
25	P11	UART RX
26	P10	P10 – (Default)1V8 Regulator Enable
27	P147	ANI18 – (Default)3V3 Regulator Monitor
28	P23	ANI3 – (Default)2V5 Regulator Monitor
29	P22	ANI2 – (Default)1V8 Regulator Monitor

30	P21	ANI1 – (Default)1V5 Regulator Monitor
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3.3 LEDs and Buttons

The function description of the used LEDs and Buttons are presented in the tables below:

Table 2. LED

LED	Function
LED2(GREEN)	Connected to 0V85 Regulator output
LED3(GREEN)	Connected to 1V Regulator output
LED4(GREEN)	Connected to 1V5 Regulator output
LED5(GREEN)	Connected to 1V8 Regulator output
LED6(GREEN)	Connected to 2V5 Regulator output
LED7(GREEN)	Connected to 3V3 Regulator output
LED1(RED+GREEN)	Connected to P60&P61, User LEDs

Table 3. Switch button

Switch	Function
S1	Switches the E1 Debug connector's TOOL0 and RESET signals between G12 and G1C(USB2Serial) controllers

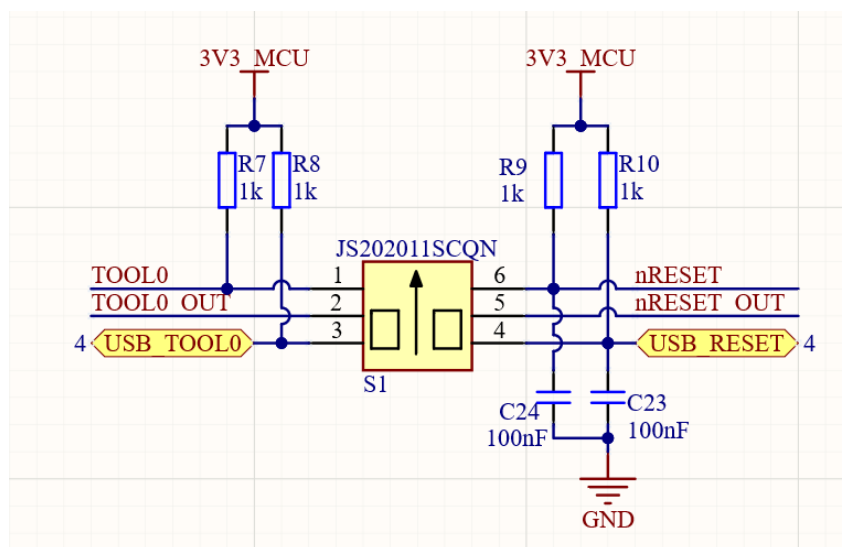


Figure 10. S1 Switch

The S1 switch allows switching the TOOL/RESET debug signals between the RL78/G1C and RL78/G12 controllers while using a single E1 Debug connector.

4. List of Components

Table 4. List of Components

Designator	Comment	Footprint	Quantity
C1, C87	470nF	C0603	2
C2, C88	100nF	C0603	2
C3, C14, C31, C39, C57, C65	150uF	CAPAE660X800N	6
C4, C15, C32, C40, C51, C58, C66	1uF	CAP0603	7
C5, C6, C16, C17, C33, C34, C41, C42, C59, C60, C67, C68	10uF	CAP1210	12
C7, C18, C35, C43, C61, C69	4.7uF	CAP0603	6
C8, C9, C10, C11, C12, C19, C20, C36, C37, C38, C44, C62, C63	100uF	CAP1210	13
C13, C22, C23, C24, C47, C48, C73, C74	100nF	CAP0603	8
C21, C45, C46, C64, C70, C71, C72	47uF	CAP1210	7
C25, C26, C27, C28, C29, C30, C49, C50, C55, C56, C81, C82	dnp	CAP0603	12
C83	10uF	C1210	1
C84	47uF	C1210	1
C85	dnp	CAPPRD500W60D1025H2200	1
C86	330nF	C0603	1
C89, C90	1uF	C0603	2
E1	75869-102LF	SHDR14W62P254_2X7_2499X920X957P	1
IC1	R5F102A7ASP	SOP65P810X140-30N	1
IC2, IC3, IC4, IC5, IC6, IC7	RAA211250	HTSSOP-16	6
IC8	RAA214401	SOOT23	1
IC9	R5F10JBCANA#U0	QFN50P500X500X80-33N-D	1
J1, J2, J3, J4, J5, J6	TB006-508-02BE	TB00650802BE	6
J7	TB006-508-04BE	TB00650804BE	1
J8	10118194-0011LF	101181940011LF	1

L1	1.5 uH	INDPM4040X310N	1
L2, L5	3.3 uH	INDPM4040X310N	2
L3	2 uH	INDPM4040X310N	1
L4	4.7 uH	INDPM4040X310N	1
L6	6 uH	WE-HCI_7030/7040/705023	1
LED1	IN-S66DAT5R5G	INS66DAT5R5G	1
LED2, LED3, LED4, LED5, LED6, LED7	APT1608SGC	LEDC1608X85N	6
Q1, Q2, Q3, Q4, Q5, Q6	2N7002	SOT96P240X120-3N	6
R1, R2, R7, R8, R9, R10, R12, R19, R20	1k	R0603	9
R3, R4, R26, R27, R36, R39, R42, R43, R52, R55, R58, R59, R68, R71	dnp	RES0603	14
R5, R6	1k	RES0603	2
R11	3k	R0603	1
R13, R14, R15, R16, R17	0R	R0603	5
R18	10k	R0603	1
R21, R22, R23, R24, R25	dnp	R0603	5
R28, R29, R31, R32, R44, R45, R46, R47, R60, R61, R62, R63	0R	RES0603	12
R30	1.25k	RES0603	1
R33	24.9k	RES0603	1
R34, R35, R37, R40, R50, R51, R53, R56, R66, R67, R69, R72	200k	RES0603	12
R38, R41, R54, R57, R70, R73	20k	RES0603	6
R48	5k	RES0603	1
R49	42.2k	RES0603	1
R64	17.8k	RES0603	1
R65	62k	RES0603	1
R74, R75, R76, R77, R78, R79	330R	RES0603	6
R80	100R	R0603	1
R81, R82	4.7k	R0603	2
S1	JS202011SCQN	JS202011SCQN	1
Y1	CSTNE12M0G550000R0	CSTNE10M0G55A000R0	1

5. Board Layout

Figure 11 depicts the EU096-3 board layout:

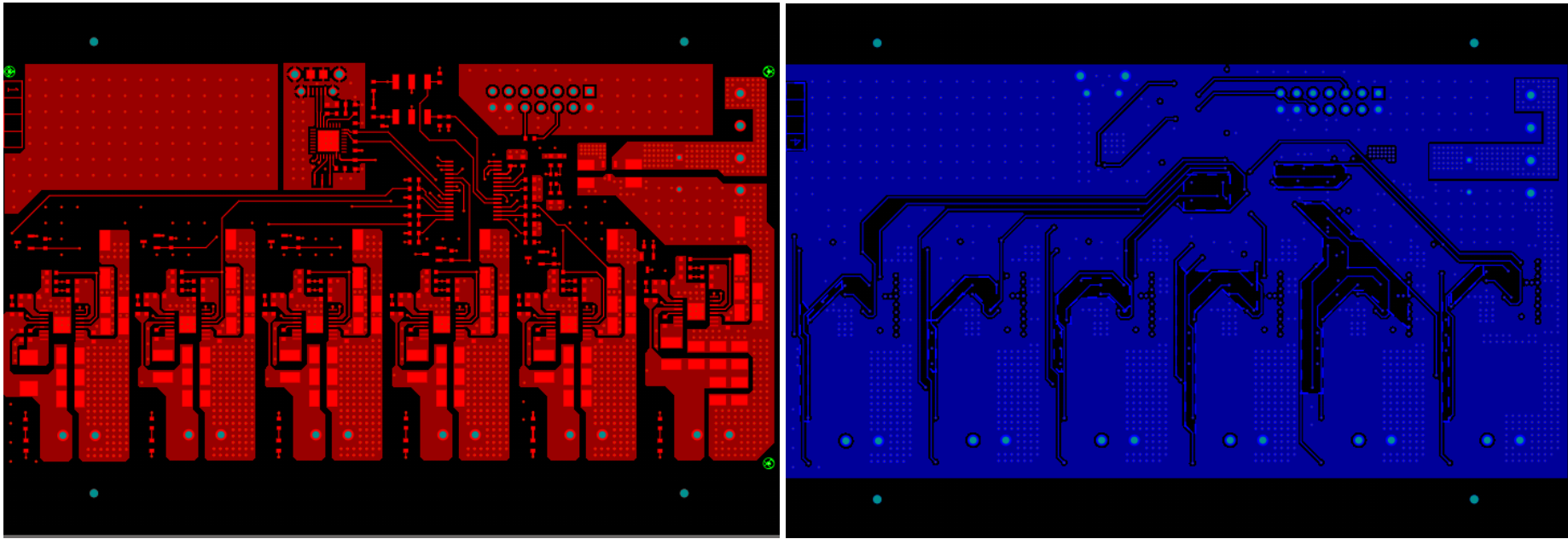


Figure 11. Top layer (left) and bottom layer (right)

6. References

- [1] Renesas Electronics, “EU096 – Software User’s Guide”.
- [2] Renesas Electronics, “EU096-3 – Quick Start Guide”.
- [3] Renesas Electronics, “RL78/G12 - User’s Manual: Hardware” Jun. 2020 - R01DS0193EJ0230
- [4] Renesas Electronics, “RAA211250-Datasheet-20220901_v2.0” Sept 2022 - R16DS0184EU0101

Revision History

Rev.	Date	Description	
		Page	Summary
1.0	05.09.2022		Initial version

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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