IDT™ 89EBPES8T5
Evaluation Board Manual

(Eval Board: 18-613-000)

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Introduction

The 89HPES8T5 switch (also referred to as PES8T5 in this manual) is a member of IDT's PCI Express® standard (PCIe®) based line of products. It is an 8-lane, 5-port switch. One upstream port is provided for connecting to the root complex (RC), and up to four downstream ports are available for connecting to PCIe endpoints or to another switch. More information on this device can be found in the 89HPES8T5 User Manual.

The 89EBPES8T5 Evaluation Board (also referred to as EB8T5 in this manual) provides an evaluation platform for the PES8T5 switch. It is also a cost effective way to add a PCIe downstream port (x1) to an existing system with a limited number of PCIe downstream ports. The EB8T5 eval board is designed to function as an add-on card to be plugged into a x4 PCIe slot available on a motherboard hosting an appropriate root complex, microprocessor(s), and four downstream ports. The EB8T5 is a vehicle to test and evaluate the functionality of the PES8T5 chip. Customers can use this board to get a headstart on software development prior to the arrival of their own hardware. The EB8T5 is also used by IDT to reproduce system-level hardware or software issues reported by customers. Figure 1.1 illustrates the functional block diagram representing the main parts of the EB8T5 board.

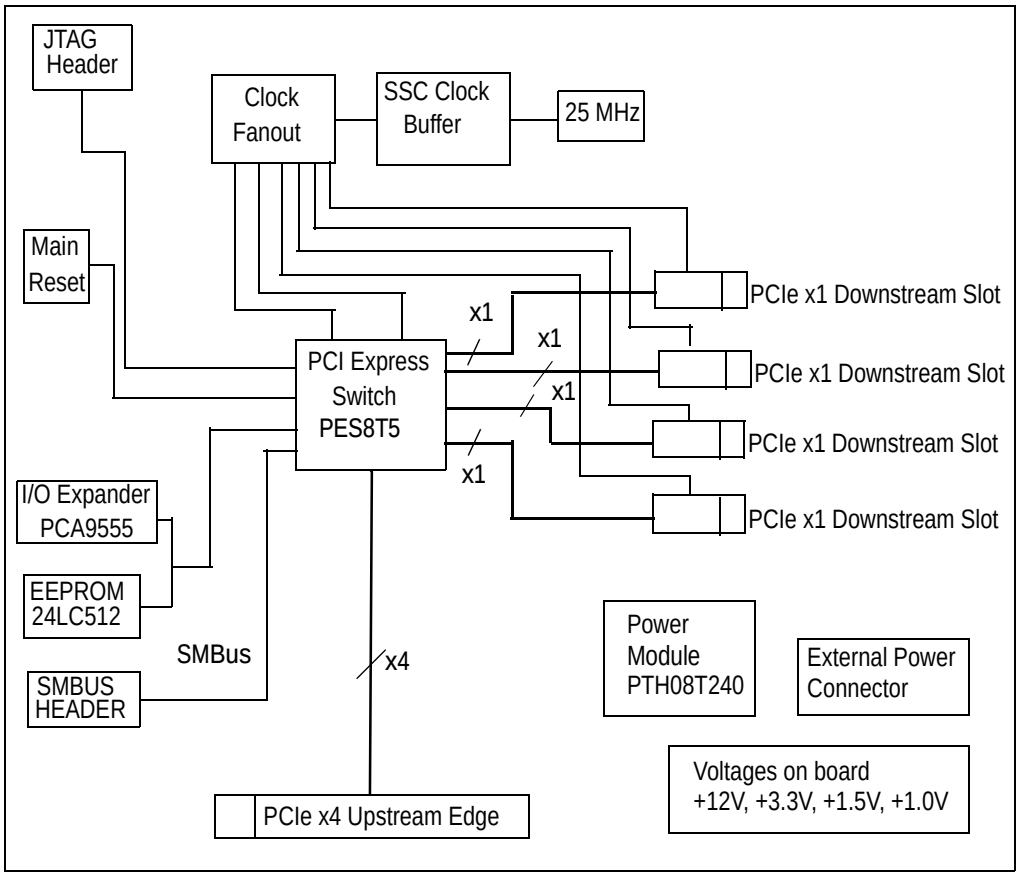


Figure 1.1 Function Block Diagram of the EB8T5 Eval Board

Notes

Board Features

Hardware

- PES8T5 PCIe 5 port switch
  - *Five ports (one x4 port and four x1 ports), 8 PCIe lanes*
  - *PCIe Base Specification Revision 1.1 compliant*
  - *4 GBps (32Gbps) aggregate switching capacity*
  - *Up to 256 byte maximum Payload Size*
  - *Automatic lane reversal and polarity inversion supported on all lanes*
  - *Automatic per port link width negotiation to x4, x2, x1*
  - *Load configuration from an optional serial EEPROM via SMBUS*
- Upstream, Downstream Port
  - *One edge connector on the upstream port, to be plugged into a slot with at least x4 capable on a host motherboard*
  - *Four slot connectors on the downstream ports, for PCIe endpoint add-on cards to be plugged in.*
- Numerous user selectable configurations set using onboard jumpers and DIP-switches
  - *Source of clock - host clock or onboard clock generator*
  - *Two clock rates and spread spectrum settings*
  - *Boot mode selection*
- SMBUS Slave Interface (4 pin header)
- SMBUS Master Interface connected to the Serial EEPROMs through I/O expander
- "Attention" button for each downstream port to initiate a hot swap event on each port
- Four pin connector for optional external power supply
- Push button for Warm Reset
- Several LEDs to display status, reset, power, "Attention", etc.
- One 10-pin JTAG connector (pitch 2.54 mm x 2.54 mm)

Software

There is no software or firmware executed on the board. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the PES8T5 within host systems running popular operating systems.

- Installation programs
  - *Operating Systems Supported: Windows2000, WindowsXP, Linux*
- GUI based application for Windows and Linux
  - *Allows users to view and modify registers in the PES8T5*
  - *Binary file generator for programming the serial EEPROMs attached to the SMBUS.*

Other

- A metal bracket is required to firmly hold in place the four endpoints plugged into the EB8T5 board.
- An external power supply may be required under some conditions.
- SMBUS cable may be required for certain evaluation exercises.
- SMA connectors are provided on the EB8T5 board for specific test points.

Revision History

October 19, 2006: Initial publication of board manual.

November 13, 2006: In Tables 2.7 and 2.8, changed MSMSDDR to MSMBADDR. Removed references to merged ports in Table 2.8.

Installation of the EB8T5 Eval Board

Notes

EB8T5 Installation

This chapter discusses the steps required to configure and install the EB8T5 evaluation board. All available DIP switches and jumper configurations are explained in detail.

The primary installation steps are:

1. Configure jumper/switch options suitable for the evaluation or application requirements.
2. Connect PCI Express endpoint cards to the downstream port PCIe slots on the evaluation board.
3. Insert the evaluation board into the host system (motherboard with root complex chipset).
4. Apply power to the host system.

The EB8T5 board is shipped with all jumpers and switches configured to their default settings. In most cases, the board does not require further modification or setup.

Hardware Description

The PES8T5 is an 8-lane, 5-port PCI Express® switch. It is a peripheral chip that performs PCI Express based switching with a feature set optimized for high performance applications such as servers and storage. It provides fan-out and switching functions between a PCI Express upstream port and 4 downstream ports or peer-to-peer switching between downstream ports.

The EB8T5 has four PCI Express downstream ports, accessible through four x1 connectors.

Basic requirements for the board to run are:

- Host system with a PCI Express root complex supporting x4 configuration through a PCI Express x4 slot. (If your host system does not offer a x4 slot, please contact ssdhelp@idt.com for alternative solutions.)
- x1 PCI Express Endpoint Cards.

Host System

The evaluation board cannot be operated as a standalone unit. A host system implementing a PCI Express root complex supporting x4 configuration through a PCI Express x4 slot is required to take full advantage of the PES8T5's capabilities. One such system is the SuperMicro X6DH8-G2 motherboard equipped with an Intel E7520 chipset which was introduced in 2004 to deploy dual-processor server chipset technology. The board has three PCI Express slots. All slots have x8 connectors, but only two are electronically connected for a x8 link width (J15 and J16). The remaining slots are electronically connected for a x4 link width. Figure 2.1 shows the proper connectors.

Notes

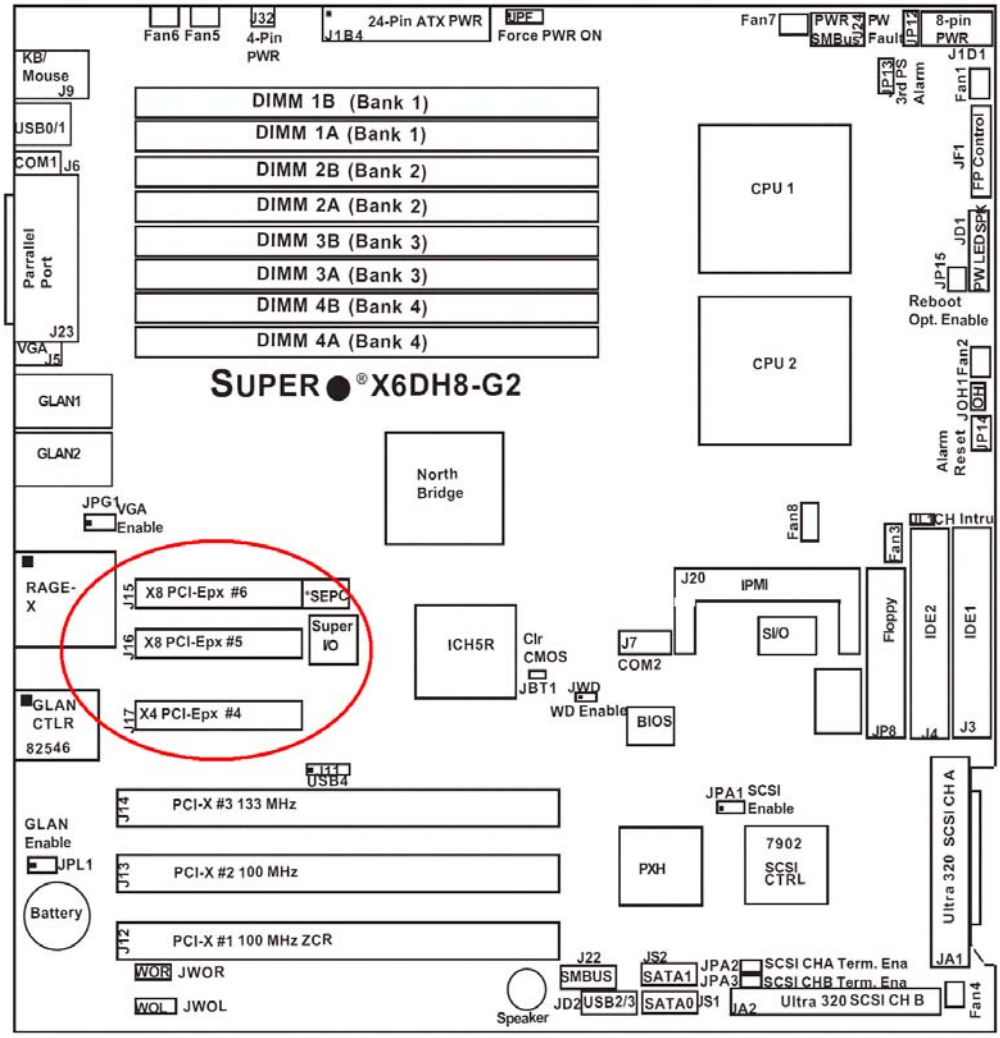


Figure 2.1 SuperMicro X6DH8-G2 Motherboard

Reference Clocks

The PES8T5 requires two differential reference clocks. The EB8T5 derives both of these clocks from a common source which is user-selectable. The common source can be either the host system's reference clock or the onboard clock generator. Selection is made by stuffing resistors described in Table 2.1.

Clock Configuration Stuffing Option	
Install	Clock Source
R36, R37	Onboard Reference Clock – Use onboard clock generator
R34, R35	Upstream Reference Clock – Host system provides clock (Default)

Table 2.1 Clock Source Selection

Notes

The source for the onboard clock is the ICS557-03 clock generator device (U8) connected to a 25MHz oscillator (Y1). When using the onboard clock generator, the EB8T5 allows selection between multiple clock rates and spread spectrum settings via DIP switches as described in Tables 2.2 and 2.3 respectively. Spread Spectrum technology reduces peak EMI emissions by modulating the frequency to spread the peak energy over a wider bandwidth.

Clock Frequency Switch - S2[2:1]		
S2[2]	S2[1]	Clock Frequency
OFF	OFF	Reserved
OFF	ON	125 MHz
ON	OFF	100 MHz (Default)
ON	ON	<Reserved>

Table 2.2 Clock Frequency Selection

Clock Spread Spectrum Switch - S2[4:3]		
S2[4]	S2[3]	Spread%
OFF	OFF	No Spread (Default)
OFF	ON	Down -0.75
ON	OFF	Down -0.50
ON	ON	Center ±0.25

Table 2.3 Clock Spread Spectrum Selection

If the Clock Spread Spectrum is used to modulate data rate, then both ports must use same modulated clock source. Therefore, if your system uses SSC, the on-board clock generator must be disabled and the upstream reference clock should be used instead.

The output of the onboard clock generator is accessible through two SMA connectors located on the Evaluation Board. See Table 2.4. This can be used to connect a scope for probing or capturing purposes and cannot be used to drive the clock from an external source.

Onboard Reference Clock Output (Differential) – J3, J2	
J3	Positive Reference Clock
J2	Negative Reference Clock

Table 2.4 SMA Connectors - Onboard Reference Clock

Power Sources

The EB8T5 and all downstream ports are powered from the upstream port slot power. If add-in cards require more power than the upstream slot can support, an external source is required to supply this extra power via an auxiliary 4-pin power connector on the board. Only downstream ports 2, 3, and 4 can be powered by this external power source through jumpers W45, W46, and W47 (see Table 2.19). Note that on the schematic pages in Chapter 4, port 2 is also referred to as port E, port 3 as port D, port 4 as port C and port 5 as port B.

External Power Source

If necessary, external power is supplied to the EB8T5 board through a 4-pin auxiliary power connector attached to J1. The external power supply provides +12V to the EB8T5 as described in Table 2.5. The +5V is unused.

Notes

Pin	Signal
1	+12V
2	GND
3	GND
4	+5V

Table 2.5 External Power Connector - J1

PCI Express Serial Data Transmit Termination Voltage Converter

A DC-DC converter (U6) provides a 1.5V PCI Express serial data transmit termination voltage (shown as VTTPE or VPETVTT) to the PES8T5.

PCI Express Digital Power Voltage Converter

A separate DC-DC converter (U3) provides a 1.0V PCI Express digital power voltage (VDDPE) to the PES8T5.

PCI Express Analog Power Voltage Converter

A separate DC-DC converter (U7) provides a 1.0V PCI Express analog power voltage (shown as VDDAPE or VDDPEA) to the PES8T5.

Core Logic Voltage Converter

A separate DC-DC converter (U1) provides the 1.0V core voltage (VDDCORE) to the PES8T5.

3.3V I/O Power Module

A 12V to 3.3V power module (U5 or U26) provides the 3.3V I/O voltage (VDDIO) to the PES8T5.

Power-up Sequence

The power-up sequence must be as following:

1. VDDIO - 3.3V
2. VDDCORE, VDDAPE, VDDPE - 1.0V
3. VTTPE - 1.5V

When powering up, each voltage level must ramp up and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations between sequential valid power level requirements. To insure that the sequencing requirements are met, a 0.047µF is used at the SOFTSTART cap on the VTTPE's voltage converter (U6 pin 36) in the EB8T5.

Required Jumpers

To deliver power to the PES8T5 switch, the following jumpers must be shunted: W10, W22-W25. These jumpers were implemented so that the power consumption of the PES8T5 can be measured.

Reset

The PES8T5 supports two types of reset mechanisms as described in the PCI Express specification:

- Fundamental Reset: This is a system-generated reset that propagates along the PCI Express tree through a single side-band signal PERST# which is connected to the Root Complex, the PES8T5, and the endpoints.
- Hot Reset: This is an In-band Reset, communicated downstream via a link from one device to another. Hot Reset may be initiated by software. This is further discussed in the 89HPES8T5 User Manual. The EB8T5 evaluation board provides seamless support for Hot Reset.

Notes

Fundamental Reset

There are two types of Fundamental Resets which may occur on the EB8T5 evaluation board:

- Cold Reset: During initial power-on, the onboard voltage monitor (TLC7733D) will assert the PCI Express Reset (PERSTN) input pin of the PES8T5.
- Warm Reset: This is triggered by hardware while the device is powered on. Warm Reset can be initiated by two methods:
  - Pressing a push-button switch (S1) located on EB8T5 board
  - The host system board IO Controller Hub asserting PERST# signal, which propagates through the PCIe upstream edge connector of the EB8T5. Note that one can bypass the onboard voltage monitor (TLC7733D) by moving the shunt from pin 1-2 to pin 2-3 (default) on W1.

Both events cause the onboard voltage monitor (TLC7733D) to assert the PCI Express Reset (PERSTN) input of the PES8T5 while power is on.

Downstream Reset

The PES8T5 provides a a choice of either a software-controlled reset for each downstream port through GPIO pins or a fundamental reset through PERST#. Selection is made by jumpers described in Table 2.6.

Port #	Jumper	Selection
5	W27	[1-2] Software controlled reset through GPIO10 [2-3] Fundamental reset PERST# (default)
4	W30	[1-2] Software controlled reset through GPIO1 [2-3] Fundamental reset PERST# (default)
3	W35	[1-2] Software controlled reset through GPIO0 [2-3] Fundamental reset PERST# (default)
2	W38	[1-2] Software controlled reset through GPIO9 [2-3] Fundamental reset PERST# (default)

Table 2.6 Downstream Reset Selection

Boot Configuration Vector

A boot configuration vector consisting of the signals listed in Table 2.7 is sampled by the PES8T5 during a fundamental reset (while PERSTN is active). The boot configuration vector defines the essential parameters for switch operation and is set using DIP switches S5 and S6 as defined in Table 2.8.

Signal	Description
CCLKDS	Common Clock Downstream. When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port. Default: 0x1
CCLKUS	Common Clock Upstream. When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port. Default: 0x1
MSMBSMODE	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 kHz. Default: 0x0

Table 2.7 Boot Configuration Vector Signals (Part 1 of 2)

Notes

Signal	Description
RSTHALT	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, the PES8T5 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the P0_SWCTL register through the SMBus. The value may be overridden by modifying the RSTHALT bit in the P0_SWCTL register. Default: 0x0
SWMODE[3:0]	Switch Mode. These configuration pins determine the PES8T5 switch operating mode. Default: 0x1 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM-based initialization 0x2 through 0x4 - Reserved 0x5 - Global SerDes test mode 0x6 - Reserved 0x7 - PLL bypass test mode 0x8 through 0xF - Reserved
REFCLKM	PCI Express Reference Clock Mode Select. This signal selects the frequency of the reference clock input. Default: 0x0 0x0 - 100 MHz 0x1 - 125 MHz
MSMBADDR[2:0]	Master SMBus Address. These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded. Default: 0x0

Table 2.7 Boot Configuration Vector Signals (Part 2 of 2)

Signal	Description	Default
S6[1]	CCLKDS	OFF
S6[2]	CCLKUS	OFF
S6[3]	MSMBSMODE	ON
S6[4]	Not Used	OFF
S6[5]	Not Used	OFF
S6[6]	Not Used	OFF
S6[7]	Not Used	OFF
S6[8]	RSTHALT	ON
S5[1]	SWMODE[0]	OFF
S5[2]	SWMODE[1]	ON
S5[3]	SWMODE[2]	ON
S5[4]	SWMODE[3]	ON
S5[5]	REFCLKM	ON
S5[6]	MSMBADDR[0]	ON
S5[7]	MSMBADDR[1]	ON
S5[8]	MSMBADDR[2]	ON

Table 2.8 Boot Configuration Vector Switches S5 & S6 (ON=0, OFF=1)

Notes

SMBus Interfaces

The System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate. It is based on the principles of operation of I^2C. Implementation of the SMBus signals in the PCI Express connector is optional and may not be present on the host system. The SMBus interface consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins.

The PES8T5 contains two SMBus interfaces: a slave SMBus interface and a master SMBus interface. The slave SMBus interface allows a SMBus Master device (such as the Intel E7520) full access to all software-visible registers. The Master SMBus interface provides connection to the external serial EEPROMs used for initialization and the I/O expander used for hot-plug signals.

SMBus Slave Interface

On the PES8T5 board, the slave SMBus interface is accessible through the PCI Express edge connector as well as a 4-pin header as described in Table 2.9.

Note: The SMBus signals to the PCI Express edge connector is disabled by default. To enable them, place 0-ohm resistors at locations R202 and R203.

.

Slave SMBus Interface Connector J10	
Pin	Signal
1	N/C
2	SCL
3	GND
4	SDA

Table 2.9 Slave SMBus Interface Connector

A fixed slave SMBus address specified by the SSMBADDR[5,3:1] pins is used.

For a fixed address, the SMBus address of the PES8T5 slave interface is 0b1110111 by default and is configurable using jumpers W40, W41, W42, and W43 as described in Tables 2.10 and 2.11.

Slave Interface Address Configuration	
Address Bit	Signal
1	SSMBUSADDR[1]
2	SSMBUSADDR[2]
3	SSMBUSADDR[3]
4	0
5	SSMBUSADDR[5]
6	1
7	1

Table 2.10 SMBus Slave Interface Address Configuration

Notes

SMBUS Slave Interface Address Setting				
W40 SSMBADDR[5]	W41 SSMBADDR[3]	W42 SSMBADDR[2]	W43 SSMBADDR[1]	Slave Interface Bus Address
OFF	OFF	OFF	OFF	0b1110111 (Default)
OFF	OFF	OFF	ON	0b1110110
OFF	OFF	ON	OFF	0b1110101
OFF	OFF	ON	ON	0b1110100
OFF	ON	OFF	OFF	0b1110011
OFF	ON	OFF	ON	0b1110010
OFF	ON	ON	OFF	0b1110001
OFF	ON	ON	ON	0b1110000
ON	OFF	OFF	OFF	0b1100111
ON	OFF	OFF	ON	0b1100110
ON	OFF	ON	OFF	0b1100101
ON	OFF	ON	ON	0b1100100
ON	ON	OFF	OFF	0b1100011
ON	ON	OFF	ON	0b1100010
ON	ON	ON	OFF	0b1100001
ON	ON	ON	ON	0b1100000

Table 2.11 PES8T5 SMBus Slave Interface Address Setting

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. Initiation of any SMBus transaction other than those listed above produces undefined results. See the SMBus 2.0 specification for a detailed description of the following transactions:

- Byte and Word Write/Read
- Block Write/Read

SMBus Master Interface

Connected to the master SMBus interface are four 16-bit I/O Expanders (PCA9555) and a serial EEPROM (24LC512). Four I/O Expanders are used as the interface for the onboard hot-plug controllers (MIC2591B). The lower three bits of the bus address for the I/O Expander are configurable as described in Tables 2.12 through 2.15.

I/O Expander 0			
W4	W7	W11	Bus Address
ON	ON	ON	0b0100000 (Default)
ON	ON	OFF	0b0100001
ON	OFF	ON	0b0100010
ON	OFF	OFF	0b0100011

Table 2.12 I/O Expander 0 Bus Address (Part 1 of 2)

Notes

I/O Expander 0			
W4	W7	W11	Bus Address
OFF	ON	ON	0b0100100
OFF	ON	OFF	0b0100101
OFF	OFF	ON	0b0100110
OFF	OFF	OFF	0b0100111

Table 2.12 I/O Expander 0 Bus Address (Part 2 of 2)

I/O Expander 1			
W2	W5	W8	Bus Address
ON	ON	OFF	0b0100001 (Default)
ON	ON	ON	0b0100000
ON	OFF	ON	0b0100010
ON	OFF	OFF	0b0100011
OFF	ON	ON	0b0100100
OFF	ON	OFF	0b0100101
OFF	OFF	ON	0b0100110
OFF	OFF	OFF	0b0100111

Table 2.13 I/O Expander 1 Bus Address

I/O Expander 2			
W3	W6	W9	Bus Address
ON	OFF	ON	0b0100010 (Default)
ON	ON	ON	0b0100000
ON	ON	OFF	0b0100001
ON	OFF	OFF	0b0100011
OFF	ON	ON	0b0100100
OFF	ON	OFF	0b0100101
OFF	OFF	ON	0b0100110
OFF	OFF	OFF	0b0100111

Table 2.14 I/O Expander 2 Bus Address

Notes

I/O Expander 4			
W31	w44	w29	Bus Address
OFF	ON	ON	0b0100100 (Default)
ON	ON	ON	0b0100000
ON	ON	OFF	0b0100001
ON	OFF	ON	0b0100010
ON	OFF	OFF	0b0100011
OFF	ON	OFF	0b0100101
OFF	OFF	ON	0b0100110
OFF	OFF	OFF	0b0100111

Table 2.15 I/O Expander 4 Bus Address

The bus address for the selected EEPROM device is **0b1000** by default and is configurable using W39 and the switch S5 as described in Table 2.16.

W39	S5[8]	S5[7]	S5[6]	Bus Address
OFF	OFF	OFF	OFF	0b0101 1111
OFF	OFF	OFF	ON	0b0101 1110
OFF	OFF	ON	OFF	0b0101 1101
OFF	OFF	ON	ON	0b0101 1100
OFF	ON	OFF	OFF	0b0101 1011
OFF	ON	OFF	ON	0b0101 1010
OFF	ON	ON	OFF	0b0101 1001
OFF	ON	ON	ON	0b0101 1000
ON	ON	ON	ON	0b0101 0000 (Default)

Table 2.16 EEPROM SMBus Address Setting

JTAG Header

The PES8T5 provides a JTAG connector J4 for access to the PES8T5 JTAG interface. The connector is a 2.54 x 2.54 mm pitch male 10-pin connector. Refer to Table 2.17 for the JTAG Connector J4 pin out.

JTAG Connector J4					
Pin	Signal	Direction	Pin	Signal	Direction
1	/TRST - Test reset	Input	2	GND	—
3	TDI - Test data	Input	4	GND	—

Table 2.17 JTAG Connector Pin Out (Part 1 of 2)

Notes

5	TDO - Test data	Output	6	GND	—
7	TMS - Test mode select	Input	8	GND	—
9	TCK - Test clock	Input	10	GND	—

Table 2.17 JTAG Connector Pin Out (Part 2 of 2)

Attention Buttons

The PES8T5 features four attention buttons, shown in Table 2.18. Each button corresponds to a particular port and is used to initiate hot-swapping events.

Button	Description
S3	Port 5 Attention Button
S4	Port 4 Attention Button
S7	Port 3 Attention Button
S8	Port 2 Attention Button

Table 2.18 Attention Buttons

Miscellaneous Jumpers, Headers

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W45-W47	Header	1-2 Shunted	1-2: 12.0V source from Upstream Port (Default) 2-3: 12.0V source from external power connector
W48-W51	Header	Shunted	Bypass hot-plug controller - Enable REFCLK to downstream ports (Default)
W12	Header	Shunted	Disable EEPROM Write protect feature (Default)
W4, W7, W11 W2, W5, W8 W3, W6, W9 W31, W44, W29	Header	ON, ON, ON ON, ON, OFF ON, OFF, ON OFF, ON, ON	I/O Expander 0 Address[2:0]. Default to 0x0 I/O Expander 1 Address[2:0]. Default to 0x1 I/O Expander 2 Address[2:0]. Default to 0x2 I/O Expander 4 Address[2:0]. Default to 0x4
W13	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Port 5 (Default)
W14	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 4 (Default)
W17	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 3 (Default)
W18	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 2 (Default)
W16	Header	2-3 Shunted	2-3: Port 5, 3.3Vaux source from Upstream port (Default) 1-2: Port 5, 3.3Vaux source from hot-plug controller

Table 2.19 Miscellaneous Jumpers, Headers (Part 1 of 2)

Notes

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W15	Header	2-3 Shunted	2-3: Port 4, 3.3Vaux source from Upstream port (Default) 1-2: Port 4, 3.3Vaux source from hot-plug controller
W20	Header	2-3 Shunted	2-3: Port 3, 3.3Vaux source from Upstream port (Default) 1-2: Port 3, 3.3Vaux source from hot-plug controller
W19	Header	2-3 Shunted	2-3: Port 2, 3.3Vaux source from Upstream port (Default) 1-2: Port 2, 3.3Vaux source from hot-plug controller
W21	Header	2-3 Shunted	2-3: Port 5, +12V source base on W45-W47 (Default) 1-2: Port 5, +12V source from hot-plug controller
W28	Header	2-3 Shunted	2-3: Port 4, +12V source base on W45-W47 (Default) 1-2: Port 4, +12V source from hot-plug controller
W33	Header	2-3 Shunted	2-3: Port 3, +12V source base on W45-W47 (Default) 1-2: Port 3, +12V source from hot-plug controller
W36	Header	2-3 Shunted	2-3: Port 2, +12V source base on W45-W47 (Default) 1-2: Port 2, +12V source from hot-plug controller
W26	Header	2-3 Shunted	2-3: Port 5, +3.3V source from upstream port (Default) 1-2: Port 5, +3.3V source from hot-plug controller
W32	Header	2-3 Shunted	2-3: Port 4, +3.3V source base on W45-W47 (Default) 1-2: Port 4, +3.3V source from hot-plug controller
W34	Header	2-3 Shunted	2-3: Port 3, +3.3V source base on W45-W47 (Default) 1-2: Port 3, +3.3V source from hot-plug controller
W37	Header	2-3 Shunted	2-3: Port 2, +3.3V source base on W45-W47 (Default) 1-2: Port 2, +3.3V source from hot-plug controller

Table 2.19 Miscellaneous Jumpers, Headers (Part 2 of 2)

LEDs

There are several LED indicators on the EB8T5 which convey status feedback. A description of each is provided in Table 2.20.

Location	Color	Definition
DS11	Green	Port 2: Power-is-good indicator
DS 12	Green	Port 3: Power-is-good indicator
DS15	Green	Port 4: Power-is-good indicator
DS14	Green	Port 5: Power-is-good indicator
DS7	Green	Port 2: Power Indicator
DS5	Yellow	Port 2: Attention Indicator
DS10	Green	Port 3: Power Indicator
DS9	Yellow	Port 3: Attention Indicator
DS8	Green	Port 4: Power Indicator
DS6	Yellow	Port 4: Attention Indicator

Table 2.20 LED Indicators (Part 1 of 2)

Notes

Location	Color	Definition
DS4	Green	Port 5: Power Indicator
DS3	Yellow	Port 5: Attention Indicator
DS13	Red	Hot Plug Controller1: Power Fault Indicator
DS16	Red	Hot Plug Controller2: Power Fault Indicator
DS2	Green	Board Power Indicator (3.3V)
DS1	Red	Board Reset Indicator
DS17	Green	Port 2: link up status output
DS18	Green	Port 2: active status output
DS19	Green	Port 3: link up status output
DS20	Green	Port 3: active status output
DS21	Green	Port 4: link up status output
DS22	Green	Port 4: active status output
DS23	Green	Port 5: link up status output
DS24	Green	Port 5: active status output

Table 2.20 LED Indicators (Part 2 of 2)

PCI Express Connectors

Pin	Side A		Side B	
1	+12V	12V power	PRSNT1#	Hot-Plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground

Table 2.21 PCI Express x4 Connector Pinout (Part 1 of 2)

Notes

Pin	Side A		Side B	
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential	RSVD	Reserved
20	PETn1	pair, Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential
22	GND	Ground	PERn1	pair, Lane 1
23	PETp2	Transmitter differential	GND	Ground
24	PETn2	pair, Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential
26	GND	Ground	PERn2	pair, Lane 2
27	PETp3	Transmitter differential	GND	Ground
28	PETn3	pair, Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential
30	RSVD	Reserved	PERn3	pair, Lane 3
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved

Table 2.21 PCI Express x4 Connector Pinout (Part 2 of 2)

Pin	Side A		Side B	
1	+12V	12V power	PRSNT1#	Hot-Plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactiva-tion	PERST#	Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock

Table 2.22 PCI Express x1 Connector Pinout

Notes

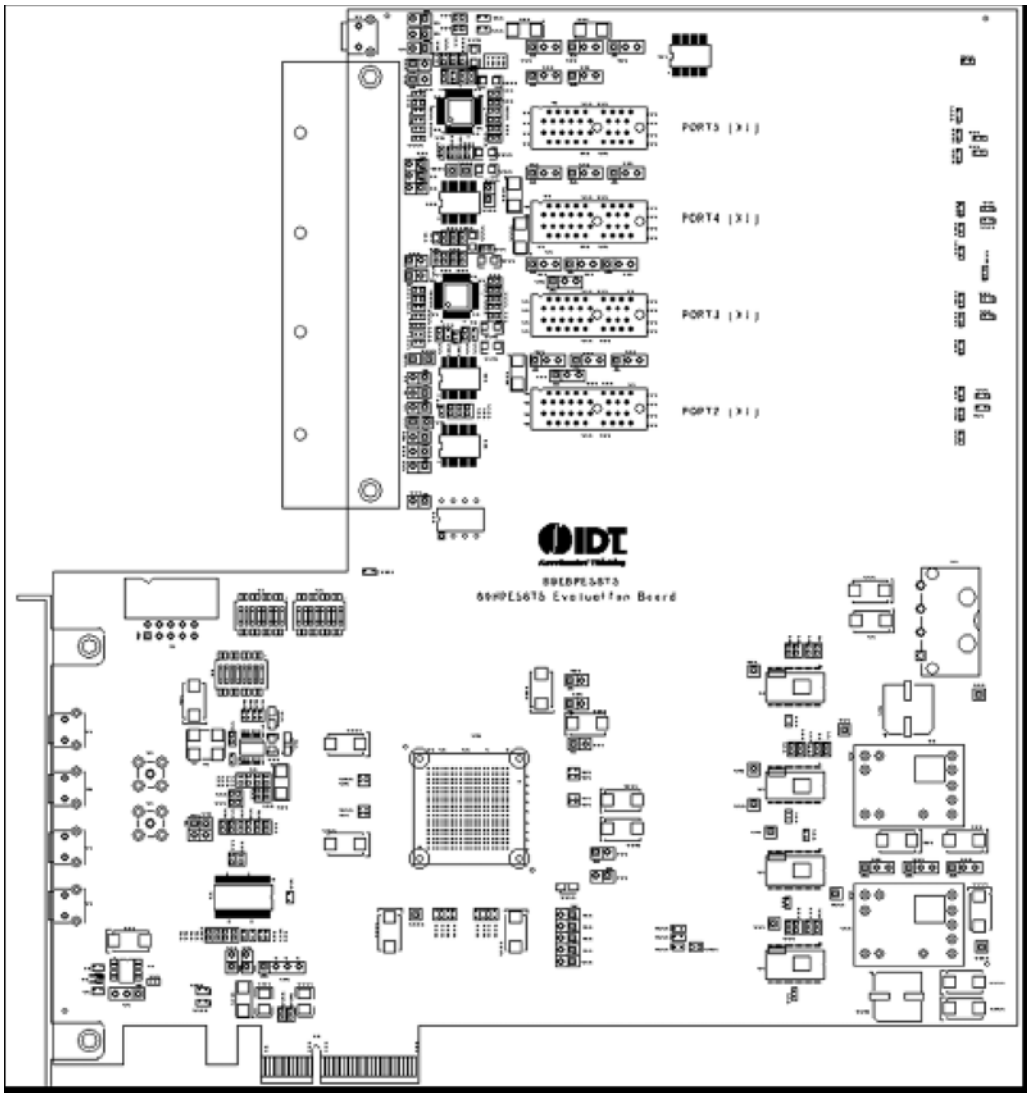
Pin	Side A		Side B	
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground

Table 2.22 PCI Express x1 Connector Pinout

Note: These x4 and x1 PCI Express connectors comply with the PCIe specification. The EB8T5 uses x1 connector on all downstream ports. According to the PCI Express specification, the PRSNT1# pin should be wired to the farthest available PRSNT2# pin on the connector. In the EB8T5, all PRSNT2# pins are tied together. This allows the board to be installed in a x1 or a x4 slot via a slot reducer.

Notes

Locations of Connectors, Jumpers, and Switches



Software for the EB8T5 Eval Board

Notes

Introduction

This chapter discusses some of the main features of the available software to give users a better understanding of what can be achieved with the EB8T5 evaluation board using the device management software.

Device management software and related user documentation are available on a CD which is included in the Evaluation Board Kit. This information is also available on IDT's FTP site. For more information, contact IDT at ssdhelp@idt.com.

Device Management Software

The primary use of the Device Management Software package is to enable users of the evaluation board to access all the registers in the PES8T5 device. This access can be achieved using the PCI Express in-band configuration cycles through the upstream port on the PES8T5.

This software also enables users to save a snapshot of the current register set into a dump file which can be used for debugging purposes. An export/import facility is also available to create and use "Configuration" files which can be used to initialize the switch device with specific values in specific registers.

A conversion utility is also provided to translate a configuration file into an EEPROM programmable data structure. This enables the user to program an appropriate serial EEPROM with desirable register settings for the PES8T5, and then to populate that EEPROM onto the Evaluation Board. It is also possible to program the EEPROM directly on the Evaluation Board using a feature provided by the software package.

The front end of the Device Management Software is a user-friendly Graphical User Interface which allows the user to quickly read or write the registers of interest. The GUI also permits the user to run the software in "simulation" mode with no real hardware attached, allowing the creation of configuration files for the PES8T5 in the absence of the actual device.

Much of the Device Management Software is written with device-independent and OS-independent code. The software will be guaranteed to work on Linux (/sys interface) and MS Windows XP. It may function flawlessly on various flavors of MS Windows, but may not be validated on all. The fact that the software is device-independent assures its scalability to future PCIe parts from IDT. Once users are familiar with the GUI, they will be able to use the same GUI on all PCIe parts from IDT. This software is customized for each device through an XML device description file which includes information on the number of ports, registers, types of registers, information on bit-fields within each register, etc.

Notes

Schematics

Notes

Schematics

RENESAS

REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
STGC-0085R01	1.0	INTIAL RELEASE	2006-07-25	J.CARRILLO

SHEET	DESCRIPTION
1	TABLE OF CONTENTS
2	BLOCK DIAGRAM
3	POWER SUPPLY AND RESET
4	CLOCKS
5	SMBUS, JTAG, I/O EXPANDER
6	HOT PLUG CONTROL PORT B/C
7	HOT PLUG CONTROL PORT D/E
8	PORT B CONN AND 8T5 PORTS
9	PORT C CONNECTOR
10	PORT D CONNECTOR
11	PORT E CONNECTOR
12	PORT A UPSTREAM CONN 8T5
13	PES8T5 - POWER
14	PES8T5 - SMBUS REFCLKS
15	LINK STATUS WAKE

TITLE: 89EBPES8T5 89HPES8T5 EVALUATION BOARD

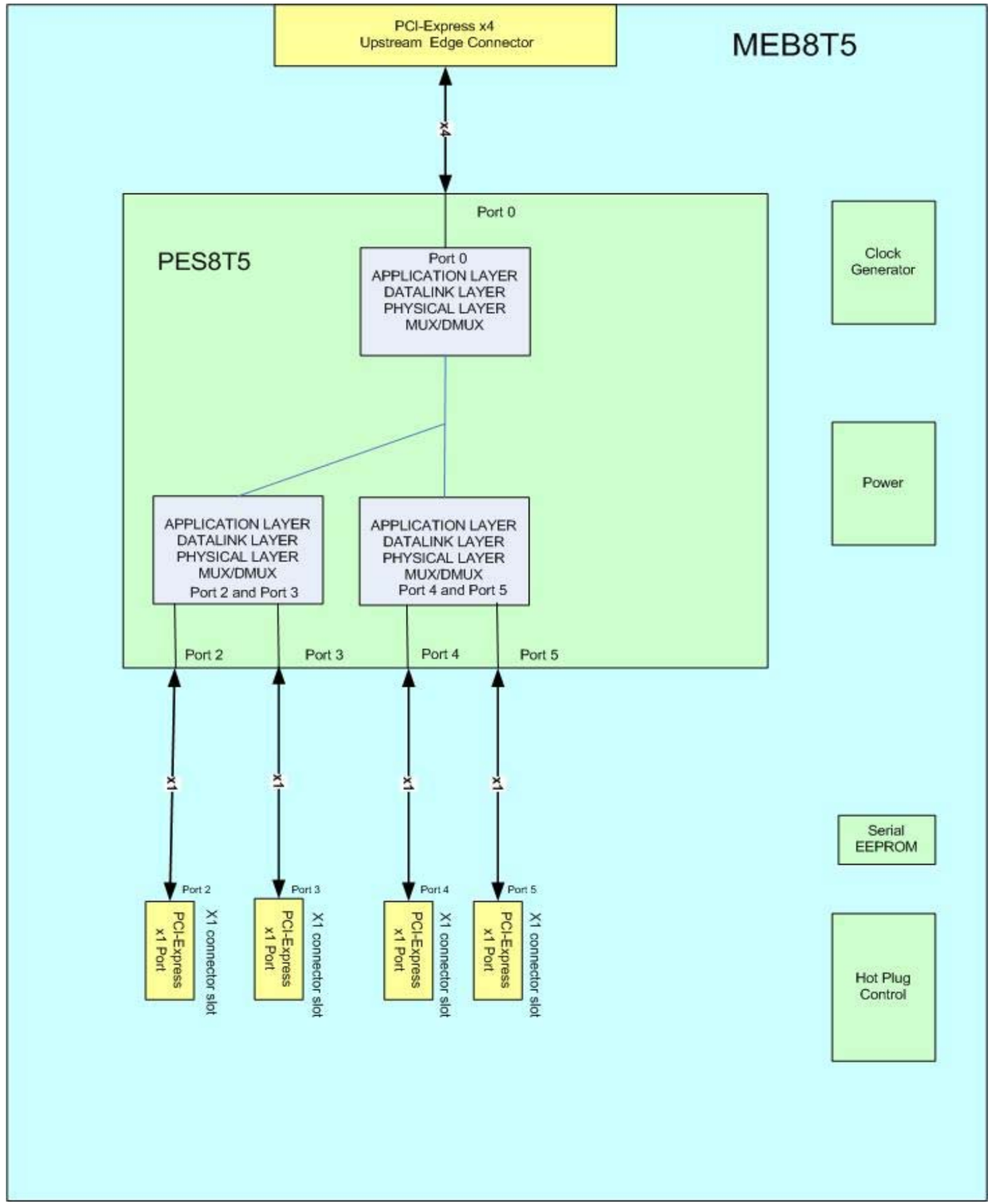
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00086	18-613-000	1.0

AUTHOR	CHECKED BY
J.CARRILLO	B.OH

Wed Nov 08 13:31:58 2006 SHEET 1 OF 15

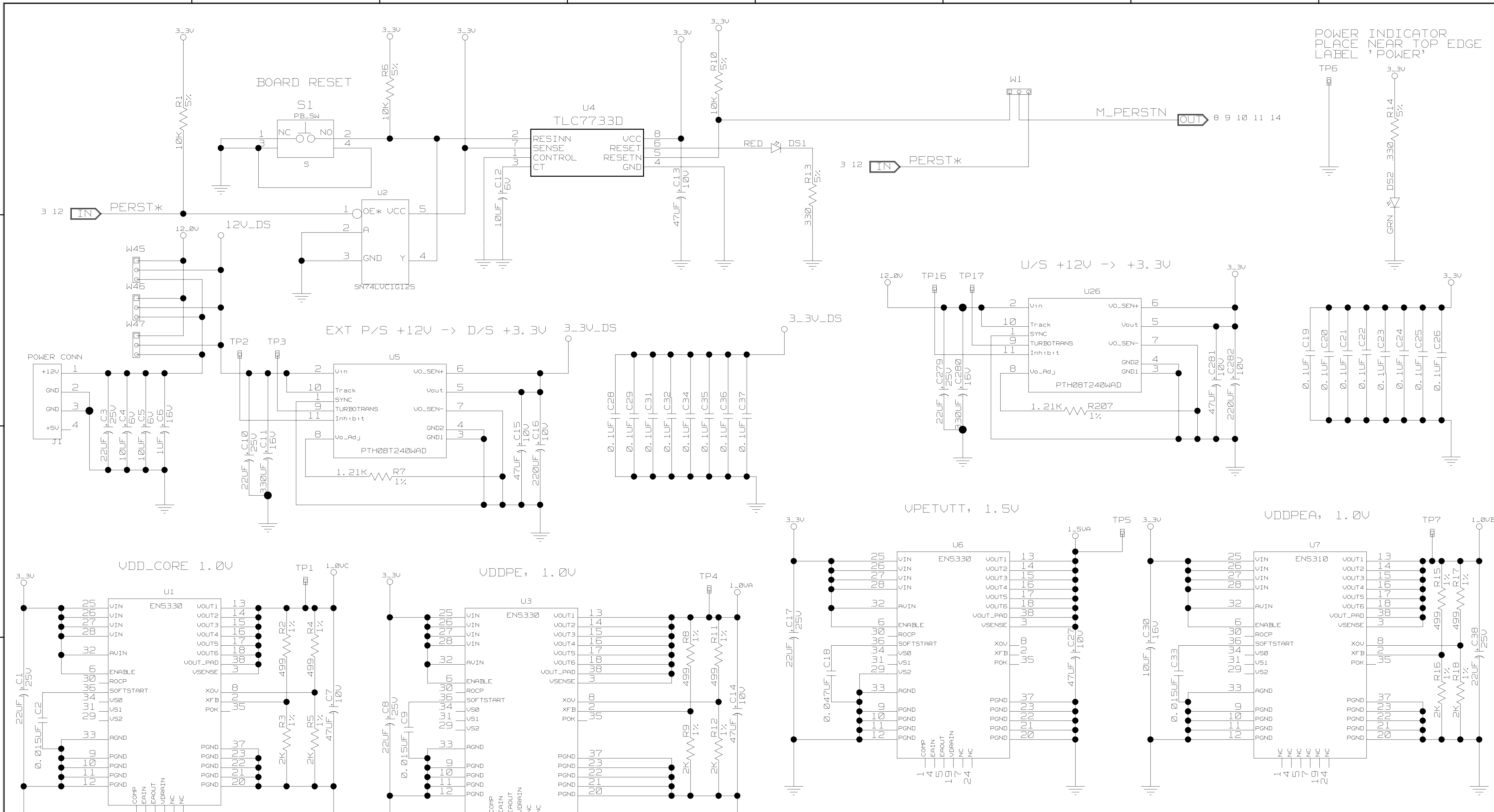
RENESAS

BLOCK DIAGRAM



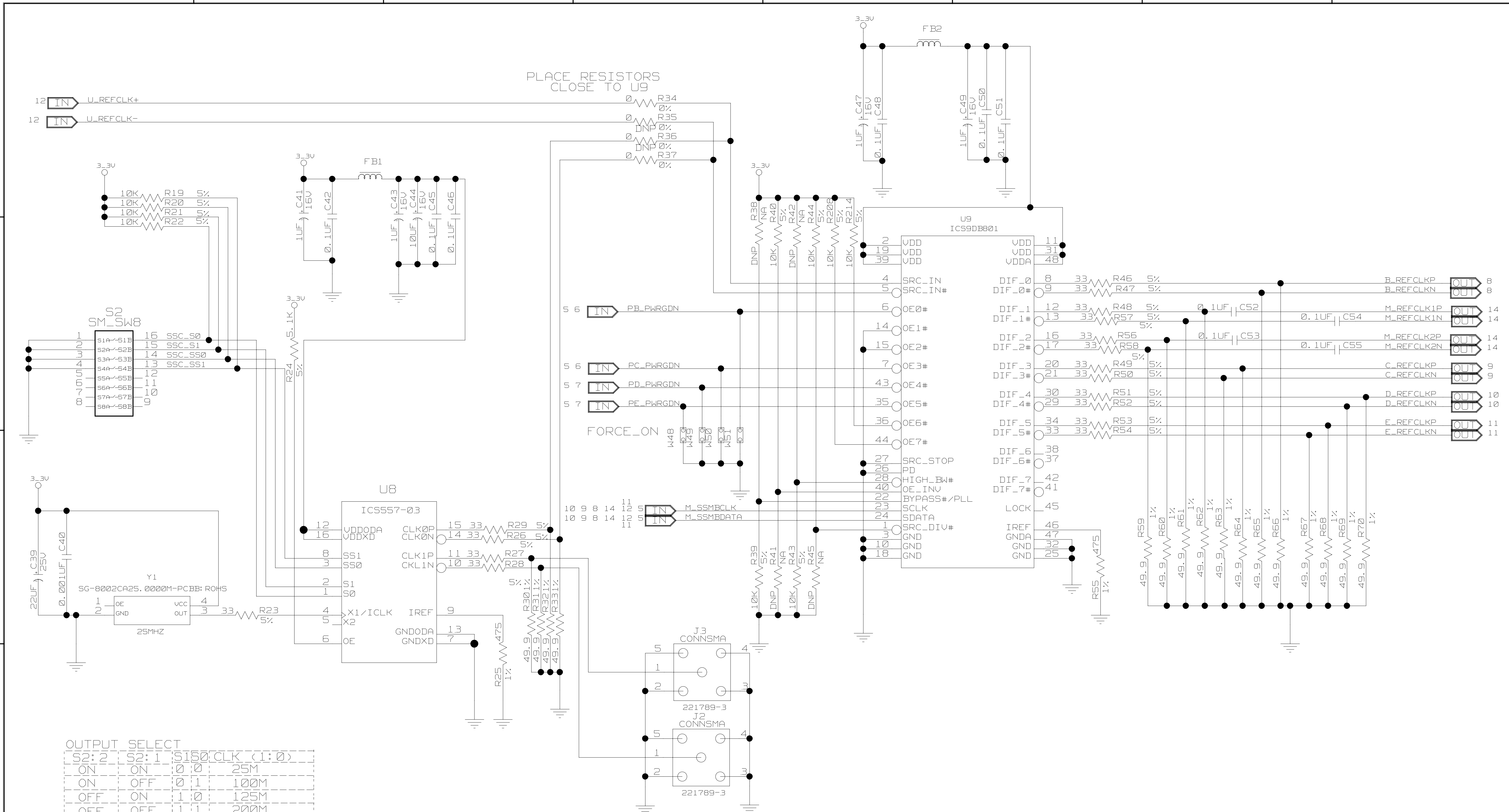
TITLE 89EBPES8T5 BLOCK DIAGRAM			
SIZE B	DRAWING NO. STGSCH-00086	FAB P/N 18-613-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Jul 24 17:25:57 2006		SHEET 2 OF 15	

RENESAS



CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC. 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138 COPYRIGHT (C) IDT 2006	TITLE 89EBPES8T5 POWER SUPPLY AND RESET
SIZE B	DRAWING NO. STGSCH-00086
FAB P/N 18-613-000	REV. 1.0
AUTHOR J. CARRILLO	CHECKED BY B. OH
Wed Nov 08 17:34:40 2006	SHEET 3 OF 15

RENESAS


PLACE RESISTORS
CLOSE TO U9
U_REFCLK+
U_REFCLK-
R34 0 0%
R35 0 DNP 0%
R36 0 DNP 0%
R37 0 0%
3_3V
R19 10K 5%
R20 10K 5%
R21 10K 5%
R22 10K 5%
FB1
C41 1UF 16V
C42 0.1UF
C43 1UF 16V
C44 10UF 16V
C45 0.1UF
C46 0.1UF
S2
SM_SW8
SSC_S0
SSC_S1
SSC_SS0
SSC_SS1
R24 5.1K 5%
FB2
C47 1UF 16V
C48 0.1UF
C49 1UF 16V
C50 0.1UF
C51 0.1UF
R38 NA DNP
R40 5% 10K
R42 NA DNP
R44 5% 10K
R208 5% 10K
R214 5% 10K
U9
ICS9DB801
VDD
VDDA
SRC_IN
SRC_IN#
OE0#
OE1#
OE2#
OE3#
OE4#
OE5#
OE6#
OE7#
SRC_STOP
PD
HIGH_BW#
OE_INV
BYPASS#/PLL
SCLK
SDATA
SRC_DIV#
GND
DIF_0
DIF_0#
DIF_1
DIF_1#
DIF_2
DIF_2#
DIF_3
DIF_3#
DIF_4
DIF_4#
DIF_5
DIF_5#
DIF_6
DIF_6#
DIF_7
DIF_7#
LOCK
IREF
GNDA
PB_PWRGDN
PC_PWRGDN
PD_PWRGDN
PE_PWRGDN
FORCE_ON
W48 W49 W50 W51
M_SSMBCLK
M_SSMBDATA
R46 33 5%
R47 33 5%
R48 33 5%
R57 33 5%
R56 33
R58 33 5%
R49 33 5%
R50 33 5%
R51 33 5%
R52 33 5%
R53 33 5%
R54 33 5%
C52 0.1UF
C53 0.1UF
C54 0.1UF
C55 0.1UF
B_REFCLKP
B_REFCLKN
M_REFCLK1P
M_REFCLK1N
M_REFCLK2P
M_REFCLK2N
C_REFCLKP
C_REFCLKN
D_REFCLKP
D_REFCLKN
E_REFCLKP
E_REFCLKN
R59 R60 R61 R62 R63 R64 R65 R66 R67 R68 R69 R70 49.9 1%
R55 475 1%
U8
ICS557-03
VDDODA
VDDXD
SS1
SS0
S1
S0
X1/ICLK
X2
OE
CLK0P
CLK0N
CLK1P
CKL1N
IREF
GNDODA
GNDXD
R29 33 5%
R26 33 5%
R27 33
R28 33
R301 R311 R321 R331 49.9 1%
R25 475 1%
R39 5% 10K
R41 NA DNP
R43 5% 10K
R45 NA DNP
J3 CONNSMA 221789-3
J2 CONNSMA 221789-3
Y1
SG-8002CA25.0000M-PCBB:ROHS
25MHZ
OE GND VCC OUT
R23 33 5%
C39 22UF 25V
C40 0.001UF

OUTPUT SELECT

S2:2	S2:1	S1	S0	CLK (1:0)
ON	ON	0	0	25M
ON	OFF	0	1	100M
OFF	ON	1	0	125M
OFF	OFF	1	1	200M

SPREAD SELECTION

S2:4	S2:3	SS1	SS0	SPREAD %
ON	ON	0	0	CENTER +-0.25
ON	OFF	0	1	DOWN -0.5
OFF	ON	1	0	DOWN -0.75
OFF	OFF	1	1	NO SPREAD

IDT™

TITLE 89EBPES8T5			
CLOCKS			
SIZE B	DRAWING NO. STGSCH-00086	FAB P/N 18-613-000	REV. 1.0
AUTHOR J.CARRILLO		CHECKED BY B.OH	
Wed Nov 08 17:34:41 2006		SHEET 4 OF 15	

RENESAS

IO EXPANDER 0

IO EXPANDER 1

IO EXPANDER 2

PLACE EEPROM ON SOCKET

EEPROM U13 24LC512

52-298-000

NOTE: CONNECTION FROM W12 TO U13-7 IS NOT IN FAB (ECN# PCBECN-00233)

JTAG HEADER

SMBUS HEADER TO UPSTREAM DEVICE

S3 PB_SW PORT B ATTN

S4 PB_SW PORT C ATTN

S7 PB_SW PORT D ATTN

S8 PB_SW PORT E ATTN

S5 SM_SW8

S6 SM_SW8

TITLE	89EBPES8T5
	SMBUS, JTAG, IO EXPANDER
SIZE	B
DRAWING NO.	STGSCH-00086
FAB P/N	18-613-000
REV.	1.0
AUTHOR	J. CARRILLO
CHECKED BY	B. OH
	Wed Nov 08 17:34:42 2006
	SHEET 5 OF 15

RENESAS

U14
MIC2591B

FORCE ON

PB_PWRGDN
PC_PWRGDN
PB_PRSNT
PC_PRSNT
PBC_INTN

B_PCIE_3_3AUX
B_PCIE_12V
B_PCIE_3_3V
C_PCIE_12V
C_PCIE_3_3V
C_PCIE_3_3AUX

Q5 PMOSFET
Q2 NMOSFET
Q6 PMOSFET
Q1 NMOSFET

3_3V_DS
12V_DS

TITLE 89EBPES8T5

HOT PLUG CONTROL PORT B/C

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00086	18-613-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO	B. OH

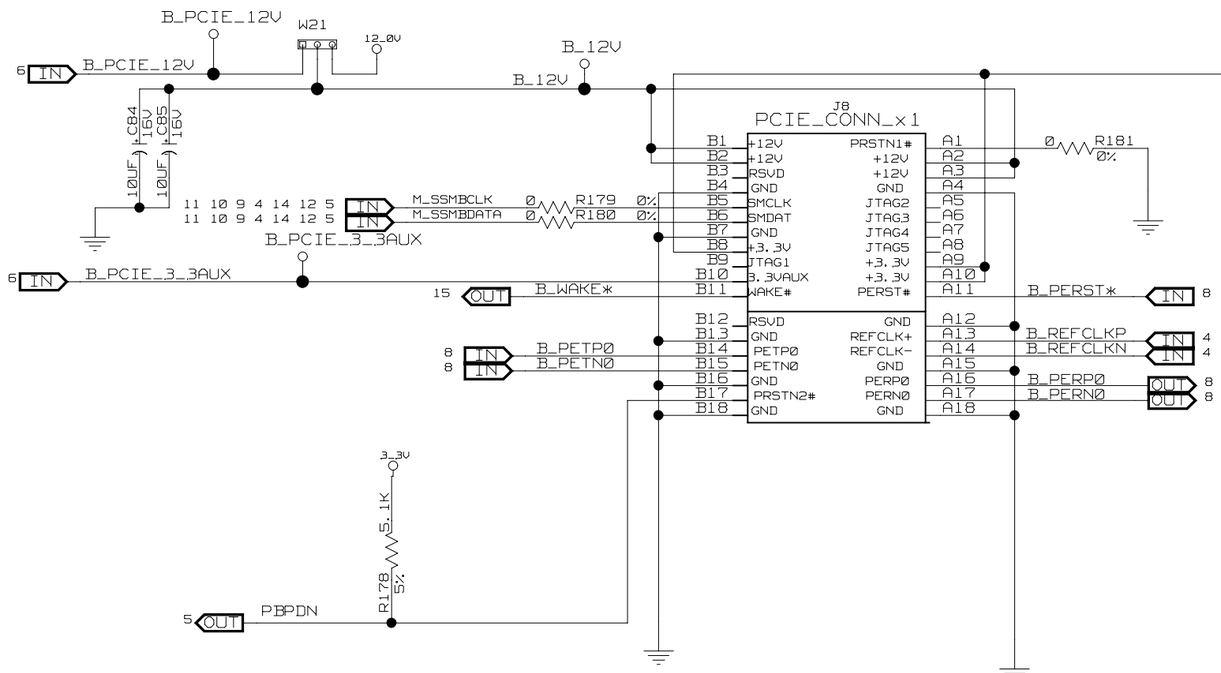
Wed Nov 08 17:34:42 2006 — SHEET 6 OF 15

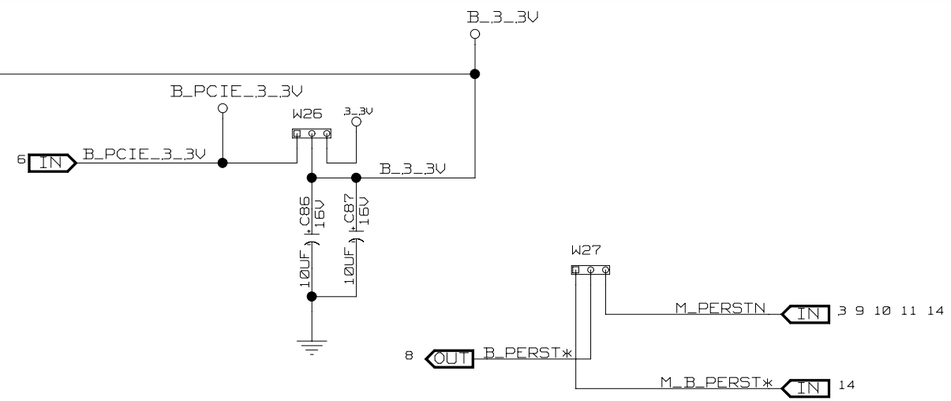
RENESAS

U17
MIC2591B

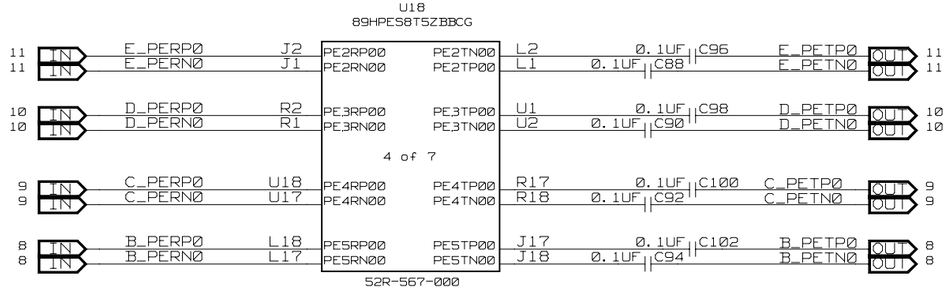
Q7 PMOSFET
Q4 NMOSFET
Q8 PMOSFET
Q3 NMOSFET

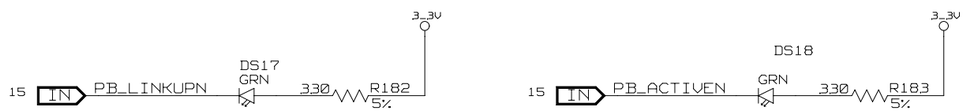
TITLE	89EBPES8T5
	HOT PLUG CONTROL PORT D/E
SIZE	B
DRAWING NO.	STGSCH-00086
FAB P/N	18-613-000
REV.	1.0
AUTHOR	J. CARRILLO
CHECKED BY	B. OH
	Wed Nov 08 17:34:43 2006
	SHEET 7 OF 15





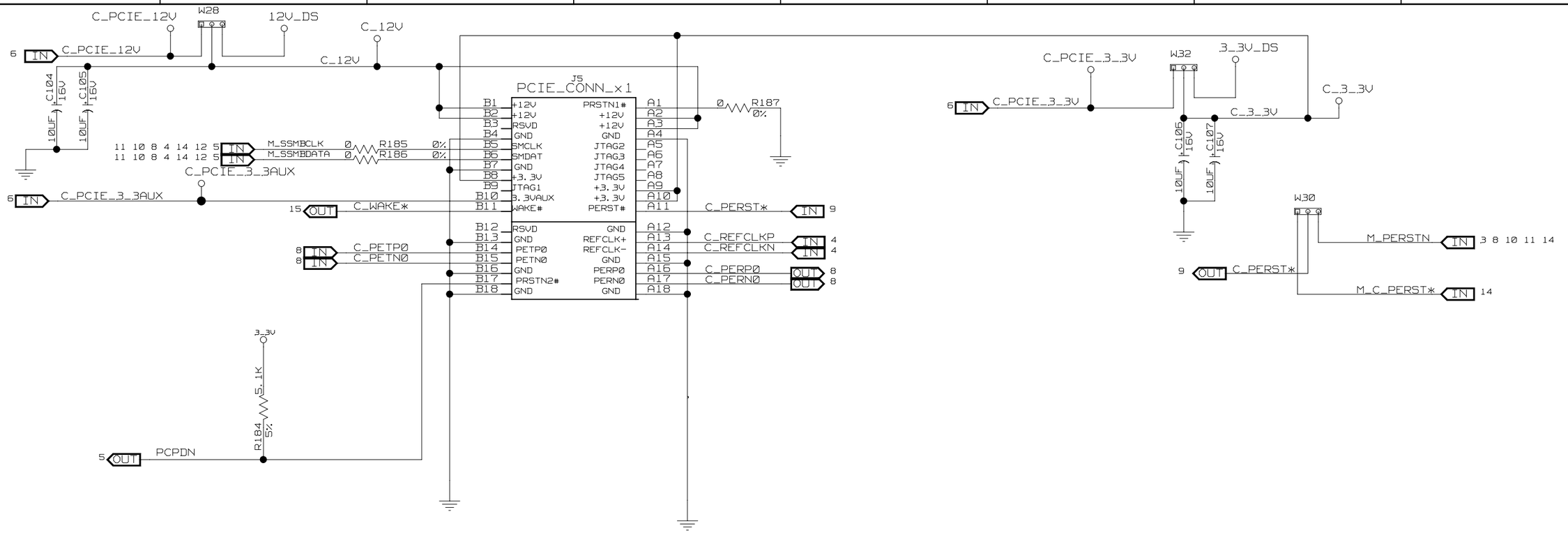
NOTE: POLARITY REVERSAL OF PE2T00
WILL BE CORRECTED ON RE-SPIN





DOWNSTREAM (PORT B) CONNECTOR

TITLE 89EBPES8T5 PORT B CONN AND 8T5 PORTS			
SIZE B	DRAWING NO. STGSCH-00086	FAB P/N 18-613-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Wed Nov 08 17:34:44 2006		SHEET 8 OF 15	



DOWNSTREAM (PORT C) CONNECTOR

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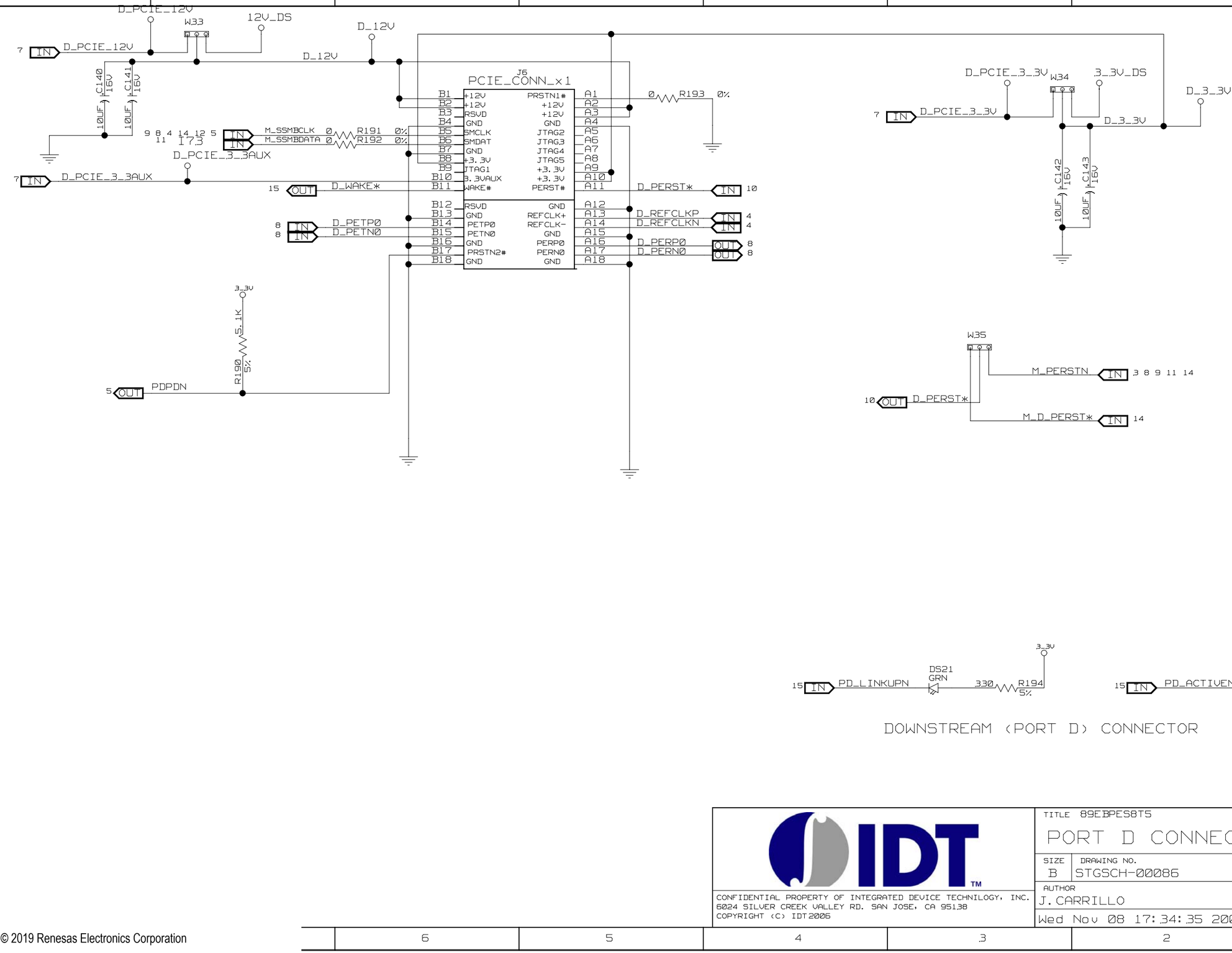
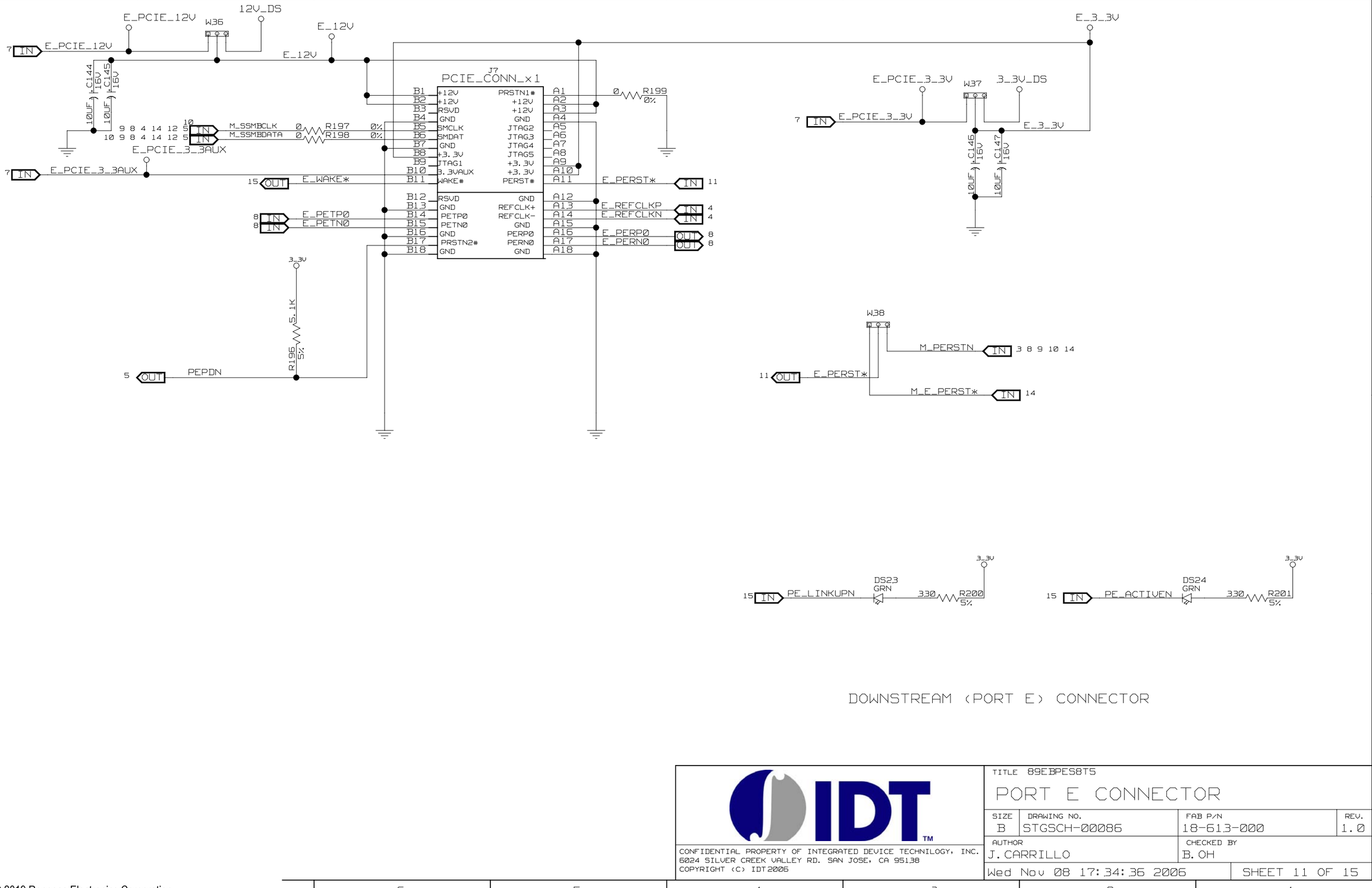
TITLE 89EBPES8T5 PORT C CONNECTOR			
SIZE B	DRAWING NO. STGSCH-00086	FAB P/N 18-613-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Wed Nov 08 17:34:44 2006		SHEET 9 OF 15	



DOWNSTREAM (PORT D) CONNECTOR

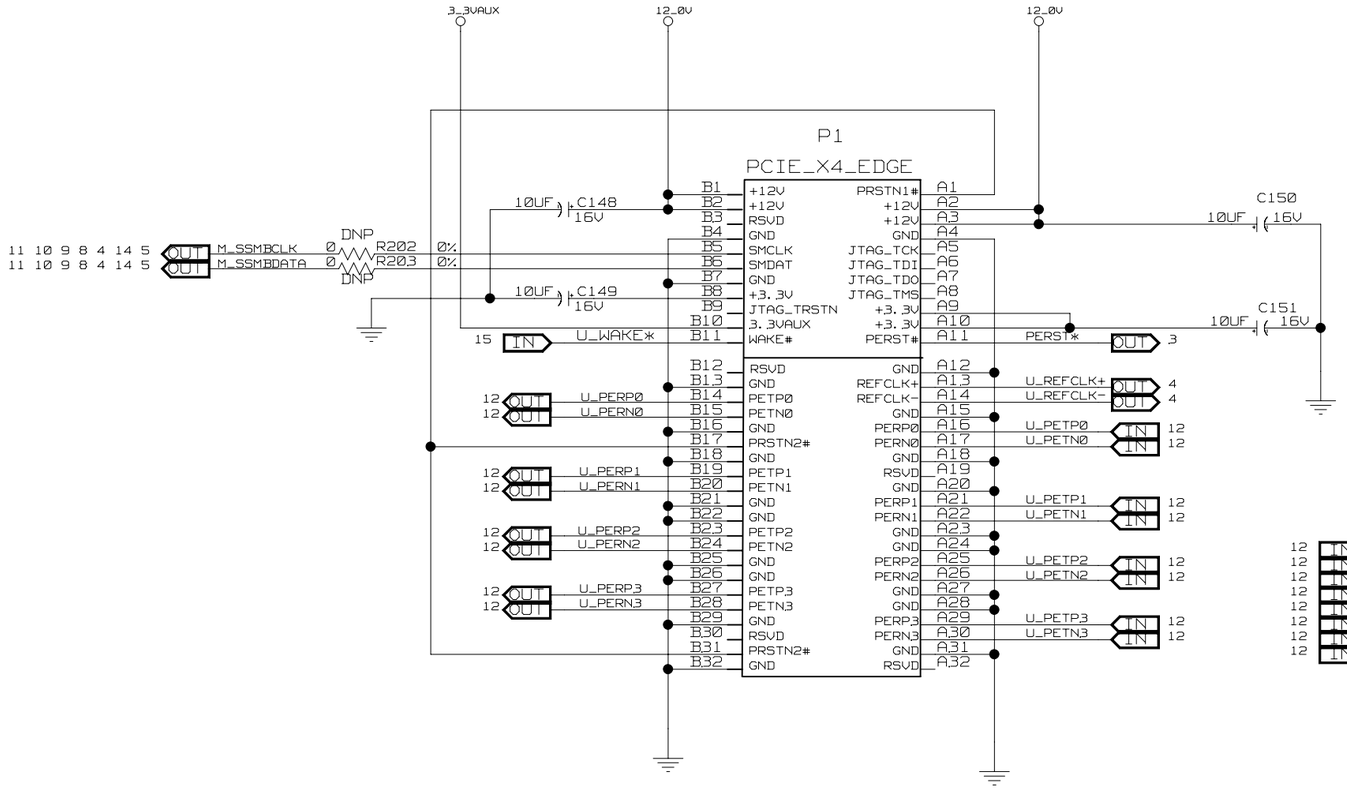
TITLE	89EBPES8T5
	PORT D CONNECTOR
SIZE	B
DRAWING NO.	STGSCH-00086
FAB P/N	18-613-000
REV.	1.0
AUTHOR	J. CARRILLO
CHECKED BY	B. OH
	Wed Nov 08 17:34:35 2006
	SHEET 10 OF 15

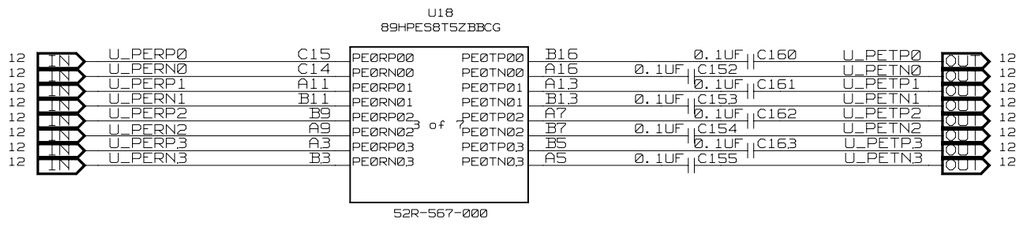


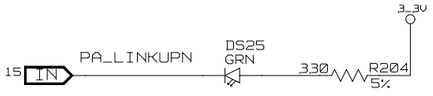
DOWNSTREAM (PORT E) CONNECTOR

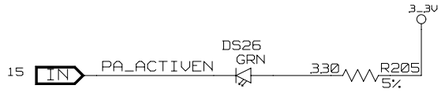
TITLE 89EBPES8T5 PORT E CONNECTOR			
SIZE B	DRAWING NO. STGSCH-00086	FAB P/N 18-613-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Wed Nov 08 17:34:36 2006		SHEET 11 OF 15	

RENESAS









PORT A UPSTREAM (EDGE) CONNECTOR

TITLE 89EBPES8T5			
PORT A UPSTREAM CONN 8T5			
SIZE B	DRAWING NO. STGSCH-00086	FAB P/N 18-613-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Wed Nov 08 17:34:37 2006		SHEET 12 OF 15	

RENESAS

JUMPERS MUST BE POPULATED FOR NORMAL OPERATION

VTT 1_5VA W23

VDDPE_J 1_0VA W22

3_3V_J 3_3V W10

VDDCORE_J 1_0VC W25

1_0VB W24

VDDPEA

1UF C170 16V

1UF C212 16V

1UF C214 16V

1UF C246 16V

0.1UF C171 C172 C173 C174 C175 C176 C177 C178 C179 C180 C181 C182 C183 C184 C185 C186

0.1UF C191 C192 C193 C194 C195 C196 C197 C198 C199 C200 C201 C202 C203 C204 C205 C206 C207 C208 C209 C210 C211

0.1UF C215 C216 C217 C218 C219 C220

0.1UF C221 C222 C223 C224 C225 C226 C227 C228 C229 C230 C231 C232

0.1UF C247 C248 C249 C250 C251 C252 C253 C254 C255 C256 C257 C258 C259 C260 C261 C262 C263 C264 C265 C266 C267 C268 C269 C270

47UF C169 10V

47UF C158 10V

47UF C189 10V

47UF C190 10V

47UF C243 10V

47UF C244 10V

FB3 FB4 FB5

1UF C187 16V

0.1UF C188

1UF C213 16V

0.1UF C233 C234 C235 C236 C237 C238 C239 C240 C241 C242 C245 C271 C272 C273 C274 C275 C276

47UF C277 10V

47UF C278 10V

U18
89HPES8T5ZBBCG
52R-567-000

D6	VDDAPE1	VDDPE1	E6
D8	VDDAPE2	VDDPE2	E8
D10	VDDAPE3	VDDPE3	E10
D12	VDDAPE4	VDDPE4	E12
N4	VDDAPE5	VDDPE5	K4
N15	VDDAPE6	VDDPE6	K15
P4	VDDAPE7	VDDPE7	L4
P15	VDDAPE8	VDDPE8	L15
R4	VDDAPE9	VDDPE9	M4
T3	VDDAPE10	VDDPE10	M15
T8	VDDAPE11	VDDPE11	P3
T10	VDDAPE12	VDDPE12	P16
T16	VDDAPE13	VDDPE13	R3
U15	VDDAPE14	VDDPE14	R6
		VDDPE15	R8
		VDDPE16	R10
		VDDPE17	R12
		VDDPE18	R16
		VDDPE19	U3
		VDDPE20	U16

1 of 7

U18
89HPES8T5ZBBCG
52R-567-000

A4	VDDCORE1	VDDIO1	B1
A6	VDDCORE2	VDDIO2	B2
A8	VDDCORE3	VDDIO3	C17
A10	VDDCORE4	VDDIO4	C18
A12	VDDCORE5	VDDIO5	G5
A14	VDDCORE6	VDDIO6	G10
A15	VDDCORE7	VDDIO7	G14
B17	VDDCORE8	VDDIO8	H5
B18	VDDCORE9	VDDIO9	H14
C4	VDDCORE10	VDDIO10	J5
C13	VDDCORE11	VDDIO11	J14
C16	VDDCORE12	VDDIO12	P9
D4	VDDCORE13	VDDIO13	P13
D14	VDDCORE14	VDDIO14	R5
D15	VDDCORE15	VDDIO15	R13
E5	VDDCORE16	VDDIO16	T14
E14	VDDCORE17		
F4	VDDCORE18	VTT1	C6
F6	VDDCORE19	VTT2	C8
F8	VDDCORE20	VTT3	C10
F10	VDDCORE21	VTT4	C12
F15	VDDCORE22	VTT5	L3
G12	VDDCORE23	VTT6	L16
H4	VDDCORE24	VTT7	N3
H7	VDDCORE25	VTT8	N16
H9	VDDCORE26	VTT9	U8
H10	VDDCORE27	VTT10	U10
H12	VDDCORE28		
H15	VDDCORE29		
J6	VDDCORE30		
J9	VDDCORE31		
J10	VDDCORE32		
J13	VDDCORE33		
K1	VDDCORE34		
K5	VDDCORE35		
K18	VDDCORE36		
L6	VDDCORE37		
L7	VDDCORE38		
L8	VDDCORE39		
L9	VDDCORE40		
L10	VDDCORE41		
L11	VDDCORE42		
L12	VDDCORE43		
L13	VDDCORE44		
M6	VDDCORE45		
M9	VDDCORE46		
M10	VDDCORE47		
M13	VDDCORE48		
N1	VDDCORE49		
N2	VDDCORE50		
N17	VDDCORE51		
N18	VDDCORE52		
P8	VDDCORE53		
P10	VDDCORE54		
P11	VDDCORE55		
T1	VDDCORE56		
T5	VDDCORE57		
T18	VDDCORE58		

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U18
89HPES8T5ZBBCG
52R-567-000

A1	VSS1	VSS67	L5
A2	VSS2	VSS68	L14
A17	VSS3	VSS69	M1
A18	VSS4	VSS70	M2
B4	VSS5	VSS71	M3
B6	VSS6	VSS72	M5
B8	VSS7	VSS73	M7
B10	VSS8	VSS74	M8
B12	VSS9	VSS75	M11
B14	VSS10	VSS76	M12
B15	VSS11	VSS77	M14
C1	VSS12	VSS78	M16
C5	VSS13	VSS79	M17
C7	VSS14	VSS80	M18
C9	VSS15	VSS81	N5
C11	VSS16	VSS82	N6
D5	VSS17	VSS83	N7
D7	VSS18	VSS84	N8
D9	VSS19	VSS85	N9
D11	VSS20	VSS86	N10
D13	VSS21	VSS87	N11
E4	VSS22	VSS88	N12
E7	VSS23	VSS89	N13
E9	VSS24	VSS90	P1
E11	VSS25	VSS91	P2
E13	VSS26	VSS92	P5
F5	VSS27	VSS93	P6
F7	VSS28	VSS94	P7
F9	VSS29	VSS95	P12
F11	VSS30	VSS96	P17
F12	VSS31	VSS97	P18
F13	VSS32	VSS98	R7
F14	VSS33	VSS99	R9
F16	VSS34	VSS100	R11
G4	VSS35	VSS101	T2
G6	VSS36	VSS102	T4
G7	VSS37	VSS103	T6
G8	VSS38	VSS104	T7
G9	VSS39	VSS105	T9
G11	VSS40	VSS106	T11
G13	VSS41	VSS107	T12
G15	VSS42	VSS108	T13
H6	VSS43	VSS109	T17
H8	VSS44	VSS110	U4
H11	VSS45	VSS111	U5
H13	VSS46	VSS112	U6
J4	VSS47	VSS113	U7
J7	VSS48	VSS114	U9
J8	VSS49	VSS115	U11
J11	VSS50	VSS116	U12
J12	VSS51	VSS117	U13
J15	VSS52	VSS118	U14
J16	VSS53	VSS119	V1
K2	VSS54	VSS120	V2
K3	VSS55	VSS121	V5
K6	VSS56	VSS122	V6
K7	VSS57	VSS123	V7
K8	VSS58	VSS124	V8
K9	VSS59	VSS125	V9
K10	VSS60	VSS126	V10
K11	VSS61	VSS127	V11
K12	VSS62	VSS128	V12
K13	VSS63	VSS129	V13
K14	VSS64	VSS130	V14
K16	VSS65	VSS131	V17
K17	VSS66	VSS132	V18

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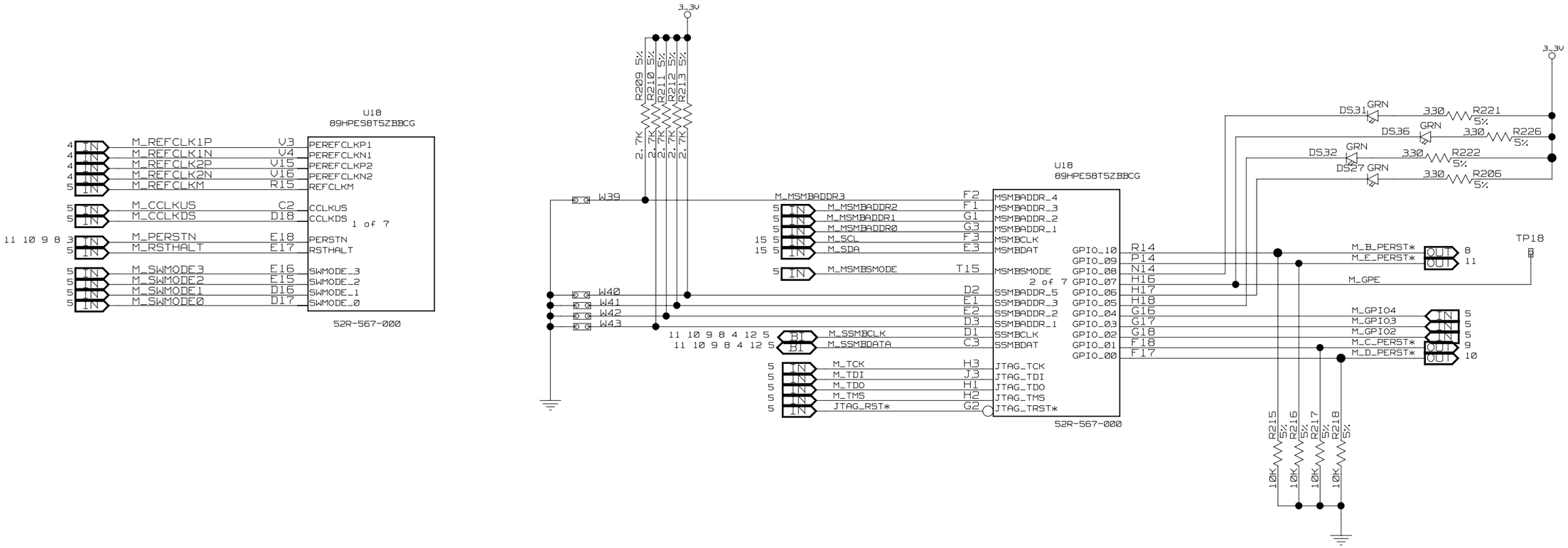
TITLE 89EBPES8T5

PES8T5 - POWER

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00086	18-613-000	1.0

AUTHOR	CHECKED BY
J. CARRILLO	B. OH

Wed Nov 08 17:34:38 2006 SHEET 13 OF 15



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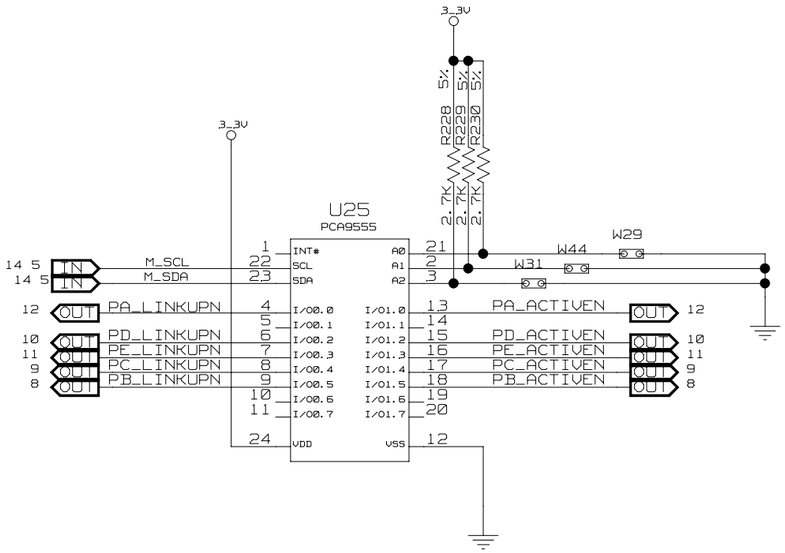
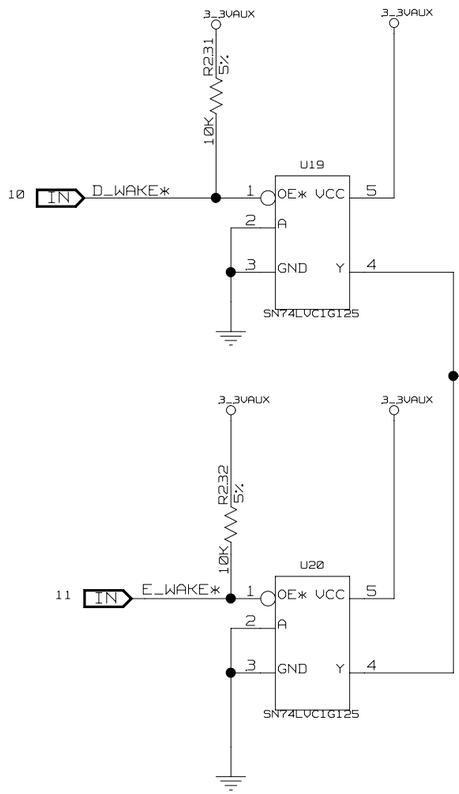
TITLE 89EBPES8T5			
PES8T5 SMBUS REFCLKS			
SIZE B	DRAWING NO. STGSCH-00086	FAB P/N 18-613-000	REV. 1.0
AUTHOR J.CARRILLO		CHECKED BY B.OH	
Wed Nov 08 17:34:39 2006		SHEET 14 OF 15	



IO EXPANDER 4



CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNILOGY, INC. 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138 COPYRIGHT (C) IDT 2006	TITLE 89EBPES8T5 LINK STATUS WAKE		
	SIZE B	DRAWING NO. STGSCH-00086	FAB P/N 18-613-000 / REV. 1.0
	AUTHOR J. CARRILLO	CHECKED BY B. OH	
	Wed Nov 08 17:34:39 2006	SHEET 15 OF 15	

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