IDT™ 89EB-LOGAN-19 Evaluation Board Manual

(Evaluation Board: 18-692-000)

February 2011

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Printed in U.S.A.

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Introduction

The 89HPES24NT24G2 switch is a member of the IDT PCI Express® Inter-Domain Switch family of products. It is a PCIe® Base Specification 2.1 compliant (Gen2) 24-lane, 24-port switch. The EB-LOGAN-19 Evaluation Board provides an evaluation platform for the PES24NT24G2 switch and for other members of this switch family including PES16NT16G2 and PES12NT12G2.

Detailed information related to configuration of number of ports and lanes in the switch device can be found in the Device User Manual and the Device Datasheet. The evaluation board, along with additional adapters and daughter boards provided by IDT, can be configured to test every possible combination of the number of lanes and ports offered by the switch. Advanced capabilities such as switch partitioning, NTB, DMA and local port clocking can be evaluated with the evaluation board.

The EB-LOGAN-19 brings out all 24 lanes of the device to two Mezzanine connectors and two SAS connectors (see Figure 1.1) located close to the device - one connector per stack of 4 lanes. Various types of daughter cards (provided by IDT) can then be plugged into the Mezzanine connectors to facilitate connectivity to one x8 or two x4 or four x2 or eight x1 link partners. Link partners may be plugged directly into these daughter cards or they can be connected to these daughter cards via SAS or SATA cables and a different board with PCIe slots known as the 12-PACK board (provided by IDT). Given that majority of the hosts / servers offer PCIe standard slots, IDT provides the necessary adapter cards that may be plugged into these host / server slots as well as the cables that connect such adapters to the daughter cards which in turn are plugged into the main evaluation board on which the IDT PCIe switch device is populated.

The EB-LOGAN-19 is also used by IDT to reproduce system-level hardware or software issues reported by customers. Figure 1.1 illustrates the functional block diagram representing the main parts of the EB-LOGAN-19 board.

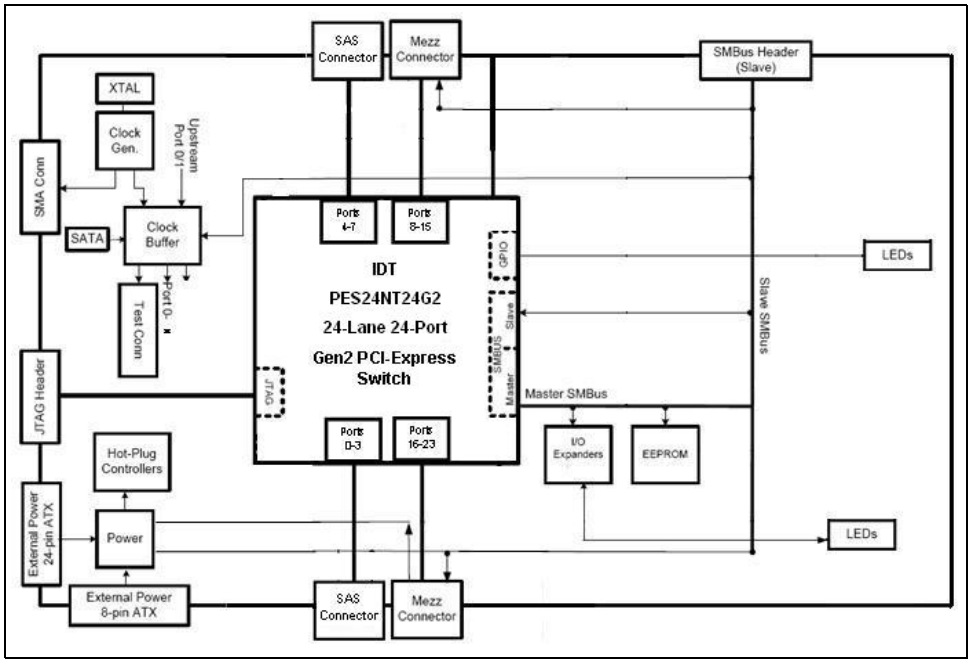


Figure 1.1 Function Block Diagram of the EB-LOGAN-19 Evaluation Board

Notes

Board Features

Hardware

- PES24NT24G2 PCIe 24-port switch
  - *Twenty four ports (each x1) - for port 8 and higher, adjacent ports may be combined to create x2, x4 or x8 ports*
  - *PCIe Base Specification Revision 2.1 compliant (Gen2 SerDes speeds of 5 GT/S)*
  - *Up to 2048 byte maximum Payload Size*
  - *Automatic lane reversal and polarity inversion supported on all lanes*
  - *Automatic per port link width negotiation to x8, x4, x2, x1*
  - *Power on reconfiguration via optional serial EEPROM connected to the SMBUS Master interface*
- Upstream, Downstream Ports
  - *The EB-LOGAN-19 has minimum of one port configured as upstream port to be plugged into a host slot through an adaptor and a cable.*
  - *Up to 23 ports can be configured as downstream ports, for PCIe endpoint add-on cards to be plugged in. The slot connectors can be configured to be x1, x2, x4 or x8, but are mechanically open-ended on one side to allow card widths greater than x8 (e.g. x16) to be populated.*
  - *When used in multi-partition mode, the device can be programmed through the serial EEPROM to generate the appropriate number of upstream and downstream ports per partition.*
- Numerous user selectable configurations set using onboard jumpers and DIP-switches
  - *Source of clock - host clock or onboard clock generator*
  - *Two clock rates (100/125 MHz) from an onboard clock generator*
  - *Flexible clocking modes*
    - *Common clock*
    - *Non-common clock*
    - *Local port clocking on ports that support this feature*
  - *Boot mode selection*
- SMBUS Slave Interface (4 pin header)
- SMBUS Master Interface connected to the Serial EEPROMs through I/O expander
- Push button for Warm Reset
- Many LEDs to display status, reset, power, hotplug, etc.
- JTAG connector to the PES24NT24G2 JTAG pins.

Software

There is no software or firmware executed on the board. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the PES24NT24G2 within host systems running popular operating systems.

- Installation programs
  - *Operating Systems Supported: WindowsServer200x, WindowsXP, Vista, Linux*
- GUI based application for Windows and Linux
  - *Allows users to view and modify registers in the PES24NT24G2*
  - *Binary file generator for programming the serial EEPROMs attached to the SMBUS.*

Other

- SMBUS cable may be required for certain evaluation exercises.
- SMA connectors are provided on the EB-LOGAN-19 board for clock outputs.

Revision History

April 13, 2010: Initial publication of evaluation board manual.

Notes

April 23, 2010: Updated Schematics in Chapter 4.

February 16, 2011: Changed default settings from Off to On in Tables 2.3 and 2.4.

Notes

Installation of the EB-LOGAN-19 Evaluation Board

Notes

EB-LOGAN-19 Installation

This chapter discusses the steps required to configure and install the EB-LOGAN-19 evaluation board. All available DIP switches and jumper configurations are explained in detail.

The primary installation steps are:

1. Configure jumper/switch options suitable for the evaluation or application requirements.
2. Connect PCI Express endpoint cards to the downstream port PCIe slots on the evaluation board.
3. Make sure that the host system (motherboard with root complex chipset) is powered off.
4. Connect the evaluation board to the host system.
5. Apply power to the host system.

The EB-LOGAN-19 board is typically shipped with all jumpers and switches configured to their default settings. In most cases, the board does not require further modification or setup however please visit IDT website and fill out the Technical Support Request form at http://www.idt.com/?app=TechSupport for other configurations.

PCI Express Mezzanine and Edge Adapters

The PCI Express lanes are broken out to four Mezzanine connectors on EB-LOGAN-19 Evaluation Board. The adapter cards are used to convert Mezzanine connector into PCI Express slot connector(s) or Internal mini SAS (iSAS) connectors or both. A Bifurcated Mezzanine Card has two mechanical x8 PCIe Slots (x4 electrically) while a Merged Mezzanine Card has single x8 PCIe Slot. Pictured in Figure 2.1.

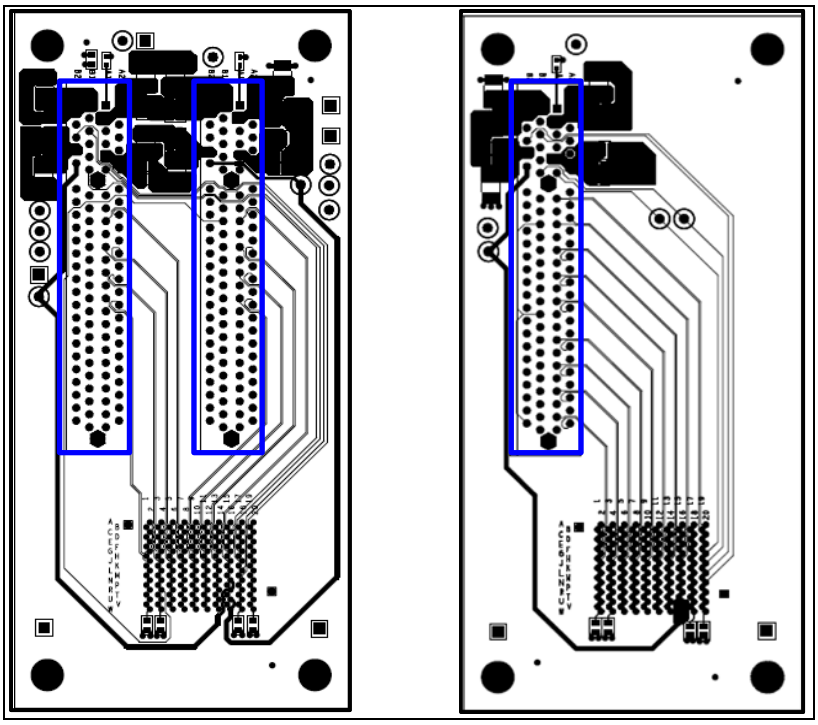


Figure 2.1 Bifurcated and Merged Mezzanine Cards

Notes

Pictured in Figure 2.2 is the mini-SAS Mezzanine card which consists of two iSAS and two SATA connectors. Each iSAS connector supports up to PCI Express x4 width and the SATA connectors are used for clock and reset signals of each x4 or less stack/port. An iSAS-to-SATA breakout cable shown in Figure 2.3 is used connect from iSAS to edge adapter and/or 12PACK.

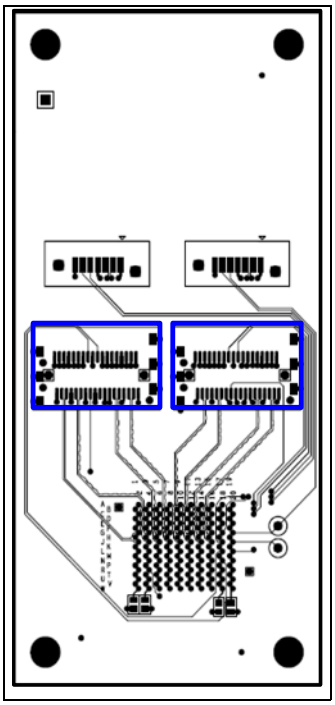


Figure 2.2 MiniSAS Mezzanine Adapter

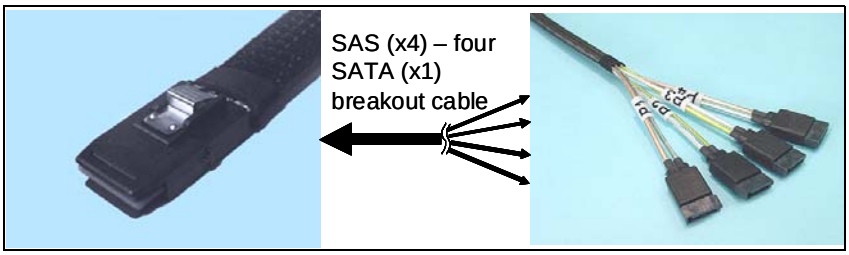


Figure 2.3 EB-LOGAN-19 iSAS-to-SATA Breakout Cable

The PCI Express Edge to SATA Adapter, pictured in Figure 2.4, can be inserted into any physical PCIe slot on a host system and in combination with mini-SAS Mezzanine Card, such as the one in Figure 2.2, to form a link between evaluation main board and the host system. There are 5 SATA connectors which one connector (J7) is for clock and reset, and the rest supports one PICe lane per SATA connector. The edge adapters can be inserted into a mechanical x1 or greater slot.

Notes

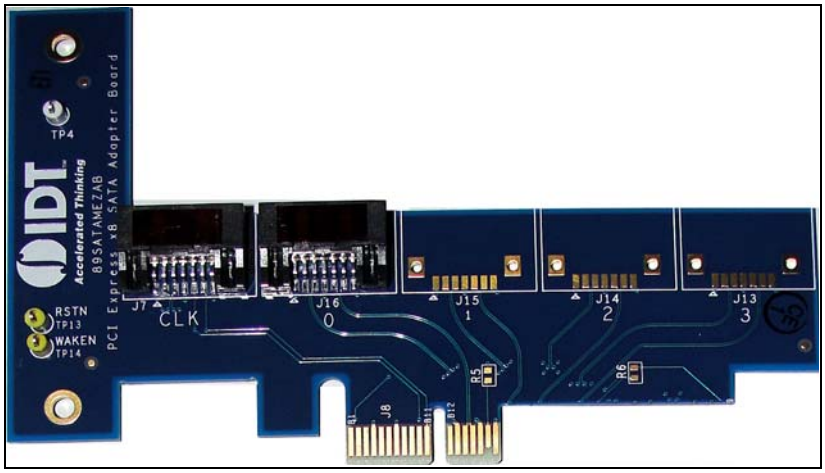


Figure 2.4 PCIe x1 Edge-to-SATA Adapter

Hardware Description

The PES24NT24G2 is a 24-lane, 24-port PCI Express® switch. It is a peripheral chip that performs PCI Express based switching with a feature set optimized for high performance applications such as servers and storage. It provides fan-out and switching functions between a PCI Express upstream port and downstream ports or peer-to-peer switching between downstream ports. Furthermore, up to eight ports can be configured as NTB ports for multi-root application.

The EB-LOGAN-19 Main Board, shown in Figure 2.5, will support up to 4 PCI Express downstream ports and up to 23 ports when using two 12PACK Daughter Boards.

Basic requirements for the board to run are:

- *Host system with a PCI Express root complex supporting x1 configuration through a PCI Express x1 slot.*
- *– x1, x2, x4, or x8 PCI Express Endpoint Cards.*

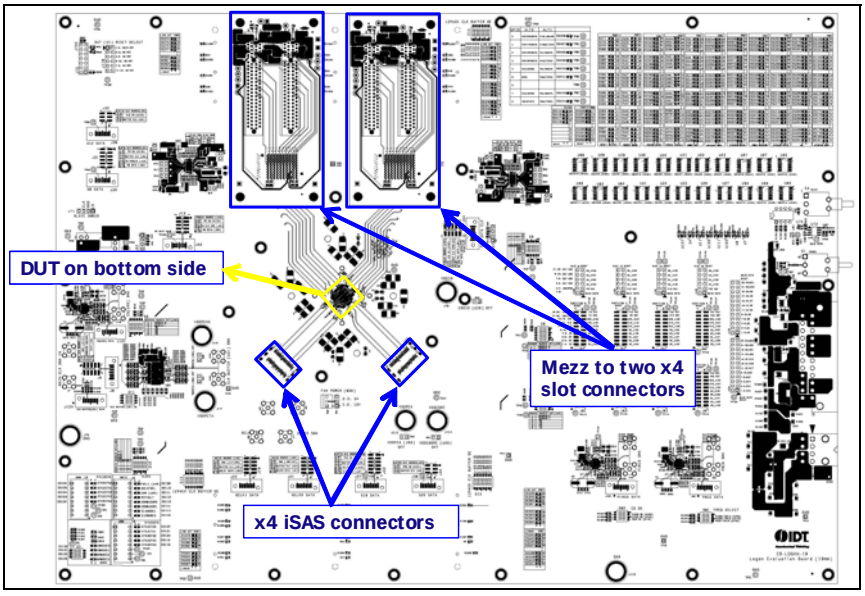


Figure 2.5 EB-LOGAN-19 Evaluation Main Board

Notes

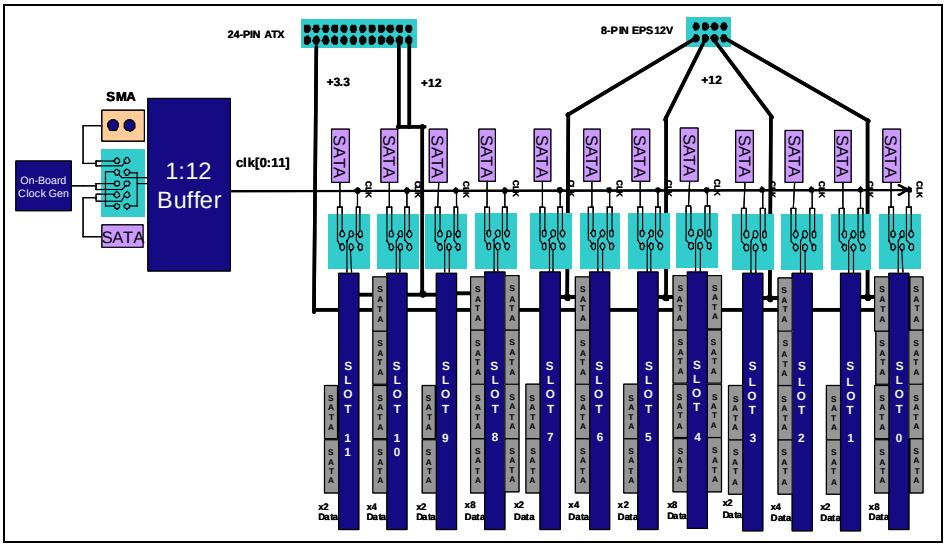


Figure 2.6 12PACK PCIe Slots Breakout Daughter Board

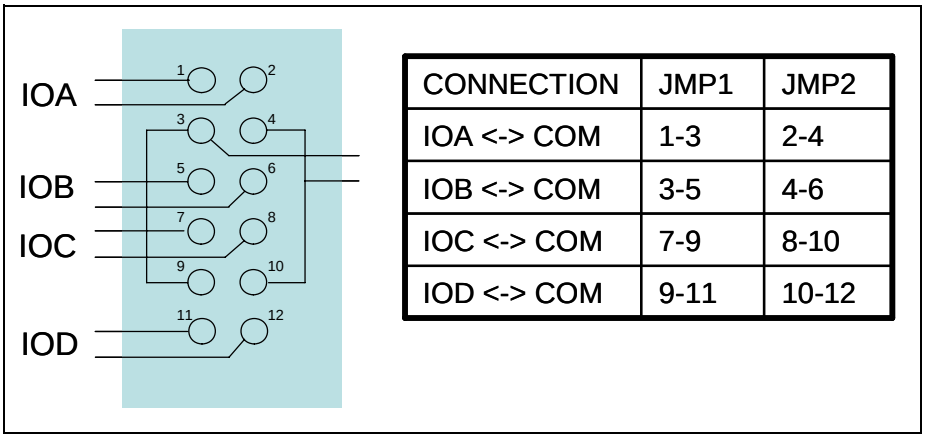
Reference Clocks

Global Reference Input Clocks

The PES24NT24G2 requires two differential reference clocks. The EB-LOGAN-19 derives these clocks from SMA connectors (J17, J20, J66, J67), clock buffer (U50), or SATA connectors (J21, J22) as described in Table 2.1 and Figures 2.7 and 2.8.

Global Clock#	Jumper	Selection
0	J18	[1-3 / 2-4] SMA (J66/J67) [5-7 /6-8] From Clock Buffer U51 (default) [7-9 / 8-10] SATA, J21
1	J19	[1-3 / 2-4] SMA (J17/J20) [5-7 /6-8] From Clock Buffer U51 (default) [7-9 / 8-10] SATA, J22

Table 2.1 EB-LOGAN-19 Global Clock Select



CONNECTION	JMP1	JMP2
IOA <-> COM	1-3	2-4
IOB <-> COM	3-5	4-6
IOC <-> COM	7-9	8-10
IOD <-> COM	9-11	10-12

Figure 2.7 Differential Jumper Arrangement

Notes

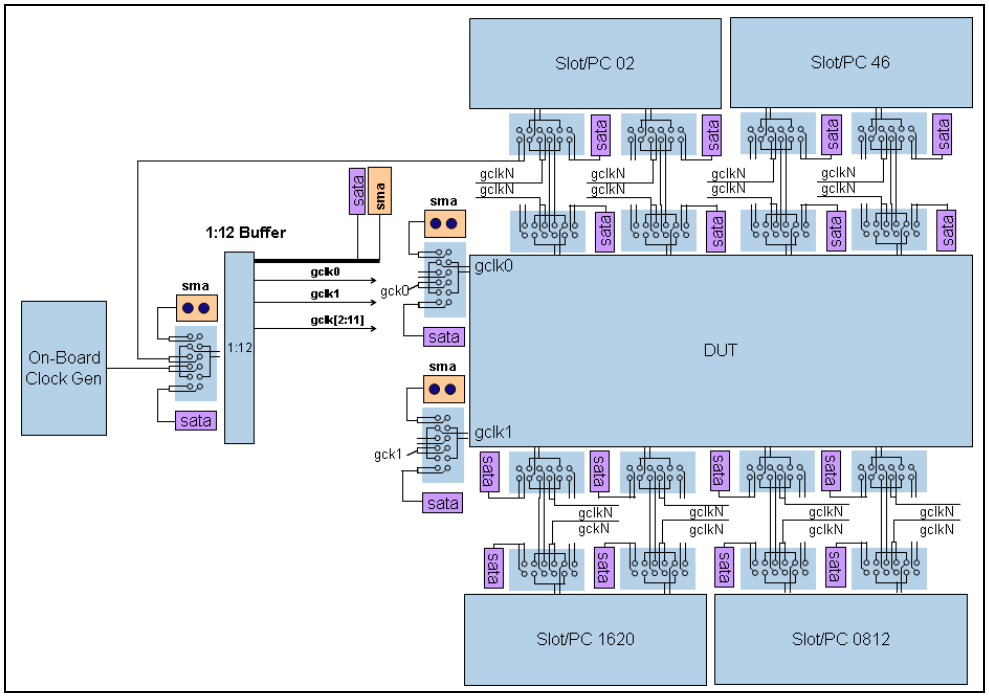


Figure 2.8 Reference Clock Configuration

By default the clock buffer derives its clock from a common source. The common source can be the host system's reference clock, the onboard clock generator, or SATA connector (J8). See Table 2.2.

.

Jumper	Selection
J6	[1-3 / 2-4] SMA (J5/J7) [5-7 / 6-8] Onboard Clock Generator (U49) [7-9 / 8-10] SATA (J8) **(default)**

Table 2.2 Clock Buffer Input Sources

The frequency of the global reference clock input may be selected by the Clock Frequency Select (GCLKFEL) pin to be either 100 MHz or 125 MHz as described in Table 2.3.

Global Clock Frequency Switch - SW10[2	
SW10[2]	Clock Frequency
ON	100 MHz **(Default)**
OFF	125 MHz

Table 2.3 Global Reference Input Clock Frequency Select

The source for the onboard clock is the ICS841484 clock generator device (U49) connected to a 25MHz oscillator (X1). When using the onboard clock generator, the output frequency is fixed at 100MHz. Therefore, ICS_FS (S10, bit 1) is ON as the default setting. See Table 2.4.

Notes

Onboard Clock Frequency Switch - S10[1]	
S10[1]	Clock Frequency
ON	100 MHz (Default)
OFF	125 MHz

Table 2.4 Onboard Clock Generator Frequency Select

The output of the onboard clock generator is accessible through two yellow colored loop connectors located on the Evaluation Board. See Table 2.5. This can be used to connect a scope for probing or capturing purposes and cannot be used to drive the clock from an external source.

Onboard Reference Clock Output (Differential)	
J119	Positive Reference Clock
J120	Negative Reference Clock
J121	SATA Reference Clock

Table 2.5 Onboard Reference Clock Generator Access Points

Local Port Input Clocks

Associated with some ports is a port reference clock input (PxCLK). Depending on the port clocking mode, a differential reference clock is driven into the device on the corresponding PxCLKP and PxCLKN pins. The frequency of a port reference clock input is always 100 MHz. Table 2.6 lists the possible sources for the port reference clock input, and Table 2.7 lists the possible sources for the slot clock input.

Port #	Header	Selection
8	J13	[1-3 / 2-4] Onboard Clock Generator (U118) [5-7 / 6-8] Slot Clock Header (J31) [7-9 / 8-10] SATA (J62) (default)
16	J15	[1-3 / 2-4] Onboard Clock Generator (U120) [5-7 / 6-8] Slot Clock Header (J33) [7-9 / 8-10] SATA (J64) (default)

Table 2.6 EB24NT24G2 Port Clock Select

Slot/Port #	Header	Selection
8	J31	[1-3 / 2-4] Onboard Clock Generator (U118) [3-5 / 4-6] From Clock Buffer (default) [7-9 / 8-10] To P08CLK Clock Header (J13) [9-11 / 8-10] SATA (J35)

Table 2.7 EB-LOGAN-19 Slot Clock Select (Part 1 of 2)

Notes

Slot/Port #	Header	Selection
12	J32	[1-3 / 2-4] From Clock Buffer (default) [3-5 / 4-6] SATA (J36)
16	J33	[1-3 / 2-4] Onboard Clock Generator (U120) [3-5 / 4-6] From Clock Buffer (default) [7-9 / 8-10] To P16CLK Clock Header (J15) [9-11 / 8-10] SATA (J37)
20	J34	[1-3 / 2-4] From Clock Buffer (default) [3-5 / 4-6] SATA (J38)

Table 2.7 EB-LOGAN-19 Slot Clock Select (Part 2 of 2)

CLKMODE Selection

All ports in the PES24NT24G2 device (upstream and downstream) use global clocked mode. The port clocking mode of a port is determined by the state of the CLKMODE[1:0] pins in the boot configuration vector as shown in Table 2.8. This field determines the initial value of the Slot Clock Configuration (SCLK) field in each port's PCI Express Link Status (PCIELSTS) register. The SCLK field controls the advertisement of whether or not the port uses the same reference clock source as the link partner. A one in the SCLK field indicates that the port and its link partner use the same reference clock source. This is defined as Common Clock Configuration by the PCI Express Base Specification. A zero in the SCLK field indicates that the port and its link partner do not use the same reference clock source.

SW10[8] CLKMODE[0]	SW10[7] CLKMODE[1]	Port 0 SCLK	Port[23:1] SCLK
ON	ON	0	0
OFF	ON	1	0
ON	OFF	0	1
OFF	OFF	1	1

Table 2.8 CLKMODE Selection PES24NT24G2

Power Sources

Power for the PES24NT24G2 and all downstream ports will be generated from the 12V from an external power connector. See Table 2.9. A 12V to 3.3V DC-DC converter will be used to provide power to five switching regulators to generate V_{DD}CORE, V_{DD}PEA, V_{DD}PETA, V_{DD}PEHA, and V_{DD}IO voltages. The 3.3V from the DC-DC converter will be used to power the clock buffers and circuitries.

The external power supply connectors are 24-pin (J69) and 8-pin (J68) molex connector as described in Tables 2.9 and 2.10. The +12V3 is used to power PES32NT24AG2 and downstream slots 16 and 20. The +12V2 is used to power downstream slots 8 and 12.

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	GND	15	GND
4	+5V	16	PS_ON
5	GND	17	GND

Table 2.9 EPS12V 24-pin Power Connector - J6 (Part 1 of 2)

Notes

Pin	Signal	Pin	Signal
6	+5V	18	GND
7	GND	19	GND
8	PWR_OK	20	NC
9	5VSB	21	+5V
10	+12V3	22	+5V
11	+12V3	23	+5V
12	+3.3V	24	GND

Table 2.9 EPS12V 24-pin Power Connector - J6 (Part 2 of 2)

Pin	Signal	Pin	Signal
1	GND	5	+12V1
2	GND	6	+12V1
3	GND	7	+12V2
4	GND	8	+12V2

Table 2.10 EPS12V 8-Pin Connector - J5

The power on switch located at S1 can be used to control the supply power from the external power supply connector. Add a shunt to W27 to enable power on switch.

PCI Express Analog Power Voltage Regulator

A voltage regulator (U65) provides a 2.5V PCI Express analog power voltage (shown as VDDPEHA) to the PES24NT24G2.

PCI Express Digital Power Voltage Converter

A separate voltage regulator (U62) provides a 1.0V PCI Express analog power voltage (shown as VDDPEA) to the PES24NT24G2.

PCI Express Transmitter Analog Voltage Converter

A separate voltage regulator (U68) provides a 1.0V PCI Express transmitter analog voltage (shown as VDDPETA) to the PES24NT24G2.

Core Logic Voltage Converter

A separate voltage regulator (U59) provides the 1.0V core voltage (VDDCORE) to the PES24NT24G2.

3.3V I/O Voltage Regulator

A separate voltage regulator (U56) provides the 3.3V I/O voltage (VDDIO) to the PES24NT24G2.

Power-up Sequence for PES24NT24G2

During power supply ramp-up, VDDCORE must remain at least 1.0V below VDDIO at all times. There are no other power-up sequence requirements for the various operating supply voltages.

Heatsink Requirement

The EB-LOGAN-19 evaluation board utilizes a heatsink with integrated fan.

Notes

Reset

The PES24NT24G2 supports two types of reset mechanisms as described in the PCI Express specification:

- *Fundamental Reset: This is a system-generated reset that propagates along the PCI Express tree through a single side-band signal PERST# which is connected to the Root Complex, the PES24NT24G2, and the endpoints.*
- *Hot Reset: This is an In-band Reset, communicated downstream via a link from one device to another. Hot Reset may be initiated by software. This is further discussed in the PES24NT24G2 User Manual. The EB-LOGAN-19 evaluation board provides seamless support for Hot Reset.*

Fundamental Reset

There are two types of Fundamental Resets which may occur on the EB-LOGAN-19 evaluation board:

- *Cold Reset: During initial power-on, the onboard voltage monitor (TLC7733D) will assert the PCI Express Reset (PERSTN) input pin of the PES24NT24G2.*
- *Warm Reset: This is triggered by hardware while the device is powered on. Warm Reset can be initiated by two methods:*
  - *Pressing a push-button switch (S3) located on EB-LOGAN-19 board*
  - *The host system board IO Controller Hub asserting PERST# signal, which propagates through the PCIe upstream edge connector of the EB-LOGAN-19.*

  Both events cause the onboard voltage monitor (TLC7733D) to assert the PCI Express Reset (PERSTN) input of the PES24NT24G2 while power is on.

Downstream Reset

Single Partition Mode without Hot Plug:

When the evaluation board initially powers on is assumes the following:

- The switch is configured in single partition mode.
- Slot 0 is the root port and controls the downstream port resets.
- Ports 1-23 are downstream ports.
- Hot Plug is disabled.

The following behavior should be observed:

- The resets to slots 1-23 should initially be asserted and remain this way until after the fundamental reset is initially de-asserted.
- The assertion of slot 0 reset should propagate to slots 1-23.

Stack Configuration

The PES24NT24G2 contains four stack blocks labeled Stack 0, Stack 1, Stack 2, and Stack 3. Stacks 0 and 1 have four x1 ports each, and stacks 2 and 3 have eight x1 ports each. This provides a total of 24 ports in the device labeled port 0 through port 23. Table 2.11 lists the ports associated with each stack.

Stacks 0 and 1 have non-mergeable x1 ports. Stacks 2 and 3 may be configured as eight x1 ports, four x2 ports, two x4 ports, one x8 port, and any combinations in between. The configuration of each stack is controlled by the Stack Configuration (STK[3:2]CFG) registers. For possible configurations please refer to the device user manual.

Notes

Stack	Ports Associated with the Stack
Stack 0	0, 1, 2, 3
Stack 1	4, 5, 6, 7
Stack 2	8, 9, 10, 11, 12, 13, 14, 15
Stack 3	16, 17, 18, 19, 20, 21, 22, 23

Table 2.11 Ports in Each Stack

Boot Configuration Vector

A boot configuration vector consisting of the signals listed in Table 2.12 is sampled by the PES24NT24G2 during a fundamental reset (while PERSTN is active). The boot configuration vector defines the essential parameters for switch operation and is set using DIP switches S5, SW8, SW9 and SW10 as defined in Table 2.13.

Signal	Description
GCLKFSEL	Global Clock Frequency Select. This pin specifies the frequency of the GCLKP and GCLKN signals.. Default: low
CLKMODE[1:0]	Clock Mode. These pins specify the clocking mode used by switch ports. See Table 2.8 for a definition of the encoding of these signals. The value of these signals may be overridden by modifying the Port Clocking Mode (PCLKMODE) register.. Default: 0x3
RSTHALT	Reset Halt. When this pin is asserted during a switch fundamental reset sequence, the switch remains in a quasi-reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the quasi-reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master. Refer to section Switch Fundamental Reset on page 3-2 for further details. Default: low
SSMBADDR[2:1]	Slave SMBus Address. SMBus address of the switch on the slave SMBus. Default: 0x3
SWMODE[3:0]	Switch Mode. These pins specify the switch operating mode. Default: 0x0
STK2CFG[4:0]	Stack 2 Configuration. These pins select the configuration of stack 2 during a switch fundamental reset. Default: 0x1
STK3CFG[4:0]	Stack 3 Configuration. These pins select the configuration of stack 3 during a switch fundamental reset. Default: 0x1

Table 2.12 Boot Configuration Vector Signals

Location	Signal	Default
S5[1]	SWMODE[0]	ON
S5[2]	SWMODE[1]	ON
S5[3]	SWMODE[2]	ON
S5[4]	SWMODE[3]	ON
SW8[1]	STK2CFG[0]	OFF
SW8[2]	STK2CFG[1]	ON

Table 2.13 Boot Configuration Vector Switches S5, SW8 - SW10 (Part 1 of 2)

Notes

Location	Signal	Default
SW8[3]	STK2CFG[2]	ON
SW8[4]	STK2CFG[3]	ON
SW8[5]	STK2CFG[4]	ON
SW9[1]	STK3CFG[0]	OFF
SW9[2]	STK3CFG[1]	ON
SW9[3]	STK3CFG[2]	ON
SW9[4]	STK3CFG[3]	ON
SW9[5]	STK3CFG[4]	ON
SW10[2]	GCLKFSEL	ON
SW10[4]	RSTHALT	ON
SW10[5]	SSMBADDR[2]	OFF
SW10[6]	SSMBADDR[1]	OFF
SW10[7]	CLKMODE[1]	OFF
SW10[8]	CLKMODE[0]	OFF

Table 2.13 Boot Configuration Vector Switches S5, SW8 - SW10 (Part 2 of 2)

SMBus Interfaces

The System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate. It is based on the principles of operation of I^2C. Implementation of the SMBus signals in the PCI Express connector is optional and may not be present on the host system. The SMBus interface consists of an SMBus clock pin and an SMBus data pin.

The PES24NT24G2 contains two SMBus interfaces: a slave SMBus interface and a master SMBus interface. The slave SMBus interface allows a SMBus Master device full access to all software-visible registers. The Master SMBus interface provides a connection to the external serial EEPROM used for initialization and the I/O expanders used for hot-plug signals.

SMBus Slave Interface

On the PES24NT24G2 board, the slave SMBus interface is accessible through a 4-pin header as described in Table 2.14.

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Slave SMBus Interface Connector J71	
Pin	Signal
1	SDA
2	GND
3	SCL
4	NC

Table 2.14 Slave SMBus Interface Connector

For a fixed address, the SMBus address of the PES24NT24G2 slave interface is 0b1110111 by default and is configurable using DIP Switches SW10[5] and SW10[6] as described in Table 2.15.

Notes

Slave Interface Address Configuration	
Address Bit	Signal
1	SSMBUSADDR[1]
2	SSMBUSADDR[2]
3	1
4	0
5	1
6	1
7	1

Table 2.15 SMBus Slave Interface Address Configuration

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. Initiation of any SMBus transaction other than those listed above produces undefined results. See the SMBus 2.0 specification for a detailed description of the following transactions:

- *Byte and Word Write/Read*
- *Block Write/Read*

SMBus Master Interface

Connected to the master SMBus interface are twenty-two 16-bit I/O Expanders (MAX7311AUG) and a serial EEPROM, U77 (24LC512). The I/O Expanders are used as the interface for the onboard hot-plug controllers (MIC2591B). The lower three bits of the bus address for the I/O Expander 0 through I/O Expander 20 are fixed through the stuffing resistor as 0x20, 0x22, 0x24, 0x26, 0x28, 0x2A, 0x2C, 0x2E, 0x50, 0x52, x54, 0x56, 0x58, 0x5A, 0x5C, 0x5E, 0xB0, 0xA2, 0xA4, 0xA6, 0xA8, and 0xAA, respectively.

Note: Hot-plug is not implemented when the PES24NT24G2 is installed.

The seven bits address for the selected EEPROM device is fixed at **`0b1010_000`** by default.

JTAG Header

The EB-LOGAN-19 provides a JTAG connector J73 for access to the PES24NT24G2 JTAG interface. The connector is a 2.54 x 2.54 mm pitch male 14-pin connector. Refer to Table 2.16 for the JTAG Connector J73 pin out.

JTAG Connector J73					
Pin	Signal	Direction	Pin	Signal	Direction
1	/TRST - Test reset	Input	2	GND	—
3	TDI - Test data	Input	4	GND	—
5	TDO - Test data	Output	6	GND	—
7	TMS - Test mode select	Input	8	GND	—
9	TCK - Test clock	Input	10	GND	—
11	3.3V		12	N/C	—
13	GND	—	14	3.3V	

Table 2.16 JTAG Connector Pin Out

Notes

PCI Express Connectors

Pin	Side A		Side B	
1	+12V	12V power	PRSNT1#	Hot-Plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential	RSVD	Reserved
20	PETn1	pair, Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential
22	GND	Ground	PERn1	pair, Lane 1
23	PETp2	Transmitter differential	GND	Ground
24	PETn2	pair, Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential
26	GND	Ground	PERn2	pair, Lane 2
27	PETp3	Transmitter differential	GND	Ground
28	PETn3	pair, Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential
30	RSVD	Reserved	PERn3	pair, Lane 3
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETp4	Transmitter differential	RSVD	Reserved

Table 2.17 PCI Express x8 Connector Pinout (Part 1 of 2)

Notes

Pin	Side A		Side B	
34	PETn4	pair, Lane 4	GND	Ground
35	GND	Ground	PERp4	Receiver differential
36	GND	Ground	PERn4	pair, Lane 4
37	PETp5	Transmitter differential	GND	Ground
38	PETn5	pair, Lane 5	GND	Ground
39	GND	Ground	PERp5	Receiver differential
40	GND	Ground	PERn5	pair, Lane 5
41	PETp6	Transmitter differential	GND	Ground
42	PETn6	pair, Lane 6	GND	Ground
43	GND	Ground	PERp6	Receiver differential
44	GND	Ground	PERn6	pair, Lane 6
45	PETp7	Transmitter differential	GND	Ground
46	PETn7	pair, Lane 7	GND	Ground
47	GND	Ground	PERp7	Receiver differential
48	PRSNT2#	Hot-Plug presence detect	PERn7	pair, Lane 7
49	GND	Ground	GND	Ground

Table 2.17 PCI Express x8 Connector Pinout (Part 2 of 2)

Notes

EB-LOGAN-19 Board Figure

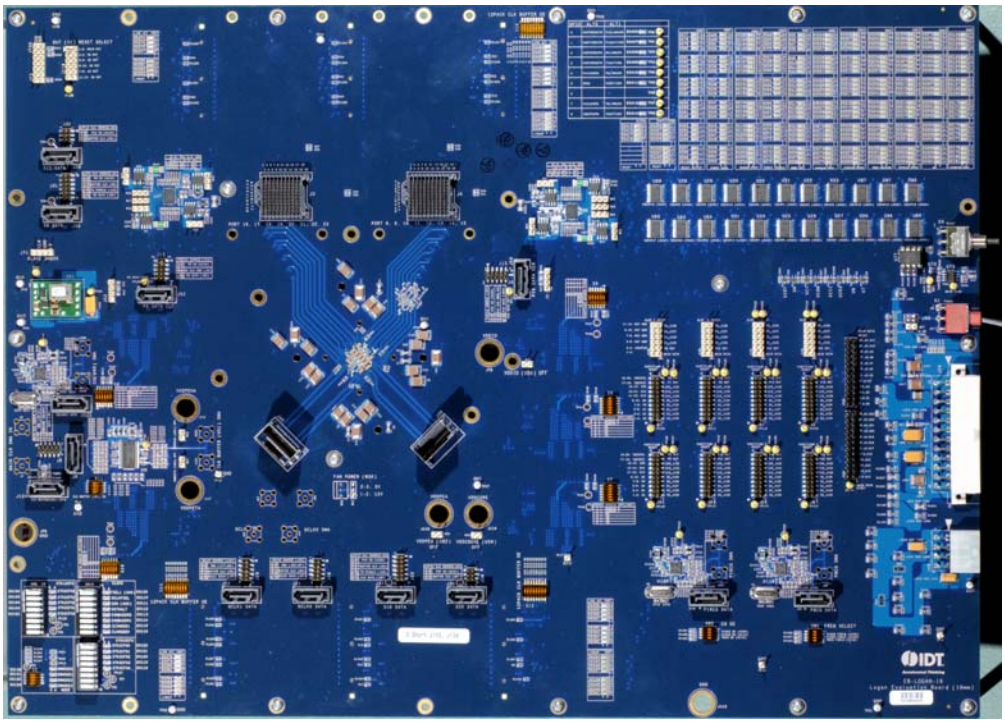

Figure 2.9 EB24NT24G2 Evaluation Board

Notes

Software for the EB-LOGAN-19 Eval Board

Notes

Introduction

This chapter discusses some of the main features of the available software to give users a better understanding of what can be achieved with the EB-LOGAN-19 evaluation board using the device management software.

Device management software and related user documentation are available on a CD which is included in the Evaluation Board Kit. This information is also available on IDT FTP site and also at my.idt.com. For more information, please go to: http://www.idt.com/?app=TechSupport&prodFamily=PCIe%20Switches or email IDT at ssdhelp@idt.com.

Device Management Software

The primary use of the Device Management Software package is to enable users of the evaluation board to access all the registers in the PES24NT24G2 device. This access can be achieved using the PCI Express in-band configuration cycles through the upstream port on the PES24NT24G2 or through the SMBUS salve interface available on the IDT PCIe switch.

This software also enables users to save a snapshot of the current register set into a dump file which can be used for debugging purposes. An export/import facility is also available to create and use "Configuration" files which can be used to initialize the switch device with specific values in specific registers.

A conversion utility is also provided to translate a configuration file into an EEPROM programmable data structure. This enables the user to program an appropriate serial EEPROM with desirable register settings for the PES24NT24G2, and then to populate that EEPROM onto the Evaluation Board. It is also possible to program the EEPROM directly on the Evaluation Board using a feature provided by the software package.

The front-end of the Device Management Software is a user-friendly Graphical User Interface which allows the user to quickly read or write the registers of interest. The GUI also permits the user to run the software in "simulation" mode with no real hardware attached, allowing the creation of configuration files for the PES24NT24G2 in the absence of the actual device.

Much of the Device Management Software is written with device-independent and OS-independent code. The software is expected to work on Linux (/sys interface) and MS Windows XP. It may function well on various flavors of MS Windows, but may not be validated on all. The fact that the software is device-independent assures its scalability to future PCIe parts from IDT. Once users are familiar with the GUI, they will be able to use the same GUI on all PCIe parts from IDT. This software is customized for each device through an XML device description file which includes information on the number of ports, registers, types of registers, information on bit-fields within each register, etc.

The actual program name of the Device Management Software is "PCIeBrowser" (an executable file under Windows or Linux). Revision 5.0.1 or later is required for devices in the PES24NT24G2 product family family.

Device Drivers

The PES24NT24G2 and other members of this switch family offer Non-Transparent Bridging and built-in DMA capability inside the device. Device drivers are needed to take advantage of these features. Sample code for these drivers is available from IDT for the Linux operating system. Additionally, there a few other software packages available from IDT. These packages are not related to the evaluation board per se, and therefore not listed here. However, several of these packages may prove to be useful for specific device or system functionality. For more information, please go to http://www.idt.com/?app=TechSupport&prodFamily=PCIe%20Switches or email IDT at ssdhelp@idt.com.

Notes

Schematics

Notes

Schematics

REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
	1.0	INITIAL RELEASE	2009-12-05	T. TRAN

1. TITLE PAGE / TABLE OF CONTENTS

TITLE: EB-LOGAN-19

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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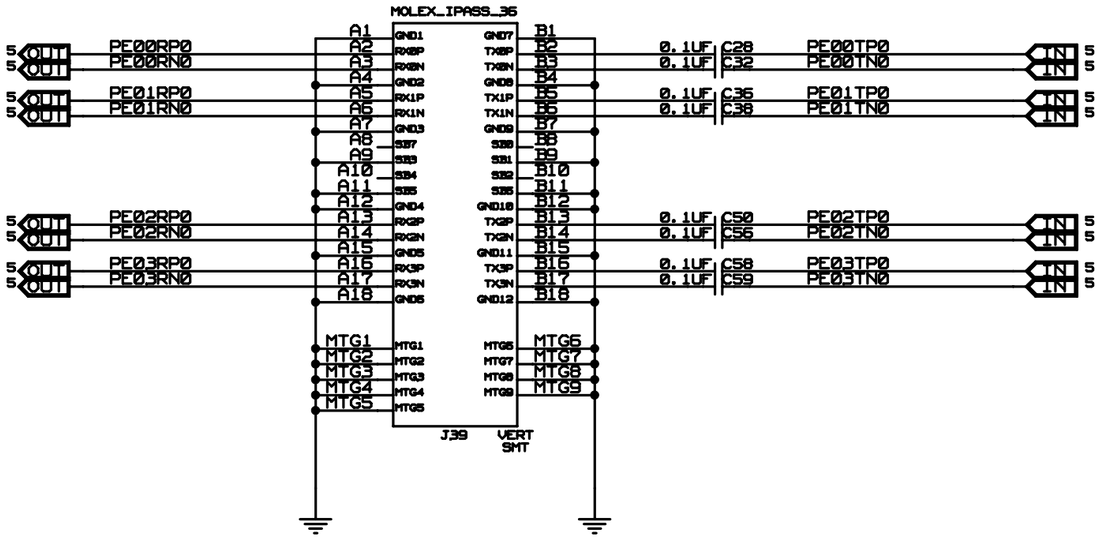

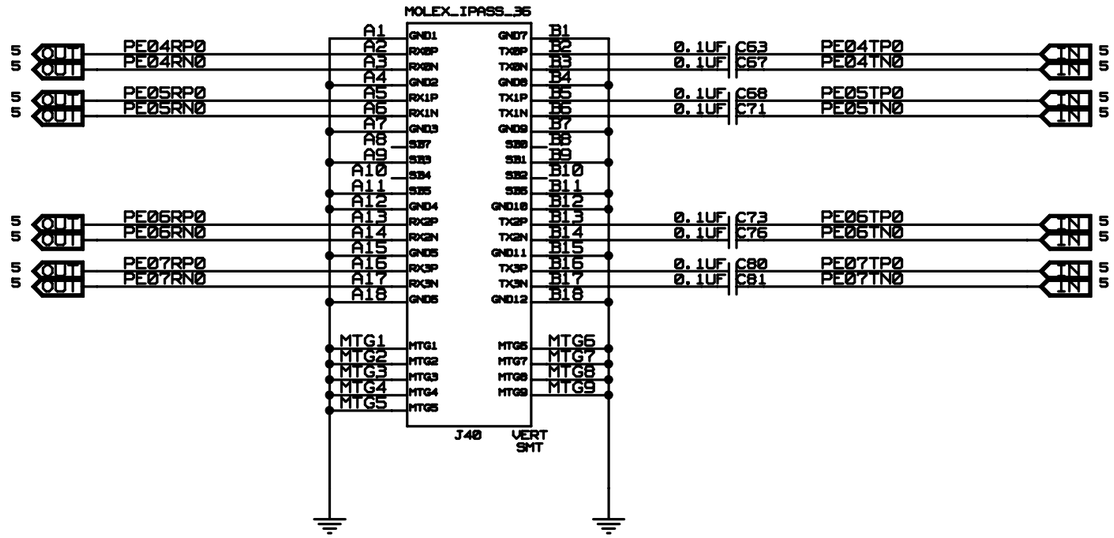

TITLE EB-LOGAN-19

SAS CONNECTOR PORTS 0-7

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B	SCH-PESEB-002	18-692-000	1.1

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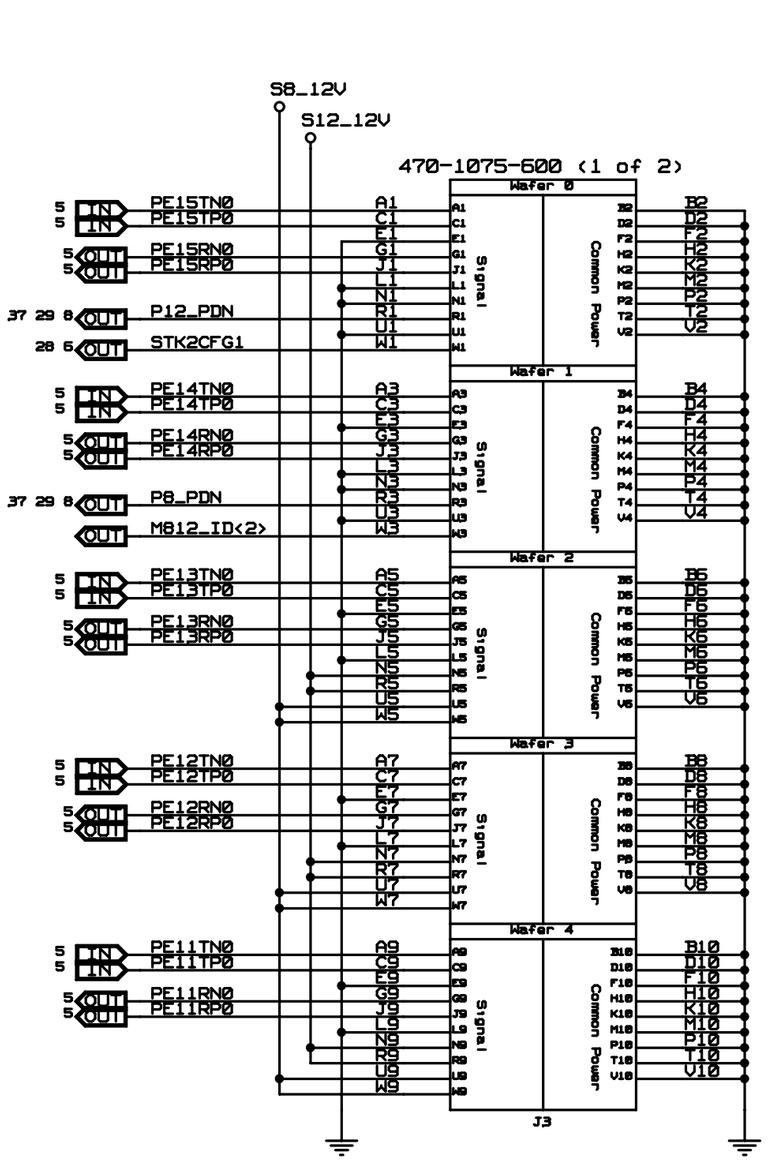
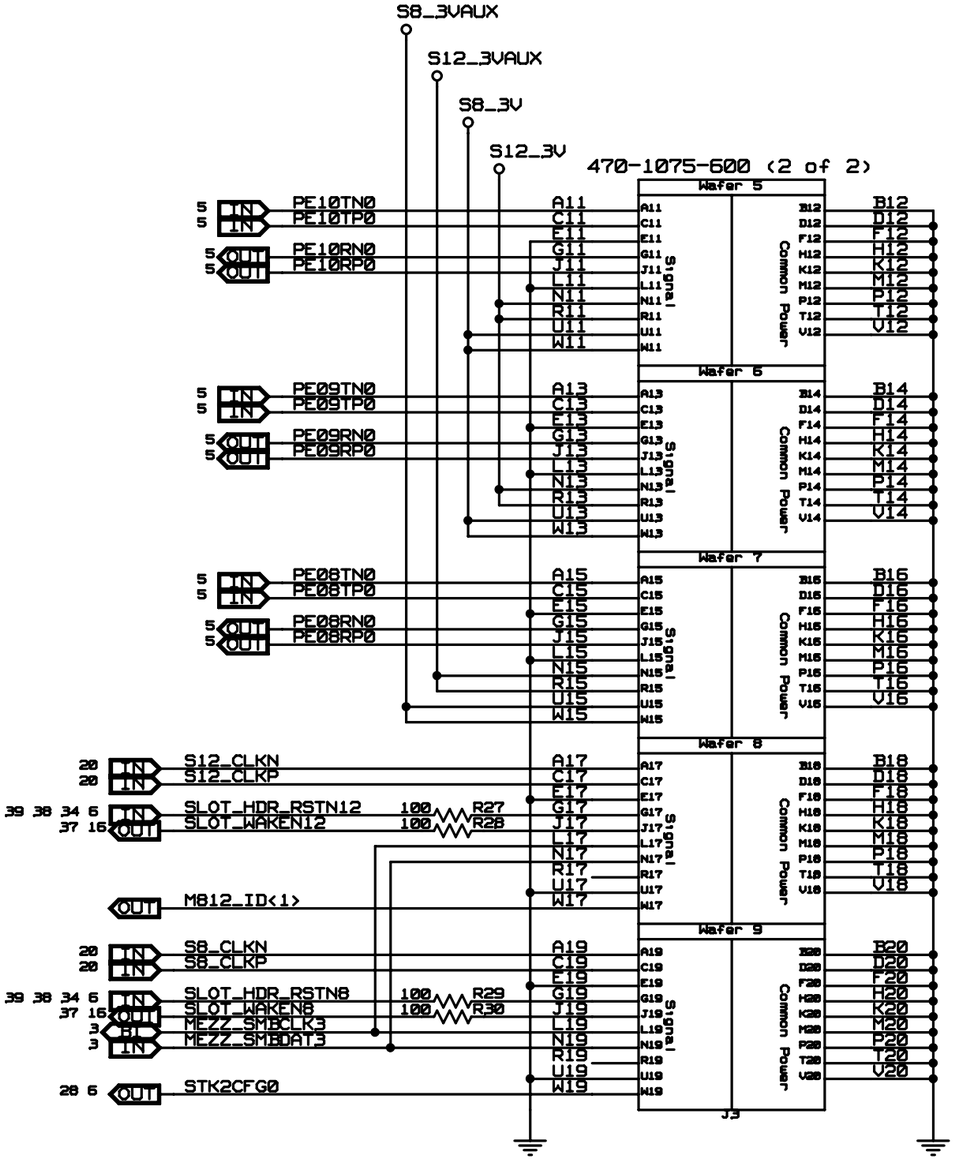
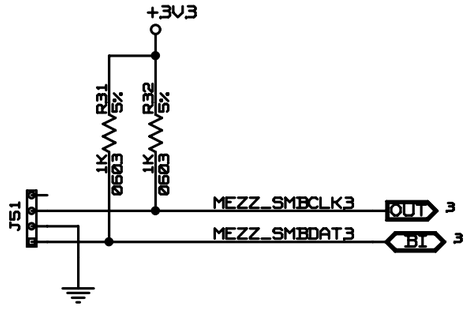




STK2CFG1 & STK2CFG0 SET BY MEZZ CARDS
X8 - STK2CFG1 = 0, STK2CFG0 = 0
X4 - STK2CFG1 = 0, STK2CFG0 = 1



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MEZZANINE CONNECTOR PORTS 8/12

SIZE	DRAWING NO.	FAB P/N	REV.
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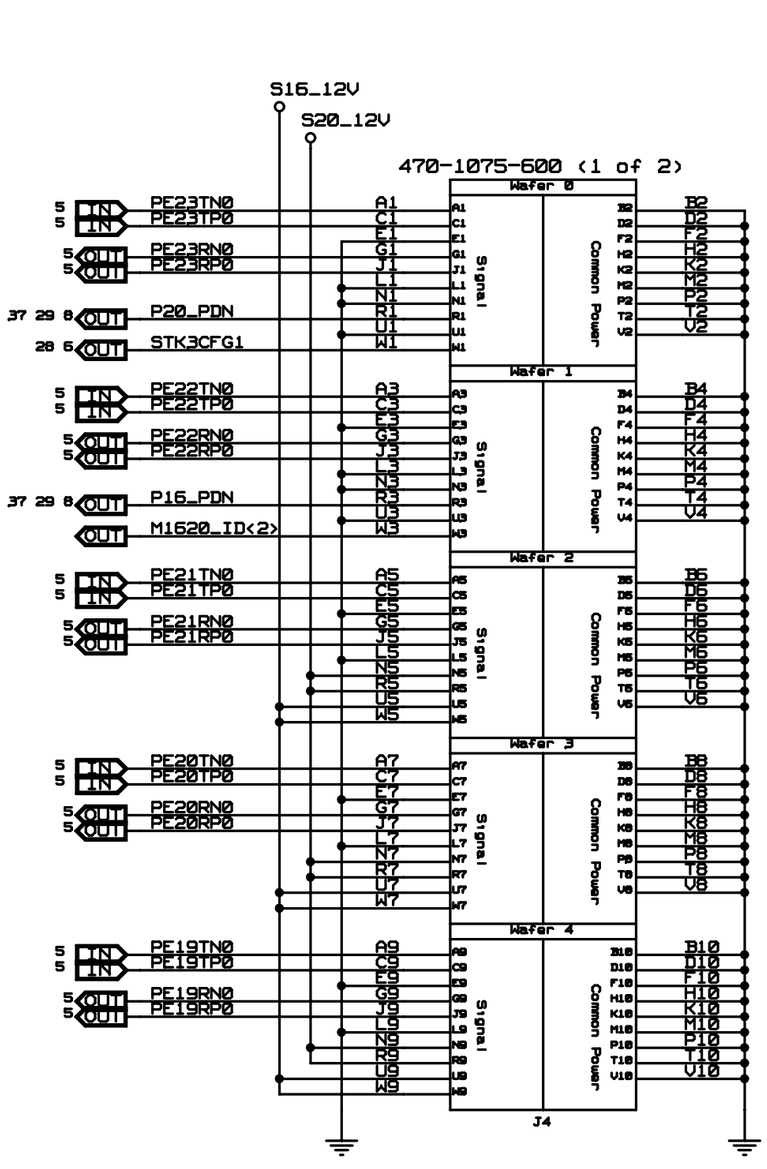
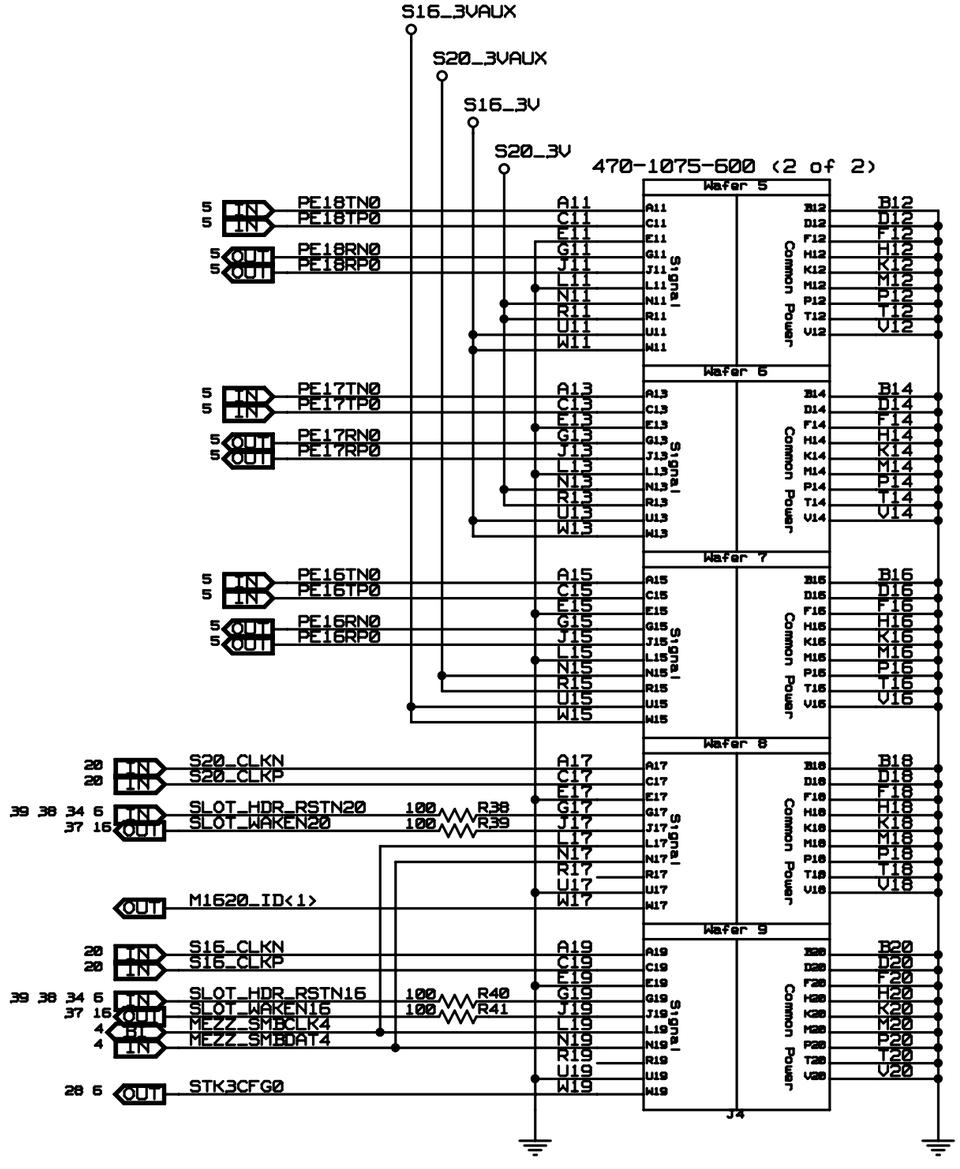
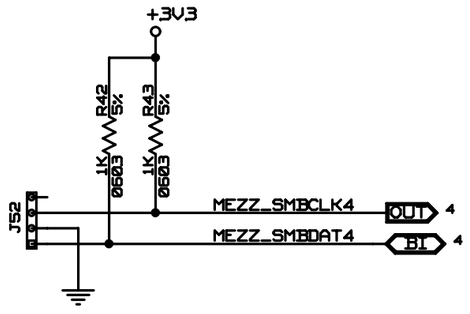




STK3CFG1 & STK3CFG0 SET BY MEZZ CARDS
X8 - STK3CFG1 = 0, STK3CFG0 = 0
X4 - STK3CFG1 = 0, STK3CFG0 = 1



TITLE EB-LOGAN-19

MEZZANINE CONNECTOR PORTS 16/20

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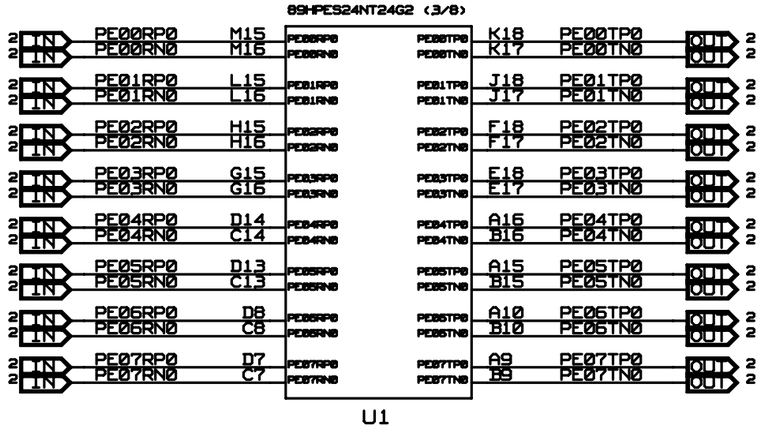

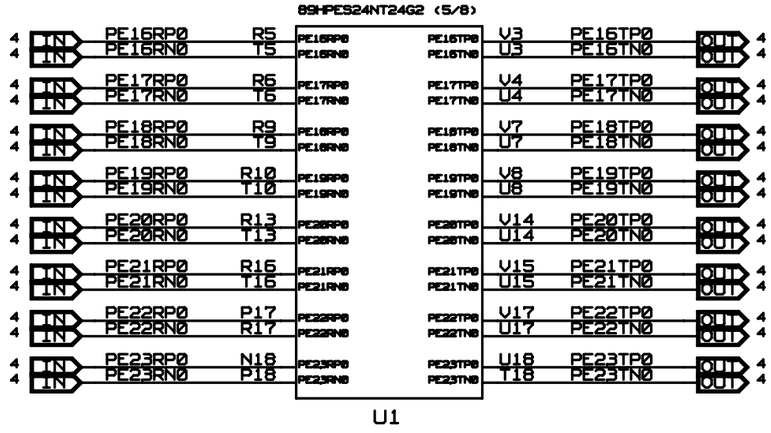

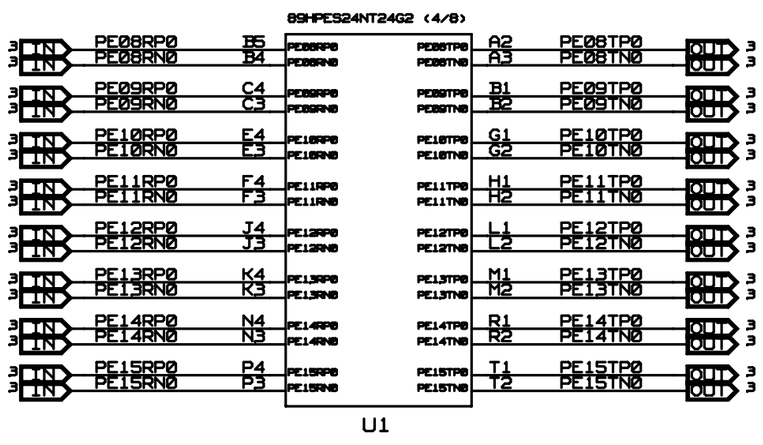

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24NT24G2 - SERDES

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B	SCH-PESEB-002	18-692-000	1.1

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DUT RESET

HDR_2x6

MAIN_RSTN
SLOT_HDR_RSTN8
SLOT_HDR_RSTN12
SLOT_HDR_RSTN16
SLOT_HDR_RSTN20

J118

89HPES24NT24G2 (1/8)

GCLK1P A12
GCLK1N B12
GCLK0P V12
GCLK0N U12
GCLKFSEL N2
PERSTN E14
RSTHALT T3
STK2CFG4 R4
STK2CFG3 C5
STK2CFG2 B6
STK2CFG1 D6
STK2CFG0 D5
STK3CFG4 U2
STK3CFG3 C6
STK3CFG2 B7
STK3CFG1 A5
STK3CFG0 E5
SWMODE3 N1
SWMODE2 R3
SWMODE1 P5
SWMODE0 T4
CLKMODE1 U1
CLKMODE0 C15

P08CLKP D1
P08CLKN D2
P16CLKP V11
P16CLKN U11
G3 A8
G2 A4
G1 B8

PLACE RESISTORS AS CLOSE TO U1 AS POSSIBLE

REFRES00 M18 REFRES07 3.01K R46
REFRES01 G17 REFRES06 3.01K R47
REFRES02 C12 REFRES05 3.01K R48
REFRES03 C9 REFRES04 3.01K R49
REFRES04 H4 REFRES03 3.01K R50
REFRES05 L4 REFRES02 3.01K R51
REFRES06 U6 REFRES01 3.01K R52
REFRES07 U16 REFRES00 3.01K R53
REFRESPLL C10 REFRESPLL 3.01K R54

U1

+3V3

R24 1K 0603 5%
R55 1K 0603 5%

MSMBCLK
MSMBDAT

R45 0

89HPES24NT24G2 (2/8)

MSMBCLK B18
MSMBDAT D16
SSMBADDR2 R18
SSMBADDR1 F15
SSMBCLK C18
SSMBDAT C17
NC1 B14
NC2 M17

JTAG_TCK D17 DUT_JTAG_TCK
JTAG_TDI E15 DUT_JTAG_TDI
JTAG_TDO B17 DUT_JTAG_TDO
JTAG_TMS D15 DUT_JTAG_TMS
JTAG_TRST_N C16 DUT_JTAG_TRST_N

GPIO00 T14
GPIO01 R14
GPIO02 T15
GPIO03 R15
GPIO04 N16
GPIO05 P16
GPIO06 N15
GPIO07 N14
GPIO08_IOEXPINTN N17

U1

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24NT24G2 - CLK, CONFIG, GPIO

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B	SCH-PESEB-002	18-692-000	1.1

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LABEL: FAN
LABEL:
1 GND
2 12V/5V
3 NC

W30

W31

+12V3_PS

+5V0_PS

+1V0_CORE

+3V3_IO

+1V0_PEA

+2V5_PEHA

+1V0_PETA

89HPES24NT24G2 (5/8)

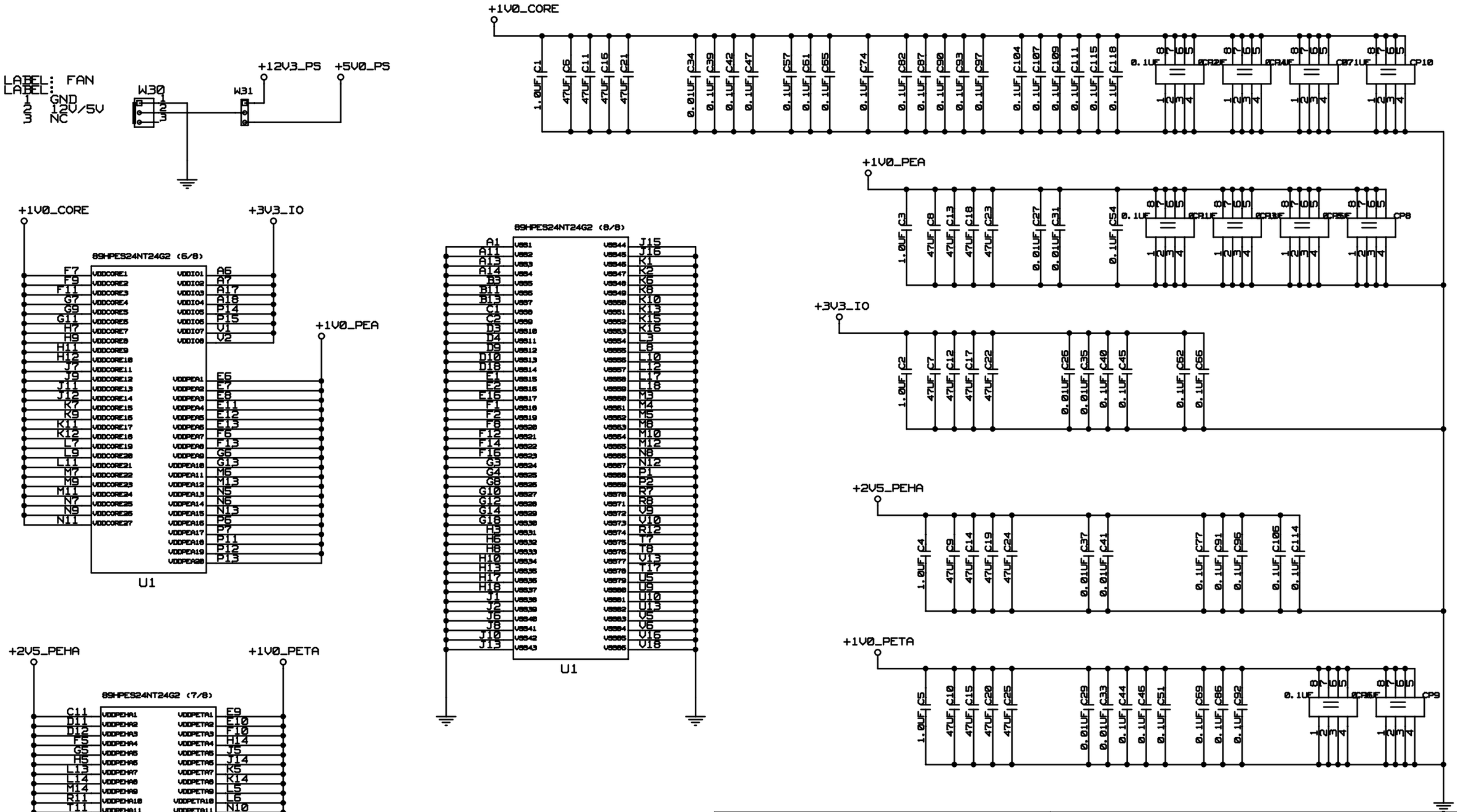
U1

89HPES24NT24G2 (8/8)

U1

89HPES24NT24G2 (7/8)

U1



TITLE EB-LOGAN-19

24NT24G2 - POWER

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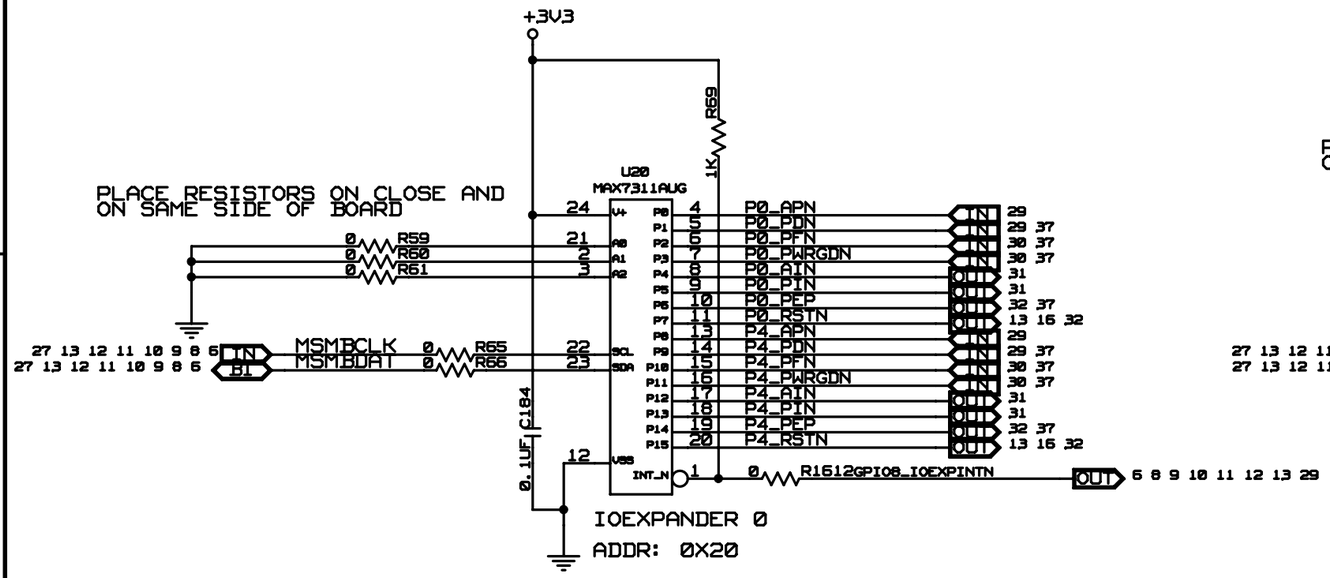

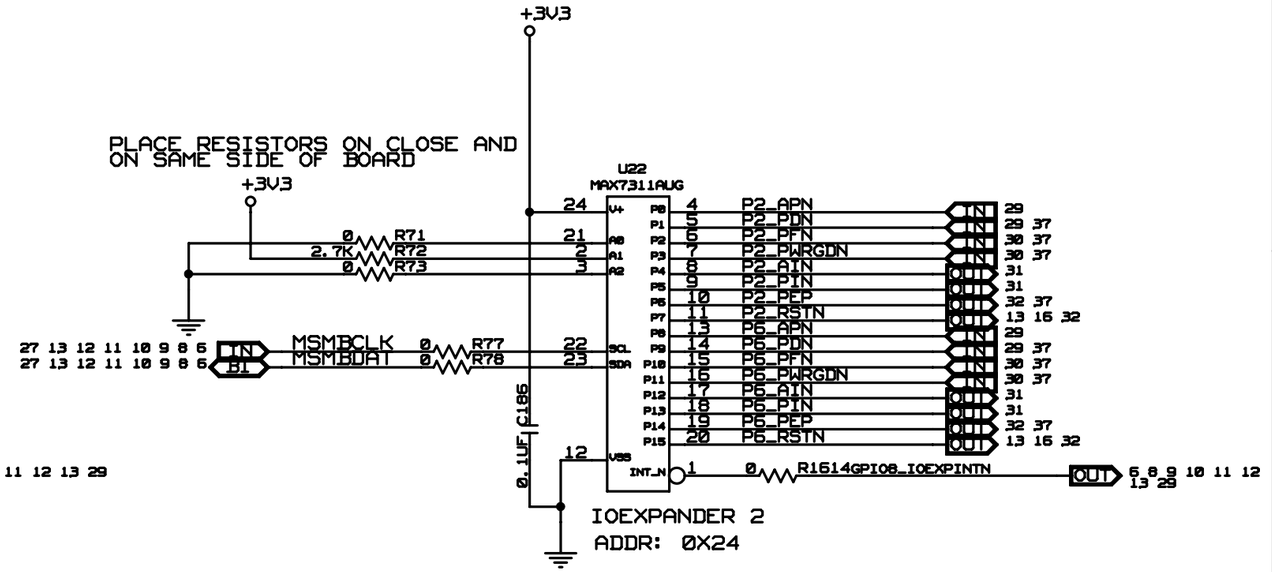

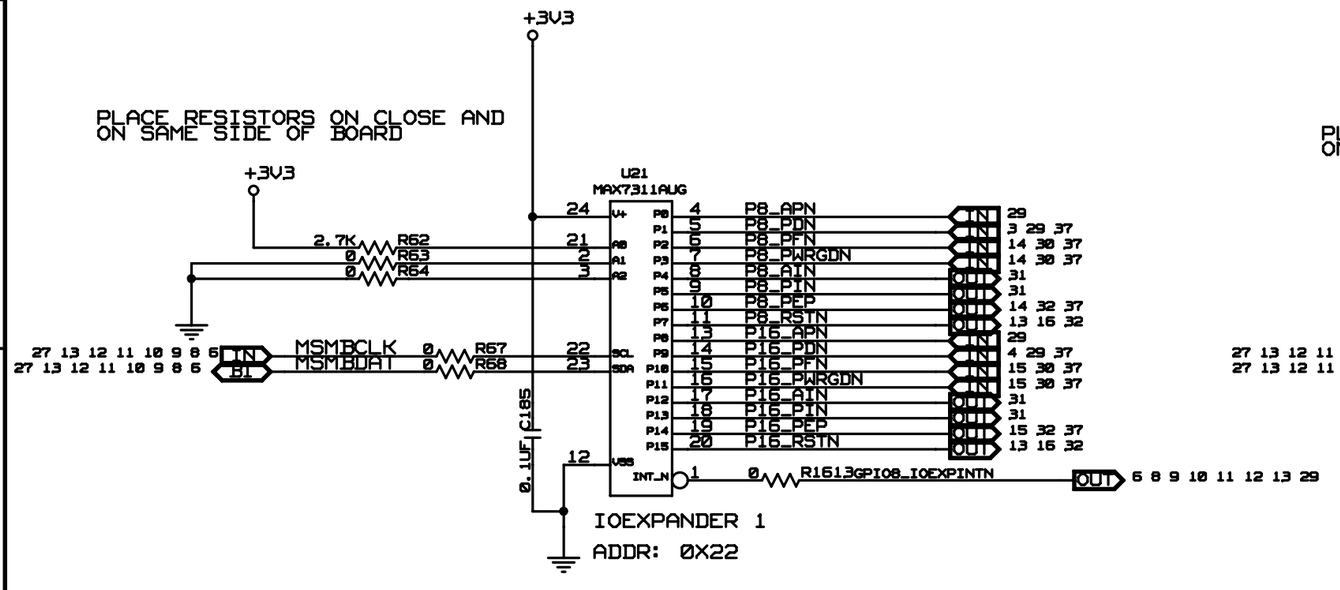

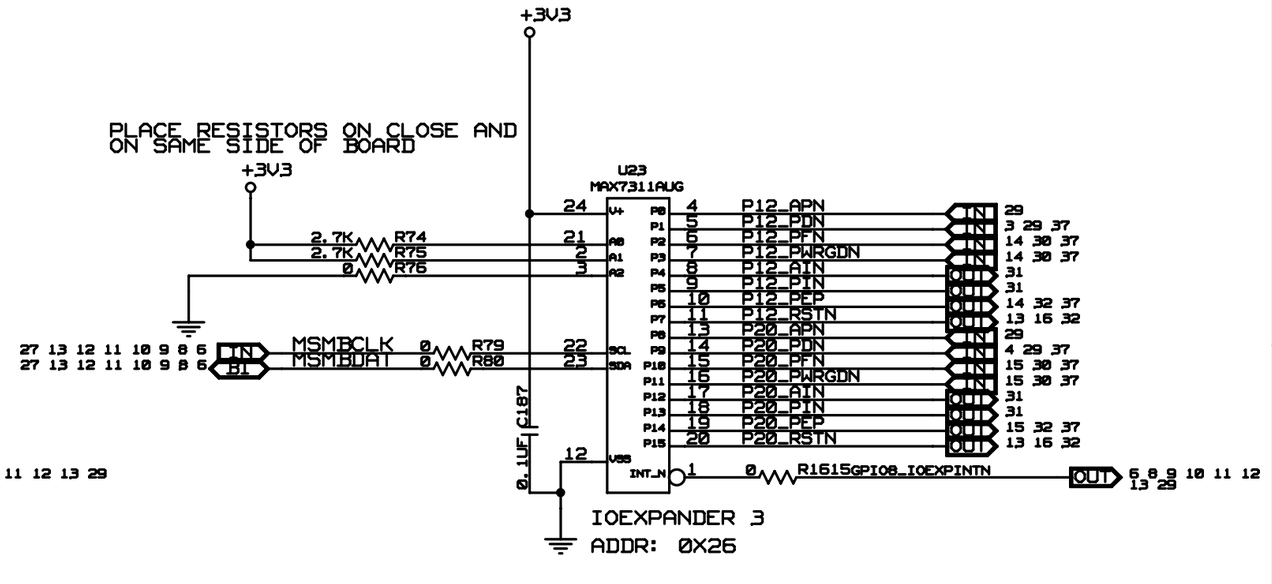

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IOEXPANDER 0-3

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

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PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

+3V3

U24 MAX7311AUG

0 R83
0 R84
2.7K R85

MSMBCLK 0 R89
MSMBDAT 0 R90

27 13 12 11 10 9 8 6 DIN
27 13 12 11 10 9 8 6 BI

0.1UF C188

P0 4 P1_APN
P1 5 P1_PDN
P2 6 P1_PFN
P3 7 P1_PWRGDN
P4 8 P1_AIN
P5 9 P1_PIN
P6 10 P1_PEP
P7 11 P1_RSTN
P8 13 P3_APN
P9 14 P3_PDN
P10 15 P3_PFN
P11 16 P3_PWRGDN
P12 17 P3_AIN
P13 18 P3_PIN
P14 19 P3_PEP
P15 20 P3_RSTN

INT_N 1 0 R1616GPIO8_IOEXPINTN OUT 6 8 9 10 11 12 13 29

IOEXPANDER 4
ADDR: 0X28

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

+3V3

U26 MAX7311AUG

0 R95
2.7K R96
2.7K R97

MSMBCLK 0 R101
MSMBDAT 0 R102

27 13 12 11 10 9 8 6 DIN
27 13 12 11 10 9 8 6 BI

0.1UF C190

P0 4 P10_APN
P1 5 P10_PDN
P2 6 P10_PFN
P3 7 P10_PWRGDN
P4 8 P10_AIN
P5 9 P10_PIN
P6 10 P10_PEP
P7 11 P10_RSTN
P8 13 P14_APN
P9 14 P14_PDN
P10 15 P14_PFN
P11 16 P14_PWRGDN
P12 17 P14_AIN
P13 18 P14_PIN
P14 19 P14_PEP
P15 20 P14_RSTN

INT_N 1 0 R1618GPIO8_IOEXPINTN OUT 6 8 9 10 11 12 13 29

IOEXPANDER 6
ADDR: 0X2C

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

+3V3

U25 MAX7311AUG

2.7K R86
0 R87
2.7K R88

MSMBCLK 0 R91
MSMBDAT 0 R92

27 13 12 11 10 9 8 6 DIN
27 13 12 11 10 9 8 6 BI

0.1UF C189

P0 4 P5_APN
P1 5 P5_PDN
P2 6 P5_PFN
P3 7 P5_PWRGDN
P4 8 P5_AIN
P5 9 P5_PIN
P6 10 P5_PEP
P7 11 P5_RSTN
P8 13 P7_APN
P9 14 P7_PDN
P10 15 P7_PFN
P11 16 P7_PWRGDN
P12 17 P7_AIN
P13 18 P7_PIN
P14 19 P7_PEP
P15 20 P7_RSTN

INT_N 1 0 R1617GPIO8_IOEXPINTN OUT 6 8 9 10 11 12 13 29

IOEXPANDER 5
ADDR: 0X2A

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

+3V3

U27 MAX7311AUG

2.7K R98
2.7K R99
2.7K R100

MSMBCLK 0 R103
MSMBDAT 0 R104

27 13 12 11 10 9 8 6 DIN
27 13 12 11 10 9 8 6 BI

0.1UF C191

P0 4 P18_APN
P1 5 P18_PDN
P2 6 P18_PFN
P3 7 P18_PWRGDN
P4 8 P18_AIN
P5 9 P18_PIN
P6 10 P18_PEP
P7 11 P18_RSTN
P8 13 P22_APN
P9 14 P22_PDN
P10 15 P22_PFN
P11 16 P22_PWRGDN
P12 17 P22_AIN
P13 18 P22_PIN
P14 19 P22_PEP
P15 20 P22_RSTN

INT_N 1 0 R1619GPIO8_IOEXPINTN OUT 6 8 9 10 11 12 13 29

IOEXPANDER 7
ADDR: 0X2E

TITLE EB-LOGAN-19

IOEXPANDER 4-7

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

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Tony Tran	Derek Huang

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PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

+3V3

U28 MAX7311AUG

R107 0
R108 0
R109 0
R113 0
R114 0
R1620GPIO8_IOEXPINTN 0

MSMBCLK
MSMBDAT

27 13 12 11 10 9 8 6 IN
27 13 12 11 10 9 8 6 BI

4	P8	P9_APN
5	P1	P9_PDN
6	P2	P9_PFN
7	P3	P9_PWRGDN
8	P4	P9_AIN
9	P5	P9_PIN
10	P6	P9_PEP
11	P7	P9_RSTN
13	P8	P11_APN
14	P9	P11_PDN
15	P10	P11_PFN
16	P11	P11_PWRGDN
17	P12	P11_AIN
18	P13	P11_PIN
19	P14	P11_PEP
20	P15	P11_RSTN

24 V+ 21 A0 2 A1 3 A2 22 SCL 23 SDA 12 VSS 1 INT_N

C192 0.1UF

OUT: 29 | 29 37 | 30 37 | 30 37 | 31 | 31 | 32 37 | 13 16 32 | 29 | 29 37 | 30 37 | 30 37 | 31 | 31 | 32 37 | 13 16 32

OUT: 6 8 9 10 11 12 13 29

IOEXPANDER 8
ADDR: 0X50

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

+3V3

U30 MAX7311AUG

R119 0
R120 2.7K
R121 0
R125 0
R126 0
R1622GPIO8_IOEXPINTN 0

MSMBCLK
MSMBDAT

27 13 12 11 10 9 8 6 IN
27 13 12 11 10 9 8 6 BI

4	P8	P17_APN
5	P1	P17_PDN
6	P2	P17_PFN
7	P3	P17_PWRGDN
8	P4	P17_AIN
9	P5	P17_PIN
10	P6	P17_PEP
11	P7	P17_RSTN
13	P8	P19_APN
14	P9	P19_PDN
15	P10	P19_PFN
16	P11	P19_PWRGDN
17	P12	P19_AIN
18	P13	P19_PIN
19	P14	P19_PEP
20	P15	P19_RSTN

24 V+ 21 A0 2 A1 3 A2 22 SCL 23 SDA 12 VSS 1 INT_N

C194 0.1UF

OUT: 29 | 29 37 | 30 37 | 30 37 | 31 | 31 | 32 37 | 13 16 32 | 29 | 29 37 | 30 37 | 30 37 | 31 | 31 | 32 37 | 13 16 32

OUT: 6 8 9 10 11 12 13

IOEXPANDER 10
ADDR: 0X54

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

+3V3

U29 MAX7311AUG

R110 0
R111 0
R112 0
R115 0
R116 0
R1621GPIO8_IOEXPINTN 0

MSMBCLK
MSMBDAT

27 13 12 11 10 9 8 6 IN
27 13 12 11 10 9 8 6 BI

4	P8	P13_APN
5	P1	P13_PDN
6	P2	P13_PFN
7	P3	P13_PWRGDN
8	P4	P13_AIN
9	P5	P13_PIN
10	P6	P13_PEP
11	P7	P13_RSTN
13	P8	P15_APN
14	P9	P15_PDN
15	P10	P15_PFN
16	P11	P15_PWRGDN
17	P12	P15_AIN
18	P13	P15_PIN
19	P14	P15_PEP
20	P15	P15_RSTN

24 V+ 21 A0 2 A1 3 A2 22 SCL 23 SDA 12 VSS 1 INT_N

C193 0.1UF

OUT: 29 | 29 37 | 30 37 | 30 37 | 31 | 31 | 32 37 | 13 16 32 | 29 | 29 37 | 30 37 | 30 37 | 31 | 31 | 32 37 | 13 16 32

OUT: 6 8 9 10 11 12 13 29

IOEXPANDER 9
ADDR: 0X52

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

+3V3

U31 MAX7311AUG

R122 0
R123 2.7K
R124 0
R127 0
R128 0
R1623GPIO8_IOEXPINTN 0

MSMBCLK
MSMBDAT

27 13 12 11 10 9 8 6 IN
27 13 12 11 10 9 8 6 BI

4	P8	P21_APN
5	P1	P21_PDN
6	P2	P21_PFN
7	P3	P21_PWRGDN
8	P4	P21_AIN
9	P5	P21_PIN
10	P6	P21_PEP
11	P7	P21_RSTN
13	P8	P23_APN
14	P9	P23_PDN
15	P10	P23_PFN
16	P11	P23_PWRGDN
17	P12	P23_AIN
18	P13	P23_PIN
19	P14	P23_PEP
20	P15	P23_RSTN

24 V+ 21 A0 2 A1 3 A2 22 SCL 23 SDA 12 VSS 1 INT_N

C195 0.1UF

OUT: 29 | 29 37 | 30 37 | 30 37 | 31 | 31 | 32 37 | 13 16 32 | 29 | 29 37 | 30 37 | 30 37 | 31 | 31 | 32 37 | 13 16 32

OUT: 6 8 9 10 11 12 13

IOEXPANDER 11
ADDR: 0X56

TITLE EB-LOGAN-19

IOEXPANDER 8-11

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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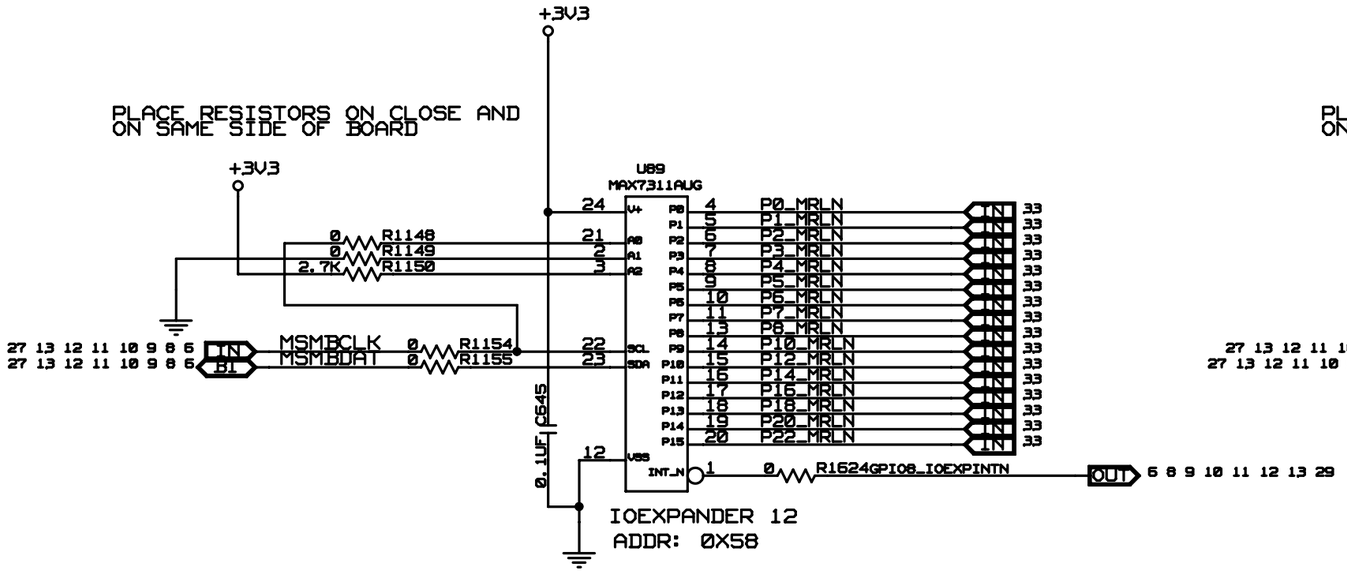
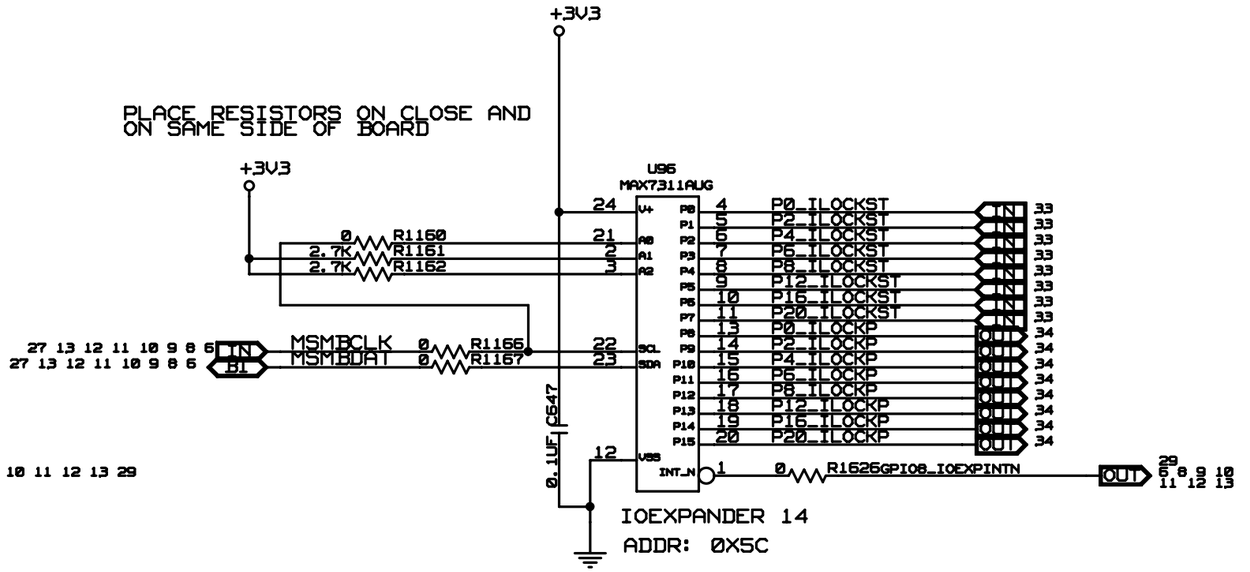
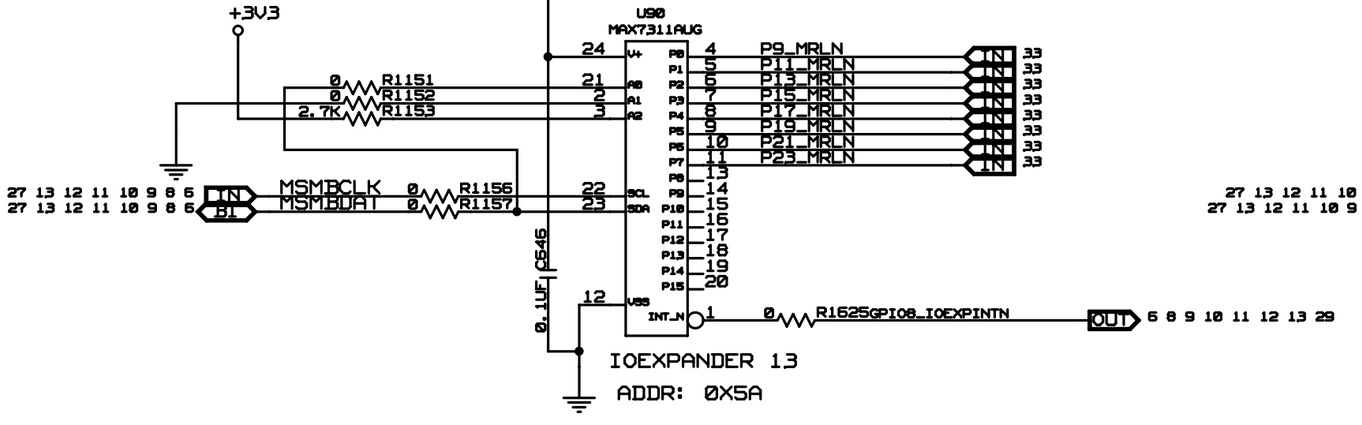
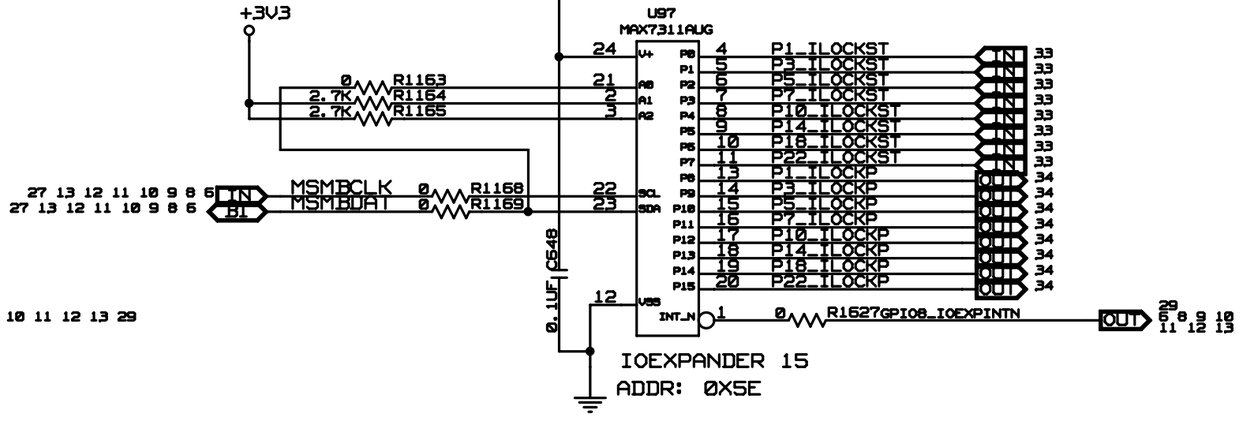
PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD





PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD





TITLE EB-LOGAN-19

IOEXPANDER 12-15

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD

+3V3

U85
MAX7311AUG

R1124 0
R1125 0
R1126 0

MSMBCLK R1130 0
MSMBDAT R1131 0

27 13 12 11 10 9 8 6 DIN
27 13 12 11 10 9 8 6 BI

C541 0.1UF

P9_ILOCKST
P11_ILOCKST
P13_ILOCKST
P15_ILOCKST
P17_ILOCKST
P19_ILOCKST
P21_ILOCKST
P23_ILOCKST
P9_ILOCKP
P11_ILOCKP
P13_ILOCKP
P15_ILOCKP
P17_ILOCKP
P19_ILOCKP
P21_ILOCKP
P23_ILOCKP

R1628GPIO8_IOEXPINTN

OUT 6 8 9 10 11 13 29

IOEXPANDER 16
ADDR: 0XB0

PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD

+3V3

U87
MAX7311AUG

R1136 0
R1137 0
R1138 0

MSMBCLK R1142 0
MSMBDAT R1143 0

27 13 12 11 10 9 8 6 DIN
27 13 12 11 10 9 8 6 BI

C543 0.1UF

P0_ACTIVEN
P1_ACTIVEN
P2_ACTIVEN
P3_ACTIVEN
P4_ACTIVEN
P5_ACTIVEN
P6_ACTIVEN
P7_ACTIVEN
P8_ACTIVEN
P9_ACTIVEN
P10_ACTIVEN
P11_ACTIVEN
P12_ACTIVEN
P13_ACTIVEN
P14_ACTIVEN
P15_ACTIVEN

IOEXPANDER 18
ADDR: 0XA4

PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD

+3V3

U86
MAX7311AUG

2.7K R1127
R1128 0
R1129 0

MSMBCLK R1132 0
MSMBDAT R1133 0

27 13 12 11 10 9 8 6 DIN
27 13 12 11 10 9 8 6 BI

C542 0.1UF

P0_LINKUPN
P1_LINKUPN
P2_LINKUPN
P3_LINKUPN
P4_LINKUPN
P5_LINKUPN
P6_LINKUPN
P7_LINKUPN
P8_LINKUPN
P9_LINKUPN
P10_LINKUPN
P11_LINKUPN
P12_LINKUPN
P13_LINKUPN
P14_LINKUPN
P15_LINKUPN

IOEXPANDER 17
ADDR: 0XA2

PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD

+3V3

U88
MAX7311AUG

2.7K R1139
R1140 0
R1141 0

MSMBCLK R1144 0
MSMBDAT R1145 0

27 13 12 11 10 9 8 6 DIN
27 13 12 11 10 9 8 6 BI

C544 0.1UF

P16_LINKUPN
P17_LINKUPN
P18_LINKUPN
P19_LINKUPN
P20_LINKUPN
P21_LINKUPN
P22_LINKUPN
P23_LINKUPN
P16_ACTIVEN
P17_ACTIVEN
P18_ACTIVEN
P19_ACTIVEN
P20_ACTIVEN
P21_ACTIVEN
P22_ACTIVEN
P23_ACTIVEN

IOEXPANDER 19
ADDR: 0XA6

TITLE EB-LOGAN-19

IOEXPANDER 16-19

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
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PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD

+3V3

U83
MAX7311AUG

R131 0
R132 0
R133 0

27 13 12 11 10 9 8 6 → IN
27 13 12 11 10 9 8 6 ← BI

MSMBCLK 0 R137
MSMBDAT 0 R138

C196 0.1UF

Pin		Net
24	V+	
21	A0	
2	A1	
3	A2	
22	SCL	
23	SDA	
12	VSS	
1	INT_N	R163 0 3GPIO8_IOEXPINTN → OUT 6 8 9 10 11 12 29
4	P0	P0_RSTN
5	P1	P2_RSTN
6	P2	P4_RSTN
7	P3	P6_RSTN
8	P4	P8_RSTN
9	P5	P12_RSTN
10	P6	P16_RSTN
11	P7	P20_RSTN
13	P8	PART0_PERSTN
14	P9	PART1_PERSTN
15	P10	PART2_PERSTN
16	P11	PART3_PERSTN
17	P12	PART4_PERSTN
18	P13	PART5_PERSTN
19	P14	PART6_PERSTN
20	P15	PART7_PERSTN

P0 P2 P4 P6 P8 P12 P16 P20 → OUT 8 16 32
PART0 PART1 PART2 PART3 PART4 PART5 PART6 PART7 → IN 34 38

IOEXPANDER 20

ADDR: 0XA8

+3V3

PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD

+3V3

U84
MAX7311AUG

2.7K R134
R135 0
R136 0

27 13 12 11 10 9 8 6 → IN
27 13 12 11 10 9 8 6 ← BI

MSMBCLK 0 R139
MSMBDAT 0 R140

C197 0.1UF

Pin		Net
24	V+	
21	A0	
2	A1	
3	A2	
22	SCL	
23	SDA	
12	VSS	
1	INT_N	
4	P0	P1_RSTN
5	P1	P3_RSTN
6	P2	P5_RSTN
7	P3	P7_RSTN
8	P4	P9_RSTN
9	P5	P10_RSTN
10	P6	P11_RSTN
11	P7	P13_RSTN
13	P8	P14_RSTN
14	P9	P15_RSTN
15	P10	P17_RSTN
16	P11	P18_RSTN
17	P12	P19_RSTN
18	P13	P21_RSTN
19	P14	P22_RSTN
20	P15	P23_RSTN

P1 P3 P5 P7 P9 P10 P11 P13 P14 P15 P17 P18 P19 P21 P22 P23 → OUT 9 16 32 / 10 16 32

IOEXPANDER 21

ADDR: 0XAA

TITLE EB-LOGAN-19

IOEXPANDER 20-21

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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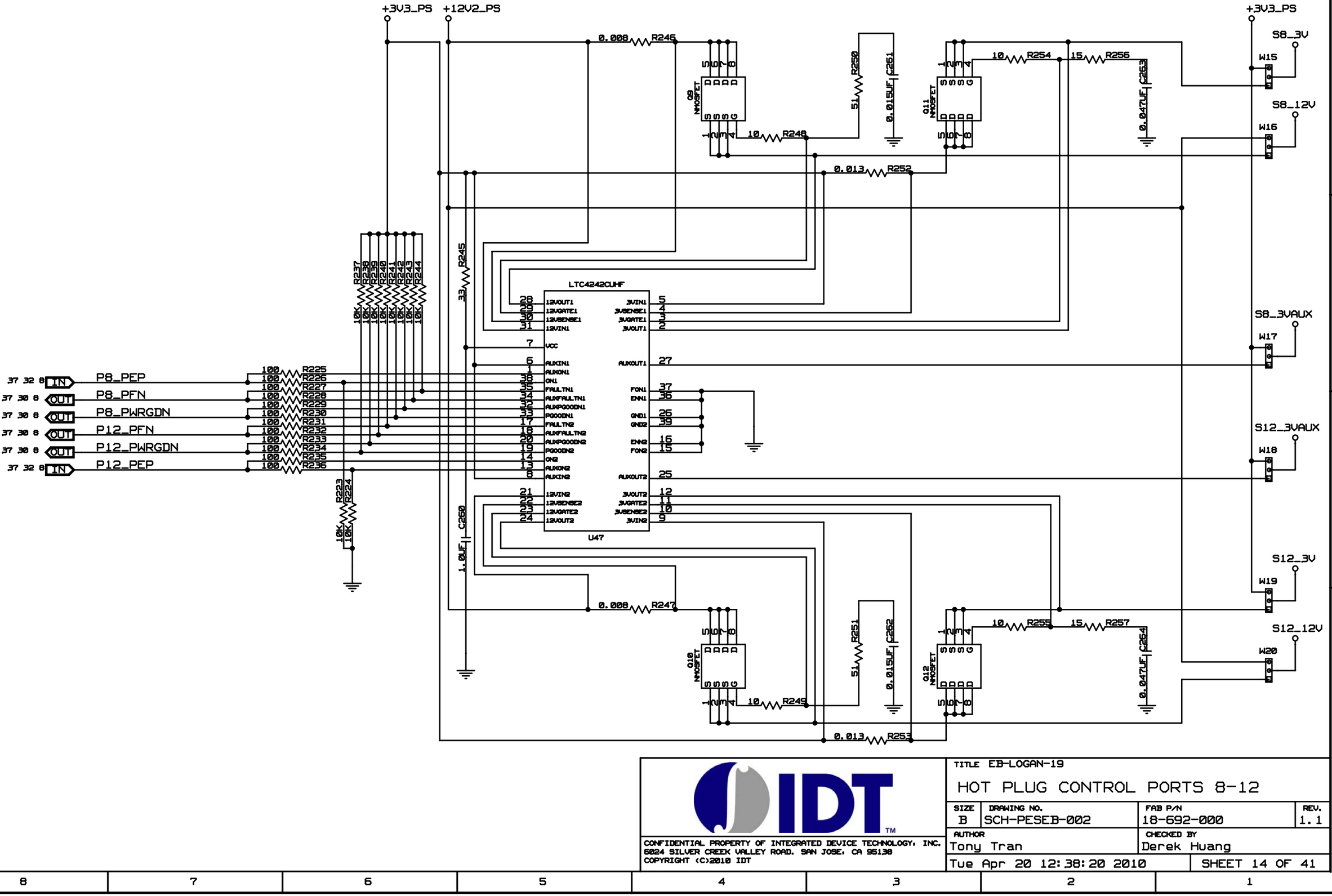

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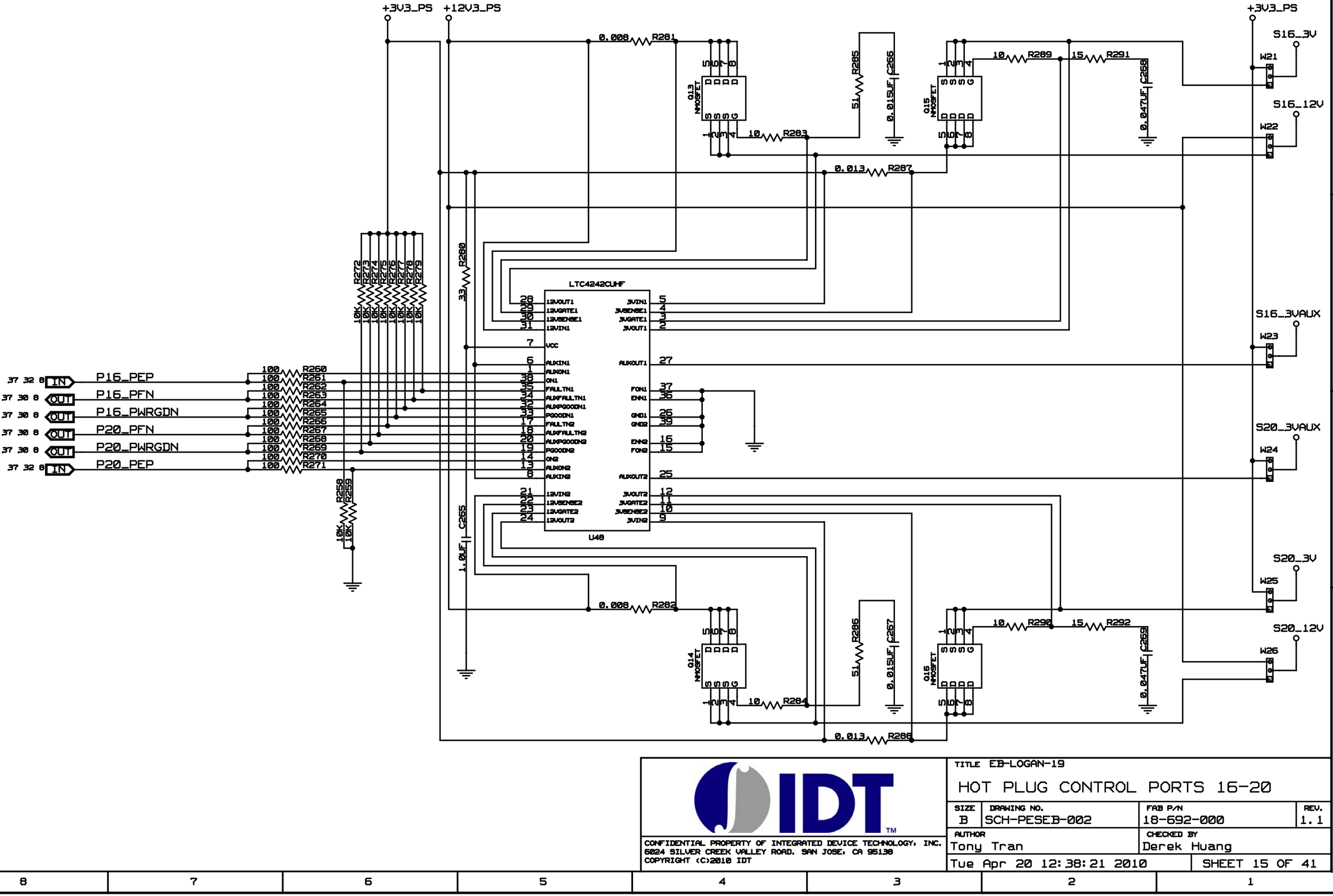
TITLE EB-LOGAN-19

HOT PLUG CONTROL PORTS 8-12

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1
AUTHOR: Tony Tran		CHECKED BY: Derek Huang	
Tue Apr 20 12:38:20 2010		SHEET 14 OF 41	



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TITLE EB-LOGAN-19

HOT PLUG CONTROL PORTS 16-20

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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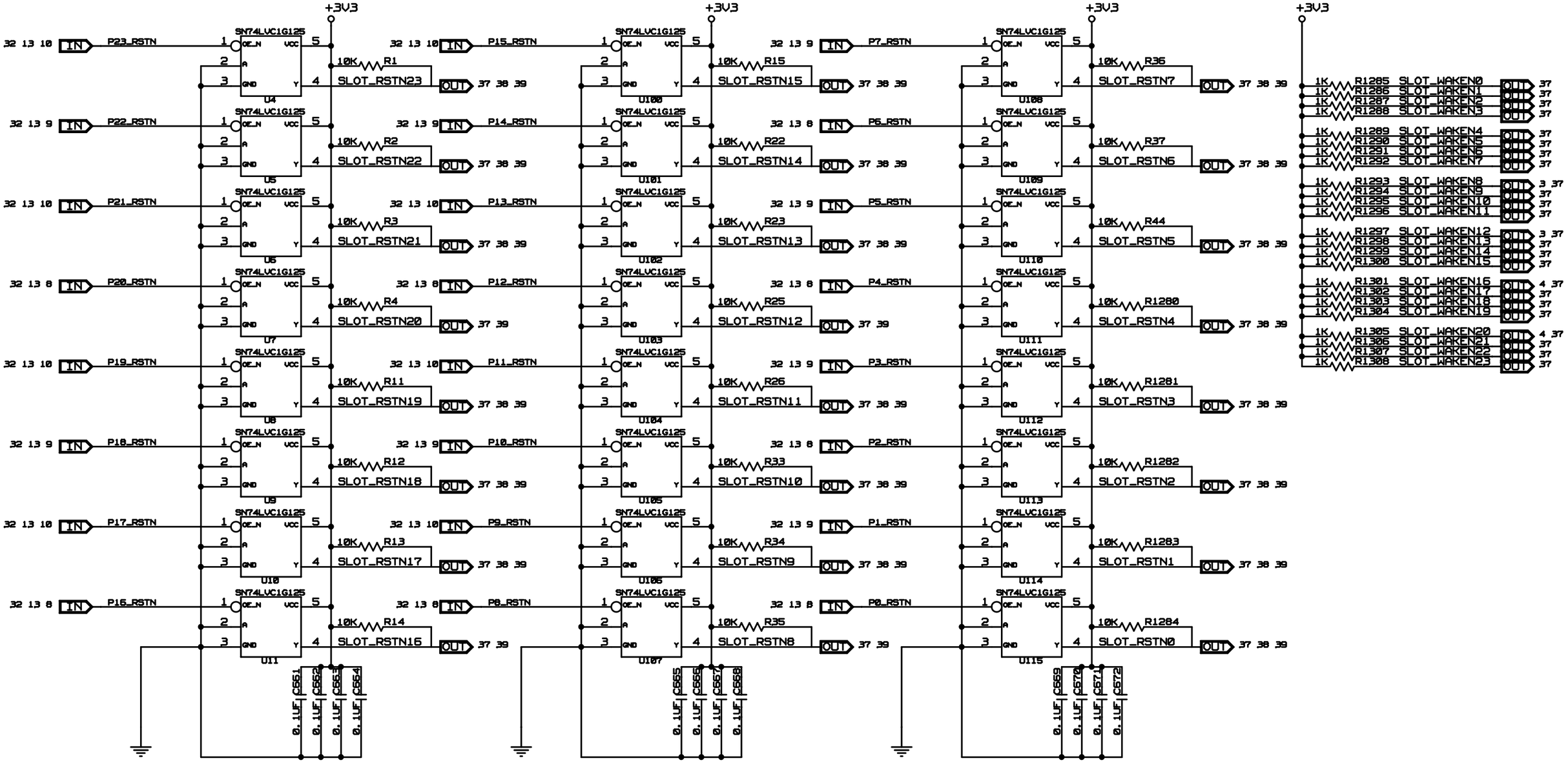

TITLE EB-LOGAN-19

SLOT RESETS AND WAKE PULL-UPS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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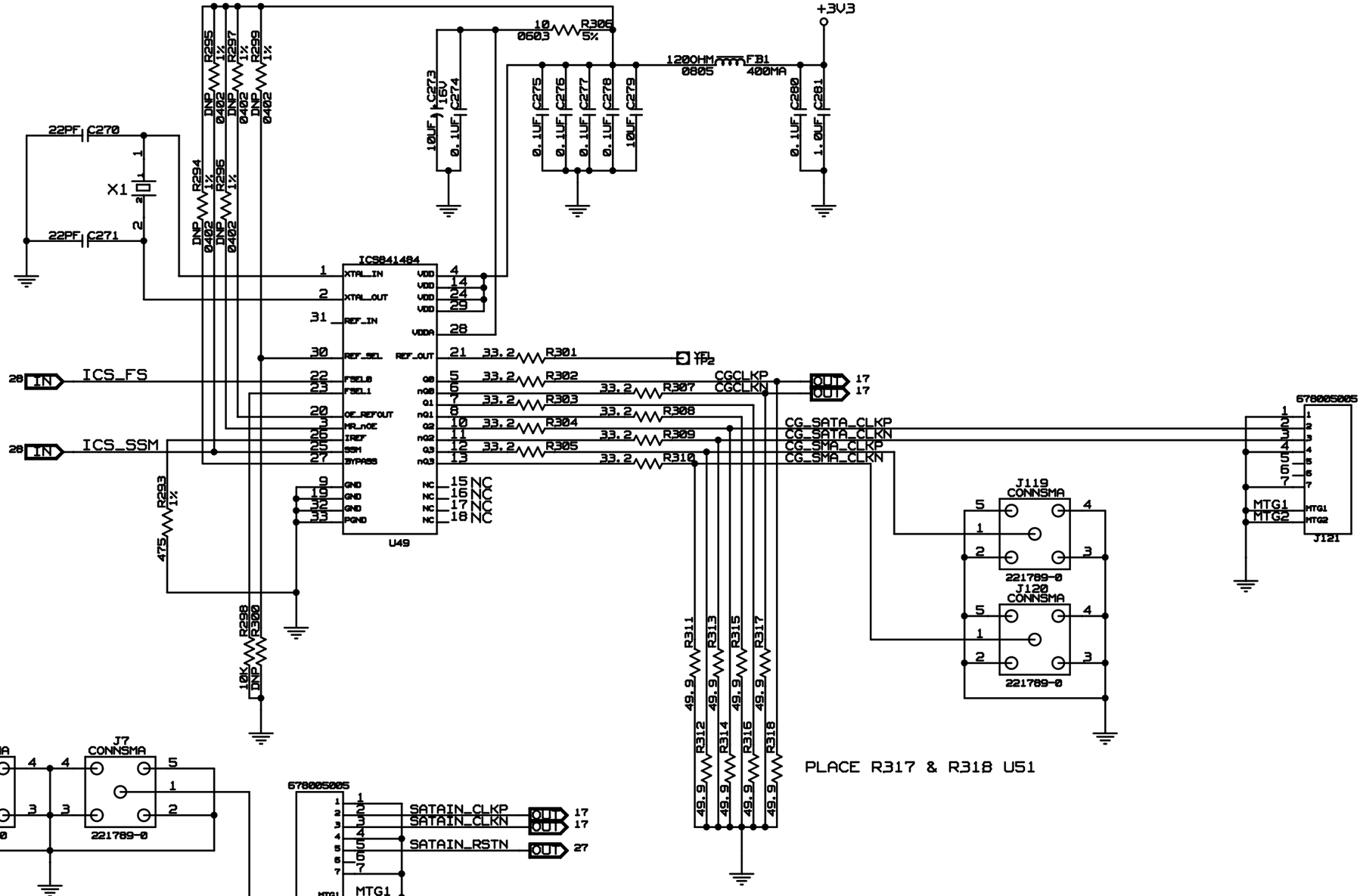

TITLE EB-LOGAN-19			
CLOCK			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-000	REV. 1.1
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Tue Apr 20 12:38:21 2010		SHEET 17 OF 41	

SILKSCREEN LABEL:
SWITCH_S11
POS DESCRIPTION
1 P8_CLK_EN
2 P12_CLK_EN
3 P16_CLK_EN
4 P20_CLK_EN

S11
SM_SW4

P8_CLK_EN
P12_CLK_EN
P16_CLK_EN
P20_CLK_EN

+3V3
600OHM/FB2 0805 500MA
C282 1.0UF C283 0.1UF
C285 10UF C286 0.1UF C287 0.1UF C288 0.1UF C289 0.1UF C290 0.1UF
2.2 R333 1%
C291 1.0UF C292 0.1UF

R320 10.0K R321 10.0K R322 10.0K R324 DNP R326 10.0K R328 DNP
R323 DNP R325 10.0K R327 DNP R329 10.0K

U50
IC99DB803

VDD 2 19 39
VDD 11 31 48
VDDA

17 IN MAIN_CLKP
17 IN MAIN_CLKN
SRC_IN 4
SRC_IN# 5

OE0# 6
OE1# 14
OE2# 15
OE3# 7
OE4# 43
OE5# 35
OE6# 36
OE7# 44
OE_INV=1

DIFF_STOP 27
PD 26
HIGH_BW# 28
OE_INV 40
BYPASS#/PLL 22
SCLK 23
SDATA 24
SRC_DIV# 1
GND 3 10 18

LOCK 45
IREF 46
GNDA 47
GND 32 55

R332 475 1%

DIF_0 8 BGCLK0P_R 33.2 R334 → BGCLK0P OUT 19
DIF_0# 9 BGCLK0N_R 33.2 R335 → BGCLK0N OUT 19
DIF_1 12 BGCLK1P_R 33.2 R336 → BGCLK1P OUT 19
DIF_1# 13 BGCLK1N_R 33.2 R337 → BGCLK1N OUT 19
DIF_2 16 BS08CLKP_R 33.2 R338 → BS08CLKP OUT 20
DIF_2# 17 BS08CLKN_R 33.2 R339 → BS08CLKN OUT 20
DIF_3 20 BS12CLKP_R 33.2 R340 → BS12CLKP OUT 20
DIF_3# 21 BS12CLKN_R 33.2 R341 → BS12CLKN OUT 20
DIF_4 30 BS16CLKP_R 33.2 R342 → BS16CLKP OUT 20
DIF_4# 29 BS16CLKN_R 33.2 R343 → BS16CLKN OUT 20
DIF_5 34 BS20CLKP_R 33.2 R344 → BS20CLKP OUT 20
DIF_5# 33 BS20CLKN_R 33.2 R345 → BS20CLKN OUT 20
DIF_6 38 → SATAOUT_CLKP
DIF_6# 37 → SATAOUT_CLKN
DIF_7 42 SMAOUT_CLKP_R 33.2 R348 → SMAOUT_CLKP
DIF_7# 41 SMAOUT_CLKN_R 33.2 R349 → SMAOUT_CLKN

YB TPS

R350 49.9 R351 49.9
R354 49.9 R355 49.9 R356 49.9 R357 49.9 R358 49.9 R359 49.9 R360 49.9 R361 49.9 R362 49.9 R363 49.9 R364 49.9 R365 49.9

J122 CONNSMA 221789-0
J123 CONNSMA 221789-0

678005005 J124
MTG1 MTG2

+3V3
R1645 DNP R1648 DNP
R1647 49.9 R1649 49.9
33.2 C753 SATAOUT_CLKP
33.2 C754 SATAOUT_CLKN

TITLE EB-LOGAN-19
CLOCK BUFFER - 1

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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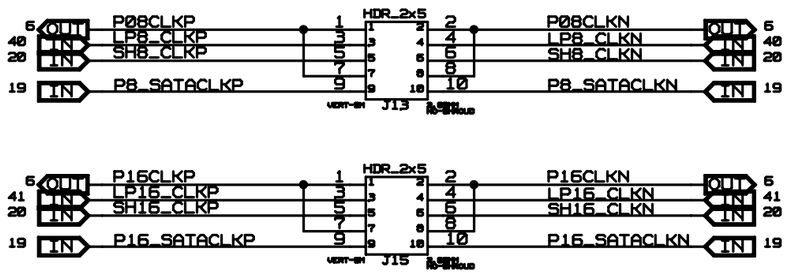
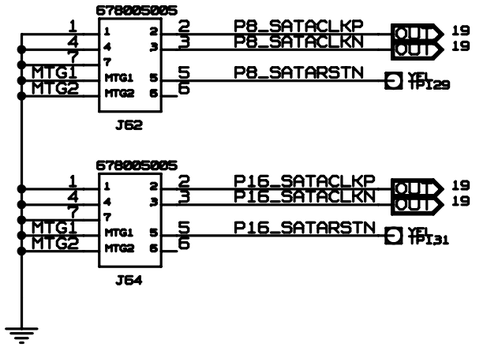
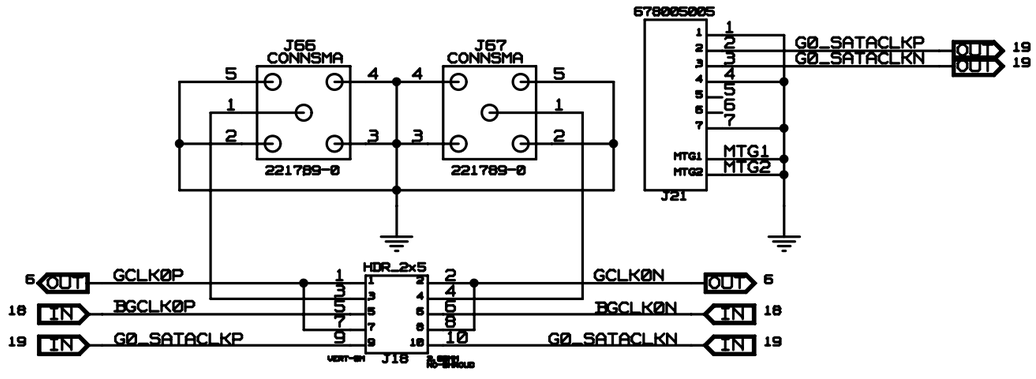
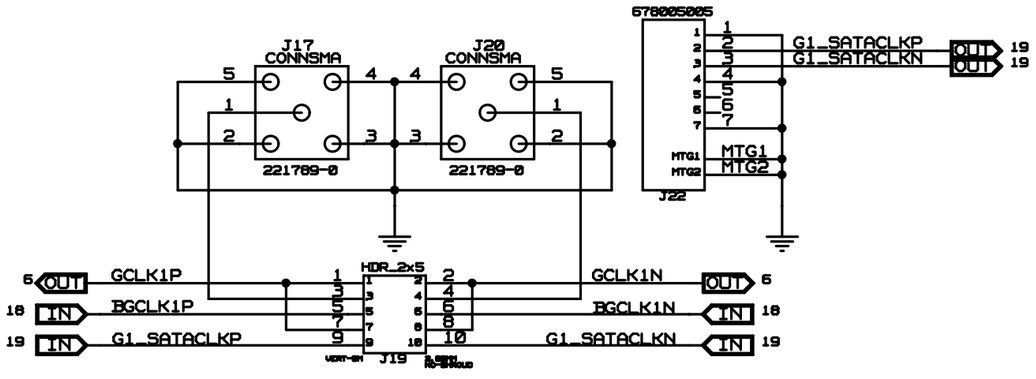
PXXCLK - DUT CLK
LPXXLCK - LOCAL CLOCK GEN. PORT CLK
SHXXCLK - SLOT HDR. CLK









TITLE EB-LOGAN-19

CLOCK SELECTOR DUT PCLK 8 & 16

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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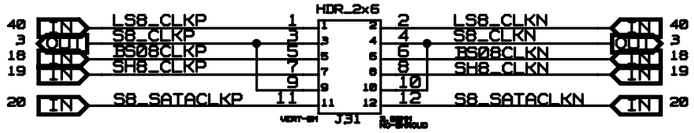
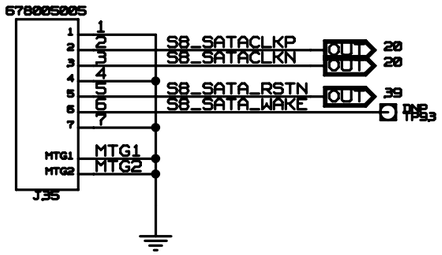
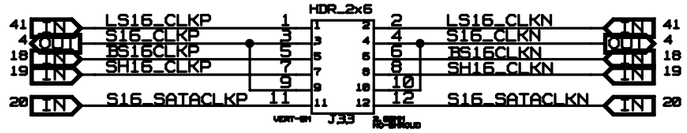
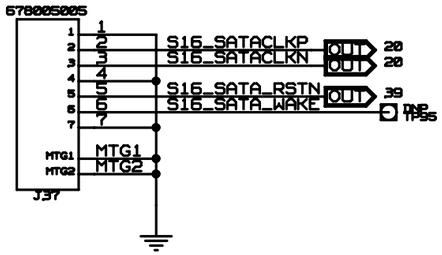
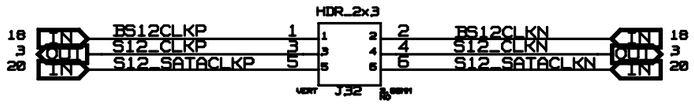
SXXCLK - SLOT CLK
BSXXLCK - BUFFER SLOT CLK
LSXXCLK - LOCAL CLOCK GEN. SLOT CLK
SHXXCLK - SLOT HDR.CLK

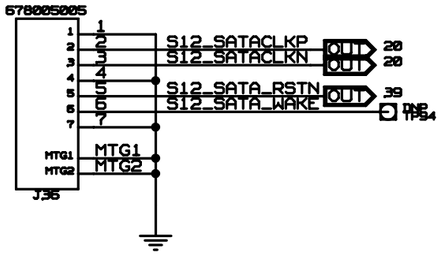


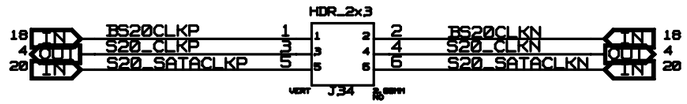


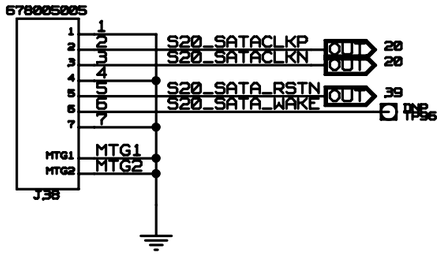












TITLE EB-LOGAN-19

CLOCK SELECTOR SLOTS 8-20

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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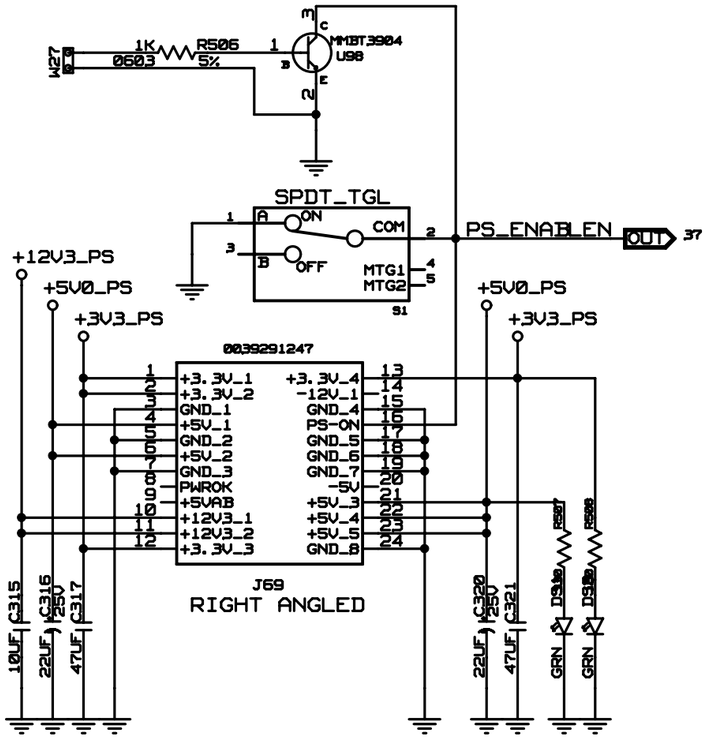

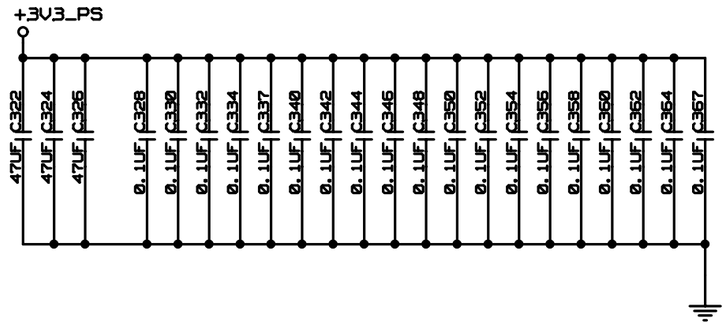

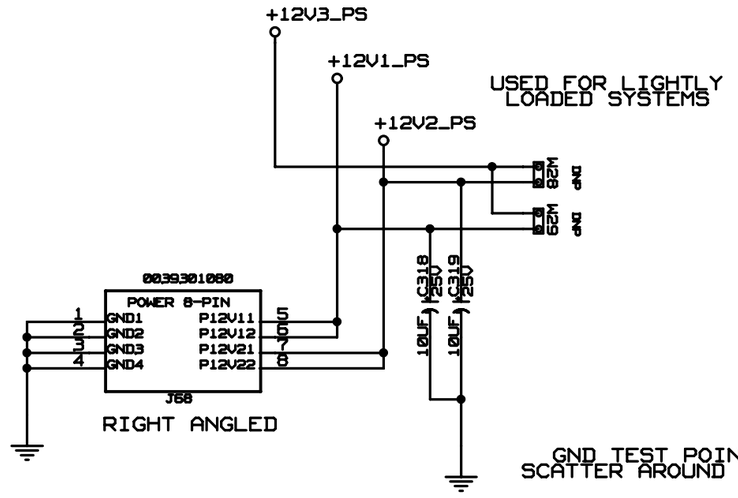

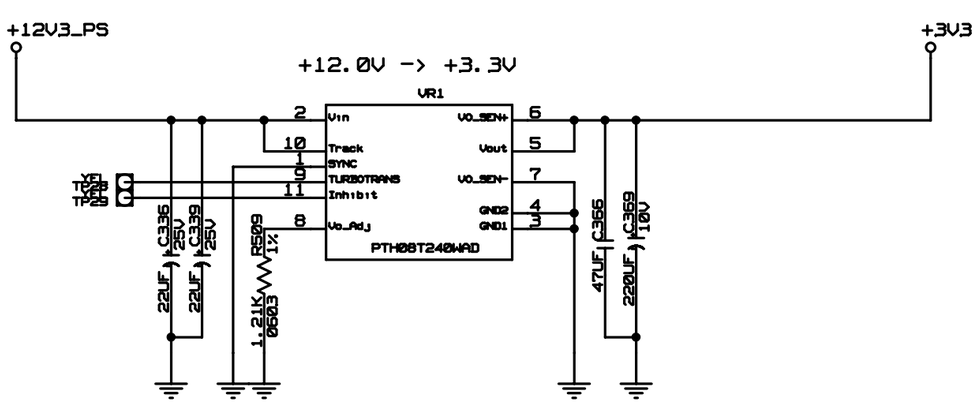

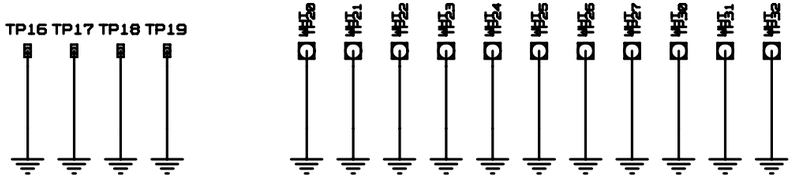

TITLE EB-LOGAN-19

POWER CONNECTORS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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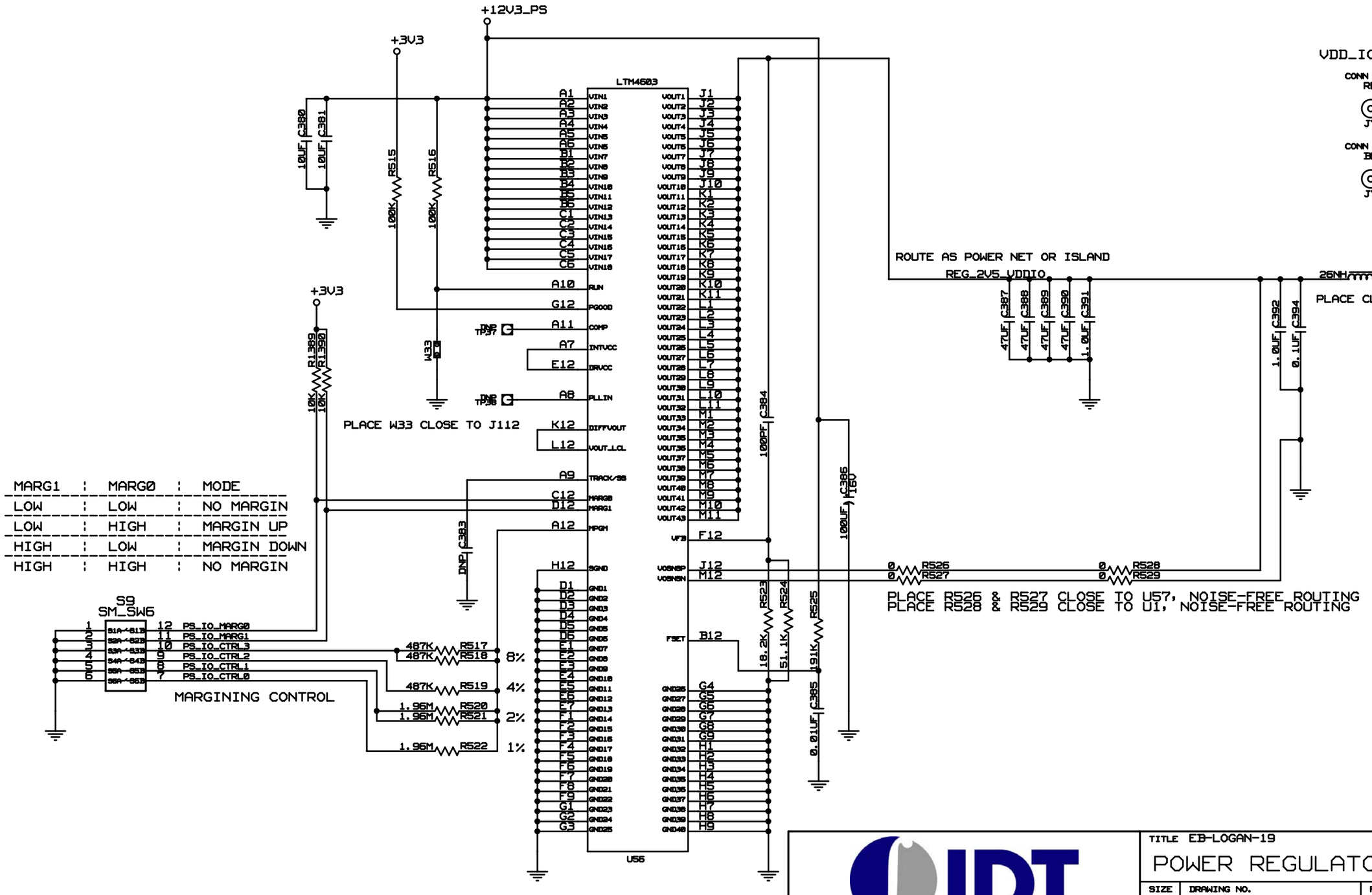

TITLE EB-LOGAN-19

POWER REGULATOR - VDDIO

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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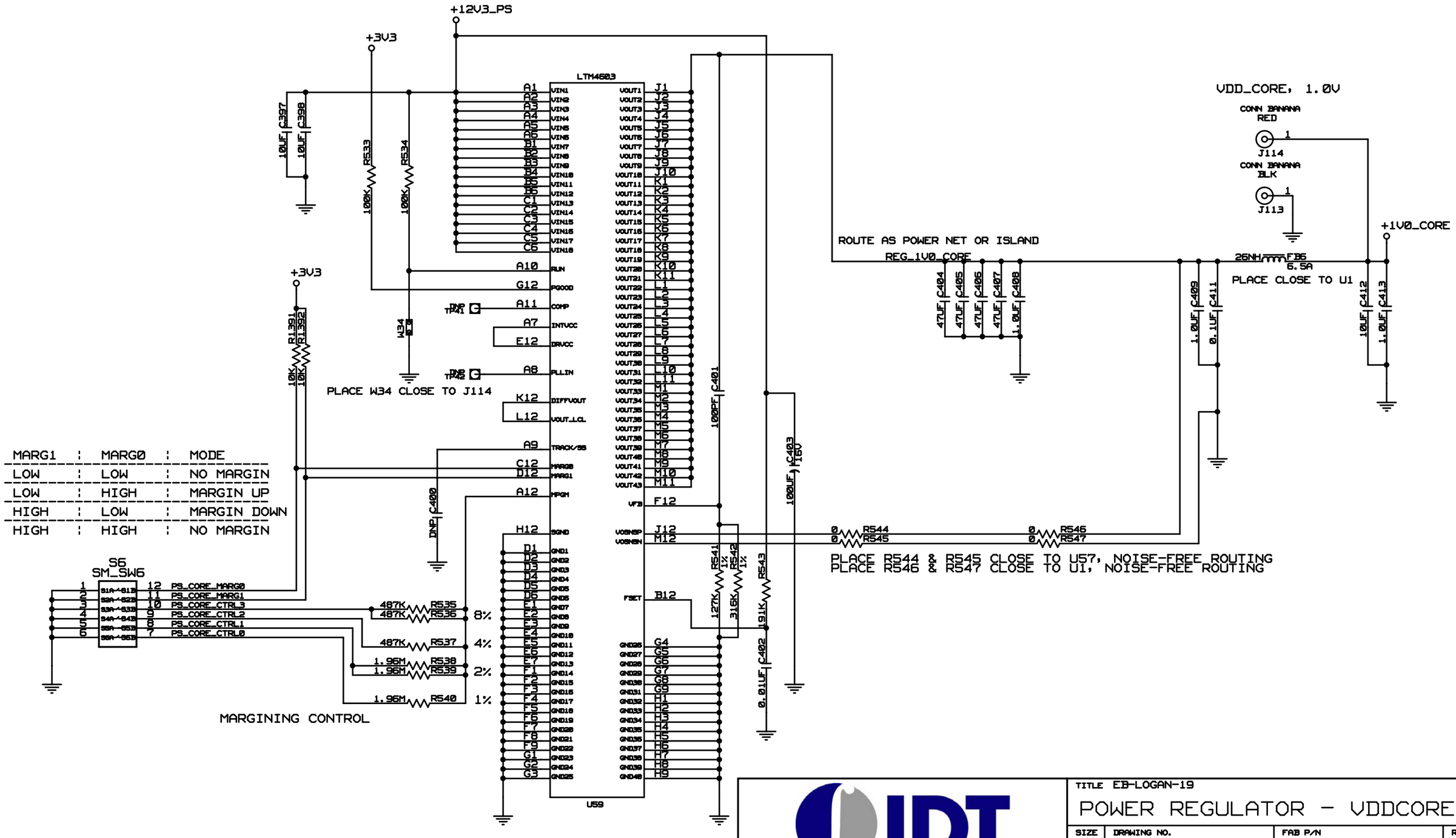

TITLE EB-LOGAN-19

POWER REGULATOR - VDDCORE

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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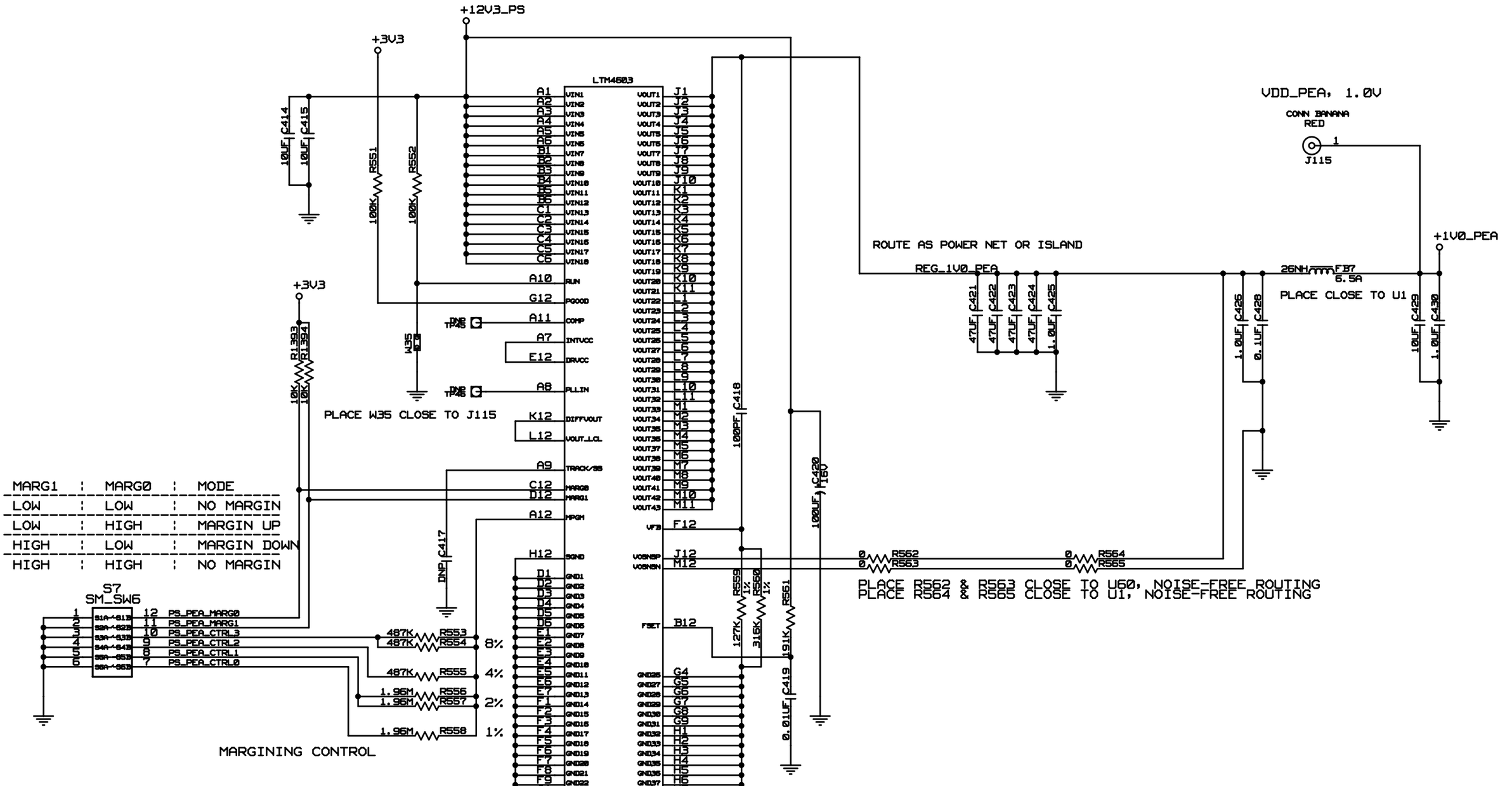

TITLE EB-LOGAN-19

POWER REGULATOR - VDDPEA

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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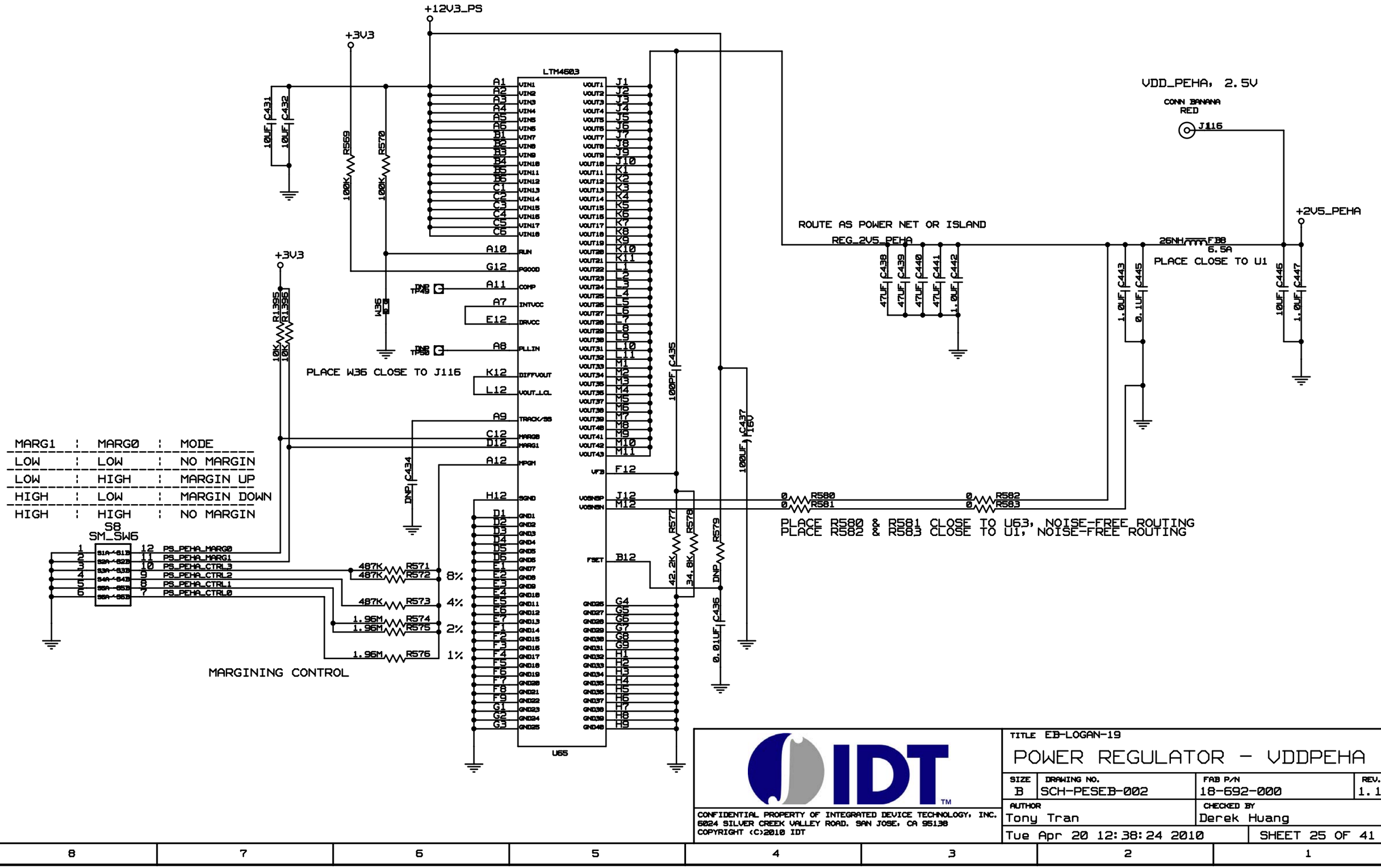

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TITLE EB-LOGAN-19

POWER REGULATOR - VDDPEHA

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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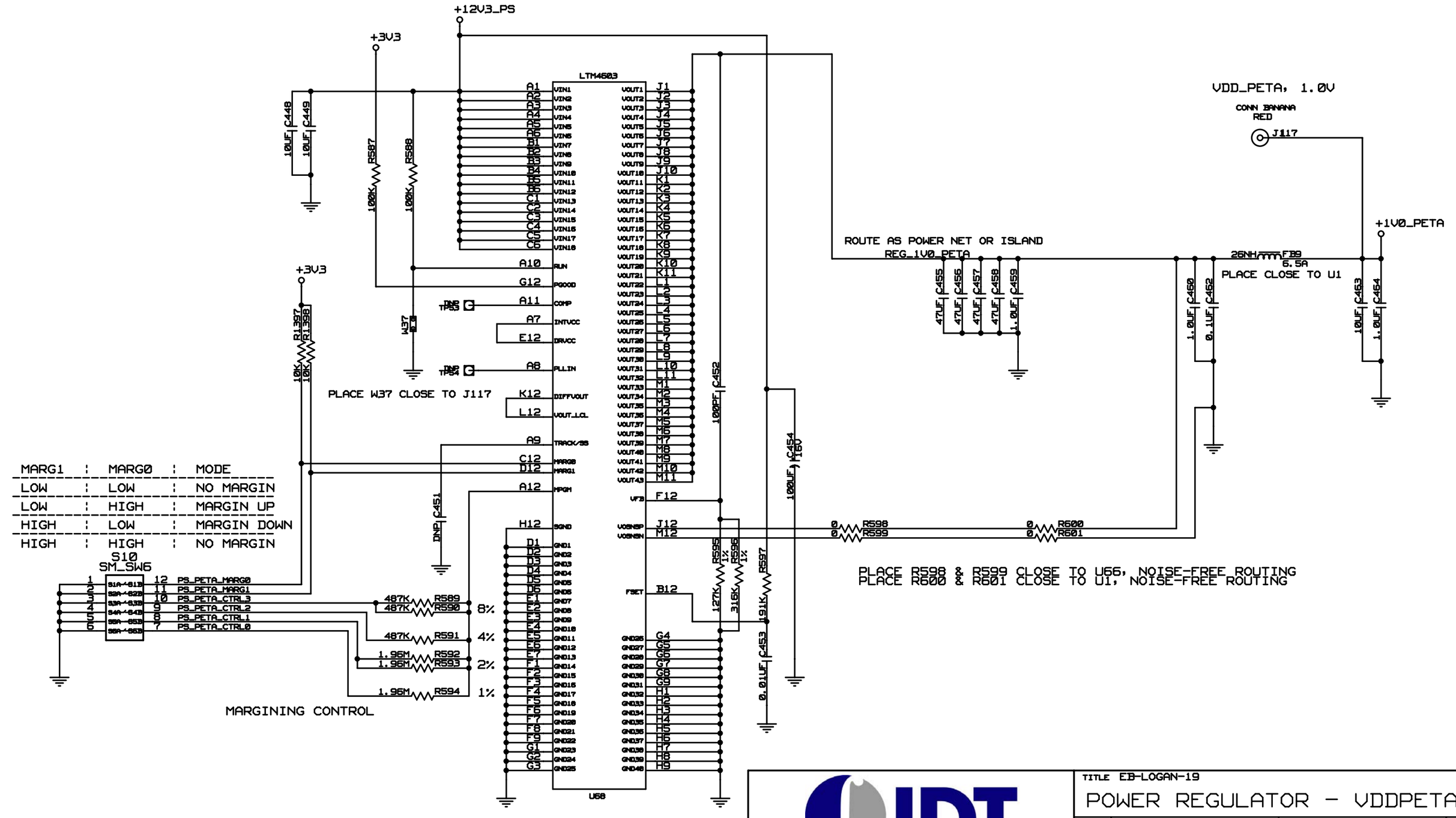


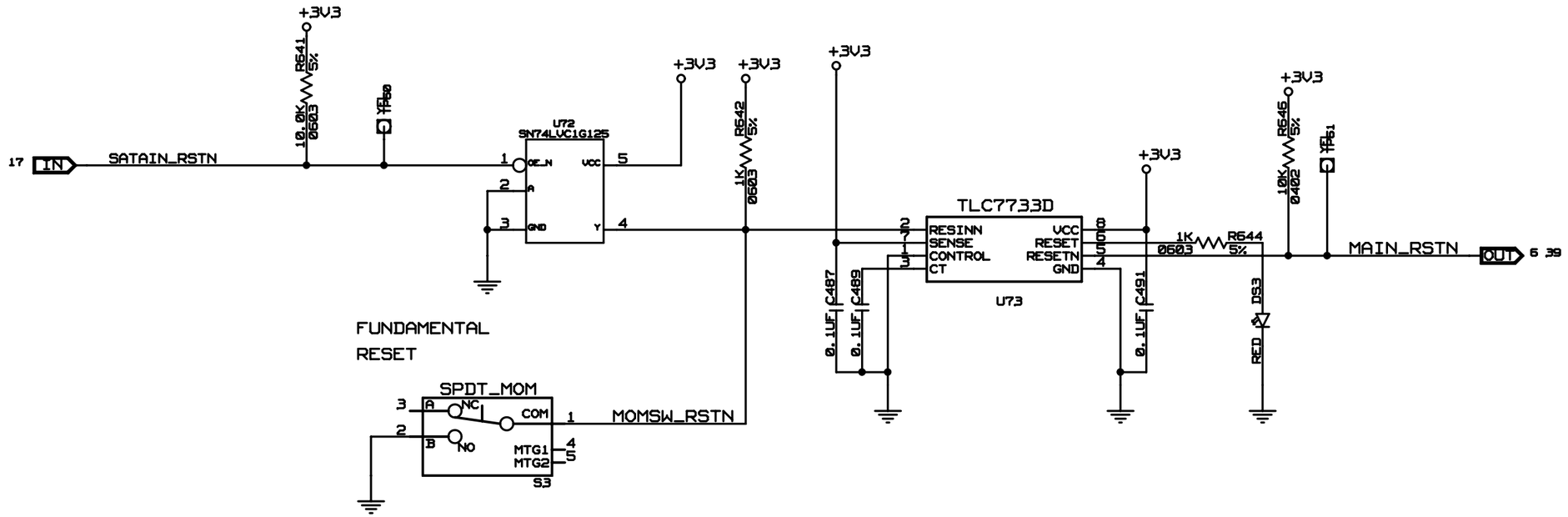
TITLE EB-LOGAN-19

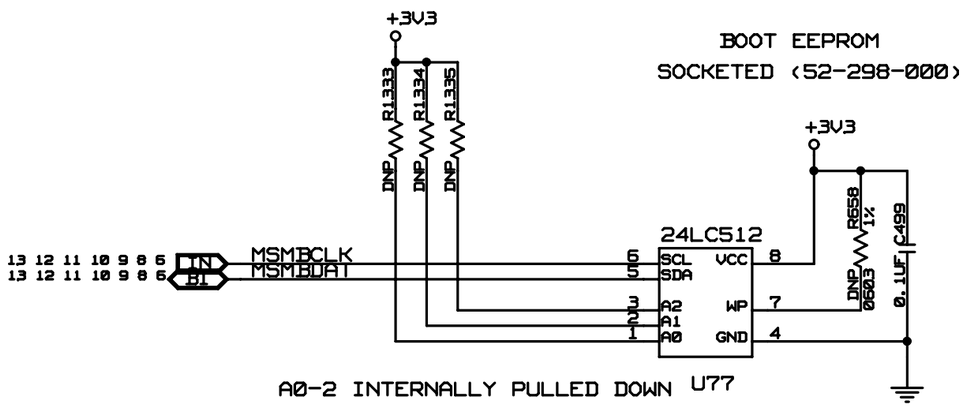
POWER REGULATOR - VDDPETA

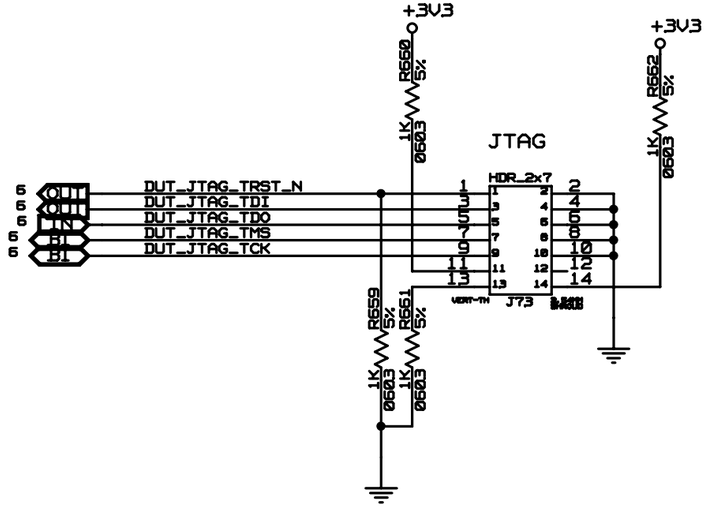
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

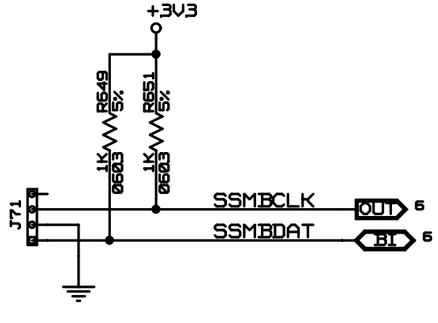
AUTHOR	CHECKED BY
Tony Tran	Derek Huang

Tue Apr 20 12:38:24 2010 — SHEET 26 OF 41









TITLE EB-LOGAN-19

RESET, SMBUS, EEPROM, JTAG

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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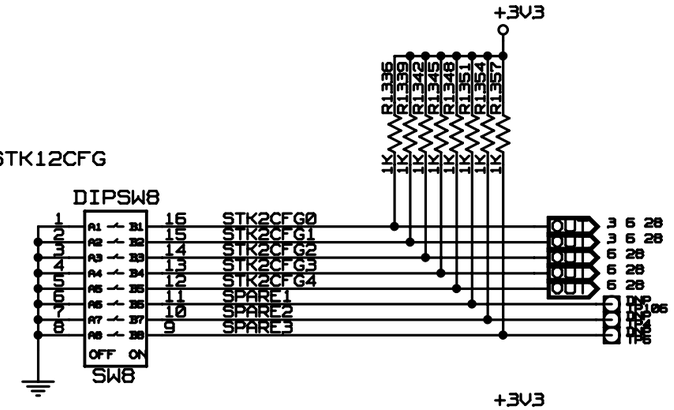
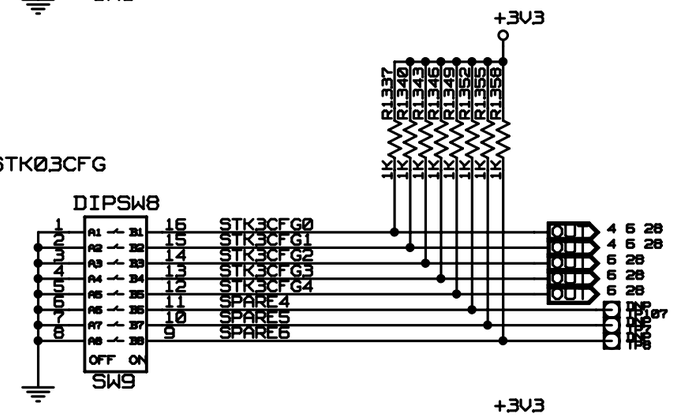
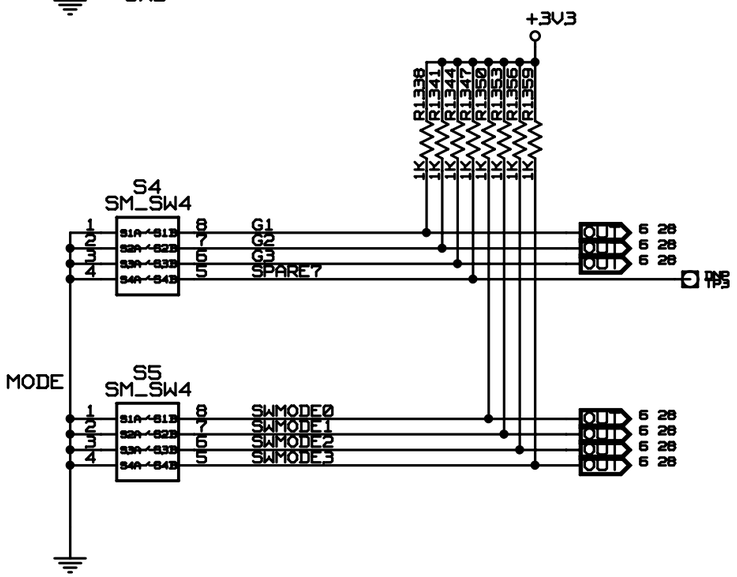
STK12CFG



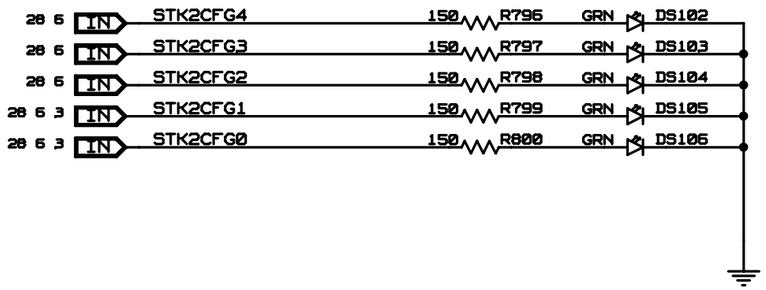
STK03CFG



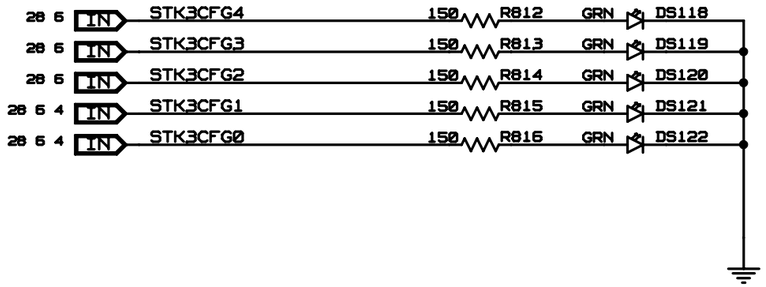
MODE



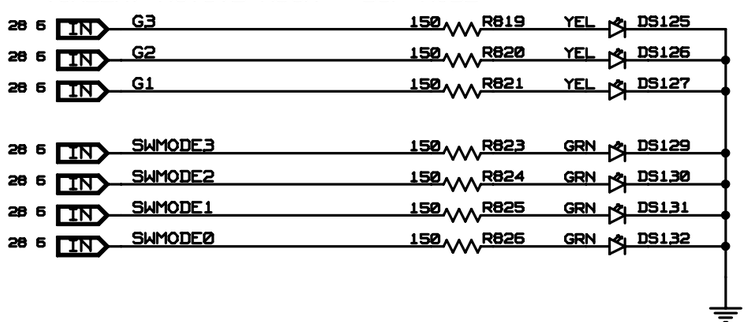
(GREEN) ACTIVE HIGH - DIP STK12CFG



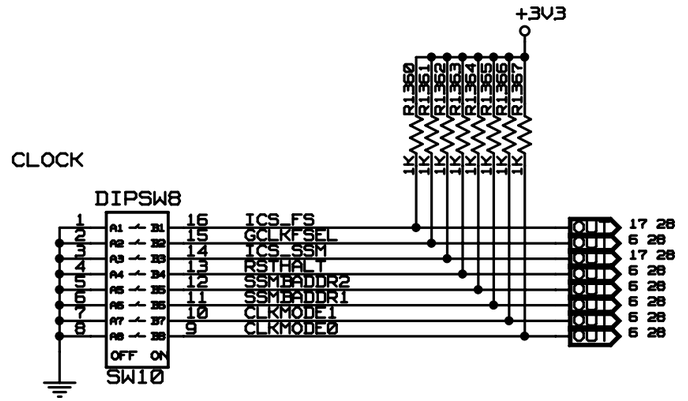
(GREEN) ACTIVE HIGH - DIP STK03CFG



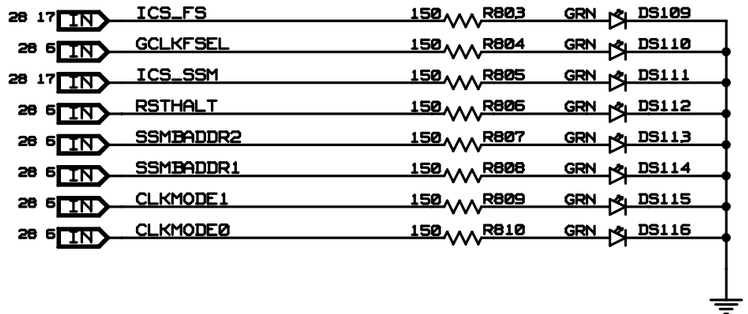
(GREEN) ACTIVE HIGH - DIP MODE



CLOCK



(GREEN) ACTIVE HIGH - DIP CLOCK



TITLE EB-LOGAN-19

DIP SWITCHES

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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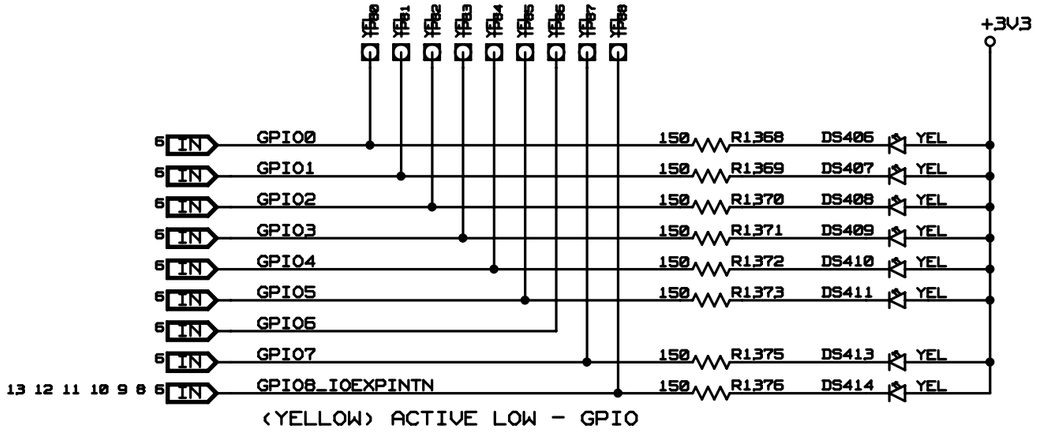
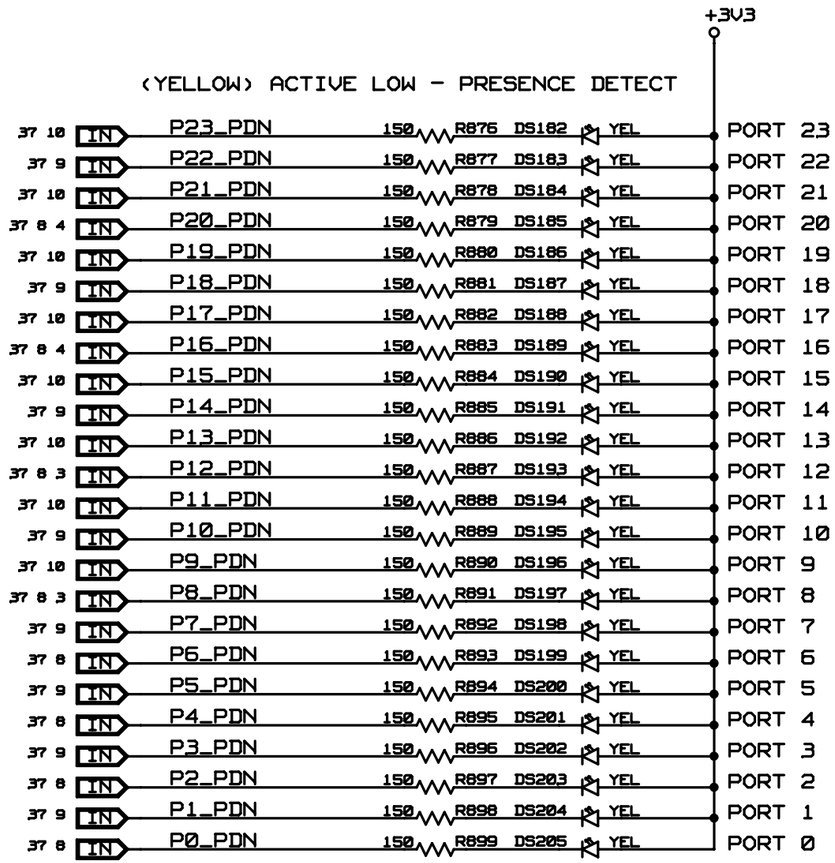


(YELLOW) ACTIVE LOW - GPIO

GPIO	ALT0	ALT1
0	PART0PERSTN	P16LINKUPN
1	PART1PERSTN	P16ACTIVEN
2	PART2PERSTN	P4LINKUPN
3	PART3PERSTN	P4ACTIVEN
4	FAILOVER0	P0LINKUPN
5	GPEN	P0ACTIVEN
7	FAILOVER2	P8LINKUPN
8	IOEXPINTN	P8ACTIVEN

(GREEN) ACTIVE LOW - ATTENTION INPUT

(YELLOW) ACTIVE LOW - PRESENCE DETECT



TITLE EB-LOGAN-19

LED - PORT STATUS (1 OF 7)

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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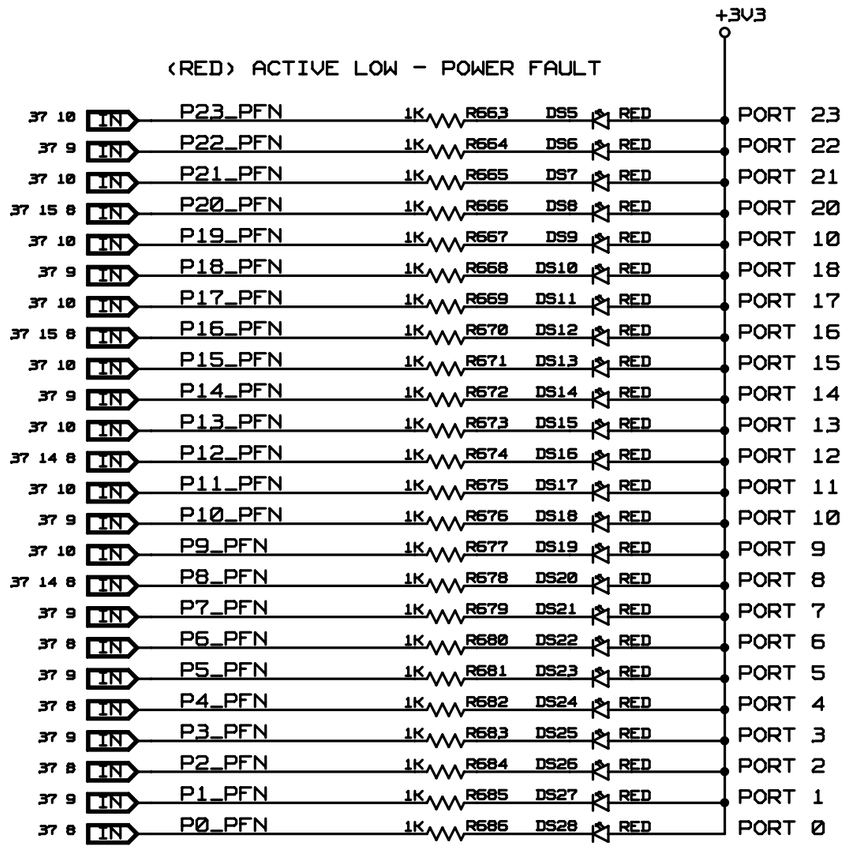

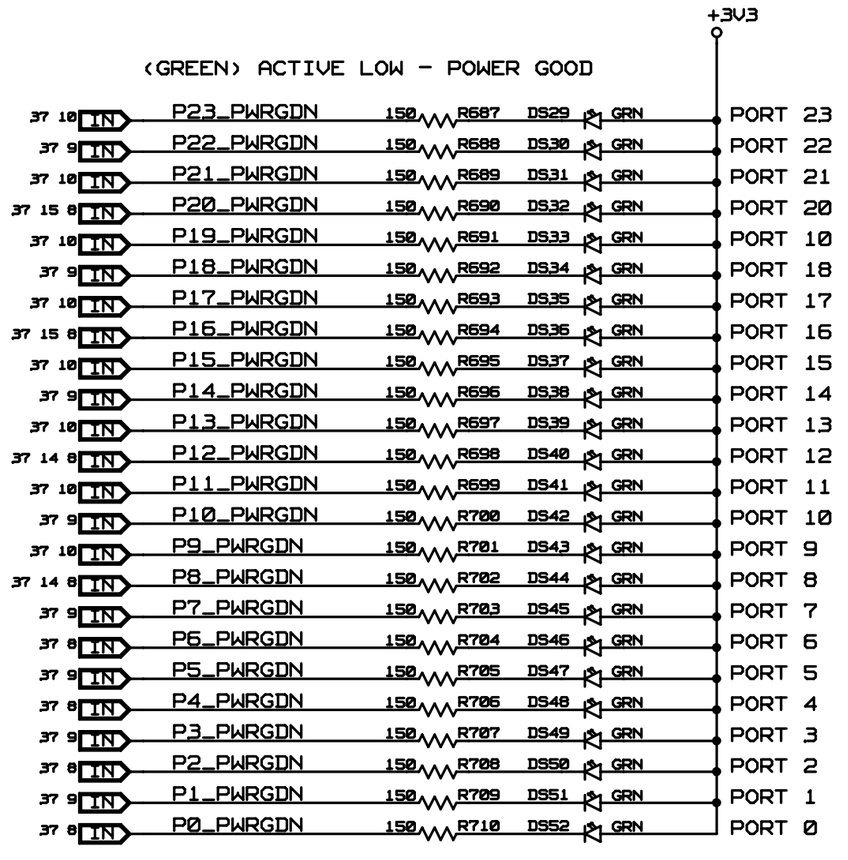

TITLE EB-LOGAN-19

LED - PORT STATUS (2 OF 7)

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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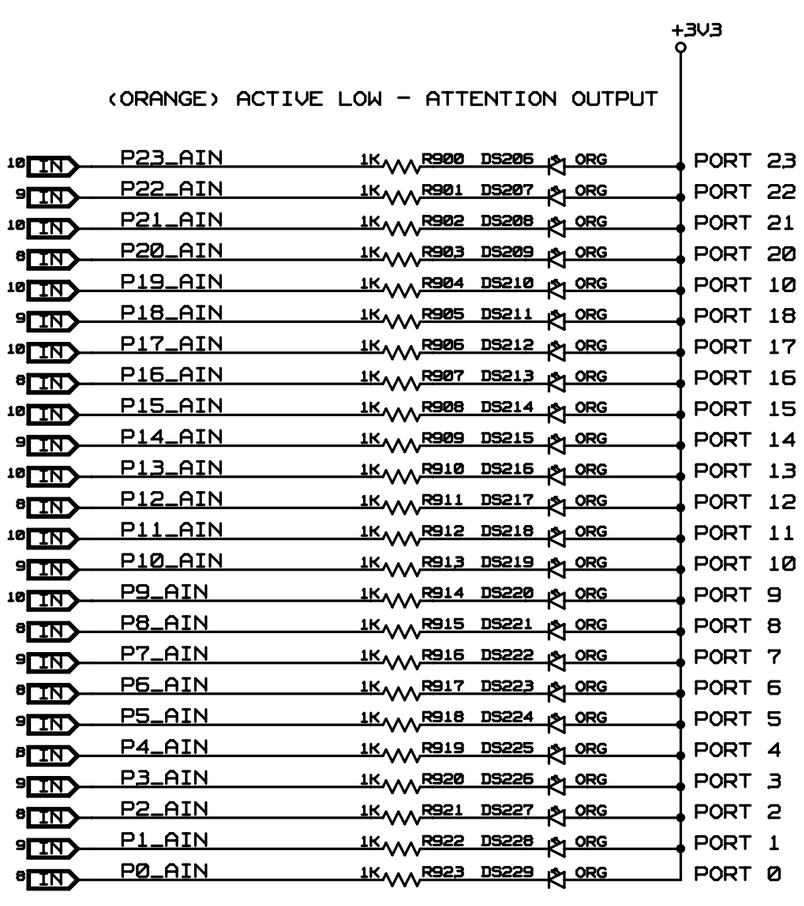

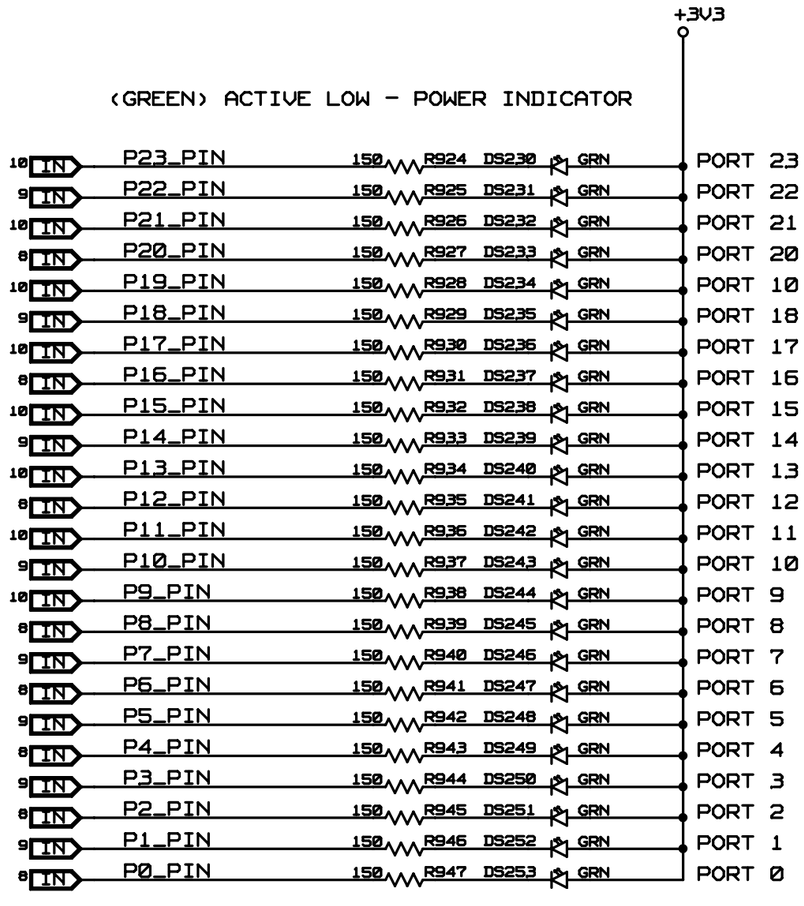

TITLE EB-LOGAN-19

LED - PORT STATUS (3 OF 7)

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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(GREEN) ACTIVE HIGH - POWER ENABLE

37 10	IN	P23_PEP	150	R711	GRN DS53	PORT 23
37 9	IN	P22_PEP	150	R712	GRN DS54	PORT 22
37 10	IN	P21_PEP	150	R713	GRN DS55	PORT 21
37 15 8	IN	P20_PEP	150	R714	GRN DS56	PORT 20
37 10	IN	P19_PEP	150	R715	GRN DS57	PORT 10
37 9	IN	P18_PEP	150	R716	GRN DS58	PORT 18
37 10	IN	P17_PEP	150	R717	GRN DS59	PORT 17
37 15 8	IN	P16_PEP	150	R718	GRN DS60	PORT 16
37 10	IN	P15_PEP	150	R719	GRN DS61	PORT 15
37 9	IN	P14_PEP	150	R720	GRN DS62	PORT 14
37 10	IN	P13_PEP	150	R721	GRN DS63	PORT 13
37 14 8	IN	P12_PEP	150	R722	GRN DS64	PORT 12
37 10	IN	P11_PEP	150	R723	GRN DS65	PORT 11
37 9	IN	P10_PEP	150	R724	GRN DS66	PORT 10
37 10	IN	P9_PEP	150	R725	GRN DS67	PORT 9
37 14 8	IN	P8_PEP	150	R726	GRN DS68	PORT 8
37 9	IN	P7_PEP	150	R727	GRN DS69	PORT 7
37 8	IN	P6_PEP	150	R728	GRN DS70	PORT 6
37 9	IN	P5_PEP	150	R729	GRN DS71	PORT 5
37 8	IN	P4_PEP	150	R730	GRN DS72	PORT 4
37 9	IN	P3_PEP	150	R731	GRN DS73	PORT 3
37 8	IN	P2_PEP	150	R732	GRN DS74	PORT 2
37 9	IN	P1_PEP	150	R733	GRN DS75	PORT 1
37 8	IN	P0_PEP	150	R734	GRN DS76	PORT 0

(RED) ACTIVE LOW - HP SLOT RST

+3V3

16 13 10	IN	P23_RSTN	1K	R735	DS77 RED	PORT 23
16 13 9	IN	P22_RSTN	1K	R736	DS78 RED	PORT 22
16 13 10	IN	P21_RSTN	1K	R737	DS79 RED	PORT 21
16 13 8	IN	P20_RSTN	1K	R738	DS80 RED	PORT 20
16 13 10	IN	P19_RSTN	1K	R739	DS81 RED	PORT 10
16 13 9	IN	P18_RSTN	1K	R740	DS82 RED	PORT 18
16 13 10	IN	P17_RSTN	1K	R741	DS83 RED	PORT 17
16 13 8	IN	P16_RSTN	1K	R742	DS84 RED	PORT 16
16 13 10	IN	P15_RSTN	1K	R743	DS85 RED	PORT 15
16 13 9	IN	P14_RSTN	1K	R744	DS86 RED	PORT 14
16 13 10	IN	P13_RSTN	1K	R745	DS87 RED	PORT 13
16 13 8	IN	P12_RSTN	1K	R746	DS88 RED	PORT 12
16 13 10	IN	P11_RSTN	1K	R747	DS89 RED	PORT 11
16 13 9	IN	P10_RSTN	1K	R748	DS90 RED	PORT 10
16 13 10	IN	P9_RSTN	1K	R749	DS91 RED	PORT 9
16 13 8	IN	P8_RSTN	1K	R750	DS92 RED	PORT 8
16 13 9	IN	P7_RSTN	1K	R751	DS93 RED	PORT 7
16 13 8	IN	P6_RSTN	1K	R752	DS94 RED	PORT 6
16 13 9	IN	P5_RSTN	1K	R753	DS95 RED	PORT 5
16 13 8	IN	P4_RSTN	1K	R754	DS96 RED	PORT 4
16 13 9	IN	P3_RSTN	1K	R755	DS97 RED	PORT 3
16 13 8	IN	P2_RSTN	1K	R756	DS98 RED	PORT 2
16 13 9	IN	P1_RSTN	1K	R757	DS99 RED	PORT 1
16 13 8	IN	P0_RSTN	1K	R758	DS100 RED	PORT 0

TITLE EB-LOGAN-19

LED - PORT STATUS (4 OF 7)

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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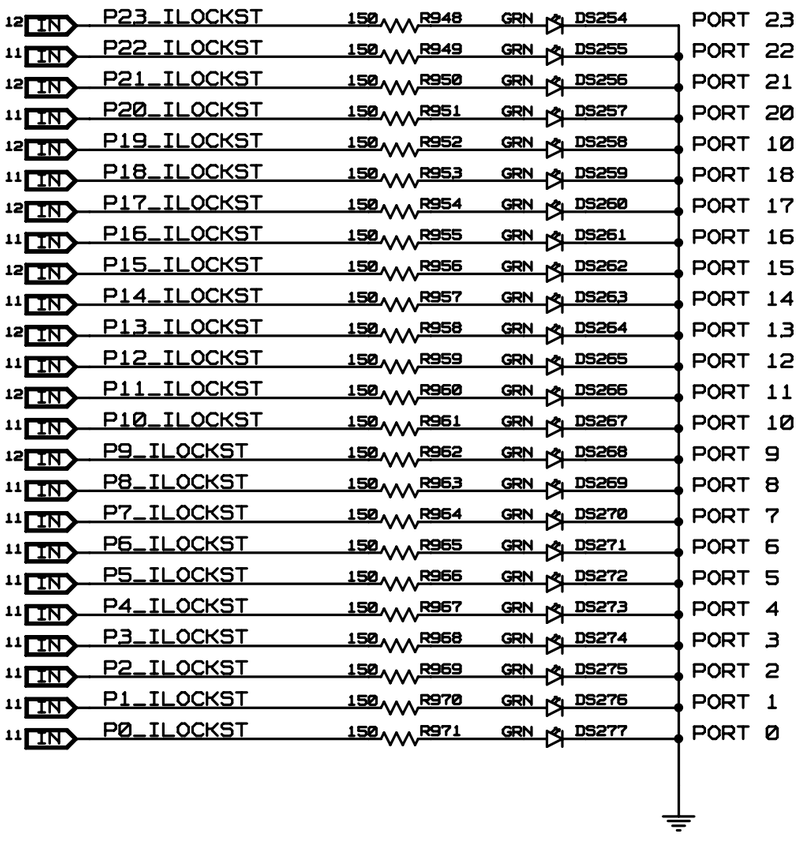
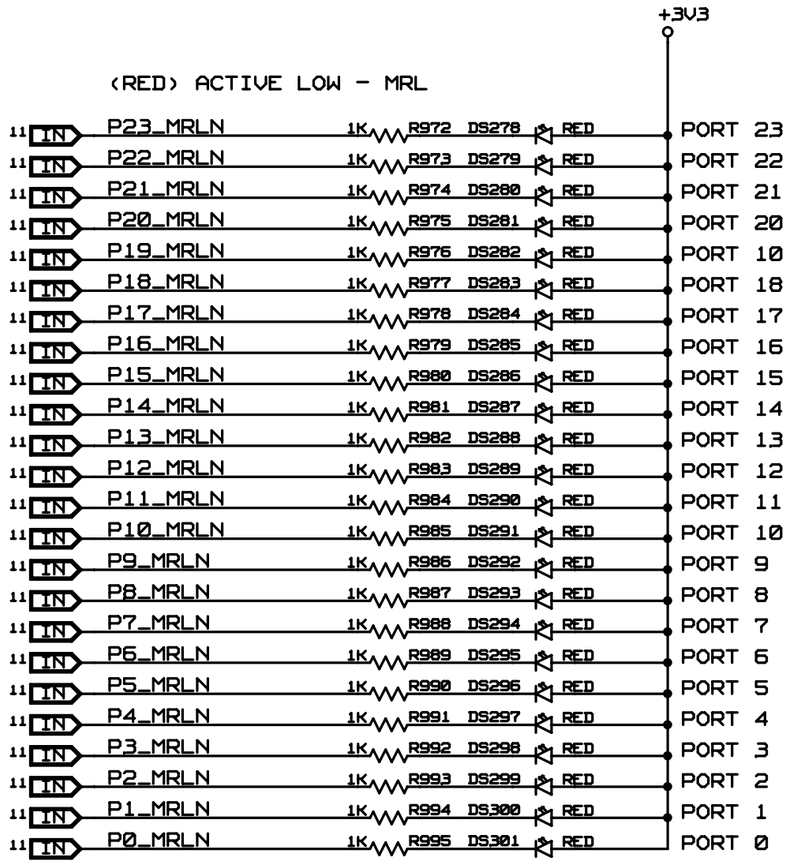
(GREEN) ACTIVE HIGH - INTERLOCK INPUT



(RED) ACTIVE LOW - MRL



TITLE EB-LOGAN-19

LED - PORT STATUS (5 OF 7)

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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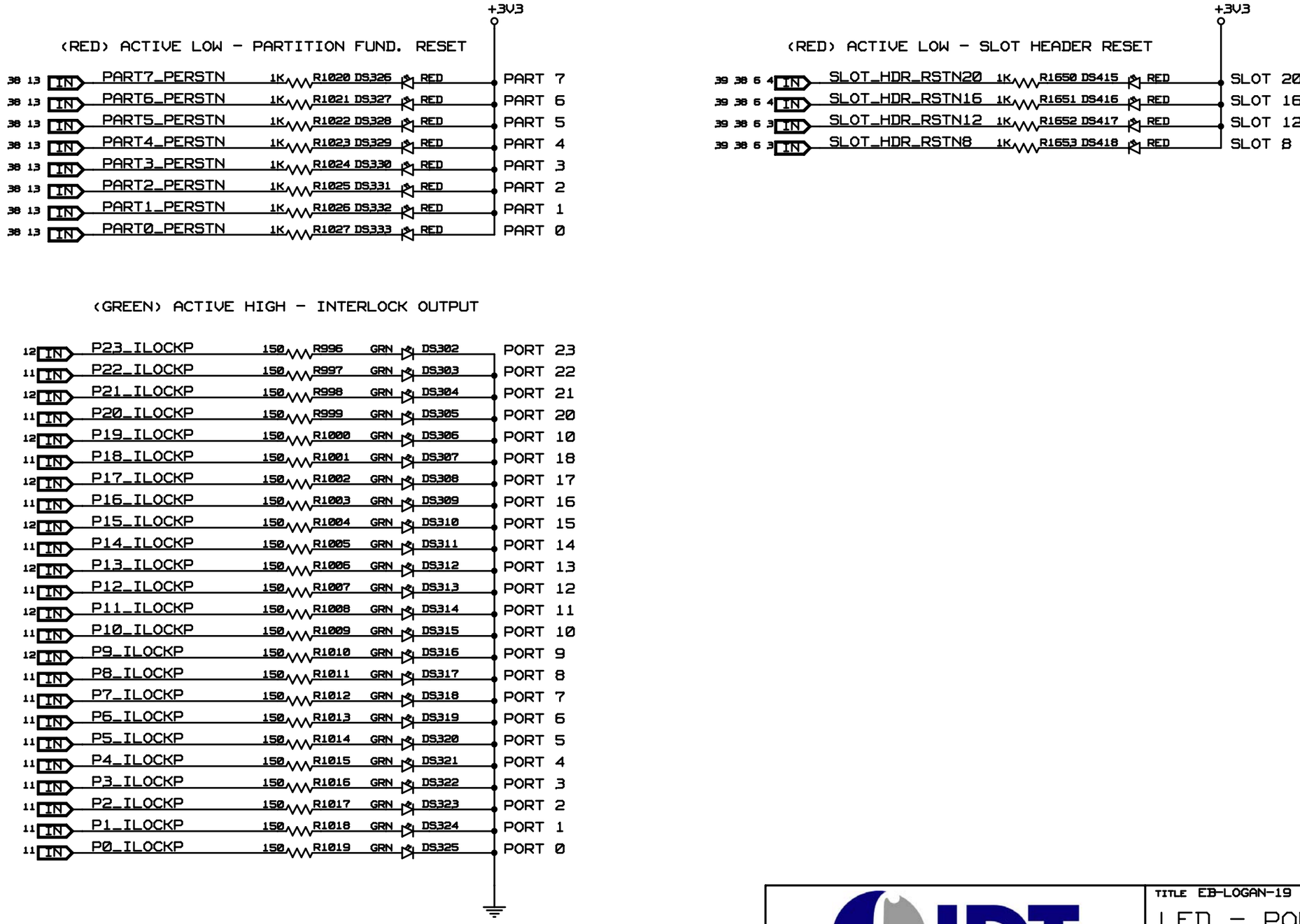

TITLE EB-LOGAN-19

LED - PORT STATUS (6 OF 7)

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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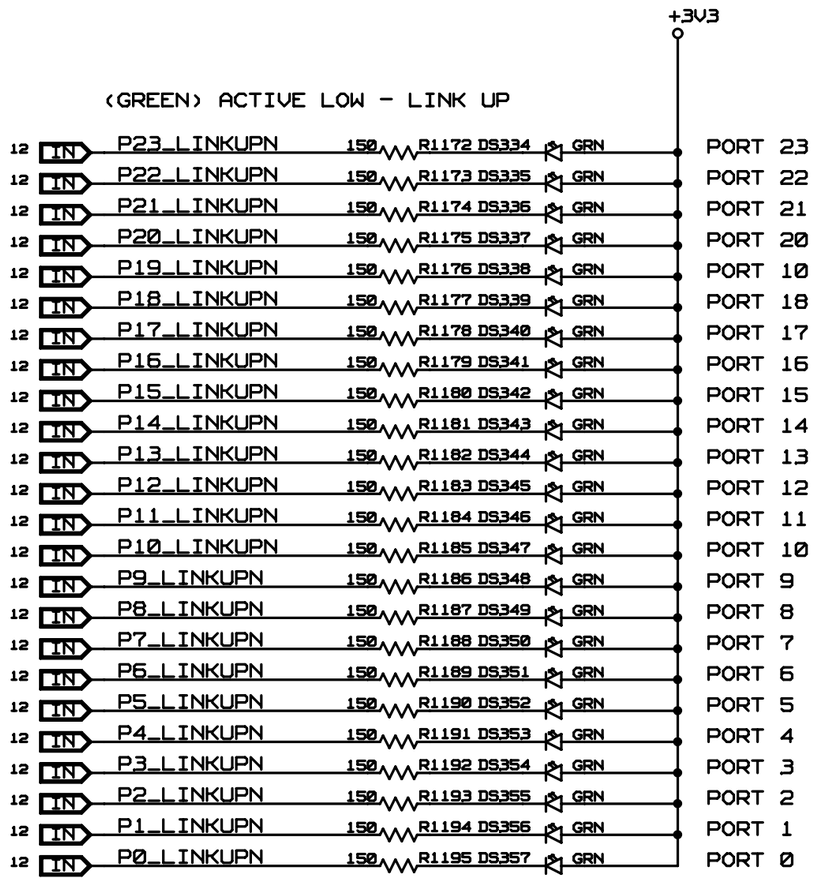

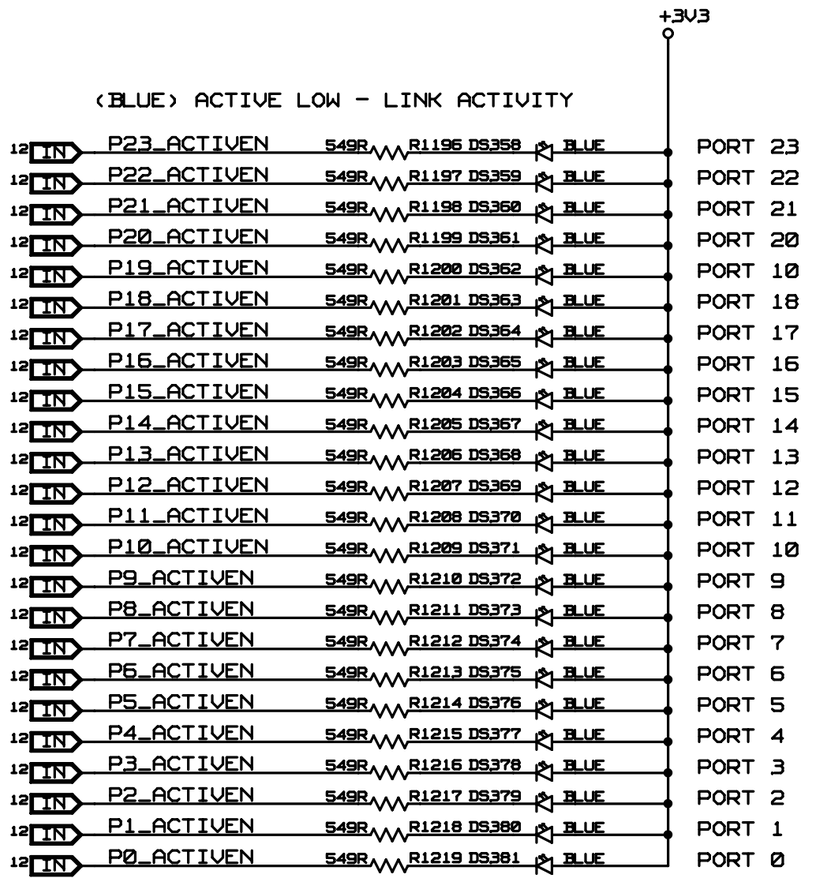

TITLE EB-LOGAN-19

LED - PORT STATUS (7 OF 7)

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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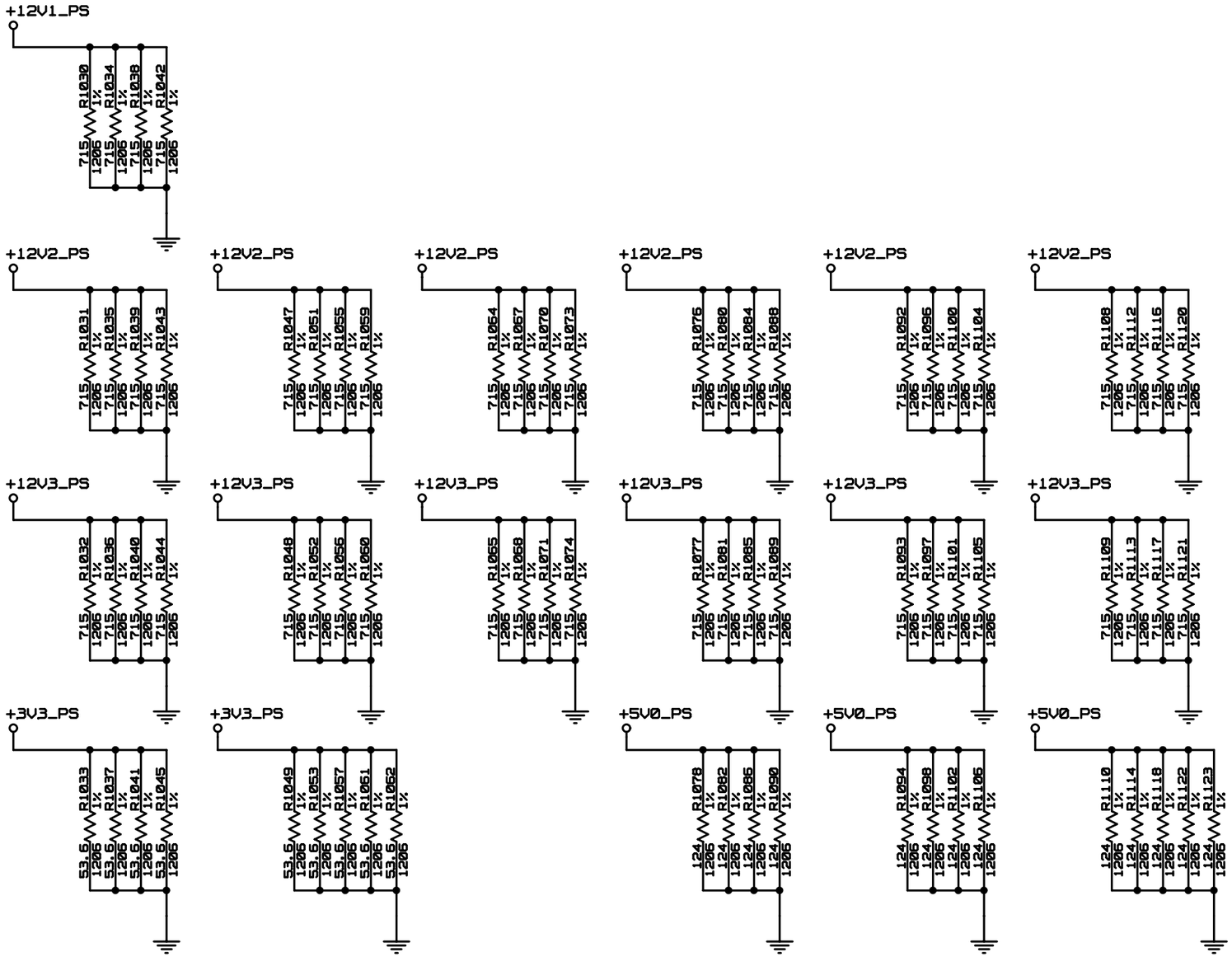
MINIMUM POWER SUPPLY LOADS



TITLE EB-LOGAN-19

MIN LOAD RESISTORS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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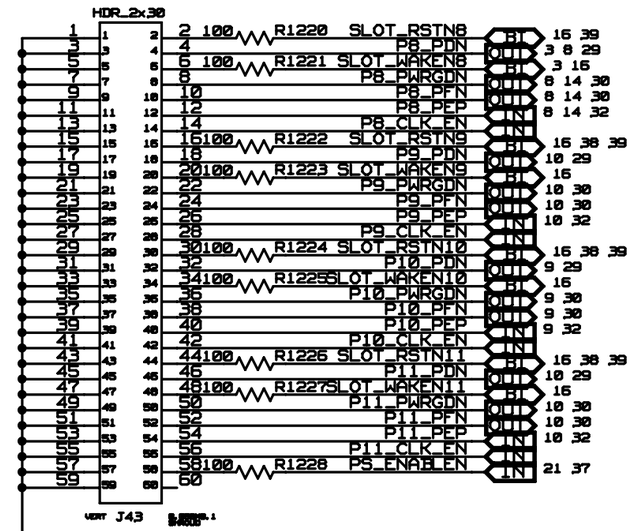
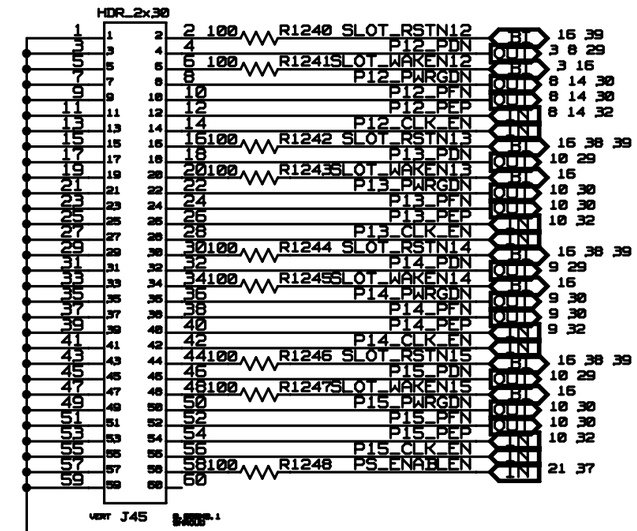
SLOT_RESETN
CARD_PRESENTN
WAKEN
POWERGOOD
PWR_FLTN
PWR_ENABLE
CLOCK_ENABLEN

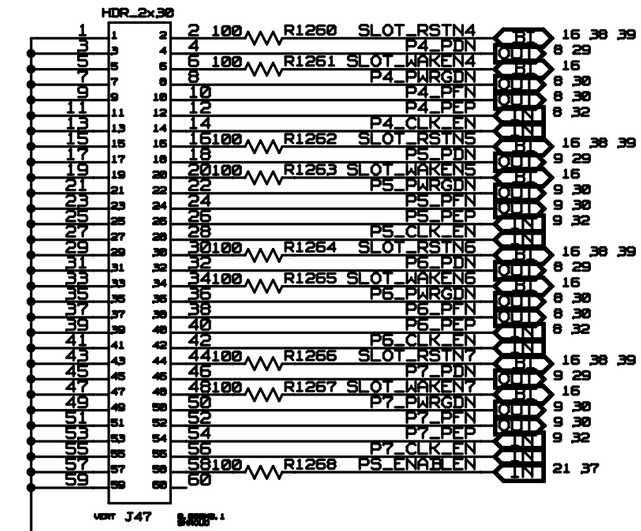
PS_ENABLEN
CABLE SENSE



PORTS 8, 9, 10, 11



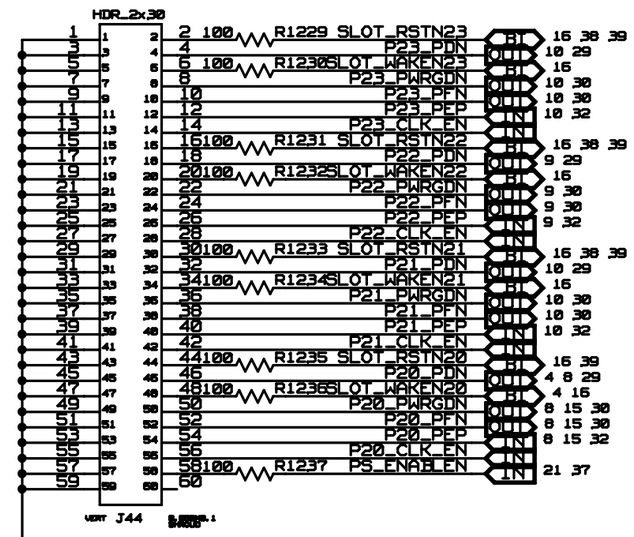
PORTS 12, 13, 14, 15



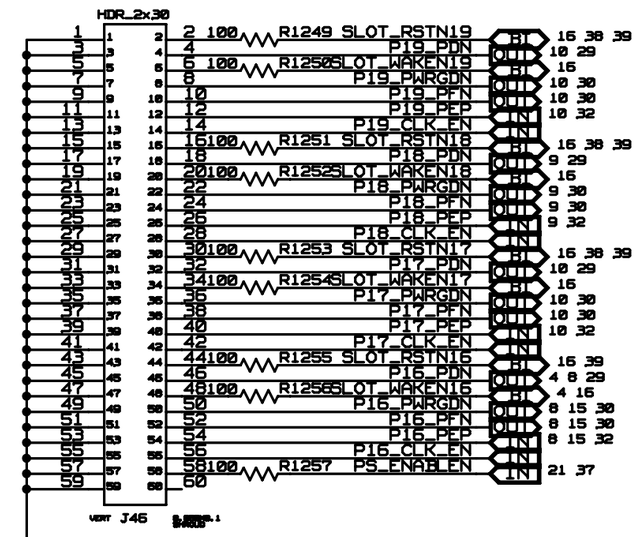
PORTS 4, 5, 6, 7

SLOT_RESETN
CARD_PRESENTN
WAKEN
POWERGOOD
PWR_FLTN
PWR_ENABLE
CLOCK_ENABLEN

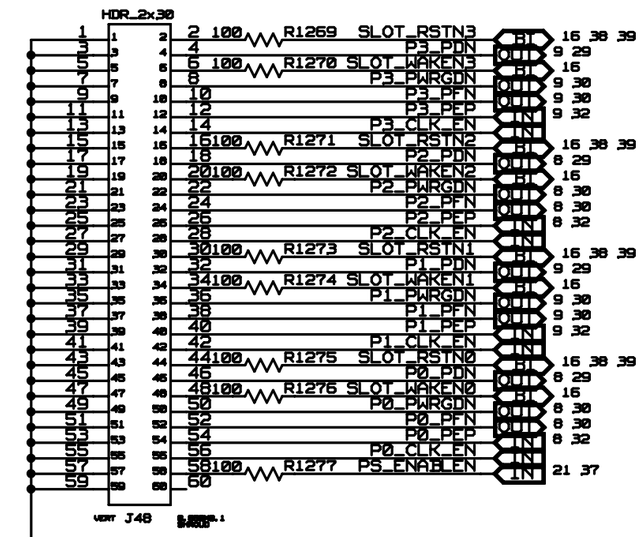
PS_ENABLEN
CABLE SENSE



PORTS 23, 22, 21, 20

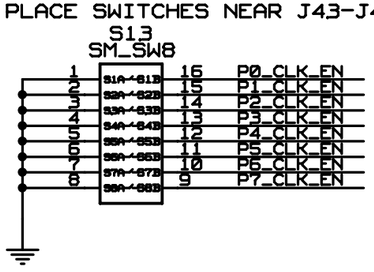


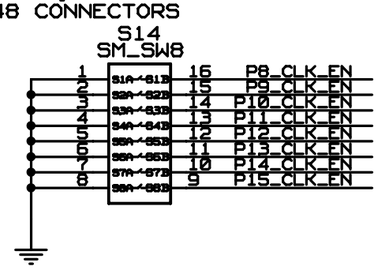
PORTS 19, 18, 17, 16

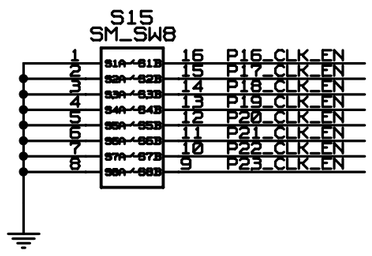


PORTS 3, 2, 1, 0

PLACE SWITCHES NEAR J43-J48 CONNECTORS



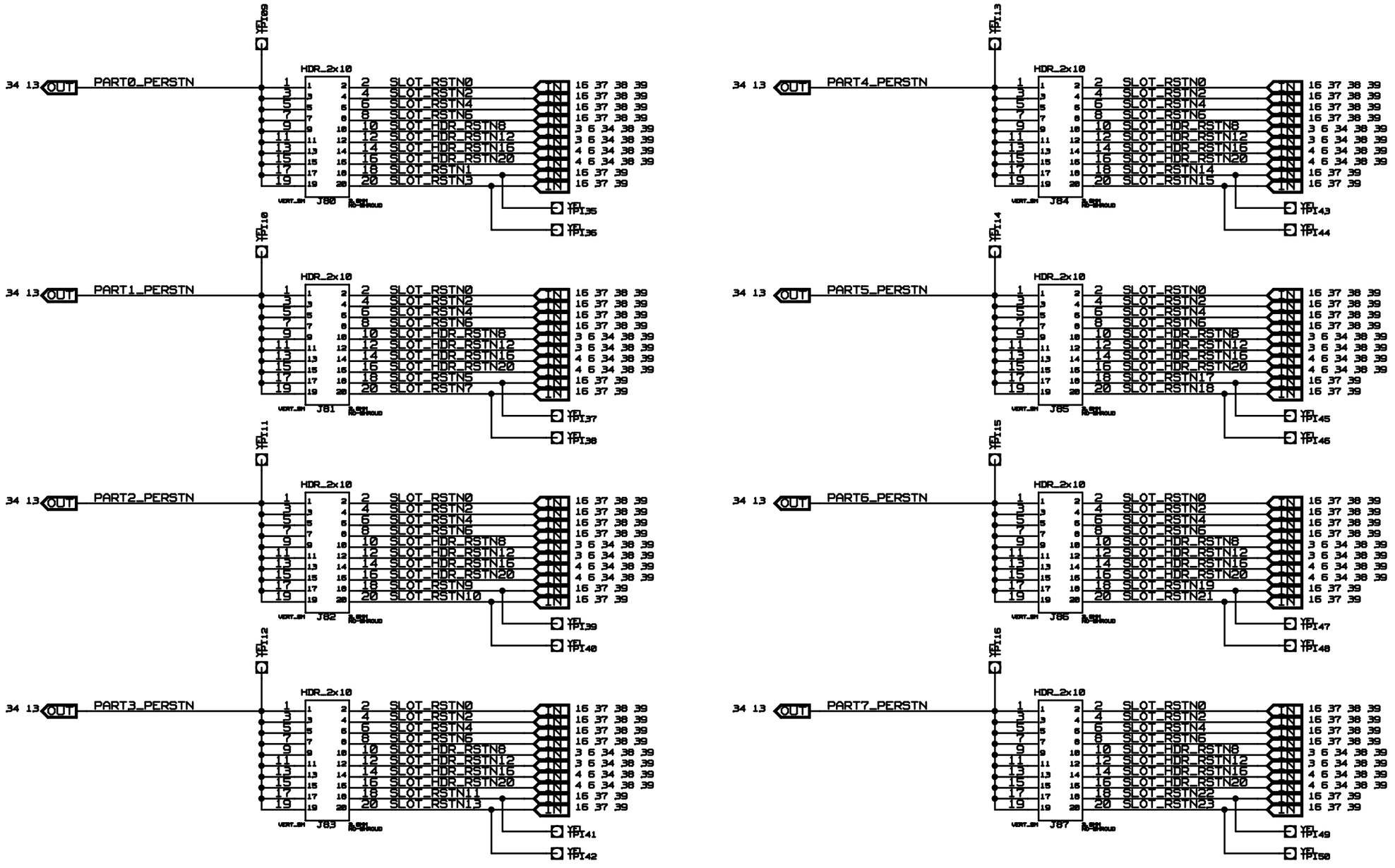




TITLE EB-LOGAN-19

SIDEBAND CONNECTORS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1
AUTHOR	Tony Tran	CHECKED BY	Derek Huang
Tue Apr 20 12:38:30 2010		SHEET 37 OF 41	



TITLE EB-LOGAN-19

PARTITION RESET SELECT HEADERS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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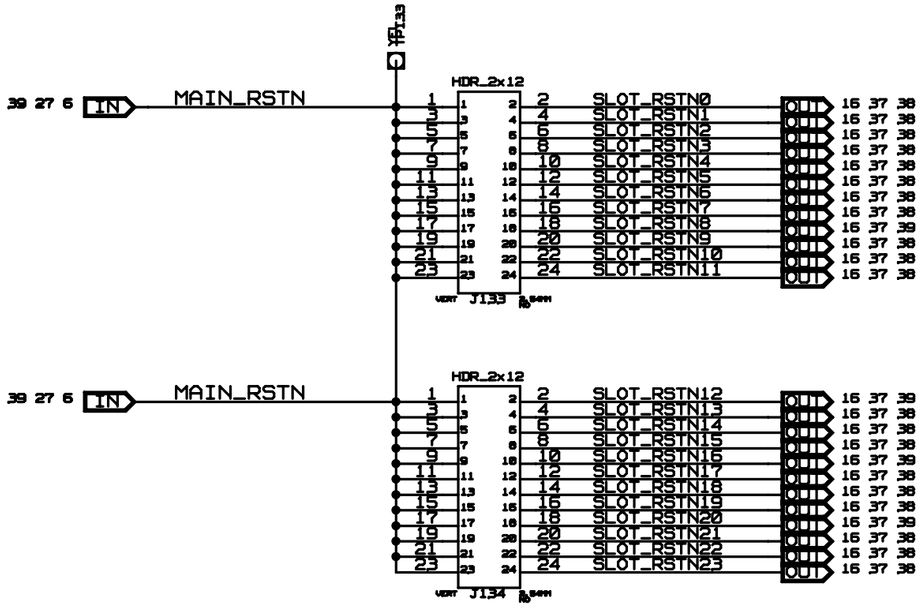
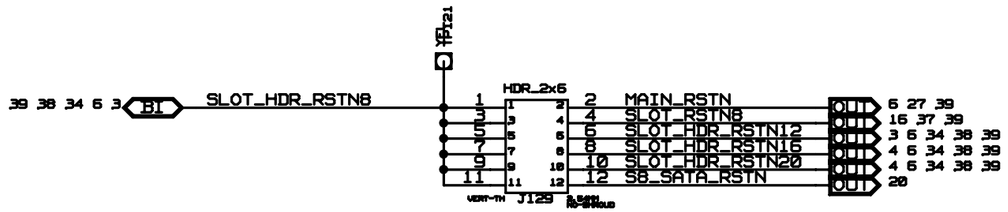
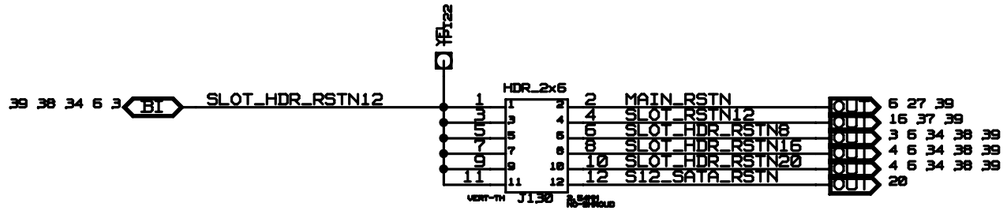
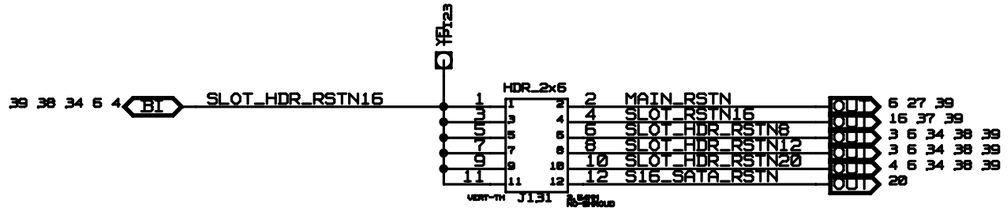
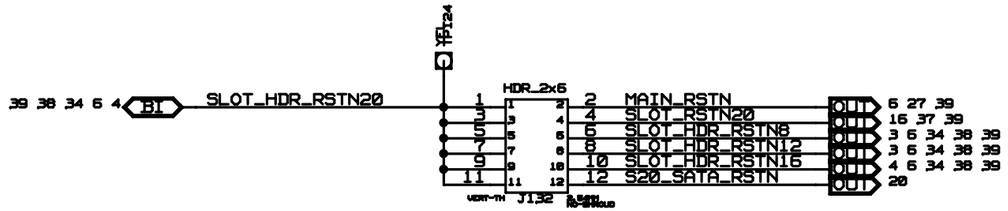
NOTE: DNP JUMPERS WHEN IOEXPANDER IS ENABLED











TITLE EB-LOGAN-19

SLOT RESET SELECT HEADERS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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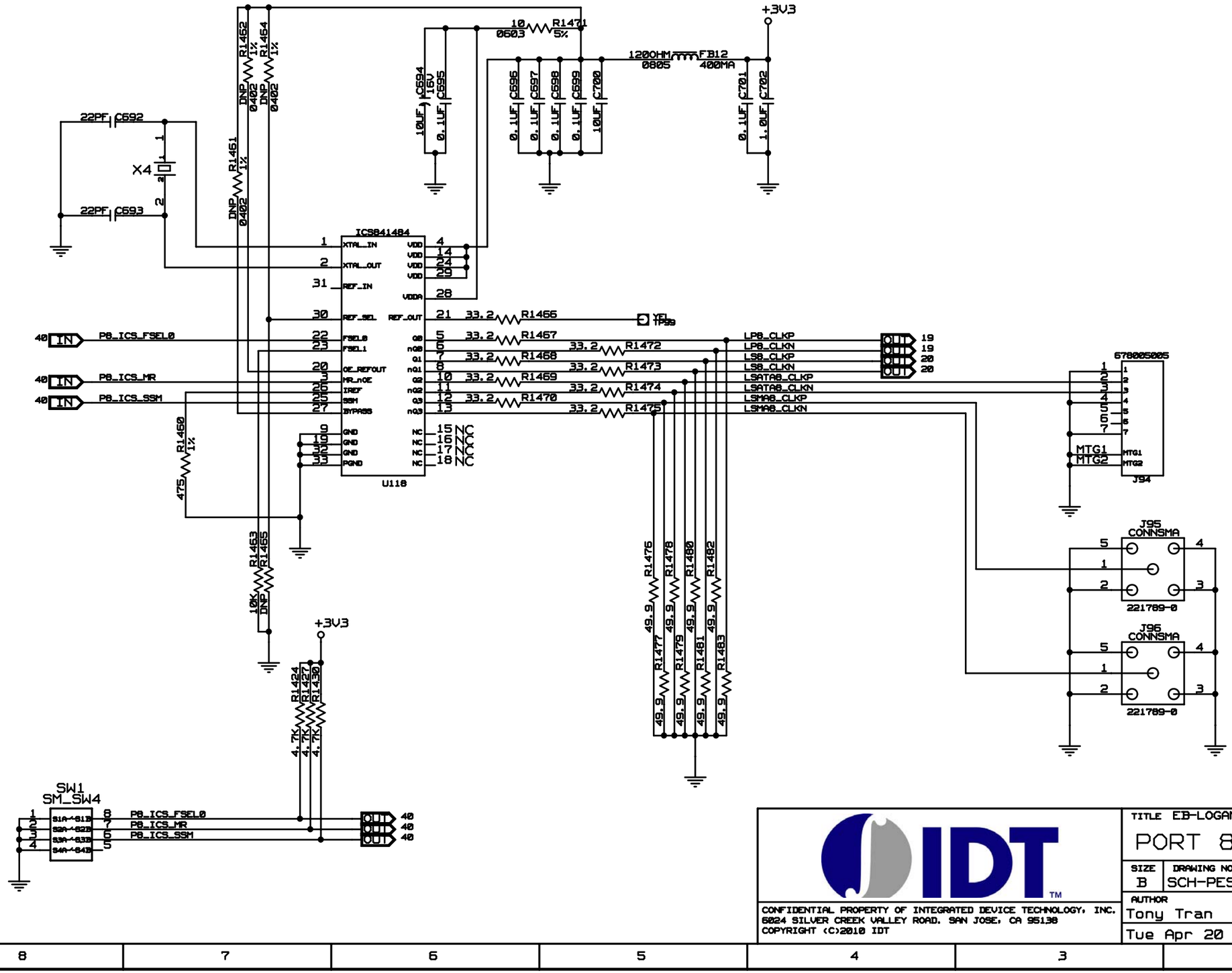

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TITLE EB-LOGAN-19

PORT 8 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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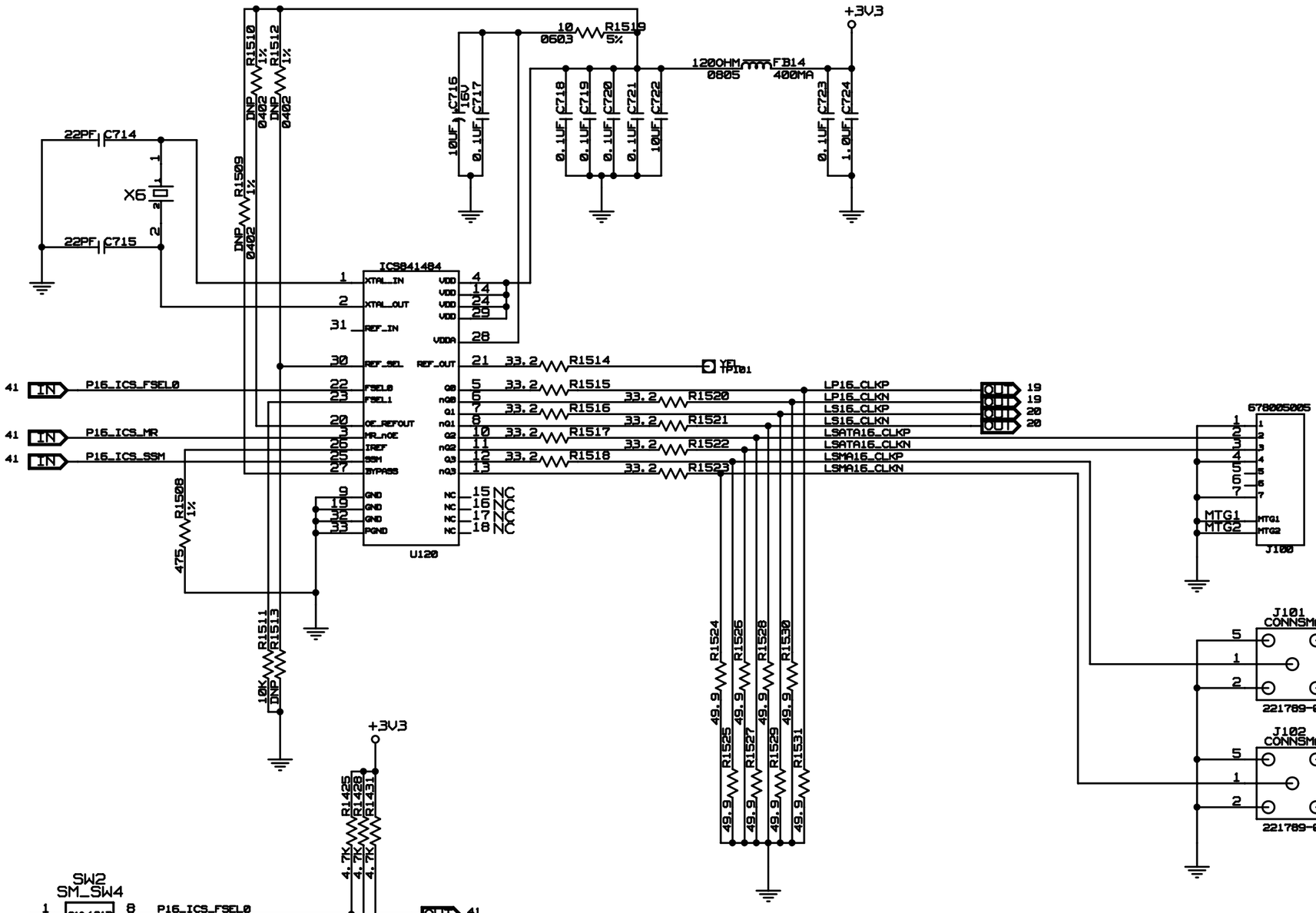

TITLE EB-LOGAN-19

PORT 16 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-000	1.1

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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