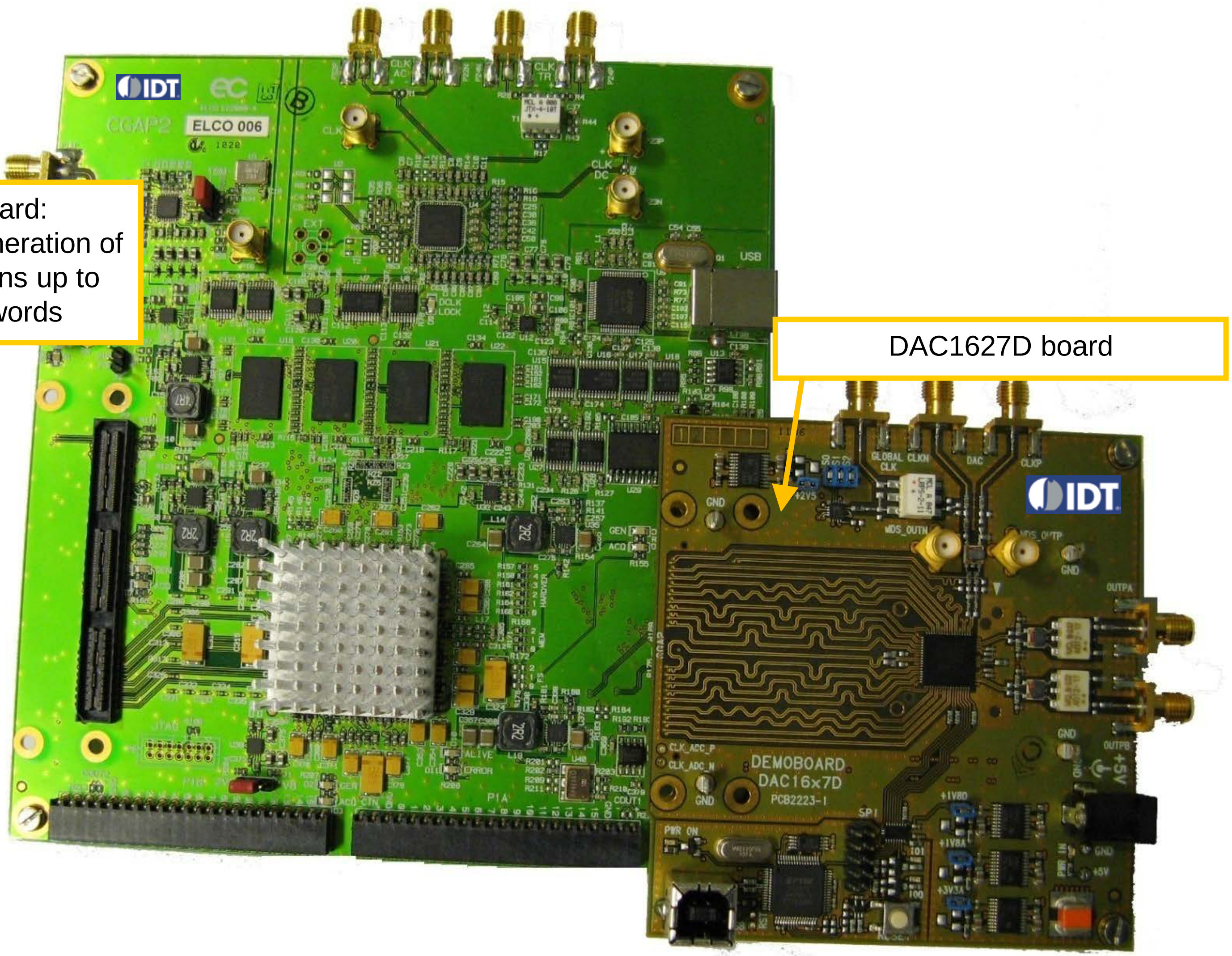
# DAC1627D Demo boards – Quick Start v2

# DAC1627D demoboard+ CGAP2

*Board presentation*

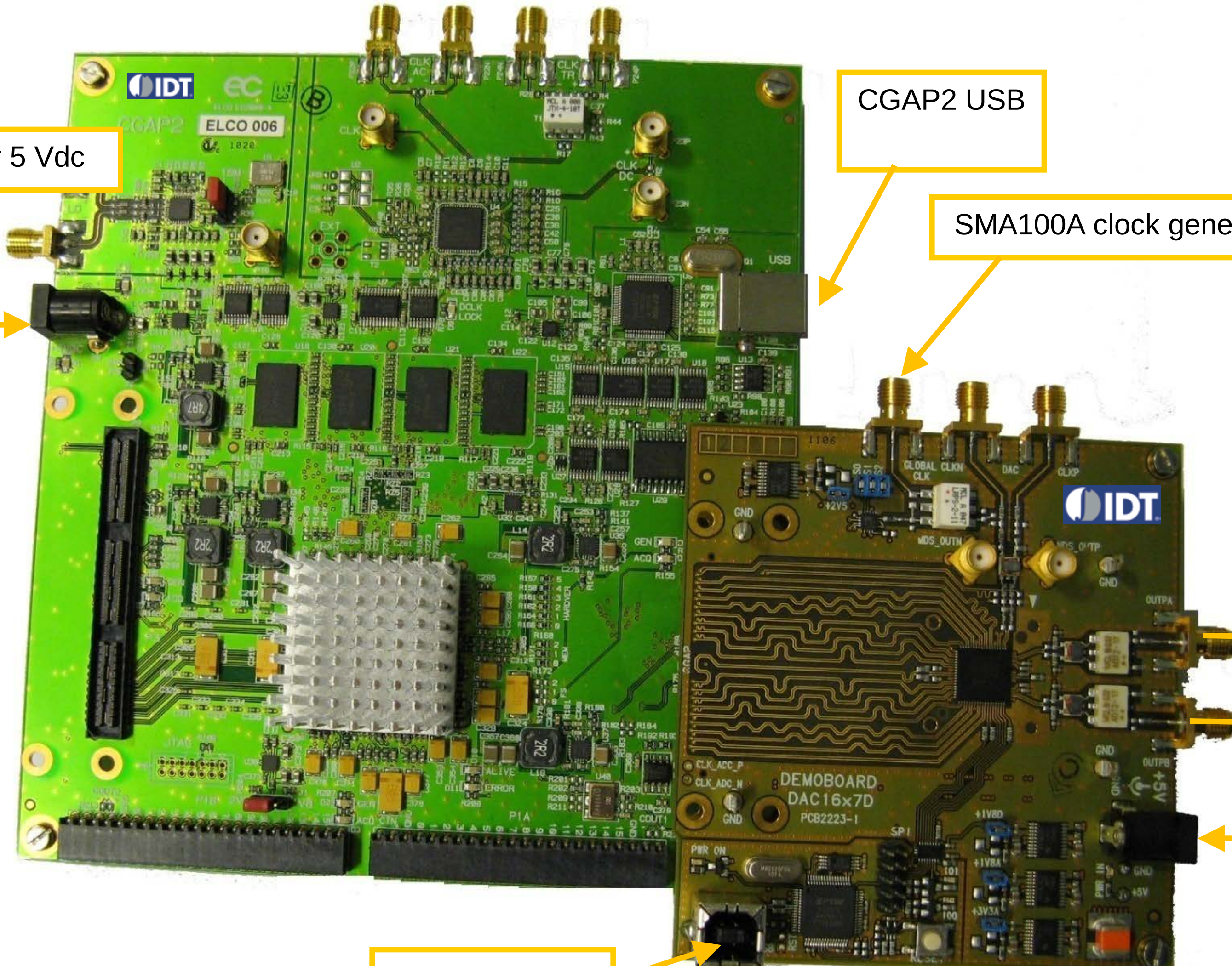
CGAP2 board:
Storage and Generation of complex patterns up to 32M (I,Q)- words

DAC1627D board



# DAC1627D demoboard+ CGAP2

***Board connections***




Power 5 Vdc

CGAP2 USB

SMA100A clock generator : DAC clock

PXA spectrum analyzer

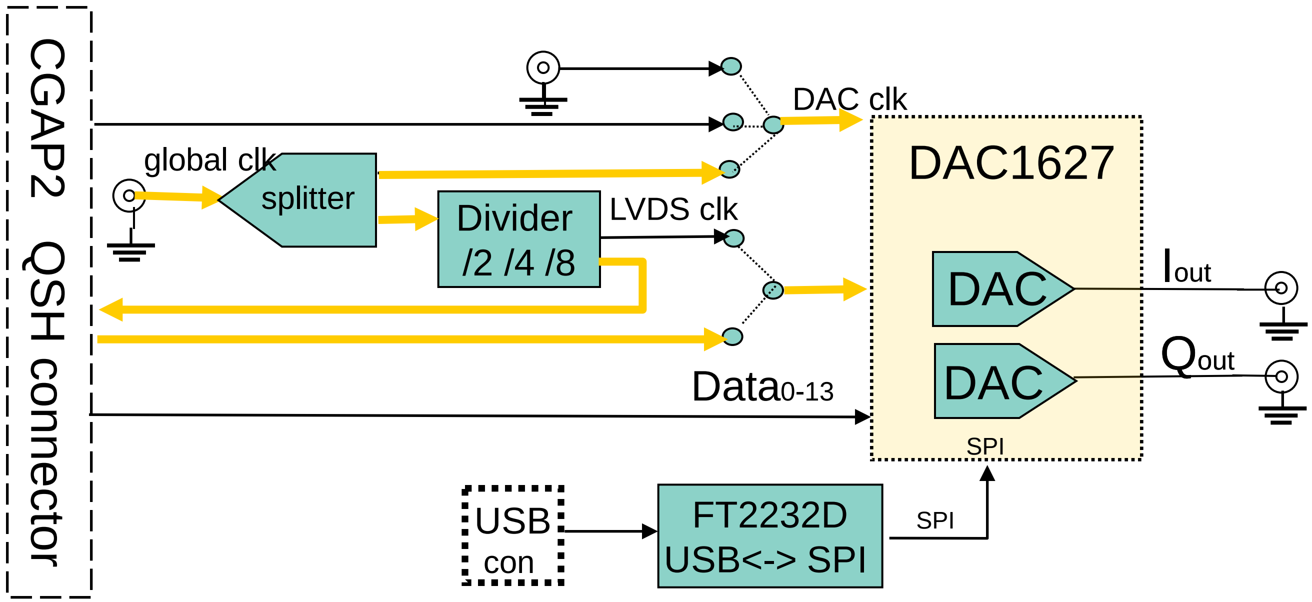
PXA spectrum analyzer

Power 5 Vdc

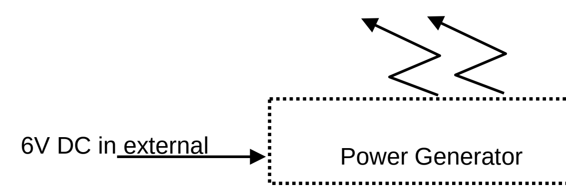
DAC1627D SPI USB control

# DAC1627 Board overview

## Block Diagram




One **Global clock** is used for both DAC board and CGAP2 board.

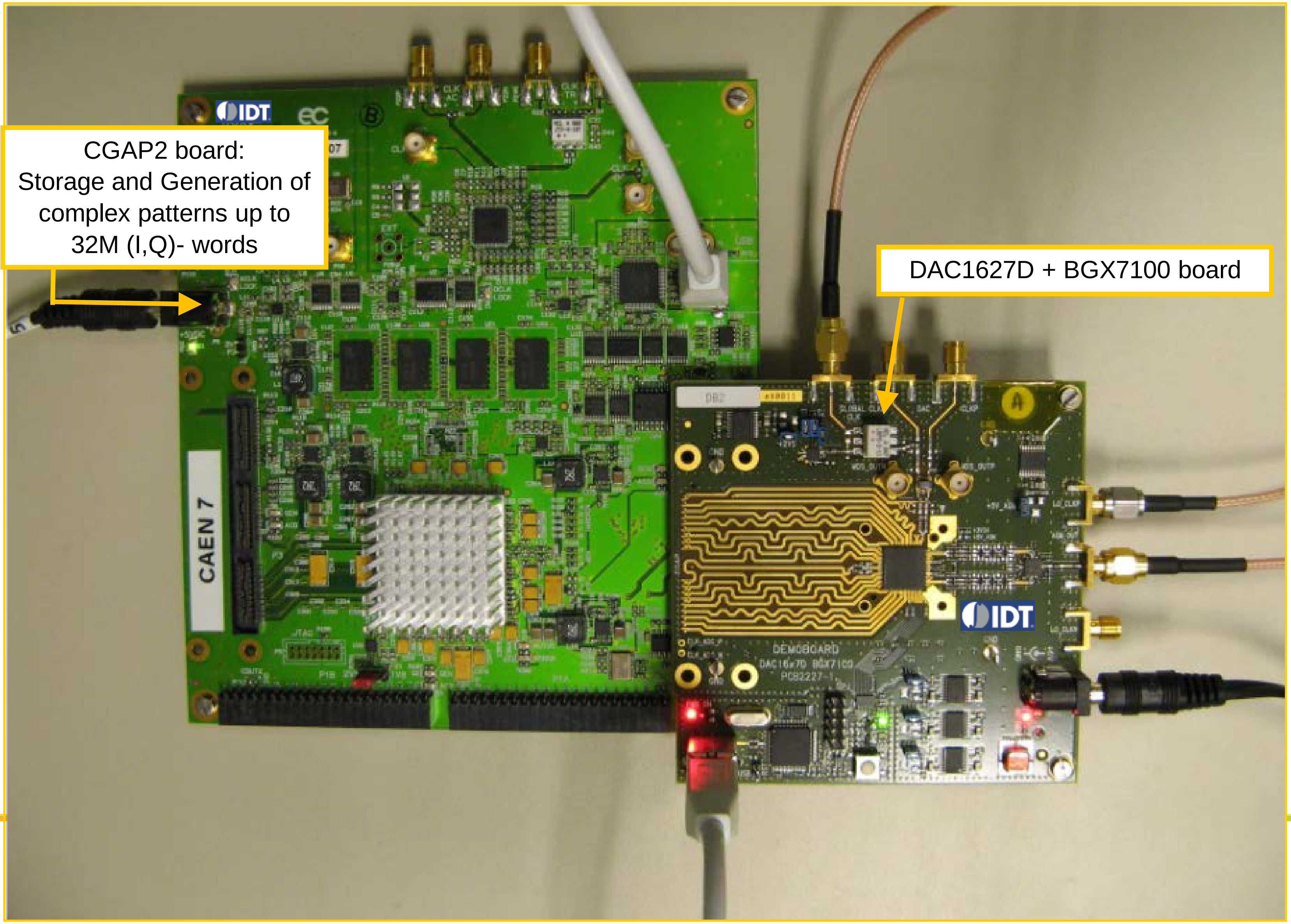



This **Global Clock** is split on two signals:

- one is feeding the DAC1627D
- one is divided and send trough the Samtec connector to the CGAP board to feed the FPGA

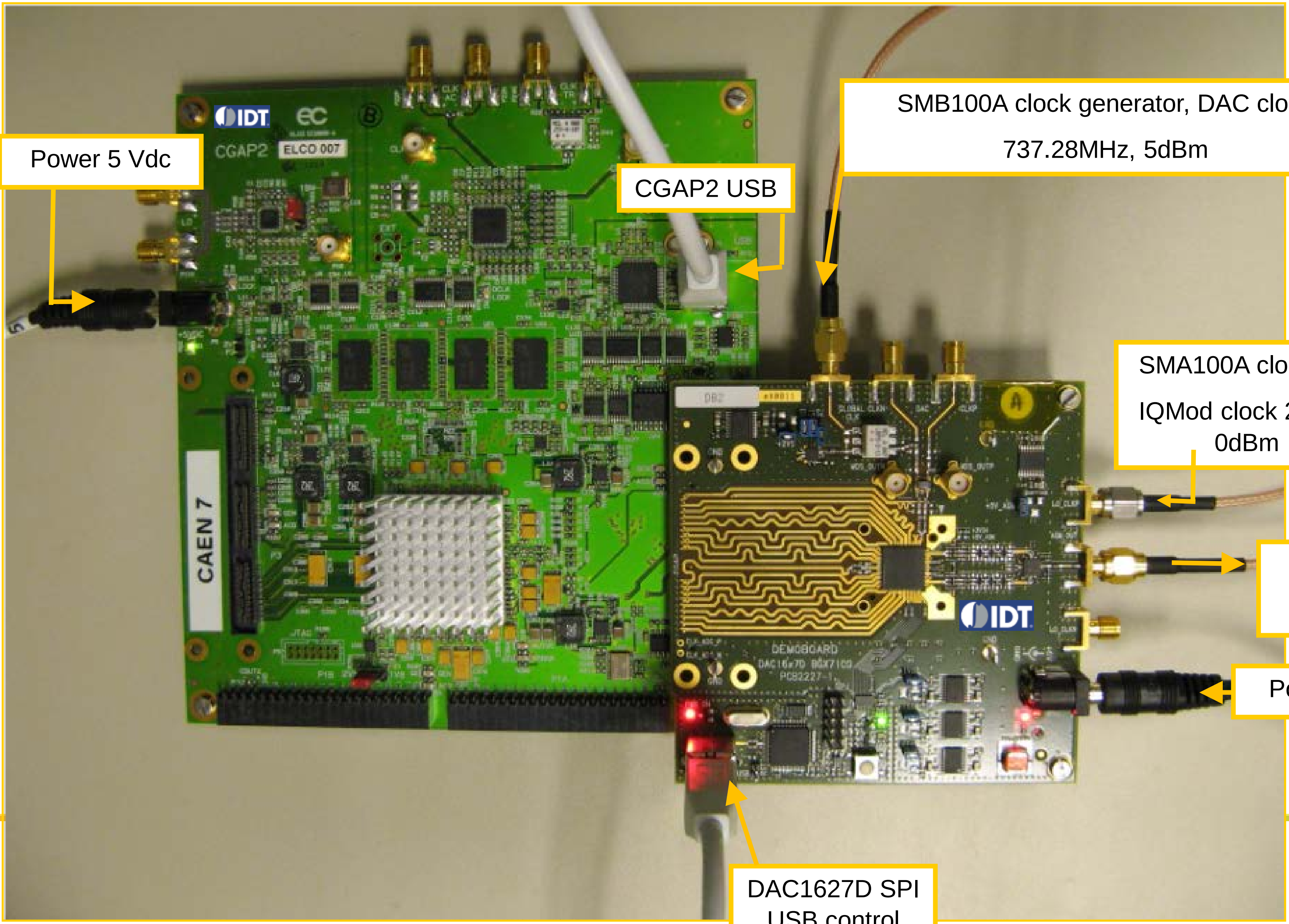
# DAC1627D + BGX7100 IQMod demoboard+ CGAP2

*Board presentation*

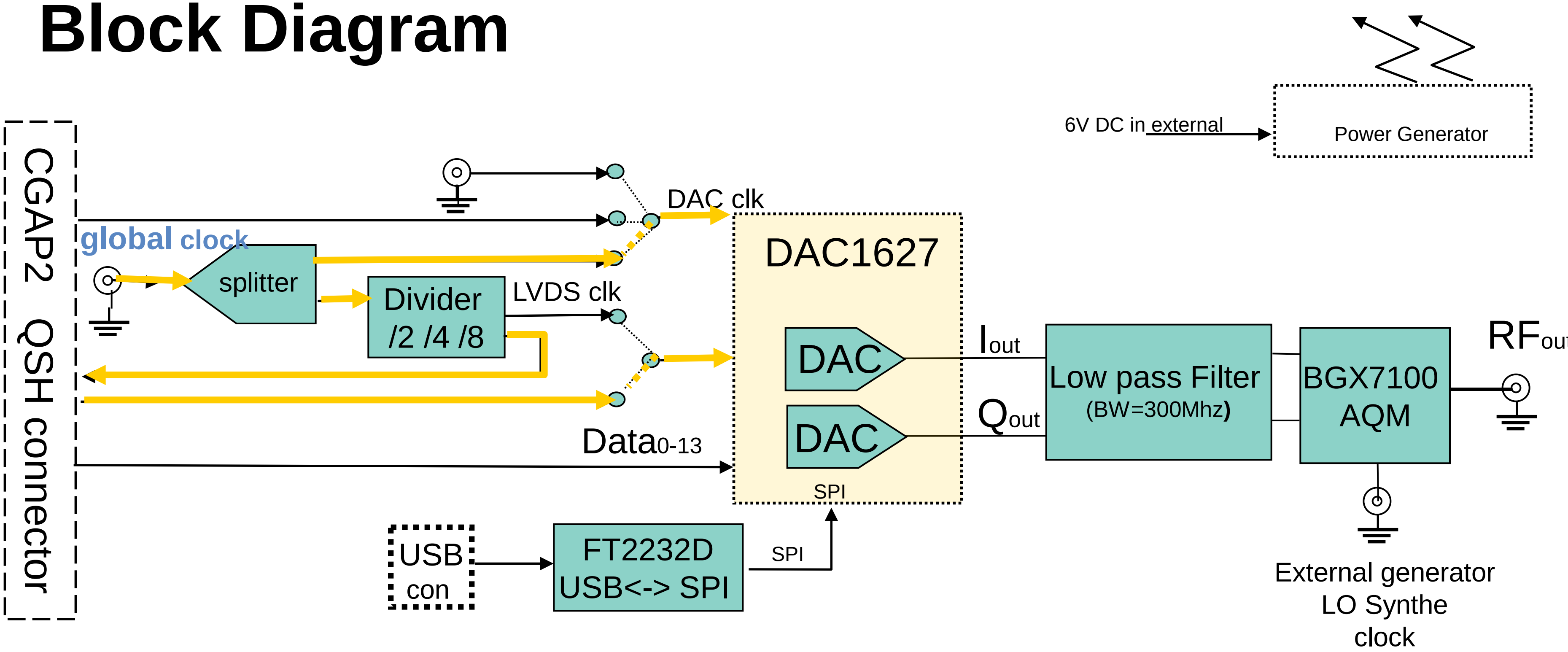


# DAC1627D + BGX7100 IQMod demoboard+ CGAP2

*Board connections*



# DAC1627/ BGX7100 Board overview
# Block Diagram




One **Global clock** is used for both DAC board and CGAP board.

This **Global Clock** is split on two signals:

- one is feeding the DAC1627D
- one is divided and send trough the Samtec connector to the CGAP board to feed the FPGA

# S0/S1/S2 jumpers position

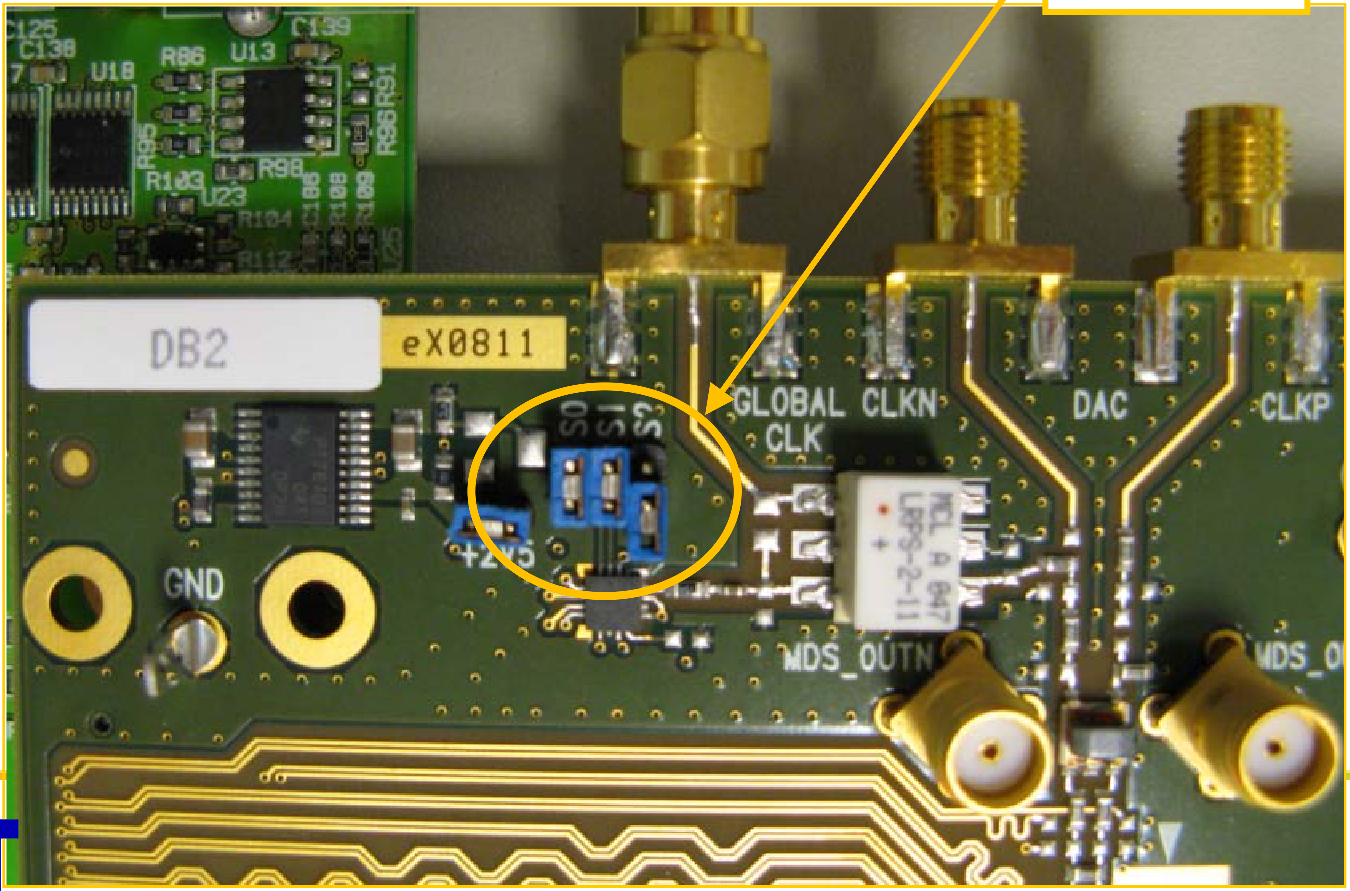
S0/S1/S2 jumpers are used to configure the divider ratio for the clock feeding the CGAP board..
For the current software revision, the **ratio value** needs to be **set to 2**.

Please, make sure that the jumpers have the following configuration on the board:

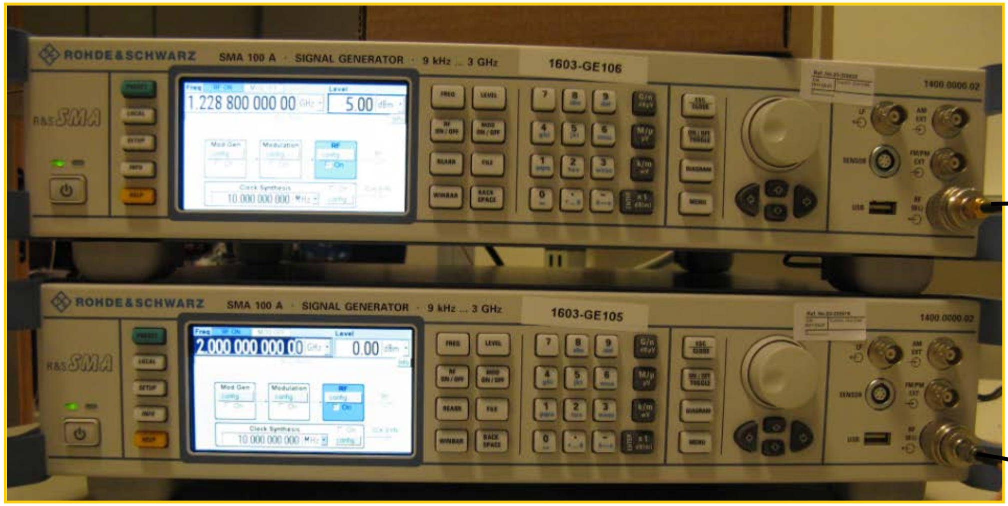
S0: ON

S1: ON

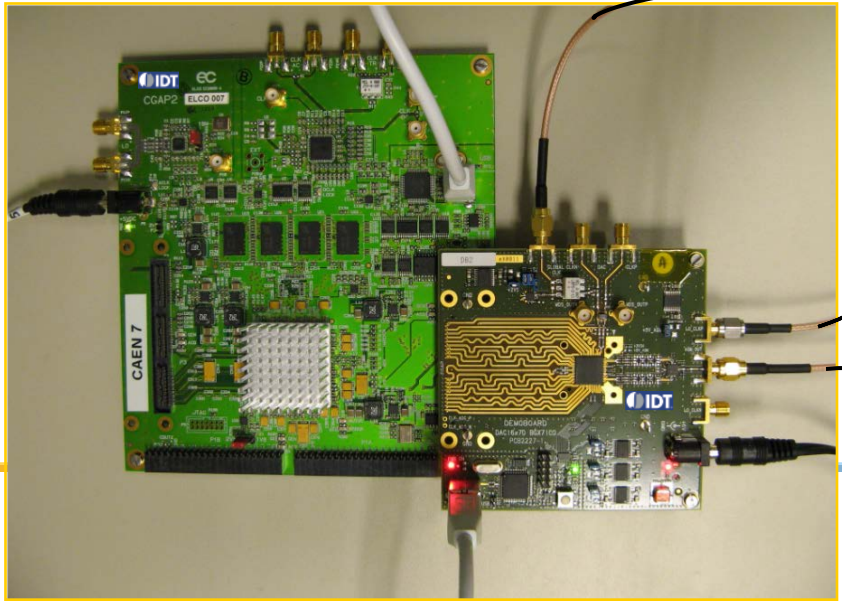
S2: OFF



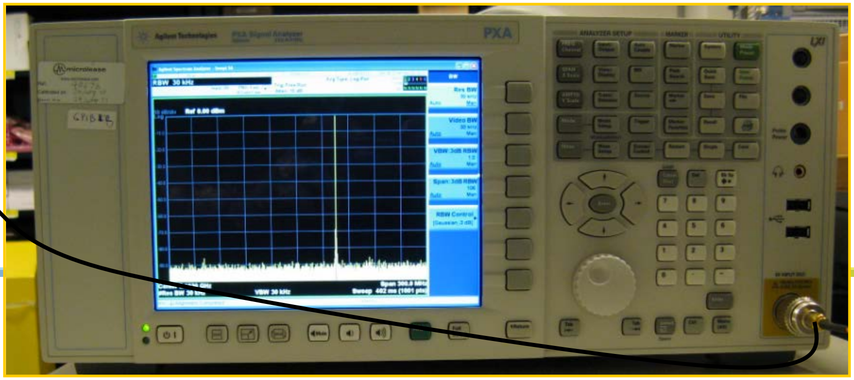
# Bench overview




CLOCKS generation
(Global Clock and LO)

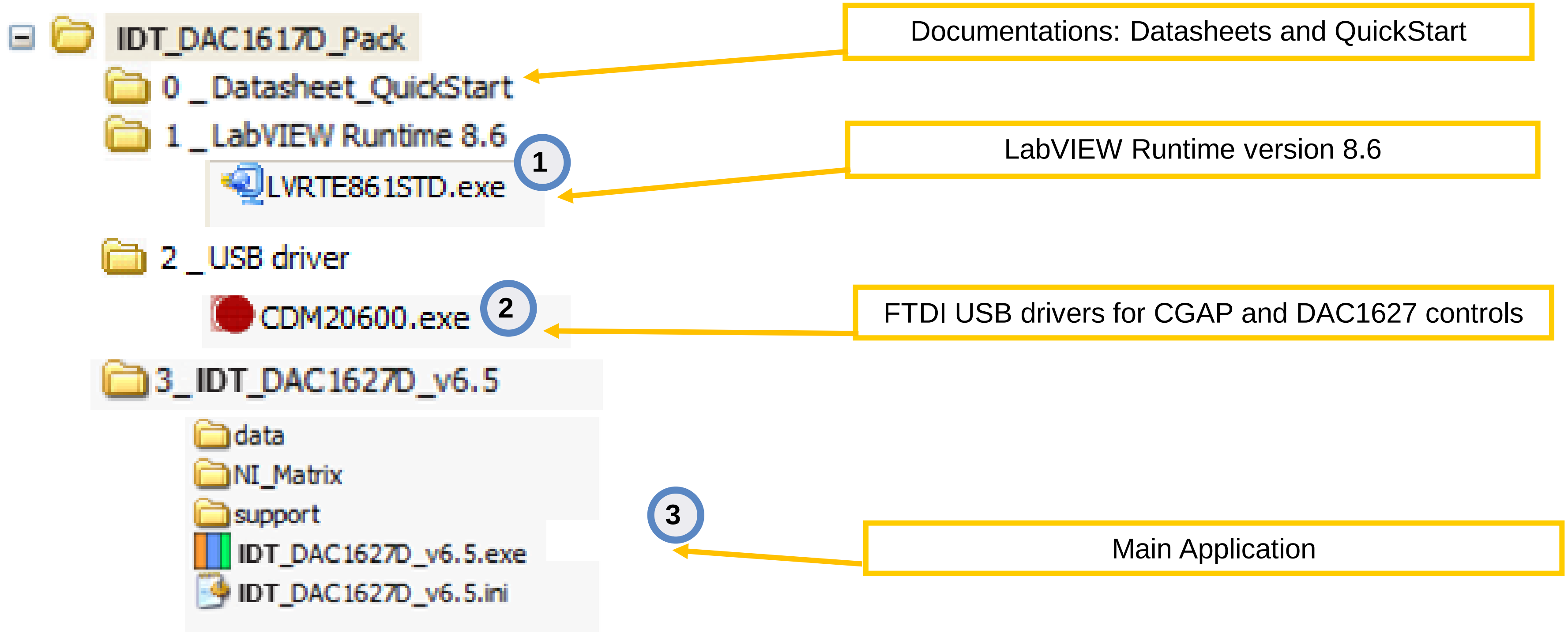



Spectrum measurement



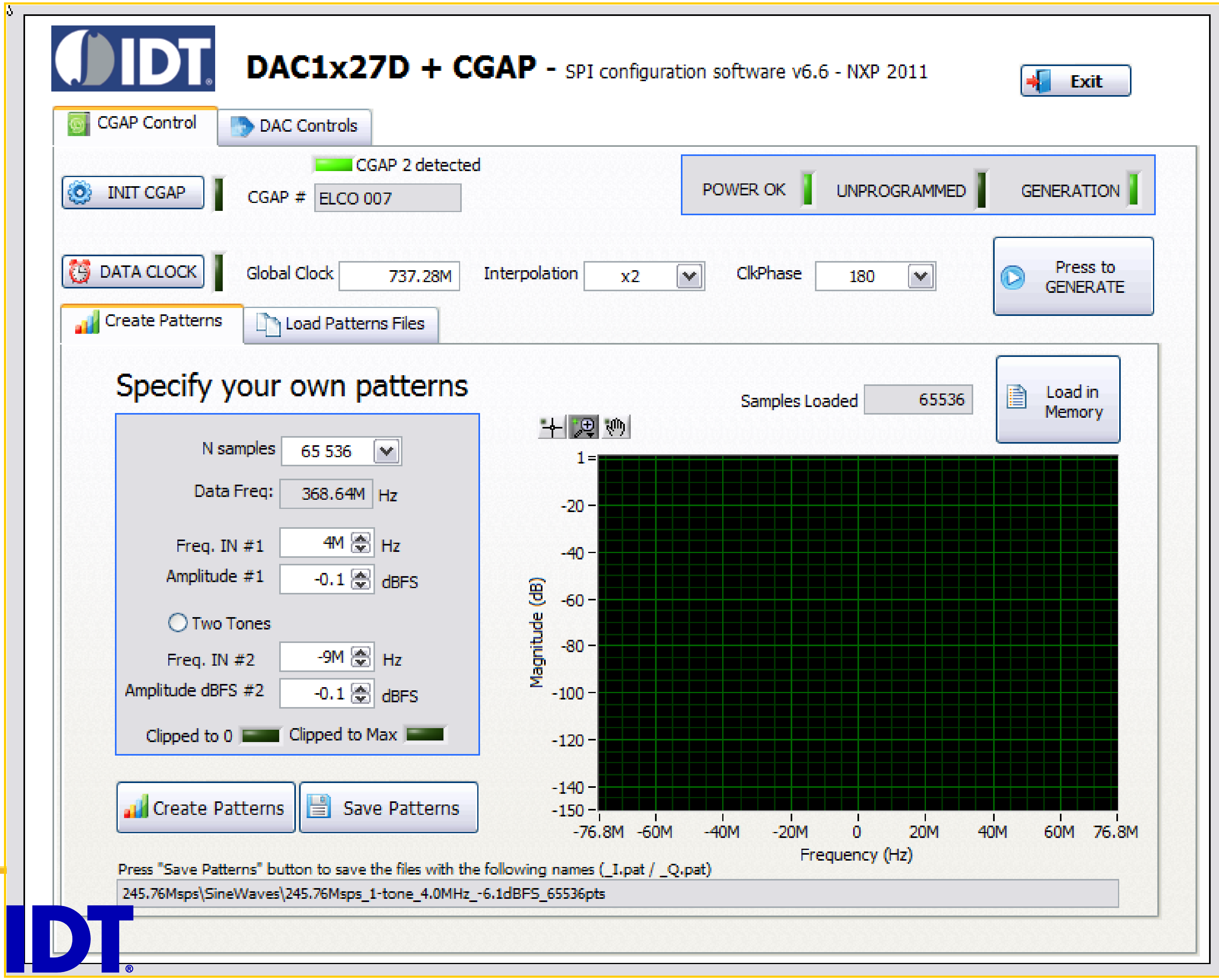
# IDT DAC1627 SPI Software

# Software Folders



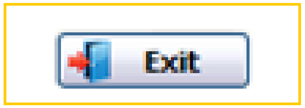

To use the **IDT_DAC1627D** software, the LabVIEW Runtime 8.6 needs to be installed first.
This Runtime could be found on the folder named **1_LabVIEW Runtime 8.6**.
The driver required to access the USB controller on the board could be found in the folder **2_USB driver**

# CGAP board control panel overview



# Warning: Exiting the Program

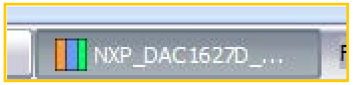
When using the IDT DAC1627D SPI Software, some **USB connexion are opened** between your laptop/desktop and the boards (CGAP2 and DAC board).

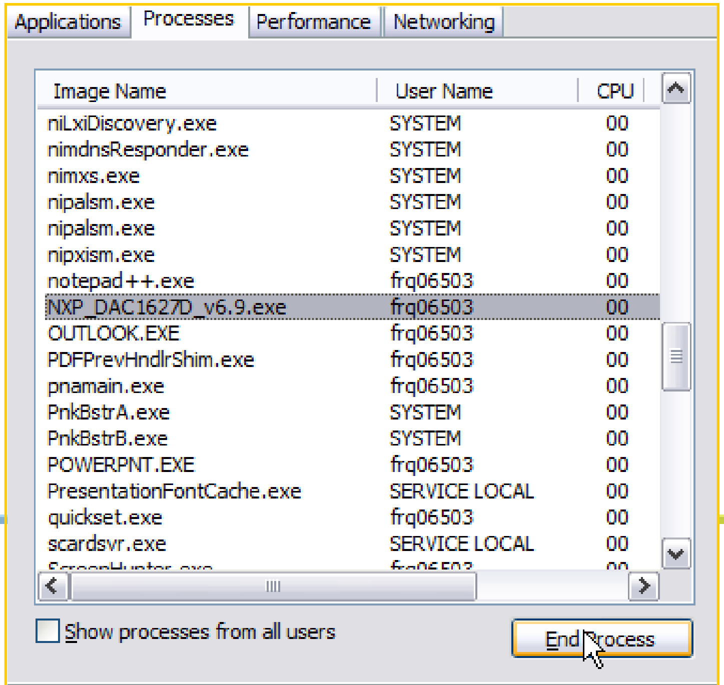



To prevent any hardware issue when closing the program, **please use the EXIT button to close properly the USB connexion.**

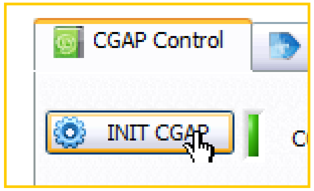
**Do not use the [X] button**, otherwise, the USB connexion will still be alive, and the program won't be closed properly.

**If this happens,** the program will be displayed in the Windows taskbar, but could not be accessed anymore.
**Please use the Task Manager to End the process:**



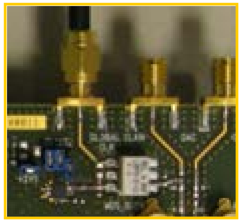



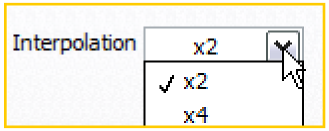
# CGAP board start up sequence



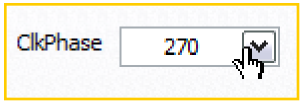

(1) **Initialize** the CGAP board USB controller


(2) Specify the **Global Clock** frequency provided to the DAC board.

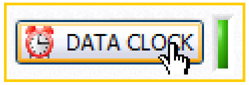





(3) Specify the **interpolation factor** programmed in the DAC1627D.

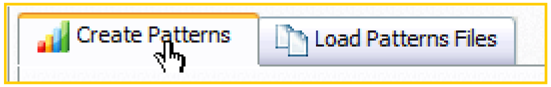



(4) Specify the **clock phase** realtionship between the LVDS clock and the DATA coming from the FPGA.

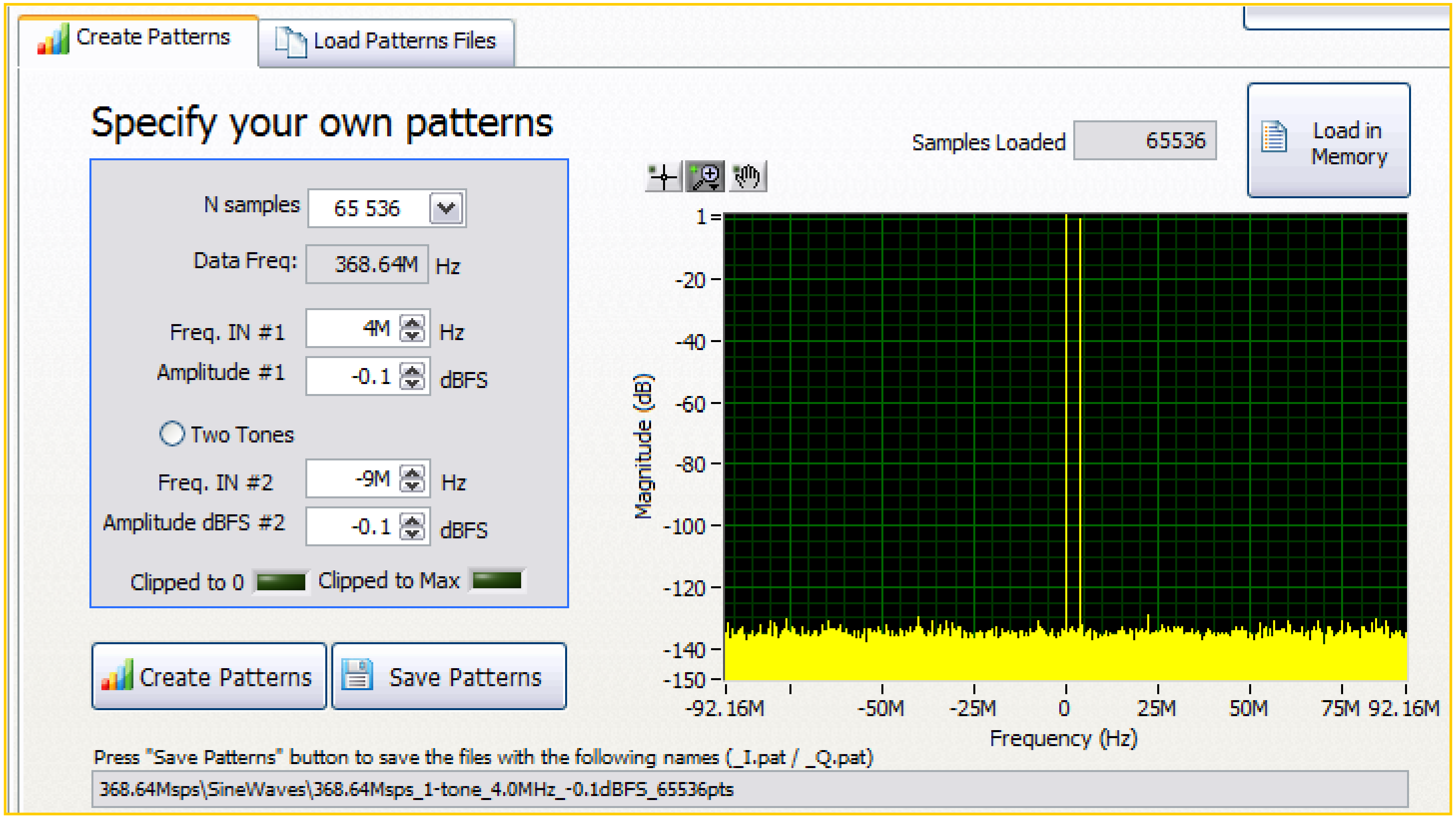



(5) Press the **'DATA CLOCK'** button to configure the CGAP board.

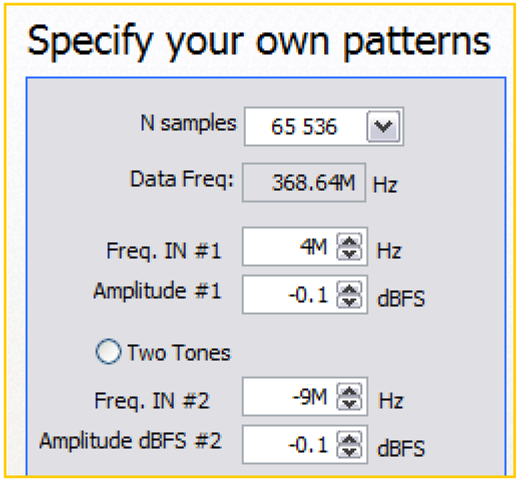
# Create Patterns and program CGAP memories 1/3



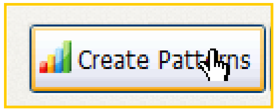

Select the ‘**Create Patterns**’ tab



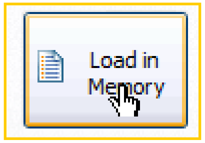
# Create Patterns and program CGAP memories 2/3




(a) Select the number **N of samples**
(b) The Data Frequency is automatically preset from the **Global clock** value and the **interpolation factor**
(c) Specify the **Frequency** of the first tone (Hz)
(d) Specify the **Amplitude** of the first tone (dBFS)
(e) Click '**Two Tones**' if needed
(f) Specify the **Frequency** of the second tone (Hz)
(g) Specify the **Amplitude** of the second tone (dBFS)

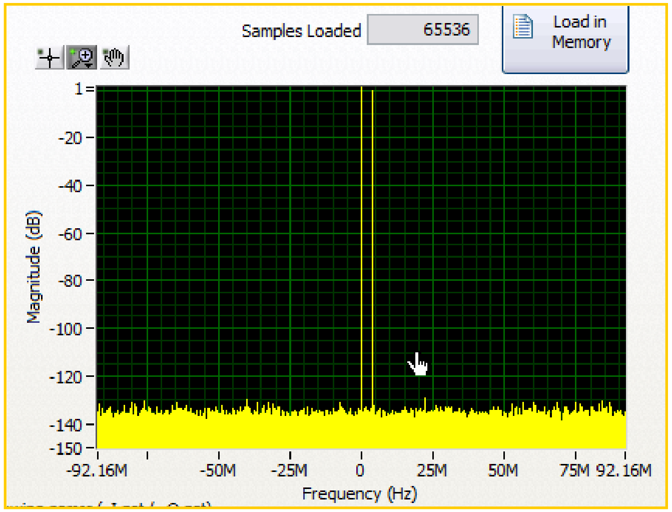


Press **'Create Patterns'** button to generate the signal (I and Q patterns are generated at the same time)



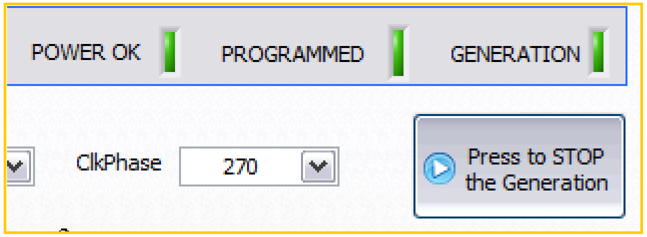
Press '**Load in Memory**' button to load the pattern files to the CGAP board memories.

# Create Patterns and program CGAP memories 3/3




The **complex spectrum** of the **generated signal** is displayed.

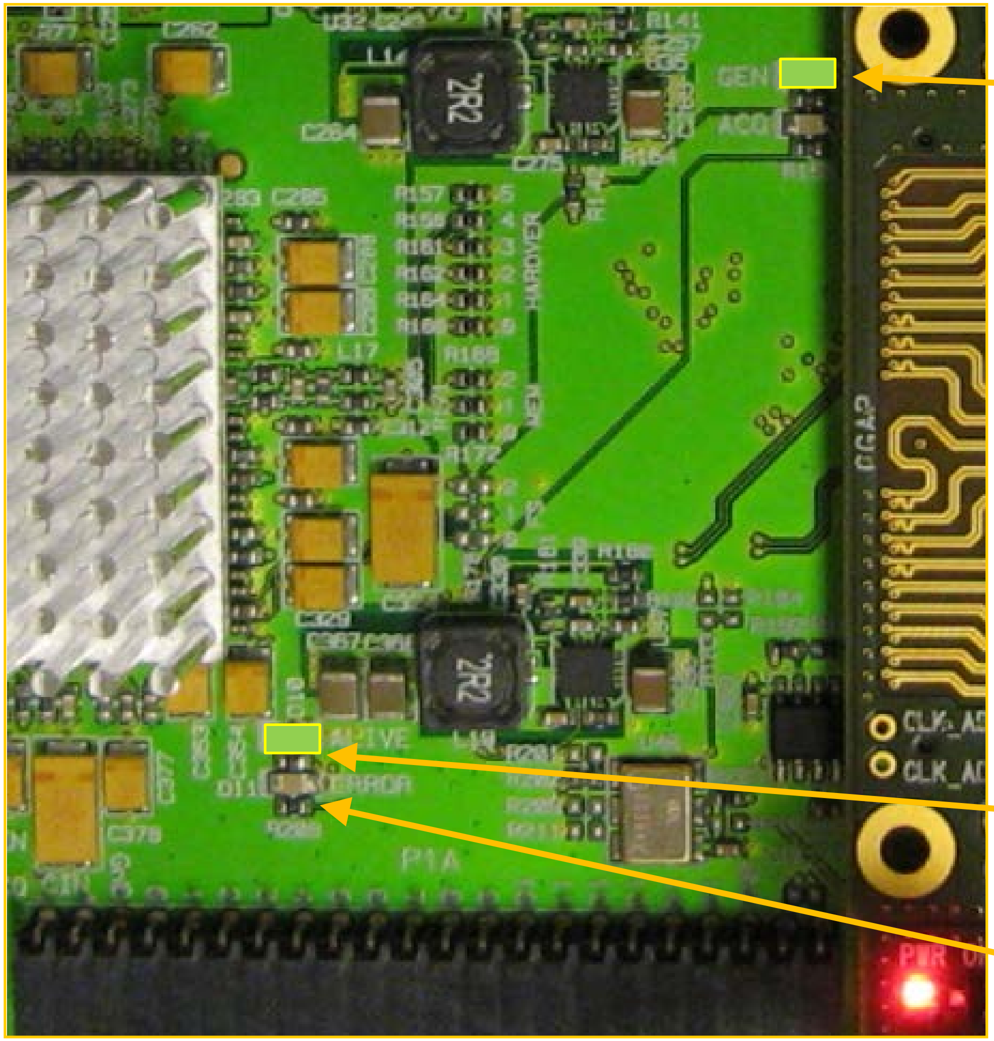

The **size** of the pattern indicator is refreshed.




The LED indicators diplays the **status of the CGAP board** (Programmed and Generation)

**The generation** of the signal is **automatically** enabled after the « Load in Memory » action.

# LED Status of the CGAP board



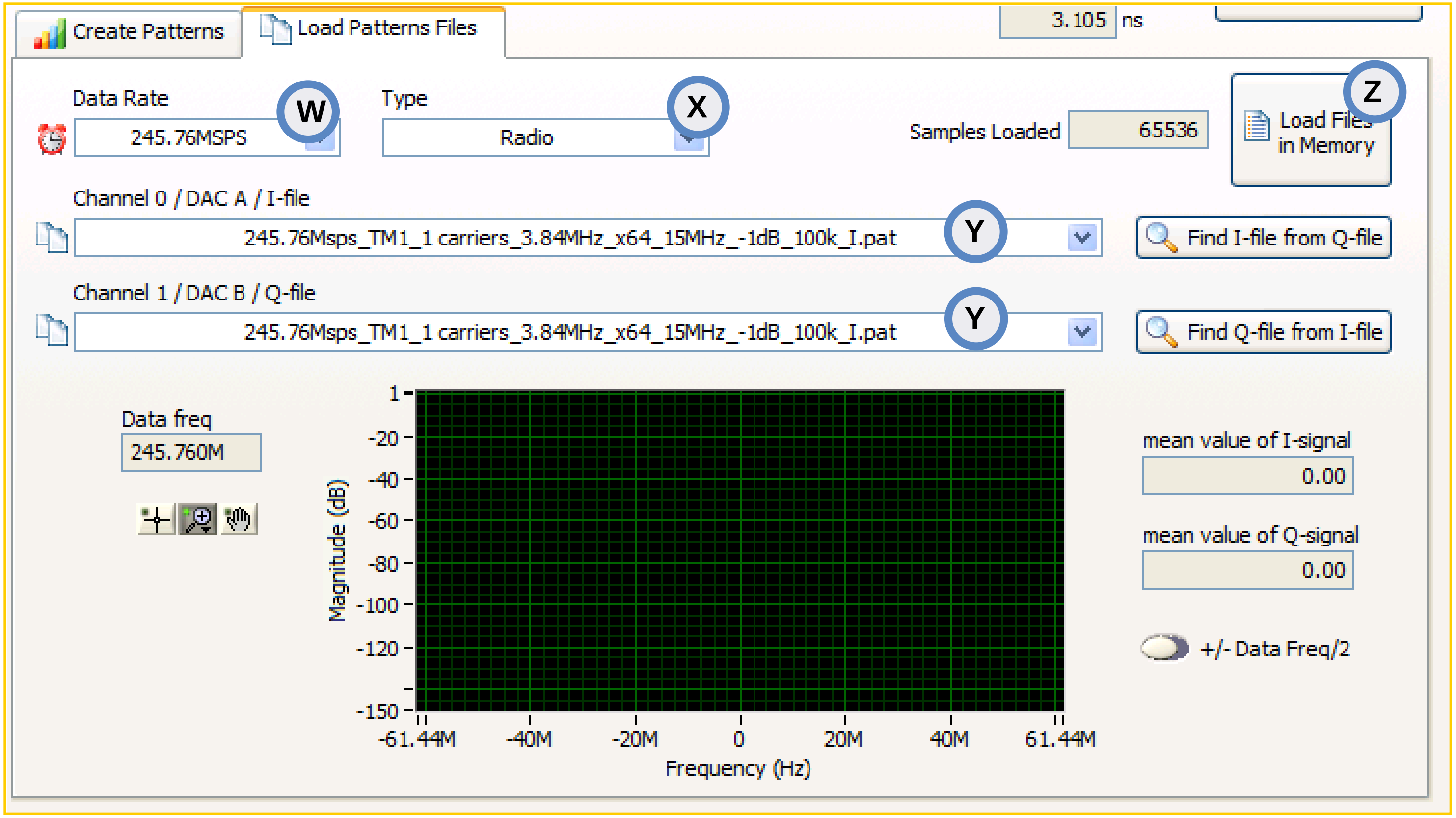

When Generation is in progress, the GEN LED is ON (green)

When the clock configuration is correctly set, the ALIVE LED is blinking (green).

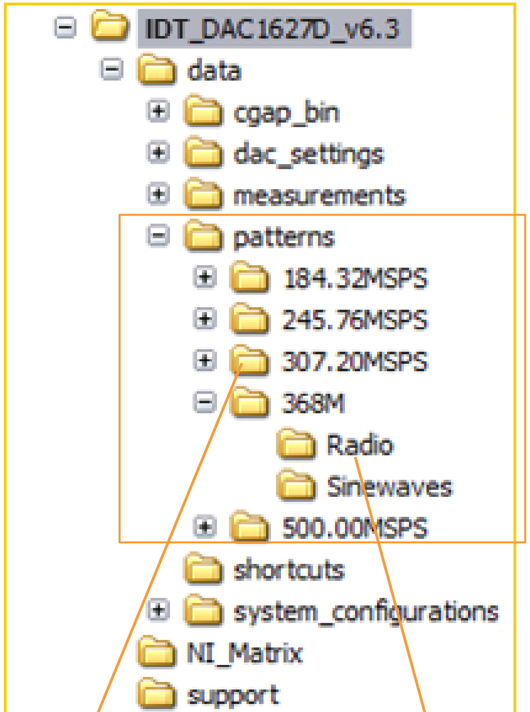
When the ERROR LED is blinking (red), the clock configuration need to be resent.

# Load Patterns Files

Some patterns are already available with the software.
You need to specify the **DATA rate** (w) and the **type** (x) of signals (Radio or Sines waves).
Then, **I-file** and **Q-file** need to be selected (y).
Press **Load in Memory** (z) to store the pattern in the FPGA memory



# Load Patterns and program CGAP memories




In the « **patterns** » folder, several subfolders are provided containing various pattern types regarding the expected frequency of the DATA signal.

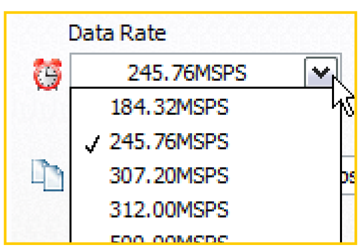
Each subfolder is splitted in two subfolders names **Radio** and **Sinewaves**.

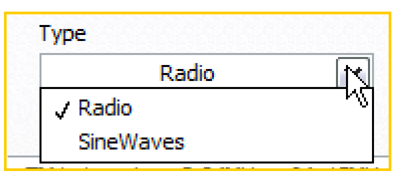
The **Radio** subfolder contains the Radio complex patterns (WCDMA, GSM, etc).

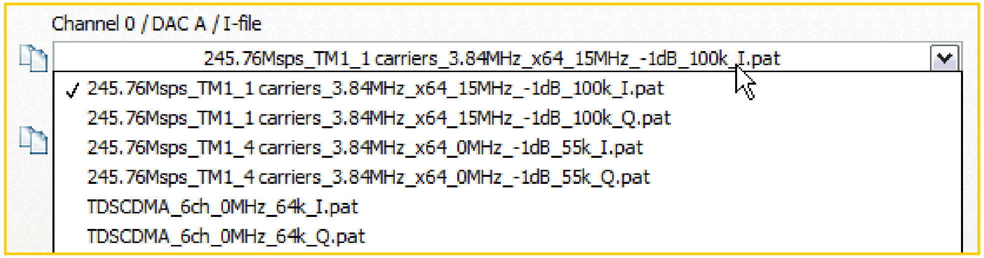
The **Sinewaves** subfolder contains the basic single or dual tones signals.

Any patterns could be added to this subset, please contact your local AE to know more about this process.

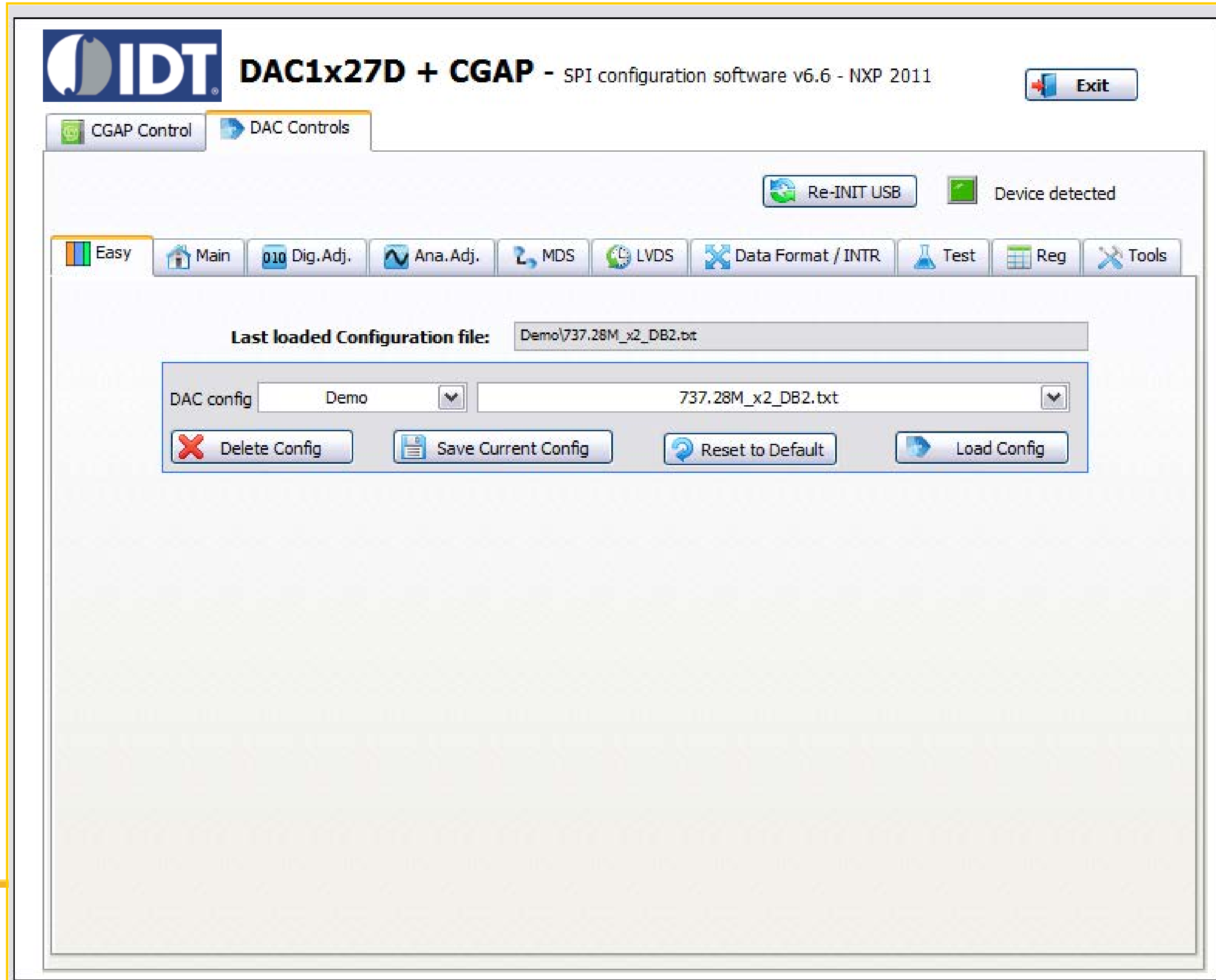
This structure is represented in the same way in the GUI.



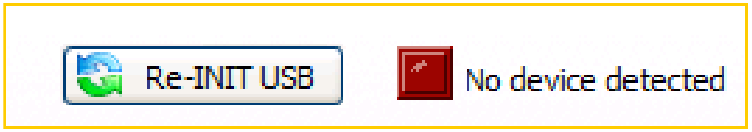



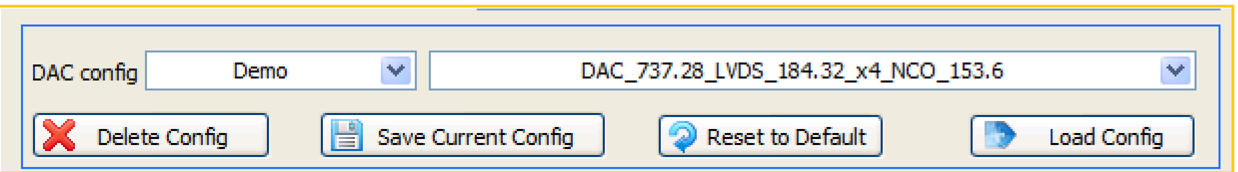
# DAC controls panel overview



# DAC controls main features

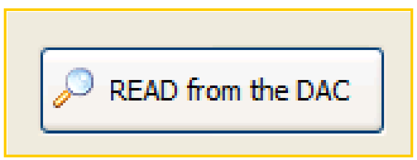



You first need to press **Re-INIT USB** device to be sure that the PC is able to communicate with the DAC1617D

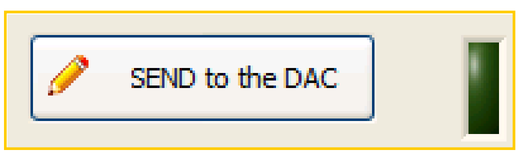



Some SPI settings are already available in the DAC Config boxes.
Select the right one, and Press **Load Config** button.
You can reset the device by pressing **Reset to Default** button.

**On all DAC tab:**




All the registers could be read to update the Graphical User Interface by pressing **READ from the DAC** button.



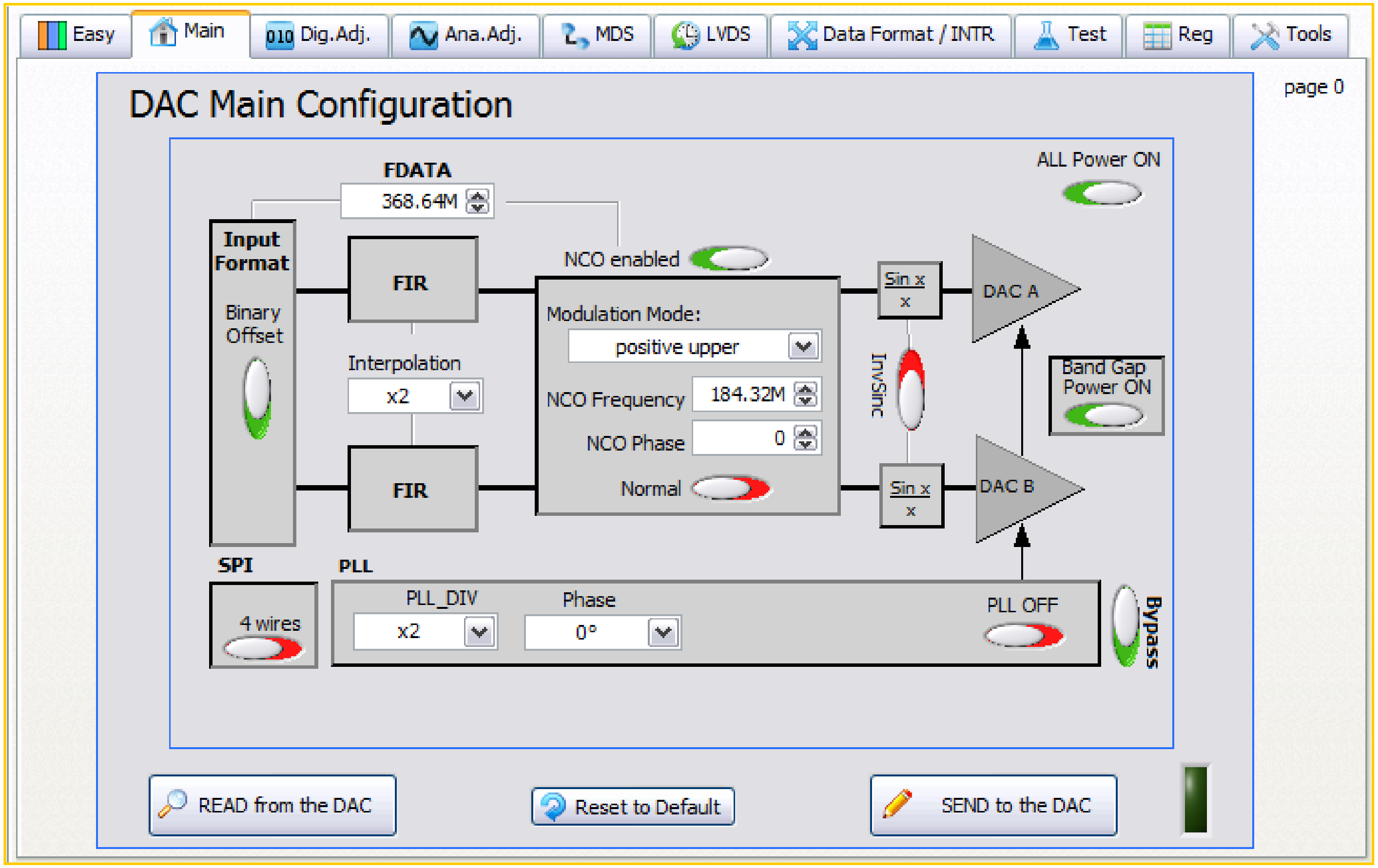

All the registers could be written by pressing **SEND to the DAC** button.

When **entering each TAB**, a **self refresh feature** is enabled to display the **real content** of the **DAC device**.

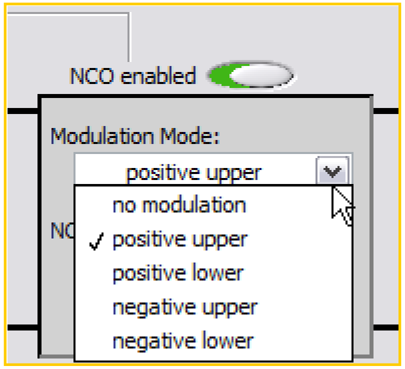
IDT

# DAC Main Configuration

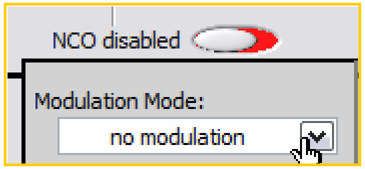
Main parameters of the DAC settings (NCO, interpolation) could be programmed from the Main tab.



# NCO enable / disable



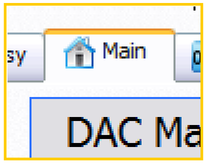

When using the NCO, **don't forget to specify** the **type of modulation**.
**Positive** or **negative** refers to the position of the final signal compare to the LO position after the Iqmod.
**Upper** and **Lower** refers to the position of the signal compare to the NCO position.



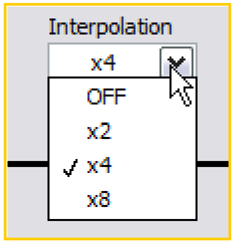

When disabling the NCO, **don't forget to specify** **no modulation.**

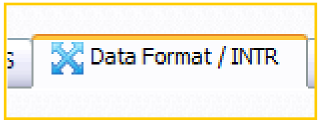
# Interpolation factor

The interpolation factor need to be specified in two pages.

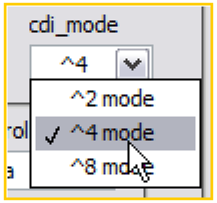



In the **Main** tab, please specify the **interpolation** ratio ➔




In the **Data Format / INTR** tab, please specify the **CDI** mode ➔

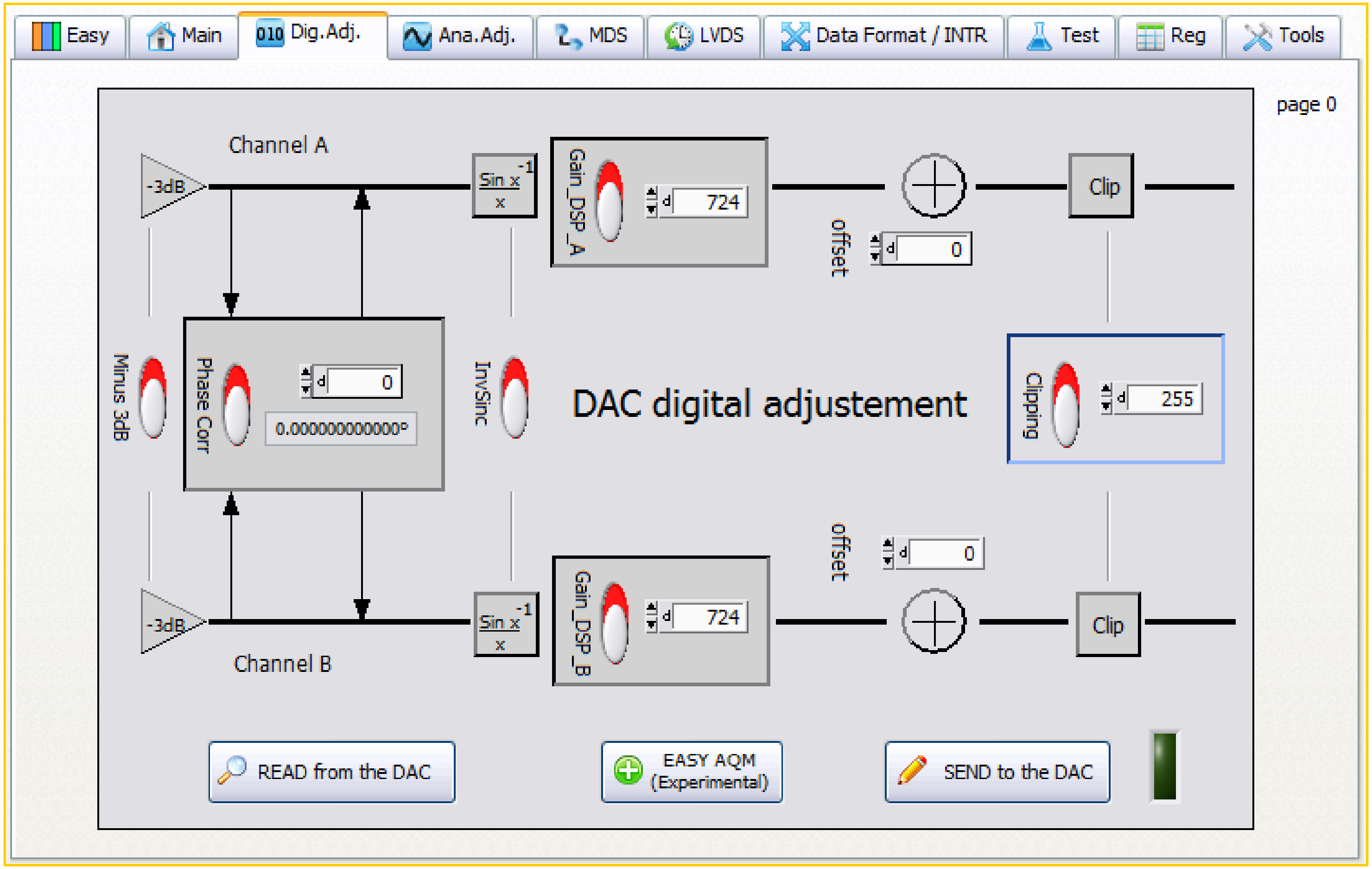



Please respect the follwing table :

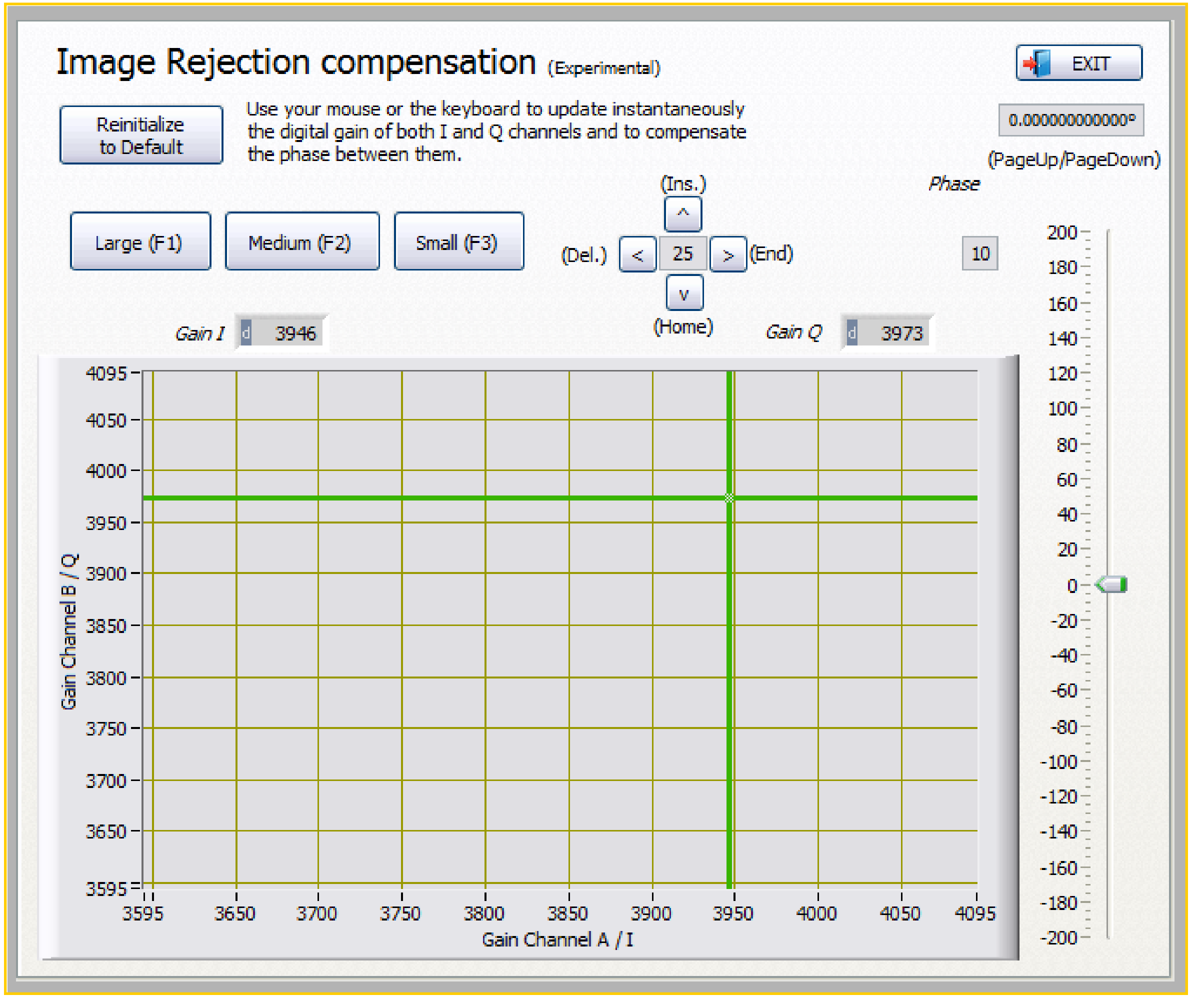
| Interpolation | CDI mode |
|---|---|
| x2 | ^2 mode |
| x4 | ^4 mode |
| x8 | ^8 mode |

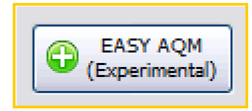
# DAC digital Adjustement

DAC digital tuning tab allows to update digital gain, phase correction, clipping of the I/Q channels to help the I/Q balance at the AQM input.



# Image Rejection compensation (experimental)



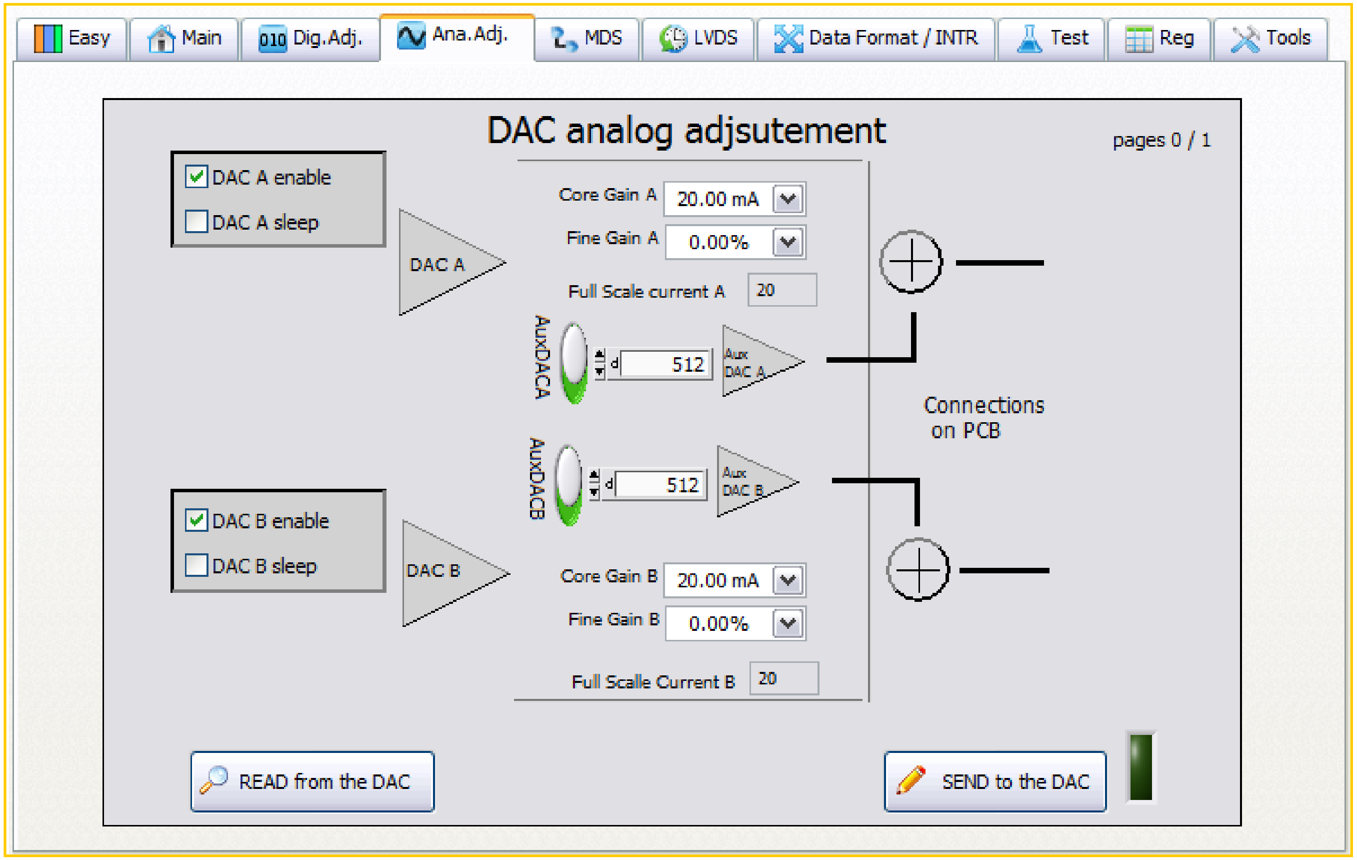

The Image Rejection compensation window allows to instantaneously update the I/Q gain and the phase compensation.

Mouse or keyboard interface could be use to update the values.

Notice: This feature is experimental for the moment, and could show some bugs.

# DAC analog adjustement

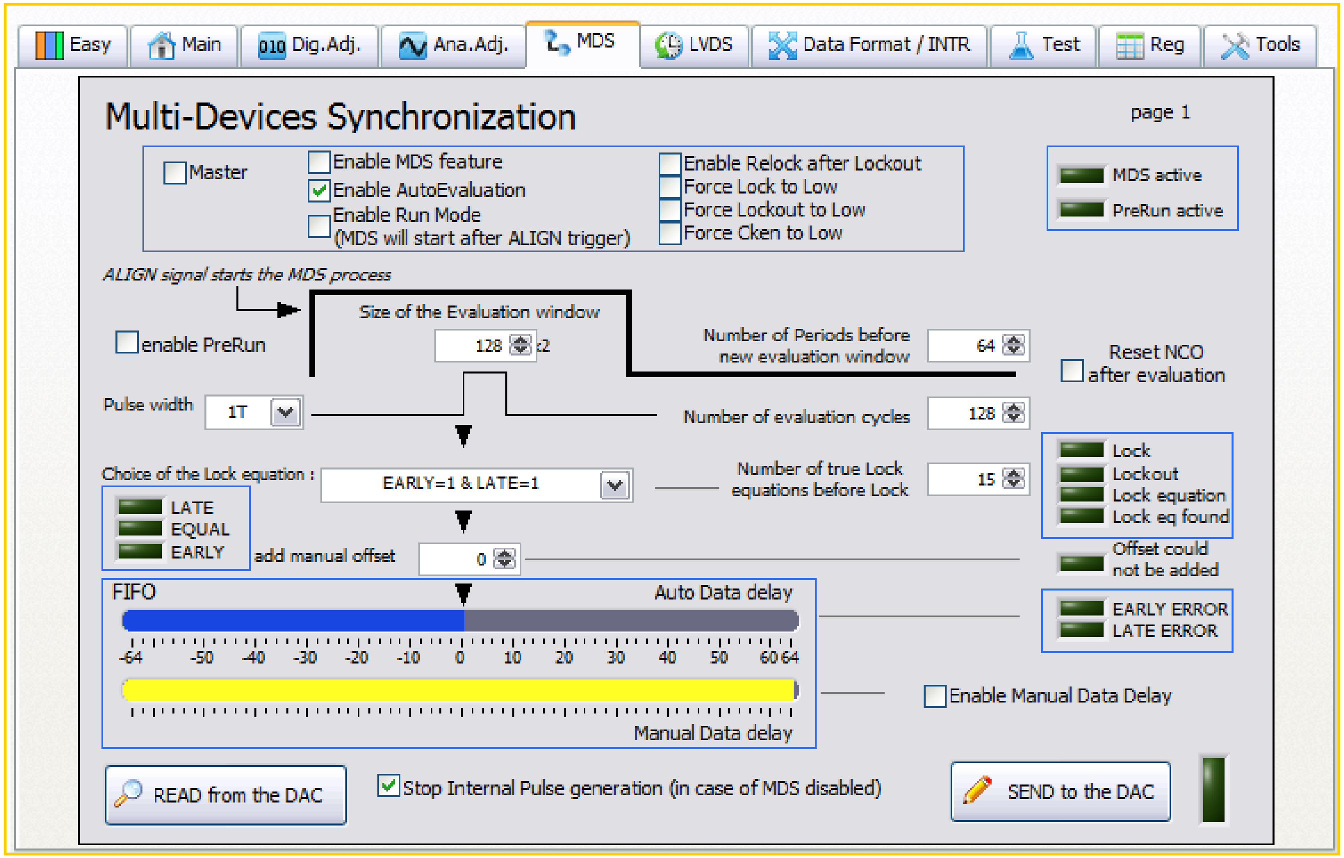
DAC analog tuning tab allows to update the analog gain, the auxiliary DACs.




IDT

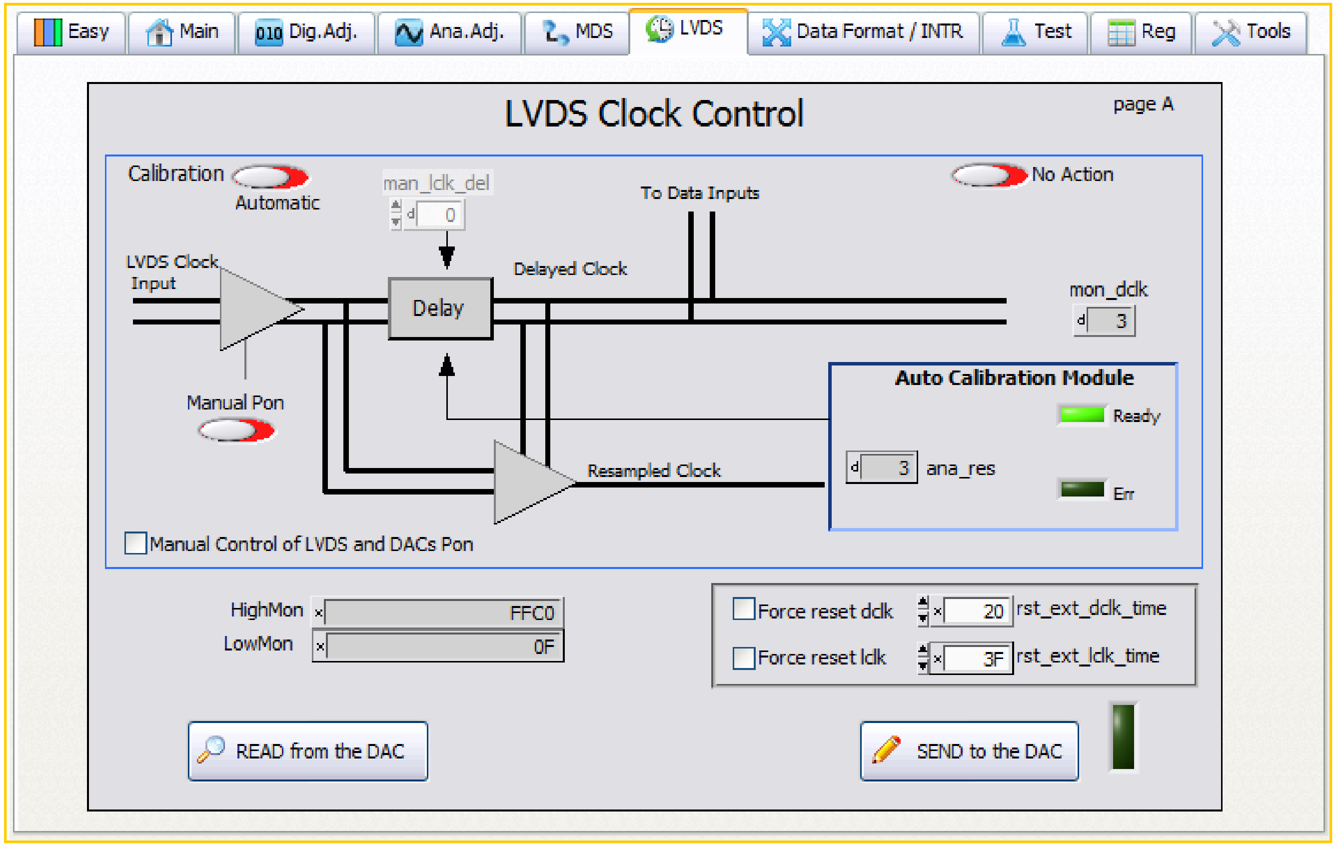
# Multi Devices Synchronization

MDS tab allows to tune the settings for the multi devices synchronization.



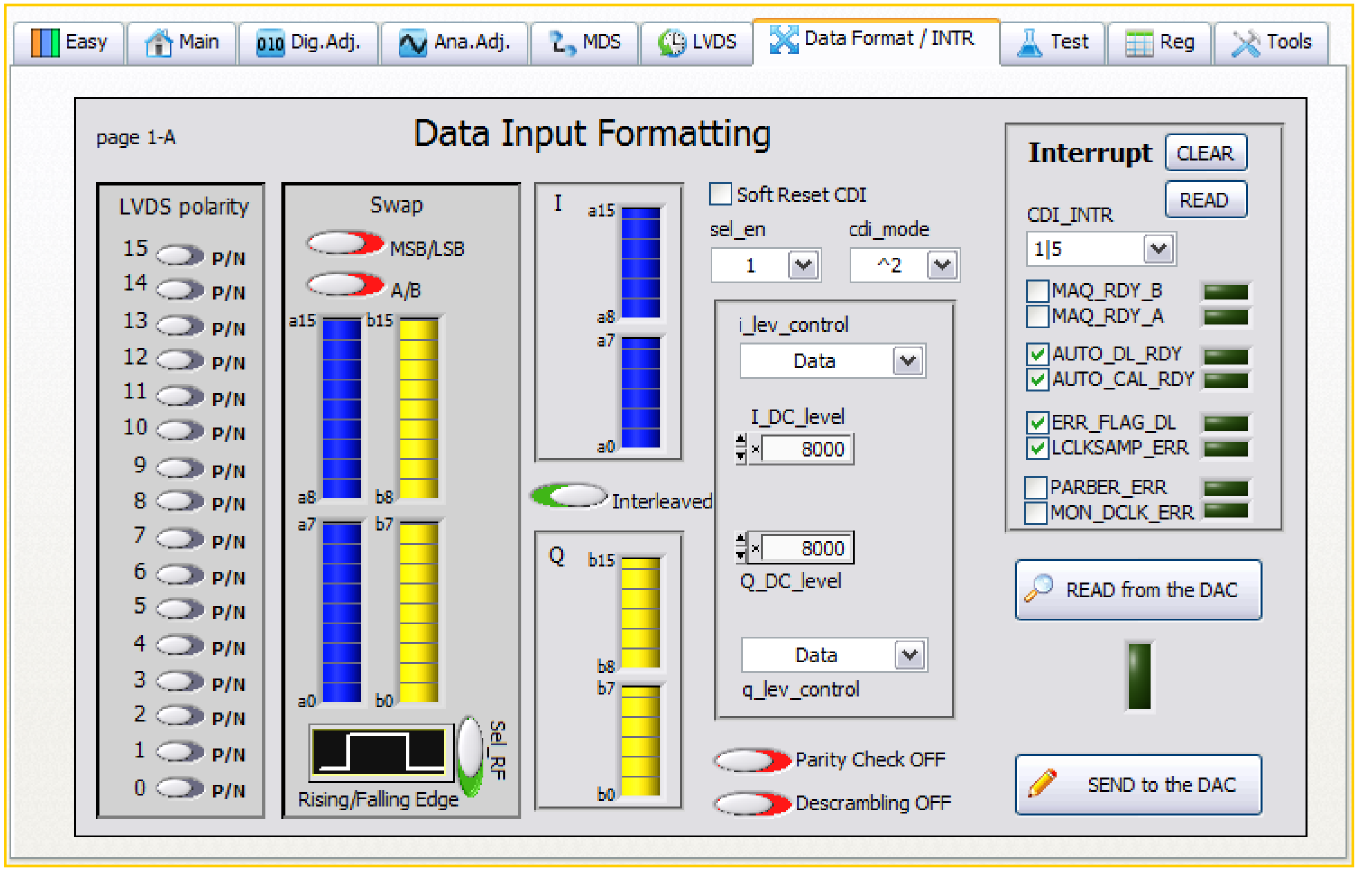
# LVDS Clock Control

LVDS buffer are automatically calibrated with regard to the LVDS clock input.
The tab allows to enable/disable the automatic/manual calibration.

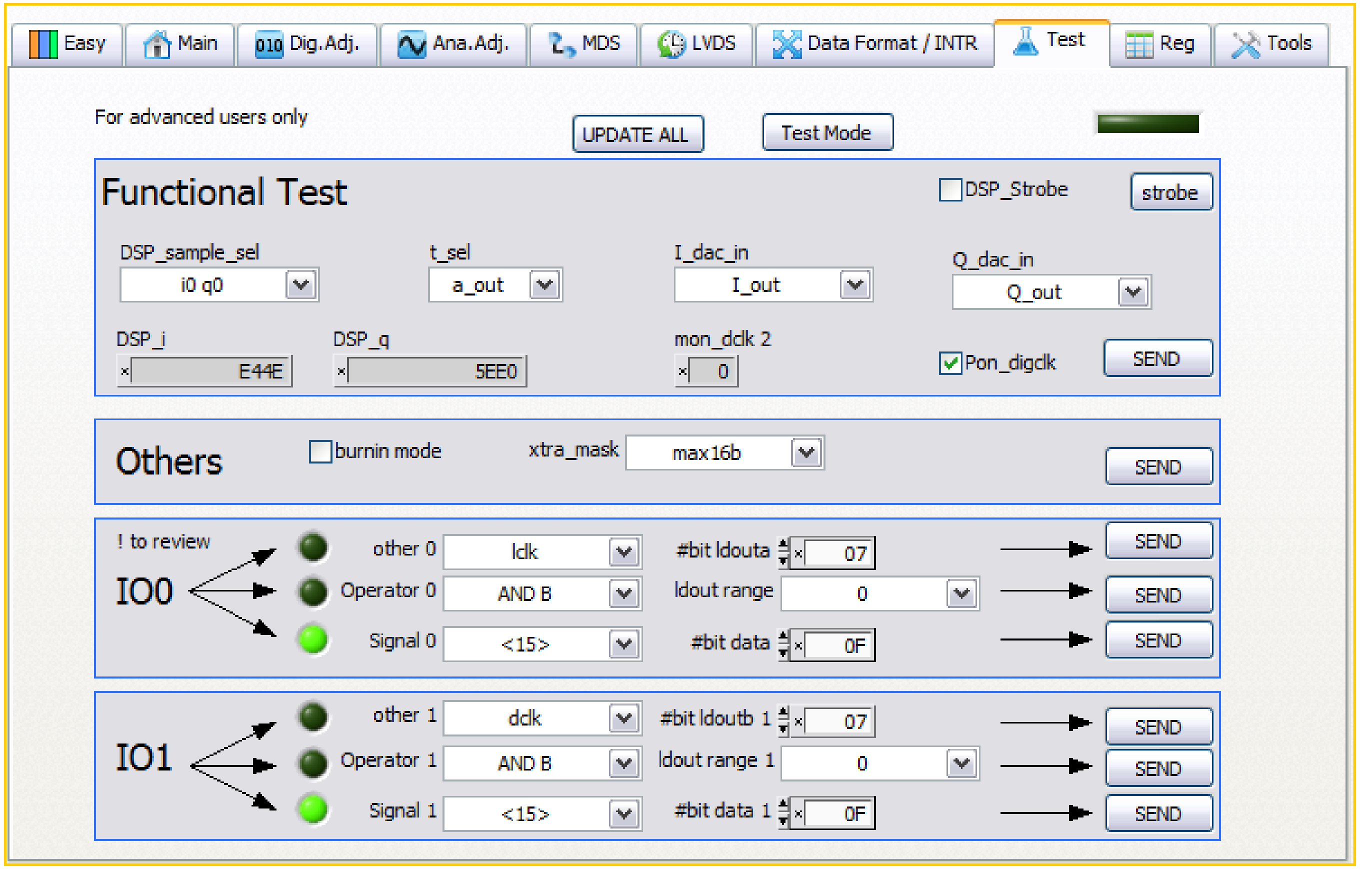


# Data Input Formatting

Interleace/Folded, bit inversions of the input interface could be set up in the Data input formatting tab.

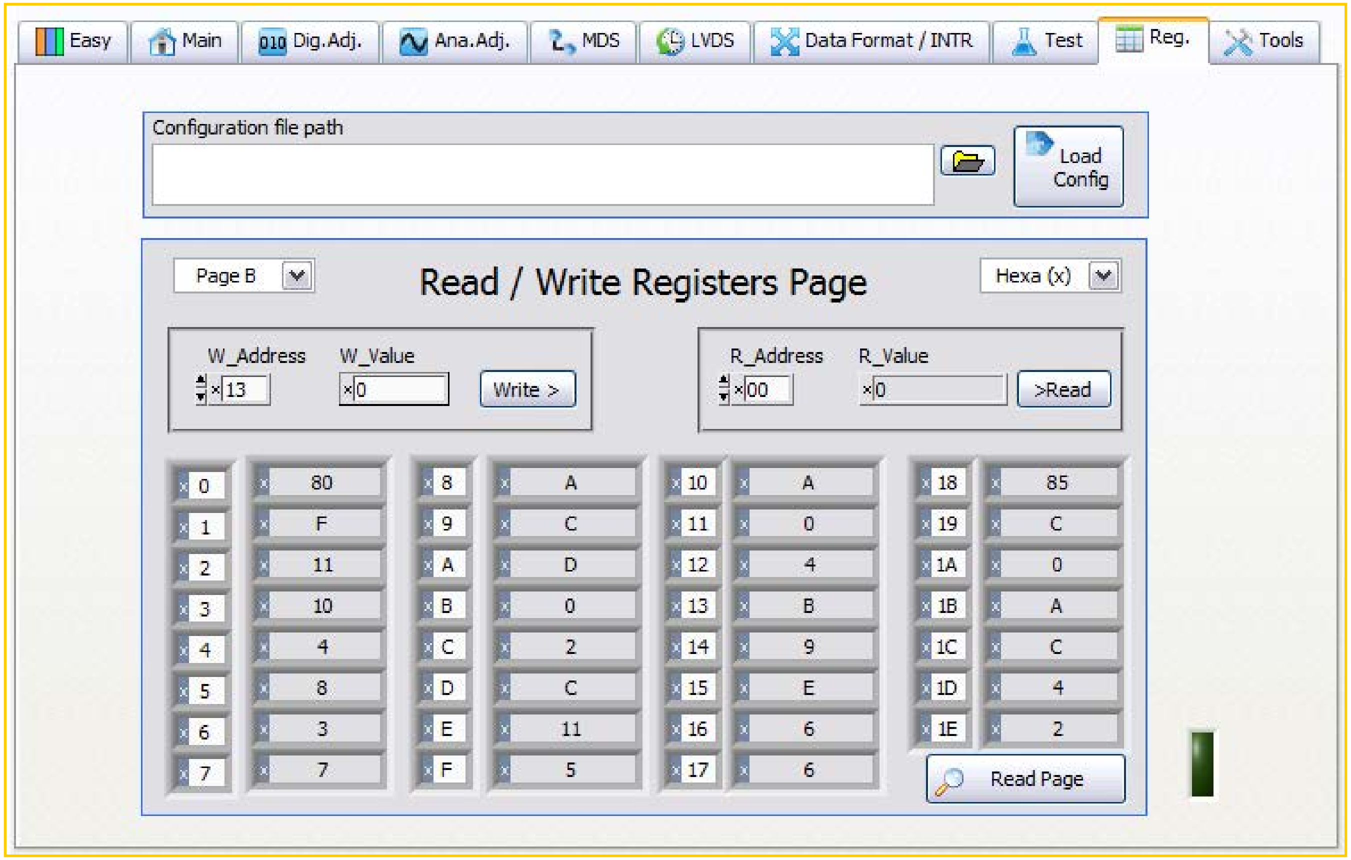


# Test


Easy
Main
Dig.Adj.
Ana.Adj.
MDS
LVDS
Data Format / INTR
Test
Reg
Tools
For advanced users only
UPDATE ALL
Test Mode
Functional Test
DSP_Strobe
strobe
DSP_sample_sel
i0 q0
t_sel
a_out
I_dac_in
I_out
Q_dac_in
Q_out
DSP_i
E44E
DSP_q
5EE0
mon_dclk 2
0
Pon_digclk
SEND
Others
burnin mode
xtra_mask
max16b
SEND
! to review
IO0
other 0
lclk
Operator 0
AND B
Signal 0
<15>
#bit ldouta
07
ldout range
0
#bit data
0F
SEND
SEND
SEND
IO1
other 1
dclk
Operator 1
AND B
Signal 1
<15>
#bit ldoutb 1
07
ldout range 1
0
#bit data 1
0F
SEND
SEND
SEND

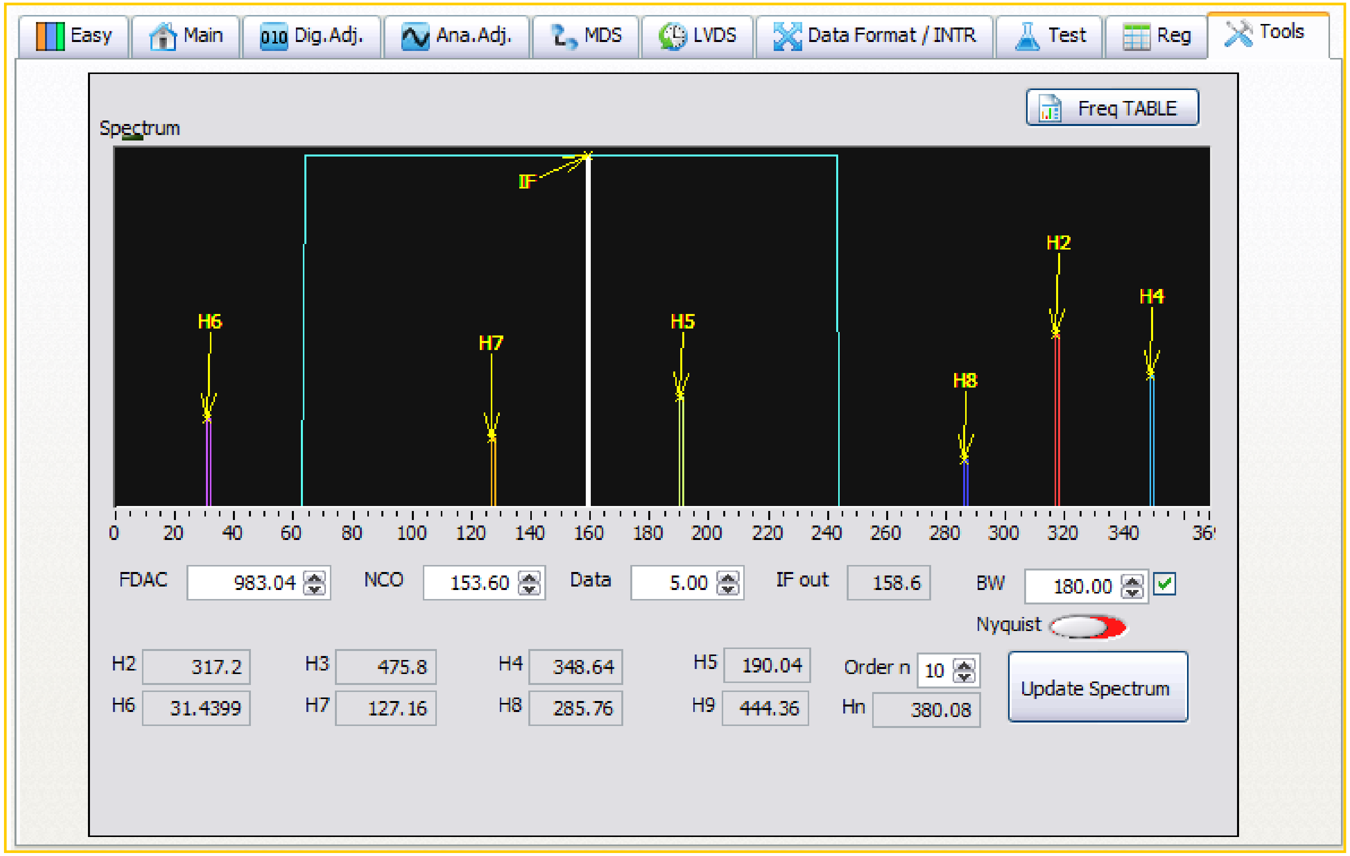
# Registers

All the registers pages could be read and save from the Registers tab.



# Tools

Tools tab allows to see the output spectrum related to the folded image at the DAC output.



# Spectral measurements

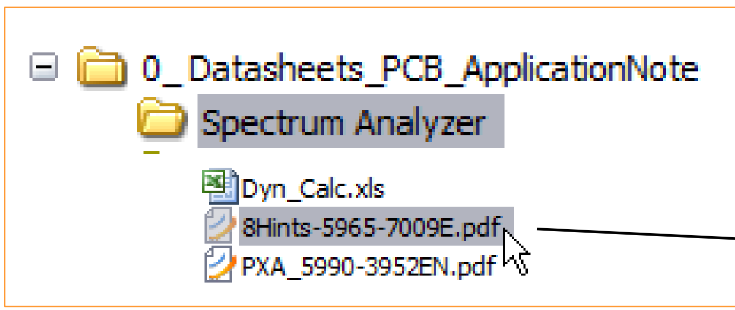
## How to correctly setup your spectrum analyzer?

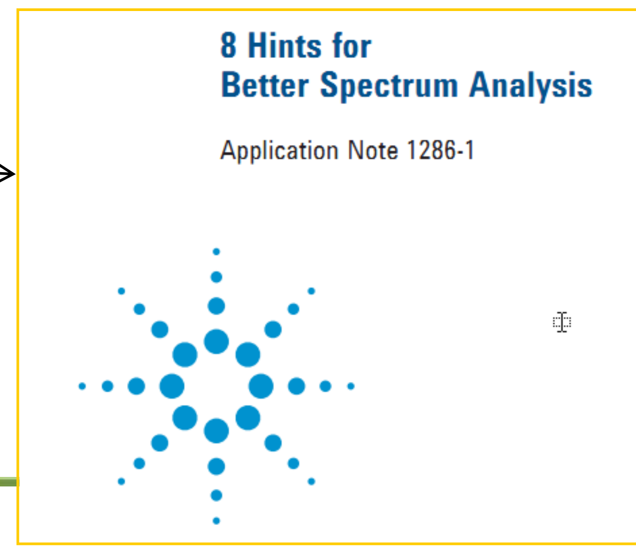
# How to specify the correct settings for the Spectrum analyzer?

**DAC1627D** and **BGX7100** provides **high end performances**, therefore, a correct measurement setup need to be established to get the real performances of the devices (and not the bad performances of the spectrum).

Please refers to the Application Note from **Agilent** to **correctly setup the Spectrum**.

Same way of working could be used for **R&S** equipment.



# How to specify the correct settings for the Spectrum analyzer?

**Mixer** will created **second** and **third order distorsion** if too much power is send at its input.

**Attenuation** needs to be correctly set up **to avoid the mixer's distorsion** to occur.

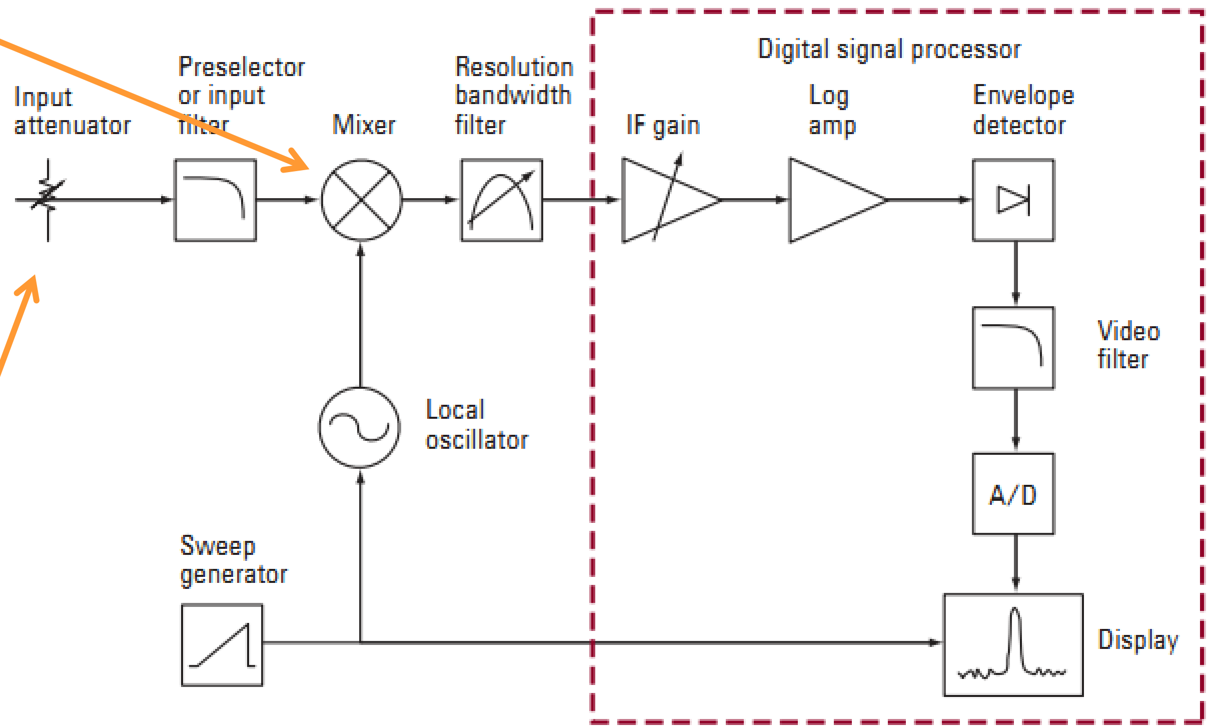



Figure 2. Block diagram of a superheterodyne spectrum analyzer

# How to specify the correct settings for the Spectrum analyzer?

You need to find **the optimum mixer levels** to avoid to measure the distorsion created by the equipment.

**Third order distorsion** created by the Spectrum Analyzer

**Second order distorsion** created by the Spectrum Analyzer

**Displayed Average Noise Level** due to the Resolution BW

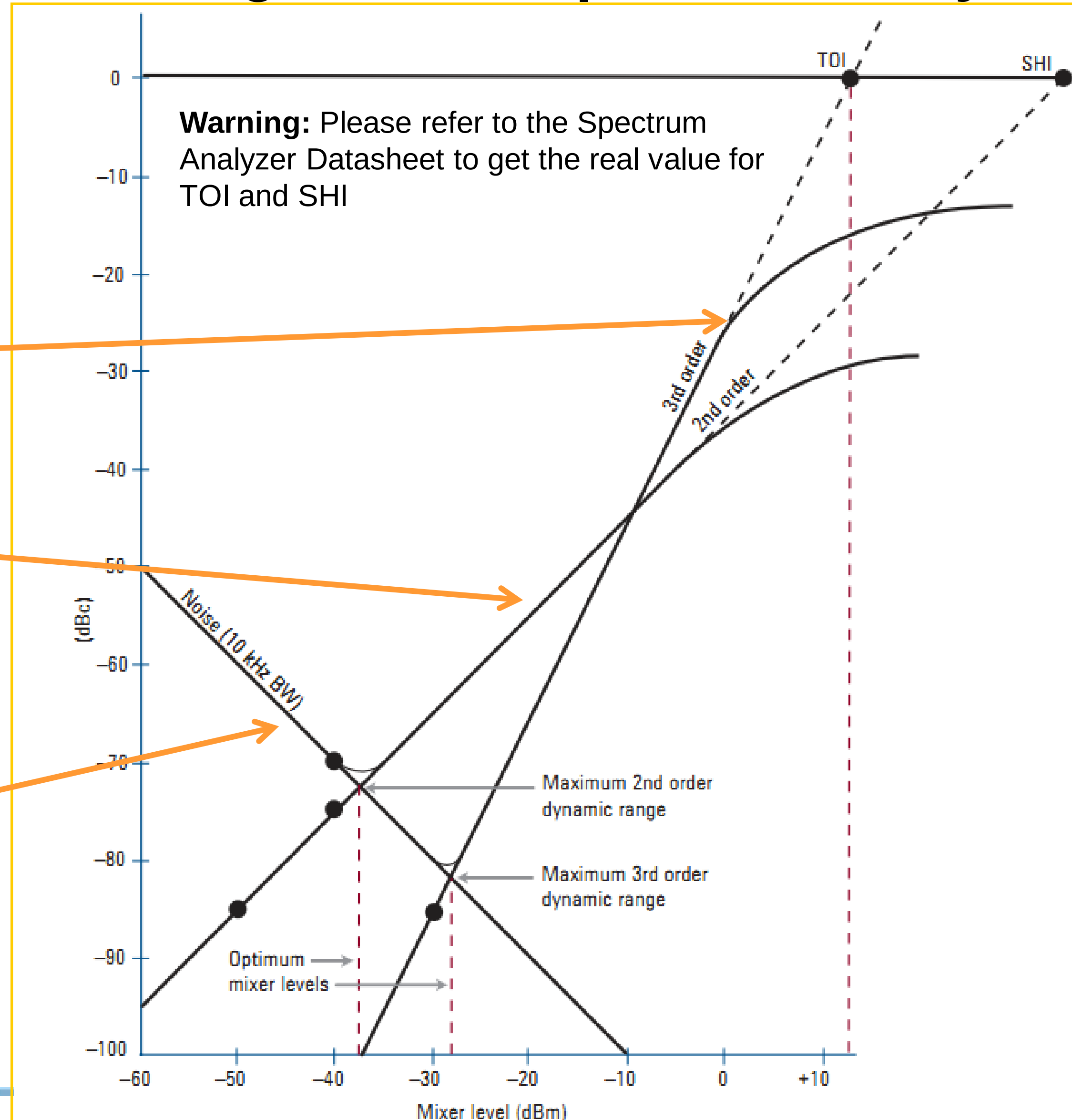



Figure 12. Dynamic range versus distortion and noise

# How to specify the correct settings for the Spectrum analyzer?

When measuring **Second harmonic (H2)** , you need to take care about the **second order distortion** of the analyzer.

**Maximum value** that could be measured from the equipment in this specific settings (RBW).

**Optimum power level** in front of the mixer. The **attenuation** need to be adjusted to fit this parameter.

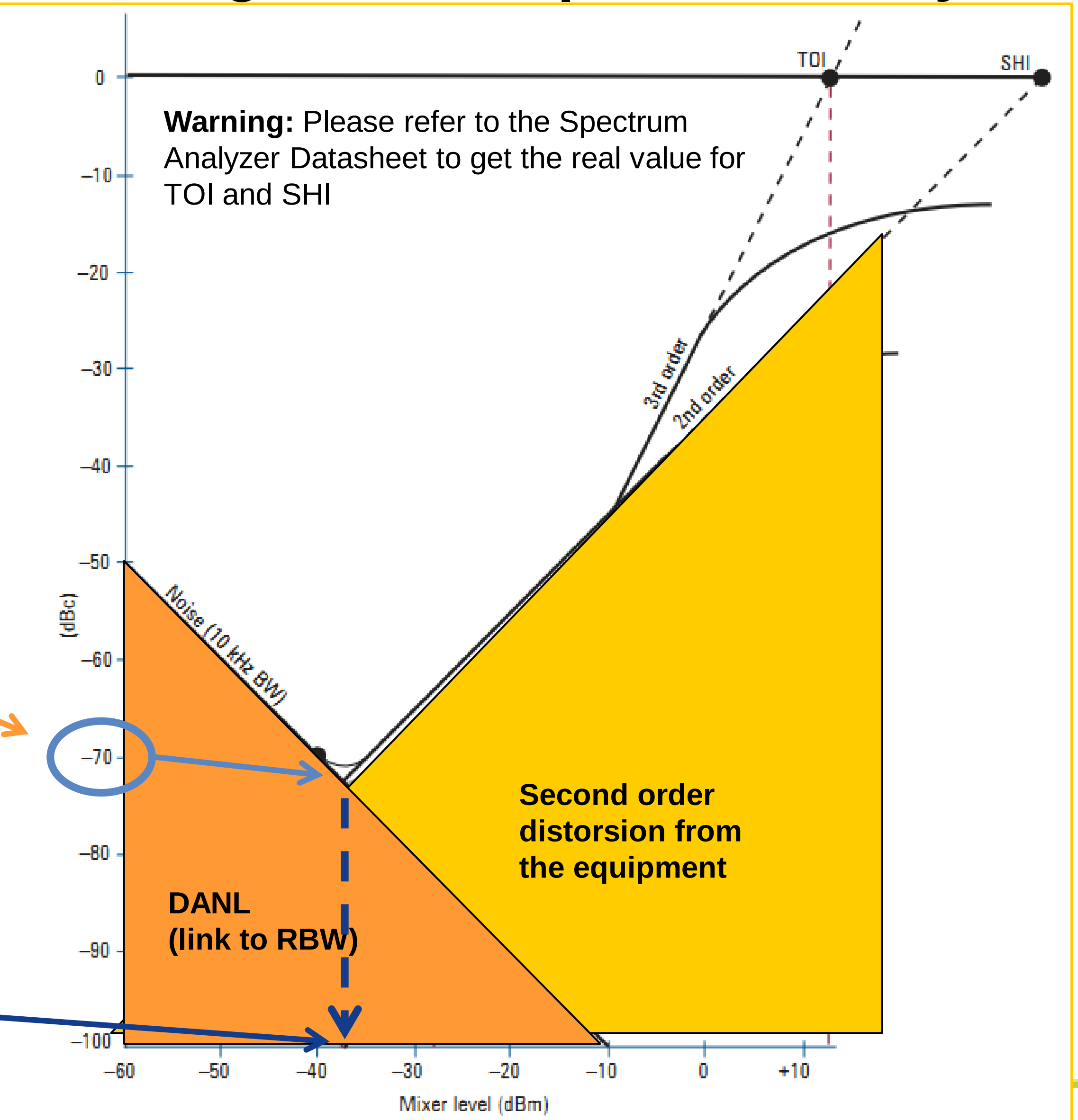



Figure 12. Dynamic range versus distortion and noise

# How to specify the correct settings for the Spectrum analyzer?

When measuring **Inter-Modulation product (IMD3)** , you need to take care about the **third order distorsion** of the analyzer.

**Maximum value** that could be measured from the equipment in this specific settings (RBW).

**Optimum power level** in front of the mixer. The **attenuation** need to be adjusted to fit this parameter.

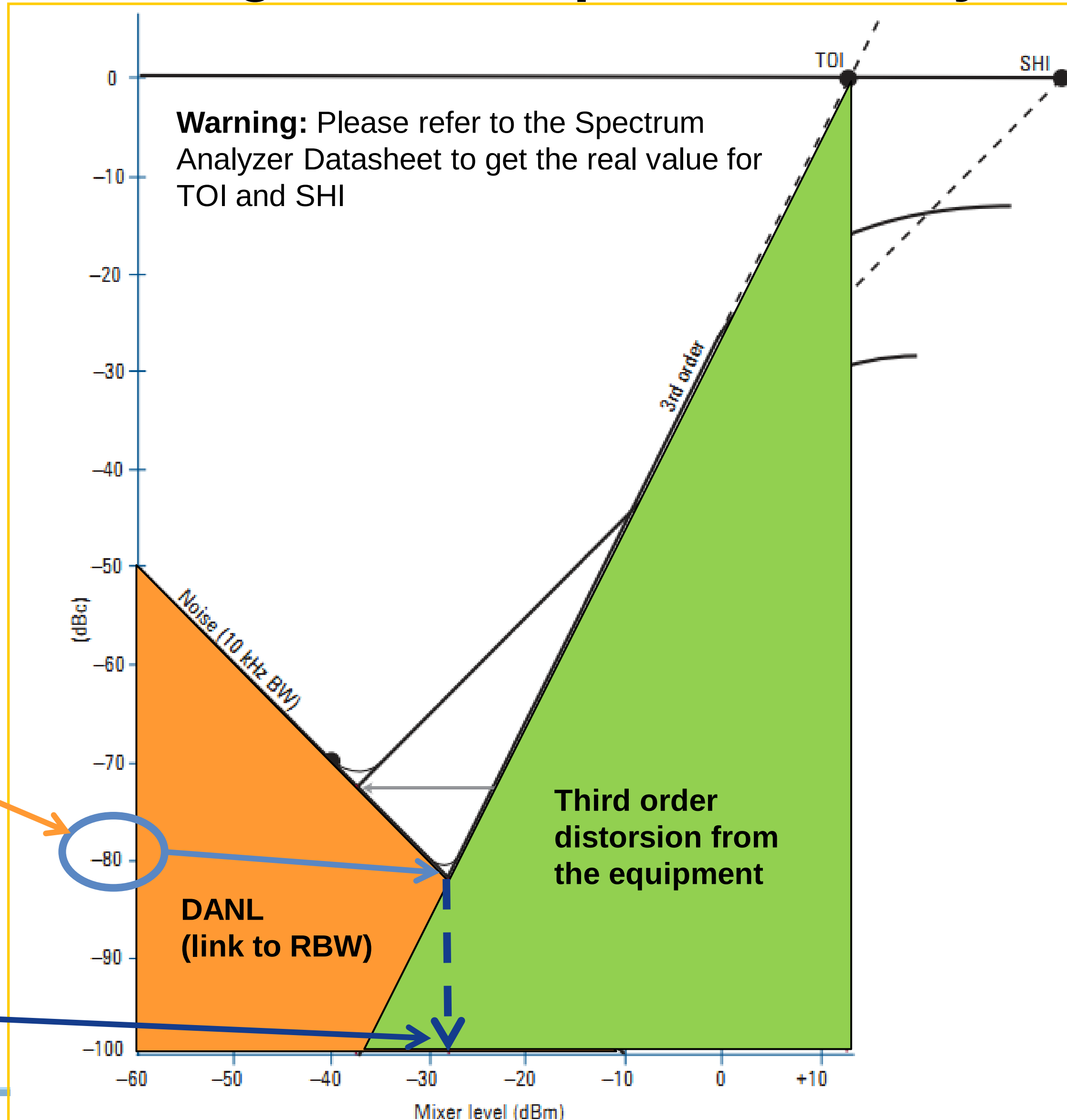



Figure 12. Dynamic range versus distortion and noise

# How to specify the correct settings for the Spectrum analyzer?

You need to find **the optimum mixer levels** to avoid to measure the distorsion created by the equipment.

When measuring a signal of 0dBm power, to avoid to get **H2** coming from the Spectrum analyser mixer, a -40dB attenuator level need to be set (it also depends of the RBW)

If the signal is about -10dBm, then use 30dB of attenuation to get -10 -30 = -40dBm at the mixer input.

When measuring **Intermodulation product (IMD3)** for a -6dBm signal, please use 22dB attenuation to avoid intermodulation product coming from the equipment.
-6-22= -28dBm at the mixer input.

Please update the figures regarding the type of equipment you are using (cf datasheet of the equipment).

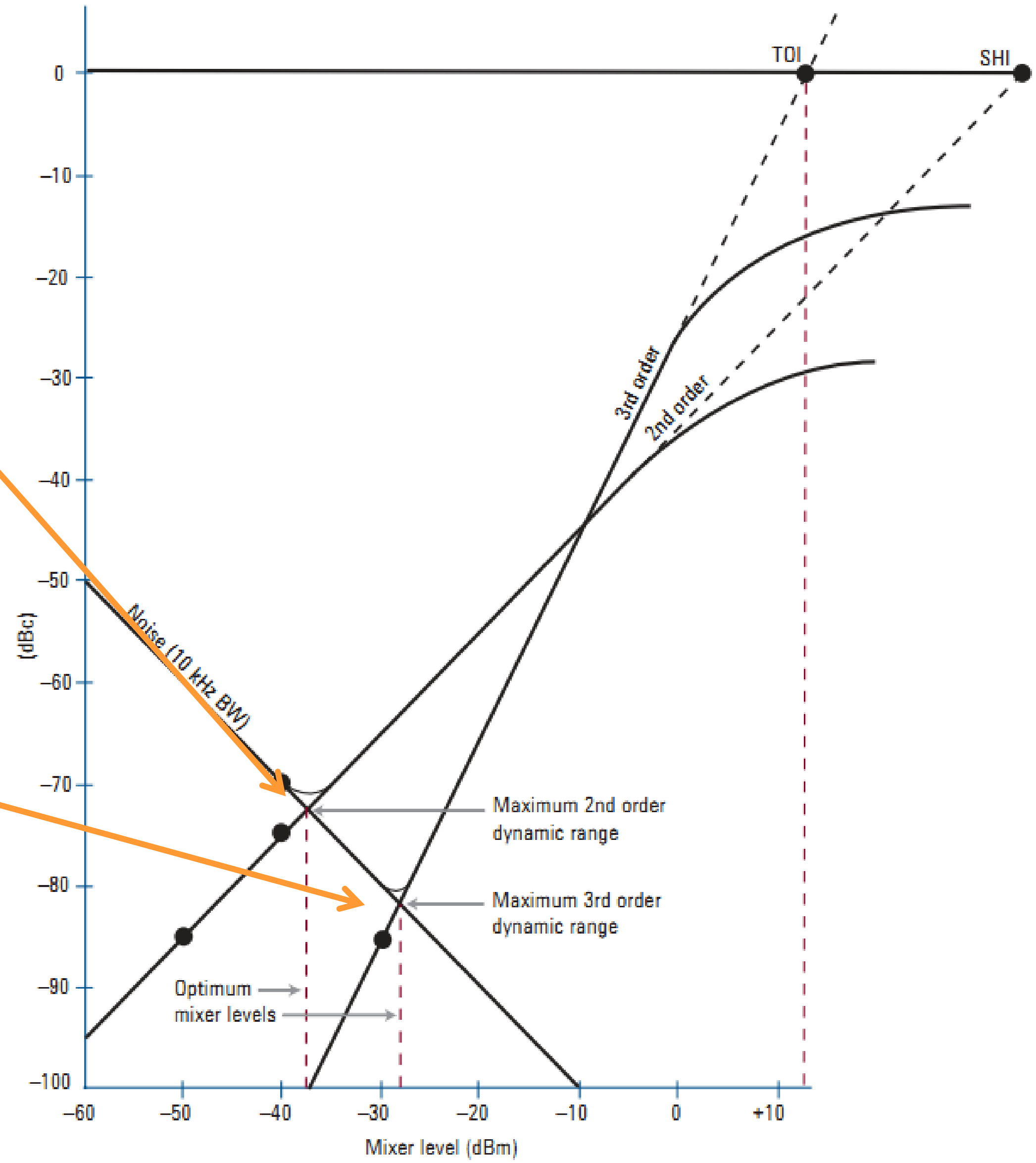


Figure 12. Dynamic range versus distortion and noise

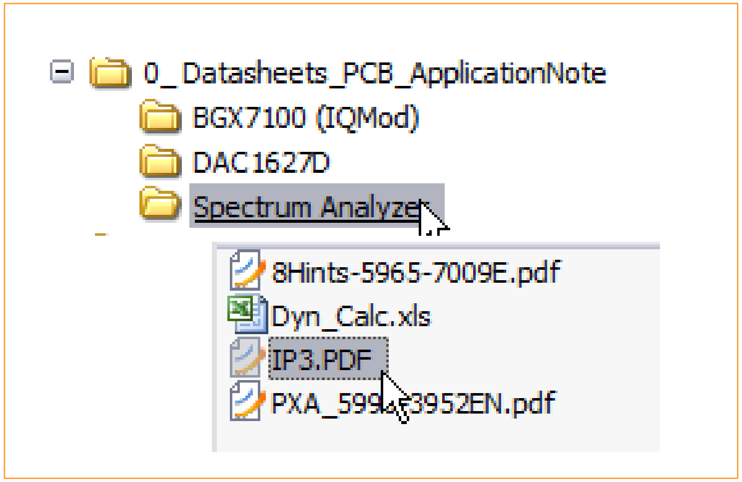
| Line-related spurious responses | | | –73 dBc** + 20log(N*) (nominal) |
|---|---|---|---|
| **Second harmonic distortion (SHI)** | | | |
| | Source frequency | Mixer level | Distortion*** |
| | 10 to 100 MHz | –15 dBm | –57 dBc/NA |
| | 0.1 to 1.8 GHz | –15 dBm | –60 dBc/NA |
| | 1.75 to 2.5 GHz | –15 dBm | –77 dBc/–95 dBc |
| | 2.5 to 4 GHz | –15 dBm | –77 dBc/–101 dBc |

# Spectral measurements

## Understand OIP3 / IMD3 after IQModulator

# Third Order Intercept measurements

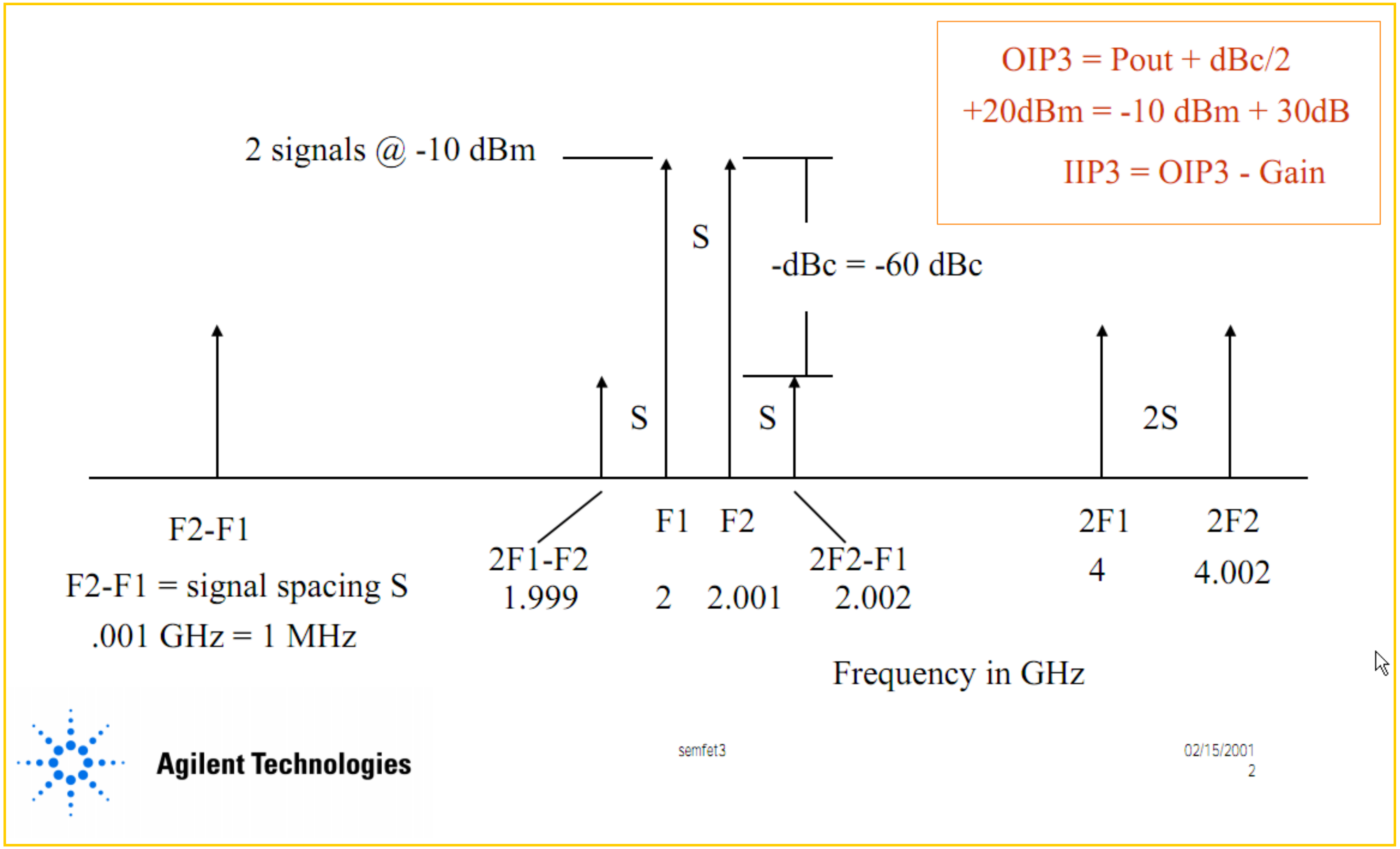
Please refers to the Application Note from **Agilent** for more details.



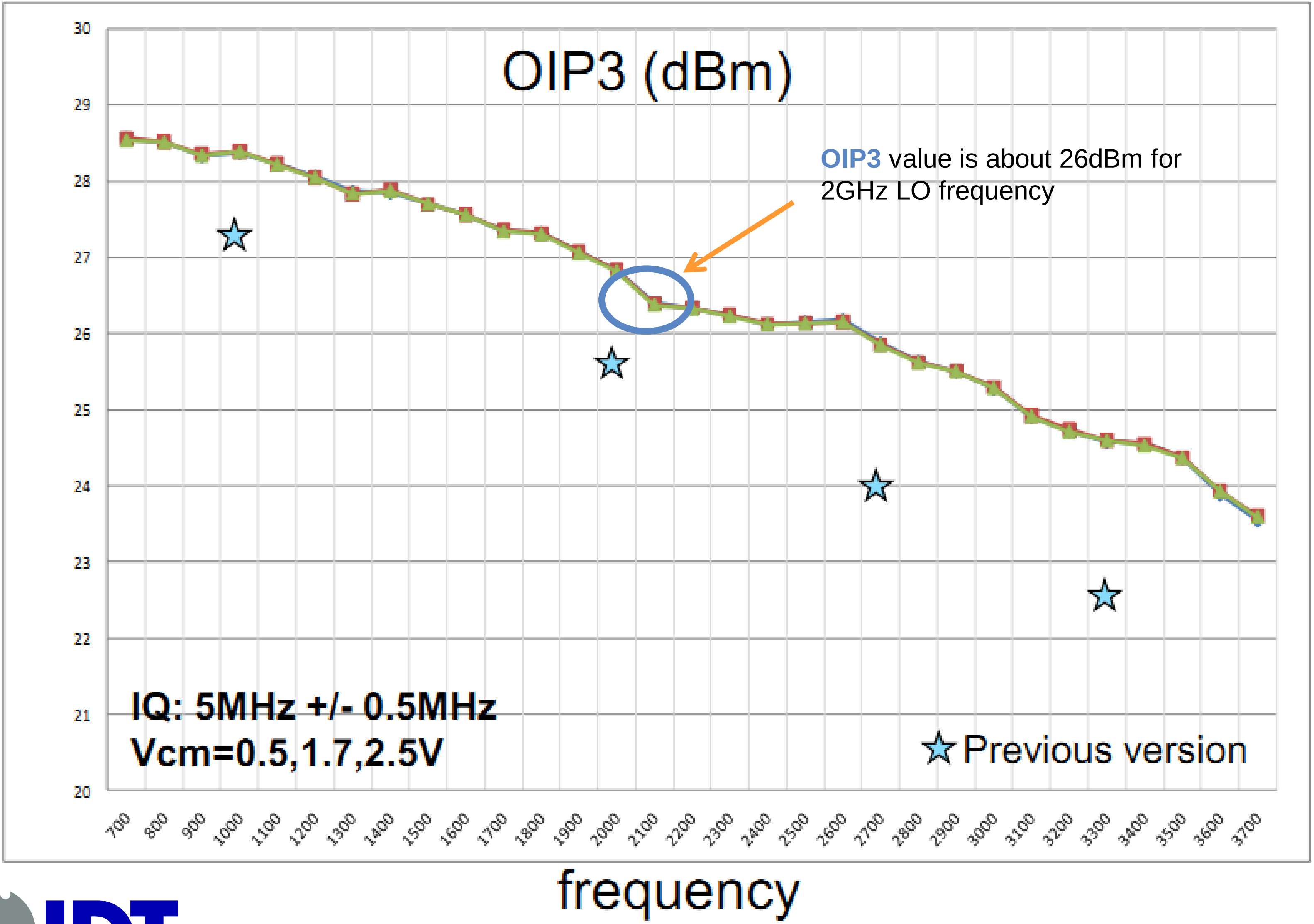

IDT

# Definition of OIP3

In telecommunications, a **third-order intercept point** (IP3 or TOI) is a measure for **nonlinear systems** and devices.The third-order intercept point relates nonlinear products caused by the **third-order nonlinear term** to the linearly amplified signal, in contrast to the second-order intercept point that uses second order terms.

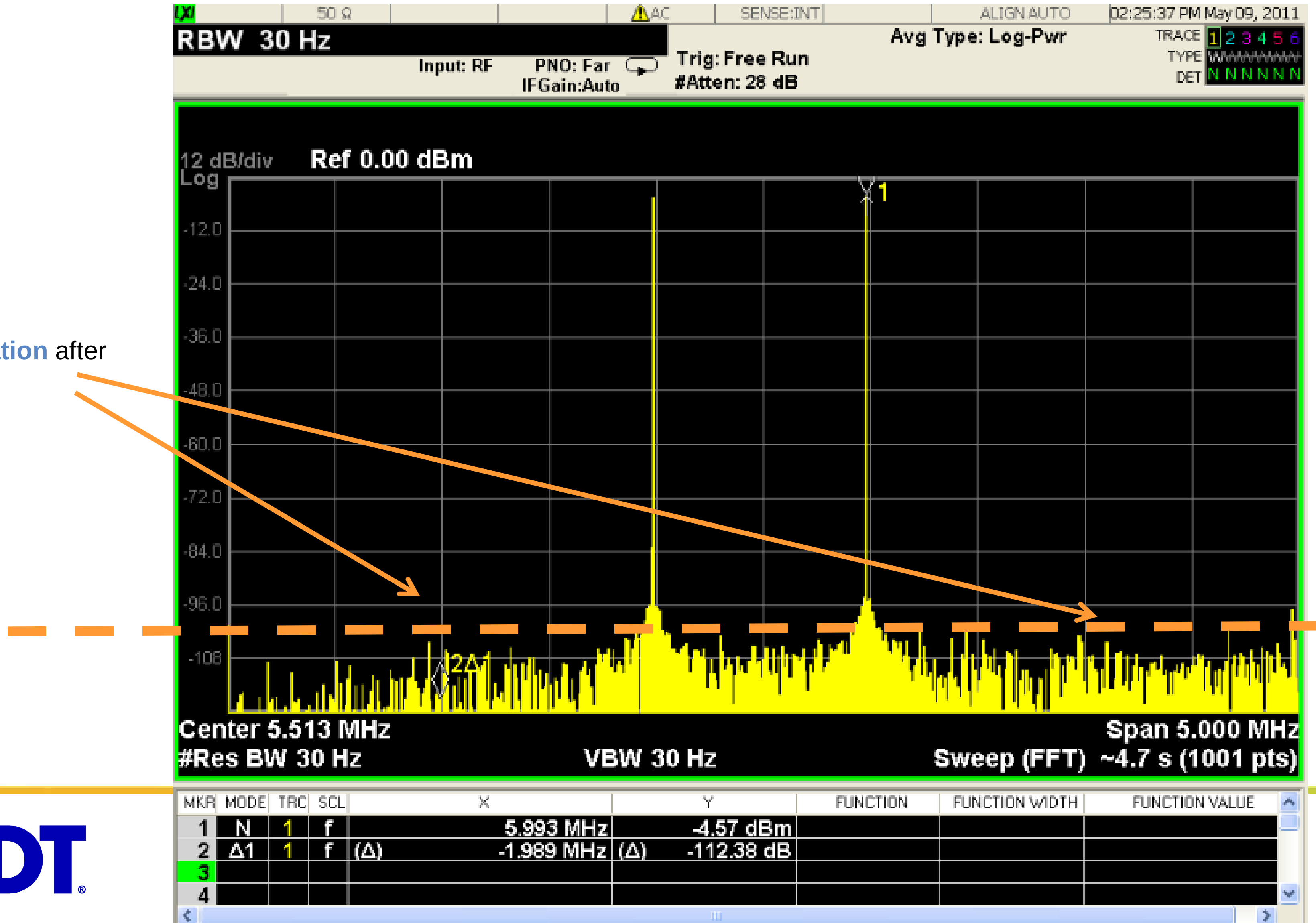


# BGX7100 OIP3



# Intermodulation see at DAC outputs

**No intermodulation** after DAC.

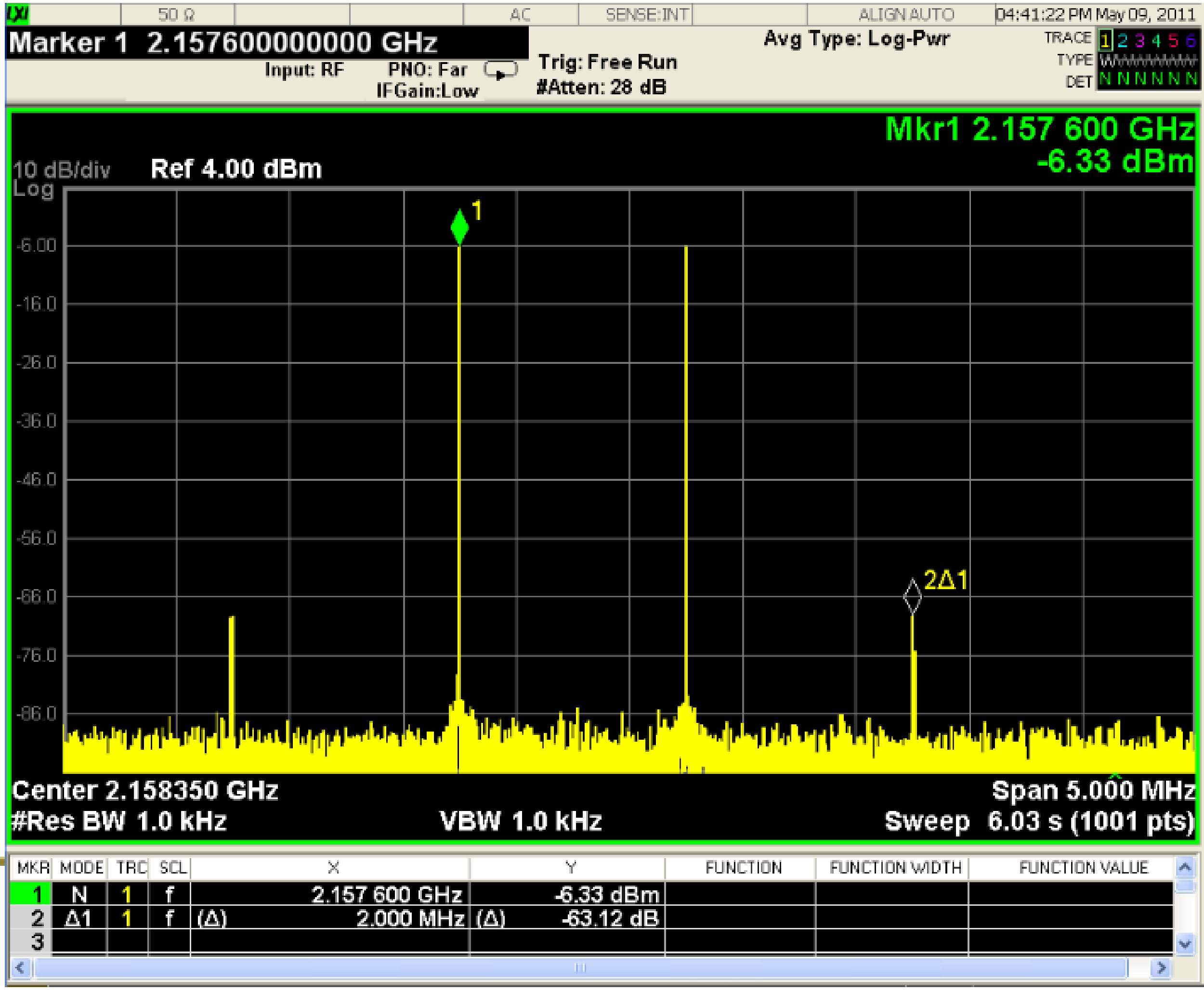


# Intermodulation after IQMod (2Ghz)

Output Power= -6.33dBm
dBc= -63.12

**OIP3**=-6.33+63.12/2**=25.23dBm**

➔ The main contribution for the intremodulation is coming from the IQmod.



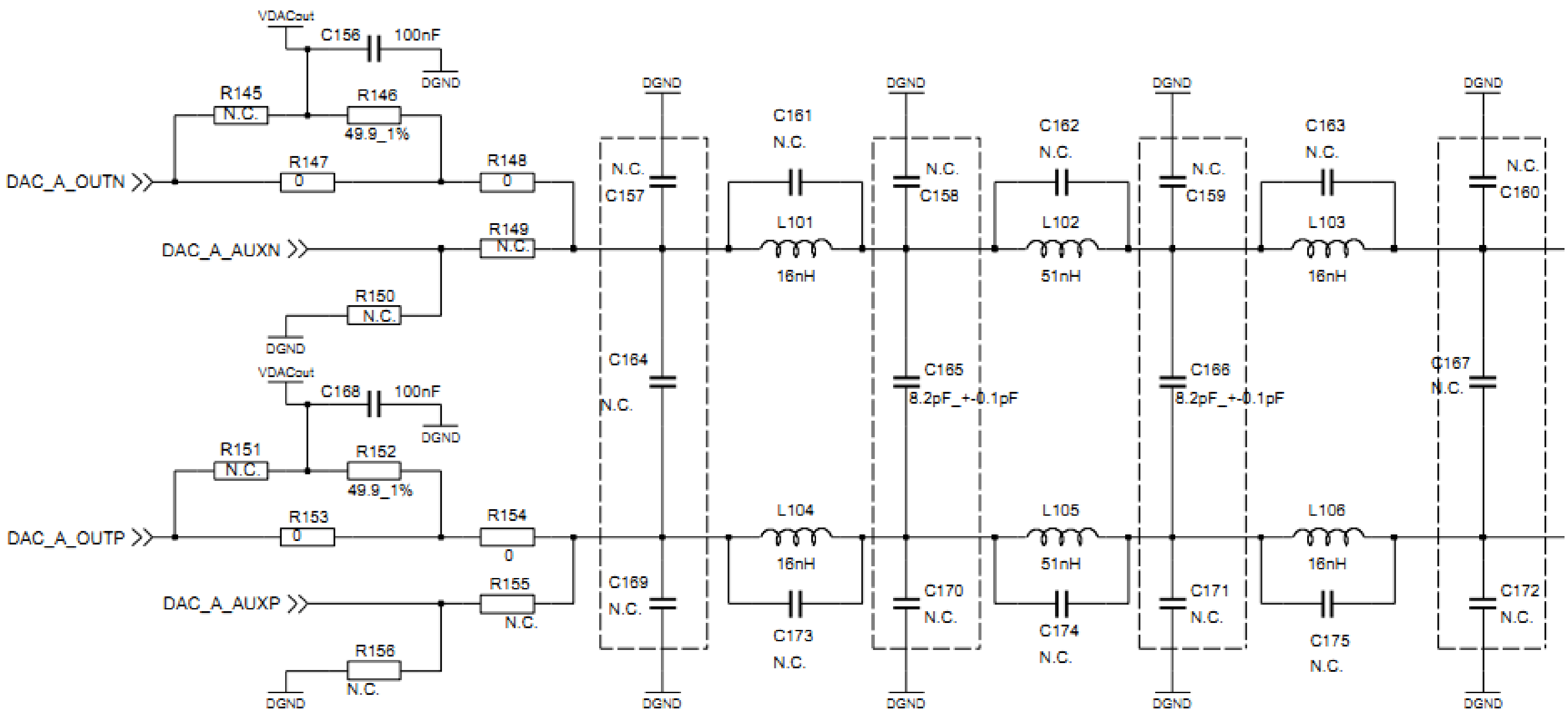
## Standard Filter between DAC1627D and BGX7100

# 300Mhz Chebychev Filter between DAC1627D and BGX7100

Refers to schematics PCB2227-1.0_17243\DOS_PCB2227-1.0_17243\ PCB2227-1-200-00_1_2.pdf

L101=L104= 39nH , L102=L105: 47nH, L103=L106 = 18nH C165= 10pf C166= 6.8pf

L107=L110= 39nH , L108=L111: 47nH, L109=L112 = 18nH C185= 10pF C186= 6.8pf



# Filter response