DA16200 DA16600 Hardware Design Guide

This user manual provides hardware design considerations for the DA16200 and DA16600.

Contents

Figures

Tables

1. Terms and Definitions

AMBA	Advanced Microcontroller Bus Architecture
DC-DC	Direct Current Direct Current
DPM	Dynamic Power Management
DTM	Direct Test Mode
EVM	Error Vector Magnitude
GPIO	General Purpose In/Out
LDO	Low Dropout
QSPI	Quad Serial Peripheral Interface
QFN	Quad Flat No-Leads
PCB	Printed Circuit Board
RF	Radio Frequency
RTC	Real-Time Clock
SFDP	Serial Flash Discoverable Parameters
SPI	Serial Peripheral Interface

2. References

[1] DA16200, Datasheet, Renesas Electronics.

[2] DA16200MOD, Datasheet, Renesas Electronics.

[3] DA16600, Datasheet, Renesas Electronics.

[4] DA14531, Datasheet, Renesas Electronics.

[5] UM-WI-011, DA16200 DA16600 Mass Production, User Manual, Renesas Electronics.

[6] UM-WI-004, DA16200 AT GUI Tool User Manual, User Manual, Renesas Electronics.

[7] UM-WI-046, DA16200 DA16600, FreeRTOS SDK Programmer Guide, User Manual, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Introduction

This document provides a set of guidelines that help developers to prepare schematics and PCB layouts for products with the DA16200, DA16200MOD, and DA16600. Recommended schematic, chip interfaces, and surrounding components as well as PCB layout guidelines of both devices are provided.

4. Guidelines of Schematic Design

The DA16200 and DA16600 application schematics include the following five parts:

- **Power supply**: Digital Power Supply, Analog Power Supply
- **RF**: Antenna components
- **Clock**: Main Clock and RTC Clock
- **Flash interface**
- **Digital I/O**: GPIO pin assignment which can be changed based on the applications requirements.

To select the proper schematic, check the items below:

- **Package type**: The DA16200 provides QFN and fcCSP packages
- **VDD of flash memory**: 1.8 V and 3.3 V flash memory can be supported with the DA16200. When a 1.8 V flash memory is applied, the DA16200 can control the flash memory directly through VDD_FDIO/FDIO_LDO_OUT (QFN pin 20 and 21, fcCSP pin M4). When a 3.3 V flash memory is applied, an additional switch is required to control the flash memory to achieve low power
  - The DA16200MOD contains a Winbond W25Q32JW flash device by default
  - The DA16600MOD contains an Adesto AT25SL321 flash device by default.
- **TX power modes**: The fcCSP package type can support normal or low power TX modes.

For further information, see the Section "Current Consumption" of Ref. [1]. Applications which do not require high power TX operation can use the low power TX mode to reduce power consumption. The QFN package type only supports the normal TX power mode. See Ref. [1] for details on how to configure the low power TX mode, Make RTOS Image for fcCSP of Ref. [7] for creating RTOS image on fcCSP Low power mode, and Appendix B for information on each application.

5. DA16200 and DA16200MOD

The DA16200 is available in two package types:

- 6x6 48-pin QFN
- 3.8x3.8 72-pin fcCSP.

The DA16200MOD is available in two formats:

- The DA16200MOD-AAC4WA32 contains an internal chip antenna
- The DA16200MOD-AAE4WA32 contains a u.FL connector for an external antenna.

Because the DA16200MOD is a module containing the DA16200 chipset, only the DA16200 contents are described below. For more information on the DA16200MOD, see Ref. [2].

5.1 48-Pin QFN

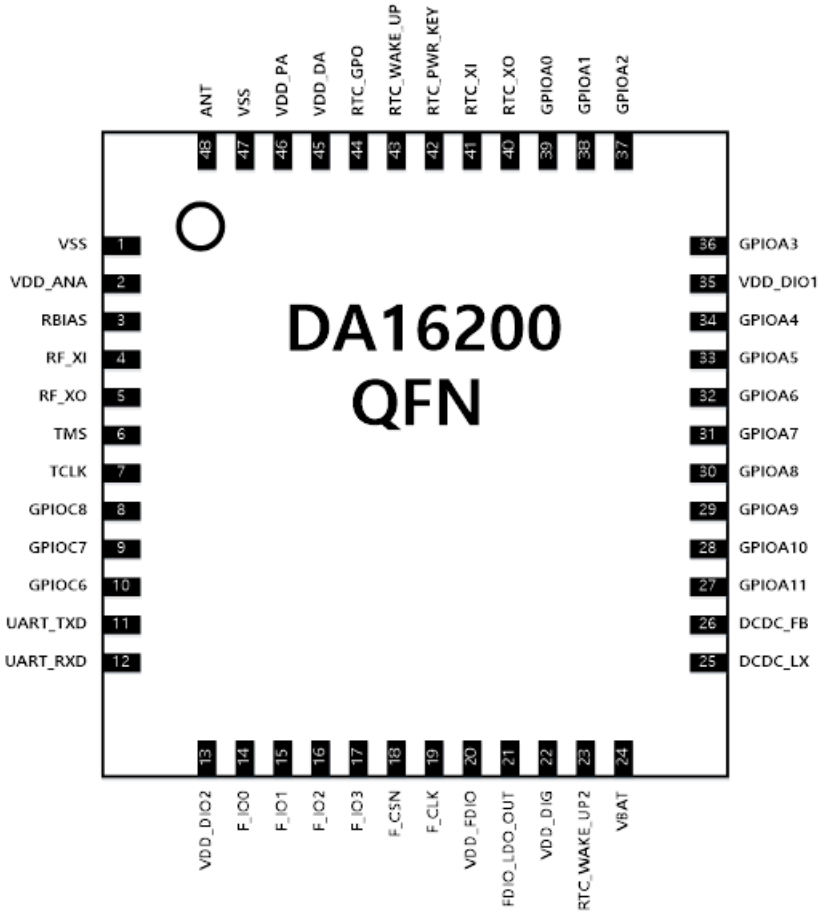


Figure 1. DA16200 QFN48 pinout diagram (Top view)

5.2 72-Pin fcCSP

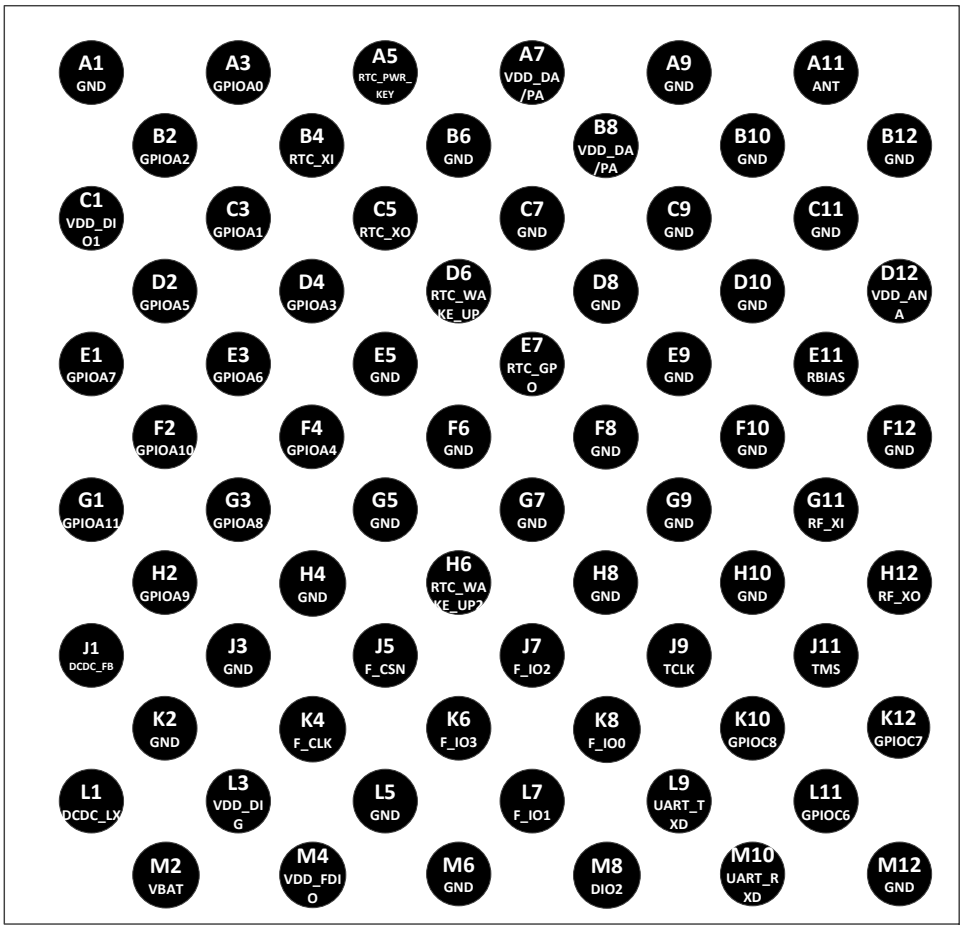


Figure 2. DA16200 fcCSP72 pinout diagram (Top view)

5.3 Pin Description

Table 1. Pin description

QFN #pin	fcCSP #pin	Pin name	Type	Drive (mA)	Initial state (Note 1)	Description
1		GND	GND			Ground
2	D12	VDD_ANA	VDD			RF VDD
3	E11	RBIAS	AIO			External reference resistor pin
4	G11	RF_XI	AI			40 MHz crystal clock input
5	H12	RF_XO	AO			40 MHz crystal clock output
6	J11	TMS	DIO	2/4/8/12	I-PU	JTAG I/F, SWDIO
7	J9	TCLK	DIO	2/4/8/12	I-PD	JTAG I/F, SWCLK, General Purpose I/O
8	K10	GPIOC8	DIO	2/4/8/12	I-PD	General Purpose I/O
9	K12	GPIOC7	DIO	2/4/8/12	I-PD	General Purpose I/O
10	L11	GPIOC6	DIO	2/4/8/12	I-PD	General Purpose I/O
11	L9	UART_TXD	DO	2/4/8/12	O	UART transmit data
12	M10	UART_RXD	DI	2/4/8/12	I	UART receive data
13	M8	VDD_DIO2	VDD			Supply power for digital I/O GPIOC6~GPIOC8, TMS/TCLK, TXD/RXD
14	K8	F_IO0	DIO			External Flash Memory I/F
15	L7	F_IO1	DIO			External Flash Memory I/F

QFN #pin	fcCSP #pin	Pin name	Type	Drive (mA)	Initial state (Note 1)	Description
16	J7	F_IO2	DIO			External Flash Memory I/F
17	K6	F_IO3	DIO			External Flash Memory I/F
18	J5	F_CSN	DIO			External Flash Memory I/F
19	K4	F_CLK	DIO			External Flash Memory I/F
20	M4	VDD_FDIO	VDD			Flash I/O Power
21		FDIO_LDO_OUT	AIO			Flash and I/O LDO output and connect to external cap. For flash LDO
22	L3	VDD_DIG	VDD			Digital power and connect to external cap. For DIG LDO
23	H6	RTC_WAKE_UP2	DI			RTC block wake-up signal
24	M2	VBAT	VDD			Supply power for internal DC-DC, DIO_LDO, and analog IP
25	L1	DCDC_LX	AIO			Connection from power MOSFETs to the Inductor in internal DC-DC
26	J1	DCDC_FB	AIO			Feedback voltage from the output of the power supply in internal DC-DC
27	G1	GPIOA11	DIO	2/4/8/12	I-PD	General Purpose I/O
28	F2	GPIOA10	DIO	2/4/8/12	I-PD	General Purpose I/O
29	H2	GPIOA9	DIO	2/4/8/12	I-PD	General Purpose I/O
30	G3	GPIOA8	DIO	2/4/8/12	I-PD	General Purpose I/O
31	E1	GPIOA7	DIO	2/4/8/12	I-PD	General Purpose I/O
32	E3	GPIOA6	DIO	2/4/8/12	I-PD	General Purpose I/O
33	D2	GPIOA5	DIO	2/4/8/12	I-PD	General Purpose I/O
34	F4	GPIOA4	DIO	2/4/8/12	I-PD	General Purpose I/O
35	C1	VDD_DIO1	VDD			Supply power for digital I/O GPIOA0~GPIOA11
36	D4	GPIOA3	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
37	B2	GPIOA2	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
38	C3	GPIOA1	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
39	A3	GPIOA0	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
40	C5	RTC_XO	AO			32.768 kHz crystal clock output
41	B4	RTC_XI	AI			32.768 kHz crystal clock input
42	A5	RTC_PWR_KEY	DI			RTC block enable signal
43	D6	RTC_WAKE_UP	DI			RTC block wake-up signal
44	E7	RTC_GPO	DO			General Purpose Output
45	A7	VDD_DA	VDD			TX DA power and RTC block power
46	B8	VDD_PA	VDD			Supply power for integrated power amplifier
47	-	GND	GND			Ground
48	A11	ANT	AI			ANT
fcCSP GND Pin A1, A9, B6, B10, B12, C7, C9, C11, D8, D10, E5, E9, F6, F8, F10, F12, G5, G7, G9, H4, H8, H10, J3, K2, L5, M6, M12						

Note 1 Status of RTC_PWR_KEY is asserted, and digital power (VDD_DIG) is stable.

Table 2. Pin type definition

Pin type	Description	Pin type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
DIOD	Digital input/output open drain	BP	Back drive protection
PU	Pull-up resistor (fixed)	SPU	Switchable pull-up resistor

Pin type	Description	Pin type	Description
PD	Pull-down resistor (fixed)	SPD	Switchable pull-down resistor
PWR	Power	GND	Ground

5.4 Power Supply

5.4.1 Power Management

The DA16200 has one internal DC-DC converter and multiple LDOs to supply power to all internal sub-blocks. Power management performs the on-off control of these regulators and is implemented through the register setting inside the RTC block.

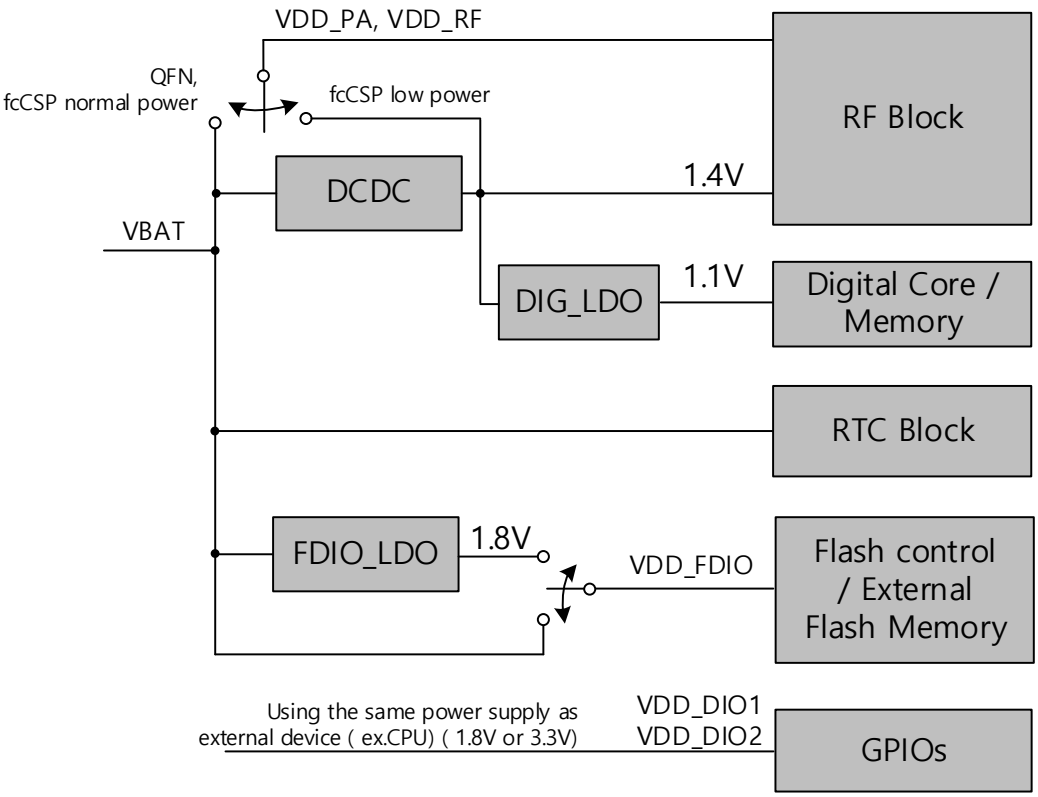


Figure 3. Power management block diagram

Details of the internal DC-DC converters and LDOs are explained below:

- DC-DC converter: from the power supply of external VBAT input, it generates 1.4 V power for the digital LDO and RF block
- LDO for digital Blocks: from the DC-DC output, it generates 1.1 V power which is used for digital blocks
- LDO for I/O and external flash memory:
  - This LDO output is used only for 1.8 V digital I/O applications
  - From external VBAT power input, it generates 1.8 V output voltage which is used for digital I/O power domain in 1.8 V digital I/O applications
  - It is also used for external flash memory
  - For 3.3 V digital I/O applications, external power (3.3 V) is directly supplied for digital I/O power
- FDIO_LDO_OUT supports only 1.8 V.

Internal DC-DC converters and LDOs generate enough power for all the DA16200's internal sub-blocks. The sequence after the initial switching from power-off to power-on of DA16200 is shown in Figure 4. The RTC_PWR_KEY is a pin that enables the RTC block of DA16200. When RTC_PWR_KEY is enabled after VBAT power is supplied, all the internal regulators are switched on automatically in the sequence pre-defined by the RTC block. When RTC_PWR_KEY is switched on, LDOs for both XTAL and digital I/O are switched on shortly

and then the DC-DC regulator is switched on according to the pre-defined interval. The enabling intervals can also be modified in the register settings after initial power-up.

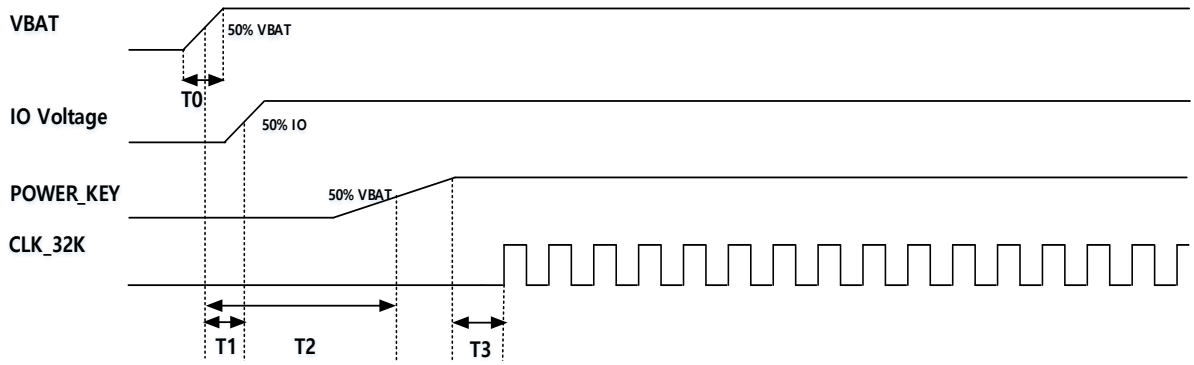


Figure 4. Power on sequence

Table 3. Power on sequence timing requirements

Name	Description	Min	Typ	Max	Unit
T0	VBAT power-on time from 10% to 90% of VBAT				ms
T1	I/O voltage and VCC supply		0		ms
T2	RTC_PWR_KEY turn-on time from 50% VBAT to 50 % POWER_KEY * (Note 1)		5*T0		ms
T3	Internal RC oscillator wake-up time		217		µs

Note 1 If the T0 = 10 ms to switch on VBAT, the recommended T2 is 50 ms for the safe booting operation. It can be externally controlled by MCU, or it can be implemented using RC filter at the input of RTC_PWR_KEY. The recommended C is 470 µF or 1 µF (not to exceed 1 µF) and R value is chosen to have T2 delay. For example, R and C values are 82 kΩ and 1 µF when T0 = 10 ms.

Table 4. Power pin descriptions

QFN #pin	fcCSP #pin	Pin name	Type	Description
1	-	GND	GND	Ground
2	D12	VDD_ANA	VDD	RF VDD
13	M8	VDD_DIO2	VDD	Supply power for digital I/O GPIOC6~GPIOC8, TMS/TCLK, TXD/RXD
20	M4	VDD_FDIO	VDD	Flash I/O Power
21		FDIO_LDO_OUT	AIO	Flash and I/O LDO output and connect to external capacitor for flash LDO
22	L3	VDD_DIG	VDD	Digital power and connect to external cap for DIG LDO
24	M2	VBAT	VDD	Supply power for internal DC-DC, DIO_LDO, and analog IP
25	L1	DCDC_LX	AIO	Internal DC-DC feedback input for digital block supply
26	J1	DCDC_FB	AIO	Internal DC-DC feedback output for digital block supply
35	C1	VDD_DIO1	VDD	Supply power for digital I/O GPIOA0~GPIOA11
45	A7	VDD_DA	VDD	TX DA power and RTC block power
46	B8	VDD_PA	VDD	Supply power for integrated power amplifier
47	-	GND	GND	Ground
fcCSP GND Pin: A1, A9, B6, B10, B12, C7, C9, C11, D8, D10, F6, F8, F10, F12, G5, G7, G9, H4, H8, H10, J3, K2, L5, M6, M12, E5				

5.4.2 VBAT

The DA16200 can operate one source for an I/O interface and internal power source (LDO and DC-DC converter), so it is important to reduce the noise component on this power line. All the input de-coupling capacitors should be located near the DA16200 IC, and the thickness of power traces should be higher than 0.3 mm. The operating voltage level of VDD is from 2.1 V to 3.6 V. This allows the use of two alkaline batteries.

5.4.3 Internal DC-DC (DCDC_LX and DCDC_FB)

The DA16200 contains one DC-DC converter for the analog and digital parts. This DC-DC converter needs to connect a series 4.7 µH power inductor for high-power efficiency and a shunt 10 µF capacitor to reduce switching noise. Therefore, the inductor and capacitor should be located as close as possible for stable power supply. And 1 µF bypass capacitors are required for the power supply.

5.4.4 VDD_DA and VDD_PA

The DA16200 supports a low power TX mode for special applications which do not require high power output for TX. The fcCSP package type can support both low and normal TX power modes whereas the QFN package type only supports the normal TX power mode.

The difference between the low and normal power TX modes is with the connection of VDD_PA and VDD_DA. Those VDDs are connected to VBAT in normal power TX mode and connected to the DC-DC output in low power TX mode. See Figure 5 for the VDD connection and the application examples of both normal and low power TX modes in the **Applications Schematic** section of Ref. [1].

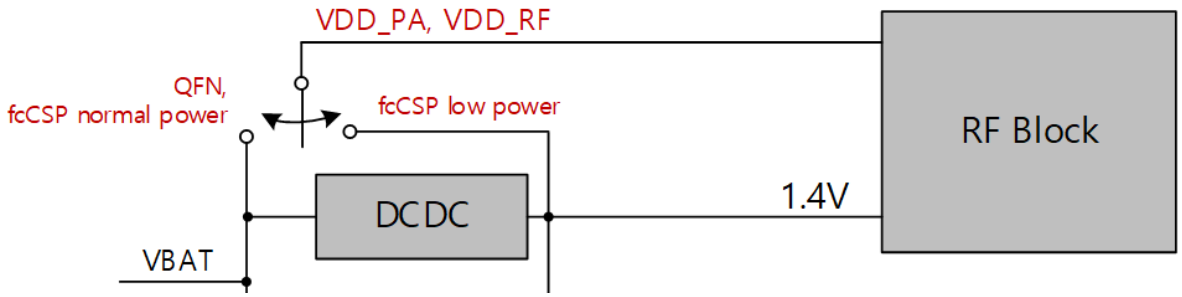


Figure 5. High/Low TX power mode connection

The typical TX output power at 1 Mbps DSSS is 18.5 dBm in normal power TX mode and 9.5 dBm in low power TX mode. See Ref. [1] for detailed performance in the Radio Characteristics section.

5.4.5 VDD_ANA

VDD_ANA is connected to DC-DC output.

5.4.6 VDD_DIG

VDD_DIG is not connected to the power supply but requires 470 nF bypass capacitor.

5.4.7 VDD_FDIO and FDIO_LDO_OUT

VDD_FDIO is connected to VDD of flash memory. This pin can be connected to FDIO_LDO_OUT when 1.8 V VDD of flash memory is used. FDIO_LDO_OUT is the internal LDO output of the DA16200 for flash memory. The voltage level of FDIO_LDO_OUT is 1.8 V, so this pin can be used when 1.8 V VDD of flash memory is used. FDIO_LDO_OUT is turned off in Sleep mode to reduce the power consumption. When 3.3 V VDD of flash memory is used, an additional load switch to control the flash VDD is needed to reduce the power consumption in Sleep mode.

5.4.8 VDD_DIO1 and VDD_DIO2

These are the I/O voltage pins of the DA16200 chip that should be set to the same voltage level as the I/O pins of a connected external device such as an MCU. The DA16200 can support both 1.8 V and 3.3 V for I/O voltage.

5.5 RBIAS

RBIAS (#3 of QFN and #E11 of fcCSP) determine the bias current of DA16200. 1% tolerance of 30 kΩ of resistor should be adopted to this pin to minimize the variation of current consumption.

5.6 RF

The RF application circuit is important to achieve optimum performance from the device. Improper circuits and layout can cause performance degradation for sensitivity, output power, error vector magnitude (EVM) and spectral mask.

5.6.1 Antenna

The antenna is the element used to convert the guided waves on the PCB traces to free-space electromagnetic radiation. The position and layout of the antenna are very important to increase coverage and data rates.

5.6.2 Antenna Information of DA16200MOD

The DA16200 chip antenna type module (DA16200MOD-AAC4WA32) includes a 2.4 GHz chip type antenna. The details of antenna are:

- **Part number:** WALSIN RFECA32160AM1T62
  - Datasheet: http://www.passivecomponent.com/wp-content/uploads/2018/10/ASC_RFECA3216060A1T_V09.pdf
  - Walsin homepage: http://www.passivecomponent.com
  - Antenna product page: http://www.passivecomponent.com/product-search/Antenna/?c2VsZWN0%5Bseries%5D%5Bvalue%5D=Chip+Antenna+%28BT%2C+Wifi+BAND%29
- **Dimension**

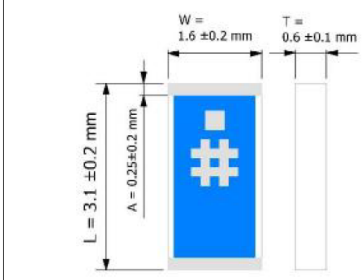
Figure	Symbol	Dimension (mm)
	L	3.10 ± 0.20
	W	1.60 ± 0.20
	T	0.60 ± 0.10
	A	0.25 ± 0.20

Figure 6. Tested antenna dimension

- **Tested Antenna Usage Example**

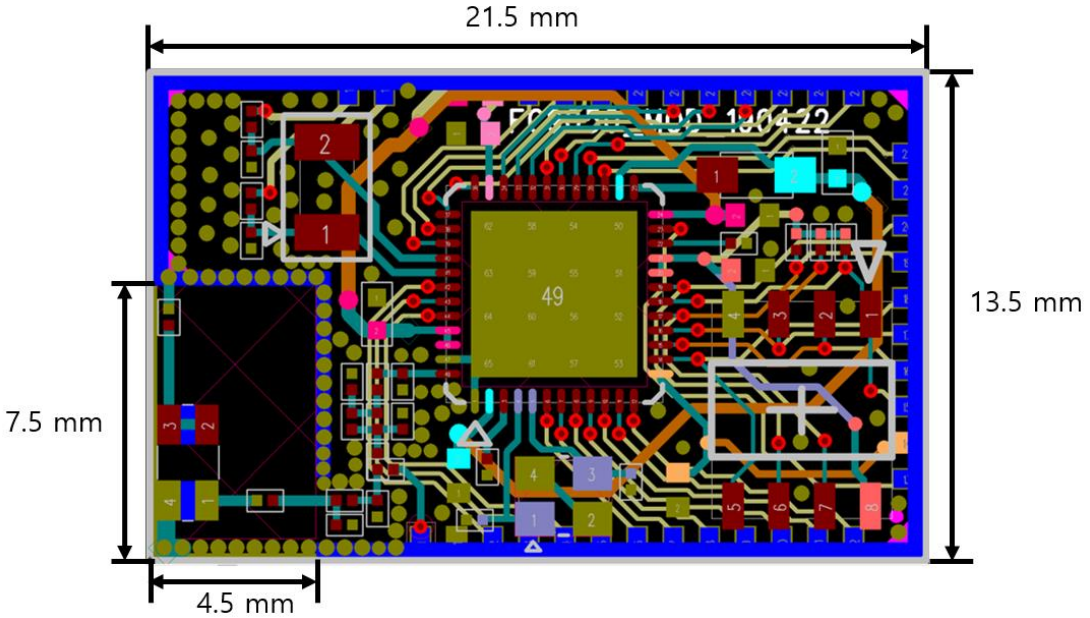


Figure 7. Tested antenna usage

- **Radiation Pattern**

Unit : dBm

Test Channel	2412 CH	2442 CH	2462 CH
T I S	72.28	72.49	72.46
Max.	75.51	76.02	76.52
Min.	67.29	67.38	64.82
NHPIS 30	70.98	71.12	71.02
UHIS	70.70	70.97	70.99
UHIS Ratio	55.27	56.61	57.46
Conduction	108.00	108.00	108.00

Unit : dBm

Test Channel	2412 CH	2442 CH	2462 CH
T R P (@30˚)	12.14	11.31	10.75
Max.	15.92	15.24	15.69
Min.	7.11	6.17	5.42
NHPRP 30˚	10.89	9.98	9.38
UHRP	10.51	9.84	9.29
UHRP Ratio	54.70%	56.48%	57.63%
Conduction	24.00	24.00	24.00

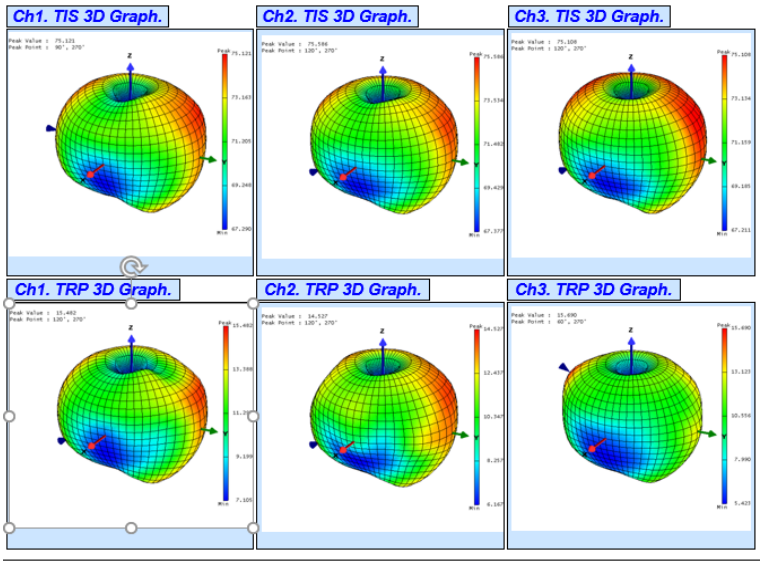


Figure 8. Tested antenna radiation pattern

Consider the following actions for the antenna performance:

- Put the antenna on the edge or corner of the PCB
- Signal lines should not be routed across the antenna elements on any layer of the PCB
- The ground is needed for copper keep-out on all layers, including inner layers
- Matching components for the antenna are needed to optimize each board
- The return loss measured at the matching components of the antenna needs to be better than 10 dB to get the optimum system performance.

5.6.3 RF Input Requirements

The RF part should have matching components and an RF filter to suppress any harmonic element. A passive filter which is made by lumped components can meet the system requirements because the DA16200 has good harmonic suppression performance.

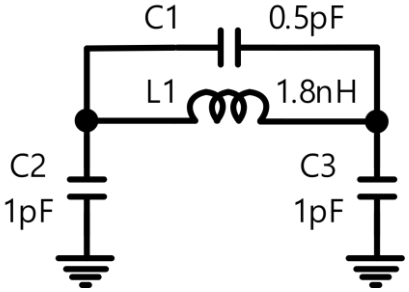


Figure 9. LC filter circuit

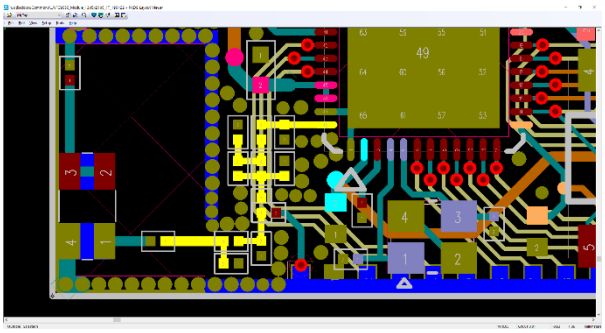


Figure 10. LC filter layout

The RF line needs to be isolated by using a ground plane with proper clearance to ensure good performance (output power, EVM, SEM, and sensitivity).

5.7 Clock

5.7.1 RF Main Clock (40 MHz)

The DA16200 has a crystal oscillator for the main clock source, which supports the external crystal clock. Basically, the external clock is 40 MHz. Make sure that the load capacitance is tuned based on the board parasitic so that the frequency tolerance is within ±20 ppm. And the clock line needs to route closer to the XTAL routing to avoid any phase noise degradation. The recommended operating conditions are described in Table 5.

Table 5. WLAN crystal clock requirements

Parameter	Conditions	Min	Typ	Max	Unit
Frequency			40		MHz
Frequency accuracy	Initial + temp + aging	-20		+20	ppm
Crystal ESR				50	Ω
Load Capacitance (Note 1)		6	8	10	pF

Note 1 Not exceeding ±20 ppm, there is an internal adjustable shunt capacitor inside the chipset, which must be written to the OTP block after crystal correction. There is a 0~12.7 pF tunable capacitor inside the DA16200, to use without shunt capacitors outside, it must be selected a crystal with a load capacitance of 6~10 pF.

The selected crystal for the DA16200MOD is the 8Z40000047 of TXC. The crystal specification is described in Table 6.

Table 6. Selected main RF XTAL specification

Parameter	Symbol	Min	Typ	Max	Unit	Note
Nominal Frequency	FL		40.00000		MHz	
Oscillator Mode			Fundamental			
Load Capacitance	CL		10		pF	
Frequency Tolerance			±7		ppm	at 25 °C ± 3 °C
Frequency Stability			±13		ppm	Over operating temp. range (Reference 25 ℃)
Operating Temperature		-40	~	-85	℃	
Aging			±1		ppm	5 years
Drive Level	DL		100		uW	
Equivalent Series Resistance	Rr			30	Ω	
Shunt Capacitance C0	C0			2	pF	
Insulation Resistance		500			MΩ	at DC 100 V
Storage Temperature Range		-40		85	℃	

5.7.1.1 40 MHz RF XTAL Trimming

The 40 MHz crystal oscillator has trimming capability. The frequency is trimmed by two on-chip variable capacitor banks. Renesas provides AT GUI tool and the frequency can be tuned easily by the tool. The tool is available on the Renesas website (https://www.renesas.com/us/en/products/wireless-connectivity/wi-fi/low-power-wi-fi).

To tune the frequency on DA16200 EVK:

1. Connect DA16200 EVK to a personal computer and run AT GUI Tool with DA16200 EVK.
   a. See Ref. [6] for details.
2. On **Certification** tab, transmit CW TX power.
   a. Click **Test Mode**.
   b. Click the **Select** button.
   c. Click **CW**.
   d. Select desired channel (frequency).
   e. Select power level (0 is maximum power).
   f. Click the **Start TX** button.

g. Check the exact TX frequency using spectrum analyzer.

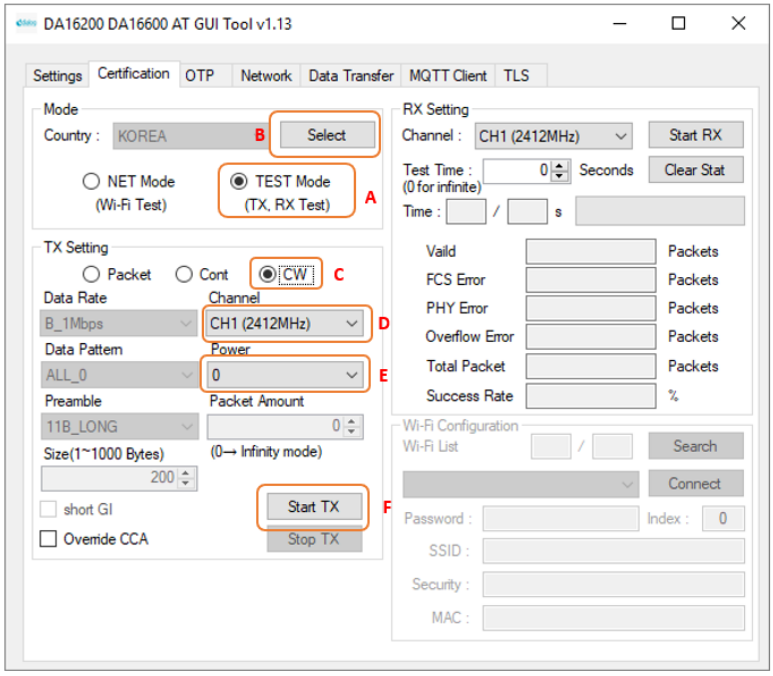


Figure 11. Transmitting CW TX power setup

3. On the OTP tab, check the current internal load capacitor value of the DA16200.
   a. Select the OTP Enable checkbox.
   b. Click the Read XTAL button to check the current internal capacitor value of the DA16200. "0x41" is the value in this example.

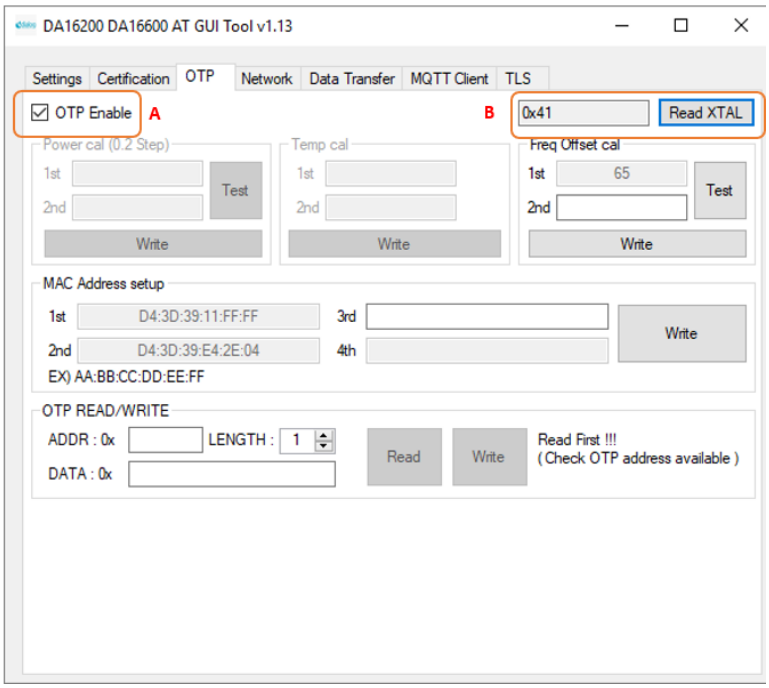


Figure 12. Read XTAL value

4. On the console window, write the desired value.
   a. Enter "AT+XTALWR=<value>" command. <value> is desired value and seven-bits to write [h'1 ~ h'7f].
   b. Click the Send button.

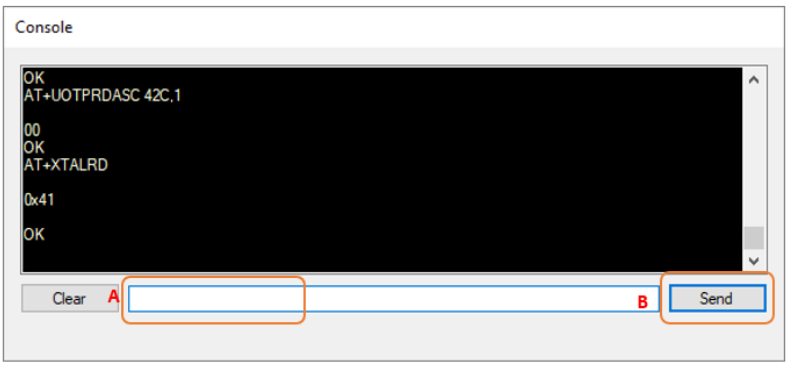


Figure 13. Write new XTAL value

NOTE
If the register value is changed significantly, it may not be possible to write the value. Changes should be less than 10.

5. Check TX frequency change on spectrum analyzer.
6. Repeat steps 4 and 5 to find the correct value.

Renesas highly recommends calibrating the RF XTAL on the production line as the frequency tolerance of Wi-Fi specification is within ±20 ppm. See Ref. [5] describes how to adopt the calibration on mass production. In the DA16200 module, RF XTAL is calibrated, and therefore, additional action is not required about the calibration.

5.7.2 RTC Clock (32.768 kHz)

The 32.768 kHz RTC clock source is necessary for the free-running counter in the RTC block.

5.7.2.1 RTC Clock Using Crystal

Table 7 shows the suitable loading capacitor value and required tolerance. Figure 14 shows connections for the RTC crystal clock.

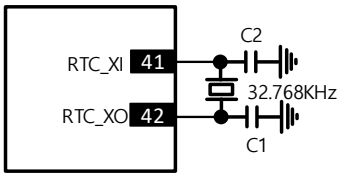


Figure 14. RTC clock

Table 7. 32 kHz XTAL oscillator - Required operating conditions

Parameter	Conditions	Min	Typ	Max	Unit
Frequency			32.768		kHz
Frequency accuracy	Initial + temp + aging	-250		+250	ppm
Crystal ESR				100k	Ω
Load Capacitance			10		pF
Shunt Capacitance (Note 1)			15		pF

Note 1 External Shunt capacitors C1 and C2 are required for tuning the RTC. On the DA16200MOD, C1 and C2 are installed with the value of 15 pF.

5.7.2.2 RTC Clock Using External Clock

When an RTC oscillator is present in the system, the DA16200 can accept this clock directly as an input. The clock is fed on the RTC_XO line through series capacitor. Figure 15 shows the external RTC input connection. Table 8 lists the external RTC digital clock requirements.

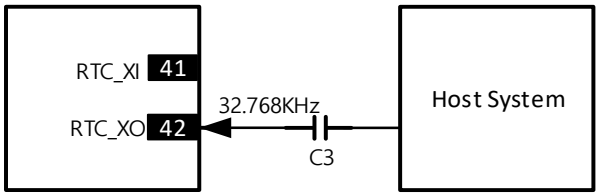


Figure 15. RTC for external connection

Table 8. 32 kHz external clock - Required operating conditions

Parameter	Conditions	Min	Typ	Max	Unit
Frequency			32.768		kHz
Frequency accuracy	Initial + temp + aging	-250		+250	ppm
Vp-p		0.5*VBAT		VBAT	V
C3 value			1	-	µF

5.8 Serial Flash

5.8.1 Serial Flash Interface

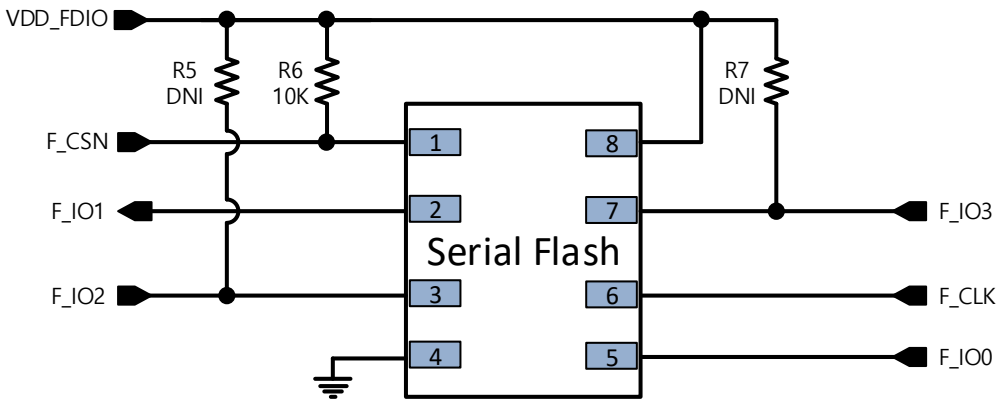


Figure 16. Serial flash application schematic

The QSPI master supports 4-line SPI communication with commercial flash memory devices and uses a Motorola SPI-compatible interface among SPI communication modes. The highest communication speed is the same as the AMBA bus clock, and the speed is adjustable in integer multiples. The designed QSPI supports 4-/2-/1-line types depending on the purpose. These types should be combined. Especially when 1-line communication mode is used, it can be used as the SPI master. Table 9 shows the connections between DA16200 and serial flash.

Table 9. Connections between DA16200 and Serial flash

DA16200			Serial flash		Note
Pin name	QFN	fcCSP	Pin name	Pin #	
F_IO0	14	K8	DI/SI/IO0	5	
F_IO1	15	L7	DO/SO/IO1	2	
F_IO2	16	J7	WP/IO3	3	
F_IO3	17	K6	HOLD/RESET	7	
F_CSN	18	J5	CSN/CSB	1	10 kΩ pull-up resistor
F_CLK	19	K4	CLK/SCK	6	

5.8.2 Serial Flash Selection Guide

SFDP (Serial Flash Discoverable Parameters) is a standard table for the main parameters of serial flash defined by JEDEC. This is information about the characteristics (access timing, supported commands, and delay parameter) of each serial flash manufactured by various vendors, which should be optimized for each serial flash. Currently the DA16200 SDK supports SFDP tables for serial flashes listed in Table 10.

Table 10. Recommended serial flash list

Vendor	Part #	Operation VDD (Typ)	Memory size
Adesto (Renesas)	AT25SL321	1.8 V	4 MB
Adesto (Renesas)	AT25SL128	1.8 V	16 MB
Giga Device	GD25LE32E	1.8 V	4 MB
ISSI	IS25LQ032B	3.3 V	4 MB
MXIC	MX25L3233F	3.3 V	4 MB
MXIC	MX25L25635F	3.3 V	32 MB
MXIC	MX25R3235F (Note 1)	1.8~3.3 V	4 MB
MXIC	MX25U3232F	1.8 V	4 MB
MXIC	MX25U3235F	1.8 V	4 MB
Winbond	W25Q32JV	3.3 V	4 MB
Winbond	W25Q32JW	1.8 V	4 MB
Winbond	W25Q128JW	1.8 V	16 MB
FM (Fudan Micro)	FM25W32	1.8~3.3V	4 MB

Note 1 This part supports both low power and high-performance modes. The DA16200 supports only the part with high performance mode as default. See descriptions of the part name and the datasheet for details.

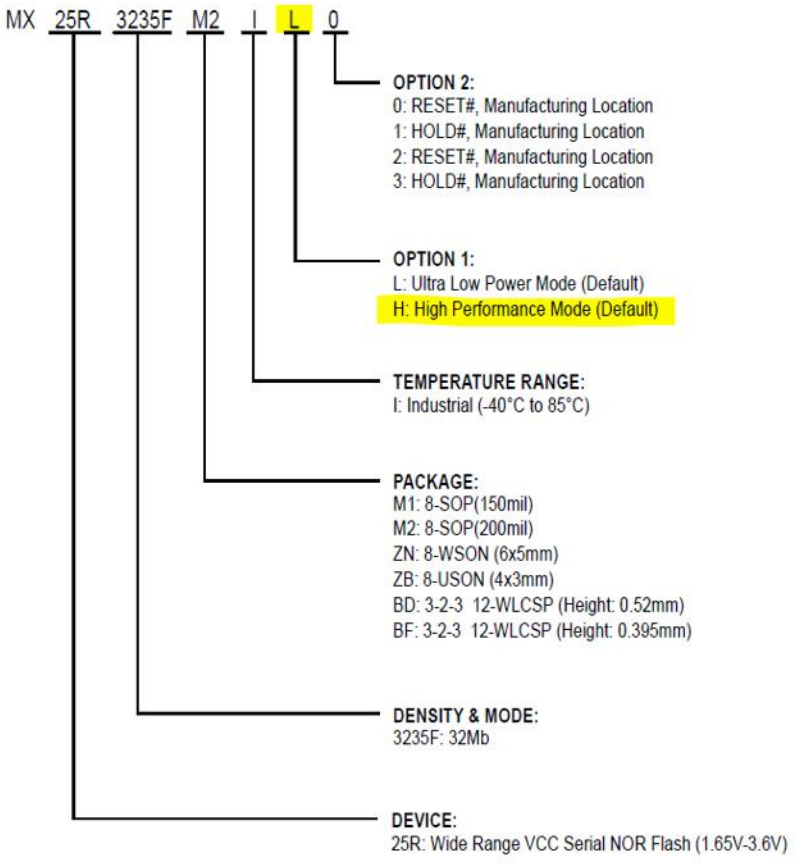


Figure 17. Part name description

If customers want to use other types of serial flash, then the extraction (from serial flash specification) and optimization of the SFDP parameters is needed. And a new serial flash should be used, the schedule shown in Table 11 is required, which the customer should take into consideration in their project planning.

Table 11. New flash verification process

Verification process
'D': date of receiving the board-adopted new serial flash. 1. Extract SFDP parameter. a. D + 10 2. Apply SFDP table to image and proceed functional test. a. D + 15 b. Functional test in normal condition 3. Reliability test a. Functional test in severe condition b. D + 21 4. Make the SFDP release with J-Link flash loader. a. D + 30

5.9 External Control Pins

5.9.1 RTC Power Key (RTC_PWR_KEY)

The RTC_PWR_KEY represents a power key for the RTC block. When this pin is enabled, the RTC starts to work by following a predefined power-up sequence and eventually all the necessary power is supplied to all the sub-blocks including the main digital block in the DA16200. When disabled, all blocks are powered off and this mode is defined as Sleep mode 1. The DA16200 consumes minimum leakage current in Sleep mode 1.

5.9.1.1 Input High/Low Voltage of RTC Block

The VDD of RTC blocks is VBAT, so DC parameters for RTC block are varied by VBAT. See Table 12 and Table 13 for references. RTC block consists of RTC_PWR_KEY, RTC_WAKE_UP, and RTC_WAKE_UP2.

Table 12. DC parameters for RTC block, 3.3 V VBAT

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.6	V
Input High Voltage	V_{IH}	Guaranteed logic High level	2.2		VBAT	V

Table 13. DC parameters for RTC block, 2.1 V VBAT

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.3	V
Input High Voltage	V_{IH}	Guaranteed logic High level	1.6		VBAT	V

When the MCU controls this pin, the voltage level of control pin from MCU should be checked.

For example, when the VBAT of the DA16200 is 3.3 V and the voltage level of control signal from MCU is 1.8 V, the RTC_PWR_KEY cannot be operated normally. In this case, the RTC_PWR_KEY can be controlled by VBAT with RC delay circuit (See Figure 18).

5.9.1.2 Power On Sequence

The RTC_PWR_KEY should be enabled after VBAT power is supplied. When an external MCU controls this pin, some delay time is needed between VBAT power-on time and RTC_PWR_KEY turn-on time. When an external MCU cannot control this pin or MCU is not used, RC delay circuit on RTC_PWR_KEY should be applied (See Figure 18)

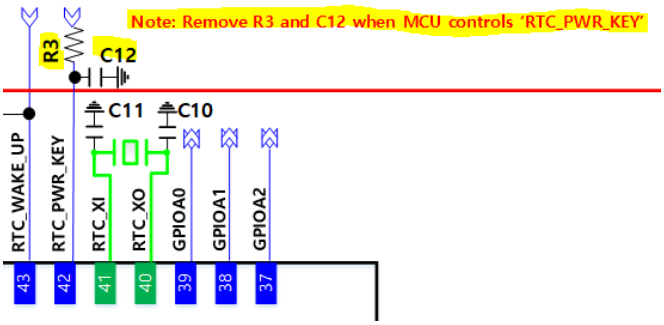


Figure 18. RTC_PWR_KEY circuit

The recommended C value is 470 nF or 1 µF (not to exceed 1 µF) and R value should have enough delay between VBAT power-on time and RTC_PWR_KEY turn-on time. For example, R and C values are 82 kΩ and 1 µF when the VBAT power-on time is 10 ms. See Section "Power Management" of Ref. [1] for more details.

5.9.2 RTC Wake-up Key (RTC_WAKE_UP and RTC_WAKE_UP2)

This is an input pin for receiving an external event signal from an external device like a sensor. The RTC block detects an external event signal through this pin and wakes up the DA16200 from Sleep mode 2 or Sleep mode 3.

5.9.2.1 Input High/Low Voltage of RTC Block

RTC_WAKE_UP1 and RTC_WAKE_UP2 are also RTC blocks, so the input high/low voltage of RTC_WAKE_UP1 and RTC_WAKE_UP2 is varied by VBAT same as RTC_PWR_KEY. See Table 12 and Table 13 for checking the voltage level of external device.

5.9.2.2 Pull-Down Resistor

4.7 kΩ pull-down resistor on RTC_WAKE_UP and RTC_WAKE_UP2 pins to avoid the leakage current. In fact, both pull-up and pull-down are available, but pull-down is better for layout. When this pin is not used, it can be connected to GND directly without a pull-down resistor.

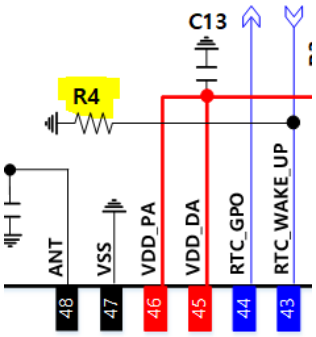


Figure 19. RTC_WAKE_UP circuit

5.9.2.3 GPIO Wake-up Pin

The normal GPIO of the DA16200 can support wake-up function when RTC_WAKE_UP1/2 cannot be used as the voltage level are different. See Section "Wake-up Controller" of Ref. [1] for details.

5.10 RTC_GPO

RTC_GPO is an output and high voltage level is "VBAT". This pin has three different functions:

- GPO: This output value can be set as '1' or '0' through register setting. It can keep the value even in Sleep mode.
  - External MCU can use this pin for monitoring whether the DA16200 enters Sleep mode 1 or Sleep mode 2.
  - The driving current is around 200 µA.
- Flash control: when in Sleep mode, it becomes '0'; when in active mode, it is 1.

- Sensor wake-up: when the sensor wake-up function is used (see Section Sensor Wake-up of Ref. [1]), a programmable periodic signal is provided for an external device. Inside the RTC, there are registers to set count values.

5.11 GPIO Pin Multiplexing

The DA16200 provides various interfaces to support many kinds of applications. By referring to the pin multiplexing in Table 14, each pin can be controlled according to the required application. Pin control can be realized through register setting. This device can use a maximum of 16 GPIO pins, and each of the GPIO pin multiplexed signals of various functions. Four pins from GPIOA0 to GPIOA3 multiplex analog signals, which also can be realized through register setting.

Table 14. DA16200 pin multiplexing

Pin	JTAG	Analog	SPI master	SPI slave	I2C master	I2C slave	SDIO slave	SDeMMC	Bluetooth coex
GPIOA0		CH0		SPI_MISO	I2C_SDA	I2C_SDA			
GPIOA1		CH1		SPI_MOSI	I2C_CLK	I2C_CLK		WRP	
GPIOA2		CH2		SPI_CSB		I2C_SDA			
GPIOA3		CH3		SPI_CLK		I2C_CLK			
GPIOA4					I2C_SDA	I2C_SDA	CMD	CMD	
GPIOA5					I2C_CLK	I2C_CLK	CLK	CLK	
GPIOA6			SPI_CSB	SPI_CSB		I2C_SDA	D3	D3	
GPIOA7			SPI_CLK	SPI_CLK		I2C_CLK	D2	D2	
GPIOA8			SPI_DIO0/ SPI_MOSI	SPI_MISO	I2C_SDA		D1	D1	BT_SIG0
GPIOA9			SPI_DIO1/ SPI_MISO	SPI_MOSI	I2C_CLK		D0	D0	BT_SIG1
GPIOA10			SPI_DIO2	SPI_MISO				WRP	BT_SIG2
GPIOA11			SPI_DIO3	SPI_MOSI					
TCLK/ GPIOA15	TCLK								
TMS	TMS								
UART_TXD									
UART_RXD									
GPIOC8	TDI								
GPIOC7	TDO								
GPIOC6	NTRST								

Table 15. DA16200 pin multiplexing (Continued)

Pin	I2S	I2S_Clock	UART1	UART2	Muxed w/Analog	Pin state (nREST=0)	Driving strength (Default: 8 mA)
GPIOA0	BCLK		TXD		Yes	I-PD	2/4/8/12 mA
GPIOA1	MCLK		RXD		Yes	I-PD	2/4/8/12 mA
GPIOA2	SDO		TXD		Yes	I-PD	2/4/8/12 mA
GPIOA3	LRCK	CLK_IN	RXD		Yes	I-PD	2/4/8/12 mA
GPIOA4	BCLK		TXD/RTS		No	I-PD	2/4/8/12 mA
GPIOA5	MCLK		RXD/CTS		No	I-PD	2/4/8/12 mA
GPIOA6	SDO		TXD		No	I-PD	2/4/8/12 mA
GPIOA7	LRCK		RXD		No	I-PD	2/4/8/12 mA
GPIOA8	BCLK				No	I-PD	2/4/8/12 mA
GPIOA9	MCLK				No	I-PD	2/4/8/12 mA
GPIOA10		CLK_IN		TXD	No	I-PD	2/4/8/12 mA
GPIOA11				RXD	No	I-PD	2/4/8/12 mA
TCLK/ GPIOA15					No	I-PD	2/4/8/12 mA

Pin	I2S	I2S_Clock	UART1	UART2	Muxed w/Analog	Pin state (nREST=0)	Driving strength (Default: 8 mA)
TMS					No	I-PD	2/4/8/12 mA
UART_TXD					No	O	2/4/8/12 mA
UART_RXD					No	I	2/4/8/12 mA
GPIOC8					No	I-PD	2/4/8/12 mA
GPIOC7				RXD	No	I-PD	2/4/8/12 mA
GPIOC6				TXD	No	I-PD	2/4/8/12 mA

5.12 Interface Pull-Up

It is an open-drain/open-collector communication standard which implies integrated circuits (IC) with different voltage supply rails can be connected for communication. Pull-up resistors need to be connected from the signal lines to the supply to enable communication.

5.12.1 I2C

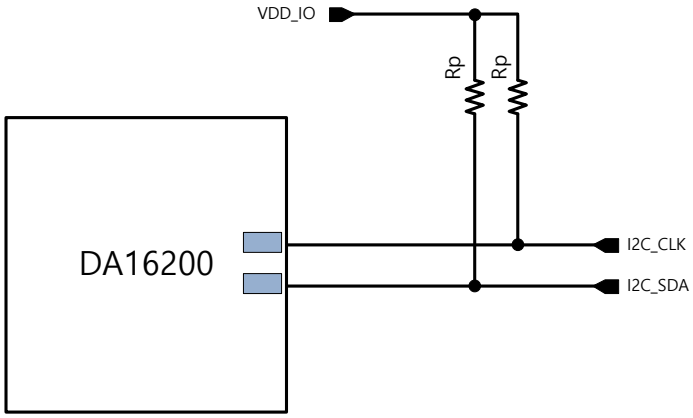


Figure 20. I2C pull-up resistors

The pull-up resistance value is a function of rise time.

$R_p = T_r / (0.8473 \times C_b)$

※ T_r: rise time, C_b: capacitive load for each bus line

Table 16. Characteristics

Parameter	Symbol	Fast mode		High speed mode		Unit
		Min	Max	Min	Max	
Rise time of both SDA and SCXL	T_R	0.02	0.3	-	0.05	µs

C_b can be different in each board layout. Therefore, it is preferred to calculate the pull-up resistor value according to layout condition.

5.12.2 SDIO

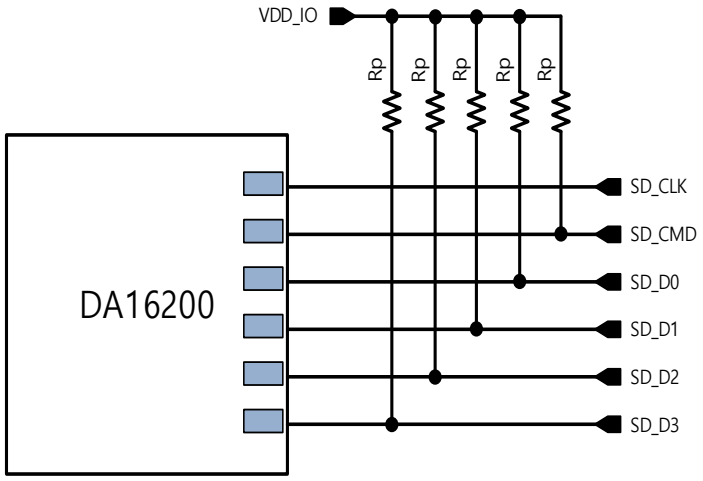


Figure 21. SDIO pull-up resistors

The recommended pull-up resistor value range is between 10k and 100k. In addition, this value affects signal rise time and leakage current.

5.13 PCB Layout

5.13.1 Grounding

- Make the internal ground area as solid as possible. Do not break the ground into pieces.
- Provide good solid ground by using multiple vias.
- Fill as much ground as possible in the area between the walls of shield cavities and the outline of the RF section.
- Connect each ground pin or via to the ground plane individually.
- Put the Ground via on the PAD of the QFN package.

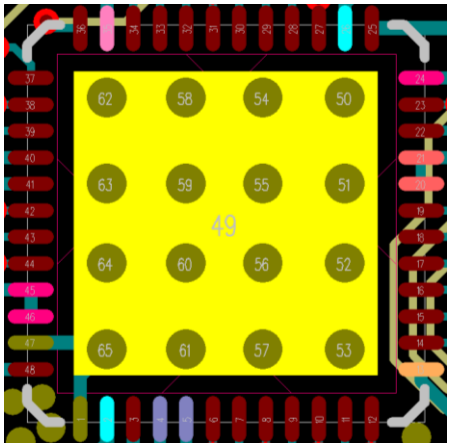


Figure 22. Ground vias on pad

5.13.2 Layout Example: DA16200MOD

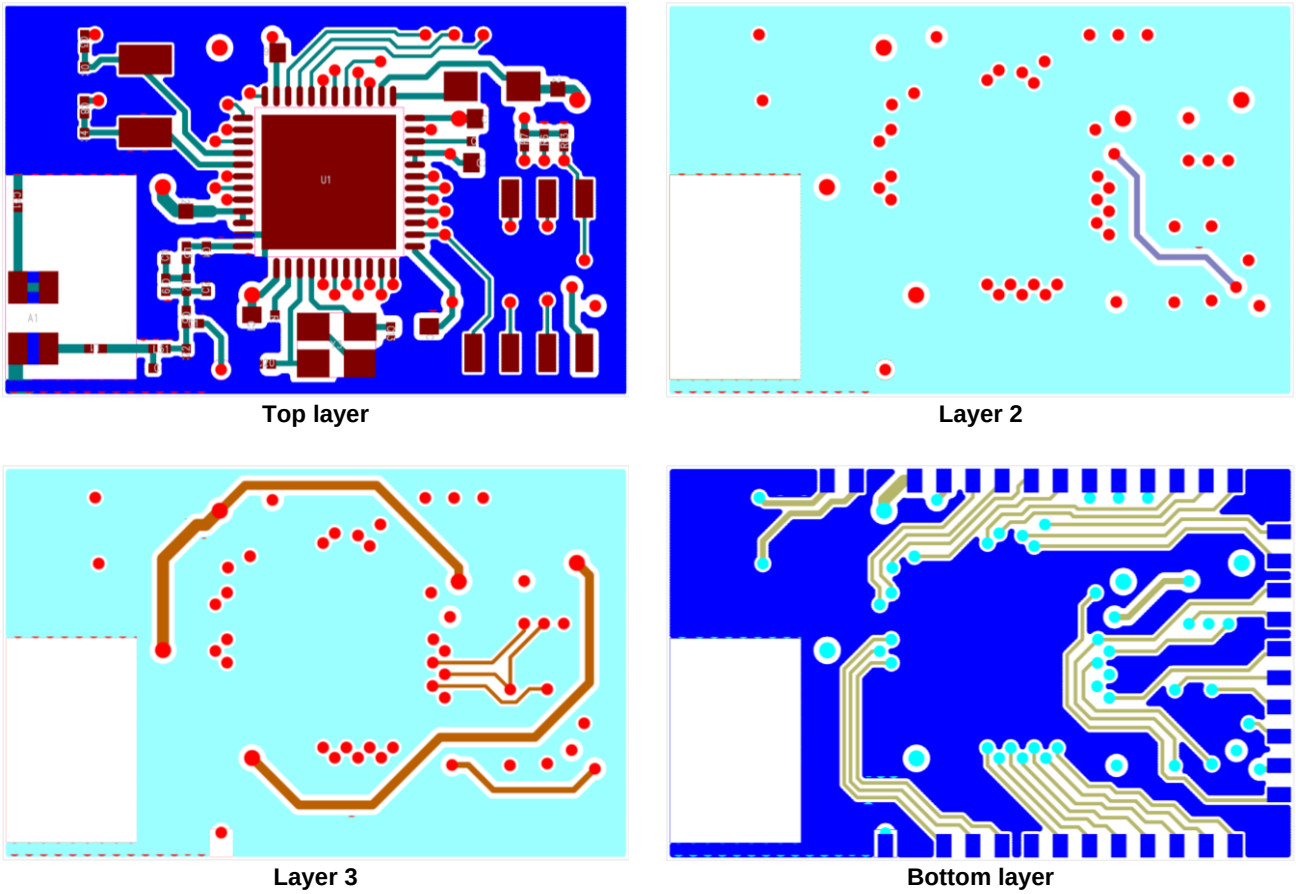


Figure 23. DA16200MOD 4-layer PCB example

5.13.3 Recommended Footprint

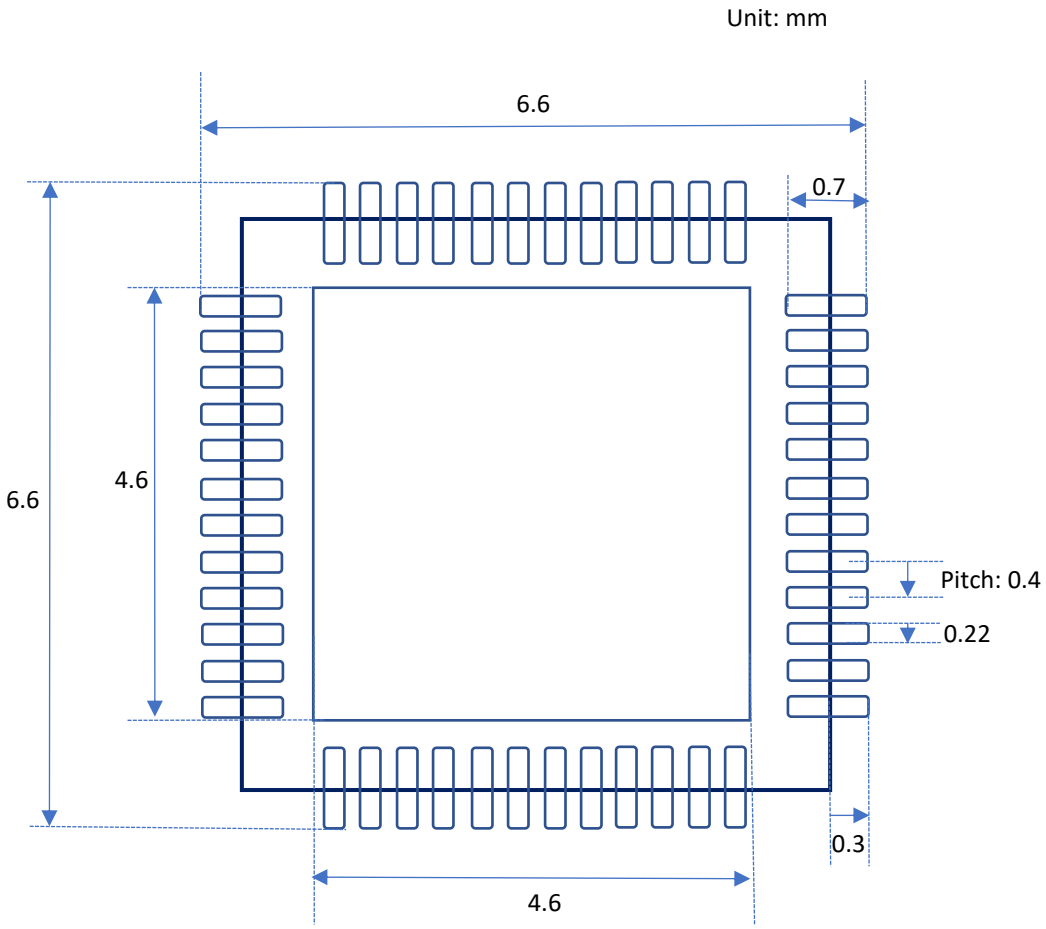


Figure 24. DA16200 ground footprint

6. DA16600

The DA16600 provides a high level of integration for a battery based wireless system supporting integrated IEEE 802.11 b/g/n and Bluetooth V5.1. The DA16600 is designed to address the needs of battery-based devices that require minimal power consumption and reliable operation.

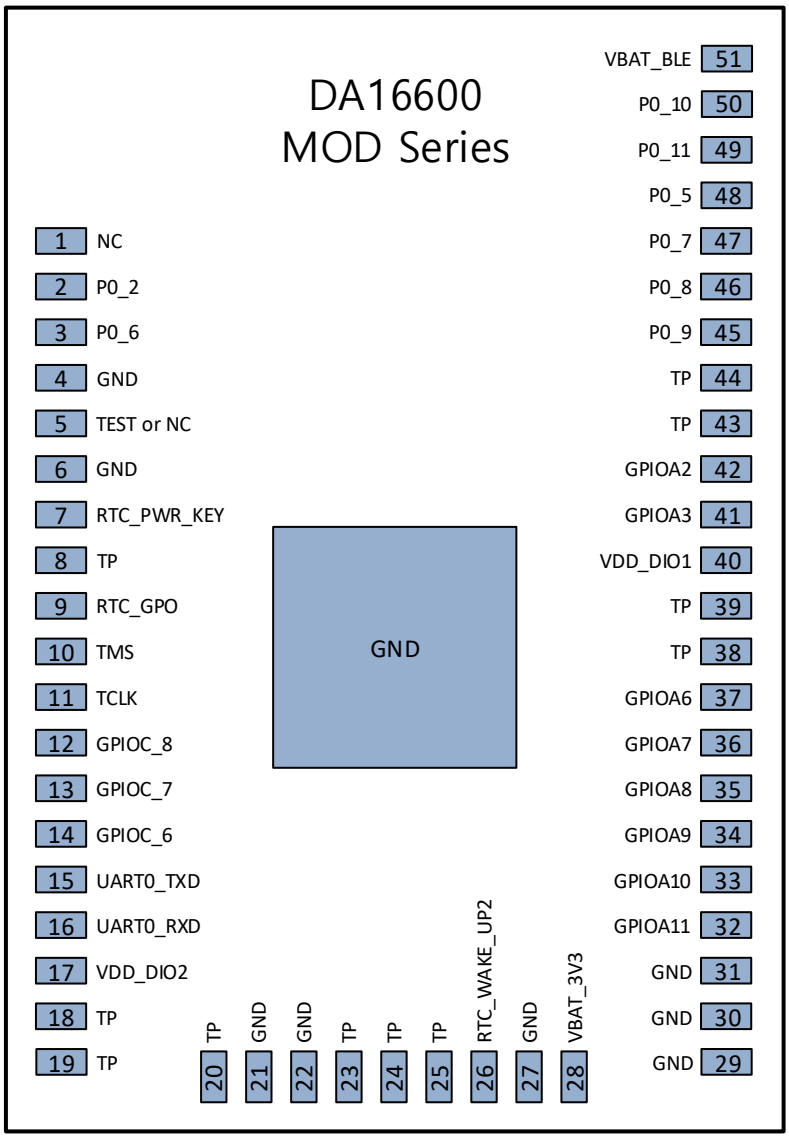


Figure 25. DA16600 51-pin pinout diagram

6.1 Pin Description

Table 17. Pin description

#Pin	Pin name	Type	Drive (mA)	Reset state	Related device	Description
1	NC	AI			DA14531	Not Connected
2	P0_2	DIO			DA14531	General Purpose I/O, JTAG I/F, SWCLK
3	P0_6	DIO			DA14531	Internally connected to RF switch (Note 1)
4	GND	GND			Common	Ground
5	TEST or NC	AI			Common	Chip antenna type: RF_Test u.FL connector type: NC
6	GND	GND			Common	Ground

#Pin	Pin name	Type	Drive (mA)	Reset state	Related device	Description
7	RTC_PWR_KEY	DI			DA16200	RTC block enable signal
8	TP	DNC			DA16200	RTC block wake up signal is internally connected. (Note 1)
9	RTC_GPO	DO			DA16200	Sensor control signal
10	TMS	DIO	2/4/8/12	I-PU	DA16200	JTAG I/F, SWDIO
11	TCLK	DIO	2/4/8/12	I-PD	DA16200	JTAG I/F, SWCLK, General Purpose I/O
12	GPIOC_8	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
13	GPIOC_7	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
14	GPIOC_6	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
15	UART0_TXD	DO	2/4/8/12	O	DA16200	UART transmit data
16	UART0_RXD	DI	2/4/8/12	I	DA16200	UART receive data
17	VDD_DIO2	VDD			DA16200	Supply power for digital I/O GPIOC6~GPIOC8, TMS/TCLK, TXD/RXD
18	TP	DNC			DA16200	F_IO0 is internally connected to Flash Memory
19	TP	DNC			DA16200	F_CLK is internally connected to Flash Memory
20	TP	DNC			DA16200	F_IO3 is internally connected to Flash Memory
21	GND	GND			Common	Ground
22	GND	GND			Common	Ground
23	TP	DNC			DA16200	F_IO1 is internally connected to Flash Memory
24	TP	DNC			DA16200	F_CSN is internally connected to Flash Memory
25	TP	DNC			DA16200	F_IO2 is internally connected to Flash Memory
26	RTC_WAKE_UP2	DI			DA16200	RTC block wake-up signal
27	GND	GND			Common	Ground
28	VBAT_3V3	VDD			DA16200	Supply power for internal DC-DC, DIO_LDO, and Analog IP of DA16200
29	GND	GND			Common	Ground
30	GND	GND			Common	Ground
31	GND	GND			Common	Ground
32	GPIOA11	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
33	GPIOA10	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
34	GPIOA9	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
35	GPIOA8	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
36	GPIOA7	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
37	GPIOA6	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
38	TP	DNC	2/4/8/12	I-PD	Common	GPIOA5 of DA16200 is internally connected to P0_3 of DA14531 (Note 1)
39	TP	DNC	2/4/8/12	I-PD	Common	GPIOA4 of DA16200 is internally connected to P0_4 of DA14531 (Note 1)
40	VDD_DIO1	VDD			DA16200	Supply power for digital I/O GPIOA0~GPIOA11
41	GPIOA3	AI/DIO	2/4/8/12	I-PD	DA16200	Aux. ADC input/General Purpose I/O

#Pin	Pin name	Type	Drive (mA)	Reset state	Related device	Description
42	GPIOA2	AI/DIO	2/4/8/12	I-PD	DA16200	Aux. ADC input/General Purpose I/O
43	TP	DNC	2/4/8/12	I-PD	Common	GPIOA1 of DA16200 is internally connected to P0_0 of DA14531 (Note 1 and Note 2)
44	TP	DNC	2/4/8/12	I-PD	Common	GPIOA0 of DA16200 is internally connected to P0_1 of DA14531 (Note 1)
45	P0_9	DIO	3.5 / 0.3	I-PD	DA14531	General Purpose I/O UART Debug TXD
46	P0_8	DIO	3.5 / 0.3	I-PD	DA14531	General Purpose I/O UART Debug RXD
47	P0_7	DIO	3.5 / 0.3	I-PD	DA14531	General Purpose I/O
48	P0_5	DIO	3.5 / 0.3	I-PD	DA14531	General Purpose I/O
49	P0_11	DIO	3.5 / 0.3	I-PD	DA14531	General Purpose I/O
50	P0_10	DIO	3.5 / 0.3	I-PD	DA14531	General Purpose I/O
51	VBAT_BLE	VDD			DA14531	Supply power for DA14531

Note 1 Pin3, Pin8, Pin 38, Pin 39, Pin 43, and Pin 44 are connected internally so these pins cannot be used as GPIO or as wake up input in application system.

Note 2 P0_0 has a reset function, but it is shared with GTL. It is recommended to connect the remaining GPIO as an additional reset function when P0_0 is not available for reset in abnormal situations.

This device provides various interfaces to support many different applications. In the DA16200, it is possible to control each pin according to the required application in reference to the pin multiplexing illustrated in Table 18 and Table 19. Pin control can be realized through register setting. In DA14531, I/O pin assignment can be configured by the software and is organized into the Port 0. See Ref. [1] and Ref. [4] for more information.

6.2 GPIO Pin Multiplexing

Table 18. DA16600 pin multiplexing

Pin	JTAG	Analog	SPI master	SPI slave	I2C master	I2C slave	Bluetooth coex
TP							
TP							
GPIOA2		CH2		SPI_CSB		I2C_SDA	
GPIOA3		CH3		SPI_CLK		I2C_CLK	
TP							
TP							
GPIOA6			SPI_CSB	SPI_CSB		I2C_SDA	
GPIOA7			SPI_CLK	SPI_CLK		I2C_CLK	
GPIOA8			SPI_DIO0/ SPI_MOSI	SPI_MISO	I2C_SDA		
GPIOA9			SPI_DIO1/ SPI_MISO	SPI_MOSI	I2C_CLK		BT_SIG0
GPIOA10			SPI_DIO2	SPI_MISO			BT_SIG1
GPIOA11			SPI_DIO3	SPI_MOSI			BT_SIG2
TCLK/GPIOA15	TCLK						
TMS	TMS						
UART_TXD							
UART_RXD							
GPIOC8	TDI						
GPIOC7	TDO						
GPIOC6	NTRST						

Table 19. DA16600 pin multiplexing (Continued)

Pin	I2S	I2S_Clock	UART2	Muxed w/Analog	Pin state (nRESET=0)	Driving strength (Default: 8 mA)
TP				Yes	I-PD	2/4/8/12 mA
TP				Yes	I-PD	2/4/8/12 mA
GPIOA2	SDO			Yes	I-PD	2/4/8/12 mA
GPIOA3	LRCK	CLK_IN		Yes	I-PD	2/4/8/12 mA
TP				No	I-PD	2/4/8/12 mA
TP				No	I-PD	2/4/8/12 mA
GPIOA6	SDO			No	I-PD	2/4/8/12 mA
GPIOA7	LRCK			No	I-PD	2/4/8/12 mA
GPIOA8	BCLK			No	I-PD	2/4/8/12 mA
GPIOA9	MCLK			No	I-PD	2/4/8/12 mA
GPIOA10		CLK_IN	TXD	No	I-PD	2/4/8/12 mA
GPIOA11			RXD	No	I-PD	2/4/8/12 mA
TCLK/GPIOA15				No	I-PD	2/4/8/12 mA
TMS				No	I-PD	2/4/8/12 mA
UART_TXD				No	O	2/4/8/12 mA
UART_RXD				No	I	2/4/8/12 mA
GPIOC8				No	I-PD	2/4/8/12 mA
GPIOC7			RXD	No	I-PD	2/4/8/12 mA
GPIOC6			TXD	No	I-PD	2/4/8/12 mA

Within the DA16600 module, various pins of the DA16200 and the DA14531 are internally connected and therefore cannot be used as GPIOs and are marked as TP (test points) on the DA16600MOD package. The GPIOs which are not available are:

- DA16200: GPIOA0, GPIOA1, GPIOA4, GPIOA5
- DA14531: P0_0, P0_1, P0_3, P0_4, P0_6

Due to these internal connections, the SDIO, SDeMMC, and UART1 interfaces of the DA16200 are not available. To support Bluetooth Coexistence, P06 of the DA14531 (which is internally connected to the RF switch) must be connected to a DA16200 GPIO pin as follows:

- For 1 pin Bluetooth Coexistence, connect P0_6 to GPIOA10
- For 3 pin Bluetooth Coexistence, connect P0_6 to GPIOA9

If GPIOA9 or GPIOA10 is used for Bluetooth Coexistence, then it cannot be used as a GPIO.

6.3 RF

The DA16600MOD contains both Wi-Fi and Bluetooth chipsets with a SPDT RF switch to select which chipset uses the RF. The RF path can be changed using the coexistence pin.

- Logic Low: Wi-Fi Path
- Logic High: BLE Path

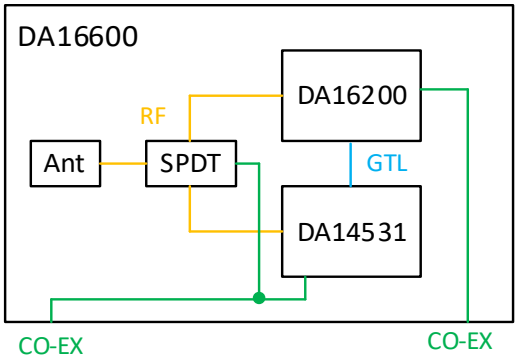


Figure 26. DA16600 RF diagram

6.3.1 Wi-Fi and Bluetooth® Coexistence

Table 20. Coexistence connection

DA14531 part	DA16200 part	Function
P0_5	GPIOA_8	Wi-Fi_ACT
P0_6	GPIOA_9	BT_ACT
P0_7	GPIOA_10	BT_PRIO

6.3.2 DA14531 Test

To perform Bluetooth RF tests, pinouts of the following two pins should be ready.

- P0_5 (#48 of DA16600MOD), it is required when DTM Test with SmartSnippets tool to download the binary (prod_test_531_1wire_P05.bin) for Bluetooth RF test.
  - The pre-built prod_test_531_1wire_P05.bin located in DA14531 SDK of DA16600 SDK: \DA16200_DA16600_SDK_FreeRTOS_Manufacture_*\utility\combo\da14531_sdk_v_6.0.14.1114\6.0.14.1114\binaries\da14531\prod_test\
- P0_0 (#43 of DA16600MOD), it is required when DTM Test with SmartSnippets tool for Bluetooth reset.

6.4 PCB Layout

6.4.1 Layout Example: DA16600

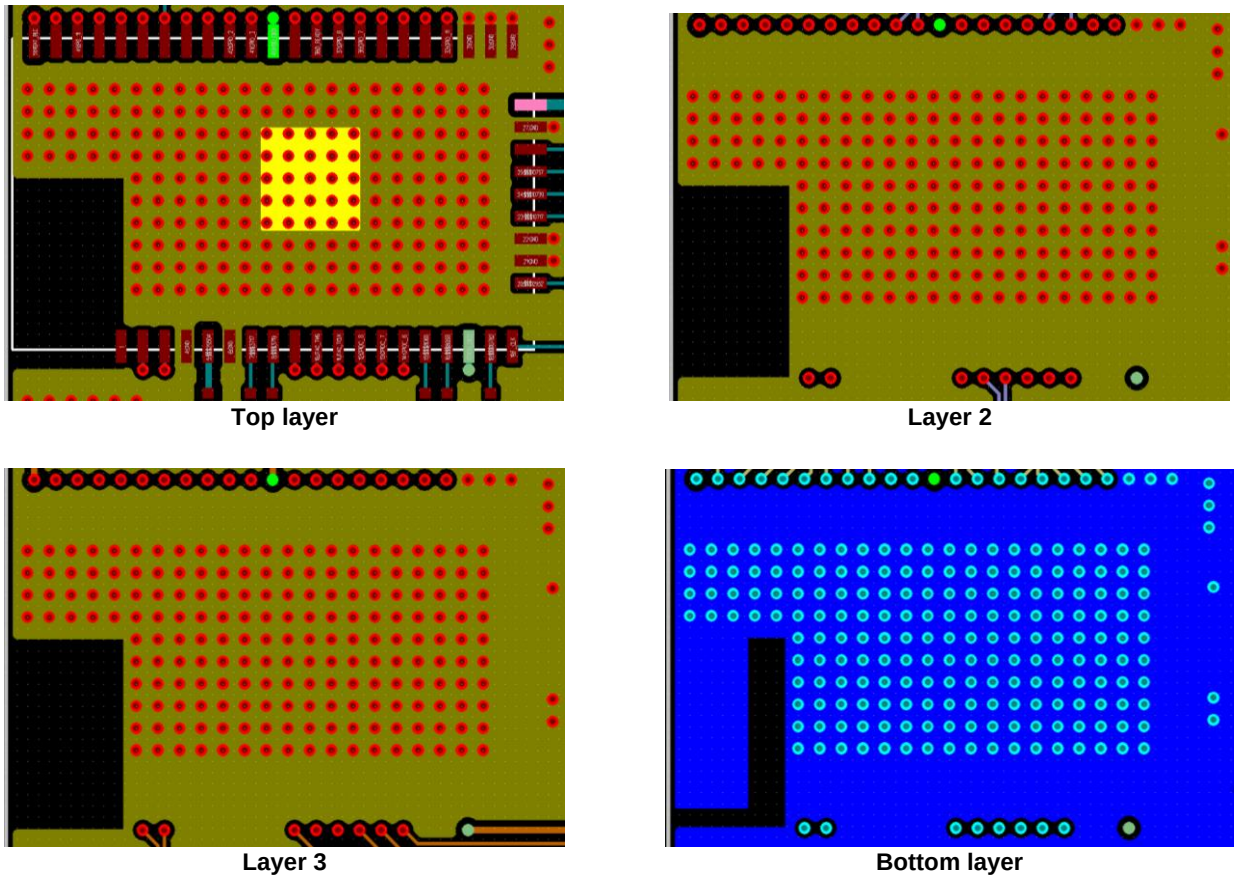


Figure 27. DA16600 4-layer PCB example

6.4.2 Recommended Footprint

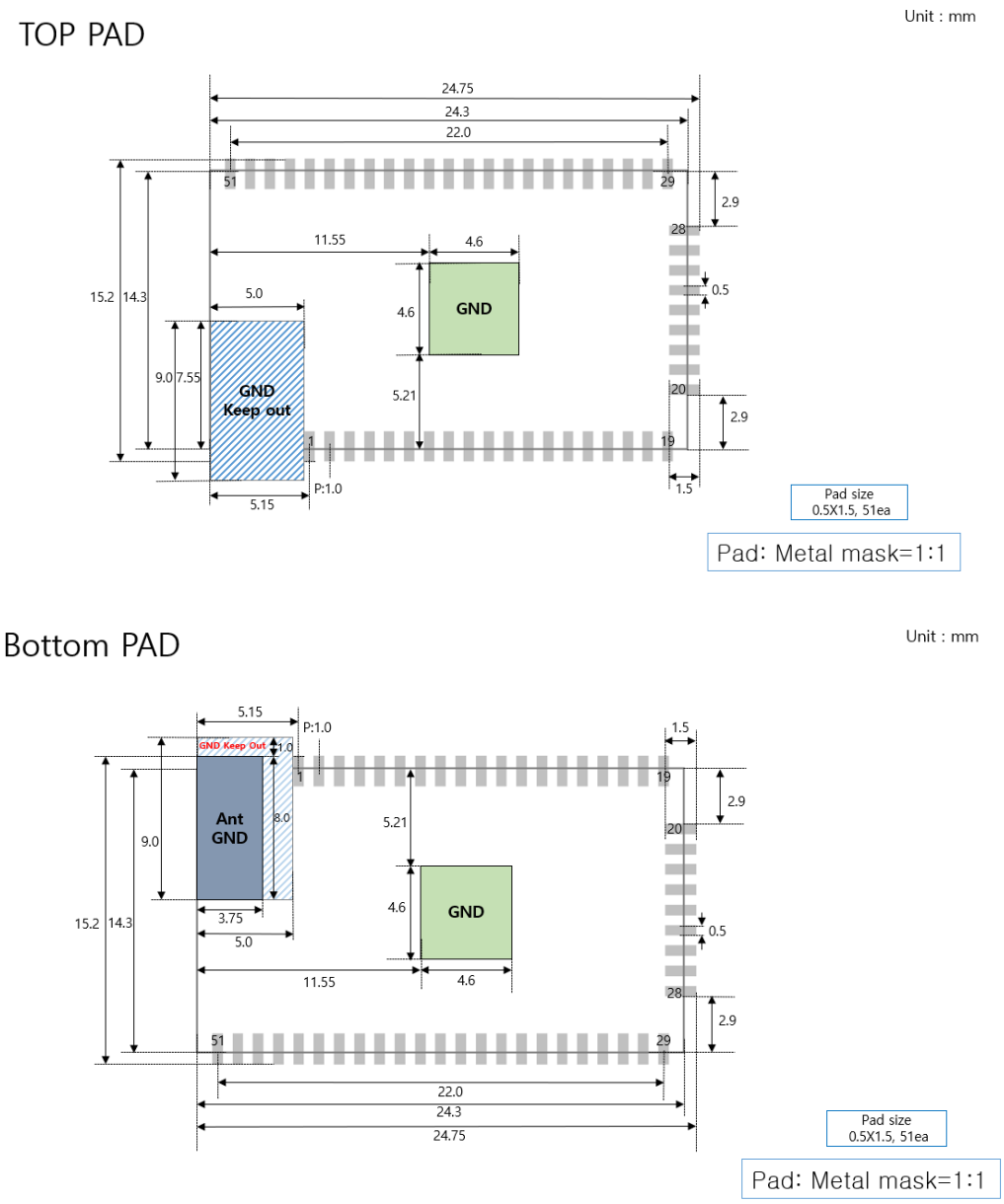


Figure 28. DA16600 ground footprint

Appendix A Antenna Diversity Function

The DA16200 and DA16600 provide an antenna switching diversity function to improve antenna performance in a multi-path environment. The PHY hardware block measures the Received Signal Strength Indicator (RSSI) of each antenna and selects the antenna with the largest RSSI. The selected antenna is also used for transmission. An external switching element is required to use the Antenna Switching Diversity function. Switch control is done through a GPIO. Two GPIOs are available for switch control. For this purpose, select any unused pins among the GPIO pins. The control signal can be changed with a register setting to match the external switching device. This function applies to single chips such as QFN or fcCSP, but not to DA16200MOD products with Antenna.

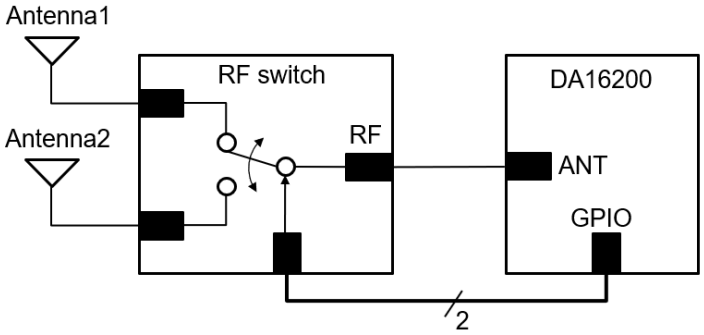


Figure 29. Antenna switch internal block diagram

A.1 Register Set

The antenna switching diversity uses the registers described in Table 21.

Table 21. GPIO alternate functions (0x4001003C)

Bit	Mode	Symbol	Description	Reset
12:0	R/W	FUNC_OUT_EN	Alternate Function output enable. [12 : UART2_TXDOE enable [11]: UART1_TXDOE enable [10]: UART0_TXDOE enable [9]: RF_SW2 enable [8]: RF_SW1 enable [7]: mSPI_CSB[3] enable (1=enable) [6]: mSPI_CSB[3] enable [5]: mSPI_CSB[1] enable [4]: Ext_Intr enable [3]: PWM_OUT[3] enable (1=enable) [2]: PWM_OUT[3] enable [1]: PWM_OUT[1] enable [0]: PWM_OUT[0] enable	0x0000

This register is responsible for designating the GPIO port as one of the alternate functions. Bit[9:8] should be set to "1" for RF switching signals used for the Antenna Switching Diversity function.

Table 22. RF switch output selection (0x40010FC8)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	RF_SW_OUTSEL	RF_SW[1:0] port selection. [7: 4]: port sel of the RF_SW2 [3: 0]: port sel of the RF_SW1	0x0000

This register is responsible for selecting the GPIO ports for RF switch control signals generated by the PHY hardware after measuring the RSSI of each antenna. When GPIOA[11] needs to be used for RF_SW2 while GPIOA[10] is used for RF SW1, 0xBA should be set, in which **B** is for GPIOA[11] and **A** for GPIOA[10].

Table 23. RF_Interface_Control (0x60C0C000)

Bit	Mode	Symbol	Description	Reset
19:18	R/W	AN_SW_Value2for_DIV	RF switch signals values when ANT2 selected	2'b01
17:16	R/W	AN_SW_Value1for_DIV	RF switch signals values when ANT1 selected	2'b10

This register is responsible for setting values for the RF switching signals of RF_SW1 and RF_SW2.

Table 24. Enabling antenna switch (0x60C036F0)

Bit	Mode	Symbol	Description	Reset
4	R/W	ANT_DIV_MODE_EN	1 for enable.	1'b0

This register enables the automatic Antenna Switching operation, when set. The PHY hardware measures the RSSI from both antennas and selects the one with the strongest RSSI generating RF switching control signals of RF_SW1 and RF_SW2 automatically. If software control is preferred over automatic antenna switching control, this register should not be enabled. It disables the automatic antenna switching operation of the PHY hardware. For manual control, the following registers are used to control the RF switch.

Table 25. Data direction set (0x40010010)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DataOut_Set	GPIO Data output enable set. 1 = Enable Output 0 = Enable Input	0x0000

Table 26. Data out (0x40010004)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	AS_VALUE	Antenna Number to select. 0: Antenna 1 1: Antenna 2	0x0000

When this register is set to value '1', the antenna with AS_VALUE in the Data direction setting register is selected and RW_SW1 and RF_SW2 must be disabled in the GPIO Alternate Functions register.

Appendix B Hardware Checklist

When creating a schematic, make sure to check the checklist for each application listed below to complete the correct schematic.

B.1 DA16200 – QFN

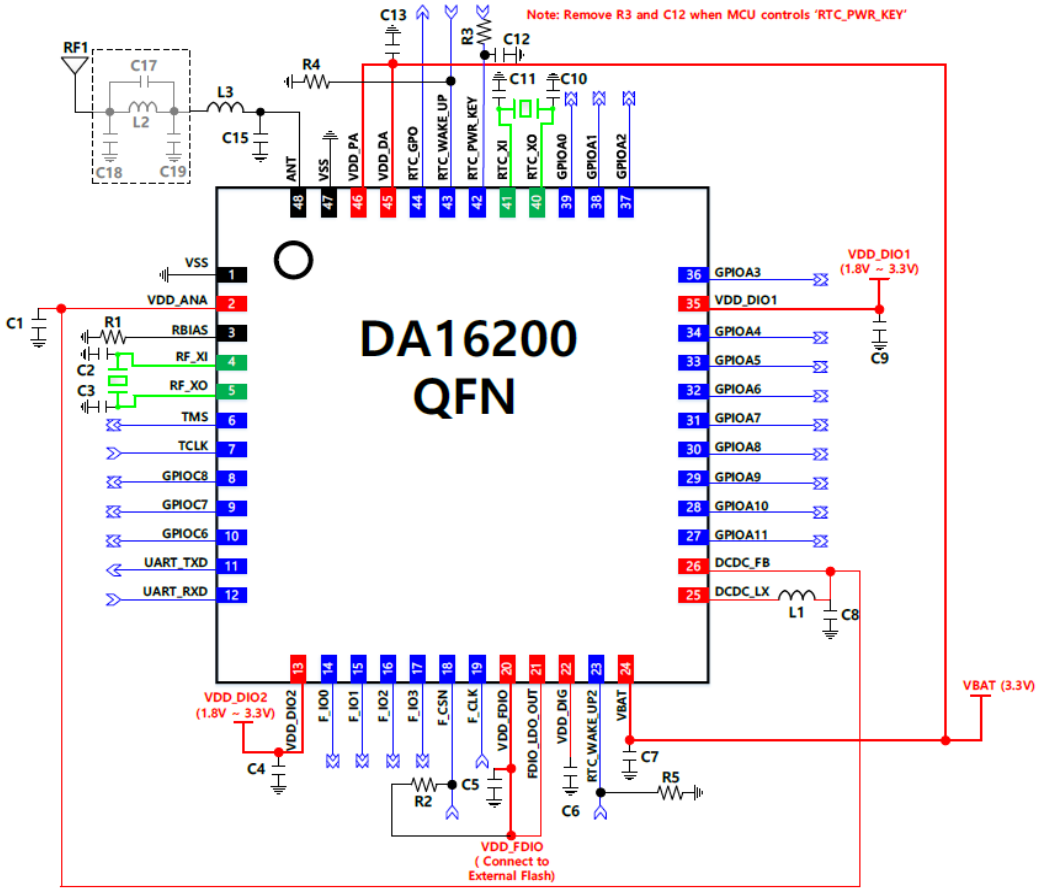


Figure 30. QFN reference for 1.8 V flash

Table 27. DA16200 QFN checklist

Pin number	Pin name	Check point
1, 47	VSS	GND
24	VBAT	Operating voltage 2.1~3.6 V (Typical 3.3 V)
2	VDD_ANA	Connect to DC-DC output (pin #25#26 DCDC_FB/DCDC_LX)
45, 46	VDD_DA, VDD_PA	Connect to VBAT (pin #24 VBAT)
25, 26	DCDC_LX, DCDC_FB	Need 4.7 µH power inductor and 10 µF capacitor
22	VDD_DIG	Do not connect to VDD (VBAT or DCDC_FB), just connect to 470nF bypass capacitor
20 21	VDD_FDIO FDIO_LDO_OUT	1.8 V flash memory: connect to FDIO_LDO_OUT (pin #21) and connect to VDD pin of flash, no need load switch
		3.3 V flash memory: connect to 3.3 V or VBAT through load switch and connect to VDD pin of flash memory
13, 35	VDD_DIO1, VDD_DIO2	Check I/O voltage of MCU (1.8~3.3 V)
3	RBIAS	Need 30 kΩ (1%)
4, 5	RF_XI, RF_XO	40 MHz RF XTAL, need to check load capacitance of XTAL (6~8 pF)

Pin number	Pin name	Check point
40, 41	RTC_XO, RTC_XI	32.768 kHz RTC XTAL is not needed when Sleep mode 1 is used.
48	ANT	Need to check the values of input matching and bandpass filter
42	RTC_PWR_KEY	Input high voltage > 2.2 V @3.3 V VDD (I/O voltage check)
		Renesas recommends that MCU controls RTC_PWR_KEY. If not, RC delay circuit (470 kΩ and 1 µF) is needed.
23, 43	RTC_WAKE_UP	Input high voltage > 2.2 V @3.3 V VDD (I/O voltage check)
		4.7 kΩ pull-down resistor (can be removed and RTC_WAKE_UP1/2 can be connected to GND directly when not used)
6, 7	TMS, TCLK	JTAG debug, test point
11, 12	UART_TXD, UART_RXD	Console debug, test point
14	F_IO0	F_SO to pin #5 (DI, SI or IO0) of flash memory
15	F_IO1	F_SI to pin #2 (DO, SO or IO1) of flash memory
16	F_IO2	F_WP to pin #3 (WP or IO2) of flash memory
17	F_IO3	F_HOLD pin #7 (HOLD, RESET or IO3) of flash memory
18	F_CSN	F_CS to pin #1 (CSN or CSB) of flash memory, 10 kΩ pull-up resistor
19	F_CLK	F_CLK to pin #6 (CLK or SCK) of flash memory
44	RTC_GPO	Need to check the purpose of this pin when this pin is used
8~10	GPIOC6~C8	Need to check GPIO pin mux (See Table 14 and Table 15)
27~34	GPIOA4~A11	
36~39	GPIOA0~A3	
31, 32	GPIOA6~A7	Need to disable the WPS/factory reset functions on SDK or add pull-up resistors to remove the leakage current.
	Serial flash	Check part number of serial flash (see supported flash list)
		Noted that the DA16200 can support only high-performance flash of MXIC.
	Interface interrupt	Assign 1 GPIO for interrupt when SPI or SDIO is used. (GPIOC6 is assigned as SPI interrupt by default.)
	Interface pull-up	Need pull-up resistors when I2C or SDIO is used.
	MCU interrupt	GPIOA11 is set as interrupt for MCU wake-up by default when AT command function is enabled.
	High speed interface	Recommend adding damping resistors (22~33 Ω) and need to review the artwork when high speed SPI/SDIO is used.
	RF test	Need pinout of UART1/2 interface if RF test is needed. (CLI through UART0 is also possible for simple RF test.)

B.2 DA16200 – fcCSP

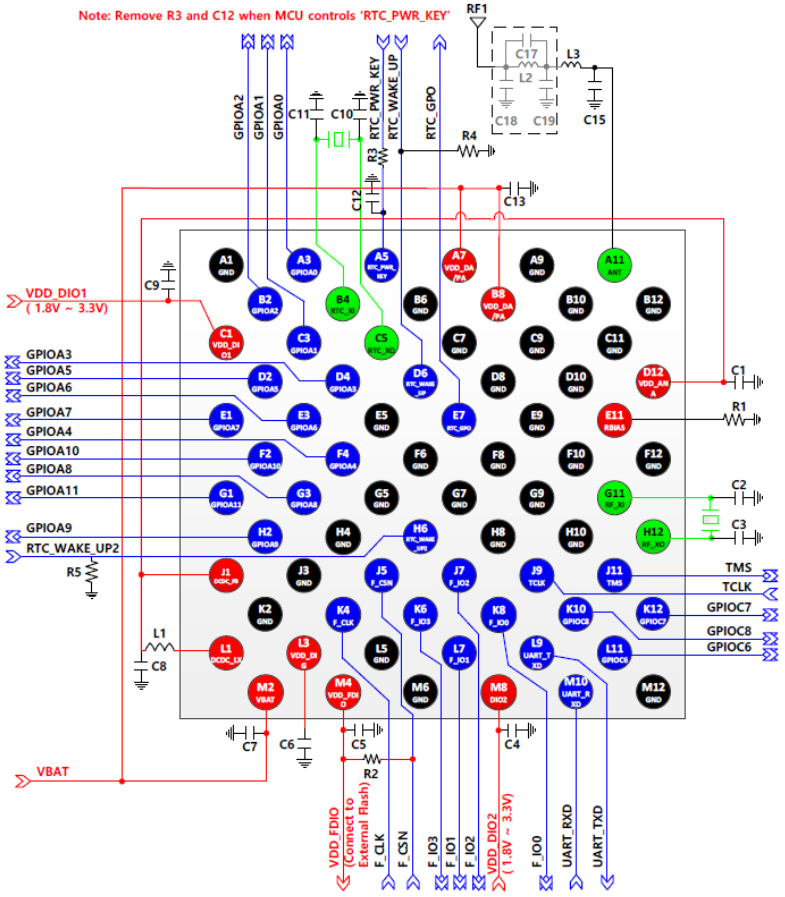


Figure 31. fcCSP reference for normal power mode with 1.8 V flash

Table 28. DA16200 fcCSP checklist

Pin number	Pin name	Check point
A1, A9	VSS	GND
B6, B10, B12		
C7, C9, C11		
D8, D10		
E5, E9		
F6, F8, F10, F12		
G5, G7, G9, H4, H8, H10		
J3		
K2		
L5		
M6, M12		
M2	VBAT	Operating voltage 2.1~3.6 V (Typical 3.3 V)
D12	VDD_ANA	Connect to DC-DC output (pin #J1/#L1 DCDC_FB/DCDC_LX)
A7, B8	VDD_DA/PA	Normal TX power mode: connect to VBAT (3.3 V) (pin #M2 VBAT)
		Low TX power mode: connect to DC-DC output (1.4 V) (pin #J1/#L1 DCDC_FB/DCDC_LX)
J1, L1	DCDC_LX, DCDC_FB	Needs 4.7 µH power inductor and 10 µF capacitor
L3	VDD_DIG	Do not connect to VDD (VBAT or DCDC_FB), just connect to 470 nF bypass capacitor

Pin number	Pin name	Check point
M4	VDD_FDIO	1.8 V flash memory: connect to VDD pin of flash, no need load switch
		3.3 V flash memory: connect to 3.3 V or VBAT through load switch and connect to VDD pin of flash memory
C1, M8	VDD_DIO1, VDD_DIO2	Check I/O voltage of MCU (1.8~3.3 V)
E11	RBIAS	Needs 30 kΩ (1%)
G11, H12	RF_XI, RF_XO	40 MHz RF XTAL, need to check load capacitance of XTAL (6~8 pF)
B4, C5	RTC_XO, RTC_XI	32.768 kHz RTC XTAL, RTC_XTAL is not needed when Sleep mode 1 is used.
A11	ANT	Need to check the values of input matching and bandpass filter
A5	RTC_PWR_KEY	Input high voltage > 2.2 V @3.3V VDD (I/O voltage check)
		Renesas recommends that MCU controls RTC_PWR_KEY. If not, RC delay circuit (470 kΩ and 1 µF) is needed.
D6, H6	RTC_WAKE_UP, UP2	Input high voltage > 2.2 V @3.3 V VDD (I/O voltage check)
		4.7 kΩ pull-down resistor (can be removed and RTC_WAKE_UP1/2 can be connected to GND directly when not used)
J9, J11	TMS, TCLK	JTAG debug, test point
L9, M10	UART_TXD, UART_RXD	Console debug, test point
K8	F_IO0	F_SO to pin #5 (DI, SI or IO0) of flash memory
L7	F_IO1	F_SI to pin #2 (DO, SO or IO1) of flash memory
J7	F_IO2	F_WP to pin #3 (WP or IO2) of flash memory
K6	F_IO3	F_HOLD pin #7 (HOLD, RESET or IO3) of flash memory
J5	F_CSN	F_CS to pin #1 (CSN or CSB) of flash memory, 10 kΩ pull-up resistor
K4	F_CLK	F_CLK to pin #6 (CLK or SCK) of flash memory
E7	RTC_GPO	Need to check the purpose of this pin when this pin is used
A3, C3, B2, D4	GPIOA0~A3	Need to check GPIO pin mux (See Table 14 and Table 15)
F4, D2, E3, E1	GPIOA4~A7	
G3, H2, F2, G1	GPIOA8~A11	
L11, K12, K10	GPIOC6~C8	
E1, E3	GPIOA6~A7	Need to disable the WPS/factory reset functions on SDK or add pull-up resistors to remove the leakage current.
	Serial flash	Check part number of serial flash (see supported flash list)
		Noted that the DA16200 can support only high-performance flash of MXIC.
	Interface interrupt	Assign 1 GPIO for interrupt when SPI or SDIO is used. (GPIOC6 is assigned as SPI interrupt by default.)
	Interface pull-up	Need pull-up resistors when I2C or SDIO is used.
	MCU interrupt	GPIOA11 is set as interrupt for MCU wake-up by default when AT command function is enabled.
	High speed interface	Recommend adding damping resistors (22~33 Ω) and need to review the artwork when high speed SPI/SDIO is used.
	RF test	Need pinout of UART1/2 interface if RF test is needed. (CLI through UART0 is also possible for simple RF test.)

B.3 DA16200MOD for FreeRTOS SDK

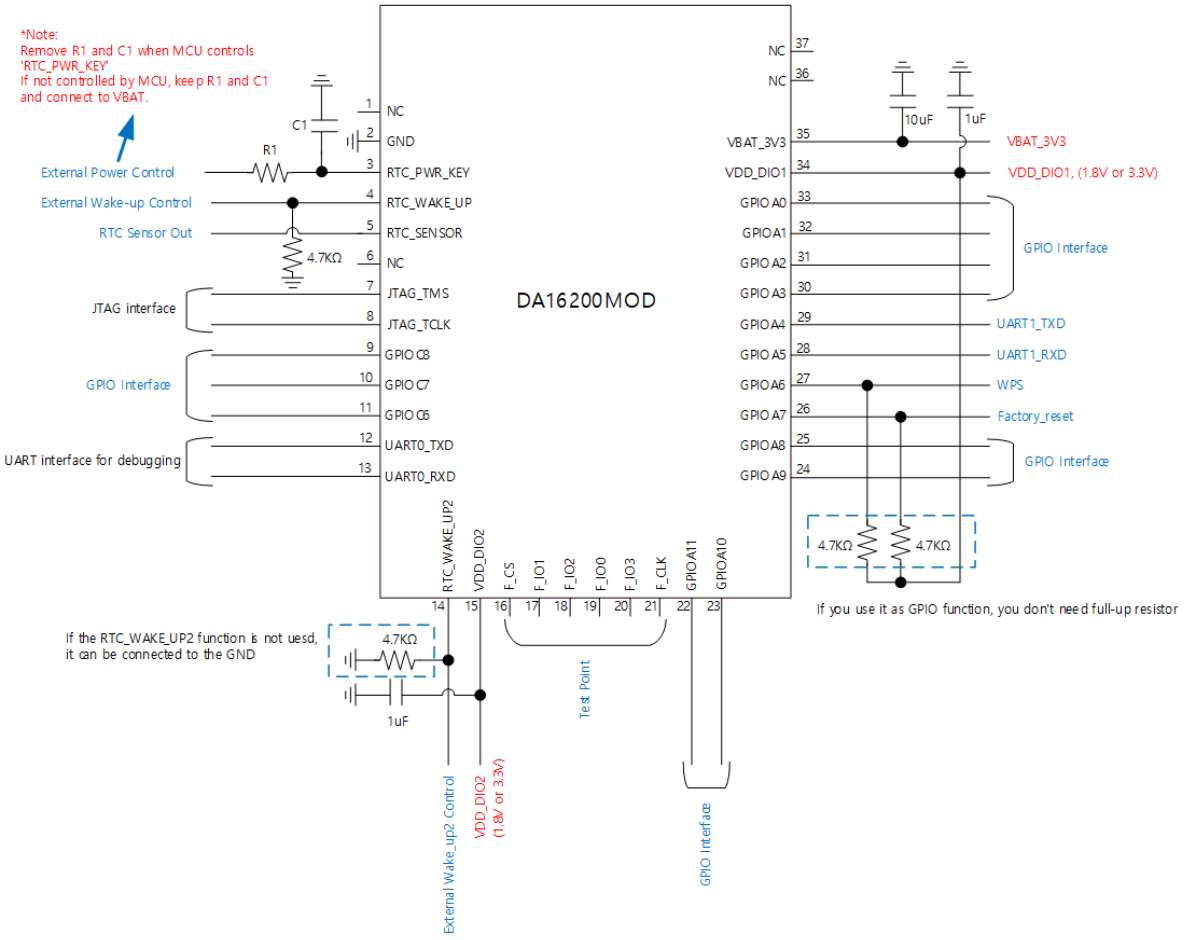


Figure 32. DA16200MOD reference for FreeRTOS SDK

Table 29. DA16200MOD checklist for FreeRTOS SDK

Pin number	Pin name	Check point
1, 6, 36, 37	NC	Not connect
2	GND	GND
35	VBAT_3V3	Operating voltage 2.1~3.6 V (Typical 3.3 V)
15, 34	VDD_DIO1, VDD_DIO2	Check I/O voltage of MCU (1.8~3.3 V)
3	RTC_PWR_KEY	Input high voltage > 2.2 V @3.3V VDD (I/O voltage check)
		Renesas recommends that MCU controls RTC_PWR_KEY. If not, RC delay circuit (470 kΩ and 1 µF) is needed.
4, 14	RTC_WAKE_UP, UP2	Input high voltage > 2.2 V @3.3 V VDD (I/O voltage check)
		4.7 kΩ pull-down resistor (can be removed and RTC_WAKE_UP1/2 can be connected to GND directly when not used)
7, 8	JTAG_TMS, JTAG_TCLK	JTAG debug, test point
12,13	UART0_TXD, UART0_RXD	Console debug, test point
16~21	F_xx	Test point
5	RTC_SENSOR	Need to check the purpose of this pin when this pin is used
9~11	GPIOC6~C8	Need to check GPIO pin mux (See Table 14 and Table 15)
22~33	GPIOA0~A11	

Pin number	Pin name	Check point
26, 27	GPIOA6~A7	Need to disable the WPS/factory reset functions on SDK or add pull-up resistors to remove the leakage current.
	Interface interrupt	Assign 1 GPIO for interrupt when SPI or SDIO is used. (GPIOC6 is assigned as SPI interrupt by default.)
	Interface pull-up	Need pull-up resistors when I2C or SDIO is used.
	MCU interrupt	GPIOA11 is set as interrupt for MCU wake-up by default when AT command function is enabled.
	High speed interface	Recommend adding damping resistors (22~33 Ω) and need to review the artwork when high speed SPI/SDIO is used.
	RF test	Need pinout of UART1/2 interface if RF test is needed. (CLI through UART0 is also possible for simple RF test.)

B.4 DA16200MOD for Linux Driver

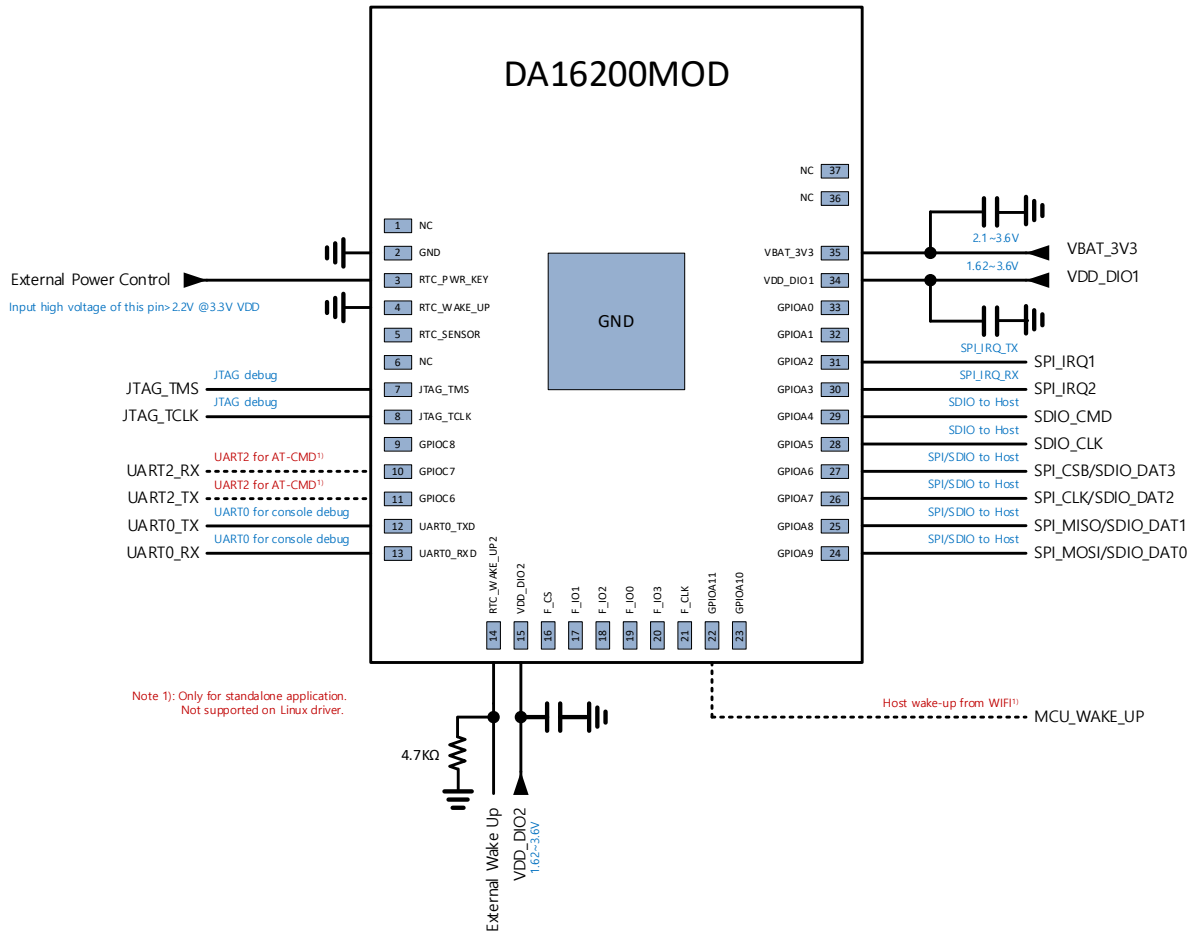


Figure 33. DA16200MOD reference for Linux driver

B.5 DA16600 for FreeRTOS SDK

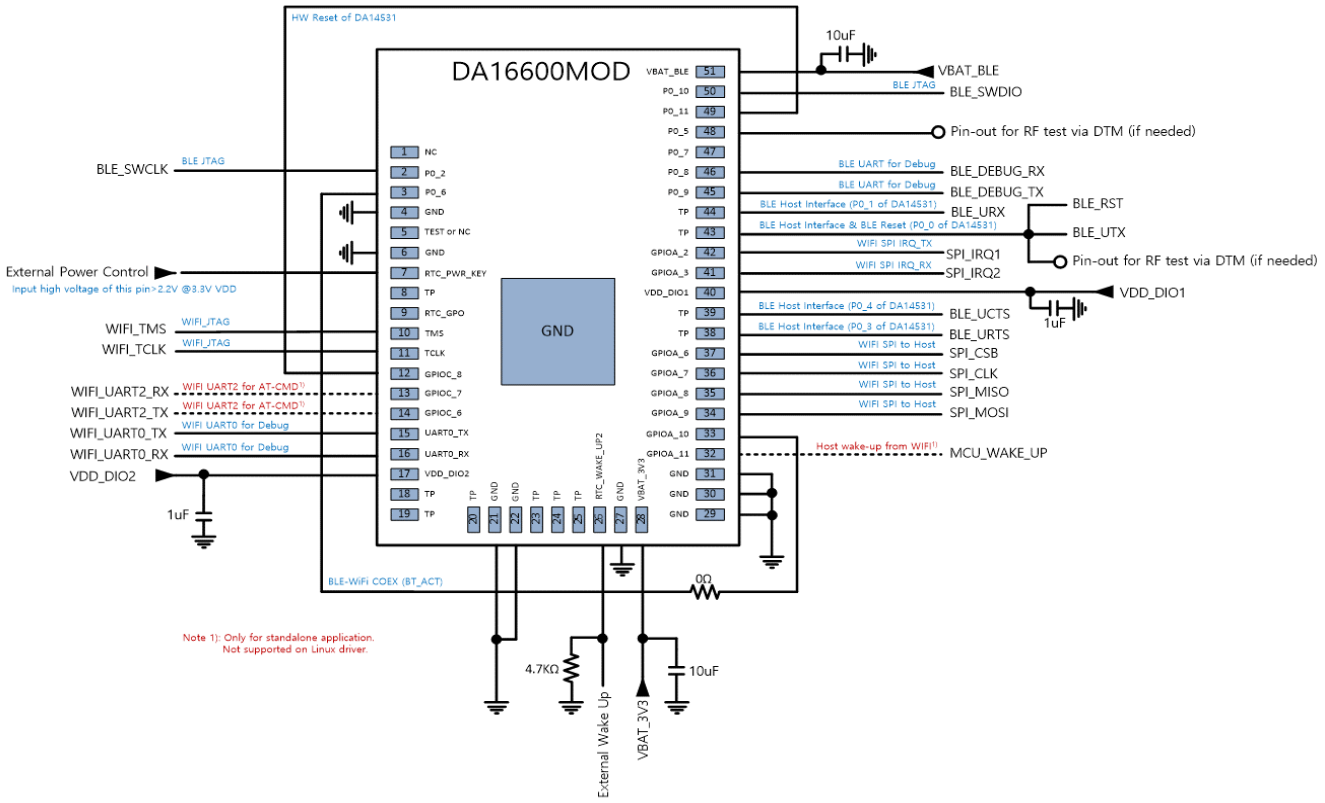


Figure 34. DA16600 reference for FreeRTOS SDK

Table 30. DA16600 checklist for FreeRTOS SDK

Pin number	Pin name	Check point
1, 5	NC	Not connected
8, 18, 19, 20 23, 24, 25 38, 39, 43, 44	TP	Test point, do not connect to other components
4, 6, 21, 22 27, 29, 30, 31	GND	GND
28	VBAT_3V3	Operating voltage 2.1~3.6 V (Typical 3.3 V), 10 µF bypass capacitor
51	VBAT_BLE	Operating voltage 1.8~3.3 V (Max 3.3 V), 10 µF bypass capacitor
17, 40	VDD_DIO1, VDD_DIO2	Check I/O voltage of MCU (1.8~3.3 V)
7	RTC_PWR_KEY	Input high voltage > 2.2 V @3.3 V VDD (I/O voltage check) Renesas recommends that MCU controls RTC_PWR_KEY. If not, RC delay circuit (470 kΩ and 1 µF) is needed.
26	RTC_WAKE_UP2	Input high voltage > 2.2 V @3.3 V VDD (I/O voltage check) 4.7 kΩ pull-down resistor (can be removed and RTC_WAKE_UP1/2 can be connected to GND directly when not used)
10, 11	TMS, TCLK	JTAG debug, test point
15, 16	UART0_TX, UART0_RX	Console debug, test point
35, 48	GPIOA8, P0_5	BT-Wi-Fi COEX: WIFI ACT, need to connect externally
34, 3	GPIOA9, P0_6	BT-Wi-Fi COEX: BT_ACT, need to connect externally (internally connected to SPDT)
33, 47	GPIOA10, P0_7	BT-Wi-Fi COEX: BT_PRIO, need to connect externally, GPIOA_10 can be assigned to BT_ACT when 1-pin COEX

Pin number	Pin name	Check point
2, 50	P0_2, P0_10	GPIO of DA14531, can be to assign as JTAG debug port
45, 46	P0_8,9	GPIO of DA14531, can be to assign as UART debug port
49	P0_11	GPIO of DA14531, recommend assigning as hardware reset pin of DA14531 with GPIOC8
9	RTC_GPO	Need to check the purpose of this pin when this pin is used
12~14	GPIOC6~C8	Need to check GPIO pin mux (See Table 14 and Table 15)
32	GPIOA11	
36, 37	GPIOA6~A7	
41, 42	GPIOA2~A3	
36, 37	GPIOA6~A7	Need to disable the WPS/factory reset functions on SDK or add pull-up resistors to remove the leakage current.
	Hardware reset of DA14531	Assign hardware reset pin for DA14531, GPIOC_8 of DA16200 and P0_11 of DA14531 is recommended.
	Interface interrupt	Assign 1 GPIO for interrupt when SPI or SDIO is used. (GPIOC6 is assigned as SPI interrupt by default.)
	Interface pull-up	Need pull-up resistors when I2C or SDIO is used.
	MCU interrupt	GPIOA11 is set as interrupt for MCU wake-up by default when AT command function is enabled.
	High speed interface	Recommend adding damping resistors (22~33 Ω) and need to review the artwork when high speed SPI/SDIO is used.
	RF test	DA16200: Need pinout of UART2 interface if RF test is needed. (CLI through UART0 is also possible for simple RF test.)
		DA14531: Need pinout of #48 P0_5 for 1 wire UART and #43 TP (P0_0) for DA14531 POR if RF test is needed.

B.6 DA16600 for Linux Driver

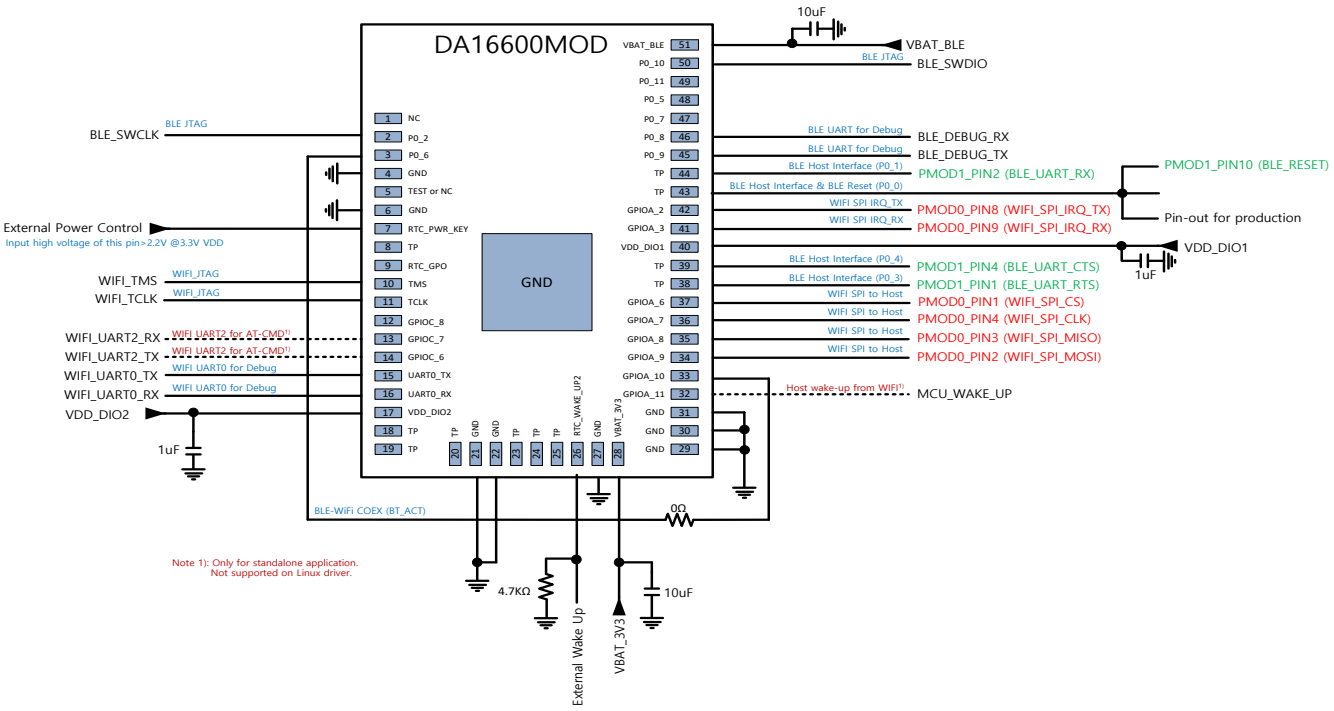


Figure 35. DA16600 reference for Linux driver

Table 31. DA16600 checklist for Linux driver

Pin number	Pin name	Check point
1, 5	NC	Not connected

Pin number	Pin name	Check point
8, 18, 19, 20	TP	Test point, do not connect to other components
23, 24, 25		
4, 6, 21, 22	GND	GND
27, 29, 30, 31		
28	VBAT_3V3	Operating voltage 2.1~3.6 V (Typical 3.3 V), 10 µF bypass capacitor
51	VBAT_BLE	Operating voltage 1.8~3.3 V (Max 3.3 V), 10 µF bypass capacitor
17, 40	VDD_DIO1, VDD_DIO2	Check I/O voltage of MCU (1.8~3.3 V)
7	RTC_PWR_KEY	Input high voltage > 2.2 V @3.3 V VDD (I/O voltage check)
		Renesas recommends that MCU controls RTC_PWR_KEY. If not, RC delay circuit (470 kΩ and 1 µF) is needed.
26	RTC_WAKE_UP2	Connected to GND as not used normally on Linux driver
10,11	TMS, TCLK	JTAG debug, test point
15,16	UART0_TX, UART0_RX	Console debug, test point
3,33	P0_6, GPIOA10	BT-Wi-Fi single-wire COEX: BT_ACT, need to connect externally (internally connected to SPDT)
2,50	P0_2/10	GPIO of DA14531, can be to assign as JTAG debug port
45,46	P0_9/8	GPIO of DA14531, can be to assign as UART debug port
49	P0_11	GPIO of DA14531
9	RTC_GPO	Need to check the purpose of this pin when this pin is used
12	GPIOC8	GPIO of DA16200
13,14	GPIOC7/C6	Can be assigned as Wi-Fi UART2 for AT command for stand-alone application
32	GPIOA11	Can be assigned as Host wake-up from Wi-Fi for AT command for stand-alone application
34	GPIOA9	Wi-Fi SPI to Host: assign as WIFI_SPI_MOSI
35	GPIOA8	Wi-Fi SPI to Host: assign as WIFI_SPI_MISO
36	GPIOA7	Wi-Fi SPI to Host: assign as WIFI_SPI_CLK
37	GPIOA6	Wi-Fi SPI to Host: assign as WIFI_SPI_CS
41,42	GPIOA3/A2	Wi-Fi SPI to Host: assign as INTs (RX/TX) for Wi-Fi SPI
38	TP (P0_3)	Bluetooth Host interface: assign as BLE_UART_RTS (P0_3)
39	TP (P0_4)	Bluetooth Host interface: assign as BLE_UART_CTS (P0_4)
43	TP (P0_0)	Bluetooth Host interface: assign as BLE_UART_TX and Bluetooth Reset (P0_0, should connect to 2 different GPIOs of MCU)
44	TP (P0_1)	Bluetooth Host interface: assign as BLE_UART_RX (P0_1)
47,48	P0_7/5	GPIO of DA14531
38,39,43,44	DA14531 Host Interface	MCU should make DA14531 UART lines as high-Z or pulled-down when DA14531 is not operated as DA14531 POR is not worked normally.
	High speed interface	Recommend adding damping resistors (22~33 Ω) and need to review the artwork when high speed SPI/SDIO is used.
	RF test	DA16200: Need pinout of UART2 interface if RF test is needed. (CLI through UART0 is also possible for simple RF test.)
		DA14531: Need pinout of #48 P0_5 for 1 wire UART and #43 TP (P0_0) for DA14531 POR if RF test is needed.

7. Revision History

Revision	Date	Description
1.9	Jan 8, 2025	Added SFDPs in Table 10
1.8	June 05, 2024	Updated the recommended serial flash list and Flash Verification Process
1.7	June 30, 2023	▪ Added note to reference document in Section 4 ▪ Updated the reference section
1.6	Jan. 12, 2023	▪ Updated RTC GPO Description in Section 5.10 ▪ Updated RTC Clock in Section 5.7.2 ▪ Added AN-WI-008 to Appendix A ▪ Added hardware checklist to Appendix B ▪ Added DA16600 information
1.5	Apr. 11, 2022	▪ Updated logo, disclaimer, and copyright ▪ Added a note about FreeRTOS SDK supporting flash sizes greater than 4 MB
1.4	Oct. 08, 2021	▪ Updated Section 5: • Added more information about package and pin • Added the information of chip antenna for DA16200MOD • Added RF XTAL trimming information • Updated the recommended serial flash list • Added Application Schematic ▪ Added Sections 5.9, 5.10, 5.11, and 5.12
1.3	Oct. 14, 2020	Updated Table 10 and Section 5.4.1
1.2	Oct. 29, 2019	Removed Draft status and finalized for release
1.1	Oct. 21, 2019	Editorial review
1.0	Aug. 30, 2019	First Release

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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