

Quick Start

DEMO8763x Demonstration Board for ADC1004S030/040/050 family

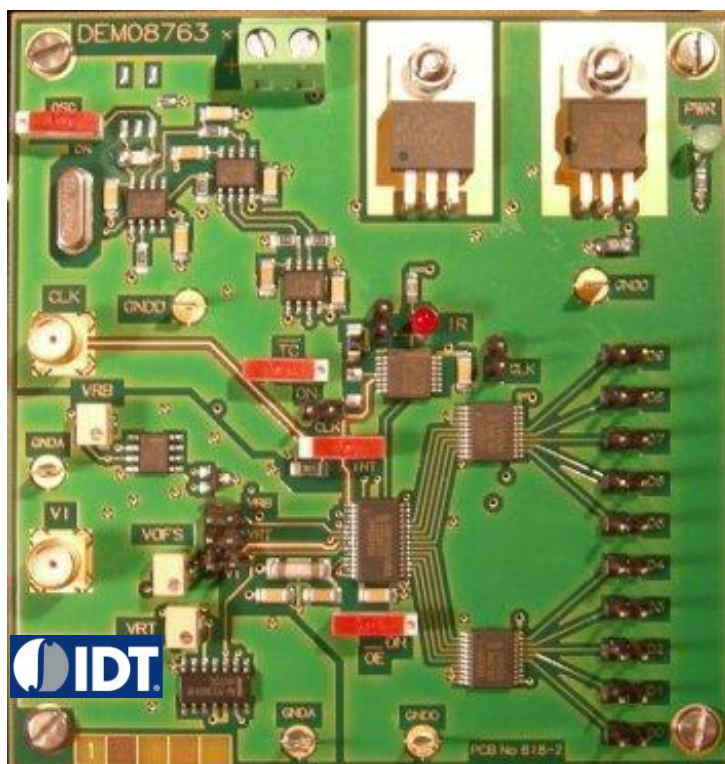
Rev. 2.0 — 2 July 2012

Quick Start

Document information

Info	Content
Keywords	DEMO8763x, PCB618-2, Demonstration board, ADC, Converter, ADC1004S030/040/050
Abstract	This document describes how to use the demonstration board DEMO8763x for the analog-to-digital converter ADC1004S030/040/050 family.

Overview



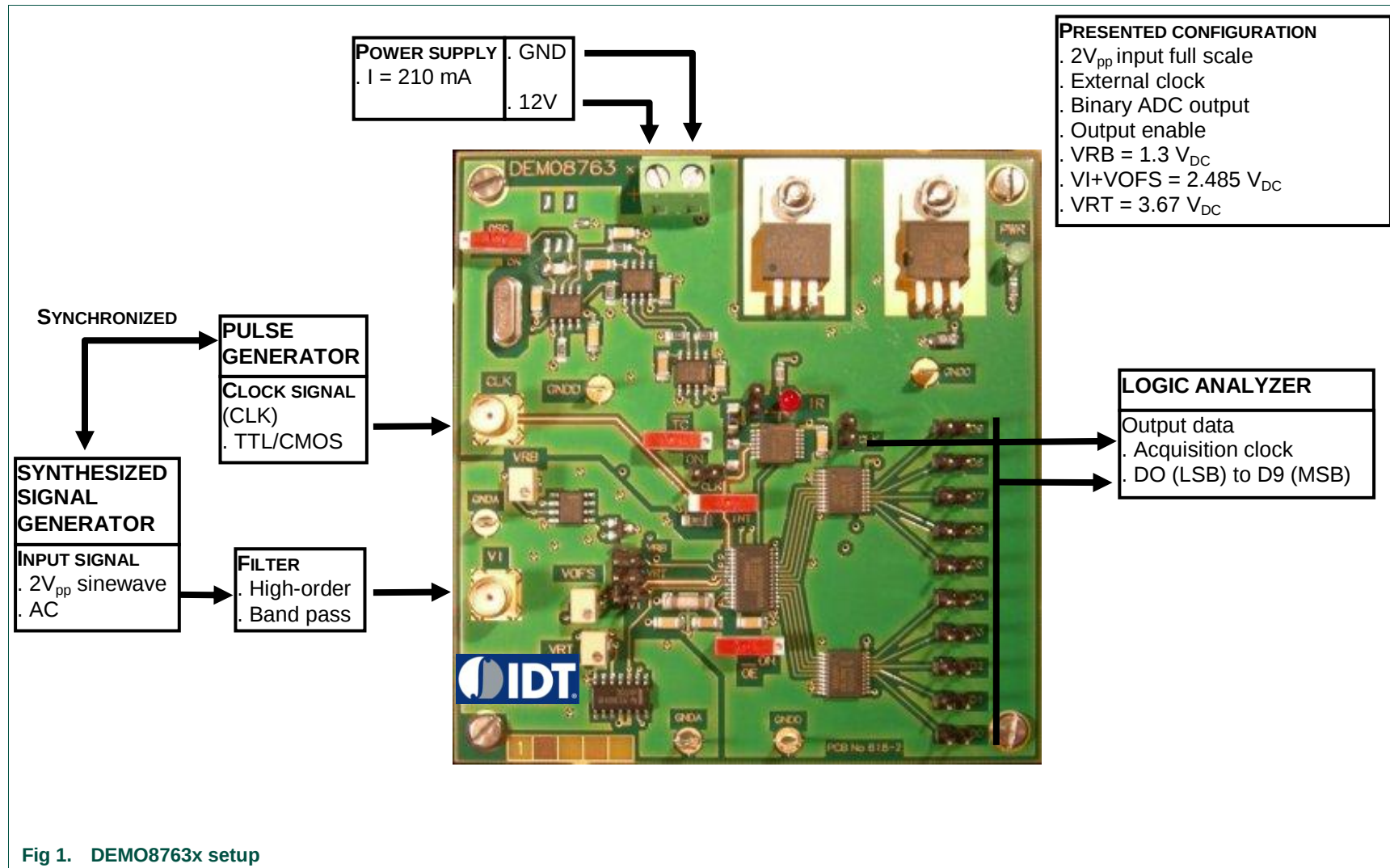
Revision history

Rev	Date	Description
2.0	20120702	Rebranded.
0.1	20080624	Initial version.

1. Quick start

1.1 Setup overview

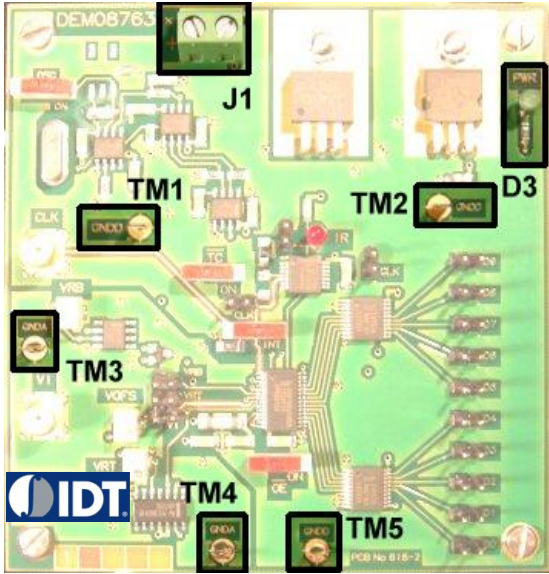
Figure Fig 1 presents the connections to measure DEMO8763x.



1.2 Power supply

The board is powered with a single 12 V_{DC} power supply. Two power supply regulators are used to supply all the 5V and 3.3V circuitry on the board.

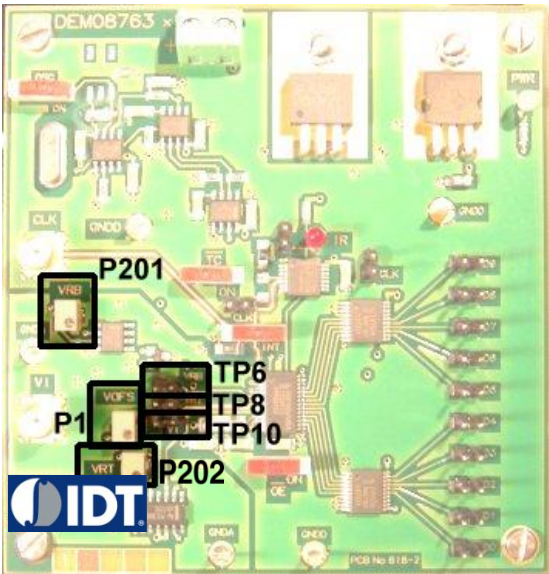
Table 1. General power supply

Name	Function	View
J1	Green connector – Power supply 12 V _{DC} / 210 mA.	
D3	PWR green light – It indicates the good supply plugging	
TM3, TM4	GNDA test point – Analog ground	
TM1, TM5	GNDD test point – Digital ground	
TM2	GNDO test point – Digital output ground	

1.3 DC voltage adjustments

The ADC1004S030/040/050 allows to adjust the full scale input signal from 1.7V to 2.5V.

Table 2. DC voltage adjustments

Name	Function	View
P202	VRT trimmer – TOP reference adjustment	
TP8	VRT test point – TOP reference value (typ 3.67 V)	
P201	VRB trimmer – BOT reference adjustment	
TP6	VRB test point – BOT reference value (typ 1.3 V)	
P1	VOFS trimmer – Input signal DC offset adjustment	
TP10	VI test point – Input signal (typ DC offset 2.485 V)	

1.4 Input signals (IN, CLK)

To ensure a good evaluation of the device, the input signal and the input clock must be synchronized together.

Moreover, the input frequency (F_i , MHz) and the clock frequency (F_{clk} , Msp/s) should follow the formula:

$$\frac{F_i}{F_{clk}} = \frac{M}{N}$$

,where M is an odd number of period and N is the number of samples.

Table 3. Input signals

Name	Function	View
J3	VI connector – Analog input signal (50Ω matching)	
J2	CLK connector – Clock input signal (50Ω matching)	
K1	OSC switch – On-board oscillator activation	
K3	CLK switch – Selection between on-board clock and external clock	
TP2	CLK test point – Clock used by the device	

1.5 Output signals (D0 to D9, IR)

Table 4. Output signals

Name	Function	View
TP11 to TP20	Array connector – ADC digital output (D0 to D9)	
D2, TP3	IR red light and test point – It indicates that the analog input signal is out of the full scale range	
TP31	CLK connector – Clock output for data acquisition	
K2	TCN switch – 2's complement output selection	
K4	OEN switch – Output enable selection	

2. Example

2.1 Setup example

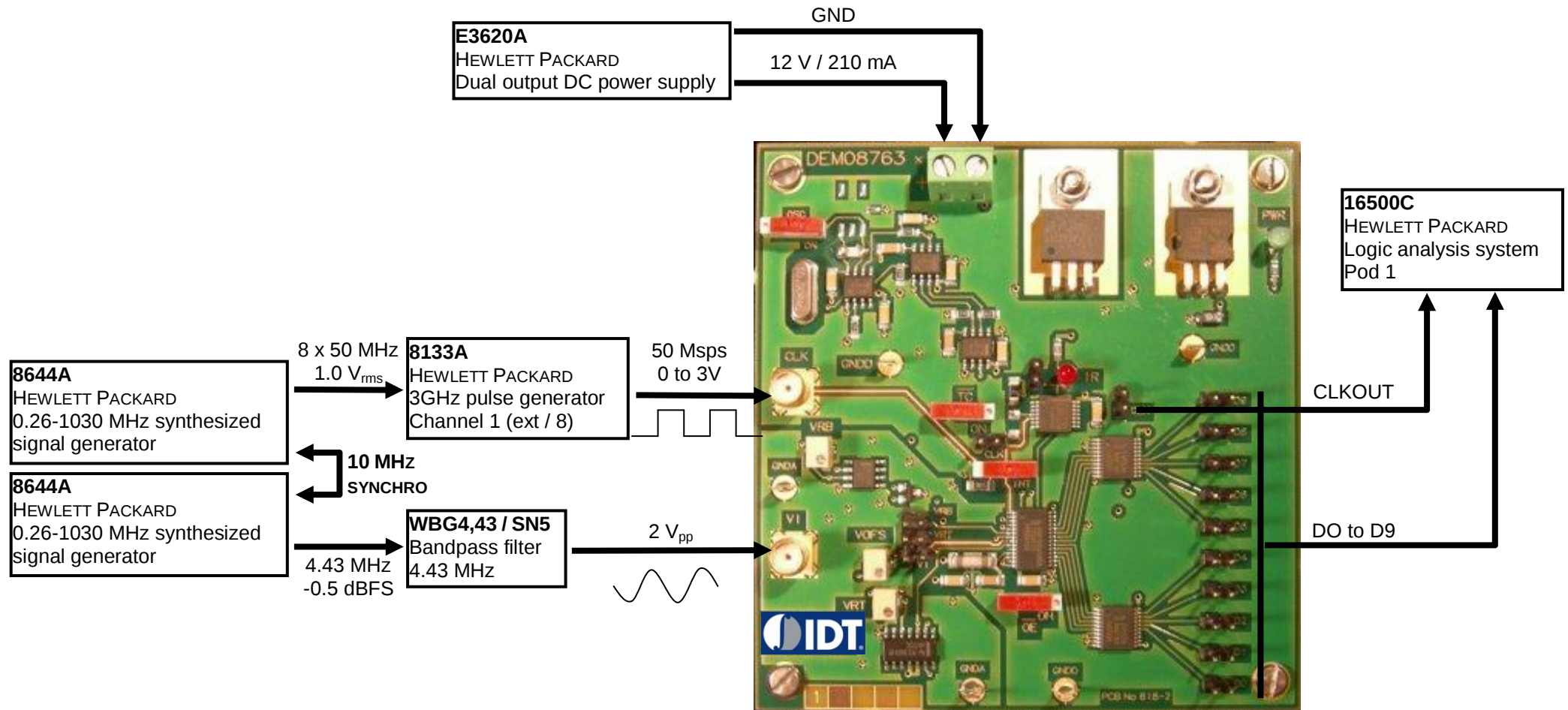


Fig 2. ADC1004S050 hardware setup