User Manual

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AB-050-FX3-U

V850ES/Fx3 Starter Board

Renesas Electronics
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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.

   The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.

   The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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- • Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- • Network requirements

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Preface

Readers This manual is intended for users who want to understand the functions of the concerned microcontrollers.

Purpose This manual presents the hardware manual for the concerned microcontrollers.

Organisation This system specification describes the following sections:

- Pin function
- CPU function
- Internal peripheral function

Module instances These microcontrollers may contain several instances of a dedicated module. In general the different instances of such modules are identified by the index “n”, where “n” counts from 0 to the number of instances minus one.

Legend Symbols and notation are used as follows:

• Weight in data notation:	Left is high order column, right is low order column
• Active low notation:	xxx (pin or signal name is over-scored) or /xxx (slash before signal name) or _xxx
• Memory map address:	High order at high stage and low order at low stage

Note Additional remark or tip

Caution Item deserving extra attention

Numeric notation

Binary:	xxxx or xxxB
Decimal:	xxxx
Hexadecimal	xxxxH or 0x xxxx

Numeric prefixes representing powers of 2 (address space, memory capacity):

K (kilo):	$2^{10} = 1024$
M (mega):	$2^{20} = 1024^2 = 1,048,576$
G (giga):	$2^{30} = 1024^3 = 1,073,741,824$

Register contents X, x = don’t care

Diagrams Block diagrams do not necessarily show the exact wiring in hardware but the functional structure. Timing diagrams are for functional explanation purposes only, without any relevance to the real hardware implementation.

How to Use This Manual

(1) Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual. The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the xxx/xx Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	xxx/xx Group Datasheet	R01DSxxxxEJxxxx
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description. Note: Refer to the application notes for details on using peripheral functions.	xxx/xx User's manual for Hardware	This User's manual
User's manual for Software	Description of CPU instruction set	xxx/xx Series User's manual for Software	R01USxxxxEJxxxx
Application Note	Information on using peripheral functions and application examples. Sample programs. Information on writing programs in assembly language and C.	Available from Renesas Electronics Web site.	
Renesas Technical Update	Product specifications, updates on documents, etc.		

(2) List of Abbreviations and Acronyms

Table of Contents

Chapter 1 Introduction

The AB-050-FX3-U is designed as a simple and easy to use Starter Board to support users with the first steps when starting with the Fx3-Series family.

The Starter Board is prepared to hold a V850ES/FK3 device (uPD70F3385). As the largest device of the Fx3-Series the FK3 offers the complete range of all Fx3 peripherals. Therefore software development for all other Fx3-Series devices is possible as well. Due to the software compatibility between the different family members porting of SW from FK3 to smaller devices is possible with only minimum efforts.

Mounting other members of the Fx3-Series on the board also is possible, at the cost of manual replacement of components and rewiring of signals.

With the NWire Debug interface and the Flash Programming interface for the RENESAS PG-FP4 Flash Programmer the standard RENESAS programming interfaces are directly available.

To enable further application development the board features drivers for five high speed CAN interfaces, eight RS-232 interfaces and eight LIN bus interfaces.

With on-board voltage regulator and reset generator a simple external DC power supply is sufficient to operate the board.

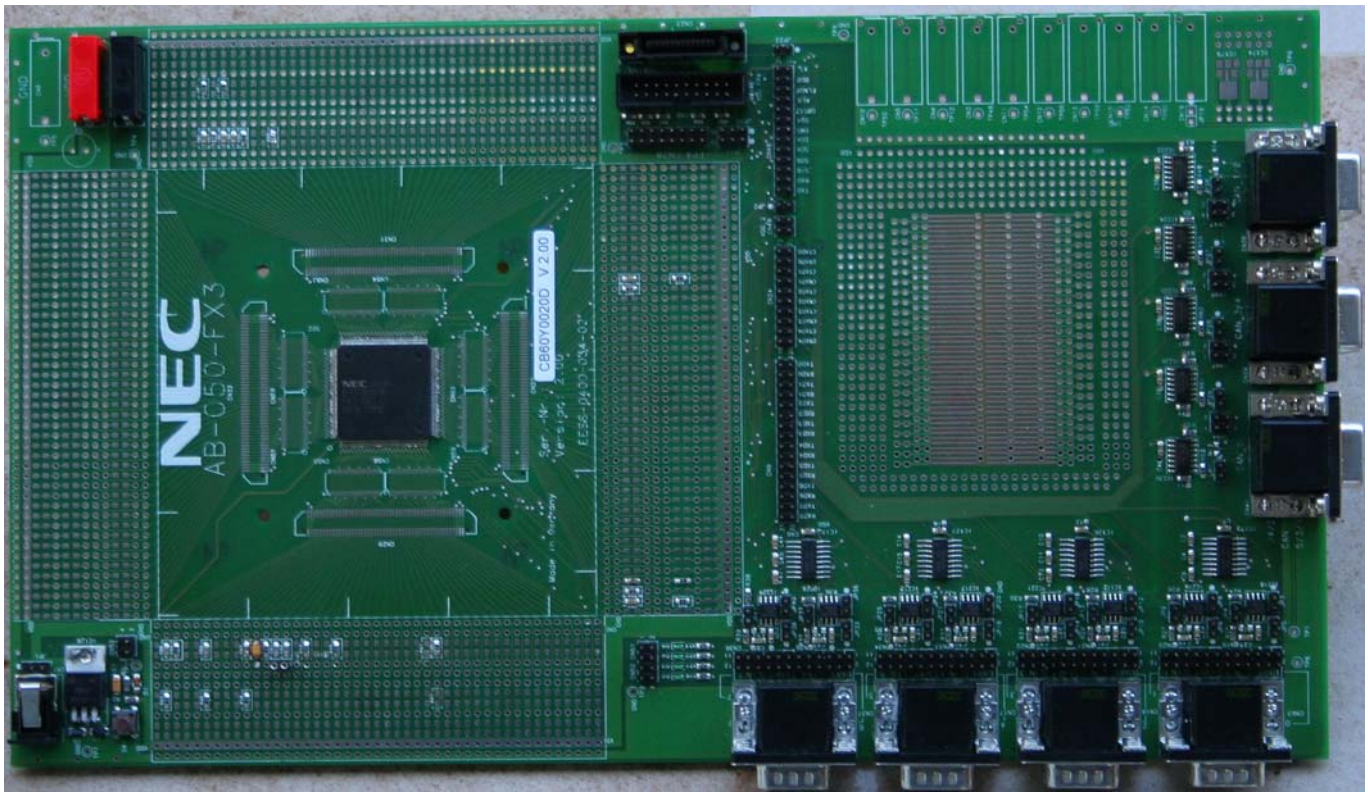


Figure 1 AB-050-FX3-U with FK3 Device

Chapter 2 Board description

2.1 Overview

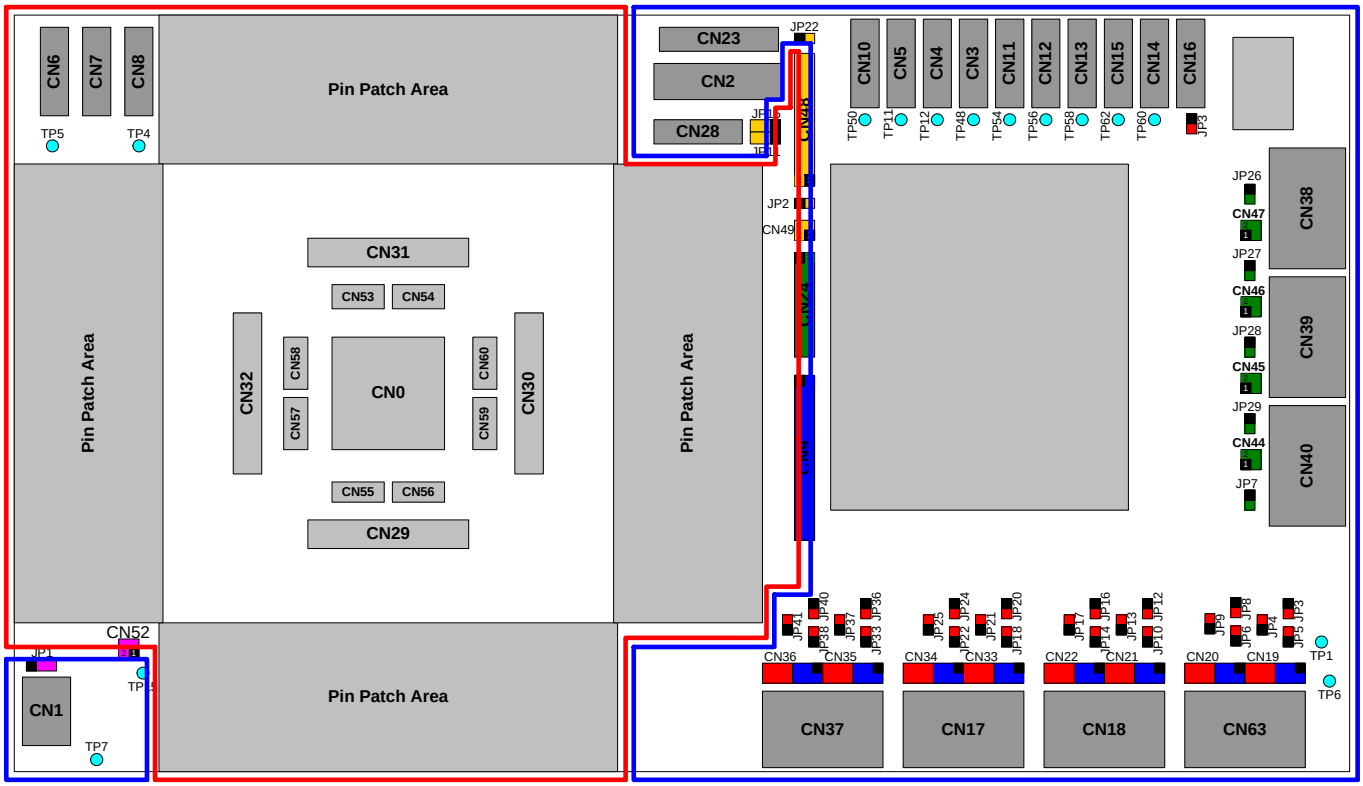


Figure 2-1 Board overview

Basically the board is divided into two areas, an ‘Electrical Area’ and a ‘Functional Area’.

In Figure 2-1 the Electrical Area is surrounded in by a red line and the Functional Area is surrounded by a blue line.

2.1.1 Electrical Area

In the center of the Electrical Area a 180 pin SMD pad field is located that any of the F-Series devices can be assembled to.
On each side of the Device Pad Field a Pin Patch Area is located. In this patch area access is given to each pin of the device

- VDD
- VSS

Further more SMD and through hole components can directly be soldered onto the Pin Patch Area to allow simple networks to be easily built up.

The circuitry available at each pin inside the Pin Patch Area is described in the figure below:

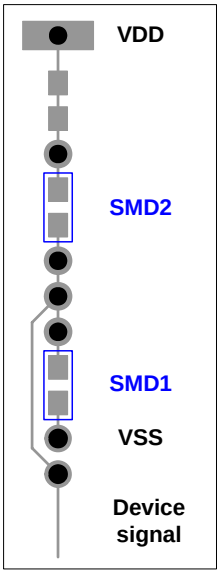


Figure 2-2 Pin Patch Area

A component assembled to the SMD1 field will therefore be connected between the device pin and VSS.

A component assembled to the SMD2 field will be connected between the device pin and VCC.

2.1.2 Functional Area

The Functional Area holds the drivers for RS-232, LIN bus and CAN. Additionally other patch areas are available as well to directly assemble LEDs, PowerDrivers and connectors to the board.

Note:

For detailed information about the operation of the used RS-232, LIN bus and CAN drivers refer to the related datasheets of those devices.

2.1.3 Connecting both areas

The Electrical and Functional Areas are not connected to one another except by a common VSS plane. Nevertheless by use of Jumpers a signal connection between the Electrical Area and the Functional Area is possible.

The following signals are available on the related jumper fields:

Signal	Jumper
_Reset	CN52
VDD	CN49
Flash programming (PG-FP4)	CN48 JP2
NWIRE	CN48
UARTDn (n=0..7)	CN9
CANn (n=0..4)	CN24

Table 2-1 Overview of functional signals

2.2 Reset

A simple Reset Generator using analog circuitry is available.

To connect the on-board Reset generator to the FK3 device close CN52 3-4.

If an external Reset signal shall be connected to the board the following setup must be used:

- Use TP15 to physically connect the external reset signal.
- Close CN52 1-2 to connect the external reset signal to the FK3 device.
- Open CN52 3-4 to disconnect the onboard Reset circuitry from the device.

2.3 NWire connection

The NWire debug cable from a RENESAS Debug Tool (e.g. MiniCube) can be connected to CN2.

Additionally a KEL connector (CN23) is available to connect third party NWire Debug Tools.

The following jumpers on CN48 must be closed in order to physically connect the NWire signals from CN2 to the corresponding pins of the FK3 device:

Signal	CN48 Pin number
SCK	9 – 10
DCK	11 – 12
DMS	13 – 14
DDI	15 – 16
DRST	17 – 18
RES	19 – 20
FLMD0	21 – 22
DDO	23 – 24

Table 2-2 CN48 – Nwire

Additionally JP2 must be closed.

2.4 PG-FP4 connection

The programming cable of the PG-FP4 Flash programmer can be connected to CN28.

To program the device via the CSI interface the following jumpers must be closed:

Connector	Pin number
JP15	2 – 3
JP11	2 – 3
CN48	5 – 6 7 – 8

Table 2-3 FP4 (CSI) Jumpers

To program the device via the UART interface the following jumpers must be closed:

Connector	Pin number
JP15	1 – 2
JP11	1 – 2
CN48	1 – 2 3 – 4

Table 2-4 FP4 (UART) Jumpers

For Flash programming using the PG-FP4 device power can either be supplied by the PG-FP4 or by the AB-050-FX3.

- For PG-FP4 power supply open JP2.
- For AB-050-FJ3 power supply close JP2.

If the clock supply for PG-FP4 programming is not on board, close CN48 Pins 25-26 to supply the clock from PG-FP4.

2.5 RS-232 / LIN

Close CN49 1 – 2 and 3 – 4 to supply power to RS-232 / LIN bus drivers.

For the LIN bus drivers additionally a VBAT voltage must be supplied. This voltage must be in a range of 5V to 12V.

For the exact specification refer to the Datasheet of the LIN Drivers.

To supply VBAT to the board use either of the two connections:

- Use TP1
- Close JP19 and use Cn16

Close the following jumpers on CN9 to physically connect the UARTD signals from the Electrical Area to the Functional Area.

Signal		CN9 Pin #
UARTD0	TXD0	1 – 2
	RXD0	3 – 4
UARTD1	TXD1	5 – 6
	RXD1	7 – 8
UARTD2	TXD2	9 – 10
	RXD2	11 – 12
UARTD3	TXD3	13 – 14
	RXD3	15 – 16
UARTD4	TXD4	17 – 18
	RXD4	19 – 20
UARTD5	TXD5	21 – 22
	RXD5	23 – 24
UARTD7	TXD6	25 – 26
	RXD6	27 – 28

UARTD6	TXD7	29 – 30
	RXD7	31 – 32

Table 2-5 UARTDn signal jumpers

To connect the RS-232 / LIN bus driver signals to the RS-232 / LIN bus connecters close the following jumpers:

Signal		Connector	Pin #
UARTD0	TXD0	CN19	1 – 2
	RXD0		3 – 4
	GND		5 – 6
UARTD1	TXD1	CN20	1 – 2
	RXD1		3 – 4
	GND		5 – 6
UARTD2	TXD2	CN21	1 – 2
	RXD2		3 – 4
	GND		5 – 6
UARTD3	TXD3	CN22	1 – 2
	RXD3		3 – 4
	GND		5 – 6
UARTD4	TXD4	CN33	1 – 2
	RXD4		3 – 4
	GND		5 – 6
UARTD5	TXD5	CN34	1 – 2
	RXD5		3 – 4
	GND		5 – 6
UARTD6	TXD6	CN35	1 – 2
	RXD6		3 – 4
	GND		5 – 6
UARTD7	TXD7	CN36	1 – 2
	RXD7		3 – 4
	GND		5 – 6

Table 2-6 RS-232 signal jumpers

To connect the LIN bus driver signals to the related RS-232/LIN bus connector close the following jumpers:

Signal		Connector	Pin #
LIN0	12V	CN19	7 – 8
	LIN		9 – 10
	GND		11 – 12
LIN1	12V	CN20	7 – 8
	LIN		9 – 10
	GND		11 – 12
LIN2	12V	CN21	7 – 8
	LIN		9 – 10
	GND		11 – 12
LIN3	12V	CN22	7 – 8
	LIN		9 – 10
	GND		11 – 12
LIN4	12V	CN33	7 – 8
	LIN		9 – 10
	GND		11 – 12
LIN5	12V	CN34	7 – 8
	LIN		9 – 10
	GND		11 – 12
LIN6	12V	CN35	7 – 8
	LIN		9 – 10
	GND		11 – 12
LIN7	12V	CN36	7 – 8
	LIN		9 – 10
	GND		11 – 12

Table 2-7 LIN bus signal jumpers

To enable the LIN drivers (IC218, IC219, IC172, IC221, IC217, IC223, IC228, IC229) the NSLP pin of the drivers must be pulled high. To do so a Jumper is available to connect the pin to VDD.

LIN channel	NSLP Jumper
0	JP3
1	JP8
2	JP12
3	JP16
4	JP20
5	JP24
6	JP40
7	JP36

The RxD pin of the LIN driver (pin #1) is an open drain output. The necessary pull-up resistor in order to interface to the Fx3 device is not assembled on the board. To enable operation of the RxD signal

- either connect an appropriate pull up resister to the related RxD input pin of the LIN channel, or
- enable the internal Pull-Up resistors available in the Fx3 devices for each LIN input pin.

The corresponding input pin for each RxD pin can be found in Table 6-11.

For additional information on the LIN driver refer to its User's Manual / Datasheet.

Caution:	**The RXD reception output pin of the LIN driver (e.g. IC218 pin1) and the RxD reception output pin of the UART driver (e.g. IC173 pin 12) are physically connected to the same pin on connector CN9 (e.g. CN9 pin 4).** **Therefore** - **when using the LIN driver lift the connected UART driver RxD output pin from the PCB.** - **when using the UART driver place the connected LIN driver in standby mode or lift the LIN driver RxD output pin from the board.**

2.6 CAN

Close CN49 1 – 2 and 3 – 4 to supply power to the CAN drivers.

Close the following jumpers to physically connect the devices CAN signals to the CAN interface drivers located on the Functional Area of the board:

Signal		CN24 Pin #
CAN0	CTXD0	1 – 2
	CRXD0	3 – 4
CAN1	CTXD1	5 – 6
	CRXD1	7 – 8
CAN2	CTXD2	9 – 10
	CRXD2	11 – 12
CAN3	CTXD3	13 – 14
	CRXD3	15 – 16

Table 2-8 CAN signal jumpers

Chapter 3 Mounting the FK3 device on the board

The AB-050-FX3-U boards is shipped with a mounted V850ES/FK3 device. Nevertheless, if mounting of another V850ES/FK3 device is required at a later time the following guideline is supplied:
To mount a FK3 device on the AB-050-FX3-U place the package in the top right corner of the SMD area.
As the FK3 with 176 pins is placed on an SMD area with 180 pins 4 pads will not be used. Due to the alignment of the device in the top right corner two pads in the lowest line and two pads in the left most line remain empty. Therefore align pin 1 of the device with pin 2 of the SMD pad area.

For details see Figure 3-1 and Figure 3-2.

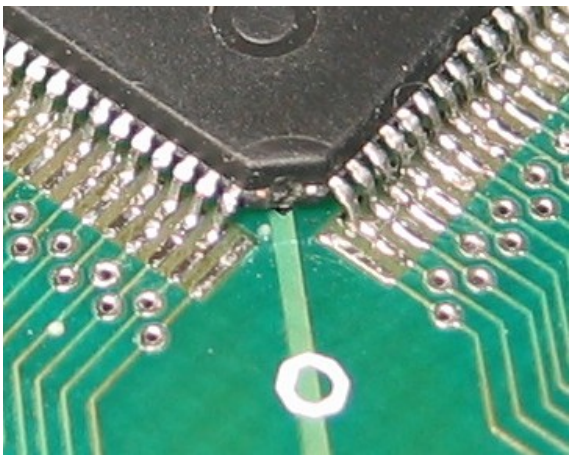


Figure 3-1 FK3 device mounting (1)

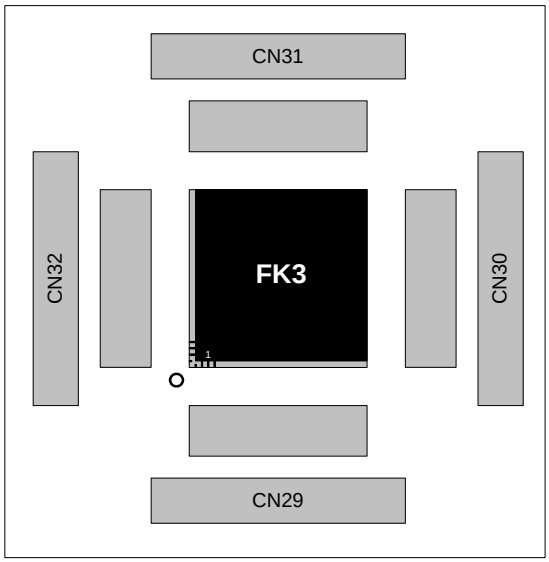


Figure 3-2 FK3 device mounting (2)

Chapter 4 Connecting the Power Supply

Power can be supplied to the board either

- by directly supplying the device operating voltage, or
- via the onboard 7805 type voltage regulator.

Direct voltage supply:
A direct supply of the device operating voltage can either be implied by using CN7 to connect VCC (typical +5V for Fx3 devices) and CN8 to connect VSS (0V), or by using CN1.

As the supplied voltage is directly connected to the device the input voltage must not exceed the specified power supply voltage range of the assembled device.

Close JP1 1-2 when directly supplying the devices voltage.

Voltage regulator supply:
Use CN1 to supply a stabilized voltage of 6V - 12V to the board. The on board 7805 type regulator will generate the 5V supply of the board.

Close JP1 2-3 when using the on board voltage regulator.

Caution:	**On CN1 the inner pin connects to VSS and the outer pin connects to VCC.**

Applying a voltage to the device outside the specified device operating voltage range may damage the device!

Chapter 5 UART / LIN CAN DSUB connectors

To physically connect the Starter Board to other UART / LIN / CAN devices DSUB type connectors are available..

5.1 UART / LIN connectors

To interface the AB-050-FX3-U board to external to UART / LIN devices a 9 pin male D-SUB connector is supplied for each of the eight available UART / LIN interfaces.

The signal layout of the UART/LIN DSUB connector can be seen in Table 5-1.

Male D-SUB, 9pin	Function
1	n/c
6	n/c
2	RS-232 TxD
7	LIN
3	RS-232 Rxd or GND
8	n/c
4	n/c
9	+12V
5	GND

Table 5-1 UART / LIN DSUB connectors

Figure 5-1 displays the assignment of each DSUB connector to its related peripheral:

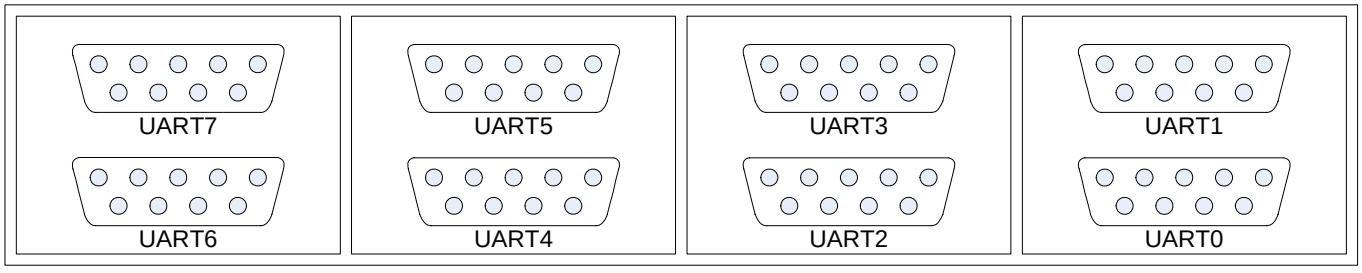


Figure 5-1 UART / LIN DSUB connectors

5.2 CAN connectors

To interface the AB-050-FX3-U board to external CAN devices a 9 pin female D-SUB connector is supplied for each of the five available CAN interfaces.

The pin functions of the CAN DSUB connectors can be seen in Table 5-2.

Female D-SUB, 9pin	Function
1	n/c
6	GND
2	CANL
7	CANH
3	GND (if jumpered)
8	n/c
4	n/c
9	n/c
5	n/c

Table 5-2 CAN DSUB connectors

Figure 5-2 displays the assignment of each DSUB connector to its related peripheral:

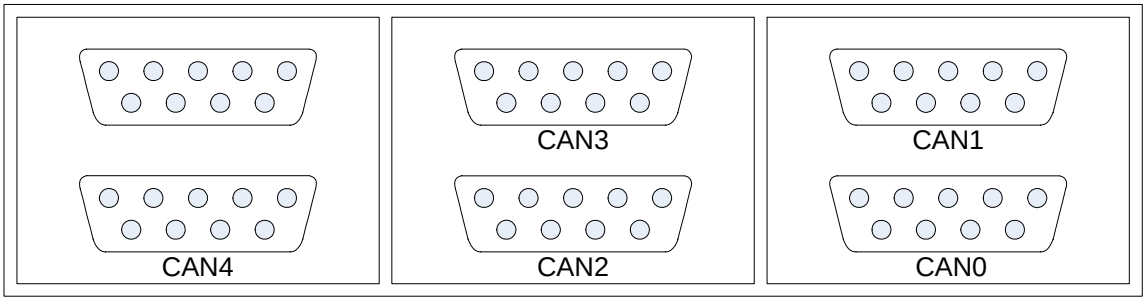


Figure 5-2 CAN DSUB connector

Chapter 6 Mounting other Fx3 devices on the board

Even though the AB-050-FX3-U is prepared for operation of the FK3 device also other devices of the Fx3-Line can be mounted on the board.

Besides mounting the new device to the board

- the components in the Pin Patch Area must be replaced according to the pin layout of the new device and
- the signals between the device pins and the jumpers connecting the Electrical Area and the Functional Area must wired manually.

Therefore the following changes must be applied:

6.1 Mounting devices

First the device must be mounted to the PCB. The alignment of the different Fx3-family devices is explained below.

6.1.1 Mounting a FE3 device

To mount a FE3 device on the AB-050-FX3-U place the package in the lower left corner of the SMD area but do not use the two pins most in the corner. Place pin 1 of the device on pin 2 of the SMD area.

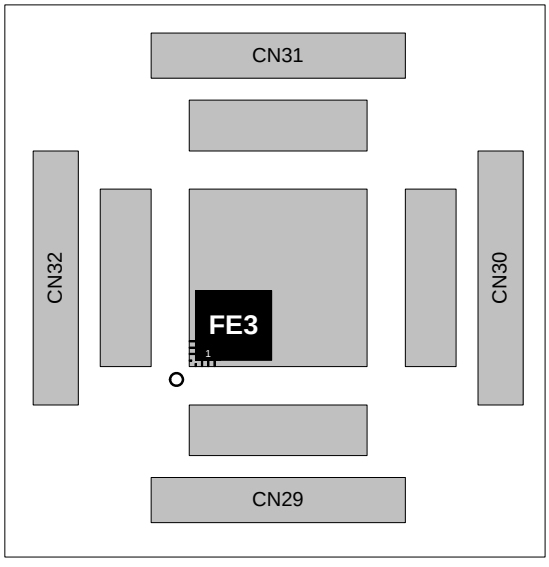


Figure 6-1 Mounting a FE3 device

6.1.2 Mounting a FF3 device

To mount a FF3 device on the AB-050-FX3-U place the package in the lower left corner of the SMD area but do not use the two pins most in the corner. Place pin 1 of the device on pin 2 of the SMD area.

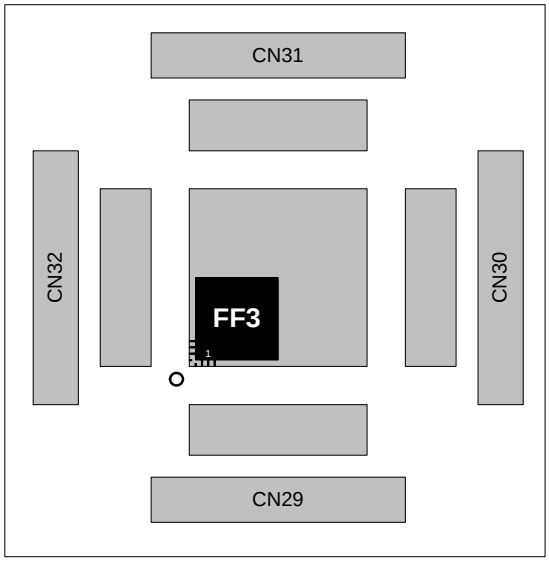


Figure 6-2 Mounting a FF3 device

6.1.3 Mounting a FG3 device

To mount a FF3 device on the AB-050-FX3-U place the package in the lower left corner of the SMD area. Place pin 1 of the device on pin 1 of the SMD area.

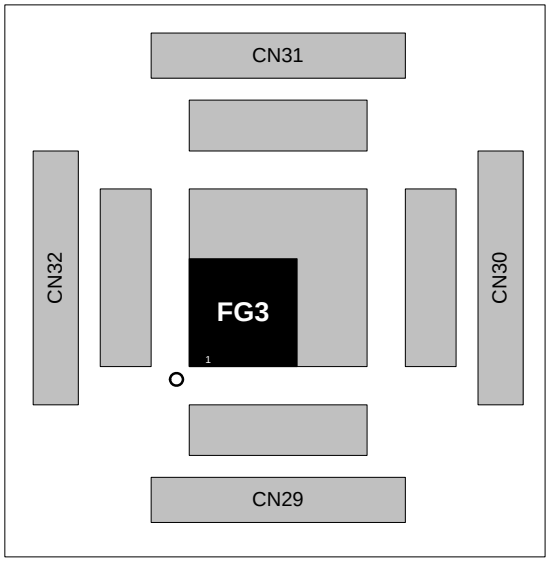


Figure 6-3 Mounting a FG3 device

6.1.4 Mounting a FJ3 device

To mount a FJ3 device on the AB-050-FX3-U place the package in the lower left corner of the SMD area. Place pin 1 of the device on pin 1 of the SMD area.

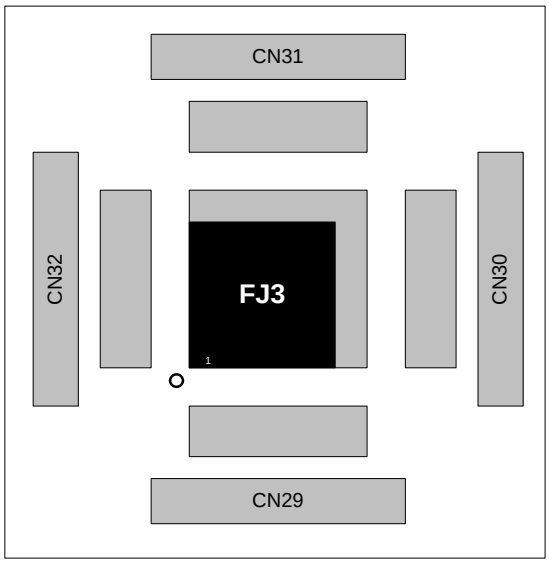


Figure 6-4 Mounting a FJ3 device

6.2 Pin connection

6.2.1 Power supply pins

Connect the devices power supply pins to the related power lines using the available SMD pads in the Pin Patch Areas.

Refer to the Fx3 User's Manual and Table 6-1 for the location of the VDD and VSS pins on the different devices.

Connect the VDD and VSS pins in the Pin Patch Areas like this:

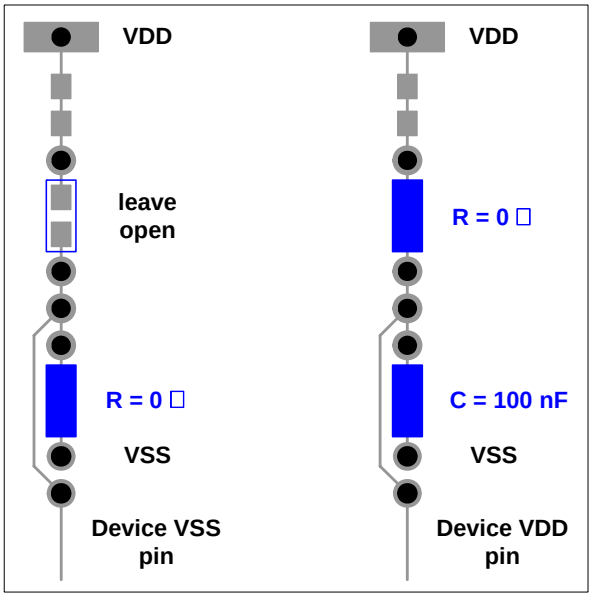


Figure 6-5 Device power supply

To connect the devices VSS pins to the VSS lane of the board place a 0 Ohm resistor on the SMD1 pad.

Signal	Fx3 pinning				
	FE3	**FF3**	**FG3**	**FJ3**	**FK3**
VSS	6	11	11	11	11
VSS1	n/a	n/a	n/a	n/a	124
AVSS	2	2	2	2	2
AVSS1	n/a	n/a	n/a	n/a	46
EVSS	32	30	33	33	28
	n/a	n/a	n/a	n/a	76
BVSS	n/a	n/a	69	103	127

Table 6-1 VSS signal connection

To connect the devices VDD pins to the VDD lane of the board place a 0 Ohm resistor on the SMD2 pad and place a 100 nF buffering capacitor on the SMD1 pad.

Signal	Fx3 pinning				
	FE3	**FF3**	**FG3**	**FJ3**	**FK3**
VDD	4	9	9	9	9
VDD1	n/a	n/a	n/a	n/a	126
AVREF0	1	1	1	1	1
AVREF1	n/a	n/a	n/a	n/a	45
EVDD	33	31	34	34	47
	n/a	n/a	5	5	5
	n/a	n/a	n/a	n/a	77
BVDD	n/a	n/a	70	104	128

Table 6-2 VDD signal connection

6.2.2 REGC pin

A buffering capacitor between the devices REGC pin(s) and VSS should be placed. Assemble the capacitor to the SMD1 pad field.

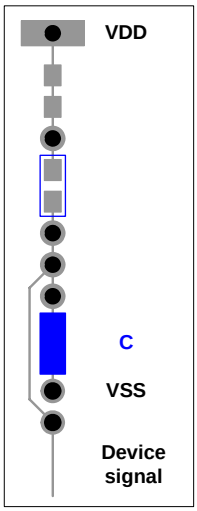


Figure 6-6 REGC pin components

Refer to the Fx3 User's Manual and Table 6-3 for the location of the RECC pin on the different devices.

Signal	Fx3 pinning				
	FE3	**FF3**	**FG3**	**FJ3**	**FK3**
REGC	5	10	10	10	10
REGC1	n/a	n/a	n/a	n/a	125

Table 6-3 REGC signal connection

6.2.3 X1, X2 pins

An external oscillator can be connected to the X1 and X2 pins of the device. Connect the oscillator between the X1 and X2 pins and place a small capacitor on the SMD1 areas of those pins.

For size of the capacitor refer to the oscillator manufacturer specification / recommendation.

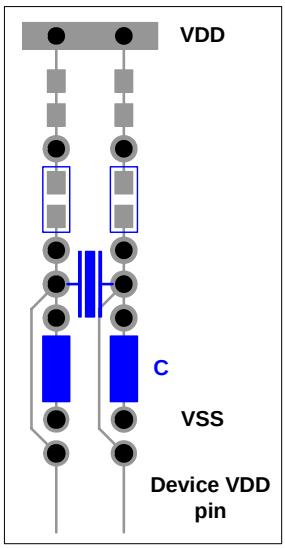


Figure 6-7 X1, X2 pin components

Refer to the Fx3 User's Manual and Table 6-4 for the location of the X1 and X2 pins on the different devices.

Signal	Fx3 pinning				
	FE3	**FF3**	**FG3**	**FJ3**	**FK3**
X1	7	12	12	12	12
X2	8	13	13	13	13

Table 6-4 X1, X2 signal connection

6.2.4 XT1, FLMD0

A pull-down resistor should be connected to input pins XT1 and FLMD0.

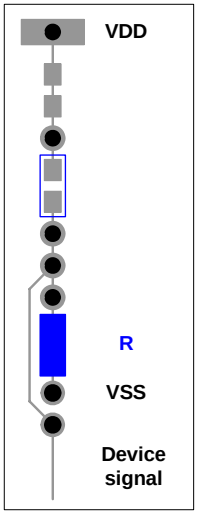


Figure 6-8 Pins with Pull-Down

Refer to the Fx3 User's Manual and Table 6-5 for the location of the XT1 and FLMD0 pins on the different devices.

Signal	Fx3 pinning				
	FE3	**FF3**	**FG3**	**FJ3**	**FK3**
XT1	10	15	15	15	15
FLMD0	3	8	8	8	8

Table 6-5 XT1, FLMD0 signal connection

6.3 Functional pin connection

As the routing of the functional signals (Reset, UARTDn, CANn, NWIRE and FP4) between the device SMD pad area and the Jumpers connecting the Electrical Area and Functional Area is based on the FK3 device, the routing of those signals for other Fx3 devices must be place manually.

To do so, connect a wire between the device pin (e.g. from one of the through holes in the Pin Patch areas) and the functional side of the related signal jumper.

Caution:	**Do not close the related Jumpers of any of the newly routed signals as this can lead to a direct connection between different device pins.**
	Be aware that no further disconnection by the use of jumpers between the Electrical Area and Functional Area is possible after wiring the signals for other than FK3 devices.

6.3.1 Jumper overview

The location of all jumpers located on the board can be seen in the Figure 6-9.

Pin 1 of each Jumper field is marked with a black square.

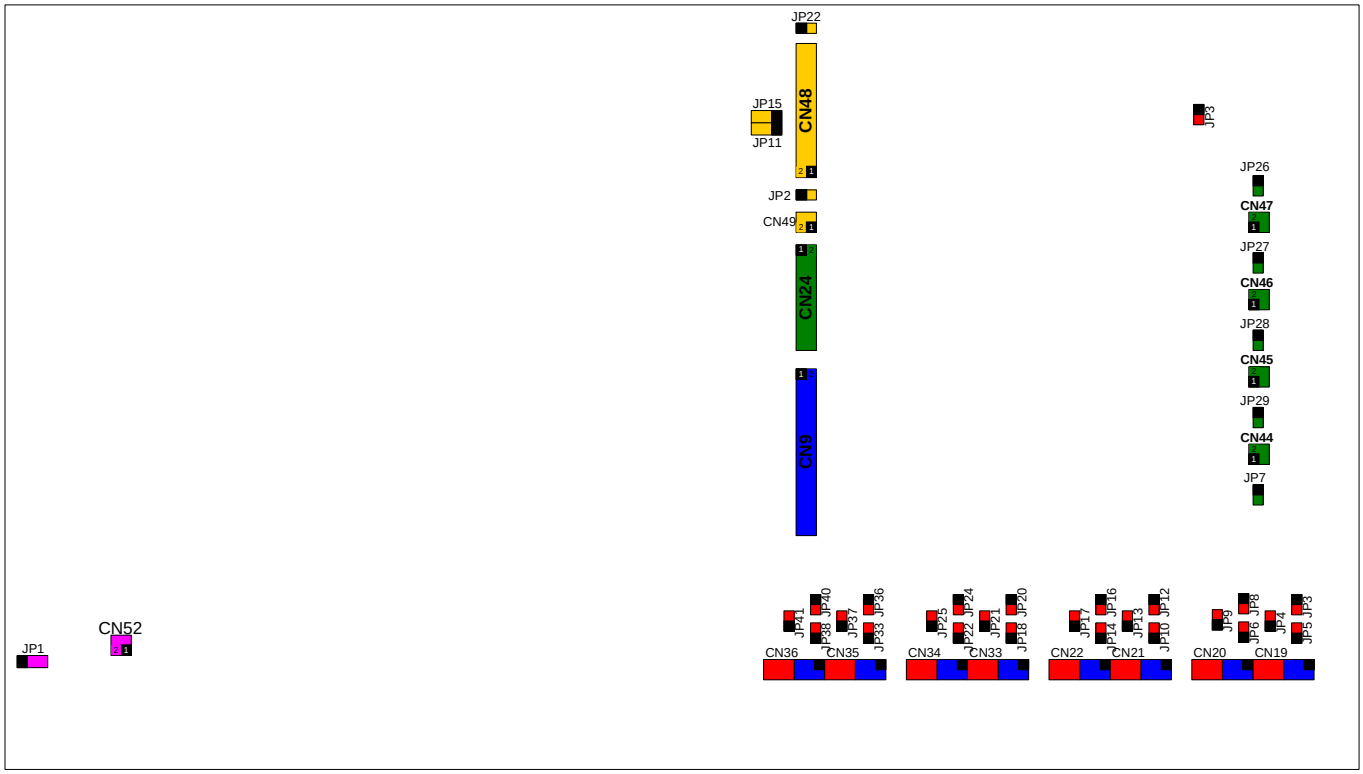


Figure 6-9 Jumpers location

The different jumper groups are highlighted in different colours according to their related functionality:

Jumper colour	Related functionality
Yellow	NWire Debug interface and Flash programming interface
Green	CAN interface signals
Blue	RS-232 interface signals
Red	LIN bus interface signals
Magenta	Power supply and Reset

Table 6-6 Colours of Jumper functionality

6.3.2 Testpoints

The available Test Points can be seen in

Figure 6-10 Test Point location

6.3.3 Reset signal

To connect the RESET signal place a wire according to the table below:

Signal	Fx3 pin number					CN52 pin number
	FE3	**FF3**	**FG3**	**FJ3**	**FK3**	
Reset	9	14	14	14	14	4

Table 6-7 Reset signal connection

6.3.4 NWIRE signals

To connect the NWIRE signals place wires according to the table below:

Signal	Fx3 pin number					CN48 pin number
	FE3	**FF3**	**FG3**	**FJ3**	**FK3**	
DCK	34	36	41	41	60	11
DMS	35	37	42	42	61	13
DDI	30	34	39	39	58	15
DRSTZ	17	17	20	20	21	17
RESET	9	14	14	14	14	19
FLMD0	3	8	8	8	8	21
DDO	31	35	40	40	59	23

Table 6-8 NWire interface signals

6.3.5 Flash Programming interface

To connect the Flash Programming signals place wires according to the table below:

Signal	Fx3 pin number					CN48 Pin number
	FE3	**FF3**	**FG3**	**FJ3**	**FK3**	
TxD	22	22	25	25	26	1
RxD	23	23	26	26	47	3
SIB	19	19	22	22	23	5
SOB	20	20	23	23	24	7
SCK	21	21	24	24	25	9

Table 6-9 Flash programming jumper settings

6.3.6 CAN interface

To connect the CAN interface signals place wires according to the table below:

Signal	Fx3 pin number					CN24 Pin number
	FE3	**FF3**	**FG3**	**FJ3**	**FK3**	
CTXD0	25 (*)	25 (*)	28 (*)	28 (*)	49 (*)	2
	18	18	21	21	22	
CRXD0	26 (*)	26 (*)	29 (*)	29 (*)	50 (*)	4
	16	7	19	19	20	
CTXD1	n/a	n/a	31	31	52	6
CRXD1	n/a	n/a	32	32	53	8
CTXD2	n/a	n/a	n/a	67 (*)	48 (*)	10
	n/a	n/a	n/a	71	92	
CRXD2	n/a	n/a	n/a	68 (*)	49 (*)	12
	n/a	n/a	n/a	72	93	
CTXD3	n/a	n/a	n/a	50	69	14
CRXD3	n/a	n/a	n/a	51	70	16
CTXD4	n/a	n/a	n/a	n/a	104	18
CRXD4	n/a	n/a	n/a	n/a	105	20

Table 6-10 CAN jumper settings

(*) Compatible pinning to the corresponding Fx2 device.

6.3.7 UARTD interface

To connect the UARTD interface signal place wires according to the table below:

Signal	Fx3 pin number					CN9
	FE3	**FF3**	**FG3**	**FJ3**	**FK3**	
TxD0	22	22	25	25	26	5
RxD0	23	23	26	26	27	7
TxD1	36	38	43	61	82	1
RxD1	37	39	44	62	83	3
TxD2	n/a	n/a	35	54	28	9
RxD2	n/a	n/a	36	55	29	11
TxD3	n/a	n/a	23	60 (*) 23	81 (*) 24	13
RxD3	n/a	n/a	22	59 (*) 22	80 (*) 23	15
TxD4	n/a	n/a	58	76	97	17
RxD4	n/a	n/a	57	75	96	19
TxD5	n/a	n/a	n/a	73	94	21
RxD5	n/a	n/a	n/a	74	95	23
TxD6	n/a	n/a	n/a	n/a	64	25
RxD6	n/a	n/a	n/a	n/a	65	27
TxD7	n/a	n/a	n/a	n/a	78	29
RxD7	n/a	n/a	n/a	n/a	79	31

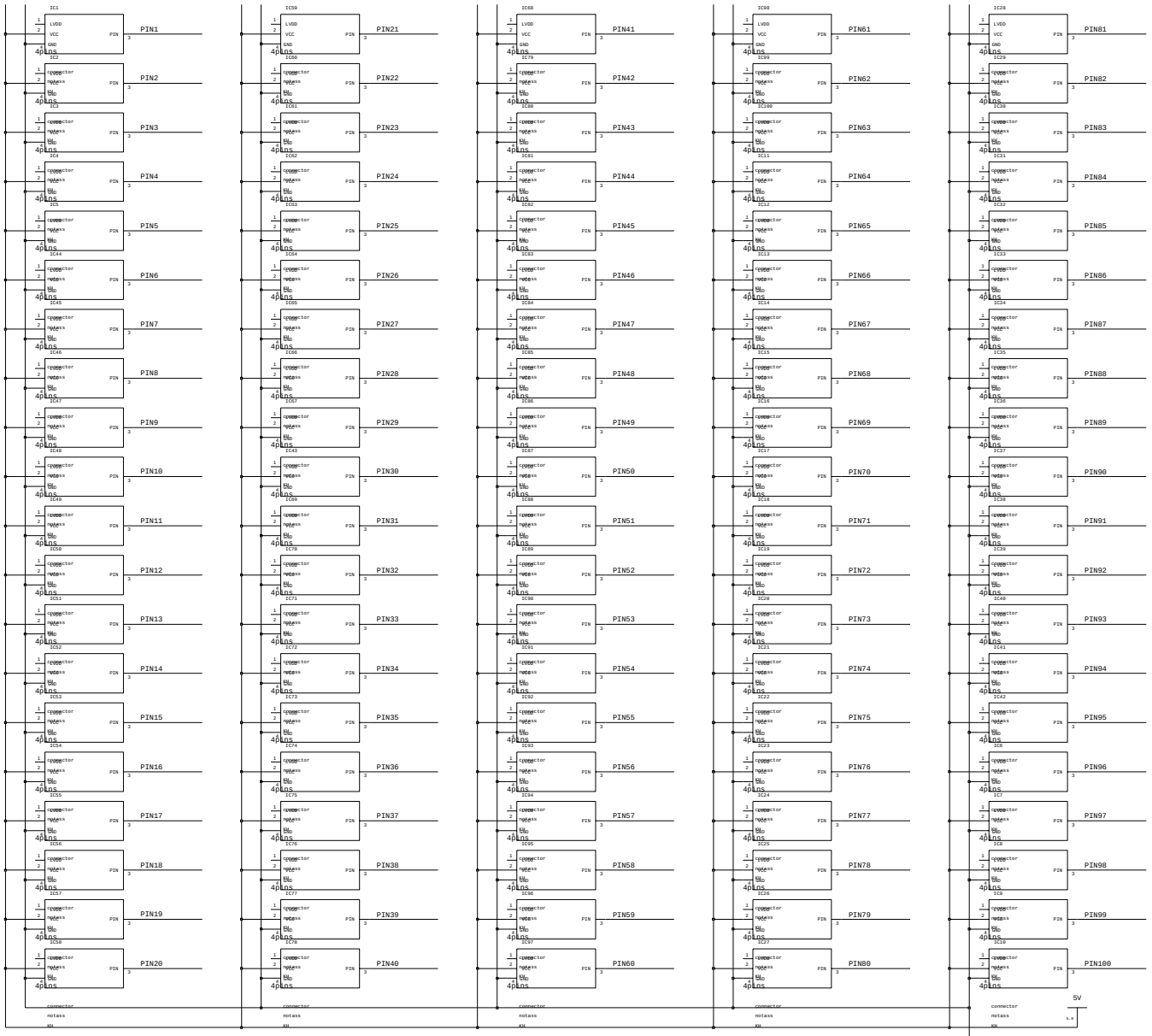
Table 6-11 UARTD jumper settings

(*) Compatible pinning to the corresponding Fx2 device.

Chapter 7 Revision History

Version	Chapter	Comment
1.0		Initial release
1.1	6.2.1 - 6.2.4 6.3.3 - 6.3.7	Added pin tables for the different devices
	All	Modified / expanded text
	6	Added chapter ‘Cautions’
	7	Added chapter ‘Revision History’
1.2	5	Added chapter for cable description
	2.5	Added information on LIN operation
2.0		Update for V2.0 revision of the AB-050-FX3 board.
2.1		Updated naming of board to AB-050-FX3-U
	2.5	Added Caution on UART / LIN driver usage
2.2	All	Update for new document number

Chapter 8 Schematic



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K.Hesse		S.Gupta

Spec.

Assembly drawing

AB-050-FK3

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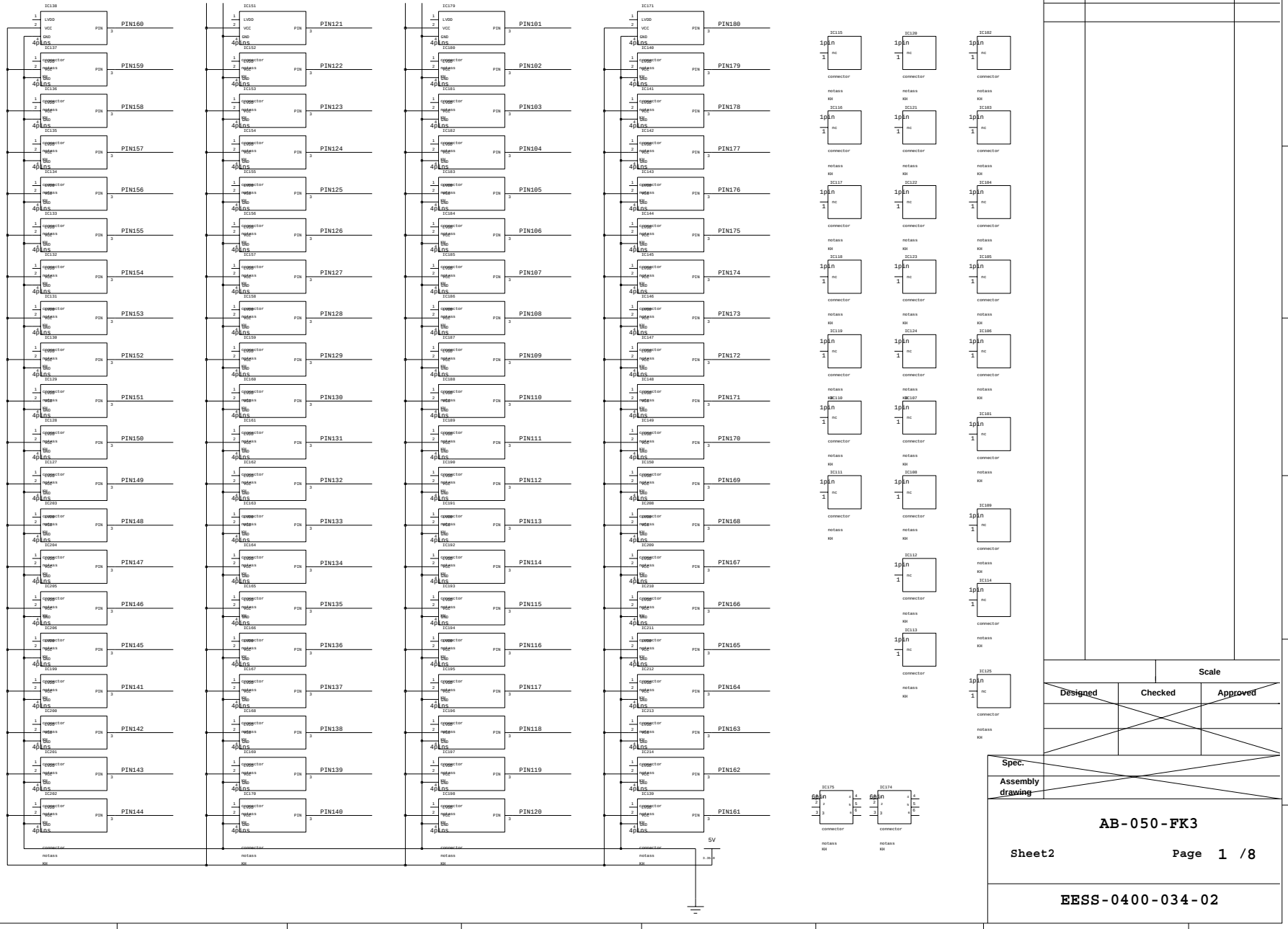
EESS-0400-034-02

Distribution:

Renesas Electronics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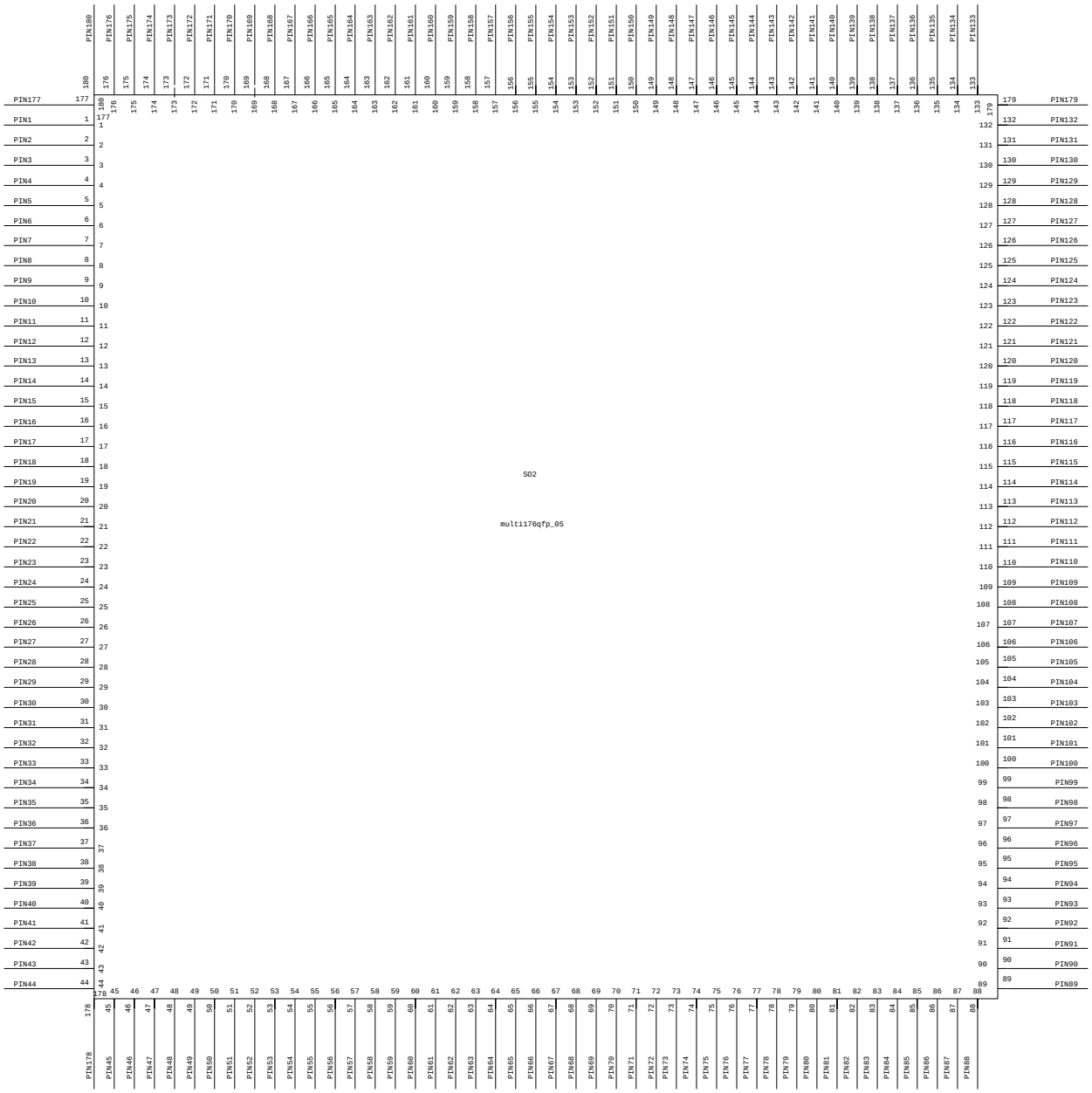

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AB-050-FK3

Multi QFP176 Footprint Page 2 /8

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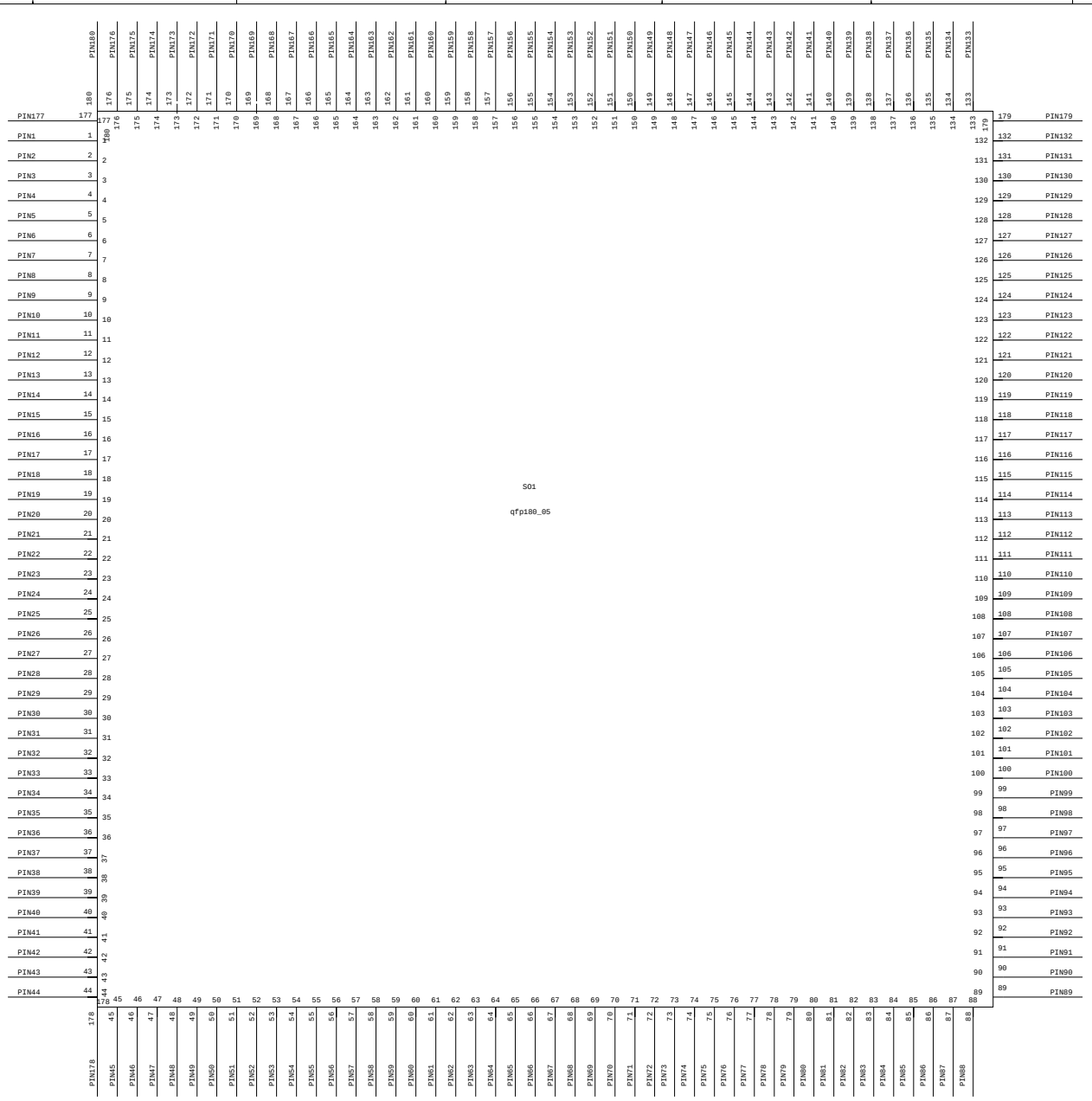

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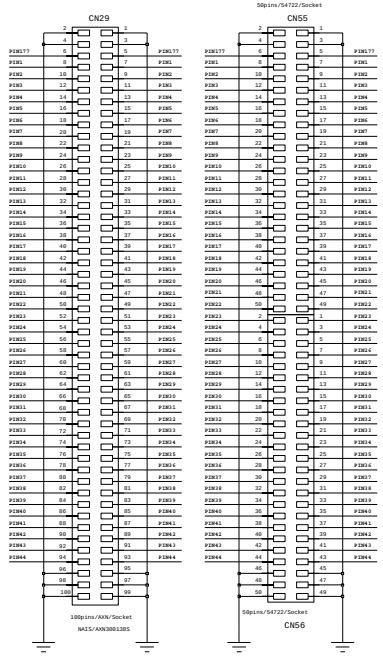

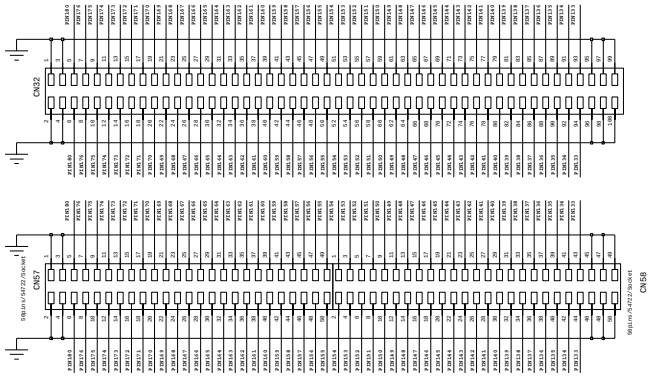

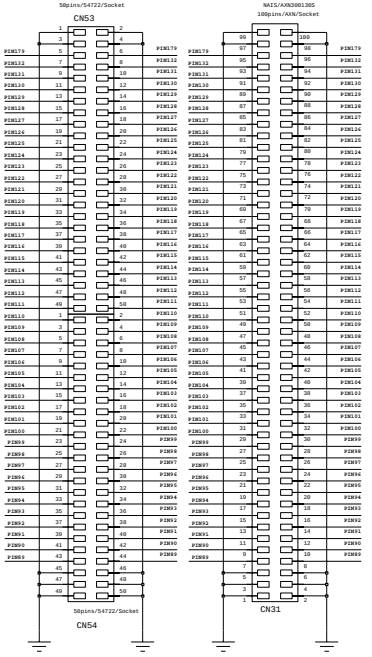

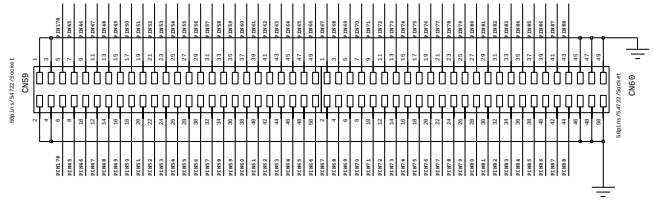

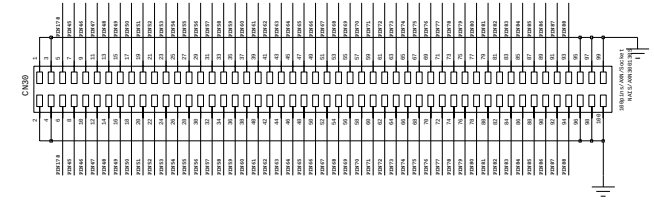

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AB-050-FK3
Board VER. 1.00

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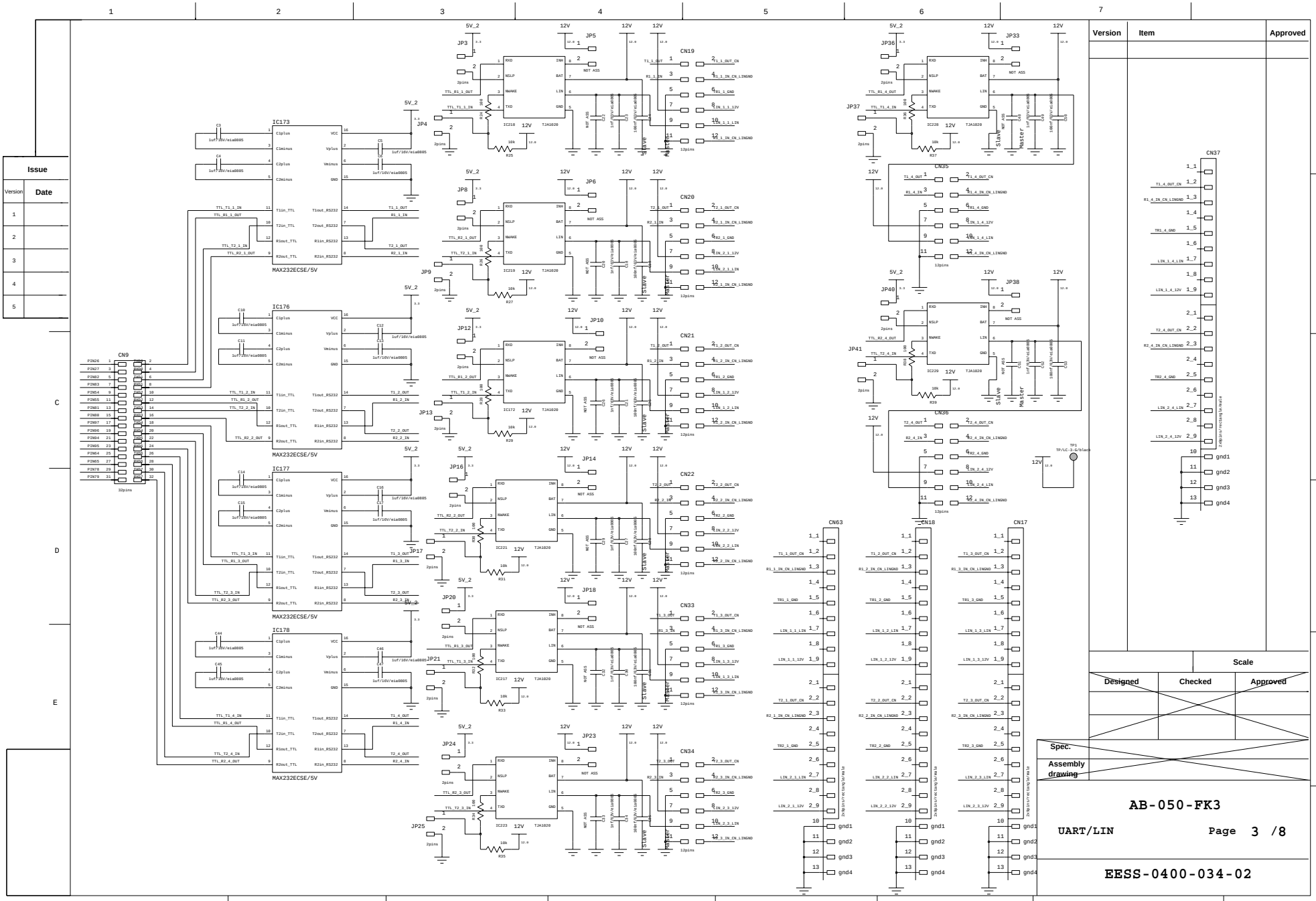
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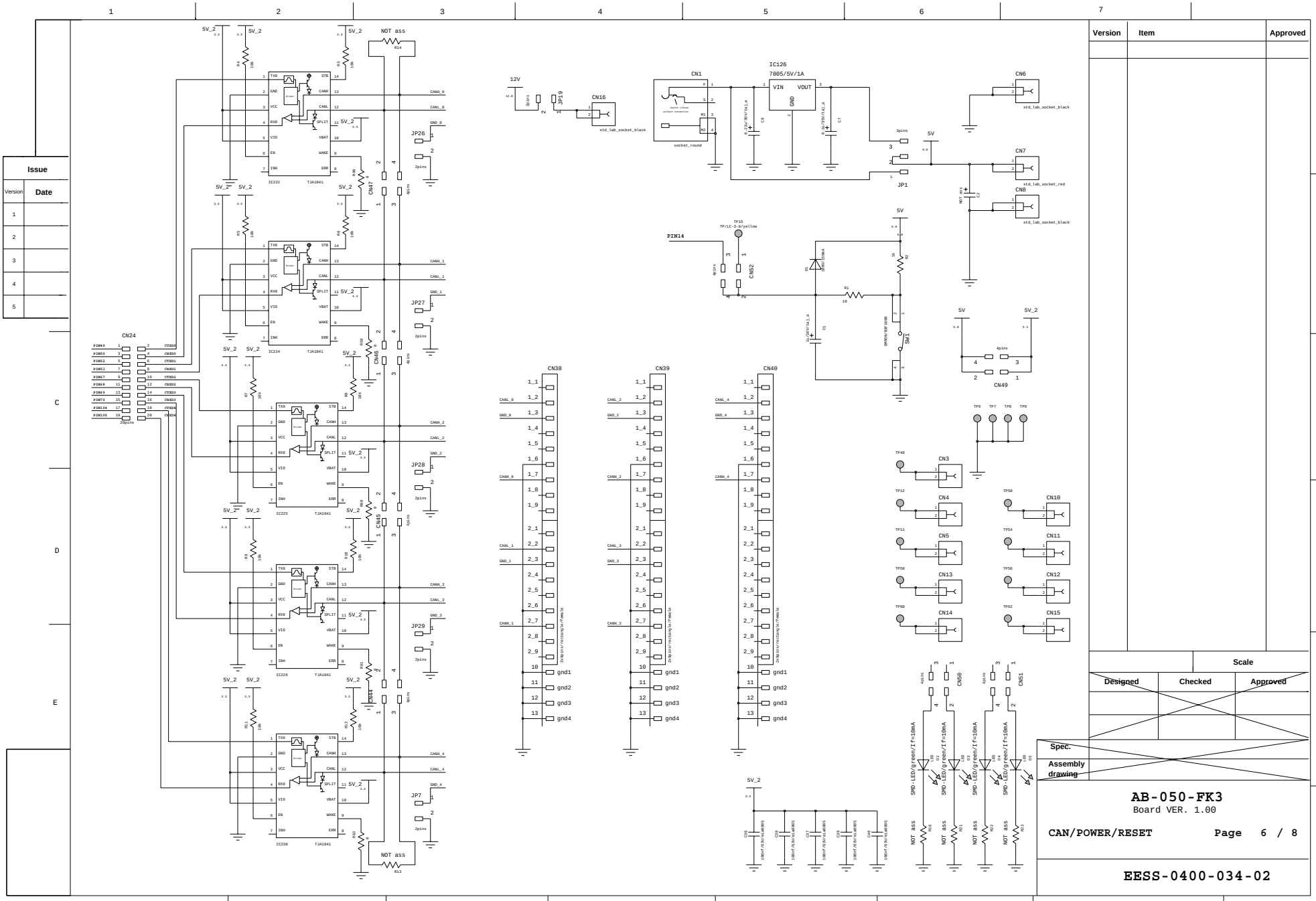
Renesas Electronics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Board VER. 1.00
CAN/POWER/RESET
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5V_2
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CN6
CN7
CN8
CN16
IC126
7805/5V/1A
VIN
VOUT
GND
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JP19
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JP28
JP29
JP7
CN24
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CN11
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CN15
CN50
CN51
SW1
IC222
IC224
IC225
IC226
IC230
TJA1041
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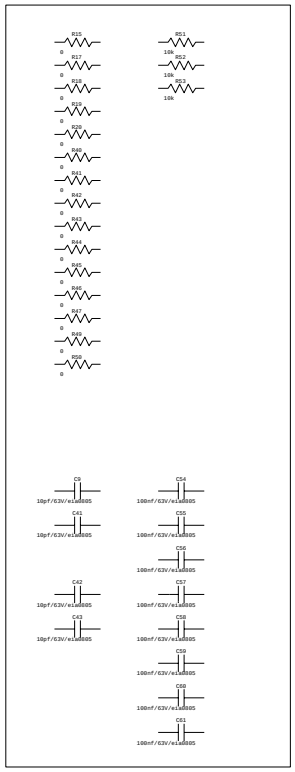
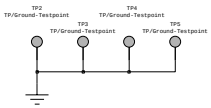
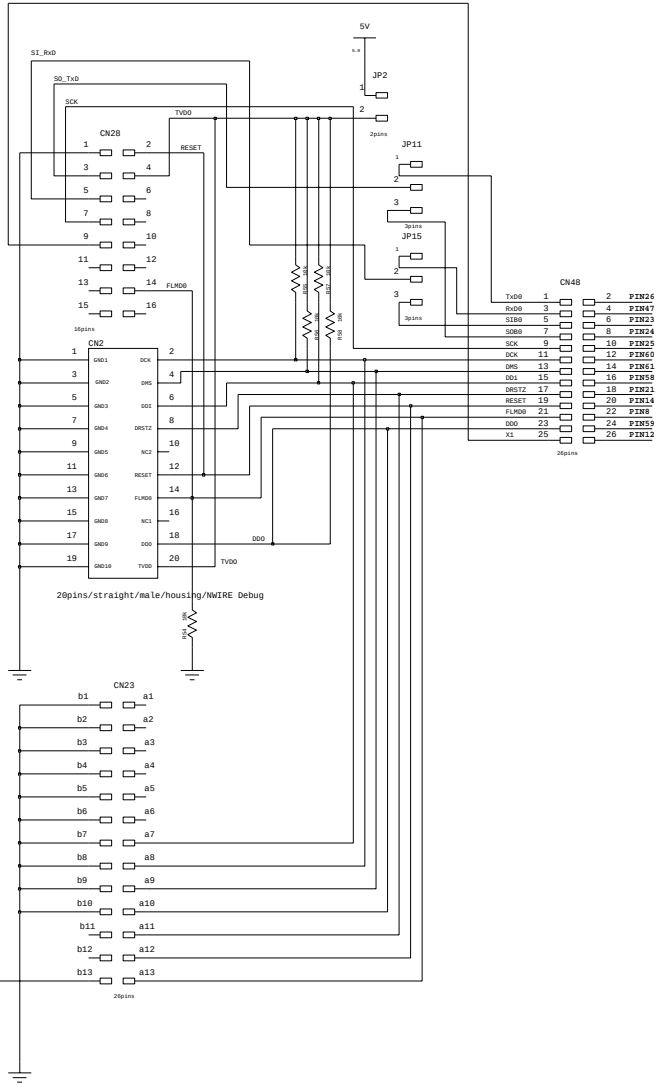
Components for Power/Ground connection.

FK3 Device







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Nwire/FP4 **Page /**

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