IDT™ 89EBPES24T6
Evaluation Board Manual

(Eval Board: 18-609-000)

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6024 Silver Creek Valley Road, San Jose, California 95138
Telephone: (800) 345-7015 • (408) 284-8200 • FAX: (408) 284-2775
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Table of Contents

Notes

Notes

List of Tables

Notes

Notes

List of Figures

Notes

Notes

Description of the EB24T6 Eval Board

Notes

Introduction

The 89HPES24T6 switch (also referred to as PES24T6 in this manual) is a member of IDT's PCI Express® standard (PCIe®) based line of products. It is a 6-port switch, with 4 serial lanes per port. Two x4 ports can be merged to form one x8 port. One upstream port is provided for connecting to the root complex (RC), and up to five downstream ports are available for connecting to PCIe endpoints or to another switch. More information on this device can be found in the 89HPES24T6 User Manual.

The 89EBPES24T6 Evaluation Board (also referred to as EB24T6 in this manual) provides an evaluation platform for the PES24T6 switch. It is also a cost effective way to add a PCIe downstream port (x4, x8) to an existing system with a limited number of PCIe downstream ports. The EB24T6 eval board is designed to function as an add-on card to be plugged into a x8 PCIe slot available on a motherboard hosting an appropriate root complex, microprocessor(s), and four downstream ports. The EB24T6 is a vehicle to test and evaluate the functionality of the PES24T6 chip. Customers can use this board to get a headstart on software development prior to the arrival of their own hardware. The EB24T6 is also used by IDT to reproduce system-level hardware or software issues reported by customers. Figure 1.1 illustrates the functional block diagram representing the main parts of the EB24T6 board.

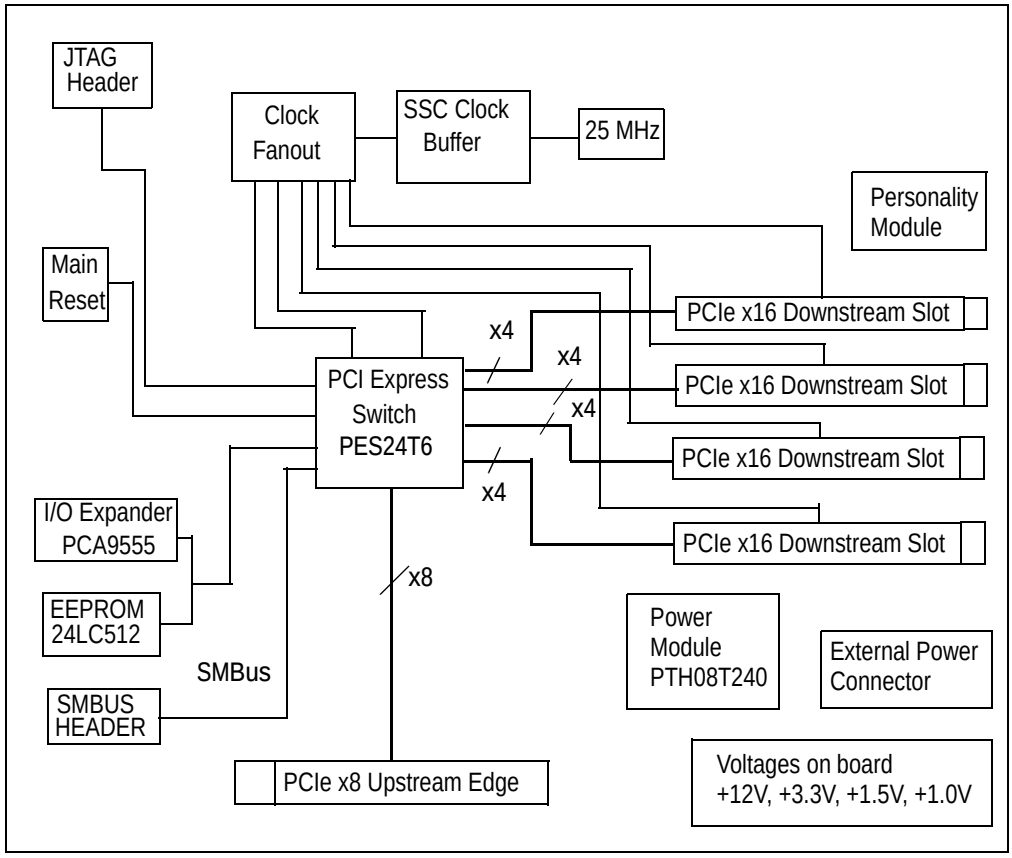


Figure 1.1 Function Block Diagram of the EB24T6 Eval Board

Notes

Board Features

Hardware

- PES24T6 PCIe 6 port switch
  - *Six x4 ports, 24 PCIe lanes*
  - *PCIe Base Specification Revision 1.1 compliant*
  - *12 GBps (96Gbps) aggregate switching capacity*
  - *Up to 2048 byte maximum Payload Size*
  - *Automatic lane reversal and polarity inversion supported on all lanes*
  - *Automatic per port link width negotiation to x8, x4, x2, x1*
  - *Load configuration from an optional serial EEPROM via SMBUS*
- Upstream, Downstream Port
  - *One edge connector on the upstream port, to be plugged into a slot with at least x8 capable on a host motherboard*
  - *Four slot connectors on the downstream ports, for PCIe endpoint add-on cards to be plugged in. These slot connectors are x16 mechanically but electronically connected as x4 or x8 only.*
  - *A personality module can be used to merge two (x4) ports into one (x8) port.*
- Numerous user selectable configurations set using onboard jumpers and DIP-switches
  - *Source of clock - host clock or onboard clock generator*
  - *Two clock rates and spread spectrum settings*
  - *Boot mode selection*
- SMBUS Slave Interface (4 pin header)
- SMBUS Master Interface connected to the Serial EEPROMs through I/O expander
- "Attention" button for each downstream port to initiate a hot swap event on each port
- Four pin connector for optional external power supply
- Push button for Warm Reset
- Several LEDs to display status, reset, power, "Attention", etc.
- One 10-pin JTAG connector (pitch 2.54 mm x 2.54 mm)

Software

There is no software or firmware executed on the board. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the PES24T6 within host systems running popular operating systems.

- Installation programs
  - *Operating Systems Supported: Windows2000, WindowsXP, Linux*
- GUI based application for Windows and Linux
  - *Allows users to view and modify registers in the PES24T6*
  - *Binary file generator for programming the serial EEPROMs attached to the SMBUS.*

Other

- A metal bracket is required to firmly hold in place three of the four endpoints plugged into the EB24T6 board.
- An external power supply may be required under some conditions.
- SMBUS cable may be required for certain evaluation exercises.
- SMA connectors are provided on the EB24T6 board for specific test points.

Notes

Revision History

October 18, 2006: Initial publication of board manual.

November 13, 2006: In Tables 2.7 and 2.8, changed references to MSMSDDR to MSMBADDR. In Table 2.8, changed P45MERGEN to Not Used.

Notes

Installation of the EB24T6 Eval Board

Notes

EB24T6 Installation

This chapter discusses the steps required to configure and install the EB24T6 evaluation board. All available DIP switches and jumper configurations are explained in detail.

The primary installation steps are:

1. Configure jumper/switch options suitable for the evaluation or application requirements.
2. Connect PCI Express endpoint cards to the downstream port PCIe slots on the evaluation board.
3. Insert the evaluation board into the host system (motherboard with root complex chipset).
4. Apply power to the host system.

The EB24T6 board is shipped with all jumpers and switches configured to their default settings. In most cases, the board does not require further modification or setup.

Hardware Description

The PES24T6 is a 24-lane, 6-port PCI Express® switch. It is a peripheral chip that performs PCI Express based switching with a feature set optimized for high performance applications such as servers and storage. It provides fan-out and switching functions between a PCI Express upstream port and 5 downstream ports or peer-to-peer switching between downstream ports.

The EB24T6 has four PCI Express downstream ports, accessible through four x16 connectors. One specific port is capable of negotiating a x1, x2, x4, or x8 link width and the remaining three ports are capable of negotiating a x1, x2, or x4 link width. All endpoint cards connected to the PES24T6 must support at least one of these link widths. A personality module can be used to provide a single x8 downstream port by merging two specific x4 ports (see section PCI Express Personality Module on page 2-16).

Basic requirements for the board to run are:

- Host system with a PCI Express root complex supporting x8 configuration through a PCI Express x8 slot. (If your host system does not offer a x8 slot, please contact ssdhelp@idt.com for alternative solutions.)
- x1, x2, x4, or x8 PCI Express Endpoint Cards.

Host System

The evaluation board cannot be operated as a standalone unit. A host system implementing a PCI Express root complex supporting x8 configuration through a PCI Express x8 slot is required to take full advantage of the PES24T6's capabilities. One such system is the SuperMicro X6DH8-G2 motherboard equipped with an Intel E7520 chipset which was introduced in 2004 to deploy dual-processor server chipset technology. The board has three PCI Express slots. All slots have x8 connectors, but only two are electronically connected for a x8 link width (J15 and J16). The remaining slots are electronically connected for a x4 link width configuration. Care must be taken to avoid using the EB24T6 in the x4 slot (J17). Figure 2.1 shows the proper connectors.

Notes

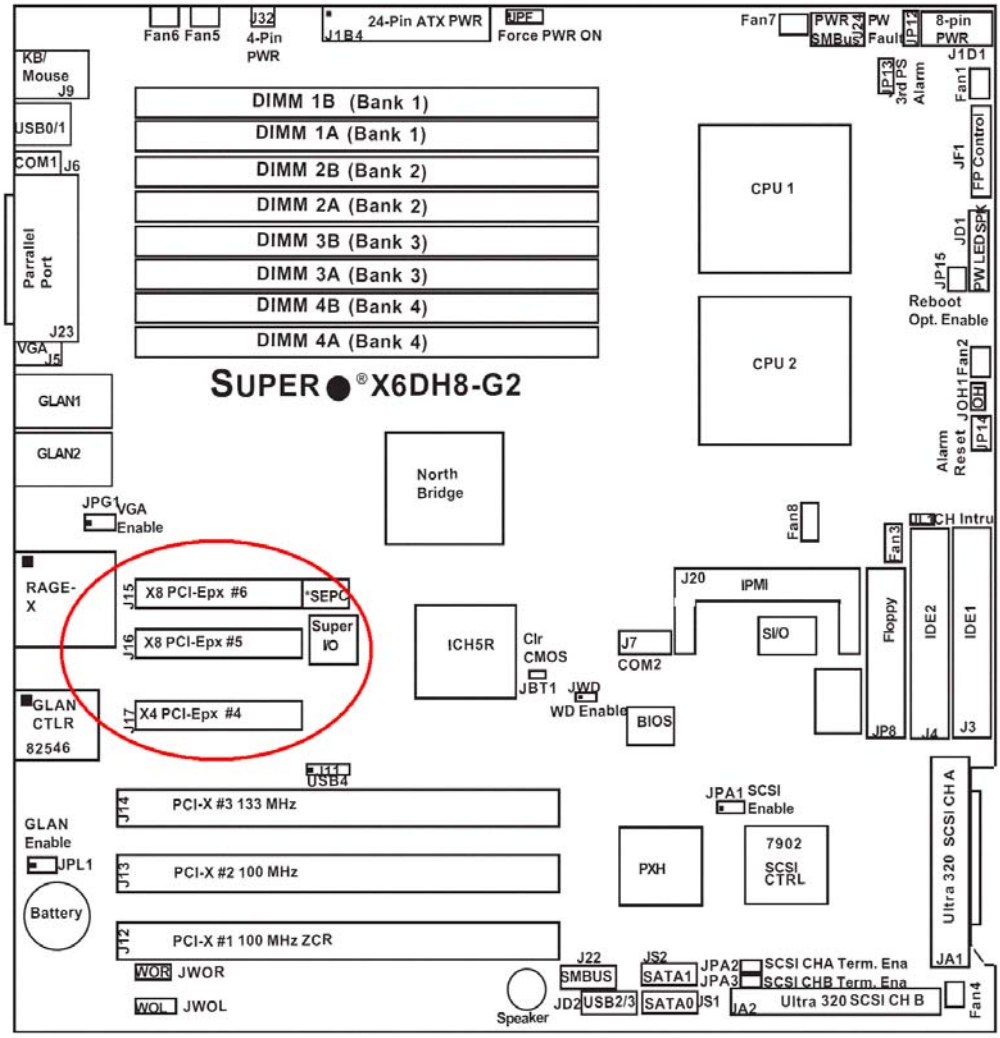


Figure 2.1 SuperMicro X6DH8-G2 Motherboard

Reference Clocks

The PES24T6 requires two differential reference clocks. The EB24T6 derives both of these clocks from a common source which is user-selectable. The common source can be either the host system's reference clock or the onboard clock generator. Selection is made by stuffing resistors described in Table 2.1.

Clock Configuration Stuffing Option	
Install	Clock Source
R36, R37	Onboard Reference Clock – Use onboard clock generator
R34, R35	Upstream Reference Clock – Host system provides clock (Default)

Table 2.1 Clock Source Selection

Notes

The source for the onboard clock is the ICS557-03 clock generator device (U8) connected to a 25MHz oscillator (Y1). When using the onboard clock generator, the EB24T6 allows selection between multiple clock rates and spread spectrum settings via DIP switches as described in Tables 2.2 and 2.3 respectively. Spread Spectrum technology reduces peak EMI emissions by modulating the frequency to spread the peak energy over a wider bandwidth.

Clock Frequency Switch - S2[2:1]		
S2[2]	S2[1]	Clock Frequency
OFF	OFF	Reserved
OFF	ON	125 MHz
ON	OFF	100 MHz (Default)
ON	ON	<Reserved>

Table 2.2 Clock Frequency Selection

Clock Spread Spectrum Switch - S2[4:3]		
S2[4]	S2[3]	Spread%
OFF	OFF	No Spread (Default)
OFF	ON	Down -0.75
ON	OFF	Down -0.50
ON	ON	Center ±0.25

Table 2.3 Clock Spread Spectrum Selection

If the Clock Spread Spectrum is used to modulate data rate, then both ports must use the same modulated clock source. Therefore, if your system uses SSC, the on-board clock generator must be disabled and the upstream reference clock should be used instead.

The output of the onboard clock generator is accessible through two SMA connectors located on the Evaluation Board. See Table 2.4. This can be used to connect a scope for probing or capturing purposes and cannot be used to drive the clock from an external source.

Onboard Reference Clock Output (Differential) – J3, J2	
J3	Positive Reference Clock
J2	Negative Reference Clock

Table 2.4 SMA Connectors - Onboard Reference Clock

Power Sources

The upstream port consists of port 0 and port 1. The EB24T6 and all downstream ports are powered from the upstream port slot power. If add-in cards require more power than the upstream slot can support, an external source is required to supply this extra power via an auxiliary 4-pin power connector on the board. Only downstream ports 2, 3, 4, and 5 can be powered by this external power source through jumpers W45, W46, and W47 (see Table 2.19). Note that on the schematic pages in Chapter 4, port 2 is also referred to as port D, port 3 as port E, port 4 as port C and port 5 as port B.

External Power Source

If necessary, external power is supplied to the EB24T6 board through a 4-pin auxiliary power connector attached to J1. The external power supply provides +12V to the EB24T6 as described in Table 2.5. The +5V is unused.

Notes

Pin	Signal
1	+12V
2	GND
3	GND
4	+5V

Table 2.5 External Power Connector - J1

PCI Express Serial Data Transmit Termination Voltage Converter

A DC-DC converter (U6) provides a 1.5V PCI Express serial data transmit termination voltage (shown as VTTPE or VPETVTT) to the PES24T6.

PCI Express Digital Power Voltage Converter

A separate DC-DC converter (U3) provides a 1.0V PCI Express digital power voltage (VDDPE) to the PES24T6.

PCI Express Analog Power Voltage Converter

A separate DC-DC converter (U7) provides a 1.0V PCI Express analog power voltage (shown as VDDAPE or VDDPEA) to the PES24T6.

Core Logic Voltage Converter

A separate DC-DC converter (U1) provides the 1.0V core voltage (VDDCORE) to the PES24T6.

3.3V I/O Power Module

A 12V to 3.3V power module (U5 or U26) provides the 3.3V I/O voltage (VDDIO) to the PES24T6.

Power-up Sequence

The power-up sequence must be as following:

1. VDDIO - 3.3V
2. VDDCORE, VDDAPE, VDDPE - 1.0V
3. VTTPE - 1.5V

When powering up, each voltage level must ramp up and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations between sequential valid power level requirements. To insure that the sequencing requirements are met, a 0.047µF is used at the SOFTSTART cap on the VTTPE's voltage converter (U6 pin 36) in the EB24T6.

Required Jumpers

To deliver power to the PES24T6 switch, the following jumpers must be shunted: W10 and W22—W25. These jumpers were implemented so that the power consumption of the PES24T6 can be measured.

Reset

The PES24T6 supports two types of reset mechanisms as described in the PCI Express specification:

- Fundamental Reset: This is a system-generated reset that propagates along the PCI Express tree through a single side-band signal PERST# which is connected to the Root Complex, the PES24T6, and the endpoints.
- Hot Reset: This is an In-band Reset, communicated downstream via a link from one device to another. Hot Reset may be initiated by software. This is further discussed in the 89HPES24T6 User Manual. The EB24T6 evaluation board provides seamless support for Hot Reset.

Notes

Fundamental Reset

There are two types of Fundamental Resets which may occur on the EB24T6 evaluation board:

- Cold Reset: During initial power-on, the onboard voltage monitor (TLC7733D) will assert the PCI Express Reset (PERSTN) input pin of the PES24T6.
- Warm Reset: This is triggered by hardware while the device is powered on. Warm Reset can be initiated by two methods:
  - Pressing a push-button switch (S1) located on EB24T6 board
  - The host system board IO Controller Hub asserting PERST# signal, which propagates through the PCIe upstream edge connector of the EB24T6. Note that one can bypass the onboard voltage monitor (TLC7733D) by moving the shunt from pin 1-2 to pin 2-3 (default) on W1.

Both events cause the onboard voltage monitor (TLC7733D) to assert the PCI Express Reset (PERSTN) input of the PES24T6 while power is on.

Downstream Reset

The PES24T6 provides a a choice of either a software-controlled reset for each downstream port through GPIO pins or a fundamental reset through PERST#. Selection is made by jumpers described in Table 2.6.

Port #	Jumper	Selection
5	W27	[1-2] Software controlled reset through GPIO10 [2-3] Fundamental reset PERST# (default)
4	W30	[1-2] Software controlled reset through GPIO1 [2-3] Fundamental reset PERST# (default)
2	W35	[1-2] Software controlled reset through GPIO0 [2-3] Fundamental reset PERST# (default)
3	W38	[1-2] Software controlled reset through GPIO9 [2-3] Fundamental reset PERST# (default)

Table 2.6 Downstream Reset Selection

Boot Configuration Vector

A boot configuration vector consisting of the signals listed in Table 2.7 is sampled by the PES24T6 during a fundamental reset (while PERSTN is active). The boot configuration vector defines the essential parameters for switch operation and is set using DIP switches S5 and S6 as defined in Table 2.8.

Notes

Signal	Description
CCLKDS	Common Clock Downstream. The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices. This pin is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be overridden by modifying the SCLK bit in the downstream port's PCIELSTS register. Default: 0x1
CCLKUS	Common Clock Upstream. The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This pin is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the P0_PCIELSTS register. Default: 0x1
MSMBSMODE	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 kHz. Default: 0x0
P01MERGEN	Port 0 and 1 Merge: When this pin is asserted (i.e. low), port 1 is merged with port 0 to form a single x8 port. Default: 0x0
P23MERGEN	Port 2 and 3 Merge: When this pin is asserted (i.e. low), port 2 is merged with port 3 to form a single x8 port. Default: 0x1
P45MERGEN	Port 4 and 5 Merge: When this pin is asserted (i.e. low), port 4 is merged with port 5 to form a single x8 port. Default: 0x1
RSTHALT	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, the PES24T6 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the P0_SWCTL register through the SMBus. The value may be overridden by modifying the RSTHALT bit in the P0_SWCTL register. Default: 0x0
SWMODE[3:0]	Switch Mode. These configuration pins determine the PES24T6 switch operating mode. Default: 0x1 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM-based initialization 0x2 through 0x4 - Reserved 0x5 - Global SerDes test mode 0x6 - Reserved 0x7 - PLL bypass test mode 0x8 through 0xF - Reserved
REFCLKM	PCI Express Reference Clock Mode Select. This signal selects the frequency of the reference clock input. Default: 0x0 0x0 - 100 MHz 0x1 - 125 MHz
MSMBADDR[2:0]	Master SMBus Address. These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded. Default: 0x0

Table 2.7 Boot Configuration Vector Signals

Signal	Description	Default
S6[1]	CCLKDS	OFF
S6[2]	CCLKUS	OFF
S6[3]	MSMBSMODE	ON

Table 2.8 Boot Configuration Vector Switches S5 & S6 (ON=0, OFF=1) (Part 1 of 2)

Notes

Signal	Description	Default
S6[4]	P01MERGEN	ON
S6[5]	P23MERGEN	OFF
S6[6]	Reserved	Must be OFF
S6[7]	Reserved	Must be OFF
S6[8]	RSTHALT	OFF
S5[1]	SWMODE[0]	OFF
S5[2]	SWMODE[1]	ON
S5[3]	SWMODE[2]	ON
S5[4]	SWMODE[3]	ON
S5[5]	REFCLKM	ON
S5[6]	MSMBADDR[0]	ON
S5[7]	MSMBADDR[1]	ON
S5[8]	MSMBADDR[2]	ON

Table 2.8 Boot Configuration Vector Switches S5 & S6 (ON=0, OFF=1) (Part 2 of 2)

SMBus Interfaces

The System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate. It is based on the principles of operation of I^2C. Implementation of the SMBus signals in the PCI Express connector is optional and may not be present on the host system. The SMBus interface consists of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins.

The PES24T6 contains two SMBus interfaces: a slave SMBus interface and a master SMBus interface. The slave SMBus interface allows a SMBus Master device (such as the Intel E7520) full access to all software-visible registers. The Master SMBus interface provides connection to the external serial EEPROMs used for initialization and the I/O expander used for hot-plug signals.

SMBus Slave Interface

On the PES24T6 board, the slave SMBus interface is accessible through the PCI Express edge connector as well as a 4-pin header as described in Table 2.9.

Note: The SMBus signals to the PCI Express edge connector is disabled by default. To enable them, place 0-ohm resistors at locations R202 and R203.

.

Slave SMBus Interface Connector J10	
Pin	Signal
1	N/C
2	SCL
3	GND
4	SDA

Table 2.9 Slave SMBus Interface Connector

A fixed slave SMBus address specified by the SSMBADDR[5,3:1] pins is used.

Notes

For a fixed address, the SMBus address of the PES24T6 slave interface is 0b1110111 by default and is configurable using jumpers W40, W41, W42, and W43 as described in Tables 2.10 and 2.11.

Slave Interface Address Configuration	
Address Bit	Signal
1	SSMBUSADDR[1]
2	SSMBUSADDR[2]
3	SSMBUSADDR[3]
4	0
5	SSMBUSADDR[5]
6	1
7	1

Table 2.10 SMBus Slave Interface Address Configuration

SMBUS Slave Interface Address Setting				
W40 SSMBADDR[5]	W41 SSMBADDR[3]	W42 SSMBADDR[2]	W43 SSMBADDR[1]	Slave Interface Bus Address
OFF	OFF	OFF	OFF	0b1110111 (Default)
OFF	OFF	OFF	ON	0b1110110
OFF	OFF	ON	OFF	0b1110101
OFF	OFF	ON	ON	0b1110100
OFF	ON	OFF	OFF	0b1110011
OFF	ON	OFF	ON	0b1110010
OFF	ON	ON	OFF	0b1110001
OFF	ON	ON	ON	0b1110000
ON	OFF	OFF	OFF	0b1100111
ON	OFF	OFF	ON	0b1100110
ON	OFF	ON	OFF	0b1100101
ON	OFF	ON	ON	0b1100100
ON	ON	OFF	OFF	0b1100011
ON	ON	OFF	ON	0b1100010
ON	ON	ON	OFF	0b1100001
ON	ON	ON	ON	0b1100000

Table 2.11 PES24T6 SMBus Slave Interface Address Setting

Notes

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. Initiation of any SMBus transaction other than those listed above produces undefined results. See the SMBus 2.0 specification for a detailed description of the following transactions:

- Byte and Word Write/Read
- Block Write/Read

SMBus Master Interface

Connected to the master SMBus interface are four 16-bit I/O Expanders (PCA9555) and a serial EEPROM (24LC512). Four I/O Expanders are used as the interface for the onboard hot-plug controllers (MIC2591B). The lower three bits of the bus address for the I/O Expander are configurable as described in Tables 2.12 through 2.15.

I/O Expander 0			
W4	W7	W11	Bus Address
ON	ON	ON	0b0100000 (Default)
ON	ON	OFF	0b0100001
ON	OFF	ON	0b0100010
ON	OFF	OFF	0b0100011
OFF	ON	ON	0b0100100
OFF	ON	OFF	0b0100101
OFF	OFF	ON	0b0100110
OFF	OFF	OFF	0b0100111

Table 2.12 I/O Expander 0 Bus Address

I/O Expander 1			
W2	W5	W8	Bus Address
ON	ON	OFF	0b0100001 (Default)
ON	ON	ON	0b0100000
ON	OFF	ON	0b0100010
ON	OFF	OFF	0b0100011
OFF	ON	ON	0b0100100
OFF	ON	OFF	0b0100101
OFF	OFF	ON	0b0100110
OFF	OFF	OFF	0b0100111

Table 2.13 I/O Expander 1 Bus Address

Notes

I/O Expander 2			
W3	W6	W9	Bus Address
ON	OFF	ON	0b0100010 (Default)
ON	ON	ON	0b0100000
ON	ON	OFF	0b0100001
ON	OFF	OFF	0b0100011
OFF	ON	ON	0b0100100
OFF	ON	OFF	0b0100101
OFF	OFF	ON	0b0100110
OFF	OFF	OFF	0b0100111

Table 2.14 I/O Expander 2 Bus Address

I/O Expander 4			
W31	w44	w29	Bus Address
OFF	ON	ON	0b0100100 (Default)
ON	ON	ON	0b0100000
ON	ON	OFF	0b0100001
ON	OFF	ON	0b0100010
ON	OFF	OFF	0b0100011
OFF	ON	OFF	0b0100101
OFF	OFF	ON	0b0100110
OFF	OFF	OFF	0b0100111

Table 2.15 I/O Expander 4 Bus Address

The bus address for the selected EEPROM device is **0b1000** by default and is configurable using W39 and the switch S5 as described in Table 2.16.

W39	S5[8]	S5[7]	S5[6]	Bus Address
OFF	OFF	OFF	OFF	0b0101 1111
OFF	OFF	OFF	ON	0b0101 1110
OFF	OFF	ON	OFF	0b0101 1101
OFF	OFF	ON	ON	0b0101 1100
OFF	ON	OFF	OFF	0b0101 1011
OFF	ON	OFF	ON	0b0101 1010

Table 2.16 EEPROM SMBus Address Setting

Notes

W39	S5[8]	S5[7]	S5[6]	Bus Address
OFF	ON	ON	OFF	0b0101 1001
OFF	ON	ON	ON	0b0101 1000
ON	ON	ON	ON	0b0101 0000 (Default)

Table 2.16 EEPROM SMBus Address Setting

JTAG Header

The PES24T6 provides a JTAG connector J4 for access to the PES24T6 JTAG interface. The connector is a 2.54 x 2.54 mm pitch male 10-pin connector. Refer to Table 2.17 for the JTAG Connector J4 pin out.

JTAG Connector J4					
Pin	Signal	Direction	Pin	Signal	Direction
1	/TRST - Test reset	Input	2	GND	—
3	TDI - Test data	Input	4	GND	—
5	TDO - Test data	Output	6	GND	—
7	TMS - Test mode select	Input	8	GND	—
9	TCK - Test clock	Input	10	GND	—

Table 2.17 JTAG Connector Pin Out

Attention Buttons

The PES24T6 features four attention buttons, shown in Table 2.18. Each button corresponds to a particular port and is used to initiate hot-swapping events.

Button	Description
S3	Port 1 Attention Button
S4	Port 6 Attention Button
S7	Port 7 Attention Button

Table 2.18 Attention Buttons

Notes

Miscellaneous Jumpers, Headers

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W45-W47	Header	1-2 Shunted	1-2: 12.0V source from Upstream Port (Default) 2-3: 12.0V source from external power connector
W49-W51	Header	Shunted	Bypass hot-plug controller - Enable REFCLK to downstream ports (Default)
W12	Header	Shunted	Disable EEPROM Write protect feature (Default)
W4, W7, W11 W2, W5, W8 W3, W6, W9 W31, W44, W29	Header	ON, ON, ON ON, ON, OFF ON, OFF, ON OFF, ON, ON	I/O Expander 0 Address[2:0]. Default to 0x0 I/O Expander 1 Address[2:0]. Default to 0x1 I/O Expander 2 Address[2:0]. Default to 0x2 I/O Expander 4 Address[2:0]. Default to 0x4
W13	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Port 7 (Default)
W14	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 1 (Default)
W17	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 6 (Default)
W16	Header	2-3 Shunted	2-3: Port 5, 3.3Vaux source from Upstream port (Default) 1-2: Port 5, 3.3Vaux source from hot-plug controller
W15	Header	2-3 Shunted	2-3: Port 1, 3.3Vaux source from Upstream port (Default) 1-2: Port 1, 3.3Vaux source from hot-plug controller
W20	Header	2-3 Shunted	2-3: Port 6, 3.3Vaux source from Upstream port (Default) 1-2: Port 6, 3.3Vaux source from hot-plug controller
W21	Header	2-3 Shunted	2-3: Port 1, +12V source base on W45-W47 (Default) 1-2: Port 1, +12V source from hot-plug controller
W28	Header	2-3 Shunted	2-3: Port 6, +12V source base on W45-W47 (Default) 1-2: Port 6, +12V source from hot-plug controller
W33	Header	2-3 Shunted	2-3: Port 7, +12V source base on W45-W47 (Default) 1-2: Port 7, +12V source from hot-plug controller
W26	Header	2-3 Shunted	2-3: Port 1, +3.3V source from upstream port (Default) 1-2: Port 1, +3.3V source from hot-plug controller
W32	Header	2-3 Shunted	2-3: Port 6, +3.3V source base on W45-W47 (Default) 1-2: Port 6, +3.3V source from hot-plug controller
W34	Header	2-3 Shunted	2-3: Port 7, +3.3V source base on W45-W47 (Default) 1-2: Port 7, +3.3V source from hot-plug controller

Table 2.19 Miscellaneous Jumpers, Headers

LEDs

There are several LED indicators on the EB24T6 which convey status feedback. A description of each is provided in Table 2.20.

Notes

Location	Color	Definition
DS11	Green	Port 5: Power-is-good indicator
DS12	Green	Port 4: Power-is-good indicator
DS15	Green	Port 2: Power-is-good indicator
DS14	Green	Port 3: Power-is-good indicator
DS7	Green	Port 5: Power Indicator
DS5	Yellow	Port 5: Attention Indicator
DS10	Green	Port 4: Power Indicator
DS9	Yellow	Port 4: Attention Indicator
DS8	Green	Port 2: Power Indicator
DS6	Yellow	Port 2: Attention Indicator
DS4	Green	Port 3: Power Indicator
DS3	Yellow	Port 3: Attention Indicator
DS13	Red	Hot Plug Controller1: Power Fault Indicator(port4, port5)
DS16	Red	Hot Plug Controller2: Power Fault Indicator (port2, port3)
DS2	Green	Board Power Indicator (3.3V)
DS1	Red	Board Reset Indicator
DS17	Green	Port 5: link up status output
DS18	Green	Port 5: active status output
DS19	Green	Port 4: link up status output
DS20	Green	Port 4: active status output
DS21	Green	Port 2: link up status output
DS22	Green	Port 2: active status output
DS23	Green	Port 3: link up status output
DS24	Green	Port 3: active status output
DS25	Green	Port 0: link up status output
DS26	Green	Port 0: active status output
DS27	Green	GPIO6
DS31	Green	GPIO8
DS36	Green	GPIO7
DS32	Green	GPIO5

Table 2.20 LED Indicators

Notes

PCI Express Connectors

Pin	Side A		Side B	
1	+12V	12V power	PRSNT1#	Hot-Plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential	RSVD	Reserved
20	PETn1	pair, Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential
22	GND	Ground	PERn1	pair, Lane 1
23	PETp2	Transmitter differential	GND	Ground
24	PETn2	pair, Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential
26	GND	Ground	PERn2	pair, Lane 2
27	PETp3	Transmitter differential	GND	Ground
28	PETn3	pair, Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential
30	RSVD	Reserved	PERn3	pair, Lane 3
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETp4	Transmitter differential	RSVD	Reserved

Table 2.21 PCI Express x16 Connector Pinout (Part 1 of 2)

Notes

Pin	Side A		Side B	
34	PETn4	pair, Lane 4	GND	Ground
35	GND	Ground	PERp4	Receiver differential
36	GND	Ground	PERn4	pair, Lane 4
37	PETp5	Transmitter differential	GND	Ground
38	PETn5	pair, Lane 5	GND	Ground
39	GND	Ground	PERp5	Receiver differential
40	GND	Ground	PERn5	pair, Lane 5
41	PETp6	Transmitter differential	GND	Ground
42	PETn6	pair, Lane 6	GND	Ground
43	GND	Ground	PERp6	Receiver differential
44	GND	Ground	PERn6	pair, Lane 6
45	PETp7	Transmitter differential	GND	Ground
46	PETn7	pair, Lane 7	GND	Ground
47	GND	Ground	PERp7	Receiver differential
48	PRSNT2#	Hot-Plug presence detect	PERn7	pair, Lane 7
49	GND	Ground	GND	Ground
50	PETp8	Transmitter differential	RSVD	Reserved
51	PETn8	pair, Lane 8	GND	Ground
52	GND	Ground	PERp8	Receiver differential
53	GND	Ground	PERn8	pair, Lane 8
54	PETp9	Transmitter differential	GND	Ground
55	PETn9	pair, Lane 9	GND	Ground
56	GND	Ground	PERp9	Receiver differential
57	GND	Ground	PERn9	pair, Lane 9
58	PETp10	Transmitter differential	GND	Ground
59	PETn10	pair, Lane 10	GND	Ground
60	GND	Ground	PERp10	Receiver differential
61	GND	Ground	PERn10	pair, Lane 10
62	PETp11	Transmitter differential	GND	Ground
63	PETn11	pair, Lane 11	GND	Ground
64	GND	Ground	PERp11	Receiver differential
65	GND	Ground	PERn11	pair, Lane 11
66	PETp12	Transmitter differential	GND	Ground
67	PETn12	pair, Lane 12	GND	Ground
68	GND	Ground	PERp12	Receiver differential
69	GND	Ground	PERn12	pair, Lane 12
70	PETp13	Transmitter differential	GND	Ground

Table 2.21 PCI Express x16 Connector Pinout (Part 2 of 2)

Notes

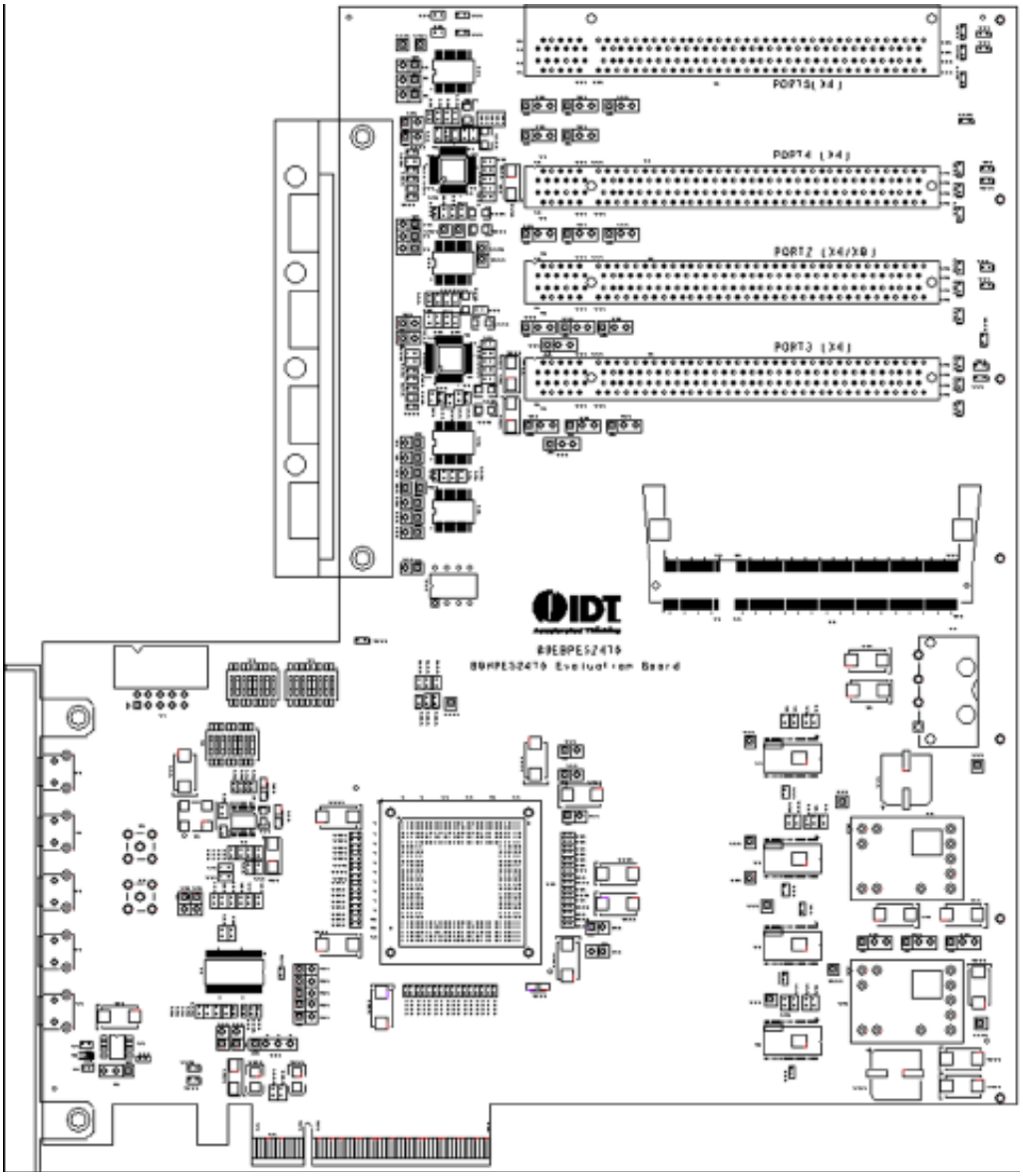
Note: These x16 PCI Express connectors comply with the PCIe specification. However, the downstream ports on the EB24T6 are electronically connected in either a x8 configuration (port 2) or a x4 configuration (ports 2, 3, 4, and 5). According to the PCIe specification, the PRSNT1# pin should be wired to the farthest available PRSNT2# pin on the connector. In the EB24T6, all PRSNT2# pins are tied together. This allows the board to be installed in a x1 or a x4 slot via a slot reducer.

PCI Express Personality Module

The PES24T6 supports port merging in a static manner during a fundamental reset. A PCI Express personality module is used in the EB24T6 to merge port 2 (x4 lane) and port 3 (x4 lane) into a single x8 port. When side 1 of the personality module is inserted into the personality module connector (J7), four PCI Express lanes are routed to port 2 and four are routed to port 3. When side 2 of the personality module is inserted into the personality module connector (J7), eight PCI Express lanes are routed to port 2, and port 3 is disconnected.

Notes

Locations of Connectors, Jumpers, and Switches



Notes

Software for the EB24T6 Eval Board

Notes

Introduction

This chapter discusses some of the main features of the available software to give users a better understanding of what can be achieved with the EB24T6 evaluation board using the device management software.

Device management software and related user documentation are available on a CD which is included in the Evaluation Board Kit. This information is also available on IDT's FTP site. For more information, contact IDT at ssdhelp@idt.com.

Device Management Software

The primary use of the Device Management Software package is to enable users of the evaluation board to access all the registers in the PES24T6 device. This access can be achieved using the PCI Express in-band configuration cycles through the upstream port on the PES24T6.

This software also enables users to save a snapshot of the current register set into a dump file which can be used for debugging purposes. An export/import facility is also available to create and use "Configuration" files which can be used to initialize the switch device with specific values in specific registers.

A conversion utility is also provided to translate a configuration file into an EEPROM programmable data structure. This enables the user to program an appropriate serial EEPROM with desirable register settings for the PES24T6, and then to populate that EEPROM onto the Evaluation Board. It is also possible to program the EEPROM directly on the Evaluation Board using a feature provided by the software package.

The front end of the Device Management Software is a user-friendly Graphical User Interface which allows the user to quickly read or write the registers of interest. The GUI also permits the user to run the software in "simulation" mode with no real hardware attached, allowing the creation of configuration files for the PES24T6 in the absence of the actual device.

Much of the Device Management Software is written with device-independent and OS-independent code. The software will be guaranteed to work on Linux (/sys interface) and MS Windows XP. It may function flawlessly on various flavors of MS Windows, but may not be validated on all. The fact that the software is device-independent assures its scalability to future PCIe parts from IDT. Once users are familiar with the GUI, they will be able to use the same GUI on all PCIe parts from IDT. This software is customized for each device through an XML device description file which includes information on the number of ports, registers, types of registers, information on bit-fields within each register, etc.

Notes

Schematics

Notes

Schematics

RENESAS

REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
STGC-0081R01	1.0	INITIAL RELEASE	2006-07-07	J.CARRILLO

SHEET	DESCRIPTION
1	TABLE OF CONTENTS
2	BLOCK DIAGRAM
3	POWER SUPPLY AND RESET
4	CLOCKS
5	SMBUS, JTAG, I/O EXPANDER
6	HOT PLUG CONTROL PORT B/C
7	HOT PLUG CONTROL PORT D/E
8	PORT B CONNECTOR
9	PORT C CONNECTOR
10	PERSONALITY MODULE CONNECTOR
11	PORT D CONNECTOR
12	PORT E CONNECTOR
13	PORT A UPSTREAM CONNECTOR
14	PES24T6 - POWER
15	PES24T6 - SMBUS REFCLKS
16	LINK STATUS WAKE

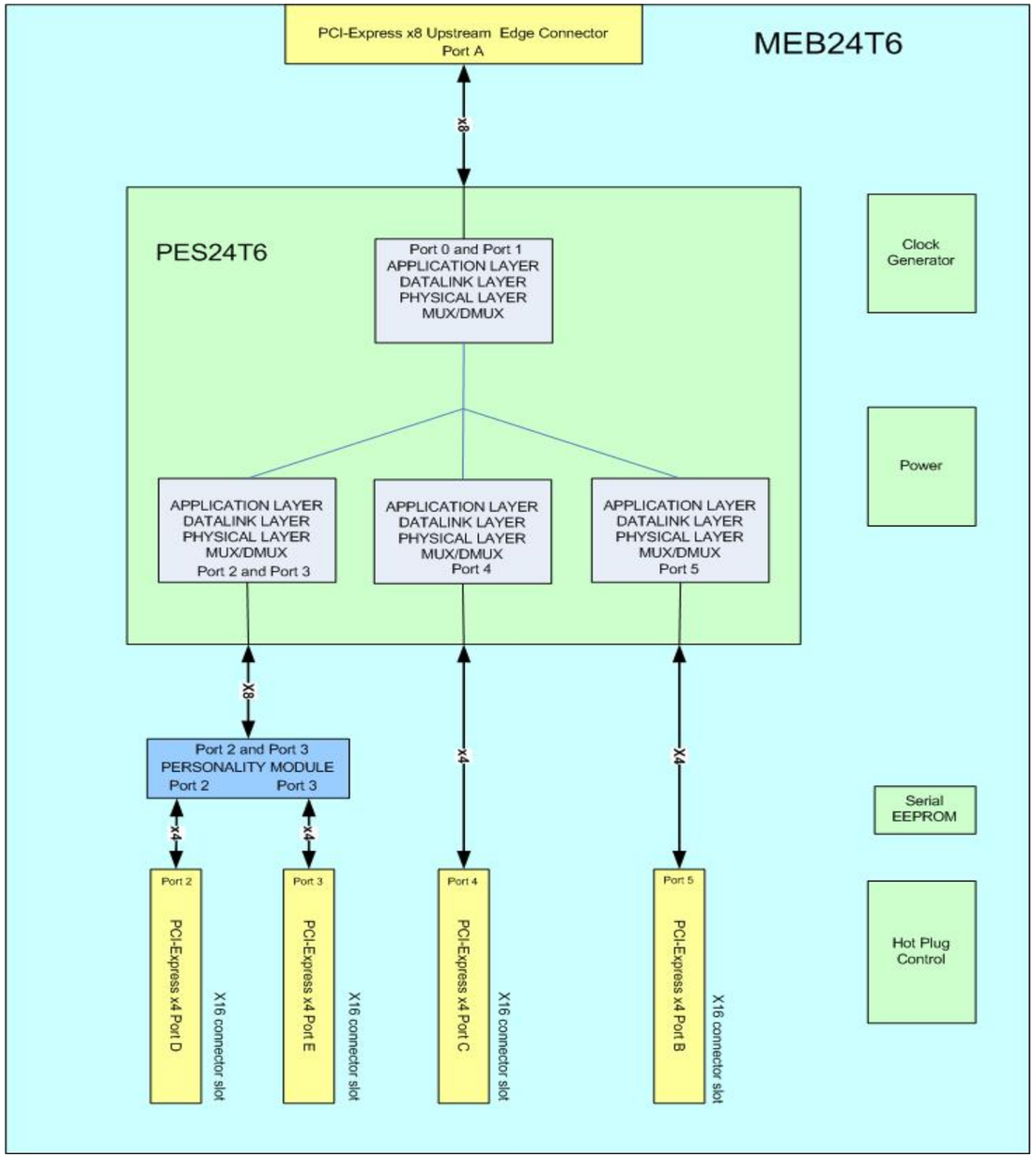
TITLE: 89EBPES24T6 89HPES24T6 EVALUATION BOARD

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00082	18-609-000	1.0

AUTHOR	CHECKED BY
J.CARRILLO	B.OH

Wed Jul 26 17:15:57 2006 SHEET 1 OF 16

BLOCK DIAGRAM



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BLOCK DIAGRAM			
SIZE B	DRAWING NO. STGSCH-00082	FAB P/N 18-609-000	REV. 1.0
AUTHOR J.CARRILLO		CHECKED BY B.OH	
Thu Jul 06 14:33:39 2006		SHEET 2 OF 16	

RENESAS

BOARD RESET

S1 PB_SW NC NO

R1 10K 5%

R6 10K 5%

R10 10K 5%

U4 TLC7733D

RESINN SENSE CONTROL CT VCC RESET RESETN GND

C12 10UF 6V

C13 47UF 10V

RED DS1

R13 330 5%

W1

M_PERSTN OUT 8 9 11 12 15

IN 3 13 PERST*

U2 SN74LVC1G125 OE* VCC A GND Y

POWER INDICATOR PLACE NEAR TOP EDGE LABEL 'POWER'

TP6

R14 330 5%

DS2 GRN

EXT P/S +12V -> D/S +3.3V

12_0V 12V_DS

W45 W46 W47

POWER CONN +12V GND GND +5V J1

C3 22UF 25V C4 10UF 16V C5 10UF 6V C6 10UF 16V

TP2 TP3

U5 PTH08T240WAD Vin Track SYNC TURBOTRANS Inhibit Vo_Adj VO_SEN+ Vout VO_SEN- GND2 GND1

C10 22UF 25V C11 330UF 16V

1.21K R7 1%

C15 47UF 10V C16 220UF 10V

3_3V_DS

C28 C29 C31 C32 C34 C35 C36 C37 0.1UF

U/S +12V -> +3.3V

TP16 TP17

U26 PTH08T240WAD

C279 22UF 25V C108 330UF 16V

1.21K R207 1%

C281 47UF 10V C282 220UF 10V

C19 C20 C21 C22 C23 C24 C25 C26 0.1UF

VPETVTT, 1.5V

TP5

U6 EN5330 1_5VA

C17 22UF 25V C18 0.047UF C27 47UF 10V

VDD_CORE 1.0V

TP1 1_0VC

U1 EN5330

C1 22UF 25V C2 0.015UF C7 47UF 10V

R2 499 1% R4 499 1% R3 2K 1% R5 2K 1%

VDDPE, 1.0V

TP4 1_0VA

U3 EN5330

C8 22UF 25V C9 0.015UF

R8 499 1% R11 499 1% R9 2K 1% R12 2K 1%

C14 47UF 10V

VDDPEA, 1.0V

TP7 1_0VB

U7 EN5310

C30 10UF 16V C33 0.015UF C38 22UF 25V

R15 499 1% R17 499 1% R16 2K 1% R18 2K 1%

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TITLE	89EBPES24T6
	POWER SUPPLY AND RESET
SIZE	B
DRAWING NO.	STGSCH-00082
FAB P/N	18-609-000
REV.	1.0
AUTHOR	J.CARRILLO
CHECKED BY	B.OH
Wed Nov 08 11:11:41 2006	SHEET 3 OF 16

RENESAS

PLACE RESISTORS CLOSE TO U9

13 IN U_REFCLK+
13 IN U_REFCLK-

R34 0 0%
R35 0 DNP 0%
R36 0 DNP 0%
R37 0 0%

3_3V

10K R19 5%
10K R20 5%
10K R21 5%
10K R22 5%

S2
SM_SW8
SSC_S0
SSC_S1
SSC_SS0
SSC_SS1

FB1
C41 1UF 16V
C42 0.1UF
C43 1UF 16V
C44 10UF 16V
C45 0.1UF
C46 0.1UF

R24 5.1K 5%

FB2
C47 1UF 16V
C48 0.1UF
C49 1UF 16V
C50 0.1UF
C51 0.1UF

U9
ICS9DB801

R38 DNP
R40 NA 5%
R42 10K 5%
R44 NA 5%
R208 10K 5%
R214 10K 5%

VDD 2
VDD 19
VDD 39
VDD 11
VDD 31
VDDA 48

SRC_IN 4
SRC_IN# 5
OE0# 6
OE1# 14
OE2# 15
OE3# 7
OE4# 43
OE5# 35
OE6# 36
OE7# 44
SRC_STOP 27
PD 26
HIGH_BW# 28
OE_INV 40
BYPASS#/PLL 22
SCLK 23
SDATA 24
SRC_DIV# 1
GND 3
GND 10
GND 18

5 6 IN PB_PWRGDN
5 6 IN PC_PWRGDN
5 7 IN PD_PWRGDN
5 7 IN PE_PWRGDN

FORCE_ON
W48 W49 W50 W51

11 9 8 15 13 5 12 IN M_SSMBCLK
IN M_SSMBDATA

R39 10K 5%
R41 DNP
R43 10K 5%
R45 DNP

DIF_0 8
DIF_0# 9
DIF_1 12
DIF_1# 13
DIF_2 16
DIF_2# 17
DIF_3 20
DIF_3# 21
DIF_4 30
DIF_4# 29
DIF_5 34
DIF_5# 33
DIF_6 38
DIF_6# 37
DIF_7 42
DIF_7# 41
LOCK 45
IREF 46
GNDA 47
GND 32
GND 25

R46 33 5%
R47 33 5%
R48 33 5%
R57 33 5%
R56 33 5%
R58 33 5%
R49 33 5%
R50 33 5%
R51 33 5%
R52 33 5%
R53 33 5%
R54 33 5%

0.1UF C52
0.1UF C53
0.1UF C54
0.1UF C55

B_REFCLKP OUT 8
B_REFCLKN OUT 8
M_REFCLK1P OUT 15
M_REFCLK1N OUT 15
M_REFCLK2P OUT 15
M_REFCLK2N OUT 15
C_REFCLKP OUT 9
C_REFCLKN OUT 9
D_REFCLKP OUT 11
D_REFCLKN OUT 11
E_REFCLKP OUT 12
E_REFCLKN OUT 12

R59 49.9 1%
R60 49.9 1%
R61 49.9 1%
R62 49.9 1%
R63 49.9 1%
R64 49.9 1%
R65 49.9 1%
R66 49.9 1%
R67 49.9 1%
R68 49.9 1%
R69 49.9 1%
R70 49.9 1%

R55 475 1%

U8
ICS557-03

VDDODA 12
VDDXD 16
SS1 8
SS0 3
S1 2
S0 1
X1/ICLK 4
X2 5
OE 6
CLK0P 15
CLK0N 14
CLK1P 11
CKL1N 10
IREF 9
GNDODA 13
GNDXD 7

R29 33 5%
R26 33 5%
R27 33 5%
R28 33 5%

R30 49.9 1%
R31 49.9 1%
R32 49.9 1%
R33 49.9 1%

R25 475 1%

Y1
SG-8002CA25.0000M-PCBB:ROHS
25MHZ
C39 22UF 25V
C40 0.001UF
R23 33 5%

J3
CONNSMA
J2
CONNSMA

OUTPUT SELECT

S2:2	S2:1	S1	S0	CLK (1:0)
ON	ON	0	0	25M
ON	OFF	0	1	100M
OFF	ON	1	0	125M
OFF	OFF	1	1	200M

SPREAD SELECTION

S2:4	S2:3	SS1	SS0	SPREAD %
ON	ON	0	0	CENTER +-0.25
ON	OFF	0	1	DOWN -0.5
OFF	ON	1	0	DOWN -0.75
OFF	OFF	1	1	NO SPREAD

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TITLE 89EBPES24T6

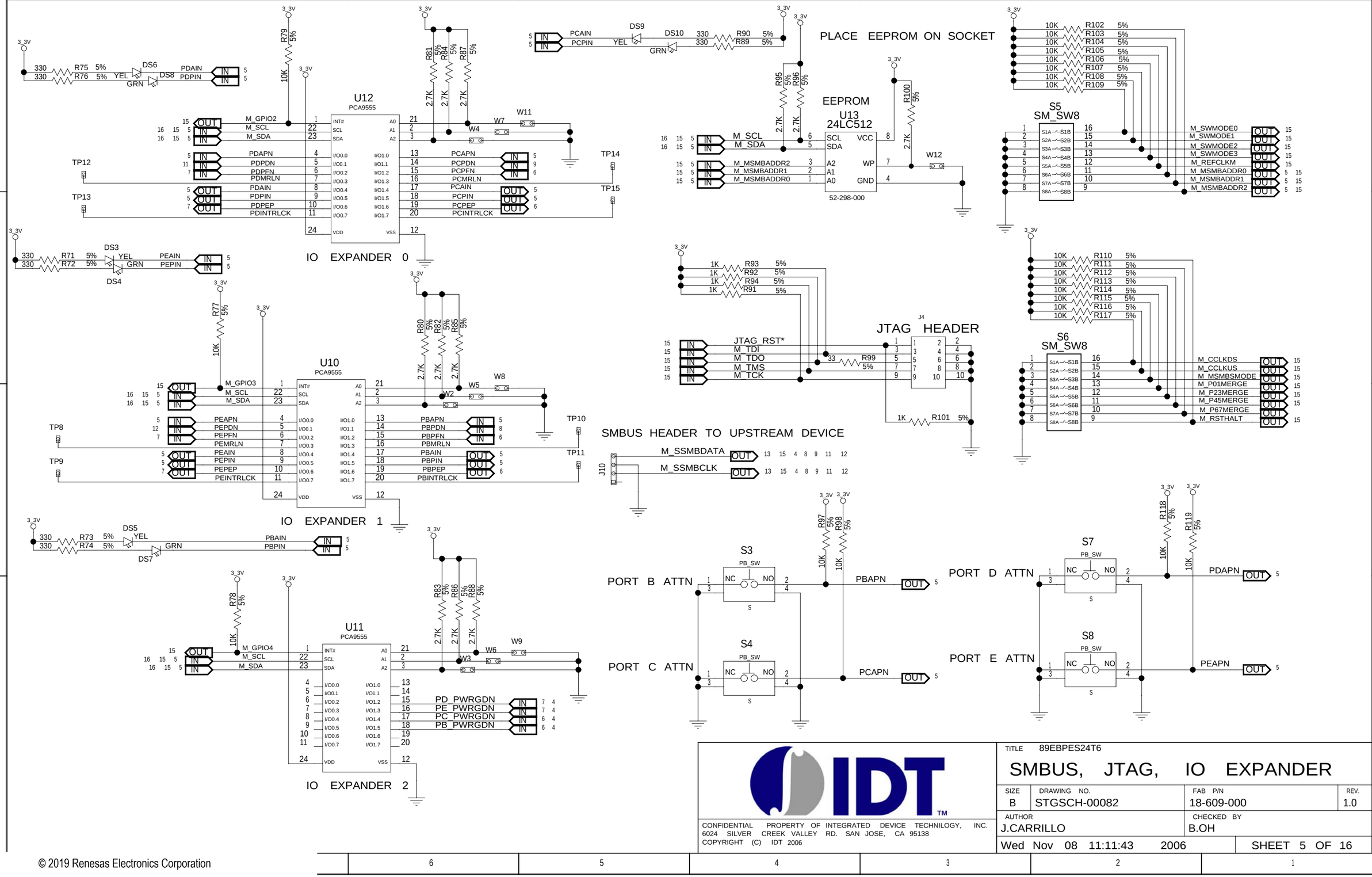
CLOCKS

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00082	18-609-000	1.0

AUTHOR	CHECKED BY
J.CARRILLO	B.OH

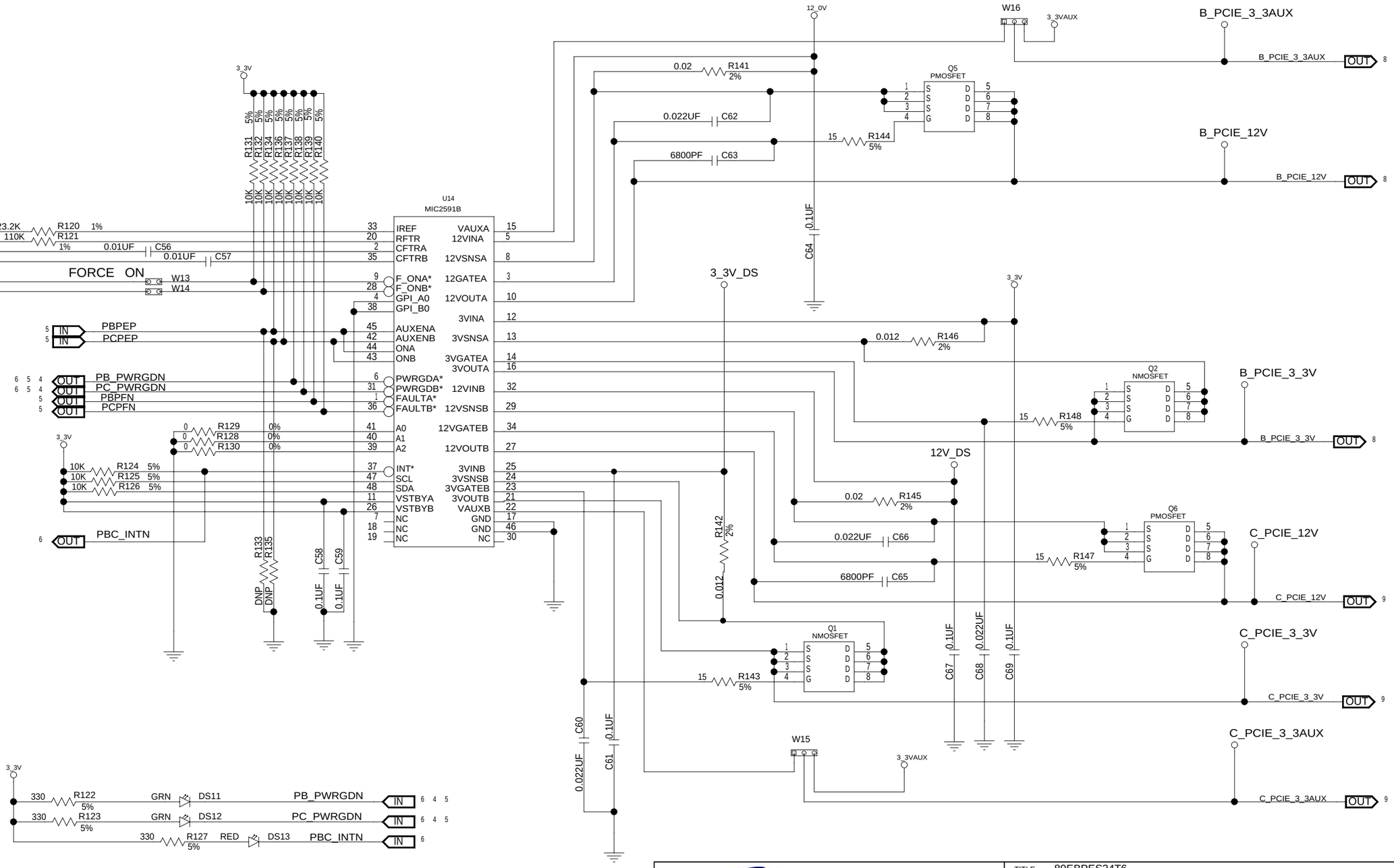
Wed Nov 08 11:11:42 2006 SHEET 4 OF 16

RENESAS



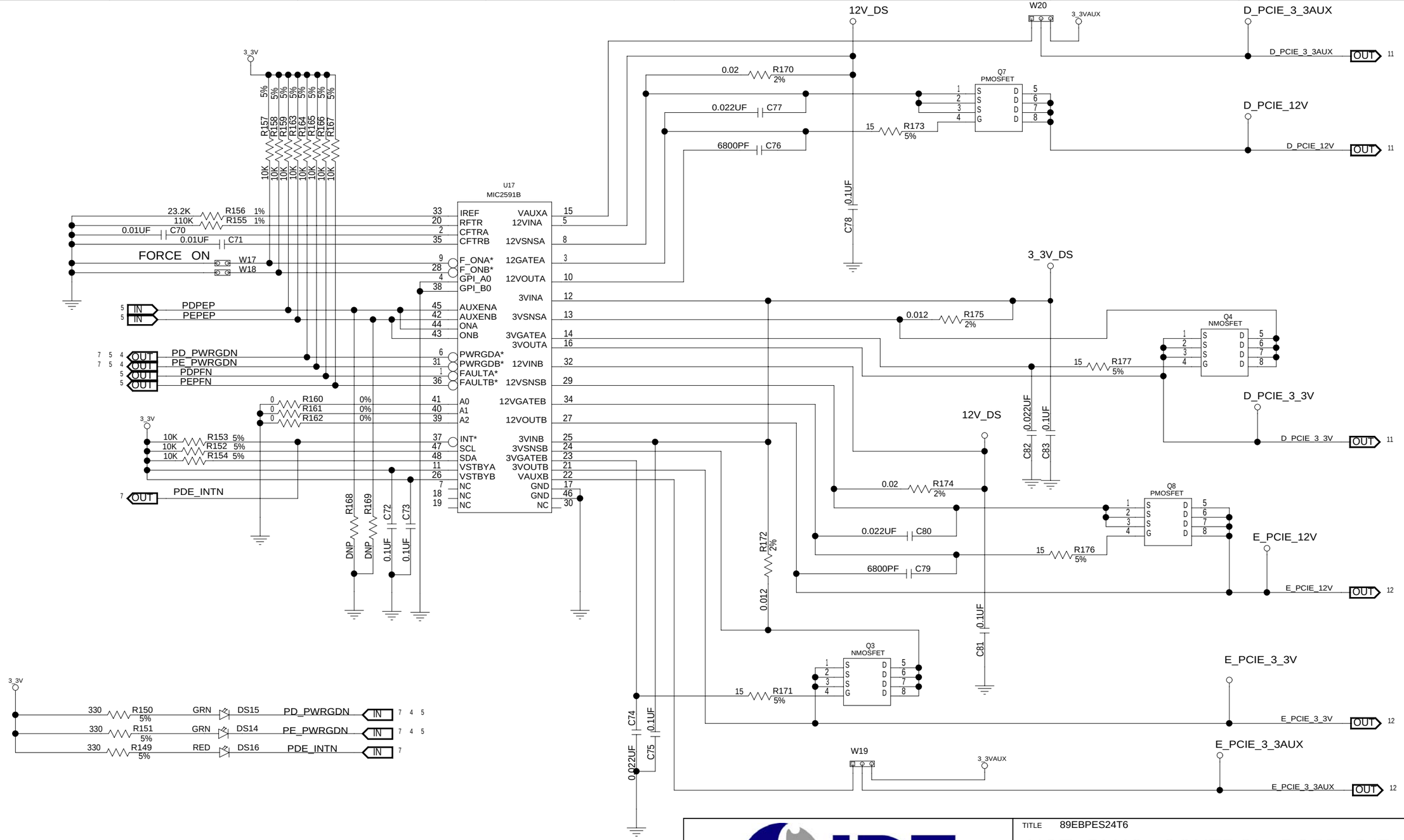
TITLE 89EBPES24T6			
SMBUS, JTAG, IO EXPANDER			
SIZE B	DRAWING NO. STGSCH-00082	FAB P/N 18-609-000	REV. 1.0
AUTHOR J.CARRILLO		CHECKED BY B.OH	
Wed Nov 08 11:11:43 2006		SHEET 5 OF 16	

RENESAS



TITLE	89EBPES24T6		
HOT PLUG CONTROL PORT B/C			
SIZE: B	DRAWING NO.: STGSCH-00082	FAB P/N: 18-609-000	REV.: 1.0
AUTHOR: J.CARRILLO		CHECKED BY: B.OH	
Wed Nov 08 11:11:44 2006		SHEET 6 OF 16	

RENESAS



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TITLE 89EBPES24T6			
HOT PLUG CONTROL PORT D/E			
SIZE B	DRAWING NO. STGSCH-00082	FAB P/N 18-609-000	REV. 1.0
AUTHOR J.CARRILLO		CHECKED BY B.OH	
Wed Nov 08 11:11:45 2006		SHEET 7 OF 16	

RENESAS

B_PCIE_12V
W21
12_0V
B_12V
J5
PCIE_X16_CONN_RA
B_3_3V
B_PCIE_3_3V
W26
3_3V
C84 16V 10UF
C85 16V 10UF
C86 16V 10UF
C87 16V 10UF
M_SSMBCLK
M_SSMBDATA
R179 0 0%
R180 0 0%
R181 0 0%
B_PCIE_3_3AUX
B_WAKE*
B_PERST*
W27
M_PERSTN
M_B_PERST*
B_PETP0
B_PETN0
B_PETP1
B_PETN1
B_PETP2
B_PETN2
B_PETP3
B_PETN3
B_REFCLKP
B_REFCLKN
B_PERP0
B_PERN0
B_PERP1
B_PERN1
B_PERP2
B_PERN2
B_PERP3
B_PERN3
PBPDN
R178 5.1K 5%

U18
89HPES24T6ZABXG
5 of 8
52R-537-000

C_PERP0 G22
C_PERN0 G23
C_PERP1 J22
C_PERN1 J23
C_PERP2 L22
C_PERN2 L23
C_PERP3 N22
C_PERN3 N23
B_PERP0 R22
B_PERN0 R23
B_PERP1 U22
B_PERN1 U23
B_PERP2 W22
B_PERN2 W23
B_PERP3 AA22
B_PERN3 AA23

G25 C96 C_PETP0
G26 C88 C_PETN0
J25 C97 C_PETP1
J26 C89 C_PETN1
L25 C98 C_PETP2
L26 C90 C_PETN2
N25 C99 C_PETP3
N26 C91 C_PETN3
R25 C100 B_PETP0
R26 C92 B_PETN0
U25 C101 B_PETP1
U26 C93 B_PETN1
W25 C102 B_PETP2
W26 C94 B_PETN2
AA25 C103 B_PETP3
AA26 C95 B_PETN3
0.1UF

DS17 GRN 330 R182 5% PB_LINKUPN
DS18 GRN 330 R183 5% PB_ACTIVEN

DOWNSTREAM (PORT B) CONNECTOR

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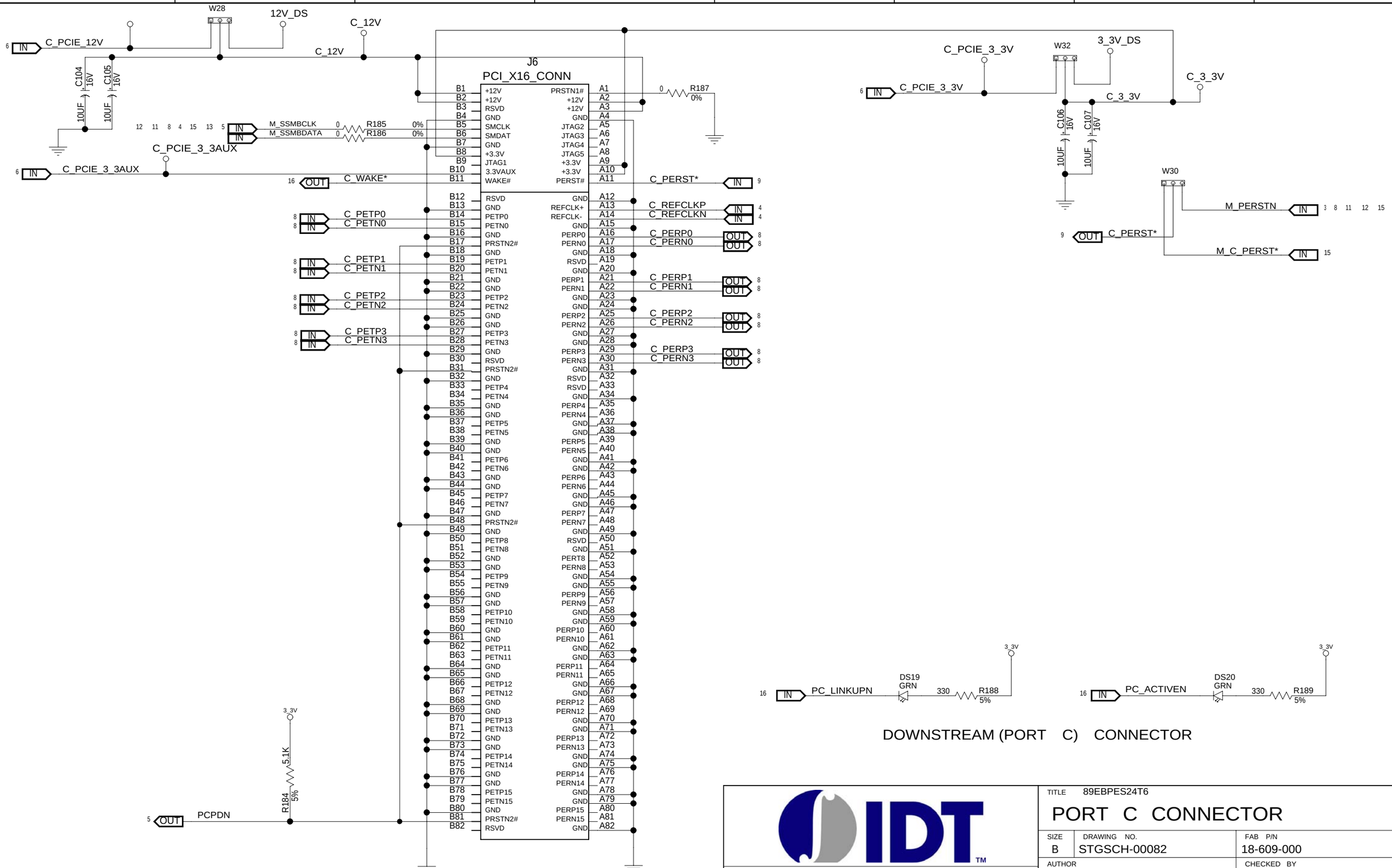
TITLE 89EBPES24T6
PORT B CONNECTOR
SIZE B | DRAWING NO. STGSCH-00082 | FAB P/N 18-609-000 | REV. 1.0
AUTHOR J.CARRILLO | CHECKED BY B.OH
Wed Nov 08 11:11:46 2006 | SHEET 8 OF 16

RENESAS



DOWNSTREAM (PORT C) CONNECTOR

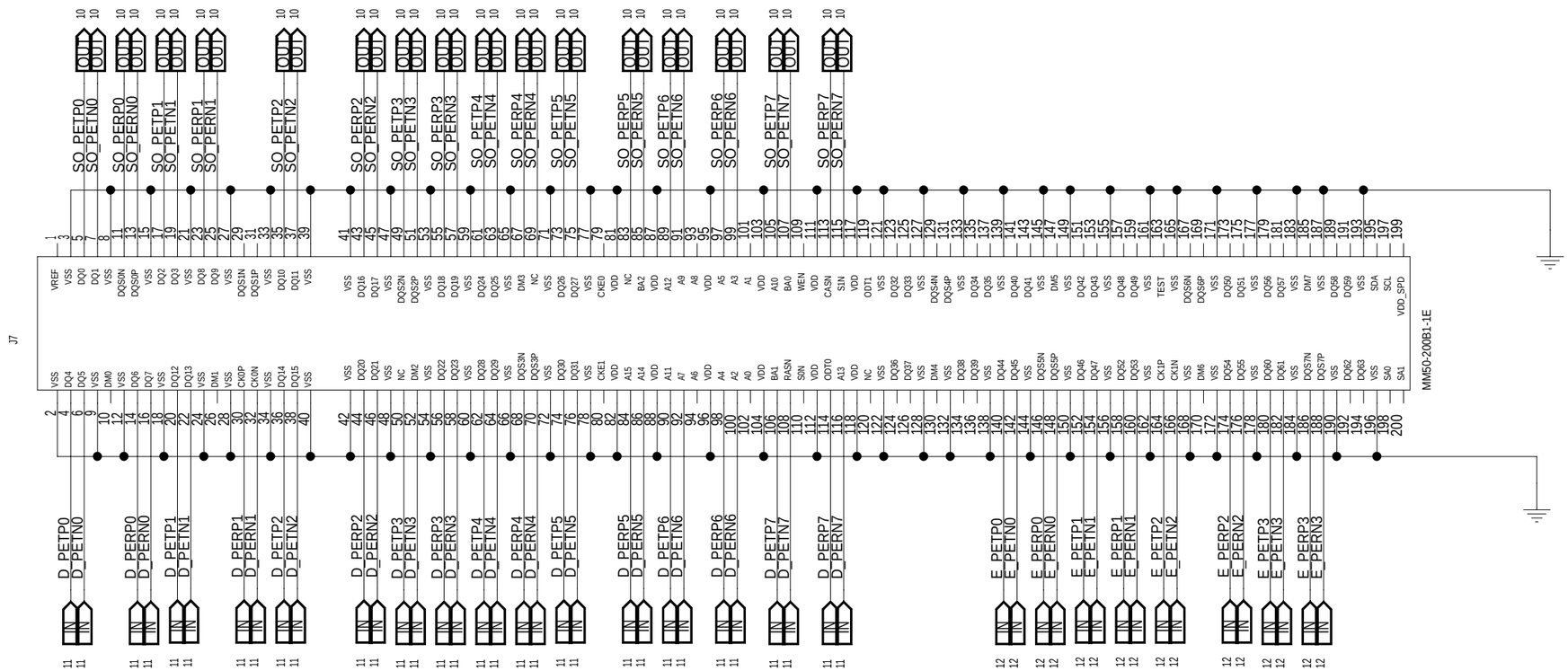
TITLE 89EBPES24T6

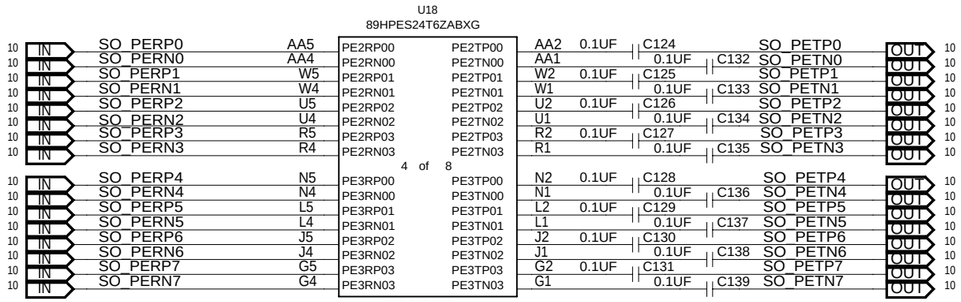
PORT C CONNECTOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00082	18-609-000	1.0

AUTHOR	CHECKED BY
J.CARRILLO	B.OH

Wed Nov 08 11:11:47 2006 SHEET 9 OF 16





TITLE	89EBPES24T6
	PERSONALITY MODULE CONN
SIZE	B
DRAWING NO.	STGSCH-00082
FAB P/N	18-609-000
REV.	1.0
AUTHOR	J.CARRILLO
CHECKED BY	B.OH
	Wed Nov 08 11:11:36 2006
	SHEET 10 OF 16

RENESAS

D_PCIE_12V W33 12V_DS D_12V

7 IN D_PCIE_12V

D_12V

C140 16V 10UF C141 16V 10UF

J8
PCI_X16_CONN

M_SSMBCLK 0 R191 0% IN
M_SSMBDATA 0 R192 0% IN

D_PCIE_3_3AUX

7 IN D_PCIE_3_3AUX

16 OUT D_WAKE*

0 R193 0%

D_PERST* IN 11

D_REFCLKP IN 4
D_REFCLKN IN 4

D_PETP0 IN 10
D_PETN0 IN 10

D_PERP0 OUT 10
D_PERN0 OUT 10

D_PETP1 IN 10
D_PETN1 IN 10

D_PERP1 OUT 10
D_PERN1 OUT 10

D_PETP2 IN 10
D_PETN2 IN 10

D_PERP2 OUT 10
D_PERN2 OUT 10

D_PETP3 IN 10
D_PETN3 IN 10

D_PERP3 OUT 10
D_PERN3 OUT 10

D_PETP4 IN 10
D_PETN4 IN 10

D_PERP4 OUT 10
D_PERN4 OUT 10

D_PETP5 IN 10
D_PETN5 IN 10

D_PERP5 OUT 10
D_PERN5 OUT 10

D_PETP6 IN 10
D_PETN6 IN 10

D_PERP6 OUT 10
D_PERN6 OUT 10

D_PETP7 IN 10
D_PETN7 IN 10

D_PERP7 OUT 10
D_PERN7 OUT 10

3_3V 5.1K R190 5%

5 OUT PDPDN

D_PCIE_3_3V W34 3_3V_DS D_3_3V

7 IN D_PCIE_3_3V

D_3_3V

C142 16V 10UF C143 16V 10UF

W35

M_PERSTN IN 3 8 9 12 15

11 OUT D_PERST*

M_D_PERST* IN 15

3_3V

16 IN PD_LINKUPN DS21 GRN 330 R194 5%

16 IN PD_ACTIVEN DS22 GRN 330 R195 5%

DOWNSTREAM (PORT D) CONNECTOR

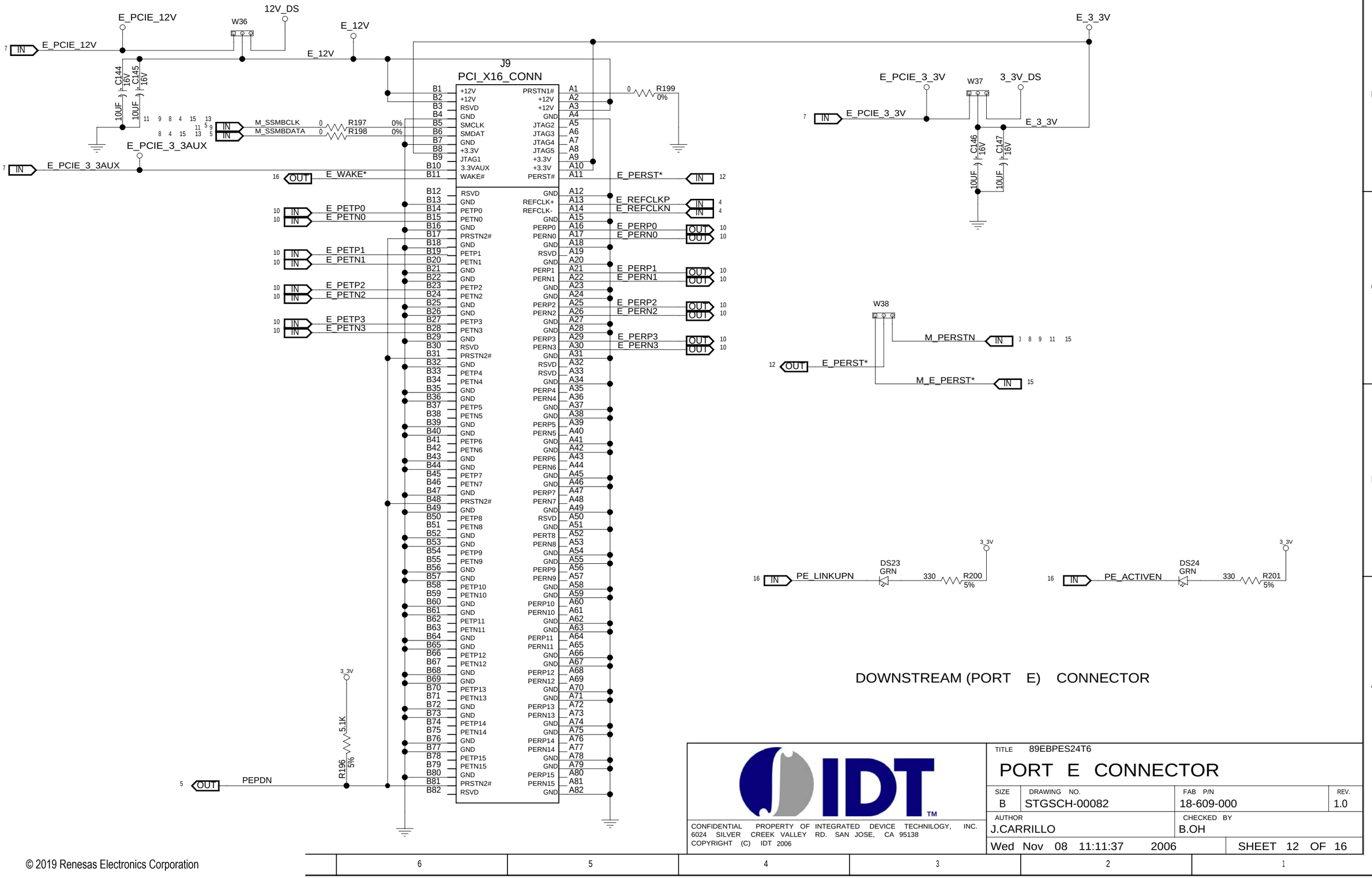
TITLE 89EBPES24T6

PORT D CONNECTOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00082	18-609-000	1.0

AUTHOR	CHECKED BY
J.CARRILLO	B.OH

Wed Nov 08 11:11:36 2006 SHEET 11 OF 16



TITLE 89EBPES24T6

PORT E CONNECTOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00082	18-609-000	1.0

AUTHOR	CHECKED BY
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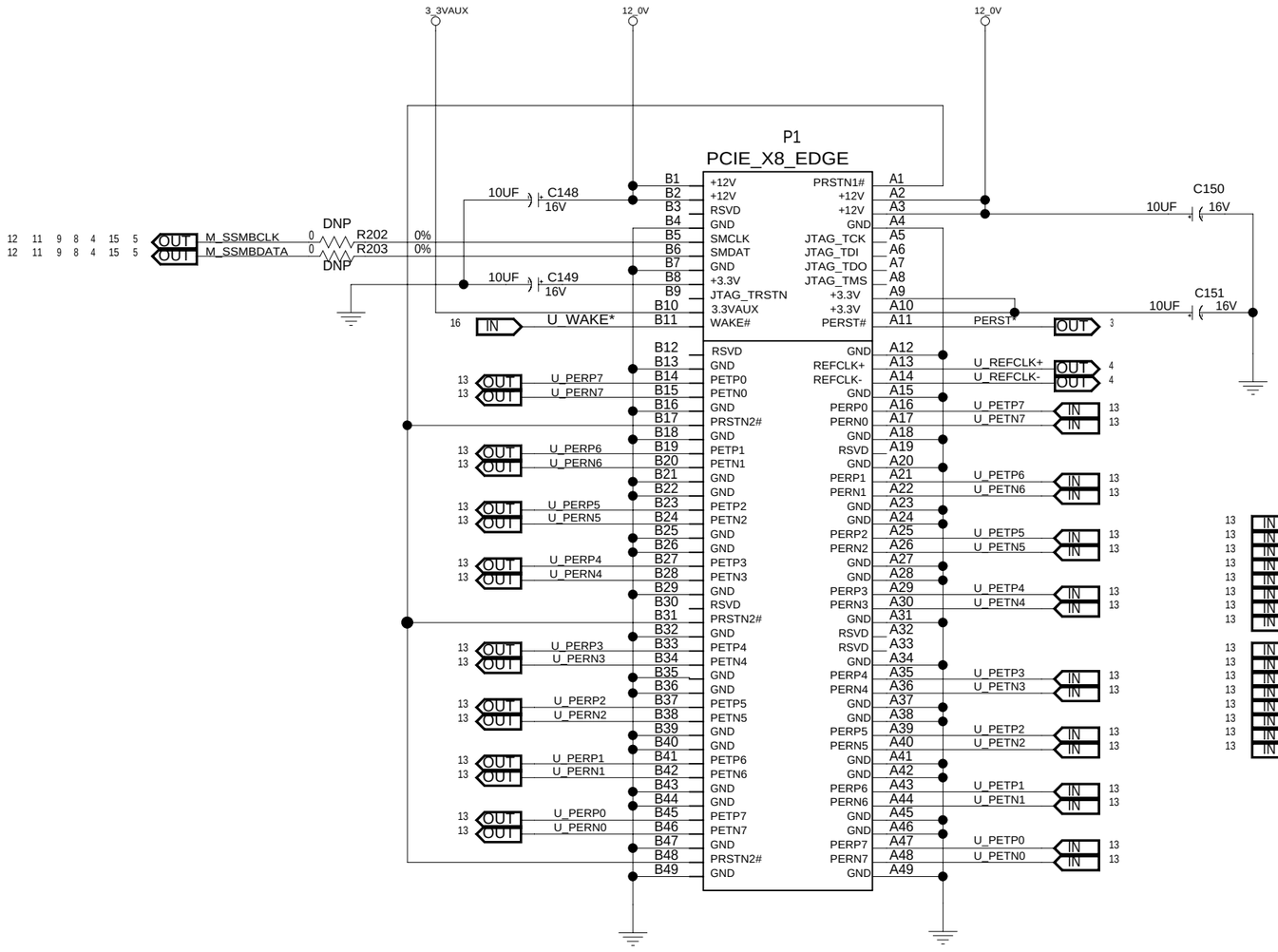
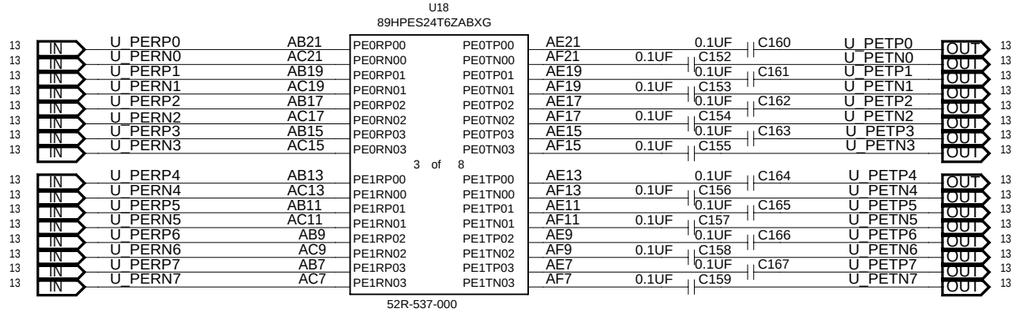
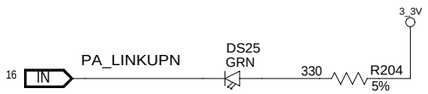
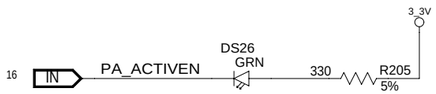
Wed Nov 08 11:11:37 2006 SHEET 12 OF 16









PORT A UPSTREAM (EDGE) CONNECTOR

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TITLE 89EBPES24T6

PORT A UPSTREAM CONNECTOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00082	18-609-000	1.0

AUTHOR	CHECKED BY	
J.CARRILLO	B.OH	
Wed Nov 08 11:11:38 2006		SHEET 13 OF 16

JUMPERS MUST BE POPULATED FOR NORMAL OPERATION

VTT W23 1_5VA

VDDPE_J W22 1_0VA

3_3V_J W10 3_3V

VDDCORE_J W25 1_0VC

1_0VB W24

VDDPEA

U18 89HPES24T6ZABXG

V3	VDDAPE1	VDDPE1	J3
T3	VDDAPE2	VDDPE2	J24
F3	VDDAPE3	VDDPE3	L3
F24	VDDAPE4	VDDPE4	L24
K3	VDDAPE5	VDDPE5	N3
K4	VDDAPE6	VDDPE6	N24
K5	VDDAPE7	VDDPE7	R3
K22	VDDAPE8	VDDPE8	R24
K23	VDDAPE9	VDDPE9	U3
K24	VDDAPE10	VDDPE10	U24
T4	VDDAPE11	VDDPE11	W3
T23	VDDAPE12	VDDPE12	W24
T24	VDDAPE13	VDDPE13	AA3
V4	VDDAPE14	VDDPE14	AA24
V5	VDDAPE15	VDDPE15	AD8
V22	VDDAPE16	VDDPE16	AD10
V23	VDDAPE17	VDDPE17	AD11
V24	VDDAPE18	VDDPE18	AD13
AB10	VDDAPE19	VDDPE19	AD15
AB14	VDDAPE20	VDDPE20	AD18
AB18	VDDAPE21	VDDPE21	AD19
AC8	VDDAPE22	VDDPE22	AD21
AC10	VDDAPE23	VDDPE23	G3
AC16	VDDAPE24	VDDPE24	G24
AC18	VDDAPE25		
AD16	VDDAPE26		

9 of 8

52R-537-000

U18 89HPES24T6ZABXG

C4	VDDCORE1	VDDIO1	A3
C14	VDDCORE2	VDDIO2	B3
C16	VDDCORE3	VDDIO3	B17
D5	VDDCORE4	VDDIO4	B24
D6	VDDCORE5	VDDIO5	C5
D8	VDDCORE6	VDDIO6	C7
D10	VDDCORE7	VDDIO7	C9
D12	VDDCORE8	VDDIO8	C11
D13	VDDCORE9	VDDIO9	C13
D15	VDDCORE10	VDDIO10	C15
D17	VDDCORE11	VDDIO11	C17
D18	VDDCORE12	VDDIO12	C19
D19	VDDCORE13	VDDIO13	C21
D21	VDDCORE14	VDDIO14	C23
D22	VDDCORE15		
E6	VDDCORE16	VTT1	H3
E7	VDDCORE17	VTT2	H4
E9	VDDCORE18	VTT3	H23
E11	VDDCORE19	VTT4	H24
E13	VDDCORE20	VTT5	M3
E15	VDDCORE21	VTT6	M4
E17	VDDCORE22	VTT7	M23
E19	VDDCORE23	VTT8	M24
E20	VDDCORE24	VTT9	P3
E21	VDDCORE25	VTT10	P4
F1	VDDCORE26	VTT11	P23
F2	VDDCORE27	VTT12	P24
F25	VDDCORE28	VTT13	Y3
F26	VDDCORE29	VTT14	Y4
M1	VDDCORE30	VTT15	Y23
M26	VDDCORE31	VTT16	Y24
P1	VDDCORE32	VTT17	AC6
P26	VDDCORE33	VTT18	AC12
T1	VDDCORE34	VTT19	AC14
T26	VDDCORE35	VTT20	AC20
V1	VDDCORE36	VTT21	AD6
V26	VDDCORE37	VTT22	AD12
AB3	VDDCORE38	VTT23	AD14
AB4	VDDCORE39	VTT24	AD20
AB5	VDDCORE40		
AB23	VDDCORE41		
AB24	VDDCORE42		
AC3	VDDCORE43		
AC4	VDDCORE44		
AC5	VDDCORE45		
AC23	VDDCORE46		
AC24	VDDCORE47		
AD3	VDDCORE48		
AD4	VDDCORE49		
AD5	VDDCORE50		
AD23	VDDCORE51		
AD24	VDDCORE52		
AE3	VDDCORE53		
AE4	VDDCORE54		
AE23	VDDCORE55		
AE24	VDDCORE56		
AF3	VDDCORE57		
AF4	VDDCORE58		
AF5	VDDCORE59		
AF10	VDDCORE60		
AF12	VDDCORE61		
AF14	VDDCORE62		
AF16	VDDCORE63		
AF23	VDDCORE64		
AF24	VDDCORE65		

7 of 8

52R-537-000

U18 89HPES24T6ZABXG

A1	VSS1	VSS64	M25
A2	VSS2	VSS65	P2
A14	VSS3	VSS66	P5
A23	VSS4	VSS67	P22
A25	VSS5	VSS68	P25
A26	VSS6	VSS69	T2
B1	VSS7	VSS70	T5
B2	VSS8	VSS71	T22
B13	VSS9	VSS72	T25
B16	VSS10	VSS73	V2
B25	VSS11	VSS74	V25
B26	VSS12	VSS75	Y1
C2	VSS13	VSS76	Y2
C6	VSS14	VSS77	Y5
C8	VSS15	VSS78	Y22
C10	VSS16	VSS79	Y25
C12	VSS17	VSS80	Y26
C18	VSS18	VSS81	AB1
C20	VSS19	VSS82	AB2
C24	VSS20	VSS83	AB6
C25	VSS21	VSS84	AB8
D2	VSS22	VSS85	AB12
D3	VSS23	VSS86	AB16
D7	VSS24	VSS87	AB20
D9	VSS25	VSS88	AB22
D11	VSS26	VSS89	AB25
D14	VSS27	VSS90	AB26
D16	VSS28	VSS91	AC1
D20	VSS29	VSS92	AC2
D24	VSS30	VSS93	AC22
D25	VSS31	VSS94	AC25
E1	VSS32	VSS95	AC26
E2	VSS33	VSS96	AD1
E3	VSS34	VSS97	AD2
E4	VSS35	VSS98	AD7
E8	VSS36	VSS99	AD9
E10	VSS37	VSS100	AD17
E12	VSS38	VSS101	AD22
E14	VSS39	VSS102	AD25
E16	VSS40	VSS103	AD26
E18	VSS41	VSS104	AE1
E22	VSS42	VSS105	AE2
E23	VSS43	VSS106	AE5
E24	VSS44	VSS107	AE6
E25	VSS45	VSS108	AE8
E26	VSS46	VSS109	AE10
F4	VSS47	VSS110	AE12
F5	VSS48	VSS111	AE14
F22	VSS49	VSS112	AE16
F23	VSS50	VSS113	AE18
H1	VSS51	VSS114	AE20
H2	VSS52	VSS115	AE22
H5	VSS53	VSS116	AE25
H22	VSS54	VSS117	AE26
H25	VSS55	VSS118	AF1
H26	VSS56	VSS119	AF2
K1	VSS57	VSS120	AF6
K2	VSS58	VSS121	AF8
K25	VSS59	VSS122	AF18
K26	VSS60	VSS123	AF20
M2	VSS61	VSS124	AF22
M5	VSS62	VSS125	AF25
M22	VSS63	VSS126	AF26

8 of 8

52R-537-000

1UF C170 16V
1UF C212 16V
1UF C214 16V
1UF C246 16V

0.1UF C171, C172, C173, C174, C175, C176, C177, C178, C179, C180, C181, C182, C183, C184, C185, C186

0.1UF C191, C192, C193, C194, C195, C196, C197, C198, C199, C200, C201, C202, C203, C204, C205, C206, C207, C208, C209, C210, C211

0.1UF C215, C216, C217, C218, C219, C220

0.1UF C221, C222, C223, C224, C225, C226, C227, C228, C229, C230, C231, C232

0.1UF C247, C248, C249, C250, C251, C252, C253, C254, C255, C256, C257, C258, C259, C260, C261, C262, C263, C264, C265, C266, C267, C268, C269, C270

C169 47UF 10V
C168 47UF 10V
47UF C189 10V
47UF C190 10V
47UF C243 10V
47UF C244 10V

FB3
FB4
FB5

1UF C187 16V
0.1UF C188
1UF C213 16V

0.1UF C233, C234, C235, C236, C237, C238, C239, C240, C241, C242, C245, C271, C272, C273, C274, C275, C276

47UF C277 10V
47UF C278 10V

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TITLE 89EBPES24T6

PES24T6 - POWER

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00082	18-609-000	1.0

AUTHOR	CHECKED BY
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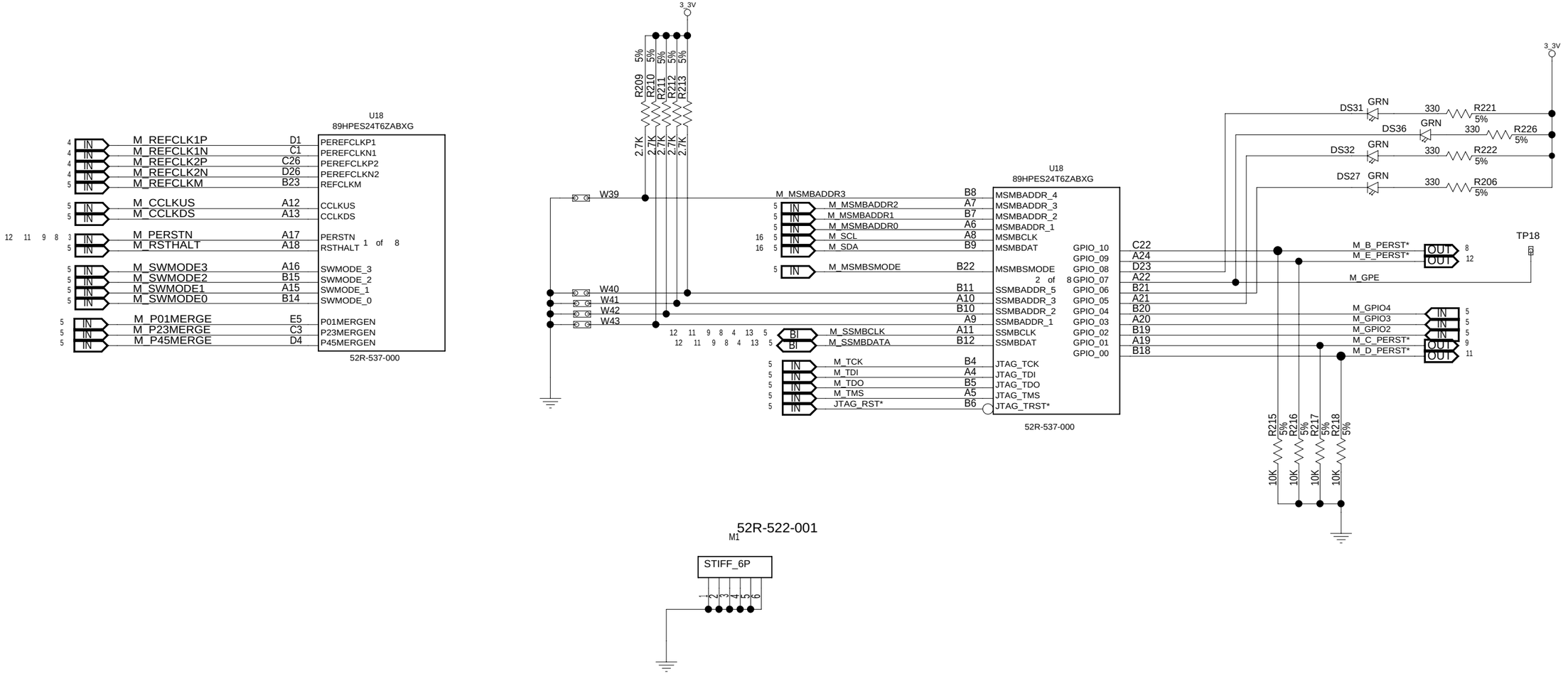
Wed Nov 08 11:11:39 2006 SHEET 14 OF 16



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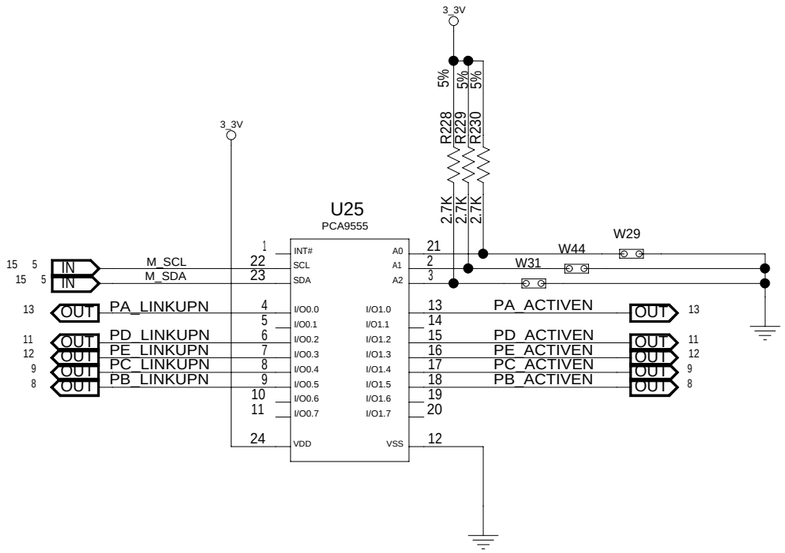
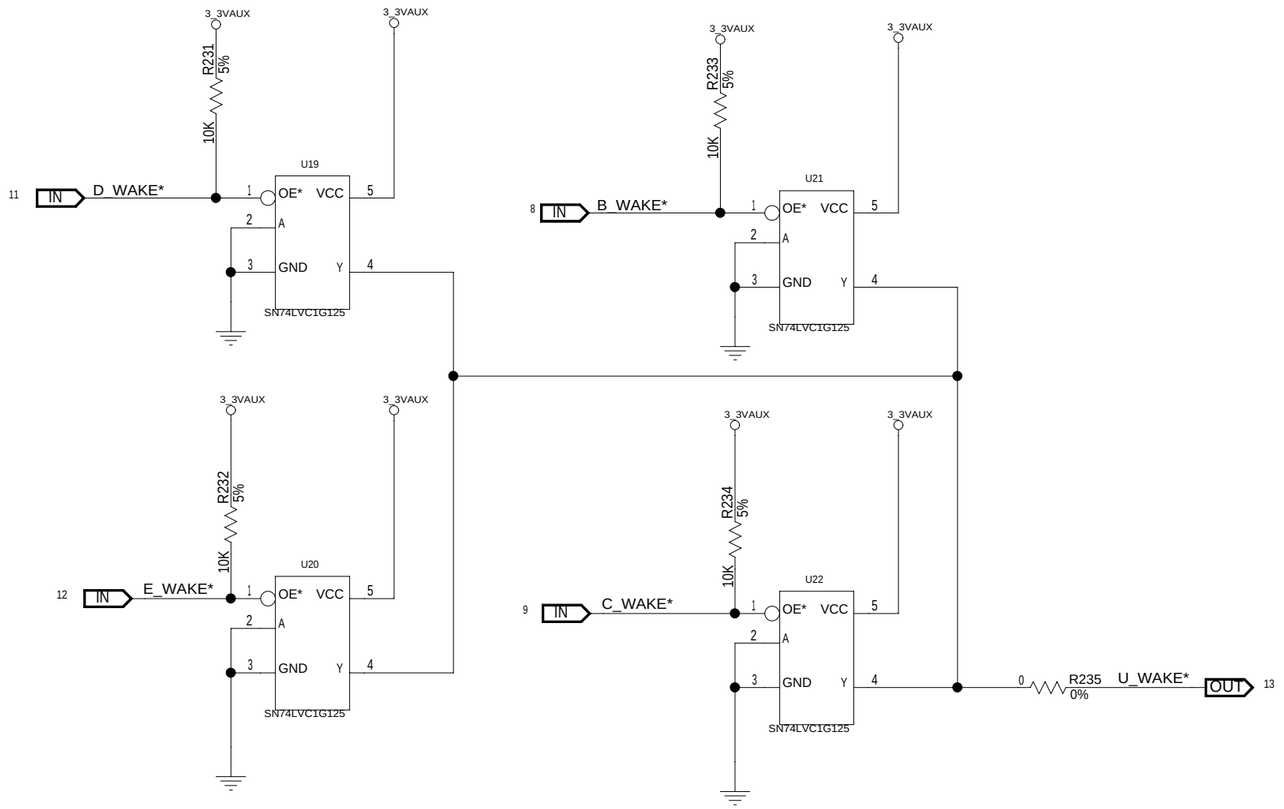
	PES24T6 SMBUS REFCLKS
SIZE B / DRAWING NO. STGSCH-00082 / FAB P/N 18-609-000 / REV. 1.0	
AUTHOR J.CARRILLO	CHECKED BY B.OH
Wed Nov 08 11:11:40 2006	SHEET 15 OF 16



IO EXPANDER 4



TITLE 89EBPES24T6

LINK STATUS WAKE

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00082	18-609-000	1.0

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Wed Nov 08 11:11:40 2006 SHEET 16 OF 16

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