IDT™ 89EBPES16NT2 Evaluation Board Manual

(Eval Board: 18-642-000)

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Introduction

The 89HPES16NT2 switch (also referred to as PES16NT2 in this manual) is a member of IDT's PCI Express® standard (PCIe®) based line of products. It is a 16-lane, 2-port peripheral chip that provides high-performance switching and non-transparent bridging (NTB) function between an upstream port and an NTB downstream port.

The 89EBPES16NT2 Evaluation Board (also referred to as EB16NT2 in this manual) provides an evaluation platform for the PES16NT2 switch. It is designed to function as an add-on card to be plugged into a x8 PCIe slot available on a motherboard hosting an appropriate root complex, microprocessor(s), and an NTB downstream port to be connected to another root complex, microprocessor(s) via a PCI Express cable. The EB16NT2 is a vehicle to test and evaluate the functionality of the PES16NT2 chip. Customers can use this board to get a headstart on software development prior to the arrival of their own hardware. The EB16NT2 is also used by IDT to reproduce system-level hardware or software issues reported by customers. Figure 1.1 illustrates the functional block diagram representing the main parts of the EB16NT2 board.

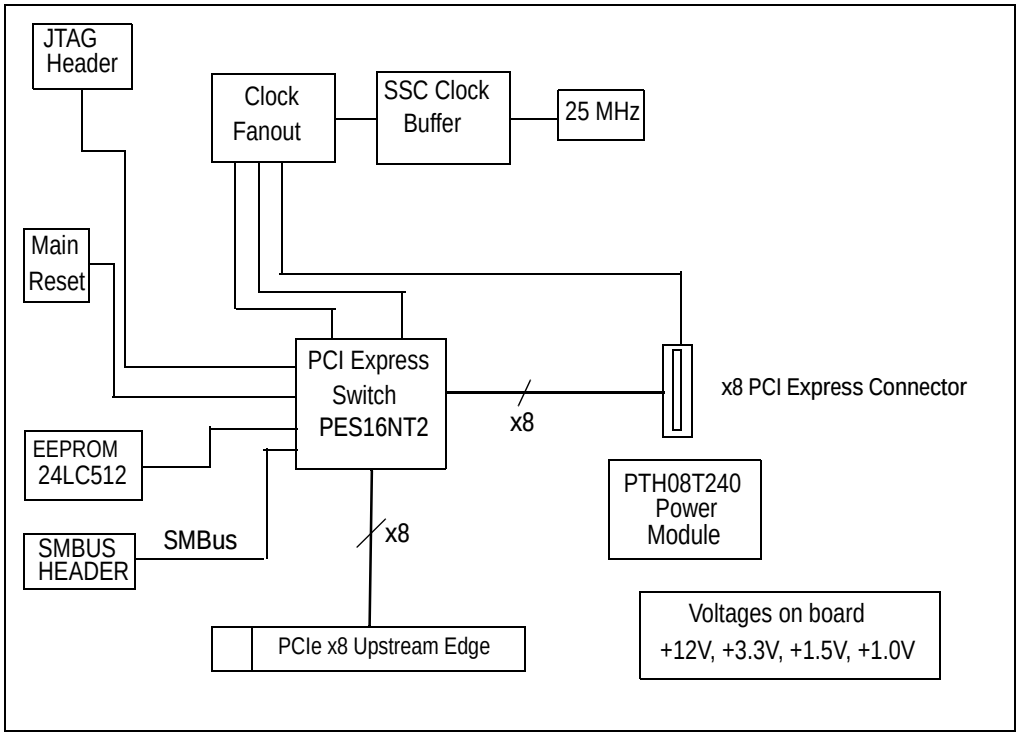

Figure 1.1 Function Block Diagram of the EB16NT2 Eval Board

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Board Features

Hardware

- PES16NT2 PCIe 2-port Non-Transparent switch
  - *Two ports, 16 PCIe lanes*
  - *PCIe Base Specification Revision 1.0a compliant*
  - *8 GBps (64Gbps) aggregate switching capacity*
  - *Up to 2048 byte maximum Payload Size*
  - *Automatic lane reversal and polarity inversion supported on all lanes*
  - *Automatic per port link width negotiation to x8, x4, x2, x1*
  - *Load configuration from an optional serial EEPROM via SMBUS*
- Upstream, Transparent/Non-Transparent Port
  - *One edge connector on the upstream port, to be plugged into a slot with x8 capable on a host motherboard*
  - *Transparent or Non-Transparent port via x8 PCI Express connector*
- Numerous user selectable configurations set using onboard jumpers and DIP-switches
  - *Source of clock - host clock or onboard clock generator*
  - *Two clock rates*
  - *Boot mode selection*
- SMBUS Slave Interface (4 pin header)
- SMBUS Master Interface connected to the Serial EEPROMs through I/O expander
- Push button for Warm Reset
- Several LEDs to display status, reset, power, etc.
- One 10-pin JTAG connector (pitch 2.54 mm x 2.54 mm)

Software

There is no software or firmware executed on the board in transparent mode. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the PES16NT2 within host systems running popular operating systems. In non-transparent mode, IDT provides Windows XP or a Linux device driver for PES16NT2 Non-Transparent Bridge endpoints. This driver includes two separate drivers, PCI endpoint driver and NDIS Ethernet miniport driver. Please contact ssdhelp@idt.com for additional information.

- Installation programs
  - *Operating Systems Supported: Windows2000, WindowsXP, Linux*
- GUI-based application for Windows and Linux
  - *Allows users to view and modify registers in the PES16NT2*
  - *Binary file generator for programming the serial EEPROMs attached to the SMBUS.*

Other

- A metal bracket is required to firmly hold in place the four endpoints plugged into the EB16NT2 board.
- SMBUS cable may be required for certain evaluation exercises.
- SMA connectors are provided on the EB16NT2 board for specific test points.

Revision History

November 13, 2007: Initial publication of board manual.

Installation of the EB16NT2 Eval Board

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EB16NT2 Installation

This chapter discusses the steps required to configure and install the EB16NT2 evaluation board. All available DIP switches and jumper configurations are explained in detail.

The primary installation steps are:

1. Configure jumper/switch options suitable for the evaluation or application requirements.
2. Insert the evaluation board into the host system (motherboard with root complex chipset).
3. Connect the NTB port to a remote system via a PCI Express® cable. An PCI Express adapter card to PCI Express Cable connector can be used on a remote system.
4. Apply power to the host system.

The EB16NT2 board is shipped with all jumpers and switches configured to their default settings. In most cases, the board does not require further modification or setup.

PCI Express Adapter Card

The PCI Express adapter card is an x8 link PCI Express card. It can be installed in a remote system. A (x8 lane) PCIe® cable is used to connect a remote system to EB16NT2 NTB port. See Figure 2.1 for the graphical presentation of this connection.

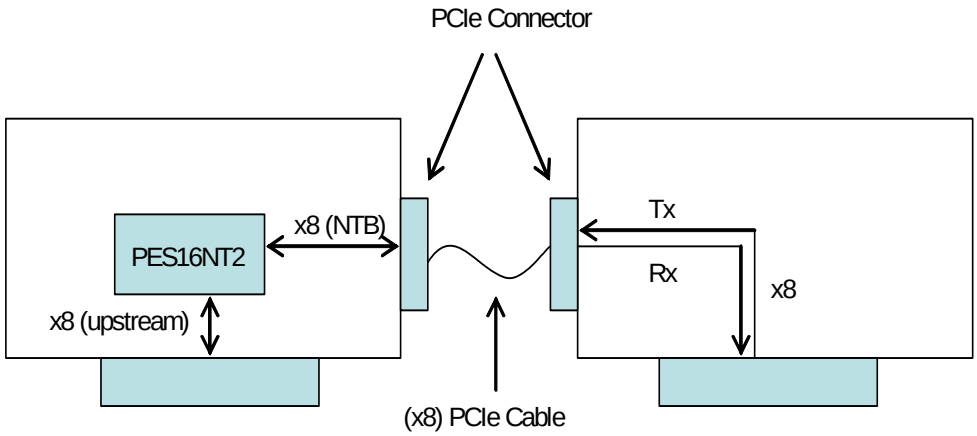

Figure 2.1 PCIe Adapter Card

Hardware Description

The 89HPES16NT2 is a member of the IDT PRECISE™ family of PCI Express switching solutions offering the next-generation I/O interconnect standard. The PES16NT2 is a 16-lane, 2-port peripheral chip that provides high-performance switching and non-transparent bridging (NTB) functions between a PCIe upstream

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port and an NTB downstream port. The PES16NT2 is a part of the IDT PCIe System Interconnect Products family and is intended to be used with IDT PCIe System Interconnect Switches. Together, the chipset targets multi-host and intelligent I/O applications such as communications, storage, and blade servers, where inter-domain communication is required.

The EB16NT2 non-transparent port is accessible through x8 PCI Express cable connectors.

Basic requirements for the board to run are:

- Host system with a PCI Express root complex supporting x8 configuration through a PCI Express x8 slot.
- A secondary remote system with a PCI Express root complex supporting x8 configuration through a PCI Express x8 slot.

Reference Clocks

The PES16NT2 requires a pair of differential reference clocks. The EB16NT2 derives these clocks from a common source which is user-selectable. The common source can be either the host system's reference clock or the onboard clock generator. Selection is made by stuffing resistors described in Table 2.1. Typical usage model for the EB16NT2 in non-transparent mode includes two root complexes: one connects to the upstream port and the other connects to a NTB port. Each root complex most likely will have its own clock source. SSC (Spread Spectrum Clock) must be disabled in this configuration.

Clock Configuration Stuffing Option	
W7 and W8	Clock Source
Pins 2 and 3	Onboard Reference Clock – Use onboard clock generator
Pins 1 and 2	Upstream Reference Clock – Host system provides clock (Default)

Table 2.1 Clock Source Selection

The source for the onboard clock is the ICS557-03 clock generator device (U8) connected to a 25MHz oscillator (Y1). When using the onboard clock generator, the EB16NT2 allows selection between multiple clock rates via DIP switches as described in Table 2.2.

Clock Frequency Switch - S2[2:1]		
S2[2]	S2[1]	Clock Frequency
OFF	OFF	Reserved
OFF	ON	125 MHz
ON	OFF	100 MHz (Default)
ON	ON	<Reserved>

Table 2.2 Clock Frequency Selection

The output of the onboard clock generator is accessible through two SMA connectors located on the Evaluation Board. See Table 2.3. This can be used to connect a scope for probing or capturing purposes and cannot be used to drive the clock from an external source.

Onboard Reference Clock Output (Differential) – J2, J3	
J2	Positive Reference Clock
J3	Negative Reference Clock

Table 2.3 SMA Connectors - Onboard Reference Clock

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Power Sources

The EB16NT2 is powered from the upstream port slot power.

PCI Express Serial Data Transmit Termination Voltage Converter

A DC-DC converter (U6) provides a 1.5V PCI Express serial data transmit termination voltage (shown as VPETVTT) to the PES16NT2.

PCI Express Digital Power Voltage Converter

A separate DC-DC converter (U3) provides a 1.0V PCI Express digital power voltage (VDDPE) to the PES16NT2.

PCI Express Analog Power Voltage Converter

A separate DC-DC converter (7) provides a 1.0V PCI Express analog power voltage (shown as VDDPEA) to the PES16NT2.

Core Logic Voltage Converter

A separate DC-DC converter (U1) provides the 1.0V core voltage (VDDCORE) to the PES16NT2.

3.3V I/O Power Module

A 12V to 3.3V power module (U26) provides the 3.3V I/O voltage (VDD_3V3) to the PES16NT2.

Power-up Sequence

The power-up sequence must be as following:

1. VDDIO - 3.3V
2. VDDCORE, VDDPEA, VDDPE - 1.0V
3. VTTPE - 1.5V

When powering up, each voltage level must ramp up and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations between sequential valid power level requirements. To insure that the sequencing requirements are met, a 0.015UF is used at the SOFTSTART cap on the VTTPE and VTTPEA voltage converter (U3 and U7 pin 36) in the EB16NT2.

Required Jumpers

To deliver power to the PES16NT2 switch, the following jumpers must be shunted: W10, W22-W25. These jumpers were implemented so that the power consumption of the PES16NT2 can be measured.

Reset

The PES16NT2 supports two types of reset mechanisms as described in the PCI Express specification:

- Fundamental Reset: This is a system-generated reset that propagates along the PCI Express tree through a single side-band signal PERST# which is connected to the Root Complex, the PES16NT2, and the endpoints.
- Hot Reset: This is an In-band Reset, communicated downstream via a link from one device to another. Hot Reset may be initiated by software. This is further discussed in the 89HPES16NT2 User Manual. The EB16NT2 evaluation board provides seamless support for Hot Reset.

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Fundamental Reset

There are two types of Fundamental Resets which may occur on the EB16NT2 evaluation board:

- Cold Reset: During initial power-on, the onboard voltage monitor (TLC7733D) will assert the PCI Express Reset (PERSTN) input pin of the PES16NT2.
- Warm Reset: This is triggered by hardware while the device is powered on. Warm Reset can be initiated by two methods:
  - Pressing a push-button switch (S1) located on EB16NT2 board
  - The host system board IO Controller Hub asserting PERST# signal, which propagates through the PCIe upstream edge connector of the EB16NT2. Note that one can bypass the onboard voltage monitor (TLC7733D) by moving the resistor from pin 1-2 to pin 2-3 on W27.

Both events cause the onboard voltage monitor (TLC7733D) to assert the PCI Express Reset (PERSTN) input of the PES16NT2 while power is on.

An external side fundamental reset is initiated when the switch is configured to operate in non-transparent mode and the PCI Express Non-Transparent Bridge Reset (PENTBRST#) signal is asserted. This results in the resetting of the transaction, data link, and PHY layers associated with the external side of the non-transparent bridge. The initialization of all registers associated with the external side of the non-transparent bridge are set to their initial values except those with a read and write when unlocked attribute and those associated with the non-transparent bridge configuration capability structure.

Boot Configuration Vector

A boot configuration vector consisting of the signals listed in Table 2.4 is sampled by the PES16NT2 during a fundamental reset (while PERSTN is active). The boot configuration vector defines the essential parameters for switch operation and is set using DIP switches S5 and S6 as defined in Table 2.5.

Signal	Description
CCLKDS	Common Clock Downstream. The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices. This pin is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be overridden by modifying the SCLK bit in the downstream port's PCIELSTS register. Default: 0x1
CCLKUS	Common Clock Upstream. The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This pin is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the P0_PCIELSTS register. Default: 0x1
MSMBSMODE	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 kHz. Default: 0x0
RSTHALT	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, the PES16NT2 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the P0_SWCTL register through the SMBus. The value may be overridden by modifying the RSTHALT bit in the P0_SWCTL register. Default: 0x0

Table 2.4 Boot Configuration Vector Signals (Part 1 of 2)

Notes

Signal	Description
SWMODE[2:0]	Switch Mode. These configuration pins determine the PES16NT2 switch operating mode. Default: 0x1 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM-based initialization 0x2 - Non-transparent mode 0x3 - Non-transparent mode with serial EEPROM initialization 0x4 - Non-transparent failover mode 0x5 - Non-transparent failover mode serial EEPROM initialization 0x7 - 0xF Reserved Default: 0x0
REFCLKM	PCI Express Reference Clock Mode Select. This signal selects the frequency of the reference clock input. Default: 0x0 0x0 - 100 MHz 0x1 - 125 MHz
MSMBADDR[2:0]	Master SMBus Address. These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded. Default: 0x0

Table 2.4 Boot Configuration Vector Signals (Part 2 of 2)

Signal	Description	Default
S6[1]	CCLKDS	OFF
S6[2]	CCLKUS	OFF
S6[3]	SWMODE[3]	ON
S6[4]	SWMODE[2]	ON
S6[5]	SWMODE[1]	ON
S6[6]	SWMODE[0]	ON
S6[7]	Not Used	ON
S6[8]	Not Used	ON
S5[1]	MSMBADDR[4]	ON
S5[2]	MSMBADDR[3]	ON
S5[3]	MSMBADDR[2]	ON
S5[4]	MSMBADDR[1]	ON
S5[5]	REFCLKM	ON
S6[6]	RSTHALT#	ON
S6[7]	MSMBSMODE	ON
S5[8]	Not Used	ON

Table 2.5 Boot Configuration Vector Switches S7 & S8 (ON=0, OFF=1)

SMBus Interfaces

The System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate. It is based on the principles of operation of I^2C. Implementation of the SMBus signals in the PCI Express connector is optional and may not be present on the host system. The SMBus interface consists of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins.

Notes

The PES16NT2 contains two SMBus interfaces: a slave SMBus interface and a master SMBus interface. The slave SMBus interface allows a SMBus Master device (such as the Intel E7520) full access to all software-visible registers. The Master SMBus interface provides connection to the external serial EEPROMs used for initialization.

SMBus Slave Interface

On the PES16NT2 board, the slave SMBus interface is accessible through the PCI Express edge connector as well as a 4-pin header as described in Table 2.6.

Note: The SMBus signals to the PCI Express edge connector is disabled by default. To enable them, place 0-ohm resistors at locations R74 and R75.

.

Slave SMBus Interface Connector J10	
Pin	Signal
1	N/C
2	SCL
3	GND
4	SDA

Table 2.6 Slave SMBus Interface Connector

A fixed slave SMBus address (0b1110_111) specified by the SSMBADDR[5,3:1] pins is used.

Slave Interface Address Configuration	
Address Bit	Signal
1	SSMBUSADDR[1]
2	SSMBUSADDR[2]
3	SSMBUSADDR[3]
4	0
5	SSMBUSADDR[5]
6	1
7	1

Table 2.7 SMBus Slave Interface Address Configuration

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. Initiation of any SMBus transaction other than those listed above produces undefined results. See the SMBus 2.0 specification for a detailed description of the following transactions:

- Byte and Word Write/Read
- Block Write/Read

SMBus Master Interface

The seven bits address for the selected EEPROM device is **0b1010_000** by default.

Notes

JTAG Header

The PES16NT2 provides a JTAG connector J4 for access to the PES16NT2 JTAG interface. The connector is a 2.54 x 2.54 mm pitch male 10-pin connector. Refer to Table 2.8 for the JTAG Connector J4 pin out.

JTAG Connector J5					
Pin	Signal	Direction	Pin	Signal	Direction
1	/TRST - Test reset	Input	2	GND	—
3	TDI - Test data	Input	4	GND	—
5	TDO - Test data	Output	6	GND	—
7	TMS - Test mode select	Input	8	GND	—
9	TCK - Test clock	Input	10	GND	—

Table 2.8 JTAG Connector Pin Out

Miscellaneous Jumpers, Headers

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W12	Header	Shunted	Disable EEPROM Write protect feature (Default)
W2	Header	Open	Force remote (PCIe Cable) power on
W32	Header	Open	Tie PCIe Cable 3.3V power to on board VCC_3V3

Table 2.9 Miscellaneous Jumpers, Headers

LEDs

There are several LED indicators on the EB16NT2 which convey status feedback. A description of each is provided in Table 2.10.

Location	Color	Definition
DS2	Green	VCC_3V3Power indicator
DS1	Red	Reset
DS4	Green	GPIO0
DS29	Green	GPIO3
DS30	Green	GPIO5
DS31	Green	GPIO7
DS33	Green	GPIO2
DS34	Green	GPIO4
DS35	Green	GPIO5
DS29	Green	GPIO9

Table 2.10 LED Indicators (Part 1 of 2)

Notes

Location	Color	Definition
DS30	Green	GPIO10
DS31	Green	GPIO12
DS32	Green	GPIO15

Table 2.10 LED Indicators (Part 2 of 2)

PCI Express Edge Connector

Pin	Side B		Side A	
1	+12V	12V power	PRSNT1#	Hot-Plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential	RSVD	Reserved
20	PETn1	pair, Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential
22	GND	Ground	PERn1	pair, Lane 1
23	PETp2	Transmitter differential	GND	Ground
24	PETn2	pair, Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential
26	GND	Ground	PERn2	pair, Lane 2

Table 2.11 PCI Express x8 Edge Connector Pinout (Part 1 of 2)

Notes

Pin	Side B		Side A	
27	PETp3	Transmitter differential	GND	Ground
28	PETn3	pair, Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential
30	RSVD	Reserved	PERn3	pair, Lane 3
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETp4	Transmitter differential	RSVD	Reserved
34	PETn4	pair, Lane 4	GND	Ground
35	GND	Ground	PERp4	Receiver differential
36	GND	Ground	PERn4	pair, Lane 4
37	PETp5	Transmitter differential	GND	Ground
38	PETn5	pair, Lane 5	GND	Ground
39	GND	Ground	PERp5	Receiver differential
40	GND	Ground	PERn5	pair, Lane 5
41	PETp6	Transmitter differential	GND	Ground
42	PETn6	pair, Lane 6	GND	Ground
43	GND	Ground	PERp6	Receiver differential
44	GND	Ground	PERn6	pair, Lane 6
45	PETp7	Transmitter differential	GND	Ground
46	PETn7	pair, Lane 7	GND	Ground
47	GND	Ground	PERp7	Receiver differential
48	PRSNT2#	Hot-Plug presence detect	PERn7	pair, Lane 7
49	GND	Ground	GND	Ground

Table 2.11 PCI Express x8 Edge Connector Pinout (Part 2 of 2)

PCI Express Cable x8 Wire Connections

Pin#	Cable Side A		CableSide B	Pin#
A1 A4 A7 A10 A13 A16 A22 A25 A28 A31 A34 B1 B4 B7 B10 B13 B22 B25 B28 B31 B34	GND	Drain Wires	GND	A1 A4 A7 A10 A13 A16 A22 A25 A28 A31 A34 B1 B4 B7 B10 B13 B22 B25 B28 B31 B34
A2	PETp0	Differential Pair	PERp0	B2
A3	PETn0		PERn0	B3
A5	PETp1	Differential Pair	PERp1	B5
A6	PETn1		PERn1	B6

Table 2.12 PCI Express Cable x8 Wire Connections (Part 1 of 3)

Notes

Pin#	Cable Side A		CableSide B	Pin#
A8	PETp2	Differential Pair	PERp2	B8
A9	PETn2		PERn2	B9
A11	PETp3	Differential Pair	PERp3	B11
A12	PETn3		PERn3	B12
A14	CREFCLKp	Differential Pair	CREFCLKp	A14
A15	CREFCLKn		CREFCLKn	A15
A17	RSVD	NC	RSVD	A17
A18	RSVD	NC	RSVD	A18
A19	SB_RTN	Hook-up Wire	SB_RTN	A19
A20	CPRSNT	Hook-up Wire	CPRSNT	A20
A21	CPWRON	Hook-up Wire	CPWRON	A21
A23	PETp4	Differential Pair	PERp4	B23
A24	PETn4		PERn4	B24
A26	PETp5	Differential Pair	PERp5	B26
A27	PETn5		PERn5	B27
A29	PETp6	Differential Pair	PERp6	B29
A30	PETn6		PERn6	B30
A32	PETp7	Differential Pair	PERp7	B32
A33	PETn7		PERn7	B33
B2	PERp0	Differential Pair	PETp0	A2
B3	PERn0		PETn0	A3
B5	PERp1	Differential Pair	PETp1	A5
B6	PERn1		PETn1	A6
B8	PERp2	Differential Pair	PETp2	A8
B9	PERn2		PETn2	A9
B11	PERp3	Differential Pair	PETp3	A11
B12	PERn3		PETn3	A12
B14	PWR	NW	PWR	B14
B15	PWR	NW	PWR	B15
B16	PWR	NW	PWR	B16
B17	PWR_RTN	NW	PWR_RTN	B17
B18	PWR_RTN	NW	PWR_RTN	B18
B19	PWER_RTN	NW	PWER_RTN	B19
B20	CWAKE#	Hook-up Wire	CWAKE#	B20
B21	CPERST#	Kook-up Wire	CPERST#	B21
B23	PERp4	Differential Pair	PETp4	A23
B24	PERn4		PETn4	A24

Table 2.12 PCI Express Cable x8 Wire Connections (Part 2 of 3)

Notes

Pin#	Cable Side A		CableSide B	Pin#
B26	PERp5	Differential Pair	PETp5	A26
B27	PERn5		PETn5	A27
B29	PERp6	Differential Pair	PETp6	A29
B30	PERn6		PETn6	A30
B32	PERp7	Differential Pair	PETp7	A32
B33	PERn7		PETn7	A33
Backshell	Chassis Ground	Overall Cable Braid	Backshell	Chassis Ground
			CableSide B	Pin#

Table 2.12 PCI Express Cable x8 Wire Connections (Part 3 of 3)

PCI Express Cable x8 Connector Definition

Pin #	Signal	Description
A1 A4 A7 A10 A13 A16 A22 A25 A28 A31 A34 B1 B4 B7 B10 B13 B22 B25 B28 B31 B34	GND	Ground Reference for Transmitter and Receiver Lanes
A2	PETp0	Differential Pair
A3	PETn0	
A5	PETp1	Differential Pair
A6	PETn1	
A8	PETp2	Differential Pair
A9	PETn2	
A11	PETp3	Differential Pair
A12	PETn3	
A14	CREFCLKp	Differential 100 MHz Cable Reference Clock
A15	CREFCLKn	
A17	RSVD	NC
A18	RSVD	NC
A19	SB_RTN	Signal Return for Single Ended Sideband Signals
A20	CPRSNT	Used for detection of whether a cable is installed and the downstream subsystem is powered
A21	CPWRON	Upstream Subsystem's Power Valid Notification

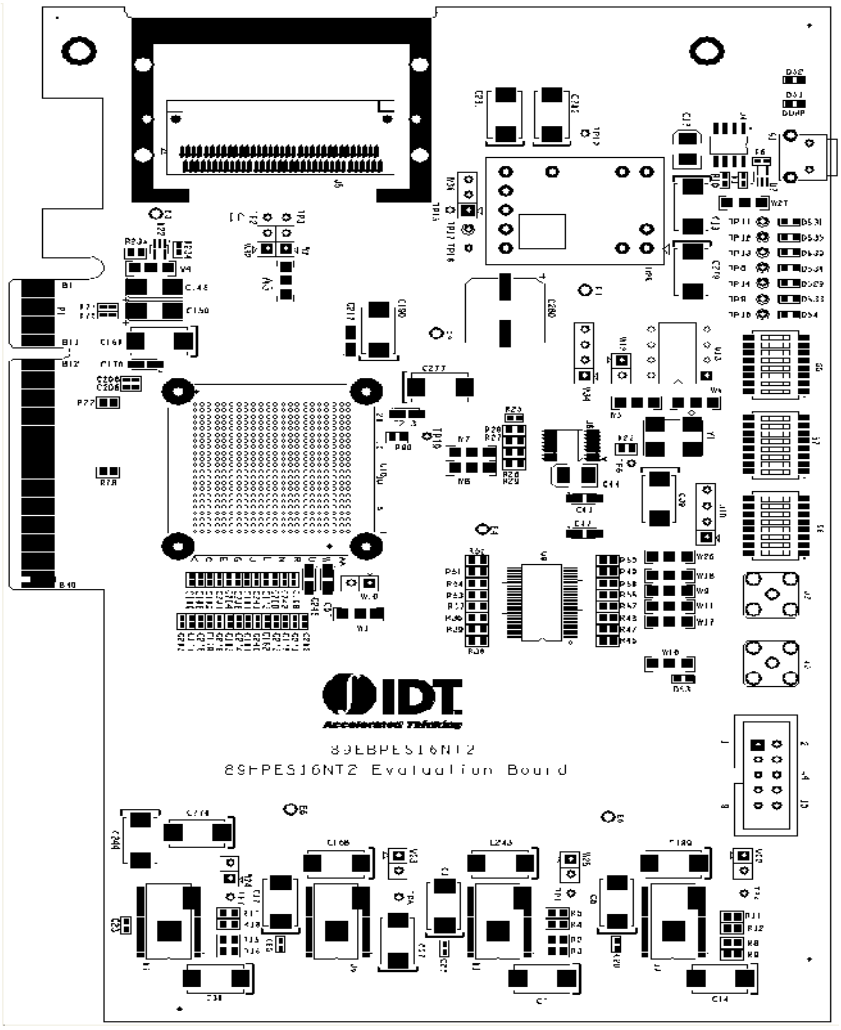
Table 2.13 PCI Express x8 Connector Definitions

Notes

Pin #	Signal	Description
A23	PETp4	Differential Pair
A24	PETn4	
A26	PETp5	Differential Pair
A27	PETn5	
A29	PETp6	Differential Pair
A30	PETn6	
A32	PETp7	Differential Pair
A33	PETn7	
B2	PERp0	Differential Pair
B3	PERn0	
B5	PERp1	Differential Pair
B6	PERn1	
B8	PERp2	Differential Pair
B9	PERn2	
B11	PERp3	Differential Pair
B12	PERn3	
B14	PWR	+3.3V Power
B15	PWR	+3.3V Power
B16	PWR	+3.3V Power
B17	PWR_RTN	Return for +3.3V Power
B18	PWR_RTN	Return for +3.3V Power
B19	PWER_RTN	Return for +3.3V Power
B20	CWAKE#	Power Management Signal for Wakeup Events
B21	CPERST#	Cable PERST#
B23	PERp4	Differential Pair
B24	PERn4	
B26	PERp5	Differential Pair
B27	PERn5	
B29	PERp6	Differential Pair
B30	PERn6	
B32	PERp7	Differential Pair
B33	PERn7	

Table 2.13 PCI Express x8 Connector Definitions

EB16NT2 Eval Board Figure



Notes

Software for the EB16NT2 Eval Board

Notes

Introduction

This chapter discusses some of the main features of the available software to give users a better understanding of what can be achieved with the EB16NT2 evaluation board using the device management software.

Device management software and related user documentation are available on a CD which is included in the Evaluation Board Kit. This information is also available on IDT's FTP site. For more information, contact IDT at ssdhelp@idt.com.

Device Management Software

The primary use of the Device Management Software package is to enable users of the evaluation board to access all the registers in the PES16NT2 device. This access can be achieved using the PCI Express in-band configuration cycles through the upstream port on the PES16NT2.

This software also enables users to save a snapshot of the current register set into a dump file which can be used for debugging purposes. An export/import facility is also available to create and use "Configuration" files which can be used to initialize the switch device with specific values in specific registers.

A conversion utility is also provided to translate a configuration file into an EEPROM programmable data structure. This enables the user to program an appropriate serial EEPROM with desirable register settings for the PES16NT2, and then to populate that EEPROM onto the Evaluation Board. It is also possible to program the EEPROM directly on the Evaluation Board using a feature provided by the software package.

The front end of the Device Management Software is a user-friendly Graphical User Interface which allows the user to quickly read or write the registers of interest. The GUI also permits the user to run the software in "simulation" mode with no real hardware attached, allowing the creation of configuration files for the PES16NT2 in the absence of the actual device.

Much of the Device Management Software is written with device-independent and OS-independent code. The software will be guaranteed to work on Linux (/sys interface) and MS Windows XP. It may function flawlessly on various flavors of MS Windows, but may not be validated on all. The fact that the software is device-independent assures its scalability to future PCIe parts from IDT. Once users are familiar with the GUI, they will be able to use the same GUI on all PCIe parts from IDT. This software is customized for each device through an XML device description file which includes information on the number of ports, registers, types of registers, information on bit-fields within each register, etc.

Notes

Schematics

Notes

Schematics

Page Number	Page Title
1	Table of Contents
2	Top level Block Diagram
3	Power Supplies
4	Clock Generation
5	89HPES16NT2 Top
6	89HPES16NT2 Ports
7	89HPES16NT2 Power
8	Port C Down-stream Interface
9	Port A Up-stream Interface

REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
STGC-0125R01	1.0	INITIAL RELEASE	2007-10-09	J.HU

02_DESIGN_TOP

TITLE: shasta 16NT2 eval board

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00124	18-642-000	1.0

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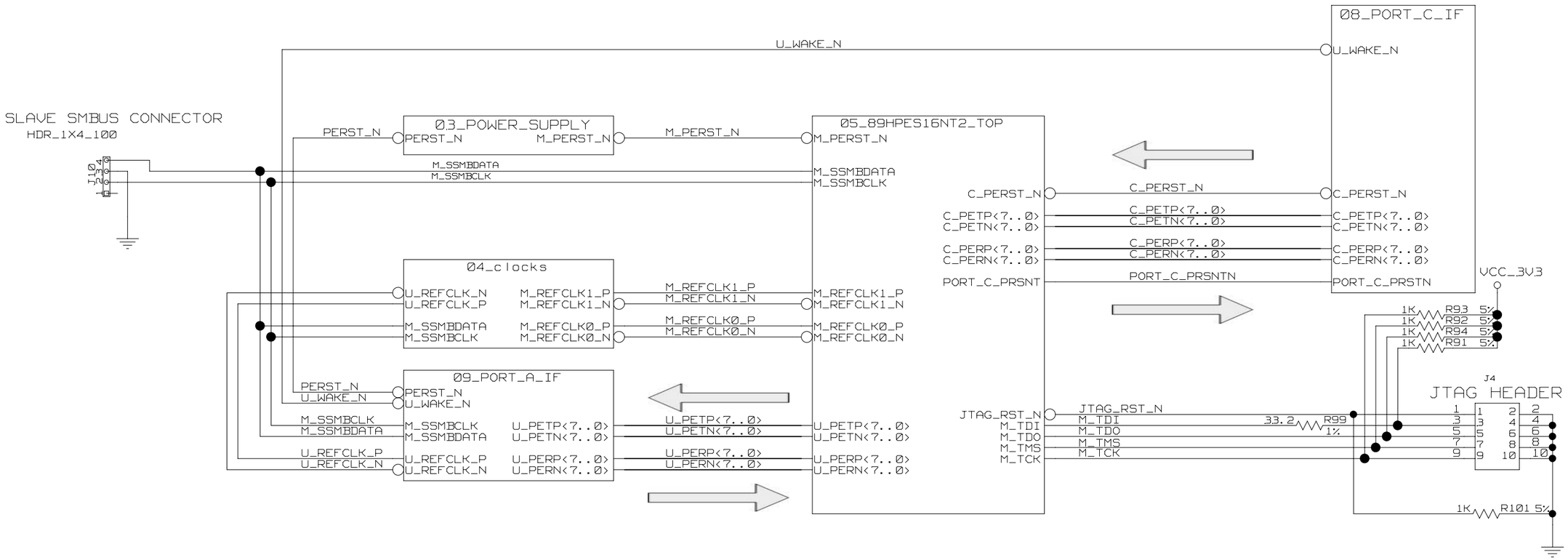

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TITLE: BLOCK DIAGRAM

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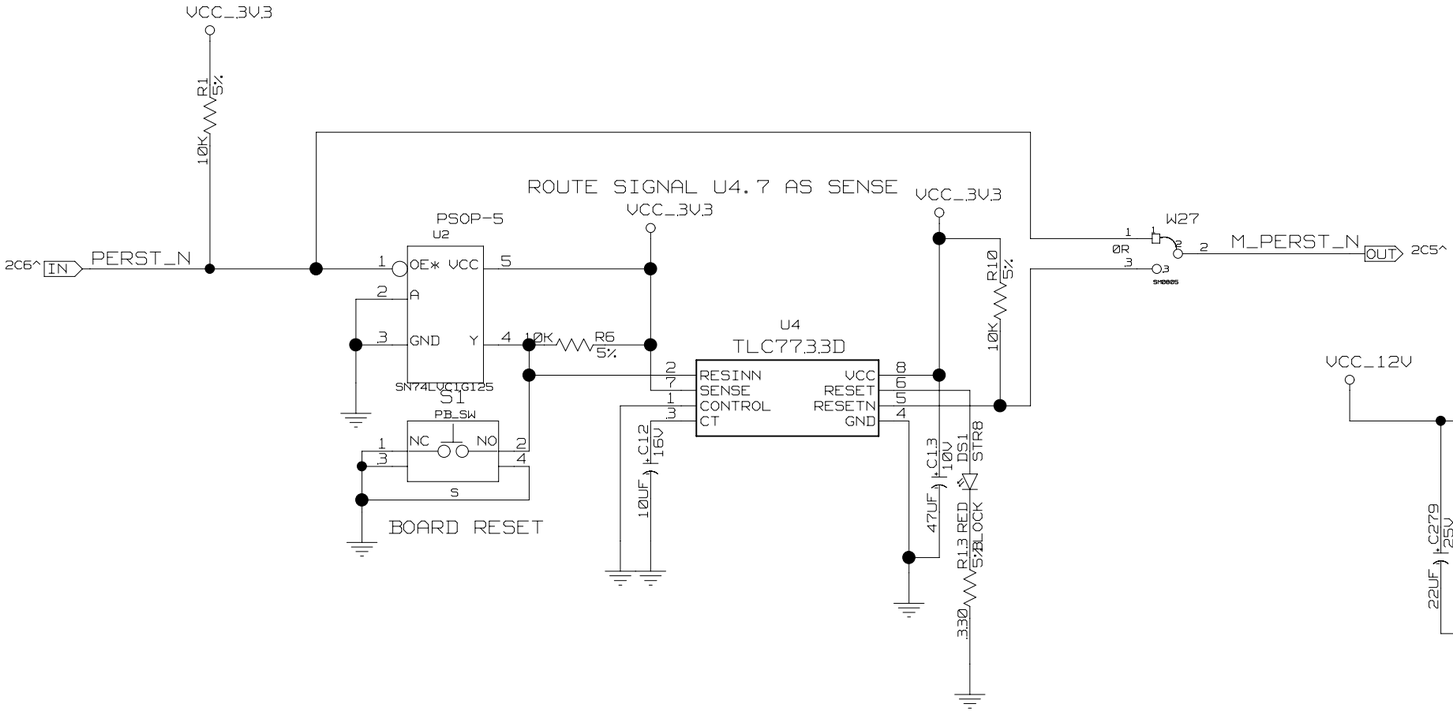
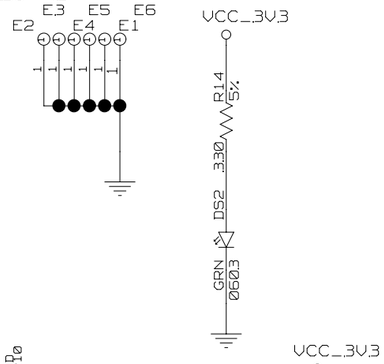
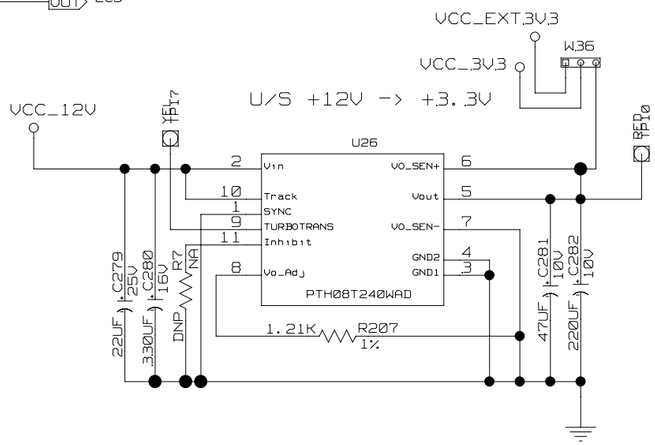
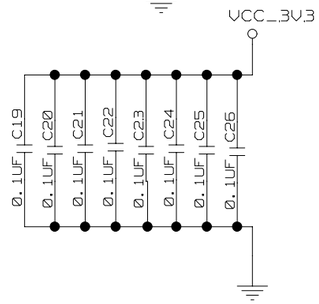
POWER INDICATOR
PLACE NEAR TOP EDGE
LABEL 'POWER'

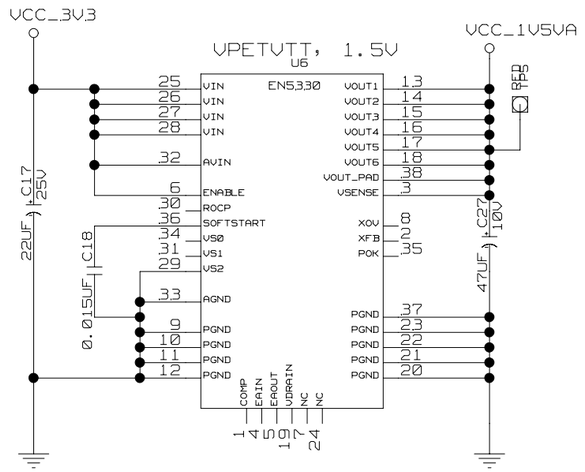
SACTTER ACROSS BOARD

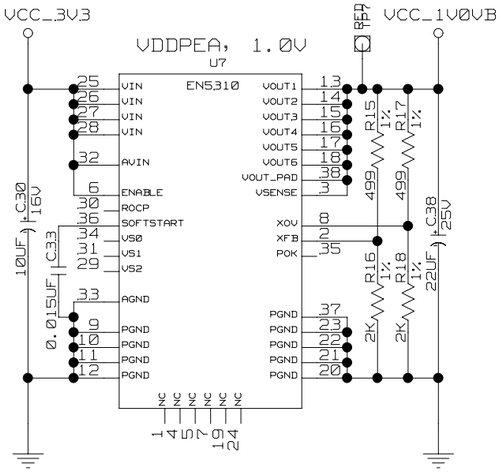


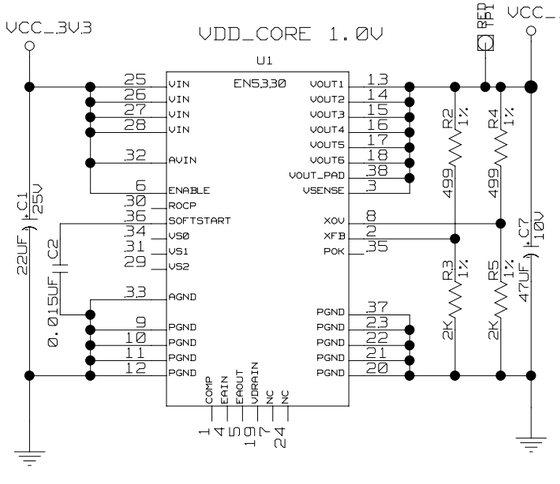


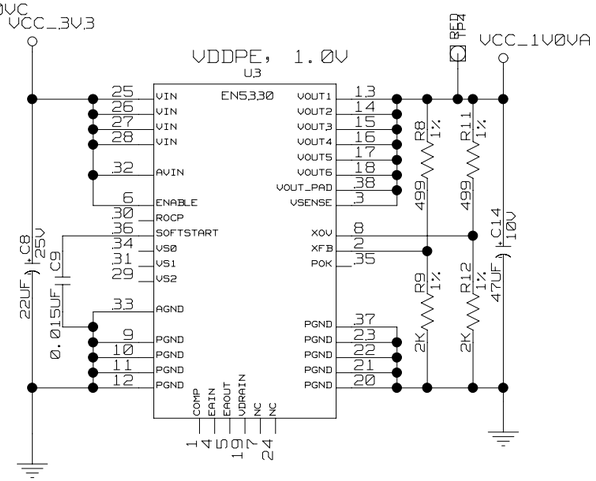












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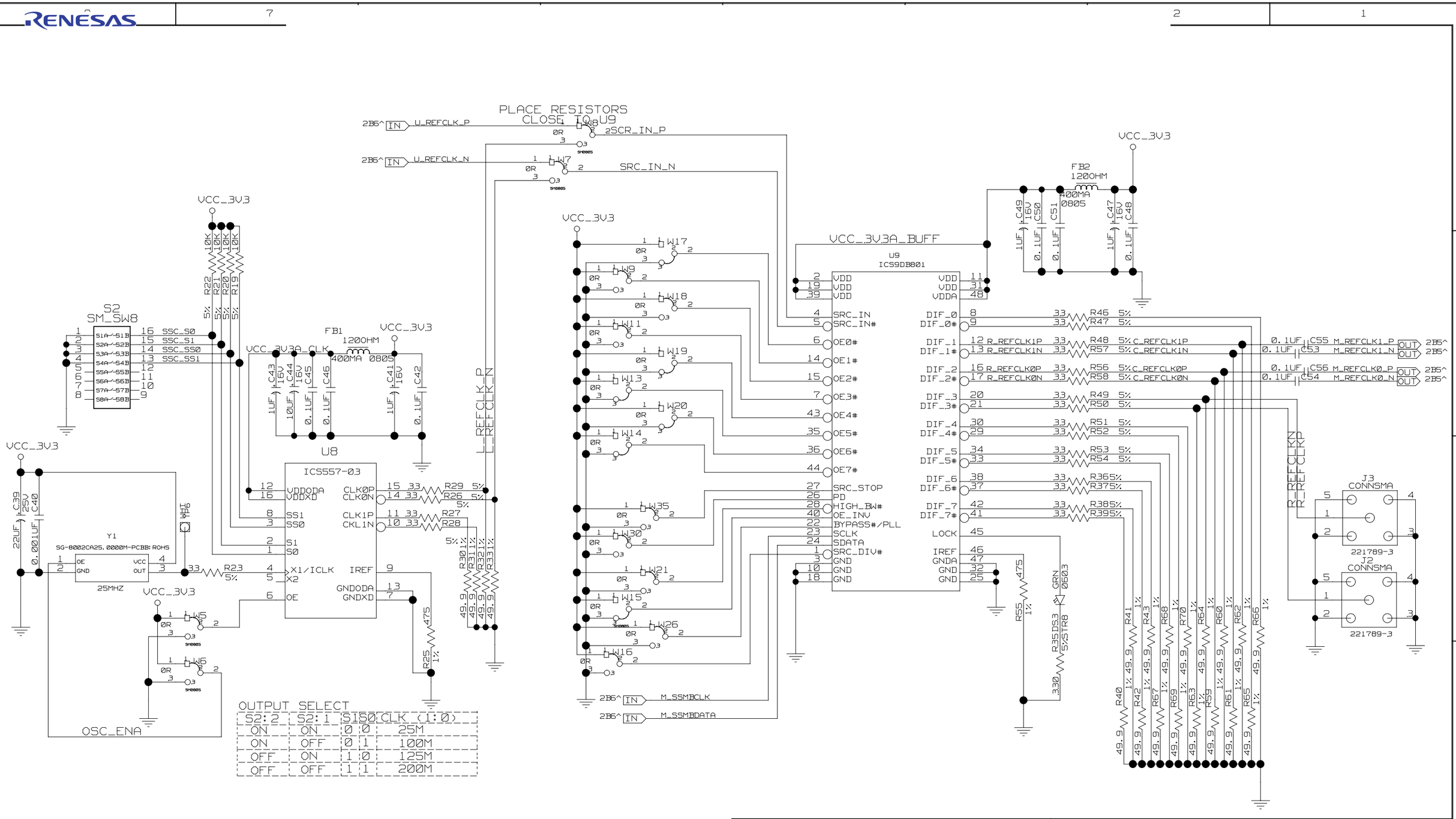
TITLE: POWER SUPPLY			
SIZE: B	DRAWING NO.: STGSCH-00124	FAB P/N: 18-642-000	REV.: 1.0
AUTHOR: jhu		CHECKED BY: B.LE	
Mon Jul 16 15:08:24 2007		PAGE 3 OF 9	



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SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00124	18-642-000	1.0

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06_89HPES16NT2_PORTS

07_89HPES16NT2_POWER

C_LREV
U_LREV

PORT A

U_PERP<7..0> IN 6C6v 2A5^ 6D6v
U_PERN<7..0> IN 6C6v 2A5^ 6D6v
U_PETP<7..0> OUT 2B5^ 6C4v 6D4v
U_PETN<7..0> OUT 2A5^ 6C4v 6D4v

PORT C

C_PERP<7..0> IN 6A6v 2B3^ 6B6v
C_PERN<7..0> IN 6A6v 2B3^ 6B6v
C_PETP<7..0> OUT 6B4v 2B3^ 6A4v
C_PETN<7..0> OUT 6B4v 2B3^ 6A4v

VCC_3V3

R95 2.7K 5%
R96 2.7K 5%
R100 2.7K 5%

PLACE EEPROM ON SOCKET

EEPROM
U13
24LC512
SCL SDA VCC WP A2 A1 A0 GND
5,3R-106,3-000

M_SCL
M_SDA
M_MSMBADDR3
M_MSMBADDR2
M_MSMBADDR1

HDR_1X4_100 W34

W12

R221 R225 R220 R224 R219 R223 R76 330 5%
DS31 DS35 DS30 DS34 DS29 DS33 DS4 GRN 060.3 STR8

M_PERST_N
C_PERST_N
M_PECRSTN
W3 W28 W31 W29 W33 0R

M_REFCLK1_P
M_REFCLK1_N
M_REFCLK0_P
M_REFCLK0_N

M_SSMBCLK
M_SSMBDATA
M_SSMBADDR5
M_SSMBADDR3
M_SSMBADDR2
M_SSMBADDR1

U10
Y21 PEREFCLKP1
Y22 PEREFCLKN1
P1 PEREFCLKP0
P2 PEREFCLKN0
AA19 REFCLKM
AB15 PERST_n
AA15 PENTBRST_n
Y15 RSTHALT
AB10 SSMBCLK
AA10 SSMBDAT
Y9 SSMBADDR_5
AA9 SSMBADDR_3
AB9 SSMBADDR_2
Y8 SSMBADDR_1
AB8 MSMBCLK
AA8 MSMBDAT
Y18 MSMBSMODE
Y7 MSMBADDR_4
AA7 MSMBADDR_3
AB7 MSMBADDR_2
Y6 MSMBADDR_1

GPIO_07 AA18 GPIO_7
GPIO_06 AB18 GPIO_6
GPIO_05_FAILOVERP Y17 U_FAILOVERP
GPIO_04_PCLINKUPN AA17
GPIO_03 AB17 GPIO_3
GPIO_02_PALINKUPN Y16
GPIO_01_PECRSTN AA16
GPIO_00 AB16 PORT_C_PRSNT IN 2B3^

JTAG_TCK AB5 M_TCK IN 2A3^
JTAG_TRST_n AA6 JTAG_RST_N IN 2B3^
JTAG_TMS AB6 M_TMS IN 2A3^
JTAG_TDI AA5 M_TDI IN 2B3^
JTAG_TDO Y5 M_TDO OUT 2A3^
W1 0R
CCLKUS Y10 M_TDO_BYPASS,3 M_CCLKUS
CCLKDS Y11 M_CCLKDS
SWMODE_3 AA14 M_SWMODE3
SWMODE_2 AB14 M_SWMODE2
SWMODE_1 Y13 M_SWMODE1
SWMODE_0 AA13 M_SWMODE0

S5
SM_SW8
S1A-S1B S2A-S2B S3A-S3B S4A-S4B S5A-S5B S6A-S6B S7A-S7B S8A-S8B
M_MSMBADDR4
M_MSMBADDR3
M_MSMBADDR2
M_MSMBADDR1
M_REFCLKM
M_RSTHALT
M_MSMBSMODE

10K R109 5%
10K R108 5%
10K R107 5%
10K R106 5%
10K R105 5%
10K R104 5%
10K R103 5%

VCC_3V3
R81 R82 R44 R45 R79 R71 R72 R73 10K 5%

S6
SM_SW8
S1B-S1A S2B-S2A S3B-S3A S4B-S4A S5B-S5A S6B-S6A S7B-S7A S8B-S8A

TITLE: 16NT2 DEVICE TOP

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00124	18-642-000	1.0

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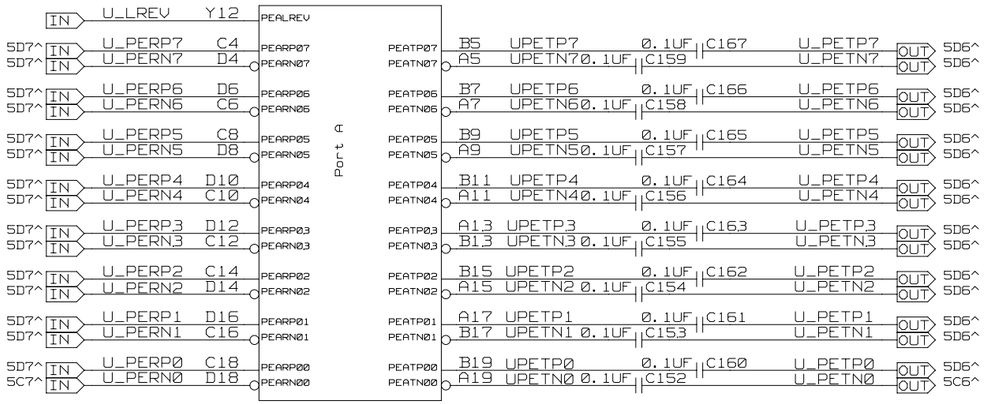
U10



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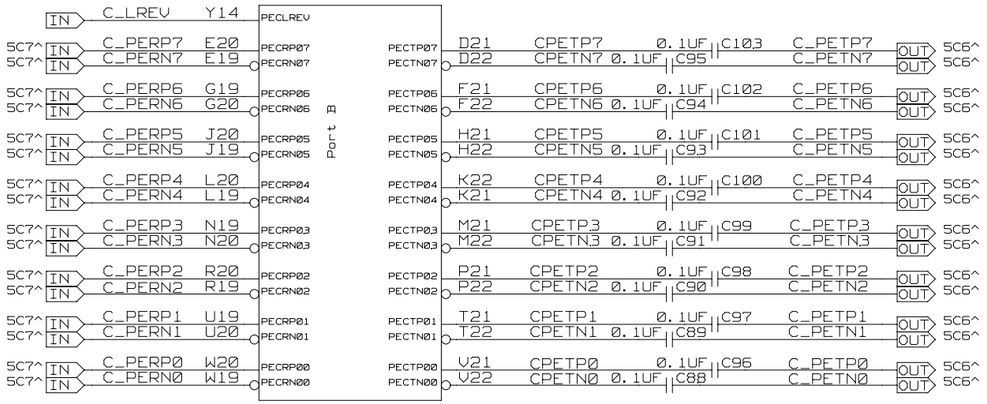

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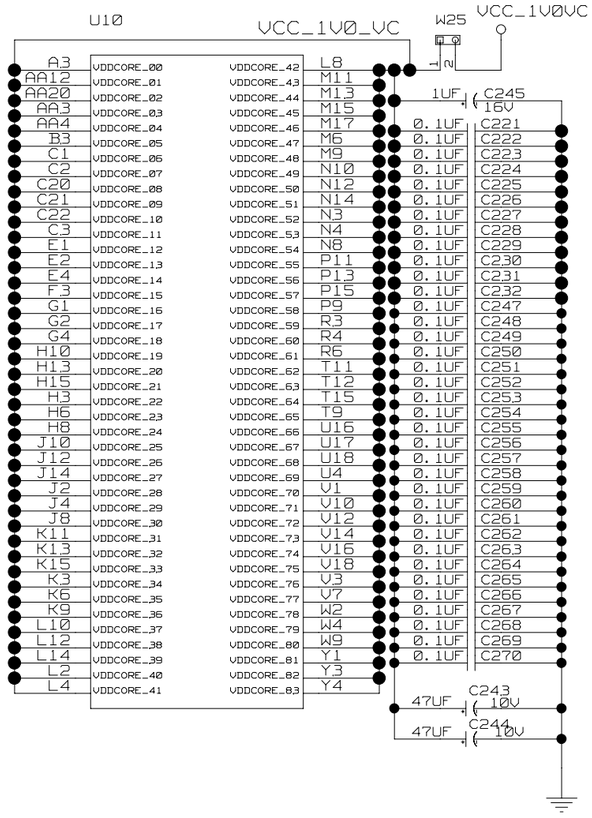
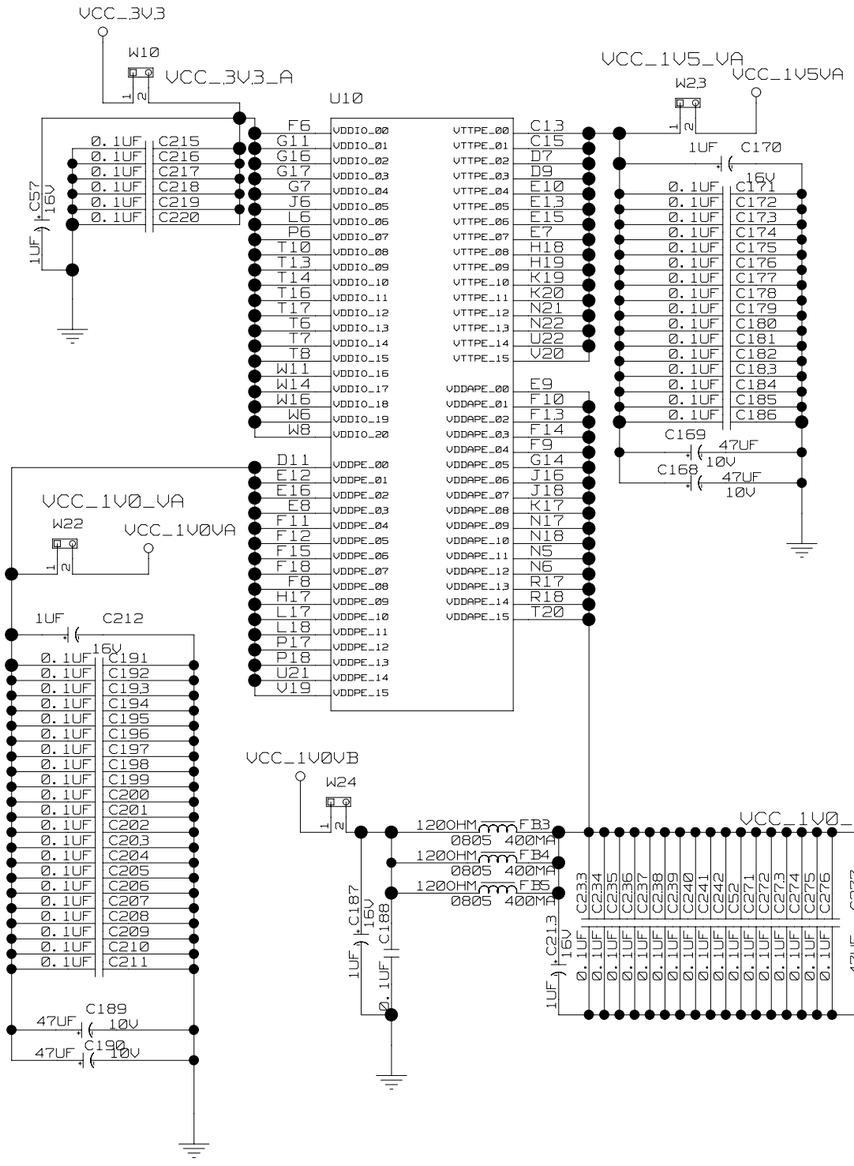
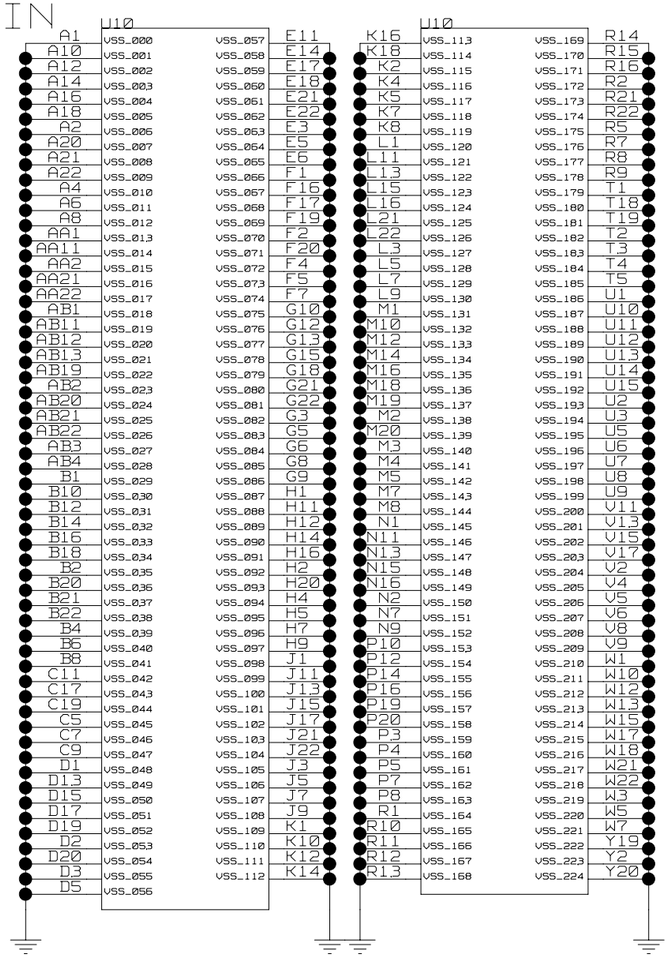
ROUTE CONNECTIONS TO W25 W10 W22 W23 W24 AS POWER 100 MILLS MIN







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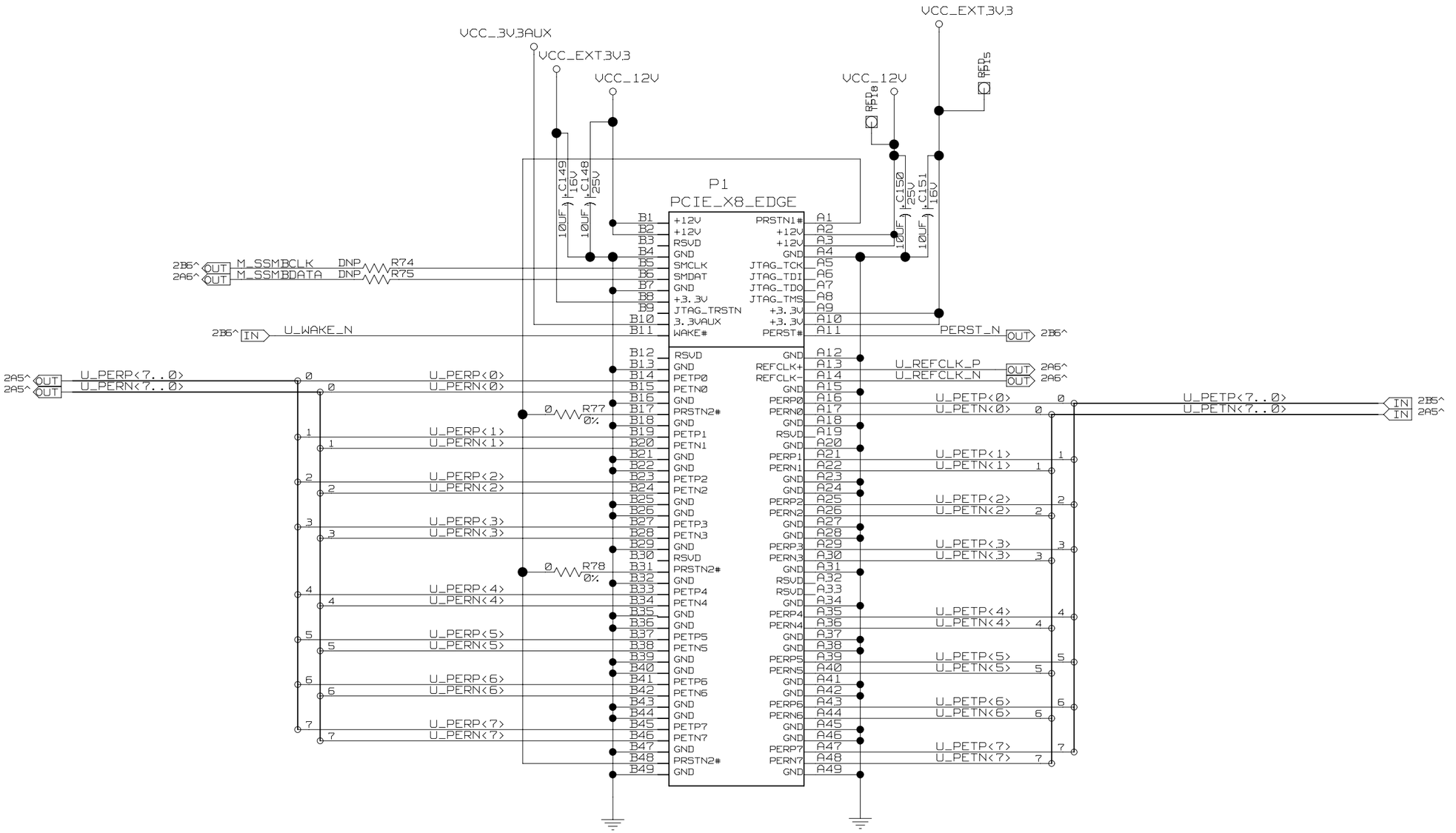

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TITLE: UPSTREAM CONNECTOR PORT A

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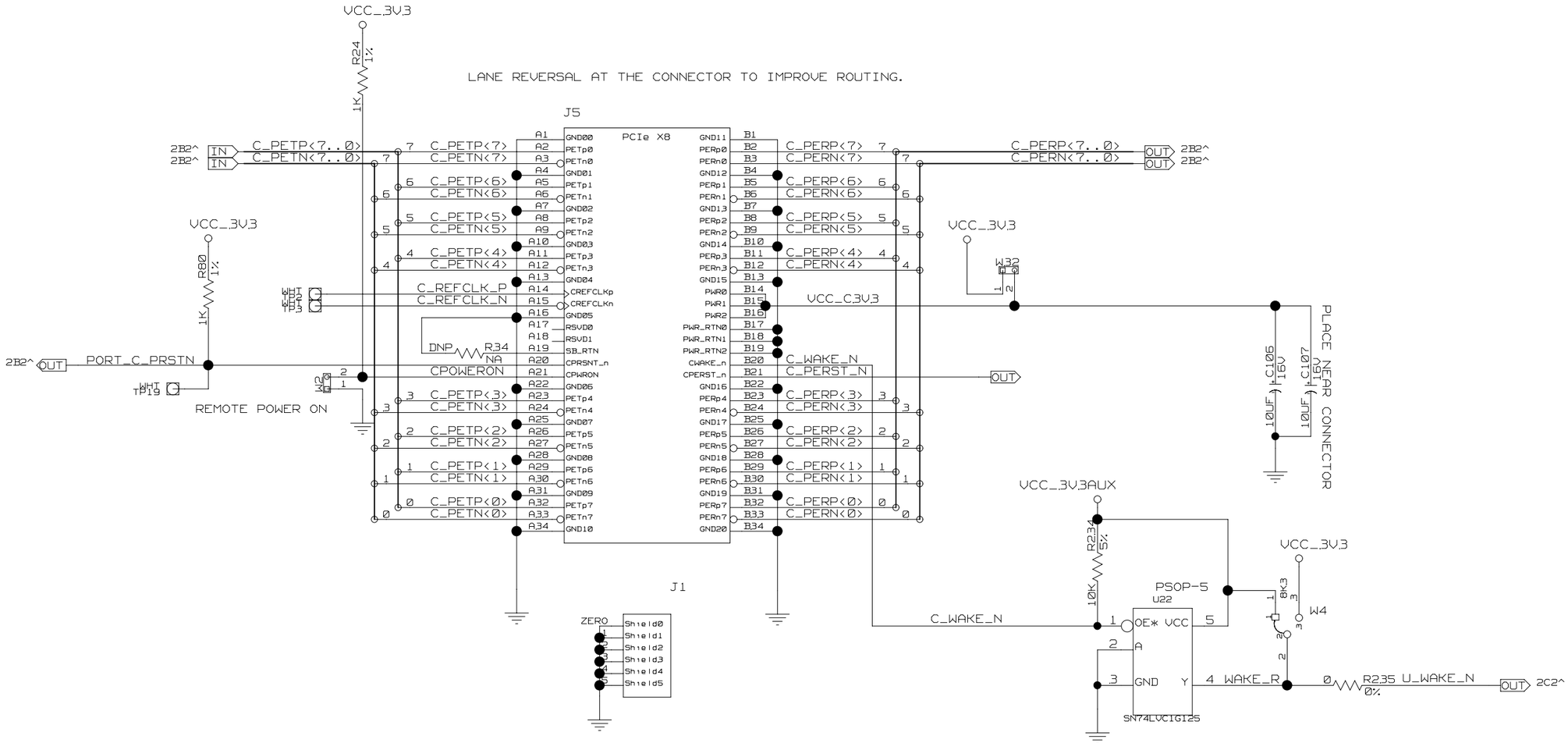

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TITLE: DOWNSTREAM CONNECTOR PORTC

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