IDT79S334A
Evaluation Board Manual

February 2001

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Description of IDT79S334A Evaluation Board

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Introduction

The IDT79RC32334 is a high performance integrated communications processor that combines IDT's RISCore32300 CPU core with system logic to control boot memory, main memory, I/O, and PCI. It also includes on-chip peripherals such as DMA channels, reset circuitry, interrupts, timers and UARTs. The RC32334 is a complete CPU subsystem for embedded designs.

The IDT79S334A Evaluation Board provides an RC32334 evaluation tool as well as a cost effective way to add I/O boards through the PCI interface. The 79S334A is a working example of a typical embedded PCI host/satellite system. This board is highly configurable and contains hardware options for various memory configurations.

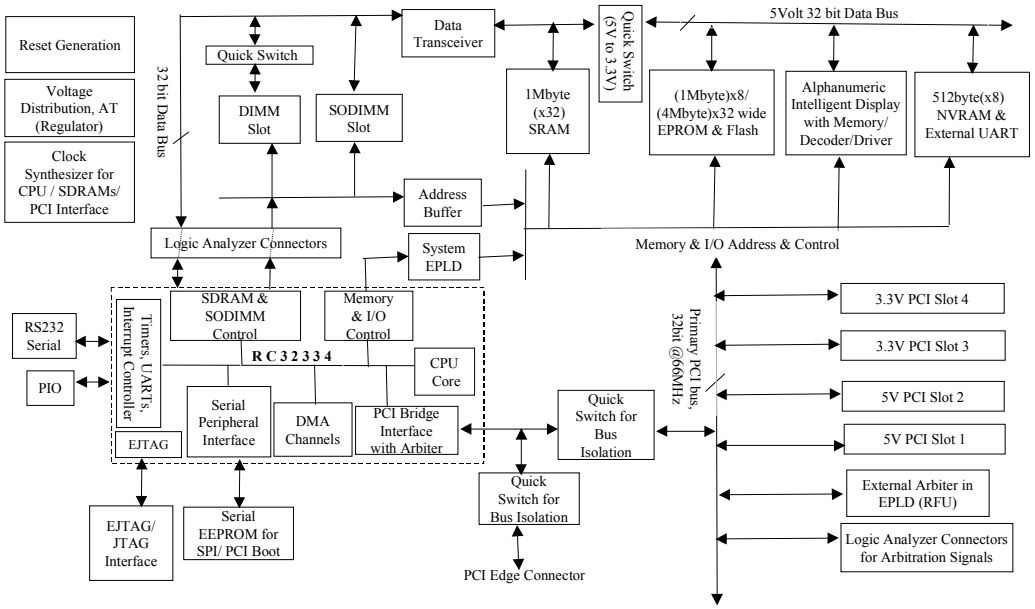


Figure 1.1 79S334A Evaluation Board Block Diagram

Revision History

July 2000: Initial publication.

September 5, 2000: New block diagram, revised schematics, PCI at 66 MHz, and various minor revisions.

January 26, 2001: Revised and re-organized Jumper and Switch Settings in Chapter 2.

February 9, 2001: Changed the Jumper numbers listed in the PIO Controller paragraph on page 3-3. Removed reference to "timers" in the same paragraph.

Notes

Overview of Features

Major features of the 79S334A Evaluation Board include:

- *Cost effective method of adding I/O boards through a PCI bus interface*
  - *4 PCI slots (two 5V—J14 and J15, two 3.3V—J16 and J17) for adding peripheral controllers. At any given instant, a maximum of two slots are available (J14 and J15 or J16 and J17).*
  - *1 PCI Edge connector*
- *EPROM 1 Mbyte*
- *SRAM 1 Mbyte*
- *SDRAM 32 Mbytes*
- *Serial EEPROM (Microwire NM93C46 and SPI AT 25256)*
- *Two on-chip serial I/O ports (16550 Compatible UARTs)*
- *External 85C30 Serial I/O Controller*
- *One 4 digit LED display*
- *512 Byte NVRAM*

Explanation of Features

IDT's S334A Evaluation Board is a complete working RC32334 system and is intended as an evaluation tool and software development platform that uses the high performance RC32334 RISController, which is based on IDT's proprietary RISCore32300 CPU core. The board requires a simple CRT video terminal or emulator and a 5-volt power supply with at least 10 AMP of current. A ±12-volt power supply is also needed to support the PCI bus requirements. The board contains four PCI slots for adding peripheral controllers.

The board contains 1 MB of EPROM. The on-board EPROM memory contains IDT's flexible System Integration Manager (IDT/sim), a debugging monitor that supports code downloading from the host system and I/O. Execution control commands include single stepping and instruction tracing, memory probing, register probing, line-based assembly and disassembly of code. Information on using IDT/sim is provided in a separate document that is available from the IDT web site **(www.idt.com)**.

The S334A evaluation board is constructed with both through-hole and surface mount devices on a 10 ¾" x 6 ½" PCB rectangular form factor board with standoffs and is intended for use as a stand-alone bench top device.

Specification Summary

Part Number

- *IDT79S334A Evaluation Board*

RISController

- *RC32334 RISController (256BGA)*

On-Board Memory Capacity

- *RISController CPU on-chip*
  - *Instruction Cache — 8kByte*
  - *Data Cache — 2kByte*
- *As shipped*
  - *SDRAM — 32MByte (144 pin SODIMM)*
  - *EPROM — 1MByte*
- *Maximum*
  - *SDRAM — 256MByte*
  - *EPROM — 4MB/Flash — 2 MB*
  - *SRAM — 1Mbyte*

Notes

Debug Monitor Flash
- *1 MByte higher density EPROM 27C080 support, containing IDT/sim*

Serial Ports
- *Controlled by 85C30 SCC controller*
- Two *RS232 DTE DB9P (9-pin male) connectors*
- *CRT video terminal connects to J19*
- *Software configurable features*
- *Default rate: 9600 Baud, 8 bits, no parity, 1 stop bit*

Interrupts
- *5 unsynchronized*

Physical Dimensions
- *Rectangular form factor:* 10 ¾" x 6 ½"

Operating Temperature
- *0-30°C*

Relative Humidity
- *5% - 50%*

Power Supply
- *5.0V ± 5%, 10 Amps typical*
- *± 12.0V ± 5%, required for PCI bus*

Flash
- *Cached/non-cached, single access*
  - *X8, X32 support*
  - *Non-interleaved*

SDRAM
- *Basic structure*
  - *144 pin SODIMM socketed (socket on board)*
  - *168 pin DIMM*
  - *PC100, 125 MHz / CL=2 component*
- *Configurations allowed*
  - *Either 144 pin SODIMM or 168 pin DIMM*
  - *Stays on page between transfers*

SRAM
- *Basic structure*
  - *Two 256 K x 16 devices*
  - *15 ns SRAM*
  - *Zero wait-state operation for block read and block write*

Programmable IO (PIO)
- *Input/Output/Interrupt source*
- *Individually programmable*

PCI Bus Interface
- *Revision 2.1 compliant*
- *Bus clock frequency up to 66 MHz*
- *Bus speed synchronizer from local system bus to PCI 66 MHz*

Notes

Installation of IDT79S334A Evaluation Board

Notes

79S334A Installation

This chapter discusses the steps required to install and boot the 79S334A Evaluation Board. The primary installation steps are as follows:

1. Connect a power source

   This involves connecting an external power supply to the board through J12.
2. Connect a video display terminal

   This involves connecting an RS232-C serial cable from a video terminal to the board through connector J19.
3. Insert the Ethernet adapter card in either J14 or J15 for Ethernet download
4. Configure jumper/switch options

   This involves altering the CPU reset initialization mode vector and changing the memory configuration. The board is shipped with the jumpers/switches set to their default configurations.
5. Run Software

   No additional software is required.
6. Boot IDT/sim

   When power to the board is turned on, the board's IDT/sim program boots and displays the start-up message.

Getting Started Quickly

The 79S334A board is shipped ready to run. Before the board is shipped, jumpers and switches are configured to the default settings shown in the tables below, and in general, they do not require further modification or setup.

Two basic requirements for the board to run are:

- *+5V power supply with at least 10 Amp of current*
- *±12V power supply to support the PCI bus requirements*

Video Terminal Requirements

The CRT video terminal can be a typical VT100 type/ANSI terminal, emulator, or PC running with 9600 baud, 8 data bits, no parity, and 1 stop bit. On the evaluation board, the RS232-C connector uses a male 9-pin DTE connector (J19) which uses the pins as shown in Table 2.12. For the default stand-alone mode, power to the board is provided by using a standard PC/AT power supply, available from a wide variety of computer equipment retailers.

Power Connector Type

The +5V power supply can be a typical PC compatible power supply. The J12 connector on the board uses the 12-pin power supply connector that mates with the two 6-pin power supply connectors on a standard PC power supply, as shown in Table 2.1.

Notes

Host Mode Power Connector (J12)

Use J12 power connectors for PCI Host mode. Use J13 power connector for PCI Satellite mode.

Pin	Definition	Color of Mating Connector Wire
1	—	Orange
2	—	Red
3	+12V	Yellow
4	-12V	Blue
5	Ground	Black
6	Ground	Black
7	Ground	Black
8	Ground	Black
9	—	White
10	+5V (vcc)	Red
11	+5V (vcc)	Red
12	+5V (vcc)	Red

Table 2.1 J12 Power Connectors

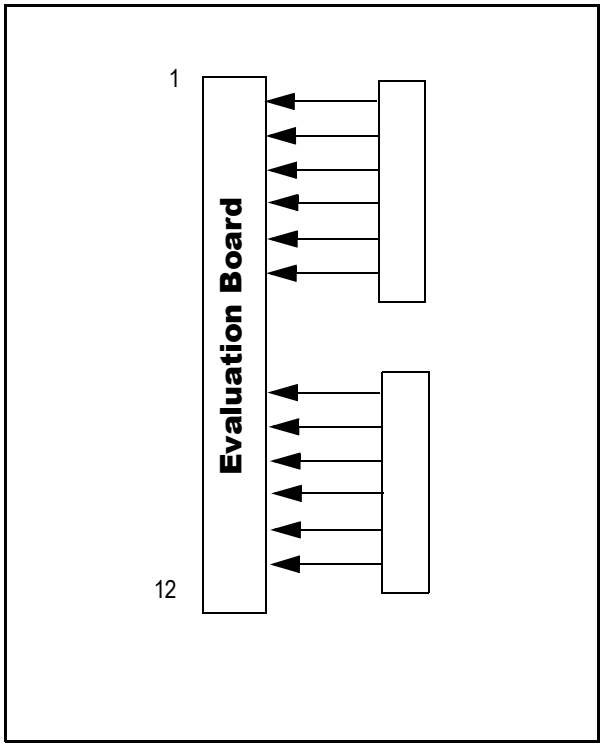


Figure 2.1 Diagram of 6-Pin Power Supply Connections to S334A Evaluation Board

Notes

Satellite Mode Power Connector (J13)

Use J13 power connectors for PCI Satellite mode. Use J12 power connectors for PCI Host mode.

Note: When connecting to J13, be sure to use a PC-AT compatible peripherals power source.

Pin	Definition	Color of Mating Connector Wire
1	+12V	Yellow
2	Ground	Black
3	Ground	Black
4	+5V	Red

Table 2.2 J13 Power Connectors

J11 (EJTAG Connector)

Pin number and signal definitions are provided in Table 2.3.

EJTAG Connector[1]		
Pin Number	**Name**	**Description**
1	TRST*	The TRST* pin is an active-low signal for asynchronous reset of the debug unit, independent of the processor logic.
3	TDI	On the rising edge of Tclk, serial input data are shifted into either the Instruction or Data register, depending on the TAP controller state. During Real Mode, this input is used as an interrupt line to stop the debug unit from Real Time mode and return the debug unit back to Run Time Mode (standard JTAG).
5	TDO	The TDO is serial data shifted out from instruction or data register on the falling edge of Tclk. When no data is shifted out, the TDO is tri-stated. During Real Time Mode, this signal provides a non-sequential program counter at the processor clock or at a division of processor clock.
7	TMS	The logic signal received at the TMS input is decoded by the TAP controller to control test operation. TMS is sampled on the rising edge of the TCLK.
9	TCLK	An input test clock, used to shift into or out of the Boundary-Scan register cells. Tclk is independent of the system and the processor clock with nominal 50% duty cycle.
11	RST*	Reset input, an active low signal for asynchronous reset of the entire target board.
13	PCST0	PC Trace Status Information 111 (STL) Pipe line Stall 110 (JMP) Branch/Jump forms with PC output 101 (BRT) Branch/Jump forms with no PC output 100 (EXP) Exception generated with an exception vector code output 011 (SEQ) Sequential performance 010 (TST) Trace is outputted at pipeline stall time 001 (TSQ) Trace trigger output at performance time 000 (DBM) Run Debug Mode During power-on reset (cold reset), PCST(2:0) serves as Mode Bit(2:0).
15	PCST1	
17	PCST2	

Table 2.3 J11 EJTAG Connector (Part 1 of 2)

Notes

EJTAG Connector[1]		
Pin Number	**Name**	**Description**
19	DCLK	Processor Clock. During Real Time Mode, this signal is used to capture address and data from the TDO signal at the processor clock speed, or any division of the internal pipeline. DCLK will be at 1/3 of the pipeline clock.
21	Debugboot	The Debugboot input is used during the reset and forces the CPU core to take a debug exception at the end of the reset sequence instead of a reset exception. This enables the CPU to boot from the ICE probe without having the external memory working. This input signal is level sensitive and is not latched internally.
23	Ref Vol	Power Status signal.

Table 2.3 J11 EJTAG Connector (Part 2 of 2)

1. All of the even numbered pins are ground pins.

JTAG Connector		
Pin Number	**Name**	**Description**
All Even	GND	
1	TRST*	The TRST* pin is an active-low signal for asynchronous reset of the debug unit, independent of the processor logic.
3	TDI	On the rising edge of Tclk, serial input data are shifted into either the Instruction or Data register, depending on the TAP controller state. During Real Mode, this input is used as an interrupt line to stop the debug unit from Real Time mode and return the debug unit back to Run Time Mode (standard JTAG).
5	TDO	The TDO is serial data shifted out from instruction or data register on the falling edge of Tclk. When no data is shifted out, the TDO is tri-stated. During Real Time Mode, this signal provides a non-sequential program counter at the processor clock or at a division of processor clock.
7	TMS	The logic signal received at the TMS input is decoded by the TAP controller to control test operation. TMS is sampled on the rising edge of the TCLK.
9	TCLK	An input test clock, used to shift into or out of the Boundary-Scan register cells. Tclk is independent of the system and the processor clock with nominal 50% duty cycle.

Table 2.4 J8 JTAG 10 Pin Connector

Memory Blocks

The DRAM Controller space is a maximum of 256 Mbytes that can be populated at any time with an SDRAM DIMM in the connector slot shown in Table 2.5.

Connector	Memory Type
U26	SRAM
U27	SRAM
U13	SDRAM DIMM
J3	SODIMM

Table 2.5 S334A Evaluation Board Memory Block Connector Locations

Notes

Jumper and Switch Settings

EPROM/Flash Selection

W1 to W7	Jumper / Setting							Description
	W1	W2	W3	W4	W5	W6	W7	
	Short between B and C	Short between A and B	Short between A and B	Short between A and B	Short between A and B	Short between A and B	Short between B and C	EPROM selected (Default)
	Short between A and B	Short between B and C	Short between B and C	Short between B and C	Short between B and C	Short between B and C	Short between A and B	Flash selected

Table 2.6 EPROM / Flash Setting

CPU Core/IO Supply

	CPU Core/IO Supply
W11 to W18	Jumpers are hard-wired to A and B. Provides 3.3V to core and IO

Table 2.7 CPU Core/IO Jumper / Settings

PCI Bus Arbitration Jumper/Setting

	Internal (Default)	External
W19	Open	Close
W21	Open	Close
W22	Short between B and C	Short between A and B
W23	Open	Close
W34	Short between B and C	Short between A and B

Table 2.8 PCI Bus Arbitration Jumper / Setting

Jumper Options

W8	**DMA Channel1** (Default—no jumper open)
	Short between A and B: External UART channel B W/REQ controls DMA Ready1
	Short between B and C: External UART channel B DTR/REQ controls DMA Ready1
W9	**DMA Channel0** (Default—no jumper open)
	Short between A and B: External UART channel A W/REQ controls DMA Ready0
	Short between B and C: External UART channel A DTR/REQ controls DMA Ready0

Table 2.9 Jumper Options (Part 1 of 2)

Notes

W10	**SDRAM DIMM**			
	Open: SODIMM (Default)			
	Close: Standard DIMM (Use 168-pin Std. DIMM in the SODIMM socket)			
W20	**CPU reset option**			
	Open: Standard reset to CPU (Default)			
	Close: Asserts permanent reset to CPU in case of JTAG testing (code not implemented in EPLD)			
W25	**EEPROM output selection**			
	Short A and B: Selects microwire serial EEPROM			
	Short B and C: Selects SPI serial EEPROM (Default)			
W26	**PCI mode selection**			
	Short A and B: PCI Satellite mode			
	Short B and C: PCI Host mode (Default)			
W27 to W34	**PIO bits 3 to 6 and 11 to 14 selection**			
	Close: Special function mode (UART) (Default)			
	Open: General purpose mode			
	Jumper	**Function**	**Setting**	**Description of Signal**
	W27	GPIO 15	Close (Default)	CTS for UART 0
			Open	General purpose
	W28	GPIO 03	Close (Default)	TX data for UART 1
			Open	General purpose
	W29	GPIO 12	Close (Default)	RTS for UART 0
			Open	General purpose
	W30	GPIO 13	Close (Default)	DTR for UART 0
			Open	General purpose
	W31	GPIO 04	Close (Default)	RX for channel 1
			Open	General purpose
	W32	GPIO 14	Close (Default)	DSR for channel 0
			Open	General purpose
	W33	GPIO 05	Close (Default)	TX for UART 0
			Open	General purpose
	W34	GPIO 06	Close (Default)	RX for UART 0
			Open	General purpose
W35	**PCI 66 MHz capability selection**			
	Close: 33 MHz capability (Default)			
	Open: Enable 66 MHz capability			
W36	**TAP control operation. JTAG probe controls the test operation of the TAP Controller.**			
	Short A and B: Selects 334 TAP control (Default)			
	Short B and C: Selects 364 TAP control			

Table 2.9 Jumper Options (Part 2 of 2)

Notes

Switch Settings (Mode bit selection)

S3-1, S3-2	**PCI boot mode selection**		
	S3-1	**S3-2**	**Description**
	On	On	Selects Boot from Memory Controller, Serial EEPROM not supported (Default)
	On	Off	Selects Boot from PCI, Serial EEPROM supported
	Off	On	Reserved
	Off	Off	Reserved
S3-3	**PCI Host/Satellite mode selection**		
	On		Host mode (Default)
	Off		Satellite mode
S3-4, S3-5	**Boot PROM port width selection**		
	S3-4 (mode bit 8)	**S3-5 (mode bit 9)**	**Port Width**
	On	On	8 bit (Default)
	On	Off	16 bit
	Off	On	32 bit
	Off	Off	RESV
S3-6	**Mode bit 7 selection (Reserved)**		
	Off (Default)		
S3-7	**CPU Timer interrupt enable/disable (Mode bit 6)**		
	On: Enable TimerInterrupt (Default)		
	Off: Disable Timer Interrupt		
S3-8, S2-1	**Mode bits 4 and 5 Reserved bits**		
	Both switches always on		
S2-2	**Big/Little endian selection (Mode bit 3)**		
	On: Little endian		
	Off: Big endian (Default)		

Table 2.10 Switch Settings (Part 1 of 2)

Notes

S2-3, S2-4, and S2-5	Clock multiplier selection			
	S2-3 (bit mode 0)	S2-4 (bit mode 1)	S2-5 (bit mode 2)	Clock multiplier
	On	On	On	X2 (Default)
	On	On	Off	X3
	On	Off	On	X4
	On	Off	Off	Reserved
	Off	On	On	Reserved
	Off	On	Off	Reserved
	Off	Off	On	Reserved
	Off	Off	Off	Reserved
S2-6, S2-7, and S2-8	Other switch settings (unused)			
	Always Off			

Table 2.10 Switch Settings (Part 2 of 2)

System Software - IDT/sim

EPROM on the 79S334A contains IDT's System Integration Manager (IDT/sim). IDT/sim is a software boot PROM debug monitor that provides functions for downloading software and for integrating hardware with software. Using IDT/sim, software can be downloaded onto the board from a SUN SPARCstation™ or a PC/AT personal computer.

IDT/sim source code can be acquired to support other I/O devices or change I/O addresses to fit their specific application: for example, to change from big-endian to little-endian addressing. The S334A board's default configuration is big-endian addressing. A copy of IDT/sim can be obtained through your local IDT sales representative.

> **Note:** IDT/sim provides two functions for measuring elapsed execution time: *timer_start()* and unsigned int *timer_stop()*. The function *timer_stop()* returns the number of microseconds elapsed since the most recent call to *timer_start()*. This functionality is independent of the system clock crystal specification on the majority of IDT evaluation boards. However, the IDT79S134 and IDT79S334A boards are exceptions. On these boards, the number of microseconds returned is accurate ONLY if the system clock crystal is 50 MHz. If a crystal with a different frequency is being used, say X MHz, you must multiply the result by 50/X to obtain the actual microseconds of elapsed time. All of the above is true for the "clock()" function supported by the Algorithmics C/C++ compiler shipped with the board.

Serial Port for CRT Video Terminal & Auxiliary Port

The 79S334A system board has four RS232 serial port connectors with pin assignments as shown in Table 2.11 and Table 2.12. The console port for the board is the DB9P connector designated as J2/J19[1] and must be set for a data rate of 9600 baud with 8 bits of data, no parity bit, and one stop bit. The J1/J18 auxiliary port is also a DB9P connector and is used for functions such as down loading software from a PC or SPARCstation™.

1. Based on SIM (for external/internal UART) the console will either be J2 or J19 (as shipped: J19).

Notes

SCC Port - A Console Connector J2		SCC Port - B Auxiliary Connector J1	
Pin	Signal	Pin	Signal
1	No connection	1	No connection
2	Txd (Output)	2	Txd (Output)
3	Rxd (Input)	3	Rxd (Input)
4	No connection	4	No connection
5	Ground	5	Ground
6	No connection	6	No connection
7	No connection	7	No connection
8	No connection	8	No connection
9	No connection	9	No connection

Table 2.11 J2/J1 Connector Pins and Signal Descriptions

79RC32334 UART - A Console Connector J19		79RC32334 UART- B Auxiliary Connector J18	
Pin	Signal	Pin	Signal
1	No connection	1	No connection
2	Txd (Output)	2	Txd (Output)
3	Rxd (Input)	3	Rxd (Input)
4	DSR (Input)	4	No connection
5	Ground	5	Ground
6	DTR (Output)	6	No connection
7	RTS (Output)	7	No connection
8	CTS (Input)	8	No connection
9	No connection	9	No connection

Table 2.12 J19/J18 Connector Pins and Signal Descriptions

Initialization and System Start-Up

System start-up is performed by turning the power supply on. If power to the board has already been supplied, then pressing the reset button will reinitialize the board. Three of the board's four LED displays indicate that the power has been successfully applied and one indicates the status of reset, as follows:

- ***DS1*** *indicates that the* ***Cold Reset*** *is* ***active*** *(Red)*
- ***DS2*** *indicates that the* ***2.5V*** *power supply is* ***ON*** *(Red)*
- ***DS3*** *indicates that the* ***3.3V*** *power supply is* ***ON*** *(Yellow)*
- ***DS4*** *indicates that the* ***5V*** *power is* ***ON*** *(Green)*

Notes

Once started, IDT/sim automatically boots and sizes the internal cache and main memory. The console is connected via the CRT serial port and a message indicating cache and memory sizes—similar to the one shown in Figure 2.2—will appear along with the first command line prompt. For more information on SIM commands, refer to the IDT/ sim User/Developer's Manual.

Note: Future upgrades will be assigned a different version number and date. **The starting address of the free memory space may differ slightly from the example shown** in Figure 2.2.

```
IDT System Integration Manager Ver. 9.0 May 2000
Copyright 1994-2000 Integrated Device Technology, Inc.

RC323xx CPU, 32-bit, Big Endian, MIPS-II, Write-Through cache
Console: 9600 baud
Instruction cache: 8 KB, Data cache: 2 KB
Memory Configuration: SDRAM only
Primary User Memory: 0XA009B2A8 to 0XA1FBFFFC. Size: 31888 KB
CAUTION: IDT/sim functions <timer_start> and <timer_stop> will work accurately only if the
crystal in socket U11 is 50 MHz. Higher (lower) rating will cause timer_stop to return higher
(lower) value!

    For HELP enter '?'

<IDT>
```

Figure 2.2 Initial Screen Display for the IDT/sim Debug Monitor

Logic Analyzer Connections

J4-6, J9, J20, J21 can be used to connect directly to an HP Logic Analyzer. The pin numbers and signal descriptions for each connector are listed in the following tables.

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	CPU_LA_CLK1	4	N.C.
5	N.C.	6	debug_cpu_ack_n
7	N.C.	8	mem_data[31]
9	N.C.	10	mem_data[30]
11	N.C.	12	mem_data[29]
13	N.C.	14	mem_data[28]
15	N.C.	16	mem_data[27]
17	N.C.	18	mem_data[26]
19	N.C.	20	mem_data[25]
21	N.C.	22	mem_data[24]
23	N.C.	24	mem_data[23]
25	N.C.	26	mem_data[22]
27	sdram_addr[21]	28	mem_data[21]
29	sdram_addr[20]	30	mem_data[20]
31	sdram_addr[19]	32	mem_data[19]

Table 2.13 Analyzer POD Connector J4 (Part 1 of 2)

Notes

Pin	Signal	Pin	Signal
33	sdram_addr[18]	34	mem_data[18]
35	sdram_addr[17]	36	mem_data[17]
37	sdram_addr[16]	38	mem_data[16]

Table 2.13 Analyzer POD Connector J4 (Part 2 of 2)

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	GND	4	N.C.
5	cpu_masterclk	6	debug_cpu_ads_n
7	sdram_addr[15]	8	sdram_we_n
9	sdram_addr[14]	10	sdram_s_n[1]
11	sdram_addr[13]	12	sdram_s_n[0]
13	sdram_addr[12	14	sdram_ras_n
15	sdram_addr[11]	16	sdram_cs_n[3]
17	sdram_addr[10]	18	sdram_cs_n[2]
19	sdram_addr[9]	20	sdram_cs_n[1]
21	sdram_addr[8]	22	sdram_cs_n[0]
23	sdram_addr[7]	24	sdram_cas_n
25	sdram_addr[6]	26	sdram_bemask_n[3]
27	sdram_addr[5]	28	sdram_bemask_n[2]
29	sdram_addr[4]	30	sdram_bemask_n[1]
31	sdram_addr[3]	32	sdram_bemask_n[0]
33	sdram_addr[2]	34	sdram_245_oe_n
35	sdram_addr[1]	36	sdram_cke_n
37	sdram_addr[0]	38	sdram_addr[12]

Table 2.14 Analyzer POD Connector J5

Pin	Signal	Pin	Signal
1	GND	2	N.C.
3	GND	4	N.C.
5	debug_cpu_i_d_n	6	debug_cpu_dma_n
7	mem_data_15	8	mem_we_n[3]
9	mem_data_14	10	mem_we_n[2]
11	mem_data_13	12	mem_we_n[1]
13	mem_data_12	14	mem_we_n[0]
15	mem_data_11	16	mem_oe_n
17	mem_data_10	18	mem_245_oe_n

Table 2.15 Analyzer POD Connector J6 (Part 1 of 2)

Notes

Pin	Signal	Pin	Signal
19	mem_data_9	20	mem_cs_n[5]
21	mem_data_8	22	mem_cs_n[4]
23	mem_data_7	24	mem_cs_n[3]
25	mem_data_6	26	mem_cs_n[2]
27	mem_data_5	28	mem_cs_n[1]
29	mem_data_4	30	mem_cs_n[0]
31	mem_data_3	32	cpu_coldreset_n
33	mem_data_2	34	cpu_nmi_n
35	mem_data_1	36	cpu_int_n[0]
37	mem_data_0	38	cpu_dt_r_n

Table 2.15 Analyzer POD Connector J6 (Part 2 of 2)

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	gnd	4	N.C.
5	ejtag_dclk	6	mem_wait_n
7	N.C.	8	N.C.
9	ejtag_pcst[2]	10	N.C.
11	ejtag_pcst[1]	12	N.C.
13	ejtag_pcst[0]	14	N.C.
15	ejtag_tms	16	N.C.
17	ejtag_debugboot	18	N.C.
19	jtag_tdi	20	dma_ready_n[1]
21	ejtag_tpc	22	dma_ready_n[0]
23	jtag_tms	24	uart_tx[1]
25	jtag_tck	26	uart_tx[0]
27	jtag_trst_n	28	uart_rx[1]
29	spi_miso	30	uart_rx[0]
31	spi_mosi	32	uart_dsr_n [0]
33	spi_ss_n	34	uart_dtr_n [0]
35	spi_sck	36	uart_rts_n [0]
37	timer_tc_n	38	uart_cts_n [0]

Table 2.16 Analyzer POD Connector J9

Notes

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	GND	4	N.C.
5	pci_clk	6	N.C.
7	pci_perr_n	8	pci_ad[15]
9	pci_serr_n	10	pci_ad[14]
11	pci_stop_n	12	pci_ad[13]
13	pci_par	14	pci_ad[12]
15	pci_cbe_n[3]	16	pci_ad[11]
17	pci_cbe_n[2]	18	pci_ad[10]
19	pci_cbe_n[1]	20	pci_ad[9]
21	pci_cbe_n[0]	22	pci_ad[8]
23	pci_lock_n	24	pci_ad[7]
25	pci_req_gnt_n[0]	26	pci_ad[6]
27	pci_req_n[2]	28	pci_ad[5]
29	pci_gnt_req_n[0]	30	pci_ad[4]
31	pci_gnt_n[2]	32	pci_ad[3]
33	pci_irdy_n	34	pci_ad[2]
35	pci_trdy_n	36	pci_ad[1]
37	pc_devsel_n	38	pci_ad[0]

Table 2.17 Analyzer POD Connector J20

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	GND	4	N.C.
5	pci_clk	6	N.C.
7	N.C.	8	pci_ad[31]
9	N.C.	10	pci_ad[30]
11	N.C.	12	pci_ad[29]
13	N.C.	14	pci_ad[28]
15	N.C.	16	pci_ad[27]
17	N.C.	18	pci_ad[26]
19	N.C.	20	pci_ad[25]
21	pci_gnt_n[1]	22	pci_ad[24]
23	pci_req_n[1]	24	pci_ad[23]
25	pci_intd_n	26	pci_ad[22]
27	pci_intc_n	28	pci_ad[21]

Table 2.18 Analyzer POD Connector J21 (Part 1 of 2)

Notes

Pin	Signal	Pin	Signal
29	pci_intb_n	30	pci_ad[20]
31	pci_inta_n	32	pci_ad[19]
33	N.C.	34	pci_ad[18]
35	N.C.	36	pci_ad[17]
37	N.C.	38	pci_ad[16]

Table 2.18 Analyzer POD Connector J21 (Part 2 of 2)

Theory of Operation and Design Notes

Notes

Introduction

This chapter provides information on the functional operation of the IDT79S334A evaluation board for the RC32334 integrated communications processor. For detailed schematics refer to Chapter 4. For detailed PLD equations, refer to Chapter 5.

Address Space Decoding

The physical addresses of the S334A board's resources are as listed in the tables that follow. The EPROM/FLASH, SRAM, Serial Communication Controller, NVRAM, LED display, and INTSTS subsystems can be accessed through selection of the Memory chip selects[0...5].

The memory_I/O controller includes the EPROM/FLASH subsystem, Serial I/O and SRAM subsystems. The **EPROM/FLASH** module is accessible through **mem_chipselect[0]**. The address ranges are shown in Table 3.1. Selection between EPROM or FLASH memory space is achieved through jumpers, as shown in Table 2.9 of Chapter 2.

		Address Range	Base Address	Base Mask
8 bit	EPROM	1FC0_0000 to 1FCF_FFFF	1FC0_0000	FFF0_0000
	FLASH	1FC0_0000 to 1FC7_FFFF	1FC0_0000	FFF8_0000
32 bit	EPROM	1FC0_0000 to 1FFF_FFFF	1FC0_0000	FFC0_0000
	FLASH	1FC0_0000 to 1FDF_FFFF	1FC0_0000	FFE0_0000

Table 3.1 EPROM/FLASH Address Mapping

The 85C30 **SCC** controller interfaces two RS232 connectors and is located at the fixed address space listed in Table 3.2, which is selected through **mem_chipselect[5]**. NVRAM is selected through **mem_chipselect[3]**, LED display through **mem_chipselect[4]** and Interrupt status through **mem_chipselect[2]**. The **SRAM** memory space is 1 Mbyte and is accessed through **mem_chipselect[1]** (see Table 3.3).

Description	Physical Address Locations	Chipset Select Allocation
ROM	1FC0_0000 – 1FFF_FFFF	mem_chipselect[0]
Flash	1FC0_0000 – 1FDF_FFFF	mem_chipselect[0]
SRAM	0400_0000 – 040F_FFFF	mem_chipselect[1]
DRAM (SDRAM)		
Bank 0 size is 16MB	0000_0000 – 00FF_FFFF	
Bank 1 size is 16MB	0100_0000 – 01FF_FFFF	
Bank 2 size is 16MB	0200_0000 – 02FF_FFFF	
Bank 3 size is 16MB	0300_0000 – 03FF_FFFF	
SCC (85C30)	1600_0000 – 17FF_FFFF	mem_chipselect[5]
79RC32334 Internal Registers	1800_0000 – 1BFF_FFFF	
LED_Display	1400_0000 – 15FF_FFFF	mem_chipselect[4]
NV_RAM	1200_0000 – 13FF_FFFF	mem_chipselect[3]
INT_Status	1000_0000 – 11FF_FFFF	mem_chipselect[2]

Table 3.2 Physical Address Mapping of 79S334 Board Resources

Notes

The **DRAM Controller** supports up to 256 Mbytes. At any time, either SODIMM or standard DIMM can be populated. Both sockets supports x64 DRAM DIMMs. Table 3.3 shows the SRAM and DRAM address locations when the SRAM option is selected. When SRAM is not selected, the address mappings are as shown in Table 3.4.

SRAM Selected, 32Mbyte DRAM SODIMM

SRAM Address Range		DRAM Address Range		DRAM Base Addresses	DRAM Mask Addresses
From	To	From	To	Banks 3:0	Banks 3:0
0000_0000	000F_FFFF	0100_0000	02FF_FFFF	0100_0000	FF00_0000
				0200_0000	
				0300_0000	
				0400_0000	

Table 3.3 SRAM/DRAM Address Range, 32Mbyte DRAM SODIMM

SRAM Not Selected, 32Mbyte DRAM SODIMM

DRAM Address Range		DRAM Base Addresses	DRAM Mask Addresses
From	To	Banks 3:0	
0000_0000	01FF_FFFF	0000_0000	FF00_0000
		0100_0000	
		0200_0000	
		0300_0000	

Table 3.4 DRAM Address Range, 32Mbyte DRAM SODIMM & SRAM Not Selected

LED_Display	
Clear display (read this port)	1400_0400
Digit 0	1400_000F
Digit 1	1400_0008
Digit 2	1400_0007
Digit 3	1400_0003

Table 3.5 LED_Display

NVRAM (512 Bytes)	
Base Addr for Read/Write	1200_0000
Base Addr for Recall/Store	1200_0400

Table 3.6 NVRAM (512 Bytes)

Notes

Interrupt Status	
Base Addr (read only):	1000_0000
Bit 0:	PCI_INT A #
Bit 1:	PCI_INT B #
Bit 2:	PCI_INT C #
Bit 3:	PCI_INT D #
Bit 4:	M66EN
Bit 5:	SCC_INT_N
Bit 6:	PCI_HOST_N
Bit 7:	UART_DCD_N

Table 3.7 Interrupt Status

The **PIO Controller** supports either 15-bit general purpose discrete I/O or specific peripheral functions. As general purpose discrete I/O pins, the controller supports I/O function such as micro wire serial EEPROM. Specific peripheral I/O functions such as on-chip UART data I/O pins, modem control, SPI, and DMA are also supported. Each of these functions are implemented through jumpers W8, W9, W25, and W27 through W34, as shown in Table 2.9. The address map of the PIO controller is shown in Table 3.8.

PIO Controller Address Mapping	
From	To
1800_0600	1800_0608

Table 3.8 PIO Controller Address Mapping

The **PCI bus interface** resources include a control core that provides a master and target controller that uses transmit and receive FIFO sizes of 8 words. The bus interface to the PCI core provides PCI bus arbitration selection, external bus request and bus grant modes, internal RC32334 arbiter mode with fixed and round robin priority selections, mailbox registers, and software programmable endianness (selectable per memory block). The internal address map for the PCI interface is shown in Table 3.9. The address mapping for these registers is shown in Table 3.10.

From	To	Allocation
1800_2000	1800_2FFF	Internal registers (4KB)
1880_0000	188F_FFFF	PCI I/O Space (1MB)
18C0_0000	18FF_FFFF	Memory space 3 (4MB) (for non-pci boot reset option)
1FC0_0000	1FFF_FFFF	Memory space 3 (4MB) (for pci boot reset option)
4000_0000	5FFF_FFFF	Memory Space 1 (512MB)
6000_0000	7FFF_FFFF	Memory Space 2 (512MB)

Table 3.9 PCI Interface Address Ranges and Definitions

Notes

Address	Registers
1800_05B0	PCI Controller Interrupt Pending Register 11
1800_05B4	PCI Controller Interrupt Mask Register 11
1800_05B8	PCI Controller Interrupt Clear Register 11
1800_05C0	PCI Satellite Mode Mailbox Interrupt Pending Register 12
1800_05C4	PCI Satellite Mode Mailbox Interrupt Mask Register 12
1800_05C8	PCI Satellite Mode Mailbox Interrupt Clear Register 12
1800_05D0	PCI to CPU Mailbox Interrupt Pending Register 13
1800_05D4	PCI to CPU Mode Mailbox Interrupt Mask Register 13
1800_05D8	PCI to CPU Mailbox Interrupt Clear Register 13
1800_20B0	PCI Memory Space 1 Base Register
1800_20B8	PCI Memory Space 2 Base Register
1800_20C0	PCI Memory Space 3 Base Register
1800_20C8	PCI I/O Space Base Register
1800_20E0	PCI Arbitration Register
1800_20E8	PCI Host Memory Space 1 Base Register
1800_2100	PCI Host IO space Base Register
1800_2CF8	PCI Configuration Address Register
1800_2CFC	PCI Configuration Data Register

Table 3.10 PCI Register Map

Four general purpose **DMA channels**[1] move data between source and destination resources such as system memory, PCI or external I/O devices (8-, 16-, or 32-bit I/O devices are treated as memory-mapped word-aligned devices). Using a flexible, memory-based descriptor structure, any of the four channels efficiently supports “scatter/gather” capability.

The RC32334 DMA supports byte, half-word (16-bit), word, and quad-word burst transfers that cross-over quad-word boundaries and are automatically split into single-word transfers until a quad-word boundary is reached. The DMA controller also automatically prevents burst transfers from crossing page boundaries and supports little- or big-endian data conversions. DMA restrictions include:

- *When the source or destination address is constant (as in I/O devices), it must be word aligned.*
- *DMA is not supported for internal UART.*

Note that the following transfers are not supported:

- *Source is incremented and destination is decremented*
- *Source is decremented and destination is incremented.*

Additional information on DMA operations is located in the RC32334/RC32332 User Reference Manual.

1. DMA channels 3 and 4 do not have the DMA_RDY pins and cannot be used to perform DMA transfers with slow I/O devices.

Notes

Register Address Maps for DMA Channels 0-3

Base Address Channel 0	Register Name	Offset Address	Effective Address Channel 0
1800_1400	Configuration Register	00	Base + Offset
	Base Descriptor Register	04	
	Current Address Register	08	
	Status/Block Size Register	10	
	Source Address Register	14	
	Destination Address Register	18	
	Nest Descriptor Address Register	1C	

Table 3.11 DMA Channel 0 Register Mapping

Base Address Channel 1	Register Name	Offset Address	Effective Address Channel 1
1800_1400	Configuration Register	40	Base + Offset
	Base Descriptor Register	44	
	Current Address Register	48	
	Status/Block Size Register	50	
	Source Address Register	54	
	Destination Address Register	58	
	Nest Descriptor Address Register	5C	

Table 3.12 DMA Channel 1 Register Mapping

Base Address Channel 2	Register Name	Offset Address	Effective Address Channel 2
1800_1900	Configuration Register	00	Base + Offset
	Base Descriptor Register	04	
	Current Address Register	08	
	Status/Block Size Register	10	
	Source Address Register	14	
	Destination Address Register	18	
	Nest Descriptor Address Register	1C	

Table 3.13 DMA Channel 2 Register Mapping

Notes

Base Address Channel 3	Register Name	Offset Address	Effective Address Channel 3
1800_1900	Configuration Register	40	Base + Offset
	Base Descriptor Register	44	
	Current Address Register	48	
	Status/Block Size Register	50	
	Source Address Register	54	
	Destination Address Register	58	
	Nest Descriptor Address Register	5C	

Table 3.14 DMA Channel 3 Register Mapping

The **Expansion Interrupt Controller** extends the CPU's CP0 interrupt control by collating the RC32334 generated interrupts into a single CPU interrupt. When a general purpose interrupt is received, the Interrupt Service Routine (ISR) first saves CPU registers, checks its Cause Register and then checks its Pending Interrupt Register. If the pending interrupt is from the RC32334, then the ISR checks the Expansion Interrupt Controller Pending Interrupt Register. After treating/noting the interrupt condition, the ISR resets the pending interrupt by writing to the corresponding bit in the Expansion Interrupt Clear Register. The ISR can then exit by restoring the CPU register and executing an RFE instruction. The register address mapping for the Expansion Interrupt Controller is shown in Table 3.15.

Expansion Interrupt Controller Address Mapping	
From	To
1800_0500	1800_05e8

Table 3.15 Expansion Interrupt Controller Address Mapping

The RC32334 has eight on-chip **Timers**: Three general purpose timers and five timers that are optionally dedicated to Watchdog, CPU bus time-out, IP bus time-out, DRAM refresh, and WarmReset. Beginning from zero, these eight system timers count on each system clock, timing out after reaching a programmable compare value and resetting to zero automatically. Uses for these timers include real-time clock, cascaded real-time clock and time-slice clock. The register address mapping for the Timer controller is shown in Table 3.16. Additional information on the functional aspects of these timers is located in the RC32334/RC32332 User Reference Manual.

Timer Controller Address Mapping	
From	To
1800_0700	1800_0778

Table 3.16 Timer Controller Address Mapping

The two 16550 UARTs are an enhanced version of the 16450 UART. Functionally the same as a 16450 at power-up, these UARTs can be put into the 16550 mode, which then relieves the CPU of software overhead. This feature allows execution of 16450 or 16550 compatible software. Two sets of 16-byte buffers are enabled during the 16550 mode: one set in the receive data path and one set in the transmit data path.

The CPU can read the UART status at any time during operation. Status information includes the type and condition of the transfer operation, as well as any error condition (parity, overrun, framing, or break interrupt). A baud rate generator is included that divides down the system clock by 1 to 65K. The baud rate generator provides the 16X clock for driving the transmitter and receiver logic.

Notes

The UART controller provides fully programmable serial characteristics such as 5, 6, 7, or 8-bit characters; even, odd, or no parity bit generation and detection; and 1, 1-1/2, or 2 stop bit generation. The register address mapping for the UART Controller is shown in Table 3.17.

UART Controller Address Mapping	
From	To
1800_0800	1800_083C

Table 3.17 UART Controller Address Map

Interrupts

Both the on-board and PCI bus interface interrupts are assigned to the CPU as shown in Table 3.18.

Interrupts	32334
INT0*	Scc (85C30) INTR
INT1*	PCI Bus INTA# OR PCI Bus INTB# OR PCI Bus INTC# OR PCI Bus INTD#
INT2*	PCI Bus INTB#
INT4*	PCI Bus INTC#
INT5*	PCI Bus INTD#
NMI*	High (Unused)

Table 3.18 CPU Interrupt Assignment for S334A Board

Notes

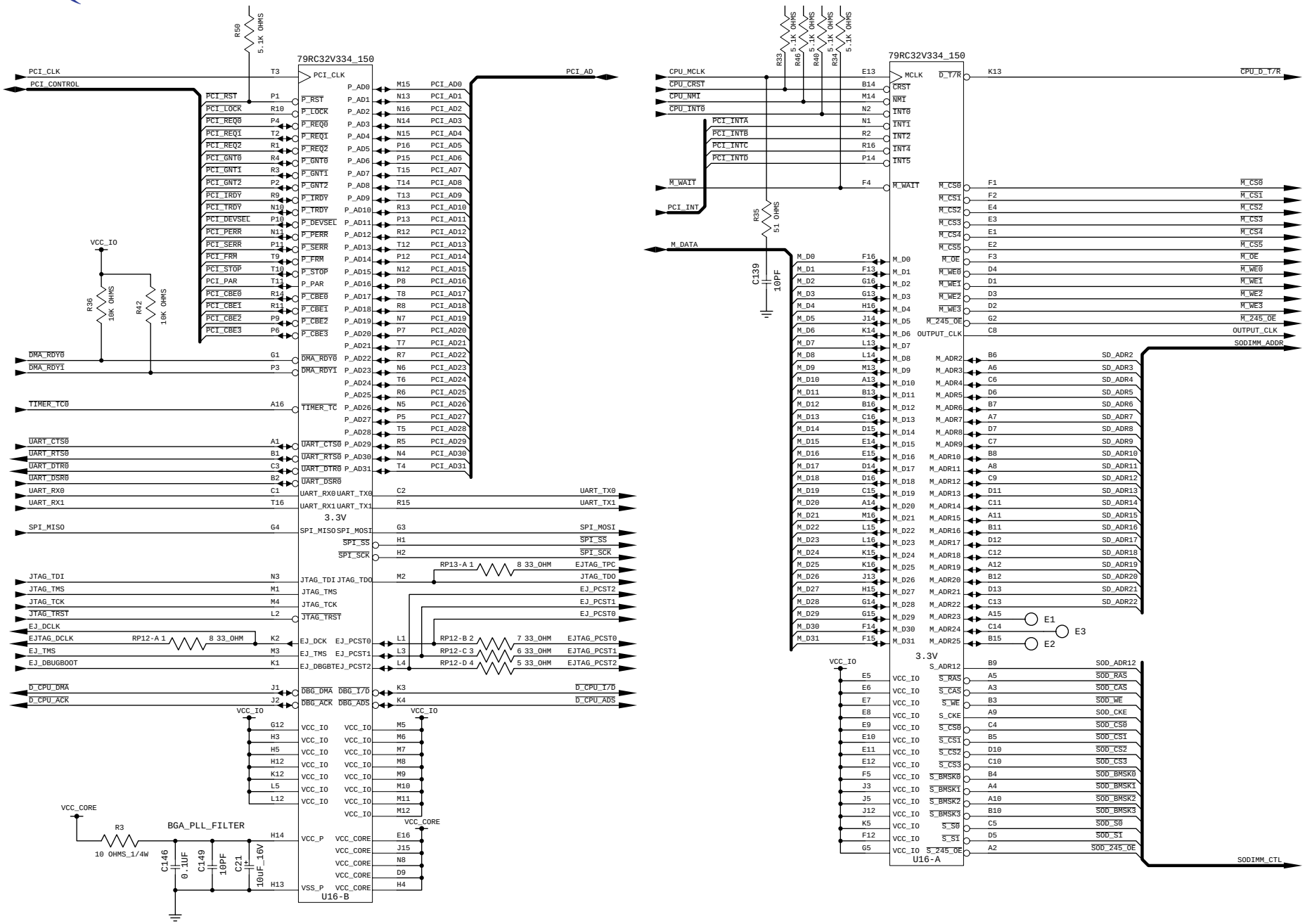
Schematics

Notes

Schematics

SH	DESCRIPTION
1	79RC32334
2	79RC32332
3	SODIMM
4	SDRAM QUICKSWITCHES
5	SDRAM DIMM
6	CLOCKS, RESET, CONFIGURATION SWITCHES
7	JTAG, EJTAG, EEPROM, INTERNAL UART
8	CPU LOGIC ANALYZER CONNECTORS
9	PCI LOGIC ANALYZER CONNECTORS
10	PCI SLOT QUICKSWITCHES
11	PCI EDGE CONNECTOR QUICKSWITCHES
12	PCI SLOT 1
13	PCI SLOT 2
14	PCI SLOT 3
15	PCI SLOT 4
16	PCI EDGE CONNECTOR
17	DATA, ADDRESS BUFFERS
18	EPLD
19	SRAM
20	EPROM/FLASH MEMORY
21	DISPLAY, NVRAM, EXTERNAL UART
22	POWER SUPPLY
23	BYPASS CAPACITORS

SHEET TITLE:	TABLE OF CONTENTS
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 0 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
DRAWN BY:	J.A./GAIL SWAMI



RC32334-BGA

SHEET TITLE:	79RC32334
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 1 OF 23
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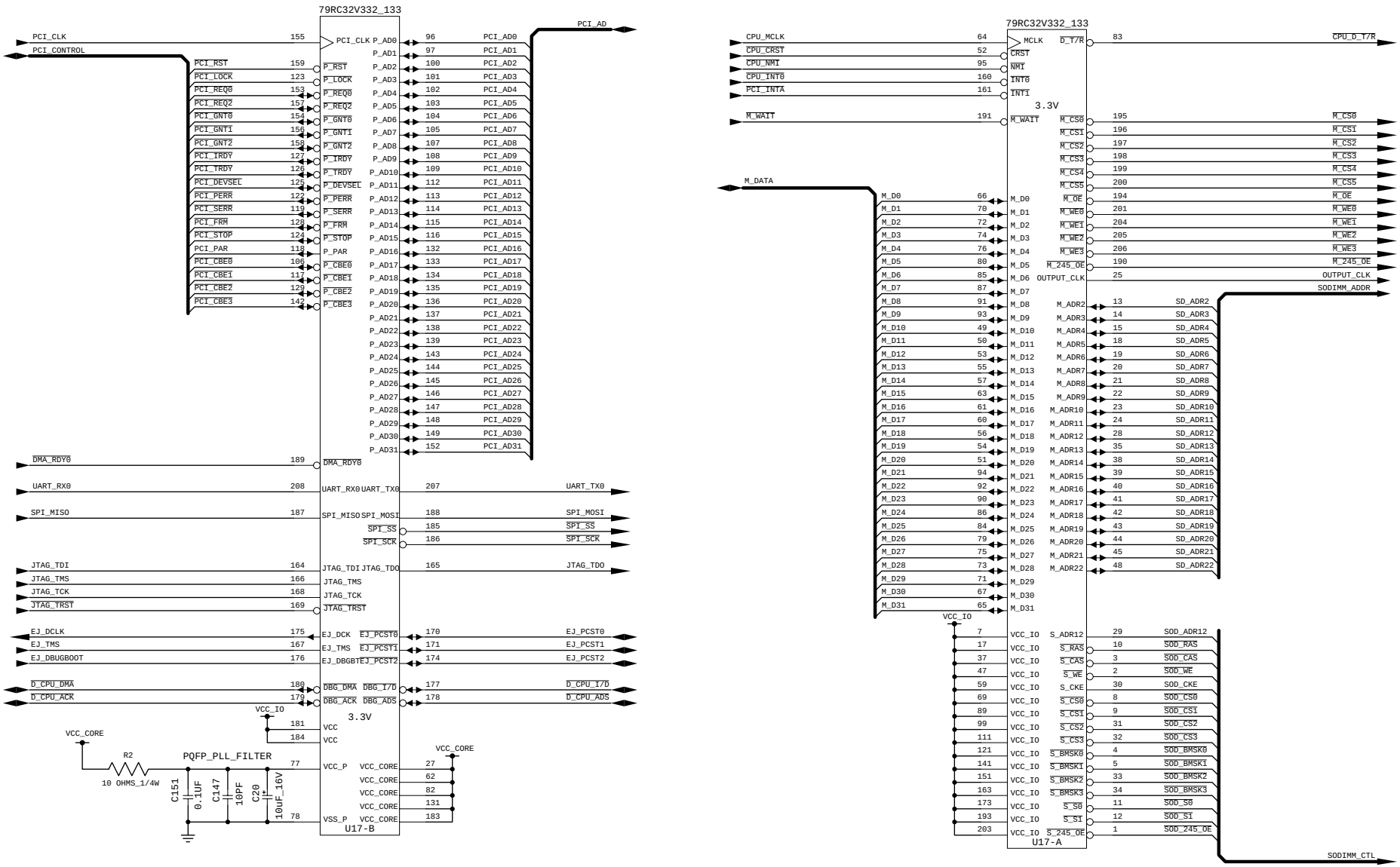

RC32332-PQFP

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PROJECT TITLE:	79S332/79S334A EVAL BD
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PART NUMBER:	400-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
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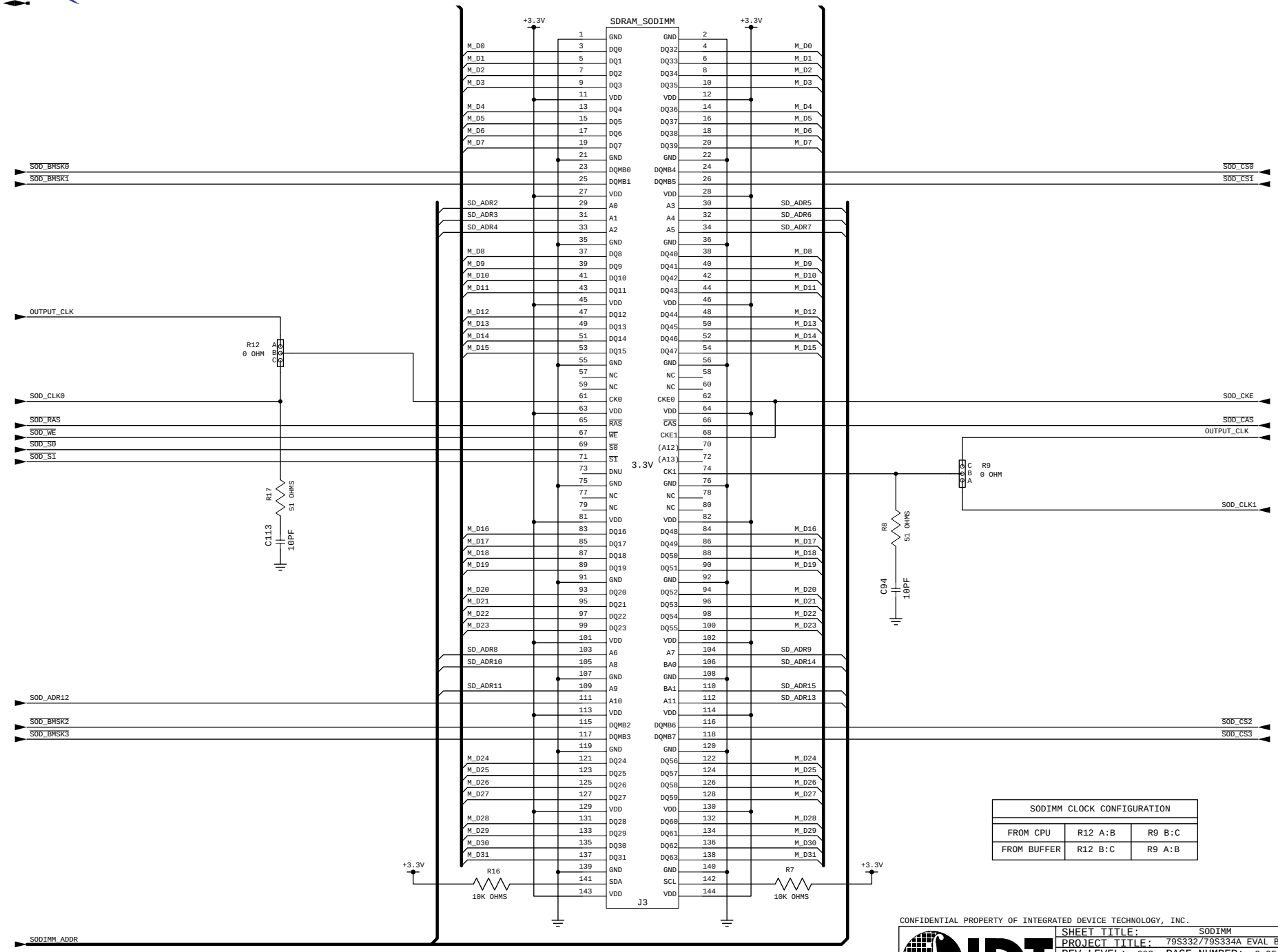

SODIMM CLOCK CONFIGURATION		
FROM CPU	R12 A:B	R9 B:C
FROM BUFFER	R12 B:C	R9 A:B

SODIMM INTERFACE

SHEET TITLE:	SODIMM
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 3 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
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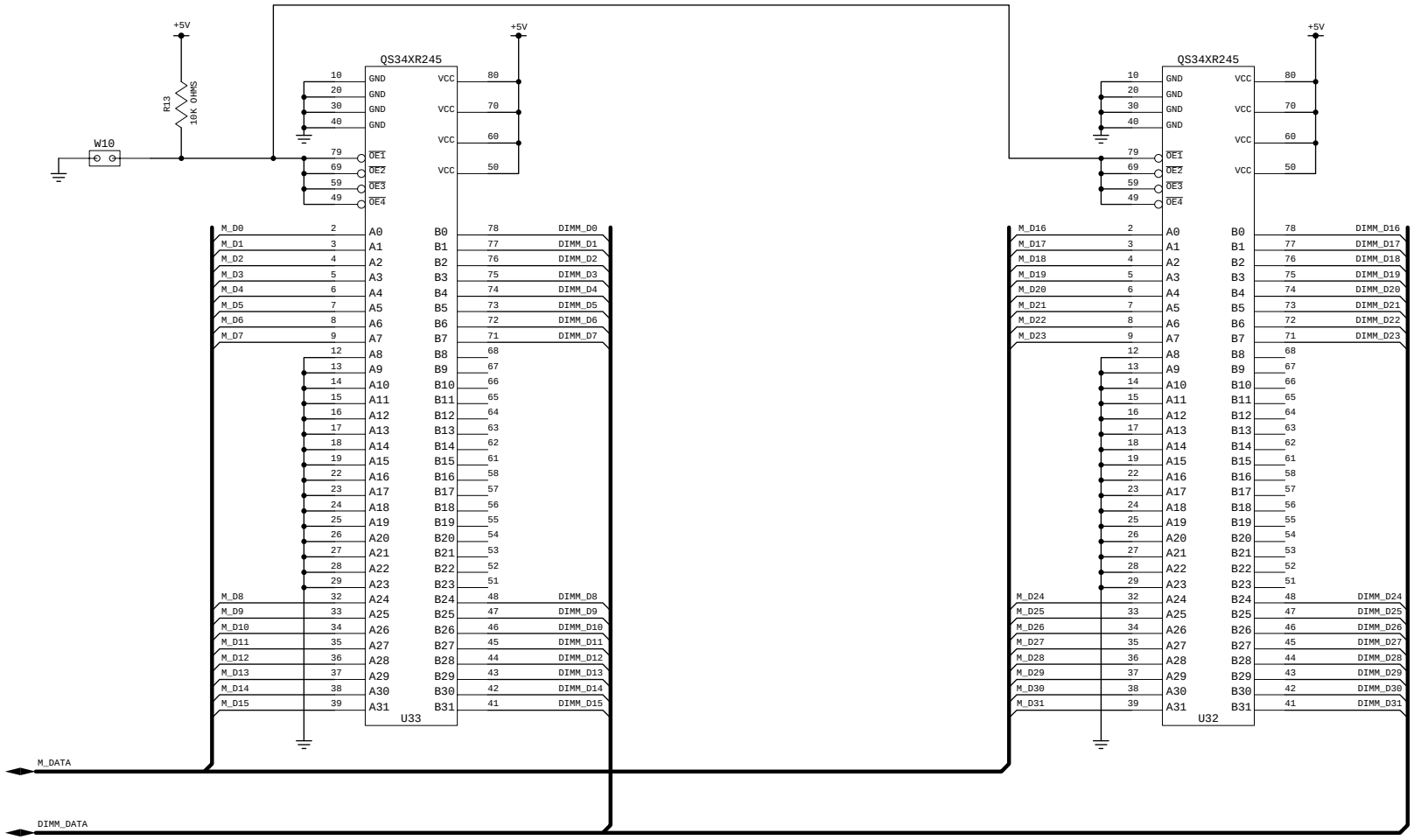


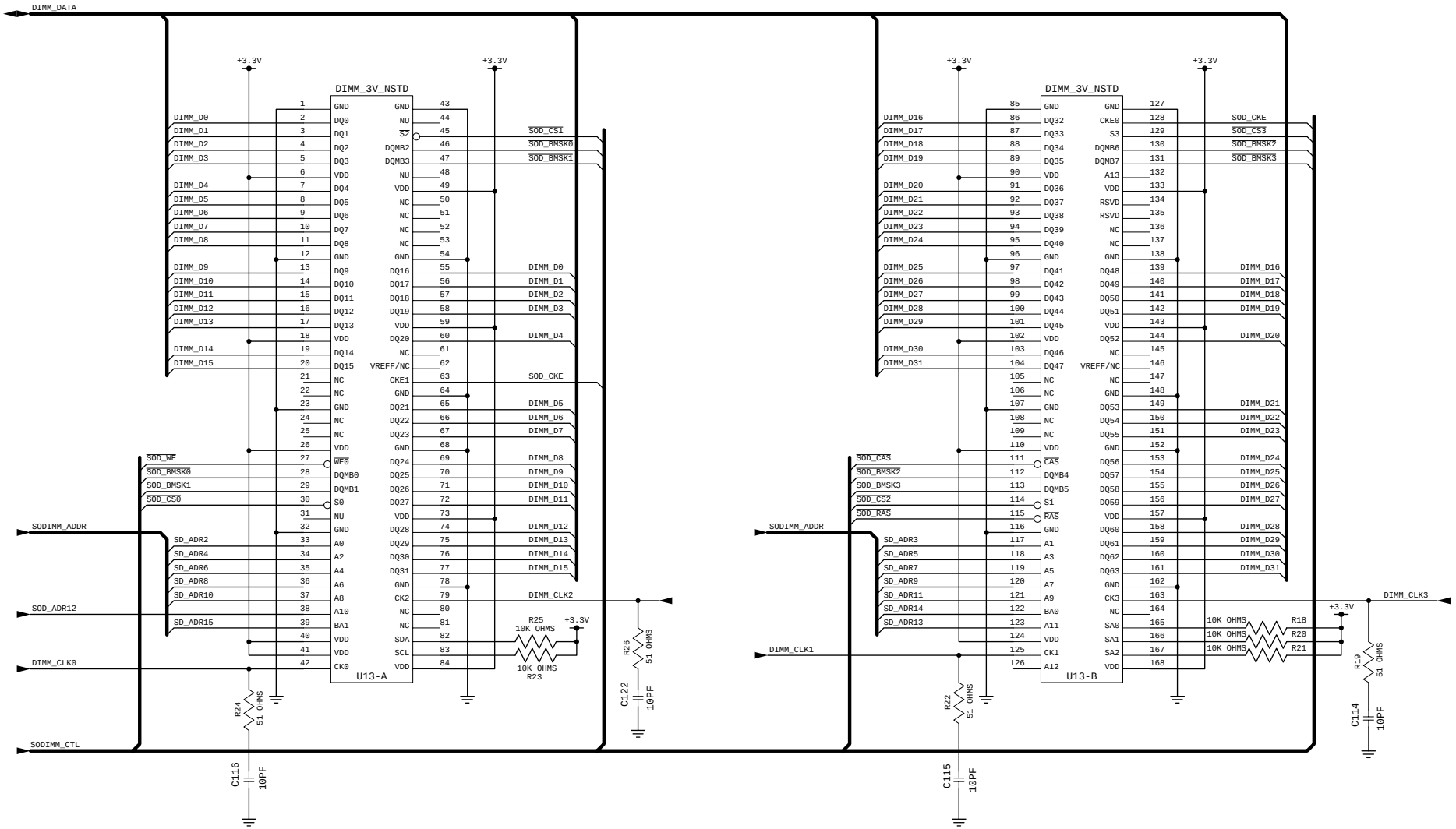
NOTE:

FOR DRAM DIMM OPERATION, INSTALL
W10 TO ENABLE QUICKSWITCHES.

FOR SODIMM OPERATION, REMOVE W10.

SHEET TITLE:	SDRAM QUICKSWITCHES
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 4 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
DRAWN BY:	J.A./GAIL SWAMI

SDRAM DIMM INTERFACE



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PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 5 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
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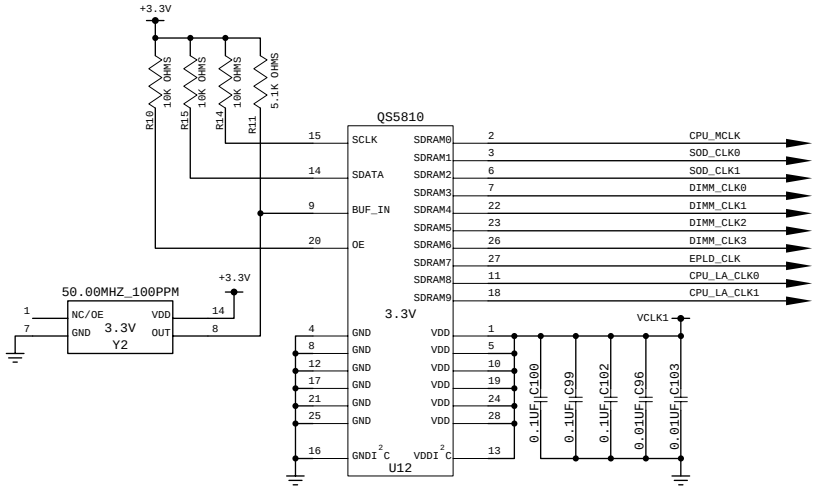
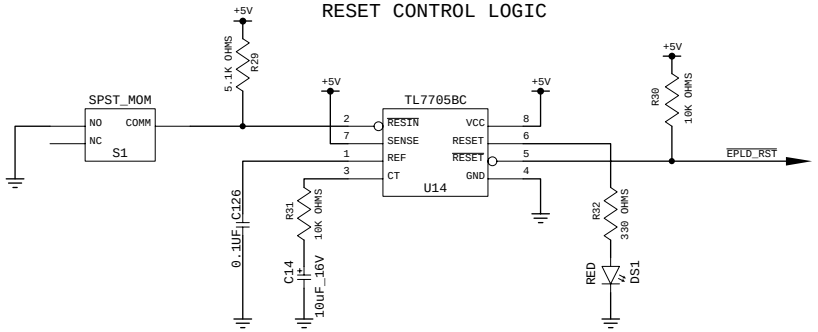
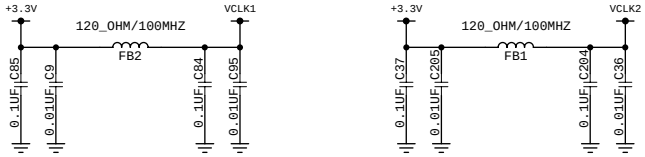
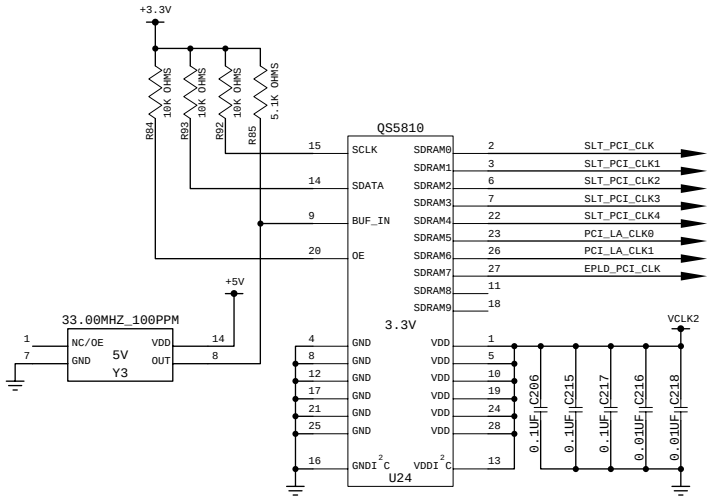


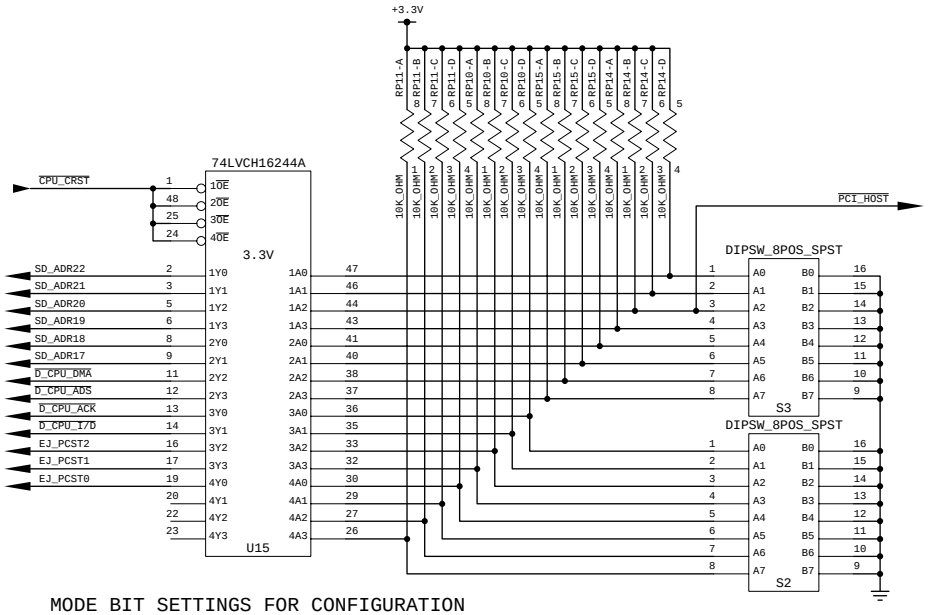
CPU & SDRAM CLOCK GENERATION







PCI CLOCK GENERATION



MODE BIT SETTINGS FOR CONFIGURATION

SHEET TITLE:	CLOCKS, RESET, CONFIG SW
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 6 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI
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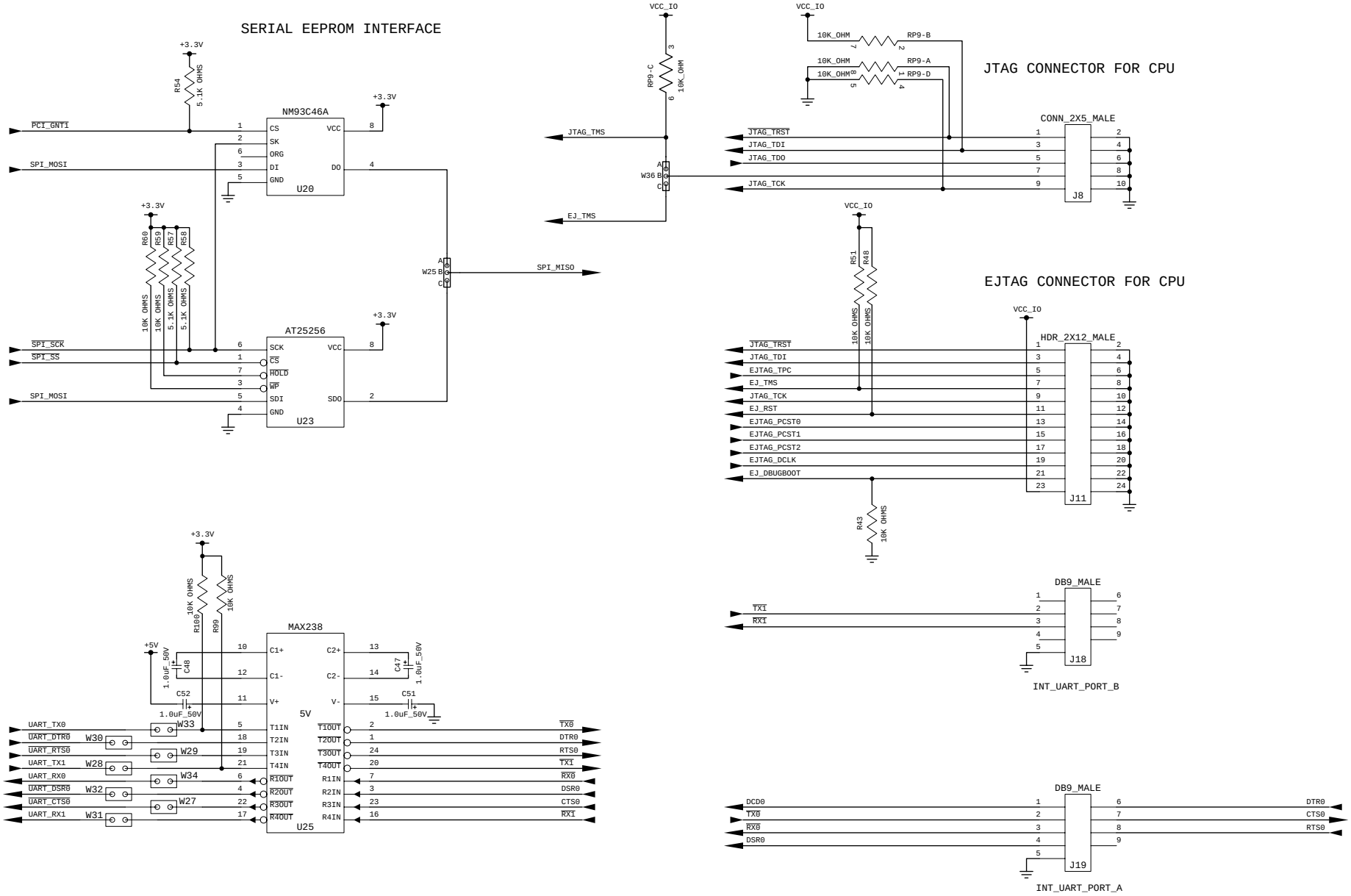

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SHEET TITLE:	JTAG, EJTAG, EEPROM, INT UART
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 7 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
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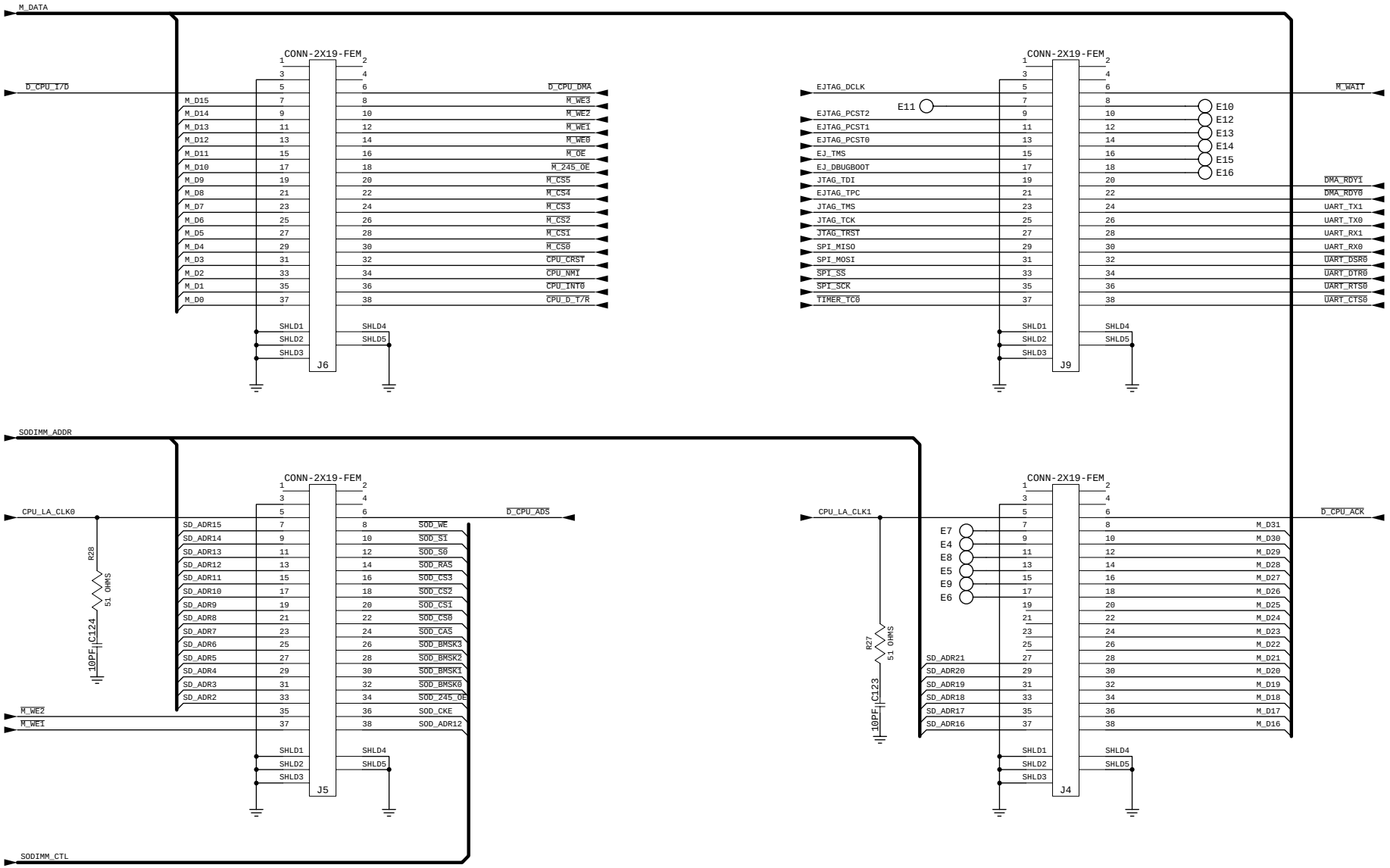

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PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 8 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
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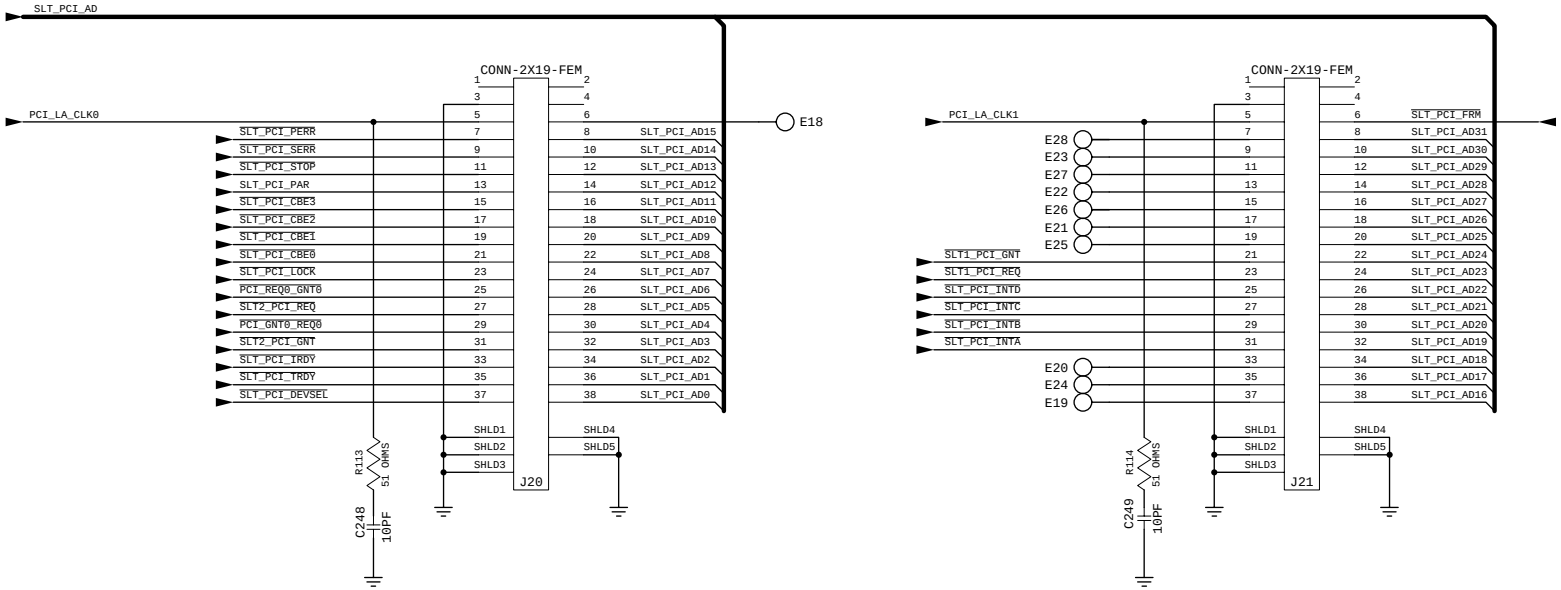

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SHEET TITLE:	PCI LOGIC ANALYZER CONN
PROJECT TITLE:	79S332/79S334A EVAL BD.
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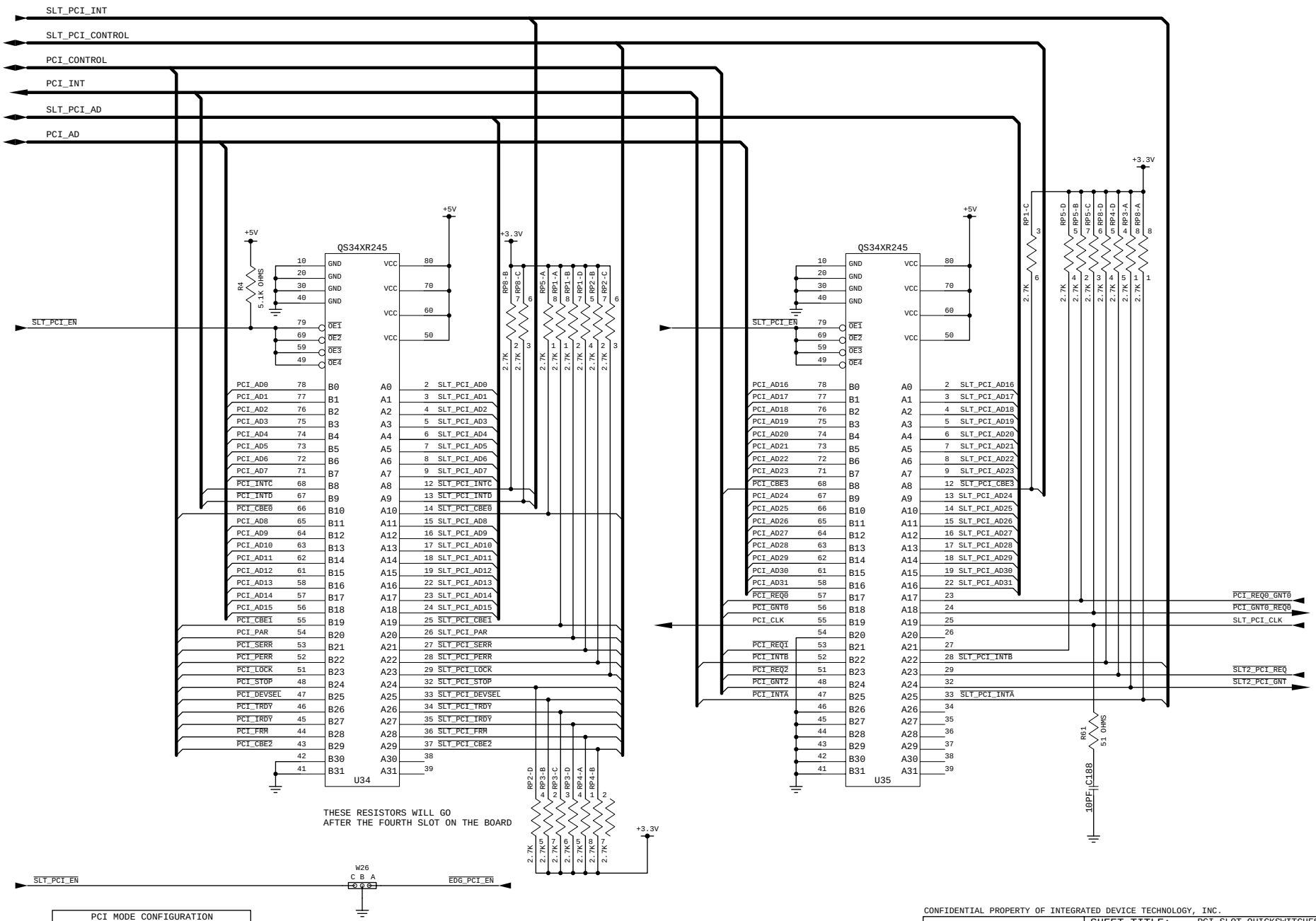
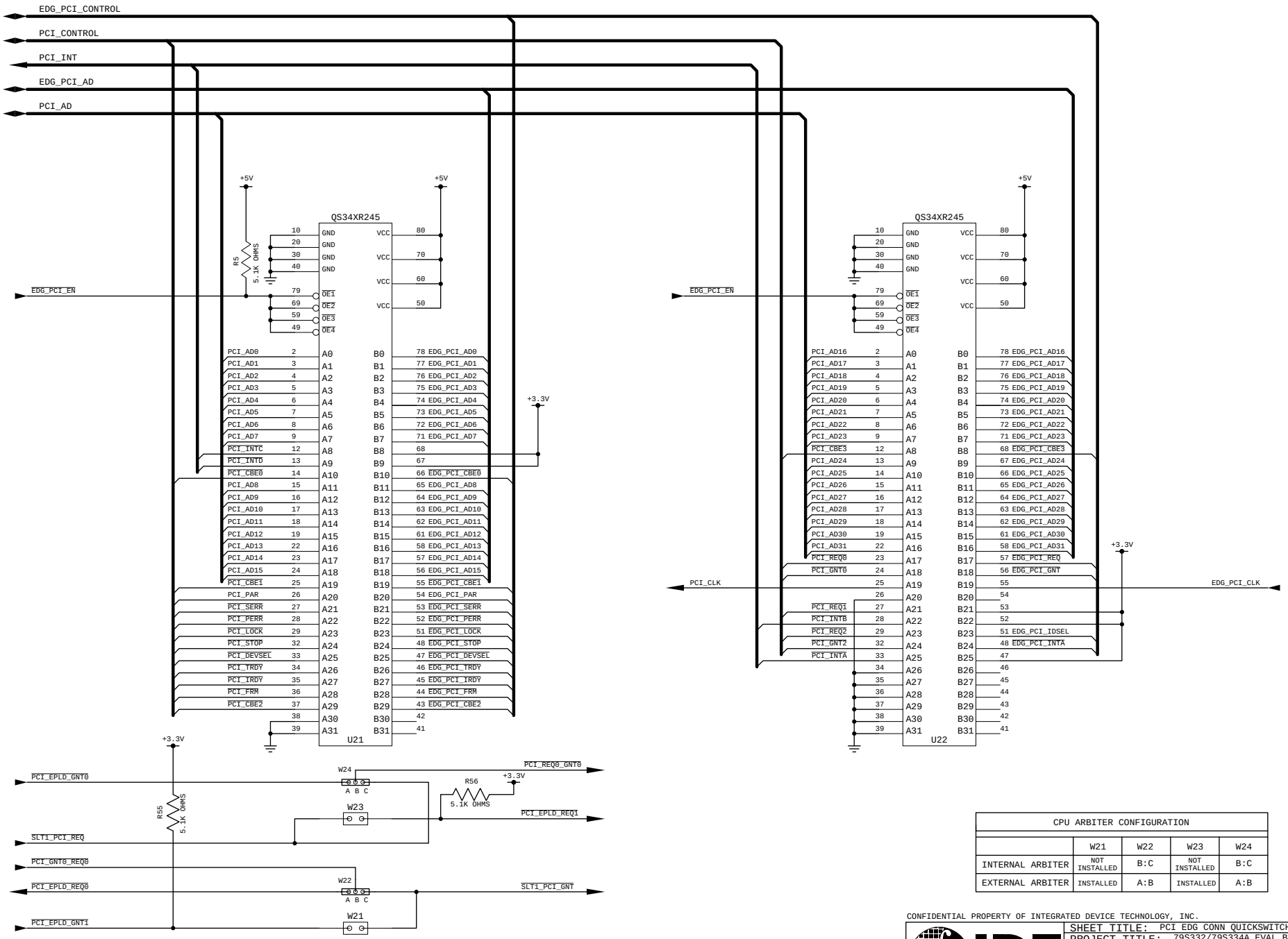
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
DRAWN BY:	J.A./GAIL SWAMI



PCI MODE CONFIGURATION	
HOST MODE (SLOT)	W26 B:C
SATELLITE MODE (EDGE)	W26 A:B

QUICKSWITCHES FOR PCI HOST MODE

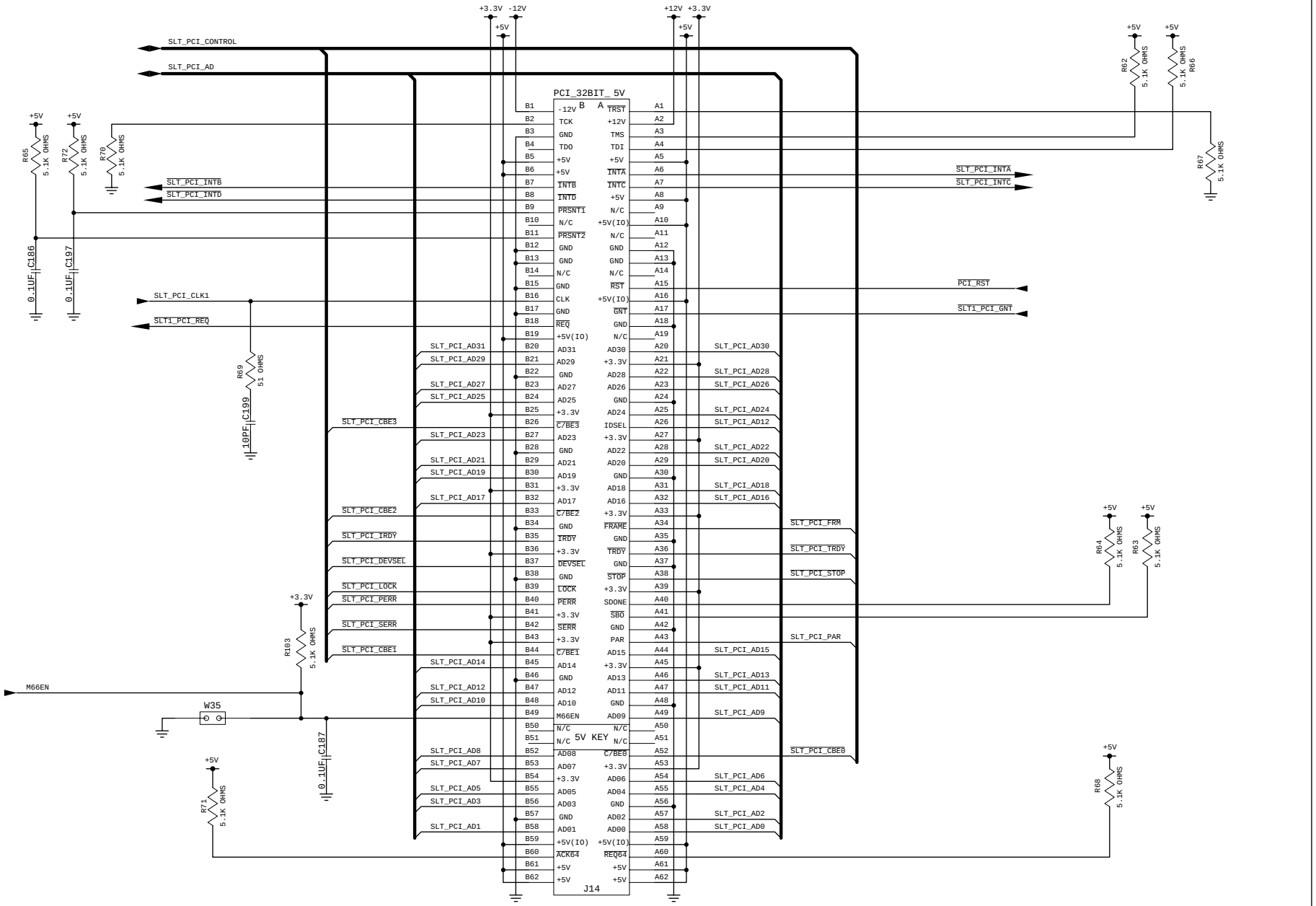
SHEET TITLE:	PCI SLOT QUICKSWITCHES
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 10 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
DRAWN BY:	J.A./GAIL SWAMI



CPU ARBITER CONFIGURATION				
	W21	W22	W23	W24
INTERNAL ARBITER	NOT INSTALLED	B:C	NOT INSTALLED	B:C
EXTERNAL ARBITER	INSTALLED	A:B	INSTALLED	A:B

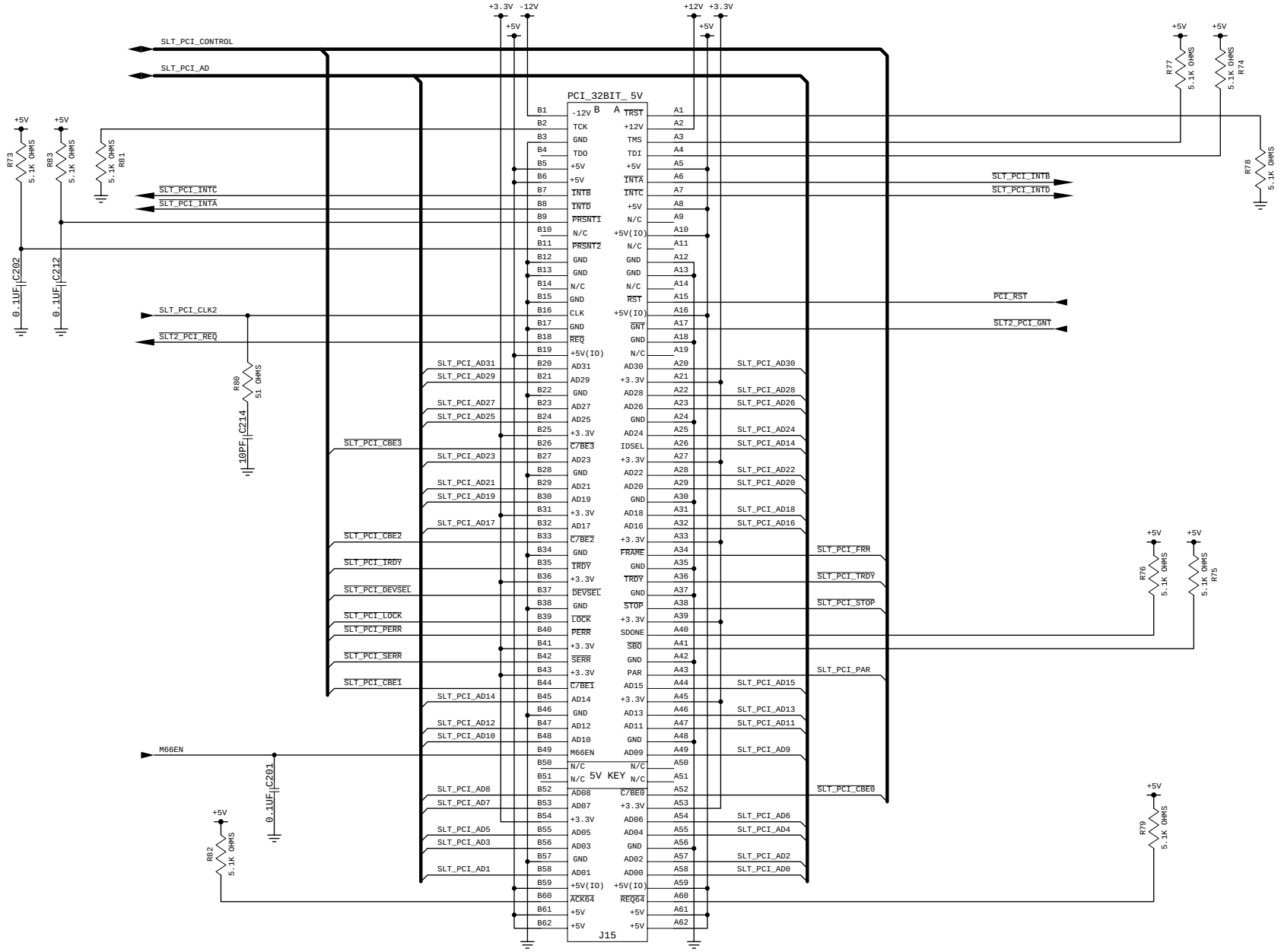
QUICKSWITCHES FOR PCI SATELLITE MODE

SHEET TITLE:	PCI EDG CONN QUICKSWITCHES
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 11 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
DRAWN BY:	J.A./GAIL SWAMI



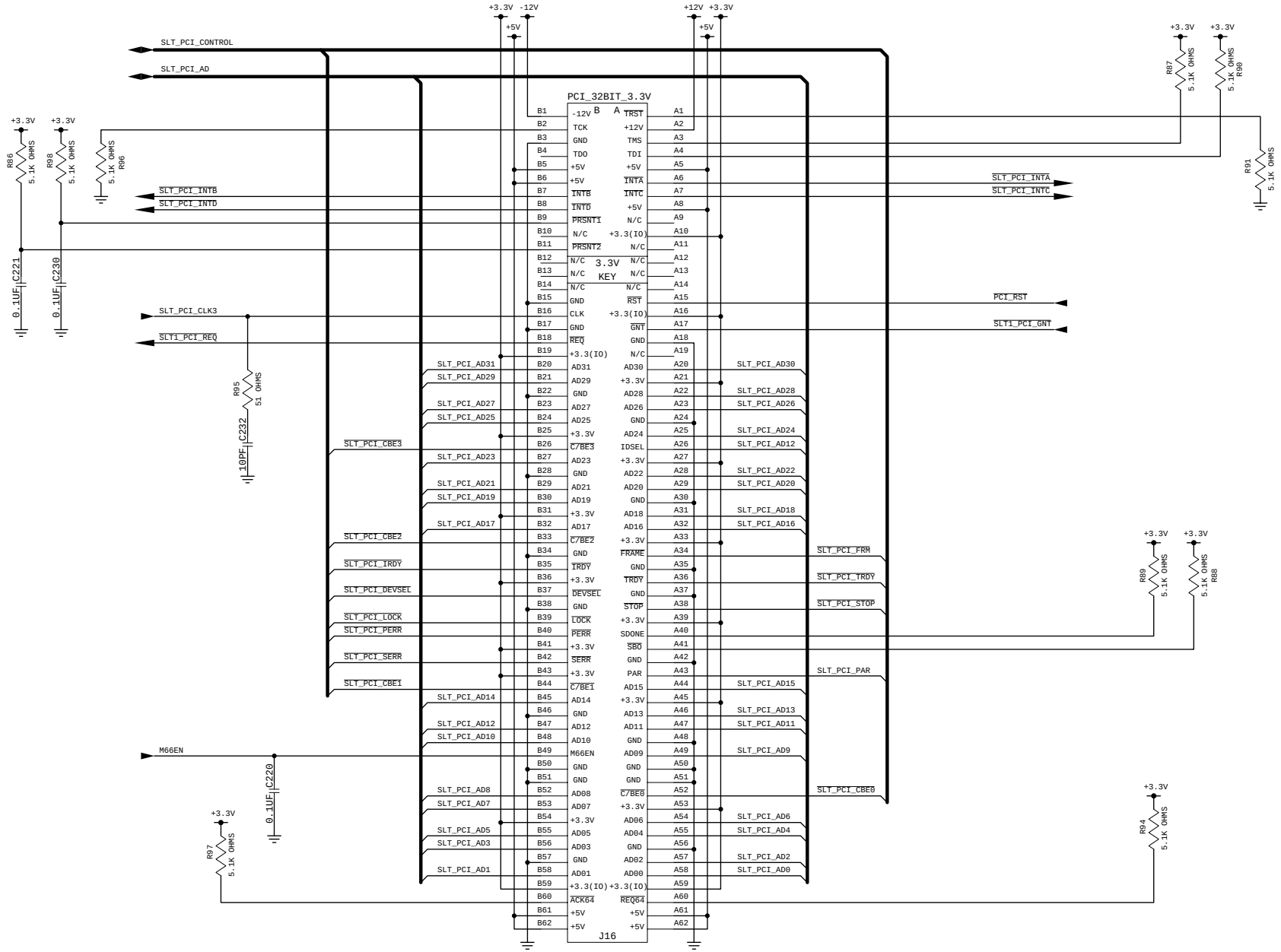
+5V PCI CONNECTOR-1

SHEET TITLE:	PCI SLOT 1
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 12 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
DRAWN BY:	J.A./GAIL SWAMI



+5V PCI CONNECTOR-2

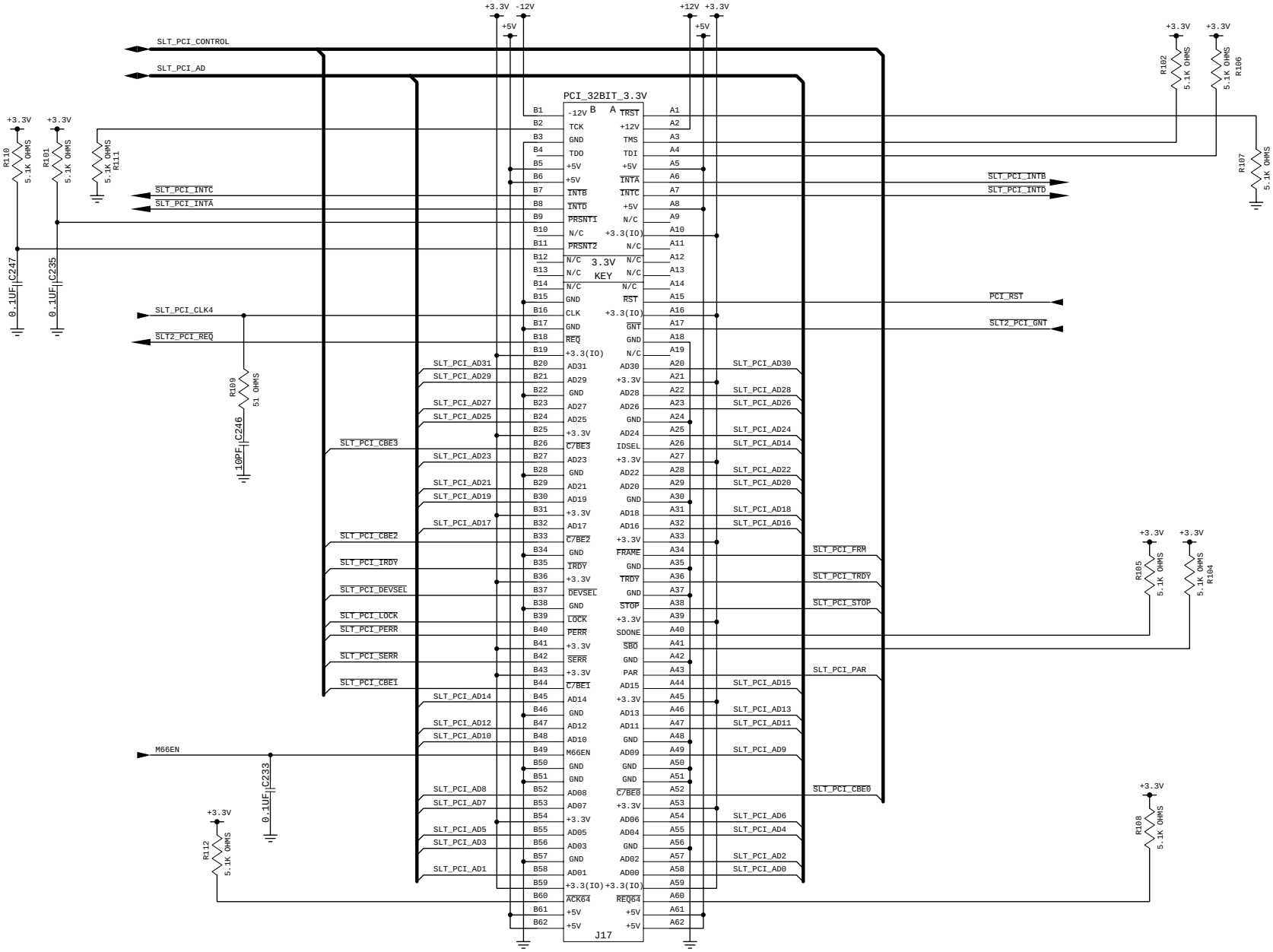
SHEET TITLE:	PCI SLOT 2
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 13 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAI/KASI
DRAWN BY:	J.A./GAIL SWAMI



+3.3V PCI CONNECTOR-1

CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.

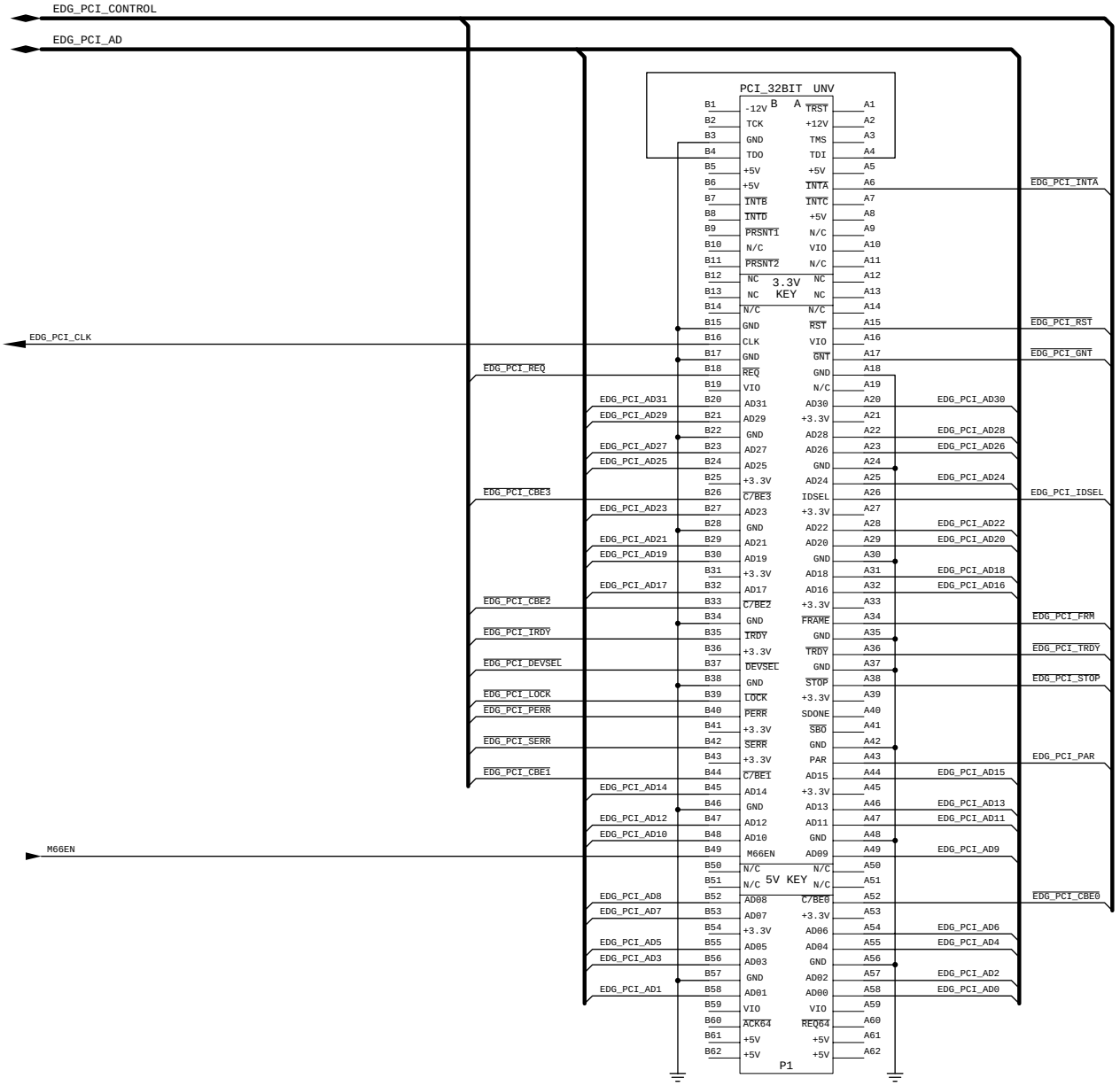
SHEET TITLE:	PCI SLOT 3
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 14 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAI/KASI
DRAWN BY:	J.A./GAIL SWAMI



+3.3V PCI CONNECTOR-2

CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.

SHEET TITLE:	PCI SLOT 4
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 15 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
DRAWN BY:	J.A./GAIL SWAMI

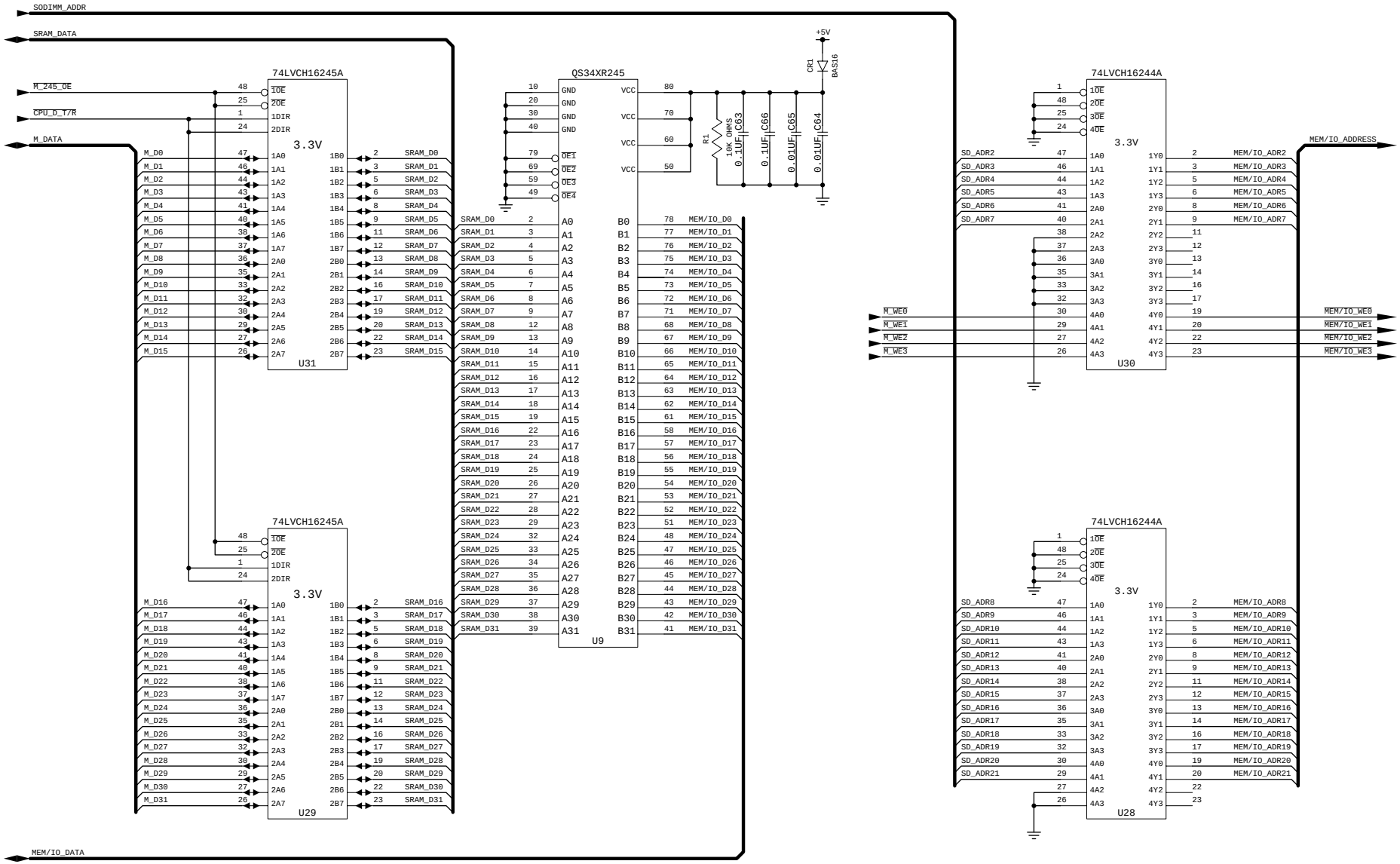


NOTE:

+5V, +3.3V, +12V AND -12V ARE NOT CONNECTED TO THE EDGE CONNECTOR. FOR SATELLITE MODE OPERATION, USE EXTERNAL SUPPLY CONNECTOR J13.

PCI UNIVERSAL EDGE CONNECTOR

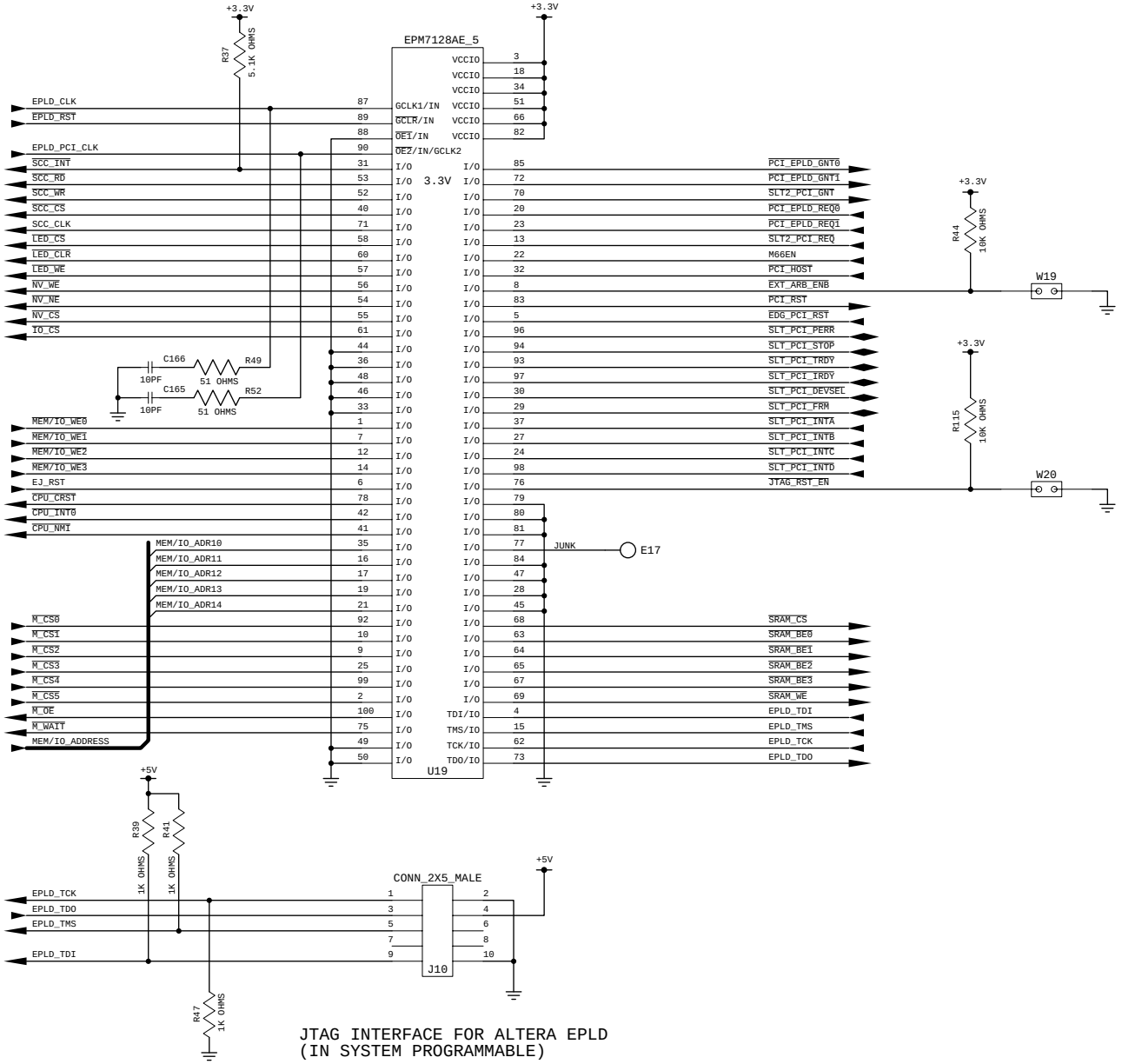
SHEET TITLE:	PCI EDG CONN
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 16 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
DRAWN BY:	J.A./GAIL SWAMI



CPU DATA AND ADDRESS BUFFERS

SHEET TITLE:	DATA, ADDRESS BUFFERS
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 17 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
DRAWN BY:	J.A./GAIL SWAMI

EPLD

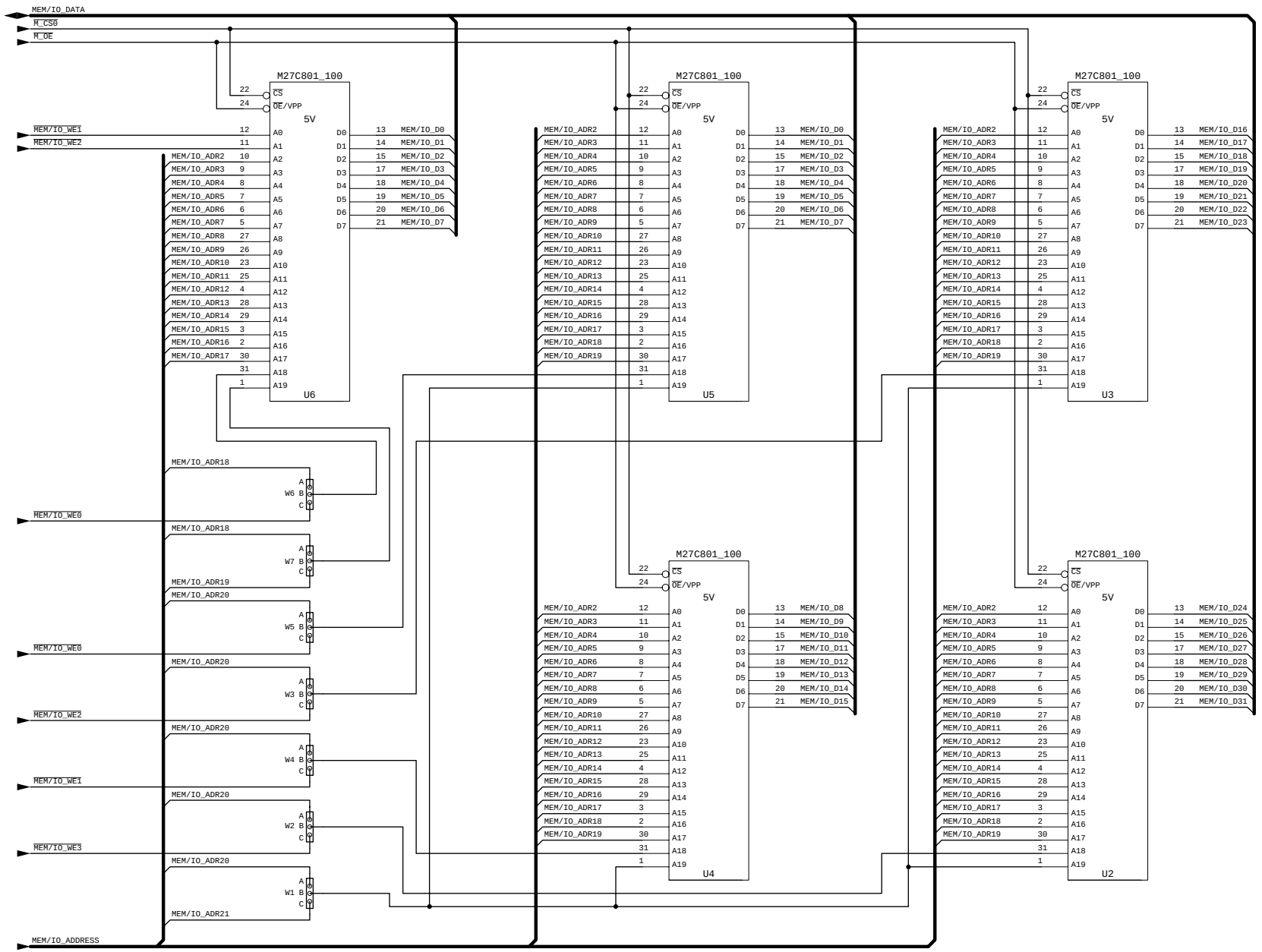


JTAG INTERFACE FOR ALTERA EPLD
(IN SYSTEM PROGRAMMABLE)

SHEET TITLE:	EPLD
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 18 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
DRAWN BY:	J.A./GAIL SWAMI

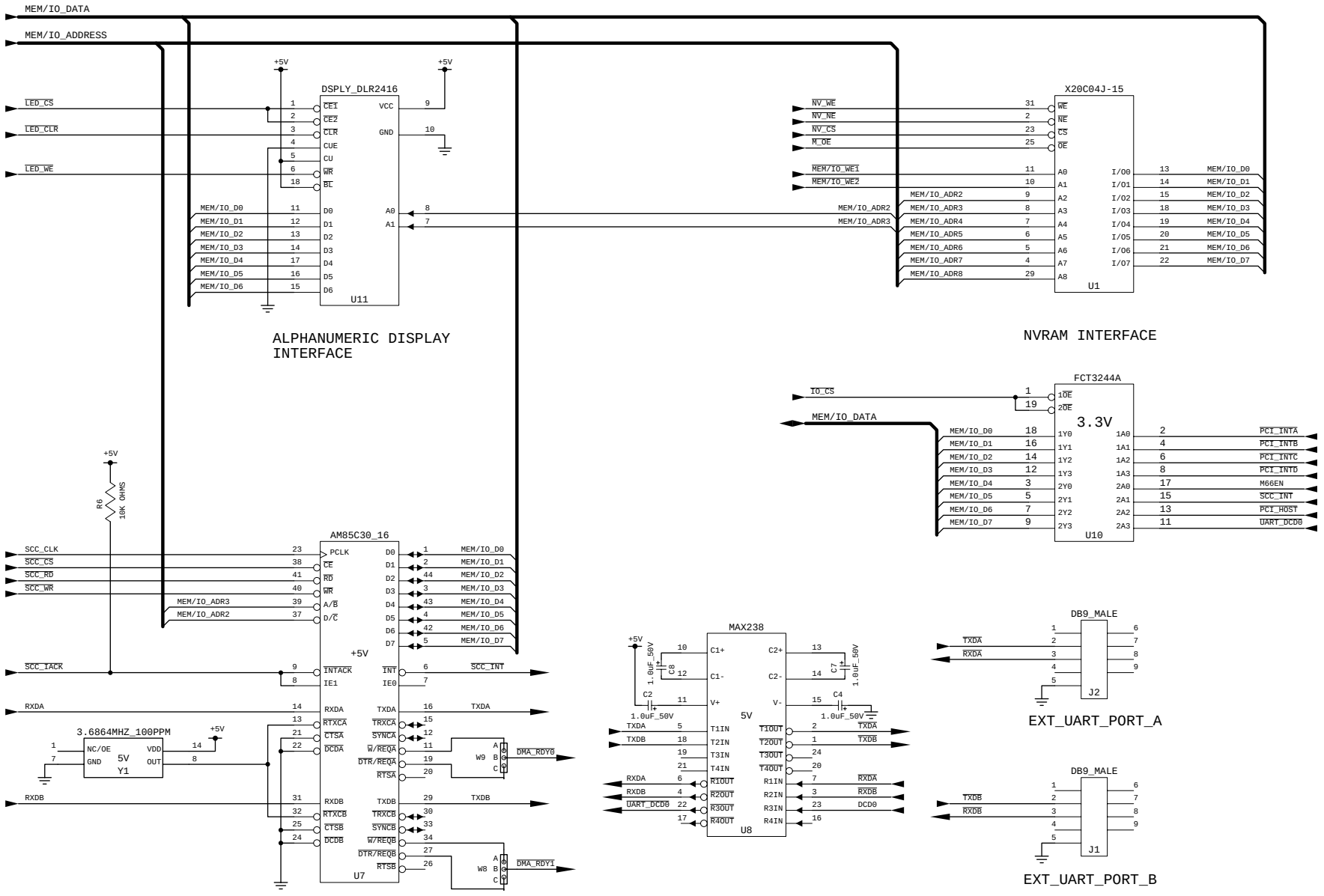
SRAM INTERFACE

SHEET TITLE:	SRAM
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 19 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
DRAWN BY:	J.A./GAIL SWAMI



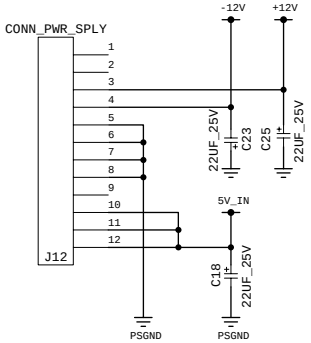
EPROM/FLASH INTERFACE

SHEET TITLE:	EPROM/FLASH MEMORY
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 20 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
DRAWN BY:	J.A./GAIL SWAMI

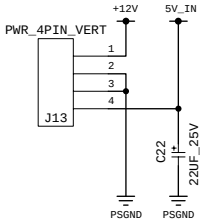


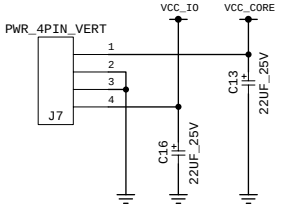
SHEET TITLE:	DISPLAY, NVRAM, EXT UART
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 001	PAGE NUMBER: 21 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
DRAWN BY:	J.A./GAIL SWAMI

AT POWER SUPPLY CONNECTOR
FOR PCI HOST MODDE

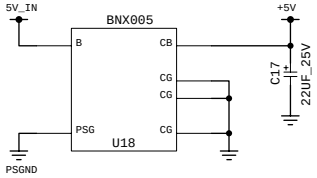


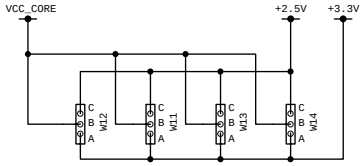
PCI CONNECTOR FOR SATELLITE MODE

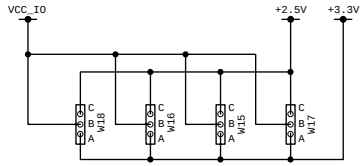




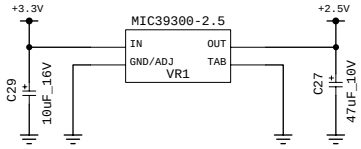
CONNECTOR FOR VARIABLE
POWER SUPPLY

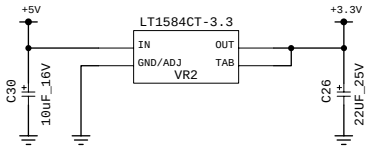




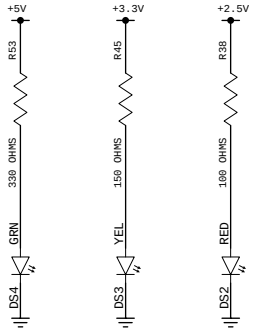


CPU VOLTAGE CONFIGURATION	
VCC_CORE: +2.5V	W11 - W14 B:C
VCC_CORE: +3.3V	W11 - W14 A:B
VCC_IO: +2.5V	W15 - W18 B:C
VCC_IO: +3.3V	W15 - W18 A:B



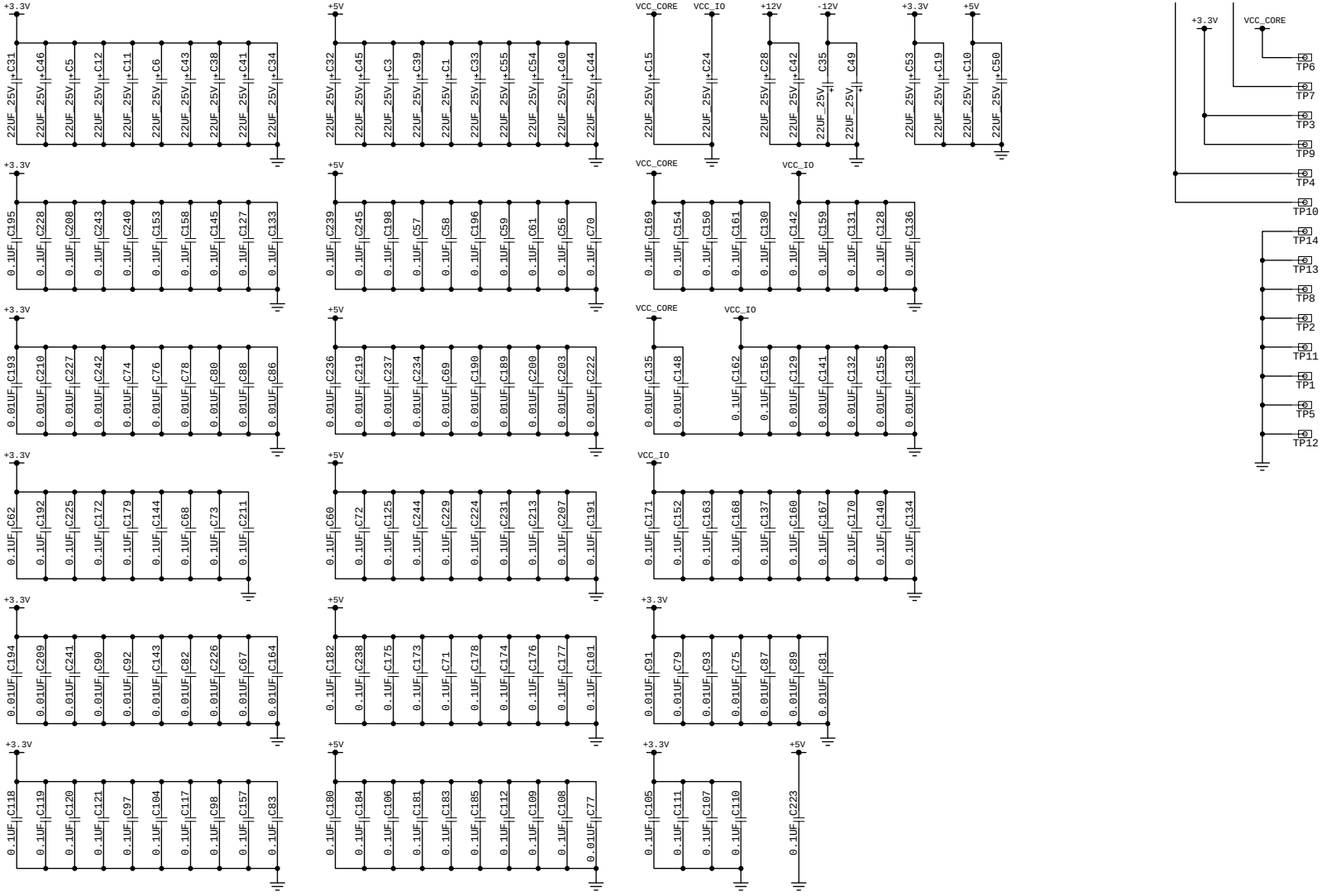


POWER-ON LED'S



CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.

SHEET TITLE:	POWER SUPPLY
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 22 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
DRAWN BY:	J.A./GAIL SWAMI



FD14	FD9	FD11	FD13	FD18
FD16	FD10	FD12	FD15	FD17
FD2	FD3	FD7	FD5	FD19
FD1	FD4	FD8	FD6	FD20
MTG2	MTG6	MTG7	FD23	FD22
MTG8	MTG4	MTG5	FD24	FD25
Z1	MTG1	MTG3	FD26	FD21

SHEET TITLE:	BYPASS CAPACITORS
PROJECT TITLE:	79S332/79S334A EVAL BD.
REV LEVEL: 003	PAGE NUMBER: 23 OF 23
PART NUMBER:	003-A1550-003
ENGINEER'S NAME:	RITESH KAPAHI/KASI
DRAWN BY:	J.A./GAIL SWAMI

Notes

EPLD Equation

Notes

SYSCONSTG

```
-- ****************************************
-- * Author: Viswanadha Rao Chopperla (KASI)      *
-- * Company: IDT Inc.,                          *
-- * Part No: (EPM7128AETC100-5)                 *
-- * Project: 79S334A EVALUATION BOARD           *
-- * Language: AHDL                              *
-- * Logic : This logic consists of              *
-- *              1. Reset (EJTAG)               *
-- *              2. Interrupt Logic             *
-- *              3. SRAM Control                *
-- *              5. LED Control                 *
-- *              6. NVRAM Control               *
-- *              7. Ext. PCI bus ARB            *
-- *              8. uart pclk gen               *
-- *                                             *
-- ****************************************
-- Title Statement (optional)
TITLE "sysconstg";

-- Subdesign Section
SUBDESIGN SYSCONSTG
(
        epld_clk                : INPUT;
        epld_rst_n              : INPUT;
        epld_pci_clk            : INPUT;
        scc_int_n               : INPUT;
        scc_rd_n                : OUTPUT;
        scc_wr_n                : OUTPUT;
        scc_cs_n                : OUTPUT;
        scc_clk                 : OUTPUT;
        led_cs_n                : OUTPUT;
        led_clr_n               : OUTPUT;
        led_we_n                : OUTPUT;
        nv_cs_n                 : OUTPUT;
        nv_ne_n                 : OUTPUT;
        nv_we_n                 : OUTPUT;
        io_cs_n                 : OUTPUT;
        ej_rst_n                : INPUT;
        edg_pci_rst_n           : INPUT;
```

```
        cpu_crst_n              : OUTPUT;
        cpu_int0_n              : OUTPUT;
        cpu_nmi_n               : OUTPUT;
        mem_io_adrs[14..10]     : INPUT;
        m_cs_n[5..0]            : INPUT;
        m_oe_n                  : INPUT;
        mem_io_we_n[3..0]       : INPUT;
        m_wait_n                : OUTPUT;
%       epld_tdi                : INPUT;
        epld_tdo                : OUTPUT;
        epld_tck                : INPUT;
        epld_tms                : INPUT;
%
        sram_cs_n               : OUTPUT;
        sram_we_n               : OUTPUT;
        sram_be_n[3..0]         : OUTPUT;
--      slt_pci_inta_n          : INPUT;
        slt_pci_inta_n          : OUTPUT;
        slt_pci_intb_n          : INPUT;
        slt_pci_intc_n          : INPUT;
        slt_pci_intd_n          : INPUT;
        slt_pci_frm_n           : INPUT;
        slt_pci_devsel_n        : INPUT;
        slt_pci_irdy_n          : INPUT;
        slt_pci_trdy_n          : INPUT;
        slt_pci_stop_n          : INPUT;
        slt_pci_perr_n          : INPUT;
        pci_rst_n               : OUTPUT;
        ext_arb_enb_n           : INPUT;
        pci_host_n              : INPUT;
        m66en                   : INPUT;
        slt2_pci_req_n          : INPUT;
        slt2_pci_gnt_n          : OUTPUT;
        pci_epld_gnt_n[1..0]    : OUTPUT;
        pci_epld_req_n[1..0]    : INPUT;
        junc                    : OUTPUT;
)
VARIABLE
        cpu_crst                : DFF;
        rst_dly[10..0]          : DFFE;
        count[2..0]             : DFF;
        osc_10mhz               : DFF;
        mem_wait_tri            : TRI;
        intr_tri                : TRI;
        pci_gnt2_tri            : TRI;
```

```
        tmp_junc                : DFF;


BEGIN

--LOGIC

DEFAULTS
        cpu_crst                = VCC;
END DEFAULTS;

--CPU_INTERRUPTS

        cpu_nmi_n               = VCC;
        --cpu_int0_n            = scc_int_n & slt_pci_inta_n & slt_pci_intb_n & slt_pci_intc_n & slt_pci_intd_n;
        cpu_int0_n              = scc_int_n;
        intr_tri.oe             = !(slt_pci_intb_n & slt_pci_intc_n & slt_pci_intd_n);
        intr_tri.in             = GND;
        slt_pci_inta_n          = intr_tri.out;

--CPU_RESET
--4/14/00 for EJTAG reset
        rst_dly[].clk           = GLOBAL(epld_clk);
        rst_dly[].clrn          = epld_rst_n & ej_rst_n;
        rst_dly[].ena           = !rst_dly[10];
        rst_dly[]               = rst_dly[] + 1;

        cpu_crst.d              = rst_dly[10];
        cpu_crst.clk            = GLOBAL(epld_clk);
        cpu_crst.clrn           = epld_rst_n & ej_rst_n & (!pci_host_n # edg_pci_rst_n);
        cpu_crst_n              = cpu_crst.q ;

-- JUNC unused
        tmp_junc.d              = m_cs_n0 # pci_epld_req_n0 # pci_epld_req_n1 # slt_pci_frm_n # slt_pci_devsel_n
                                # slt_pci_perr_n #slt_pci_trdy_n # slt_pci_irdy_n # slt_pci_stop_n # m66en
                                # slt2_pci_req_n # ext_arb_enb_n;
        tmp_junc.clk            = GLOBAL(epld_pci_clk);
        junc                    = tmp_junc.q;

--SRAM
sram_we_n               = !epld_rst_n # m_cs_n1 # (mem_io_we_n3 & mem_io_we_n2 & mem_io_we_n1 & mem_io_we_n0);
sram_be_n3              = !epld_rst_n # m_cs_n1 # (mem_io_we_n3 & m_oe_n);
sram_be_n2              = !epld_rst_n # m_cs_n1 # (mem_io_we_n2 & m_oe_n);
sram_be_n1              = !epld_rst_n # m_cs_n1 # (mem_io_we_n1 & m_oe_n);
sram_be_n0              = !epld_rst_n # m_cs_n1 # (mem_io_we_n0 & m_oe_n);
sram_cs_n               = m_cs_n1;
```

```
--SCC
%
Base Address for chip select_5 is $1600_0000

Soft_reset UART address is $1600_0400 (Read this port)

Channel_B command port address is $1600_0003
Channel_B data port address is $1600_0007
Channel_A command port address is $1600_000B
Channel_A data port address is $1600_000F
%
scc_cs_n            = m_cs_n5;
scc_rd_n            = epld_rst_n & (m_oe_n # m_cs_n5  # mem_io_adrs14 # mem_io_adrs13
                    # mem_io_adrs12 # mem_io_adrs11 );
scc_wr_n            = epld_rst_n & (mem_io_we_n0 # m_cs_n5  # mem_io_adrs14 # mem_io_adrs13
                    # mem_io_adrs12 # mem_io_adrs11 )
                    & (m_oe_n # m_cs_n5 # mem_io_adrs14 # mem_io_adrs13 # mem_io_adrs12
                    # mem_io_adrs11 # !mem_io_adrs10);

-- The PCLK of SCC is approx. One sixth of epld_clk

count[2..0].clrn    = GLOBAL(epld_rst_n);
count[2..0].clk     = GLOBAL(epld_clk);
IF count[2..0].q    == 2 THEN
count[2..0].d       = 0;
ELSE
count[2..0].d       = count[2..0].q + 1;
END IF;
osc_10mhz.clrn      = GLOBAL(epld_rst_n);
osc_10mhz.d         = !osc_10mhz.q;
osc_10mhz.clk       = count[1].q;
scc_clk             = osc_10mhz.q;

--AN_DISPLAY/LED_DISPLAY
%
Base address for chip select_4 is $1400_0000
Address to clear digits is $1400_0400 (Read this port)
Address for digit0 is $1400_000F
Address for digit1 is $1400_0007
Address for digit2 is $1400_000B
Address for digit3 is $1400_0003
%

led_cs_n            = (!epld_rst_n # m_cs_n4 # mem_io_adrs14 # mem_io_adrs13
                    # mem_io_adrs12# mem_io_adrs11 # mem_io_adrs10);
```

```
led_clr_n           = (!epld_rst_n # m_cs_n4 # m_oe_n # mem_io_adrs14 # mem_io_adrs13
                    # mem_io_adrs12 # mem_io_adrs11 # !mem_io_adrs10);
led_we_n            = (!epld_rst_n # m_cs_n4 # mem_io_we_n0 # mem_io_adrs14 # mem_io_adrs13
                    # mem_io_adrs12 # mem_io_adrs11 # mem_io_adrs10);

--NV_RAM
%
Base address for chip select_3 is $1200_0000
Base address for read/write cycle is $1200_0000 (RAM operations)
Base address for recall/store cycle is $1200_0400 (Non-volatile operations)
%

nv_cs_n             = (!epld_rst_n # m_cs_n3 # mem_io_adrs14 # mem_io_adrs13
                    # mem_io_adrs12 # mem_io_adrs11);
nv_ne_n             = (!epld_rst_n # m_cs_n3 # mem_io_adrs14 # mem_io_adrs13
                    # mem_io_adrs12 # mem_io_adrs11 # !mem_io_adrs10);
nv_we_n             = (!epld_rst_n # m_cs_n3 # mem_io_adrs14 # mem_io_adrs13
                    # mem_io_adrs12 # mem_io_adrs11 # mem_io_we_n0);

--IO_INTERRUPTS_SOURCE
%
Base address for chip select_2 is $1000_0000
%
io_cs_n             = (!epld_rst_n # m_oe_n # m_cs_n2 # mem_io_adrs14 # mem_io_adrs13
                    # mem_io_adrs12 # mem_io_adrs11 # mem_io_adrs10);
--WAIT_CONTROL
m_wait_n            = mem_wait_tri;
mem_wait_tri.oe     = vcc;
mem_wait_tri        = vcc;

--PCI_CLK

pci_rst_n           = cpu_crst.q & ej_rst_n & (!pci_host_n # edg_pci_rst_n);
pci_epld_gnt_n[1..0] = VCC;
--slt2_pci_gnt_n    = VCC;
pci_gnt2_tri.in     = GND;
pci_gnt2_tri.oe     = !ext_arb_enb_n;
slt2_pci_gnt_n      = pci_gnt2_tri.out;

END;
```

Notes

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