NEC

Preliminary User's Manual

IMAPCAR2 Video I/F Board

Hardware

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Table of Contents

1 Introduction

The Video I/F board is to interface external imagers and display with the IMAPCAR2 evaluation board.

2 Specification

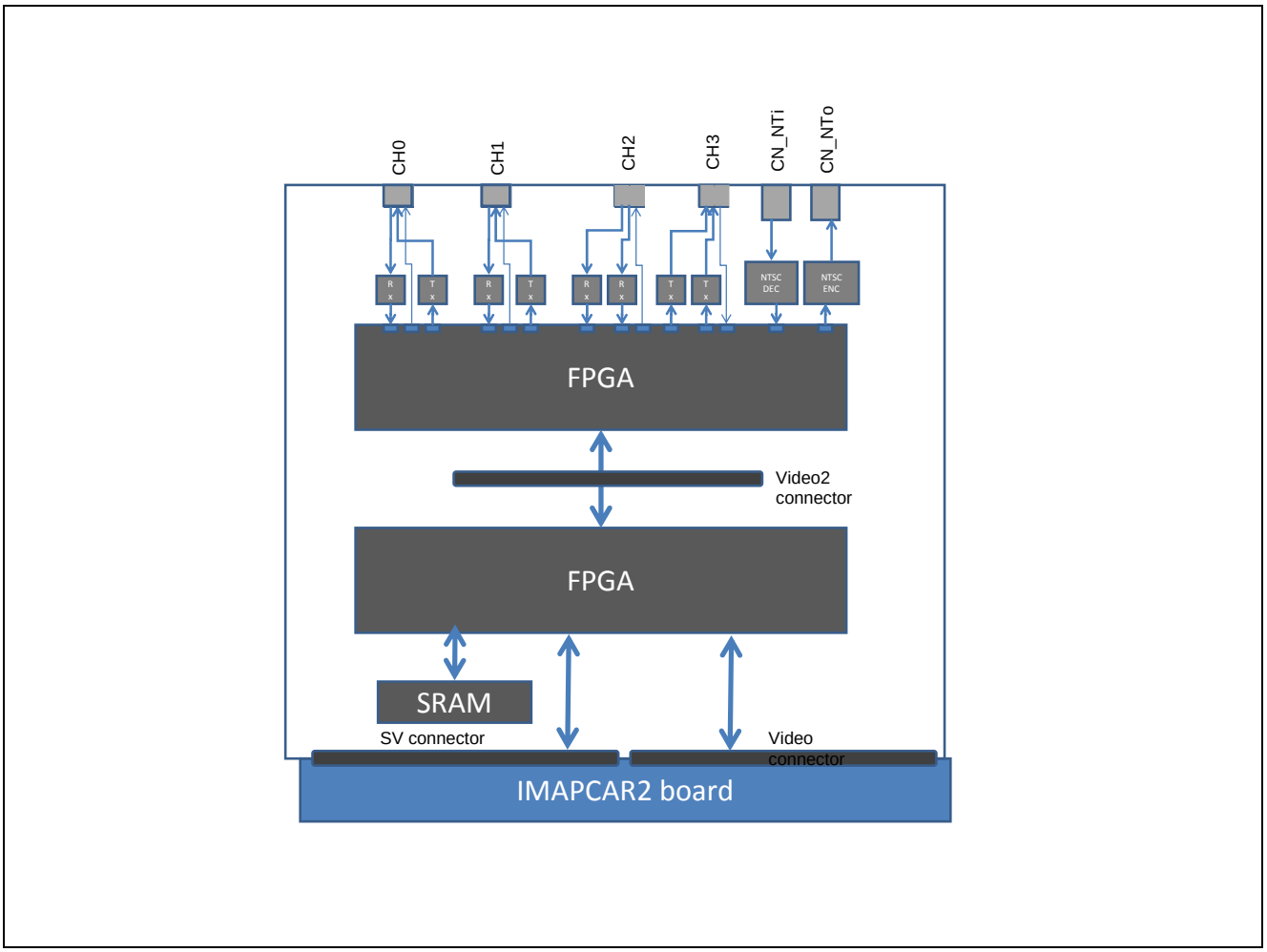
The Video I/F board is composed by the following main components:

FPGA	Xilinx XC3S2000-4FGG676C (676pinBGA) Xilinx XCF08PV0G48C (48pinTSOP)	Spartan3 ROM for FPGA config
LVDS	THine THCV213 (48pinTQFP) Transmitter THine THCV214 (48pinTQFP) Receiver	・18 bits ×20MHz fixation use ・18 bits ×20MHz fixation use
RS485	Linear Technology LTC2850IMS8 (8pinMSOP) Transceiver	・20Mbps
NTSC/PAL	OKI ML86V7655 (100pinTQFP) OKI ML86V7666 (100pinTQFP)	・NTSC/PAL encoder ・NTSC/PAL decoder
SRAM	NEC μPD444016LG5-A8-7JF-A (44pinTSOP)	・4Mbit (256Kword×16bit)
Dip SW	COPAL CHS-10TB (20pinTSOP) COPAL CHS-8TB (16pinTSOP)	・SW1 ・SW6/7/8/9/10
Push SW	FUJISOKU SMT3-01-Z (SMD7X6)	・SW_HRESET/SW_PRESET
LED	ROHM SML-210VTT86 RED ROHM SML-210PTT86 GREEN	・LED15 ・LED1～14、LED16～23
Power supply	Input power supply	・12V (Input range：4.5V-14V) and +1A or more

3 General overview and block diagrams

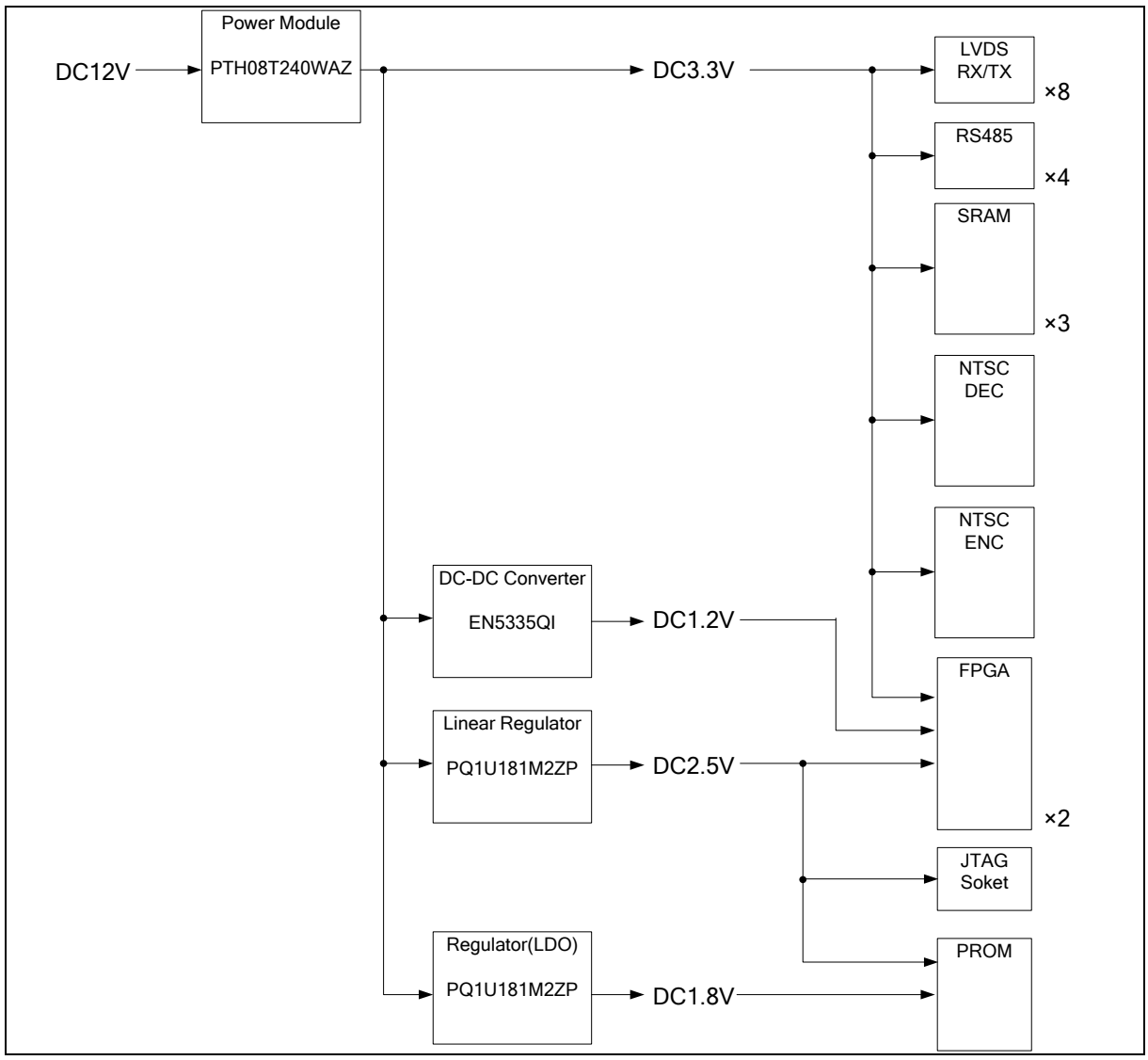
3.1 Video Board IF overview

The following figure is the general overview on the IMAPCAR2 video IF board



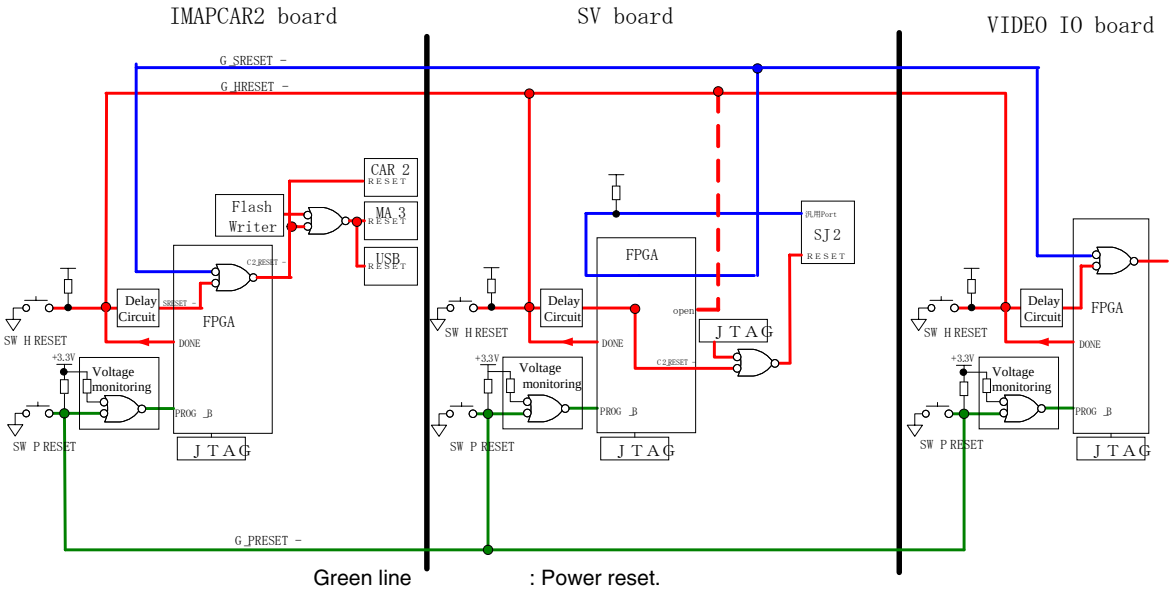
3.2 Power Supply block diagram

The following figure describes the block diagram of the power supply.



3.3 Reset block diagram

The following system describes the reset management of the entire system (including the IMAPCAR2-300 evaluation board)

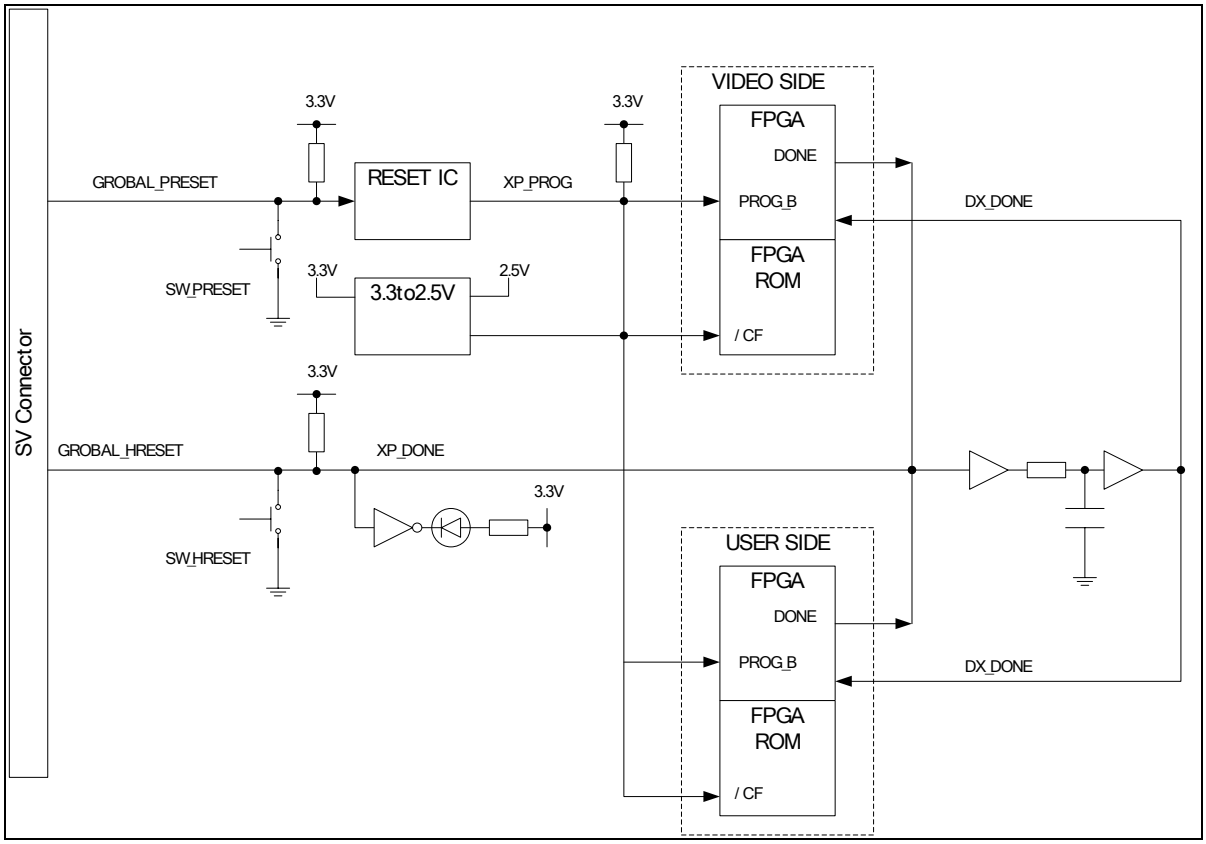


Green line : Power reset.

Red line : hard reset.

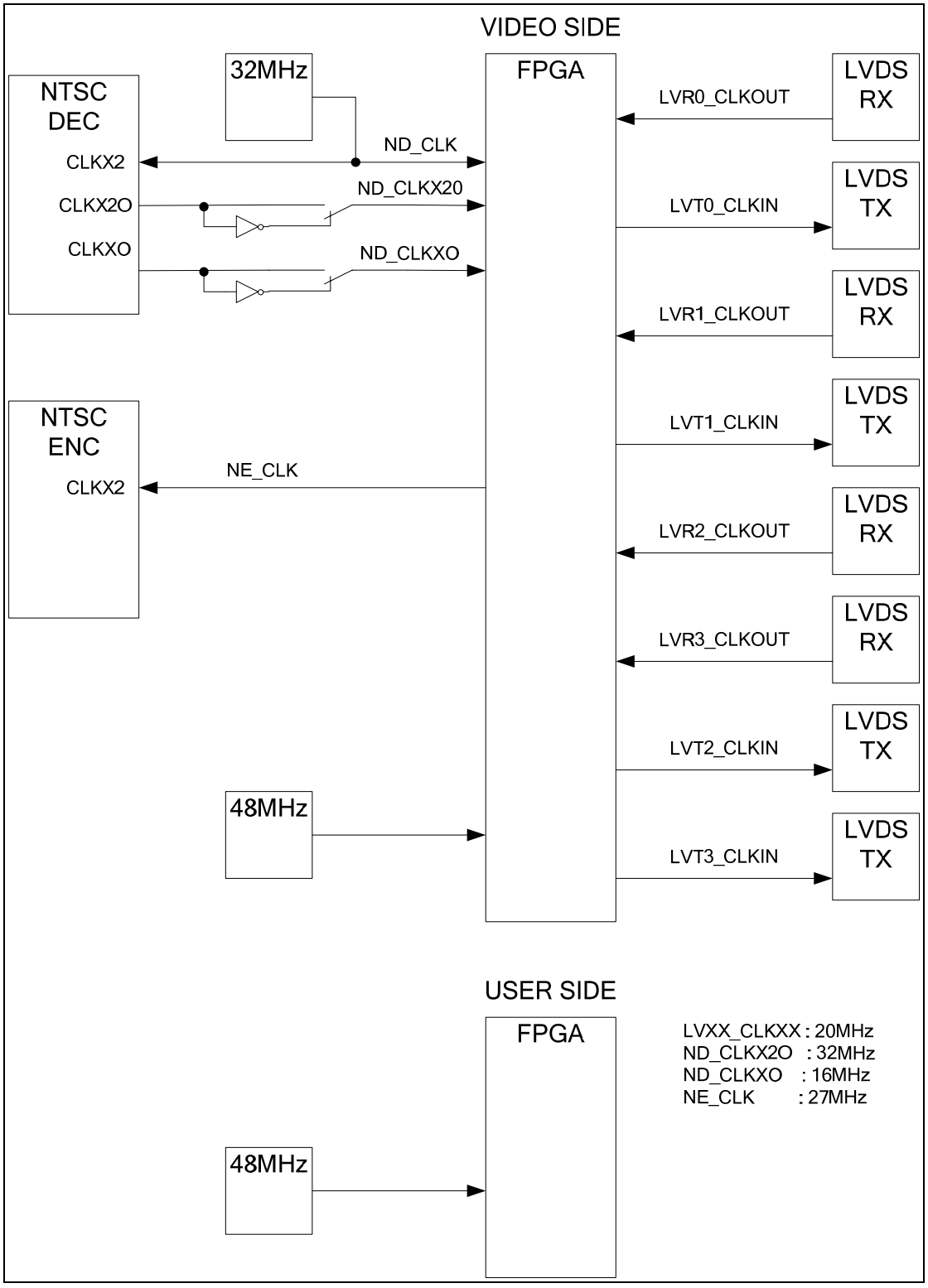
Blue Line : Soft Reset

The following figure describes the reset schematic for the IMAPCAR2 video I/F board reset.



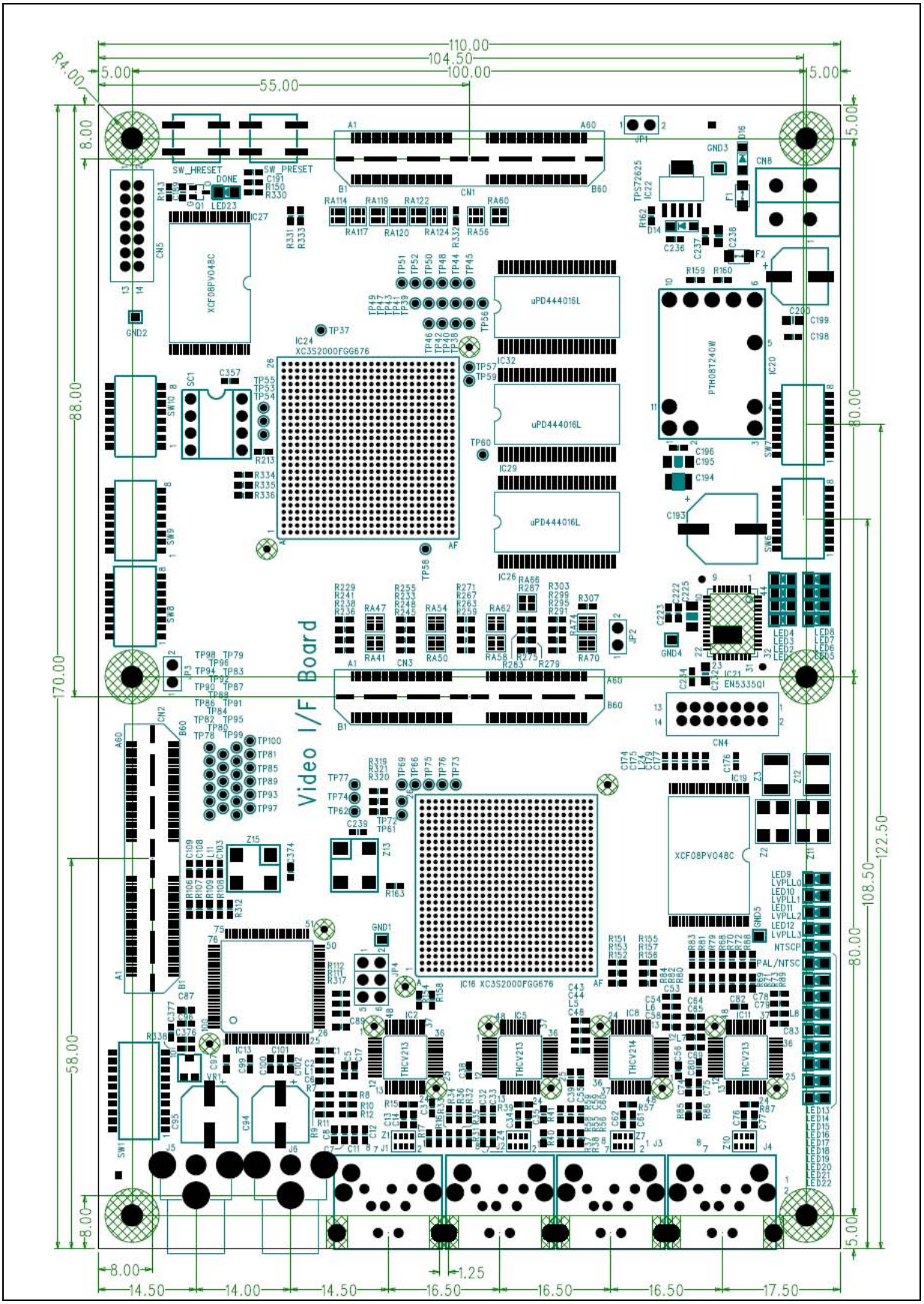
3.4 Clock block diagram

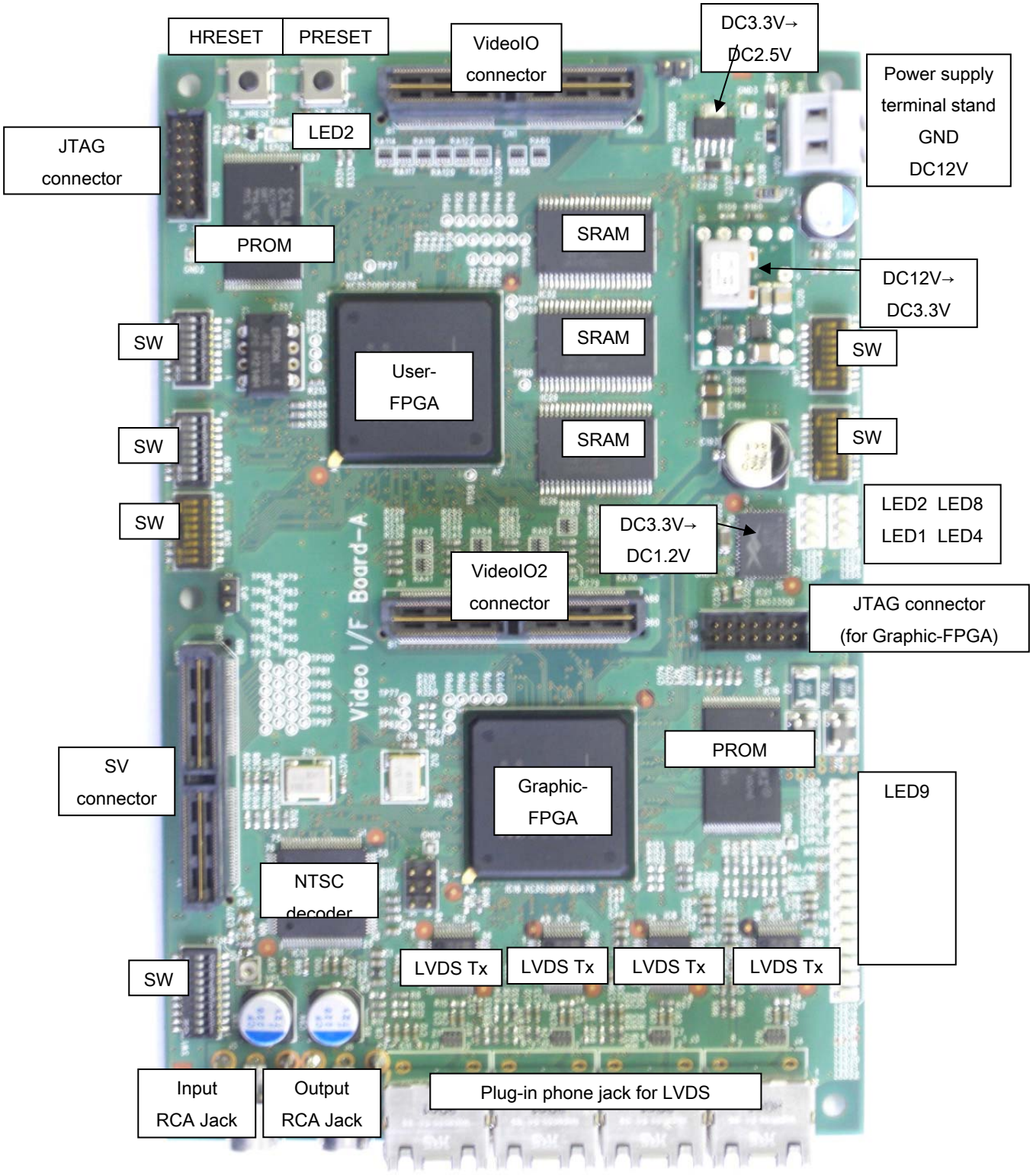
The following figure describes the block diagram of the system clock.

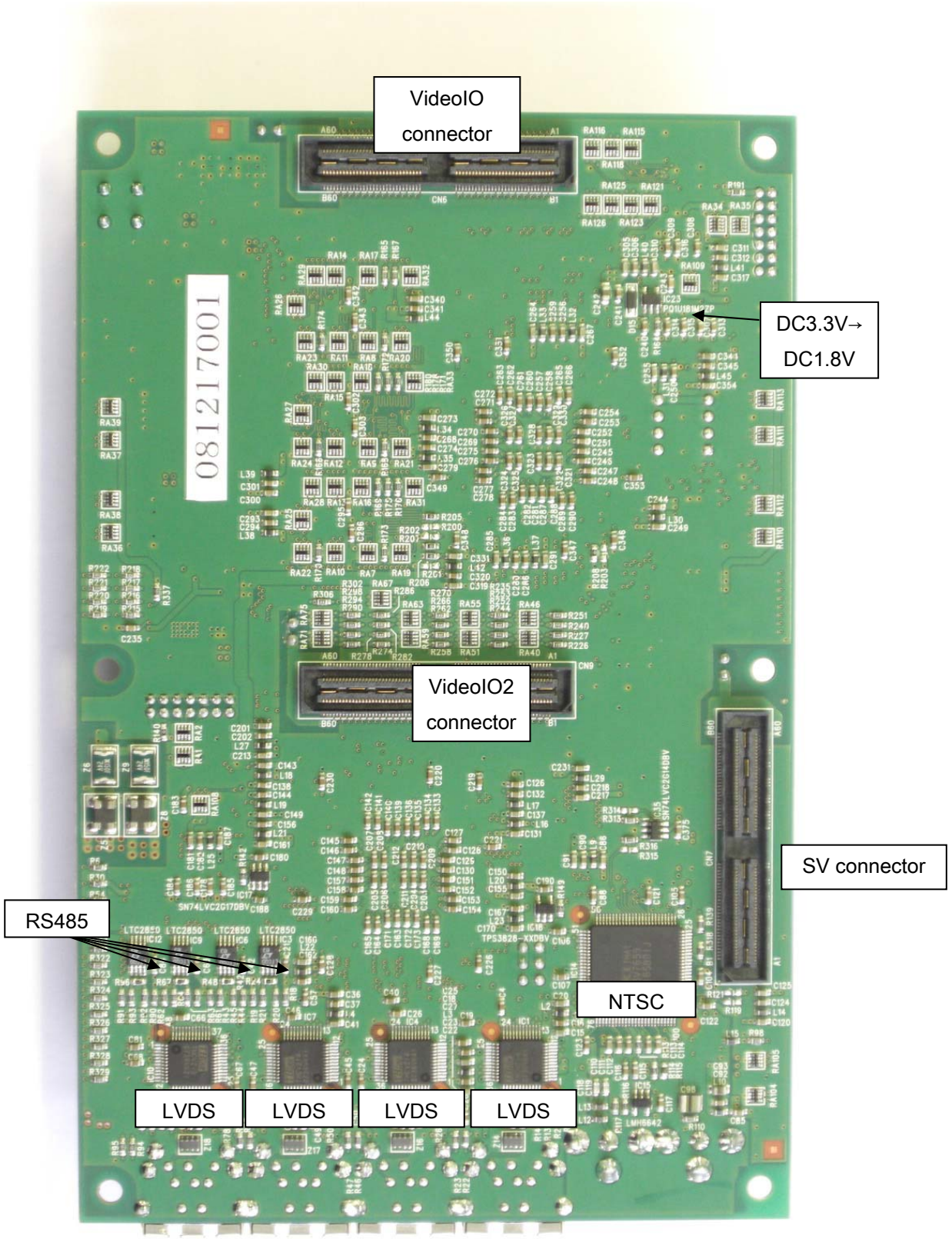


3.5 PCB overview

The following figure shows a PCB overview



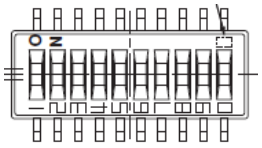

HRESET
PRESET
VideoIO connector
DC3.3V→ DC2.5V
Power supply terminal stand GND DC12V
JTAG connector
LED2
PROM
SRAM
SRAM
SRAM
DC12V→ DC3.3V
SW
SW
User-FPGA
SW
SW
SW
DC3.3V→ DC1.2V
LED2 LED8 LED1 LED4
VideoIO2 connector
JTAG connector (for Graphic-FPGA)
Video I/F Board-A
SV connector
PROM
Graphic-FPGA
LED9
NTSC decoder
SW
LVDS Tx
LVDS Tx
LVDS Tx
LVDS Tx
Input RCA Jack
Output RCA Jack
Plug-in phone jack for LVDS


VideoIO
connector
DC3.3V→
DC1.8V
VideoIO2
connector
SV connector
RS485
NTSC
LVDS
LVDS
LVDS
LVDS

4 Board description

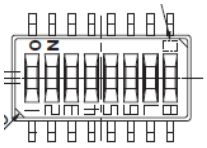
4.1 Switch description

4.1.1 SW1 – NTSC decoder



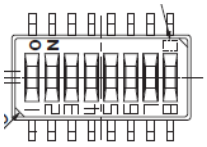
No	Name	Initial Configuration	Description
1	[3 :1] : GAINS 2-0	OFF	Amplifier gain setting SW1.3-1 is active only if SW1.8：OFF [SW1.3-1] Gain values (x times) [OFF：OFF：OFF] 0.55 [OFF：OFF：ON] 0.70 [OFF：ON ：OFF] 0.93 [OFF：ON ：ON] 1.21 [ON ：OFF：OFF] 1.60 [ON ：OFF：ON] 2.09 [ON ：ON ：OFF] 2.65 [ON ：ON ：ON] 3.45 ※SW ON•"1"、OFF•"0"
2		OFF	
3		OFF	
4	[5-4] :MODE 1-0	OFF	Input mode - Register $00/MRA[0]=0 (default value) SW1.5：OFF•NTSC / ON•PAL - Invalid when register $02/MRC[7]=1(NTSC/PAL auto recognition) SW1.4: OFF ->ITU-R BT.601 / ON -> Square Pixel Setting for NTSC 4fsc is available only by register $00/MRA[5:3]. ※SW ON•"1"、OFF•"0"
5		OFF	
6	[7-6] : MODE3-2	OFF	External output pin configuration - Register $00/MRA[0]=0 (default value) [SW1.7-6] [OFF：OFF] ITU-R BT.656(10bit Y/CbCr) [OFF：ON] 10bit Y/CbCr (10bit Y/CbCr+Sync.) [ON ：OFF] 20bit Y/CbCr (10bit Y + 10bit CbCr+Sync.) [ON ：ON] 24bit RGB/YCbCr (RGB orYCbCr 8+8+8bit+Sync.) - Register $10/CHRCB[1]=0：24bitRGB / 1：24bitYCbCr ※SW ON•"1"、OFF•"0"
7		ON	
8	M[8]	OFF	Selecting method to set the amplifier gain and input terminal OFF: External pin mode Amplifier gain setting: use SW1.3-1 Input terminal setting: use pin92-94 INS[2:0] ON: Register mode Amplifier gain setting: use register $1E/ADC2[6:4] Input terminal setting: use register $1D/ADC1[2:0] ※SW ON•"1"、OFF•"0"
9	M[9]	OFF	I2C Slave address selection OFF：1000 001X (X: 0=Write 1=Read) ON ：1000 011X (X: 0=Write 1=Read) ※SW ON•"1"、OFF•"0"
10	Not used	OFF	

4.1.2 SW6 – user FPGA general purpose SW



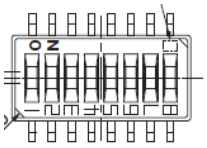
No	Name	Initial Configuration	Description
1	Not used	OFF	
2	Reserved	OFF	
3	Reserved	OFF	
4	Not used	OFF	
5	Not used	OFF	
6	Not used	OFF	
7	Not used	OFF	
8	Not used	OFF	

4.1.3 SW7 - user FPGA general purpose SW



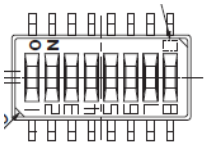
No	Name	Initial Configuration	Description
1	Not used	OFF	
2	Not used	OFF	
3	Not used	OFF	
4	Not used	OFF	
5	Not used	OFF	
6	Not used	OFF	
7	Not used	OFF	
8	Not used	OFF	

4.1.4 SW8 – NTSC encoder



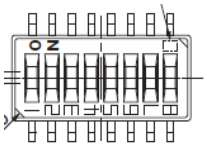
No	Name	Initial Configuration	Description
1	[3 :1] MOD2-0	OFF	Input mode control ※SW ON•"1"、OFF•"0" For more data, please see ML86V7655 data-sheet
2		OFF	
3		OFF	
4	IPAL	OFF	PAL/NTSC mode select ※SW ON•"1"、OFF•"0" ON ：PAL、 OFF：NTSC
5	IRGB	OFF	RGB/YCbCr Input select ※SW ON•"1"、OFF•"0" ON ：RGB Input、 OFF：YCbCr input
6	IPRG	OFF	Progressive / Interlaced input select ※SW ON•"1"、OFF•"0" ON ：Progressive input, OFF：interlaced input
7	I444	OFF	4:2:2/4:4:4 input select ※SW ON•"1"、OFF•"0" ON ：4:4:4 input、 OFF：4:2:2 input
8	OPRD	OFF	Progressive / Interlaced output select ※SW ON•"1"、OFF•"0" ON ：Progressive output, OFF：interlaced output

4.1.5 SW9 – general purpose SW for graphic FPGA



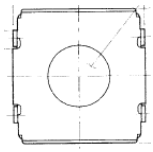
No	Name	Initial Configuration	Description
1	Select Mode	OFF	[SW9.2-1] ※SW ON•"0"、OFF•"1" [ON , ON] : Mode 0 [ON , OFF] : Mode 1 [OFF , ON] : Mode 2 [OFF , OFF] : Mode 3 For details of each mode, please refer to figure 5.1.1 to 5.1.4 When connecting 1394 board, mode is changed to mode 2 forcedly.
2		OFF	
3	Not used	OFF	
4	Not used	OFF	
5	Not used	OFF	
6	Not used	OFF	
7	Not used	OFF	
8	Not used	OFF	

4.1.6 SW10 – general purpose SW for graphic FPGA



No	Name	Initial Configuration	Description
1	reserved	OFF	
2	reserved	OFF	
3	reserved	OFF	
4	reserved	OFF	
5	Not used	OFF	
6	Not used	OFF	
7	Not used	OFF	
8	reserved	OFF	

4.1.7 SW_HRESET

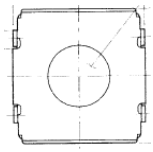


It is a button switch for board reset.

By pushing this switch, the following device will be reset and the FPGA will be reconfigured as well.

- NTSC decoder,
- NTSC encoder, and
- FPGA internal circuit

4.1.8 SW_PRESET



It is a button switch for hard reset.

By pushing this switch, the following device will be reset.

- NTSC decoder,
- NTSC encoder, and
- FPGA internal circuit

4.2 Jumper description

- Power supply (12V) is supplied through the JP1: VideoIO connector.

Please make it to OPEN when it is unnecessary.

  - Initial condition (when the board is shipped by NEC): SHORT.

- Power supply (12V) is supplied through the JP2: VideoIO2 connector.

Please make it to OPEN when it is unnecessary.

  - Initial condition (when the board is shipped by NEC):SHORT.

- Power supply (12V) is supplied through the JP3: SV connector.

Please make it to OPEN when it is unnecessary.

  - Initial condition (when the board is shipped by NEC):SHORT.

- External connecting the I2C bus of JP4: IC13 (NTSC decoder) and IC14 (NTSC encoder) becomes possible.

  - Initial condition (when the board is shipped by NEC):OPEN.

4.3 LED description

The following table describes the LEDS related to user FPGA

No	Color	Name	State after reset	Features
LED1	Green	PLL Lock status	On	PLL Lock : ON PLL unlock : OFF
LED2	Green		Off	
LED3	Green		Off	
LED4	Green		Off	
LED5	Green		Off	
LED6	Green		Off	
LED7	Green		Off	
LED8	Green		Off	

The following table describes the LEDS related to user NTSC device

No	Color	Name	State after reset	Features
LED9	Green	LVDS RX（IC1) PLL LOCK ON：PLL locked OFF：PLL unlocked	Off	LED9 indicates the status of receiving from J1 connector.
LED10	Green	LVDS RX（IC4) PLL LOCK ON：PLL locked OFF：PLL unlocked	Off	LED10 indicates the status of receiving from J2 connector.
LED11	Green	LVDS RX（IC7) PLL LOCK ON：PLL locked OFF：PLL locked	Off	LED11 indicates the status of receiving from J3 connector.
LED12	Green	LVDS RX（IC8) PLL LOCK ON：PLL locked OFF：PLL unlocked	Off	LED12 indicates the status of receiving from J4 connector.
LED13	Green	NTSC decoder (ML86V7666) STATUS1 ON：PLL locked OFF：PLL unlocked	Off	For more details, please check ML86V7666 user's manual
LED14	Green	NTSC decoder (ML86V7667) STATUS2 ON：PAL OFF：NTSC	Off	For more details, please check ML86V7667 user's manual

The following table describes the LEDS related to graphic FPGA

No	Color	Name	State after reset	Features
LED15	Red	Not used	Off	
LED16	Green	Not used	Off	
LED17	Green	Not used	Off	
LED18	Green	Not used	Off	
LED19	Green	Not used	Off	
LED20	Green	Not used	Off	
LED21	Green	Not used	Off	
LED22	Green	Not used	Off	

The following table describes the LEDS related to FPGA reconfiguration completion

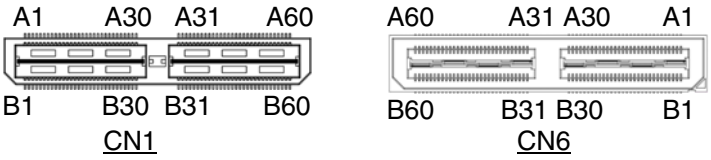
No	Color	Name	Normal State	Features
LED23	Red	FPGA configuration completion ON : config OK OFF : config not OK	ON	Check if the FPGA configuration is finished correctly

4.4 Connector description

4.4.1 Video I/O connector (CN1/CN6)

Manufacturer: SAMTEC

Model: QTH-060-05-L-D-A/QSH-060-01-L-D-A



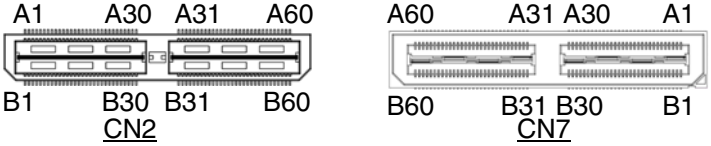
Meaning of the IO field value is seen from Video IF board side.

Description	SignalName	ID	B		A	ID	Signalname	Description
	PID_VID[4]	-	1	N	1	-	UART0_RX/PID_VID[0]	
CAR2VIN Ch0	ODDEVENI[0]	0	2	P	2	-	UART0_TX/PID_VID[2]	
	HSYNCIB[0]	0	3	N	3	0	VSYNCIB[0]	CAR2VIN Ch0
	SCLKI[0]	0	4	P	4	0	SCLK2I[0]	
	ch0_idata[0]/SRI[0]	0	5	N	5	0	ch0_idata[1]/SRI[1]	
	ch0_idata[2]/SRI[2]	0	6	P	6	0	ch0_idata[3]/SRI[3]	
	ch0_idata[4]/SRI[4]	0	7	N	7	0	ch0_idata[5]/SRI[5]	
	ch0_idata[6]/SRI[6]	0	8	P	8	0	ch0_idata[7]/SRI[7]	
	ch0_idata[8]/SRI[8]	0	9	N	9	0	ch0_idata[9]/SRI[9]	
	ch0_idata[10]/SRI[10]	0	10	P	10	0	ch0_idata[11]/SRI[11]	
	ch0_idata[12]	0	11	N	11	0	ch0_idata[13]	
	ch0_idata[14]	0	12	P	12	0	ch0_idata[15]	
	PID_VID[5]	-	13	N	13	-	UART1_RX/PID_VID[1]	
CAR2VIN ch1	ODDEVENI[1]	0	14	P	14	-	UART1_TX/PID_VID[3]	
	HSYNCIB[1]	0	15	N	15	0	VSYNCIB[1]	
	SCLKI[1]	0	16	P	16	0	SCLK2I[1]	
	ch1_idata[0]/SRI[12]	0	17	N	17	0	ch1_idata[1]/SRI[13]	
	ch1_idata[2]/SRI[14]	0	18	P	18	0	ch1_idata[3]/SRI[15]	CAR2VIN ch1
	ch1_idata[4]/SRI[16]	0	19	N	19	0	ch1_idata[5]/SRI[17]	
	ch1_idata[6]/SRI[18]	0	20	P	20	0	ch1_idata[7]/SRI[19]	
	ch1_idata[8]/SRI[20]	0	21	N	21	0	ch1_idata[9]/SRI[21]	
	ch1_idata[10]/SRI[22]	0	22	P	22	0	ch1_idata[11]/SRI[23]	
	ch1_idata[12]	0	23	N	23	0	ch1_idata[13]	
	ch1_idata[14]	0	24	P	24	0	ch1_idata[15]	
	PID_VID[10]	-	25	N	25	-	UART2_RX/PID_VID[6]	
CAR2VIN ch2	ODDEVENI[2]	0	26	P	26	-	UART2_TX/PID_VID[8]	
	HSYNCIB[2]	0	27	N	27	0	VSYNCIB[2]	
	SCLKI[2]	0	28	P	28	0	SCLK2I[2]	
	ch2_idata[0]/SRI[24]	0	29	N	29	0	ch2_idata[1]/SRI[25]	
	ch2_idata[2]/SRI[26]	0	30	P	30	0	ch2_idata[3]/SRI[27]	
	ch2_idata[4]/SRI[28]	0	31	N	31	0	ch2_idata[5]/SRI[29]	CAR2VIN ch2
	ch2_idata[6]/SRI[30]	0	32	P	32	0	ch2_idata[7]/SRI[31]	
	ch2_idata[8]/SRI[32]	0	33	N	33	0	ch2_idata[9]/SRI[33]	
	ch2_idata[10]/SRI[34]	0	34	P	34	0	ch2_idata[11]/SRI[35]	
	ch2_idata[12]/SRI[36]	0	35	N	35	0	ch2_idata[13]/SRI[37]	
	ch2_idata[14]/SRI[38]	0	36	P	36	0	ch2_idata[15]/SRI[39]	
	PID_VID[11]	-	37	N	37	-	UART3_RX/PID_VID[7]	
CAR2VOUTcommo	ODDEVEN00	I	38	P	38	-	UART3_TX/PID_VID[9]	
	HSYNC00B	I	39	N	39	0	VSYNC00B	AR2VOUT commo
	SCLK00	I	40	P	40	0	SCLK200	
CAR2VOUT ch0	ch0_odata[0]/SRO[0]	I	41	N	41	0	ch0_odata[1]/SRO[1]	
	ch0_odata[2]/SRO[2]	I	42	P	42	0	ch0_odata[3]/SRO[3]	CAR2VOUT ch0
	ch0_odata[4]/SRO[4]	I	43	N	43	0	ch0_odata[5]/SRO[5]	
	ch0_odata[6]/SRO[6]	I	44	P	44	0	ch0_odata[7]/SRO[7]	
CAR2VOUT ch1	ch1_odata[0]/SRO[8]	-	45	N	45	-	ch1_odata[1]/SRO[9]	
	ch1_odata[2]/SRO[10]	-	46	P	46	-	ch1_odata[3]/SRO[11]	CAR2VOUT ch1
	ch1_odata[4]/SRO[12]	-	47	N	47	-	ch1_odata[5]/SRO[13]	
	ch1_odata[6]/SRO[14]	-	48	P	48	-	ch1_odata[7]/SRO[15]	
CAR2VOUT ch2	ch2_odata[0]/SRO[16]	I	49	N	49	I	ch2_odata[1]/SRO[17]	
	ch2_odata[2]/SRO[18]	I	50	P	50	I	ch2_odata[3]/SRO[19]	CAR2VOUT ch2
	ch2_odata[4]/SRO[20]	I	51	N	51	I	ch2_odata[5]/SRO[21]	
	ch2_odata[6]/SRO[22]	I	52	P	52	I	ch2_odata[7]/SRO[23]	
	CSID_RX/PID_VID[13]	-	53	N	53	-	CSII_RX/PID_VID[12]	
	CSID_TX/PID_VID[15]	-	54	P	54	-	CSII_TX/PID_VID[14]	
	CSID_CLK/PID_VID[17]	-	55	N	55	-	CSII_CLK/PID_VID[16]	
#7 I2C_SDA	I2C_SDA/PID_VID[19]	ID	56	P	56	I	Camera reset /PID_VID[18]	general purpose port
#7 I2C_SCL	I2C_SCL/PID_VID[21]	ID	57	N	57	I	NTSC decoder reset /PID_VID[20]	general purpose port
Power supply	12V	-	58	P	58	-	12V	Power supply
	12V	-	59	N	59	-	12V	
-	-	-	60	P	60	-	12V	

4.4.2 Supervisor connector (CN2/CN7)

Manufacturer: SAMTEC

Model: QTH-060-05-L-D-A/QSH-060-01-L-D-A



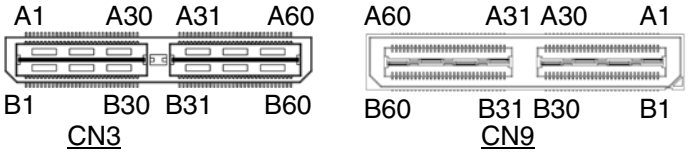
Column B	Pin name	I/O	Description
1	A[2]	I	CPU Bus :Address line
2	A[4]	I	
3	A[6]	I	
4	A[8]	I	
5	A[10]	I	
6	A[12]	I	
7	A[14]	I	
8	A[16]	I	
9	A[18]	I	
10	A[20]	I	
11	A[22]	I	
12	A[24]	I	
13	A[26]	I	
14	A[28]	I	
15	D[0]	IO	CPU Bus :data lines
16	D[2]	IO	
17	D[4]	IO	
18	D[6]	IO	
19	D[8]	IO	
20	D[10]	IO	
21	D[12]	IO	
22	D[14]	IO	
23	WR_B	I	CPU bus :Write signal
24	CS0_B	-	Reserve (FPGA connection)
25	CS1_B	I	CPU Bus :chip select
26	CS2_B	-	Reserve (FPGA connection)
27	YOBIBUSREQ	-	Reserve (FPGA connection)
28	SV_BUSREQ	-	Reserve (FPGA connection)
29	SV_BUSRESET	-	Reserve (FPGA connection)
30	YOBIPORT[3]	-	Reserve (FPGA connection)
31	GLOABAL_HRESET	IO	Hard reset
32	PIO_VID[1]	-	Unsed
33	PIO_VID[3]	-	
34	PIO_VID[5]	-	
35	PIO_VID[7]	-	
36	PIO_VID[9]	-	
37	PIO_VID[11]	-	
38	PIO_VID[13]	-	
39	PIO_VID[15]	-	
40	PIO_VID[17]	-	
41	PIO_VID[19]	-	
42	PIO_VID[21]	-	
43	CAR2_PORT0[1]	-	Spares (FPGA connections)
44	CAR2_PORT0[3]	-	
45	CAR2_PORT0[5]	-	
46	CAR2_PORT0[7]	-	
47	CAR2_PORT0[9]	-	
48	CAR2_PORT1[1]	-	
49	CAR2_PORT1[3]	-	
50	CAR2_PORT1[5]	-	
51	CAR2_INTP[1]	-	Spares (FPGA connections)
52	CAR2_CSICLK	-	
53	CAR2_CSITX	-	
54	CAR2_CSICS	-	
55	CAR2_DCON10	-	
56	CAR2_REGON25	-	
57	GLOABAL_SRESET	I	Soft reset
58	YOBIPORT[2]	-	Spars (FPGA connections)
59	12V	-	power supply
60	-	-	Unsed

Column A	Pin name	I/O	Description
1	A[1]	I	CPU Bus :Address line
2	A[3]	I	
3	A[5]	I	
4	A[7]	I	
5	A[9]	I	
6	A[11]	I	
7	A[13]	I	
8	A[15]	I	
9	A[17]	I	
10	A[19]	I	
11	A[21]	I	
12	A[23]	I	
13	A[25]	I	
14	A[27]	I	
15	D[1]	IO	CPU Bus :data lines
16	D[3]	IO	
17	D[5]	IO	
18	D[7]	IO	
19	D[9]	IO	
20	D[11]	IO	
21	D[13]	IO	
22	D[15]	IO	
23	RD_B	I	CPU bus :Read signal
24	WAIT0_B	-	Reserve (FPGA connection)
25	WAIT1_B	O	CPU bus :Wait signal
26	WAIT2_B	-	Reserve (FPGA connection)
27	YOBIBUSBUSY	-	Reserve (FPGA connection)
28	SV_BUSBUSY	-	Reserve (FPGA connection)
29	SV_BUSSTAT	-	Reserve (FPGA connection)
30	SV_BURST	I-	N.C.
31	GLOABAL_PRESET	IO	Power reset
32	PIO_VID[0]	-	Unsed
33	PIO_VID[2]	-	
34	PIO_VID[4]	-	
35	PIO_VID[6]	-	
36	PIO_VID[8]	-	
37	PIO_VID[10]	-	
38	PIO_VID[12]	-	
39	PIO_VID[14]	-	
40	PIO_VID[16]	-	
41	PIO_VID[18]	-	
42	PIO_VID[20]	-	
43	CAR2_PORT0[0]	-	Spares (FPGA connections)
44	CAR2_PORT0[2]	-	
45	CAR2_PORT0[4]	-	
46	CAR2_PORT0[6]	-	
47	CAR2_PORT0[8]	-	
48	CAR2_PORT1[0]	-	
49	CAR2_PORT1[2]	-	
50	CAR2_PORT1[4]	-	
51	CAR2_INTP[0]	-	Spares (FPGA connections)
52	CAR2_INTP[2]	-	
53	CAR2_CSIRX	-	
54	CAR2_ERROROUT	-	
55	CAR2_HDRSTB	-	
56	CAR2_DCON19	-	
57	CAR2_FAILDC	-	
58	YOBIPORT[1]	-	
59	12V	-	power supply
60	12V	-	

4.4.3 Video I/O connector 2 (CN3/CN9)

Manufacturer: SAMTEC

Model: QTH-060-05-L-D-A/QSH-060-01-L-D-A



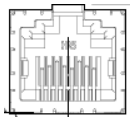
Meaning of the IO field value is seen from 1394 board side.

Features	Signalnames	ID	B		A	ID	SignalNames	Features
Spare	Spare	ID	1	N	1	ID	UART_RX_Pi	Reserved
MAPCAR2 image IF :Ch0	FRAME_VALID_Pi	I	2	P	2	ID	UART_TX_Pi	Reserved
	HSYNC_Pi	I	3	N	3	I	VSYNC_Pi	MAPCAR2 image IF :Ch0
	PCLK_Pi	I	4	P	4	I	PCLK2_Pi	
	D0_Pi	I	5	N	5	I	D1_Pi	
	D2_Pi	I	6	P	6	I	D3_Pi	
	D4_Pi	I	7	N	7	I	D5_Pi	
	D6_Pi	I	8	P	8	I	D7_Pi	
	D8_Pi	I	9	N	9	I	D9_Pi	
Spare	Spare	ID	10	P	10	ID	Spare	Spare
Spare	Spare	ID	11	N	11	ID	Spare	Spare
Spare	Spare	ID	12	P	12	ID	Spare	Spare
Spare	Spare	ID	13	N	13	ID	Spare	Spare
ECU_SJ2 control	CAM_FRM_VALID	I	14	P	14	ID	Spare	Spare
MAPCAR2 image input IF : Ch1 Assign the CPU signals of ECU/SV (reserved)	NBDSYNC#	O	15	N	15	I	NBDEVNT#	MAPCAR2 image input IF : Ch1 Assign the CPU signals of ECU/SV (reserved)
	NBDCLK	O	16	P	16	O	NBDDOE#	
	NBD_DI0	I	17	N	17	I	NBD_DI1	
	NBD_DI2	I	18	P	18	I	NBD_DI3	
	NBD_DO0	O	19	N	19	O	NBD_DO1	
	NBD_DO2	O	20	P	20	O	NBD_DO3	
Reserved	ECU_D8	ID	21	N	21	ID	ECU_D9	Reserved
Reserved	ECU_D10	ID	22	P	22	ID	ECU_D11	Reserved
Spare	Spare	ID	23	N	23	ID	Spare	Spare
Spare	Spare	ID	24	P	24	ID	Spare	Spare
Spare	Spare	ID	25	N	25	ID	UART_RX_Ni	Reserved
MAPCAR2 image IF :Ch2	FRAME_VALID_Ni	I	26	P	26	ID	UART_TX_Ni	Reserved
	HSYNC_Ni	I	27	N	27	I	VSYNC_Ni	MAPCAR2image IF :Ch2
	PCLK_Ni	I	28	P	28	I	PCLK2_Ni	
	D0_Ni	I	29	N	29	I	D1_Ni	
	D2_Ni	I	30	P	30	I	D3_Ni	
	D4_Ni	I	31	N	31	I	D5_Ni	
	D6_Ni	I	32	P	32	I	D7_Ni	
	D8_Ni	I	33	N	33	I	D9_Ni	
Spare	Spare	ID	34	P	34	ID	Spare	Spare
Spare	Spare	ID	35	N	35	ID	Spare	Spare
Spare	Spare	ID	36	P	36	ID	Spare	Spare
Spare	Spare	ID	37	N	37	ID	Spare	Spare
MAPCAR2 image output IF sync signal Common for Ch0, 1, 2	FRAME_VALID_Po	O	38	P	38	ID	Spare	Spare
	HSYNC_Po	O	39	N	39	O	VSYNC_Po	MAPCAR2 image output IF sync signal Common for Ch0, 1, 2
	PCLK_Po	O	40	P	40	O	PCLK2_Po	
MAPCAR2 image output IF : Ch2	D0_Po	O	41	N	41	O	D1_Po	MAPCAR2 image output IF : Ch2
	D2_Po	O	42	P	42	O	D3_Po	
	D4_Po	O	43	N	43	O	D5_Po	
	D6_Po	O	44	P	44	O	D7_Po	
	D8_Po	O	45	N	45	O	D9_Po	
MAPCAR2 image output IF sync signal Common for Ch0, 1, 2	FRAME_VALID_No	O	46	P	46	O	Spare	Spare
	HSYNC_No	O	47	N	47	O	VSYNC_No	MAPCAR2 image output IF sync signal Common for Ch0, 1, 2
	PCLK_No	O	48	P	48	O	PCLK2_No	
MAPCAR2 IF :Ch0	D0_No	O	49	N	49	O	D1_No	MAPCAR2 inahe IF Ch0
	D2_No	O	50	P	50	O	D3_No	
	D4_No	O	51	N	51	O	D5_No	
	D6_No	O	52	P	52	O	D7_No	
	D8_No	O	53	N	53	O	D9_No	
Spare	Spare	ID	54	P	54	O	Reserved (NTSC_RESET_B)	Reserved (Reset signal for NTSC encoder/decoder IC. dedicated signal to Video IF
1394board RESET output	1394_RESET_B	O	55	N	55	O	Reserved (CAMERA_RESET_B)	Reserved (Reset signal for parallel camera. dedicated signal to Video IF board)
Reserved	I2C_SDA	ID	56	P	56	O	OE_Po	Control parallel output '0' : 1394 board output '1' : Video IF board output
Reserved	I2C_SCL	ID	57	N	57	O	OE_No	Control NTSC output '0' : 1394 board output '1' : Video IF board output

4.4.4 Plug-in phone jack for CH0 differential motion (J1)

Manufacturer: Hirose

Model: TM24RSG-5A-88

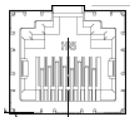


Pin Number	Signal Name	Direction of the signal (from FPGA point of view)	Description
1	CN0_RX+	Input	LVDS differential motion reception line + side
2	CN0_RX-	Input	LVDS differential motion reception line - side
3	UART0A	Input/Output	RS485 differential signal + side
4	CN0_TX+	Input	LVDS differential motion transmission line + side
5	CN0_TX-	Input	LVDS differential motion transmission line + side
6	UART0B	Input/output	RS485 differential signal - side
7	DC12V	-	Power supply line (DC12C°
8	GND	-	GND

4.4.5 Plug-in phone jack for CH1 differential motion (J2)

Manufacturer: Hirose

Model: TM24RSG-5A-88

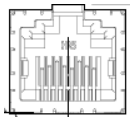


Pin Number	Signal Name	Direction of the signal (from FPGA point of view)	Description
1	CN1_RX+	Input	LVDS differential motion reception line + side
2	CN1_RX-	Input	LVDS differential motion reception line - side
3	UART1A	Input/Output	RS485 differential signal + side
4	CN1_TX+	Input	LVDS differential motion transmission line + side
5	CN1_TX-	Input	LVDS differential motion transmission line + side
6	UART1B	Input/output	RS485 differential signal - side
7	DC12V	-	Power supply line (DC12C°
8	GND	-	GND

4.4.6 Plug-in phone jack for CH2 differential motion (J3)

Manufacturer: Hirose

Model: TM24RSG-5A-88

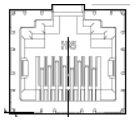


Pin Number	Signal Name	Direction of the signal (from FPGA point of view)	Description
1	CN2_RX0+	Input	LVDS differential motion reception line + side
2	CN2_RX0-	Input	LVDS differential motion reception line - side
3	UART2A	Input/Output	RS485 differential signal + side
4	CN2_RX1+	Input	LVDS differential motion transmission line + side
5	CN2_RX1-	Input	LVDS differential motion transmission line + side
6	UART2B	Input/output	RS485 differential signal - side
7	DC12V	-	Power supply line (DC12C)
8	GND	-	GND

4.4.7 Plug-in phone jack for CH3 differential motion (J4)

Manufacturer: Hirose

Model: TM24RSG-5A-88



Pin Number	Signal Name	Direction of the signal (from FPGA point of view)	Description
1	CN3_TX0+	Input	LVDS differential motion reception line + side
2	CN3_TX0-	Input	LVDS differential motion reception line - side
3	UART3A	Input/Output	RS485 differential signal + side
4	CN3_TX1+	Input	LVDS differential motion transmission line + side
5	CN3_TX1-	Input	LVDS differential motion transmission line + side
6	UART3B	Input/output	RS485 differential signal - side
7	DC12V	-	Power supply line (DC12C°
8	GND	-	GND

4.4.8 NTSC input RCA Jack (J5)

Manufacturer: CUI INC

Model: RCJ-013

RCA Jack: White

4.4.9 NTSC output RCA Jack (J6)

Manufacturer: CUI INC

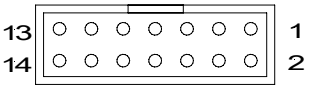
Model: RCJ-011

RCA Jack: Black

4.4.10 JTAG connector

Manufacturer: MOLEX

Model: 87331-142



Pin Number	Signal Name	Description
1	GND	Ground
2	VCC_2.5V	Power supply (2.5V)
3	GND	Ground
4	TMS	Test Mode Select / 2.5V pull-up
5	GND	Ground
6	TCK	Test Clock / 2.5V pull-up
7	GND	Ground
8	TDO	Test Data Output / 2.5V pull-up
9	GND	Ground
10	TDI	Test Data Input / 2.5V pull-up
11	GND	Ground
12	N.C.	-
13	GND	Ground
13	N.C.	-

4.4.11 Power supply terminal stand (CN8)

Manufacturer: Sato

Model: ML-950-2

Pin Number	Signal Name	Description
1	+12V	Power supply (+12V)
2	+12V	Power supply (+12V)
3	GND	Ground
4	GND	Ground

5 Hardware component

5.1 FPGA

Supplier: XILINX

Model XC3S2000-4FGG676C 676pinBGA

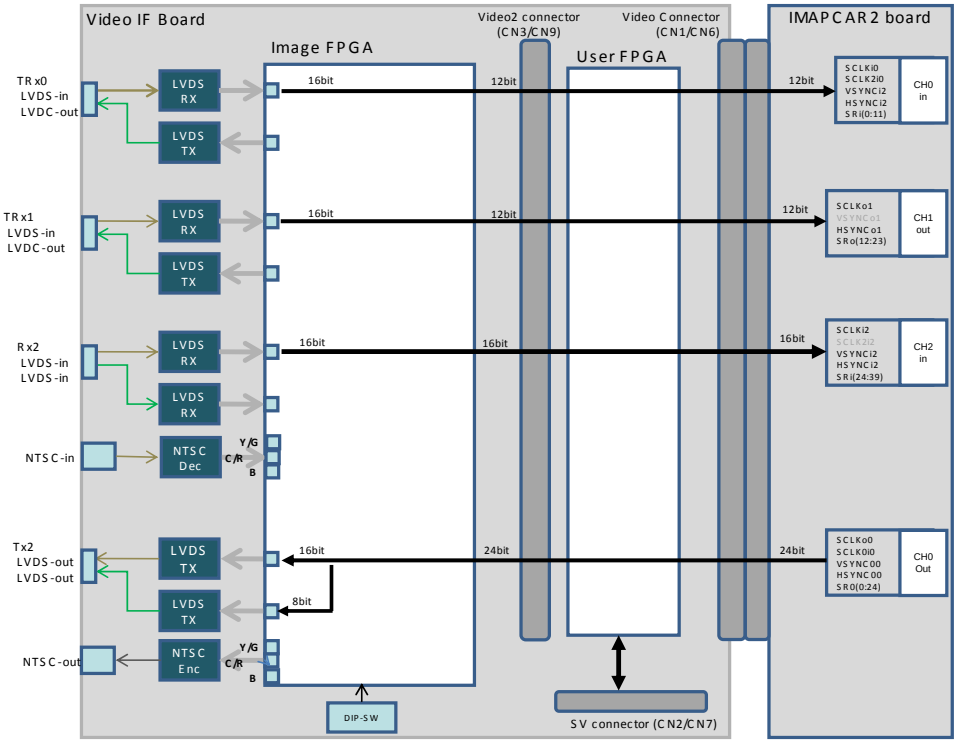
5.1.1 Image System Block

(1)Overview

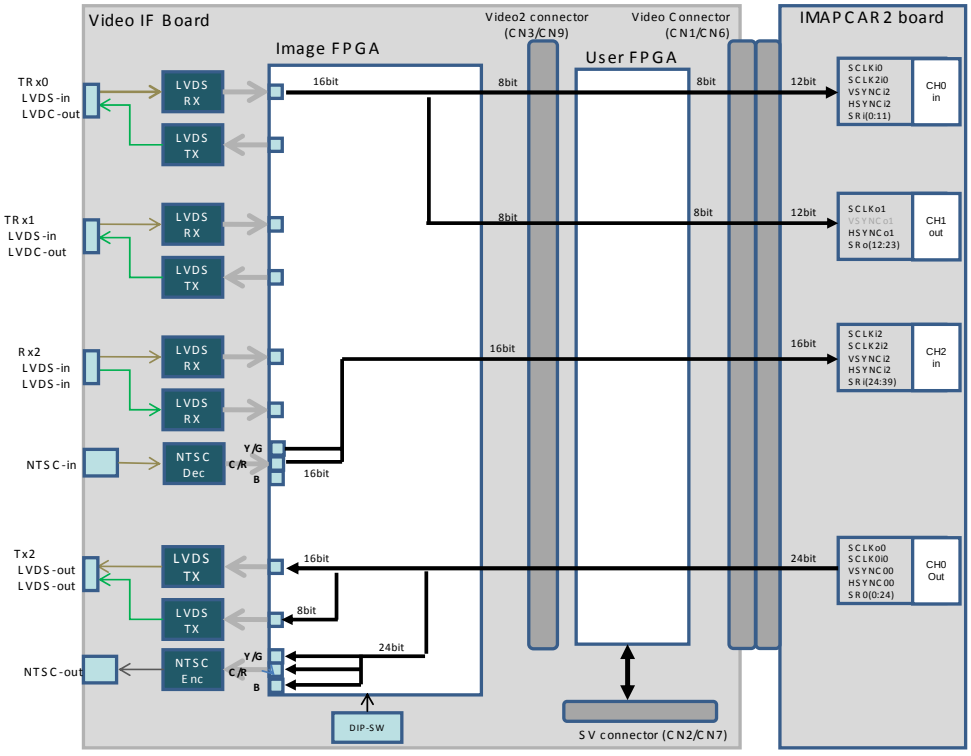
Image System Block is based on Thine IF and NTSC decoder/encoder IF.

Six types of the configuration for the image can be selected by setting the DIP switch (SW9.1-3).

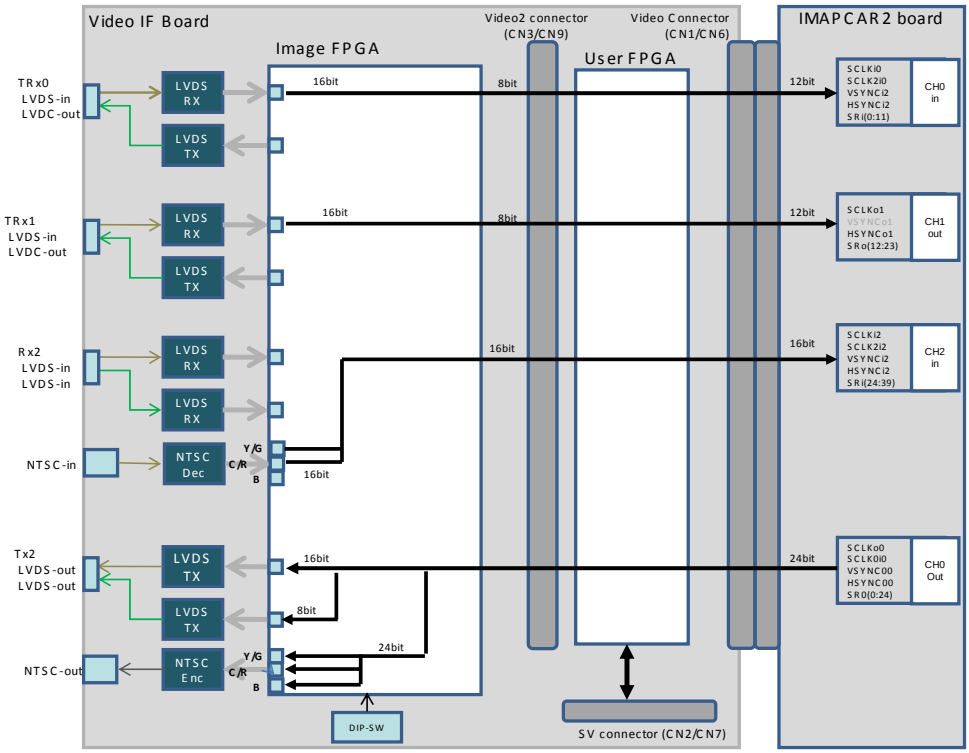
Mode	SW9			Description
	3	2	1	
Mode 0	OFF	OFF	OFF	Input 3ch images from the progressive camera to IMAPCAR2
Mode 1	OFF	OFF	ON	Input 2ch images from the progressive camera (2ch color images) to IMAPCAR2
Mode 2	OFF	ON	OFF	Input 2ch images from the progressive camera and the NTSC camera image to IMAPCAR2 Output the NTSC camera image from the NTSC encoder
Mode 3	OFF	ON	ON	Input 1ch images from the progressive camera and the NTSC camera image to IMAPCAR2. Output the NTSC camera image from the NTSC encoder.
Mode 4	ON	OFF	OFF	Output back the NTSC image for cascading the video interface boards (for transmission)
Mode 5	ON	OFF	ON	For cascading the video interface boards (for reception)



Internal composition of FPGA chart mode 0 (image system)

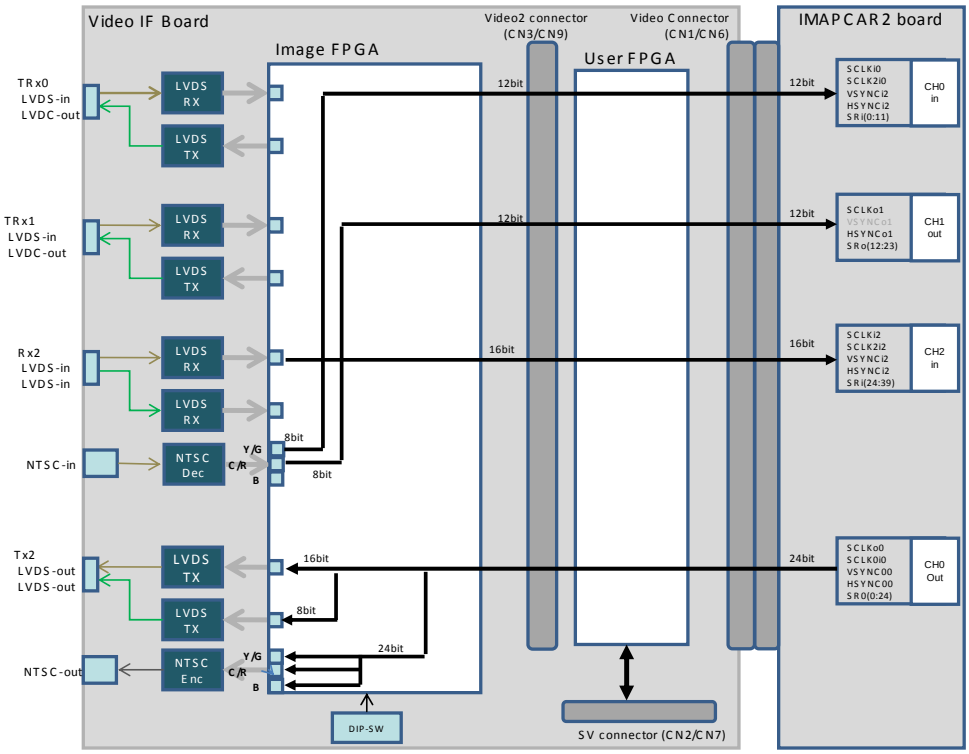


Internal composition of FPGA chart mode 1 (image system)

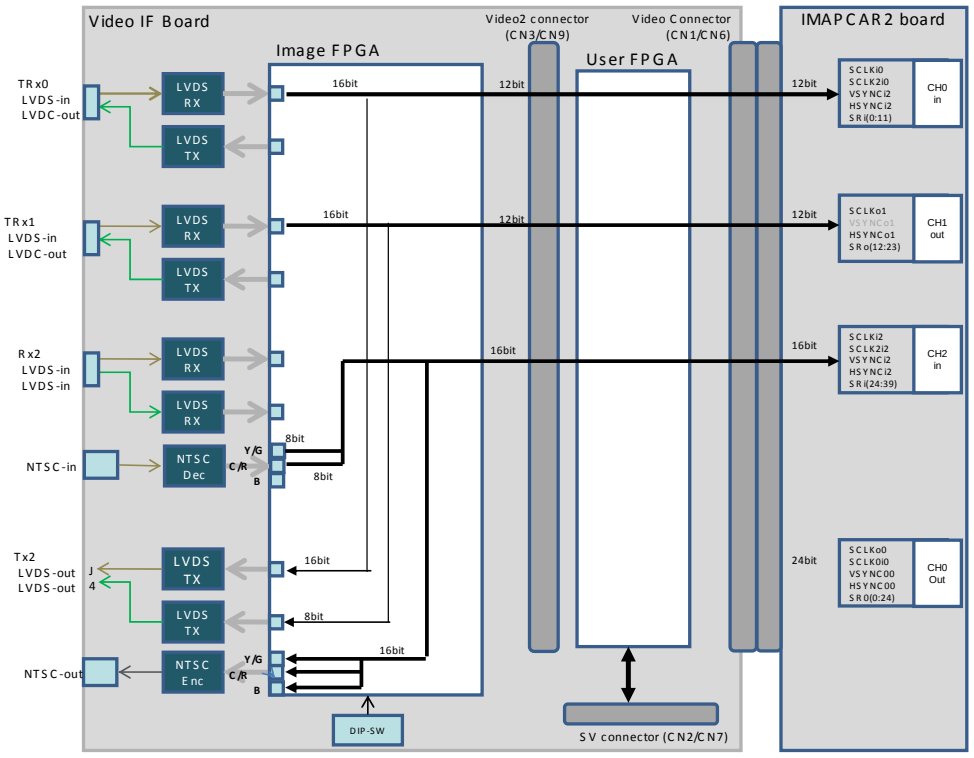


III

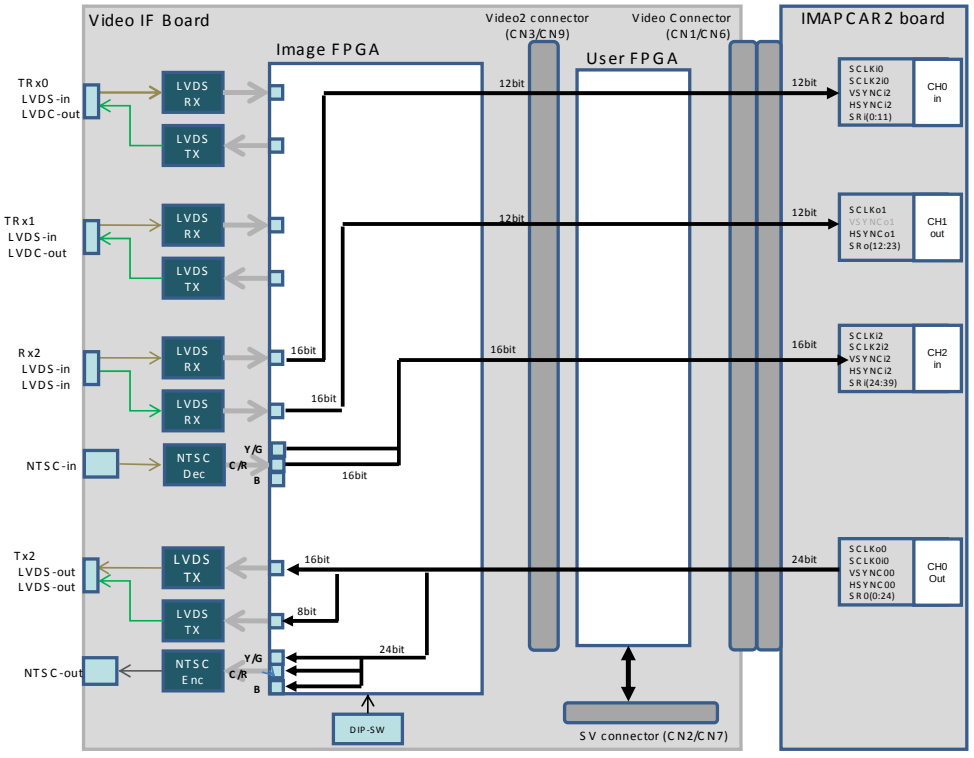
Internal composition of FPGA chart mode 2 (image system)



Internal composition of FPGA chart mode 3 (image system)



Internal composition of FPGA chart mode 4 (image system)



Internal composition of FPGA chart mode 5 (image system)

5.1.2 Communication system block

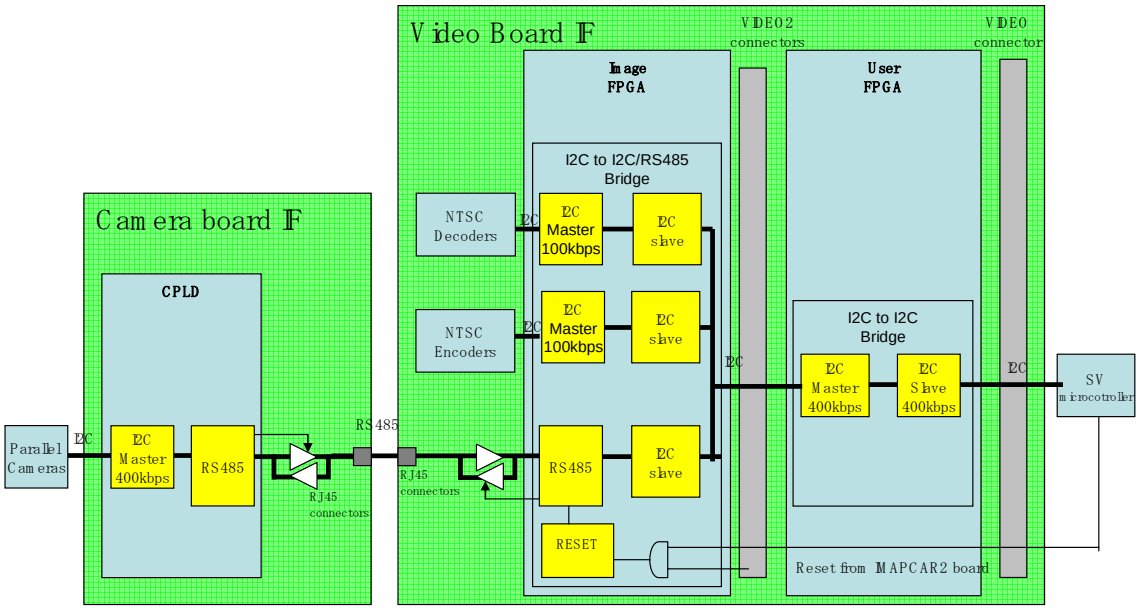
(1) Overview

- Another equipment connected with the plug-in phone jack can be controlled by the control and the I2C⇔RS485 conversion function of NTSC encoder/decoder device by I2C.

  (However, the RS485⇔I2C conversion function is needed on the connected equipment side.)

- It is possible to reset camera IF board by the port control by Host (SV microcomputer and 1394 boards). This reset is done via the RS485 communication.

Communication route outline is shown below.

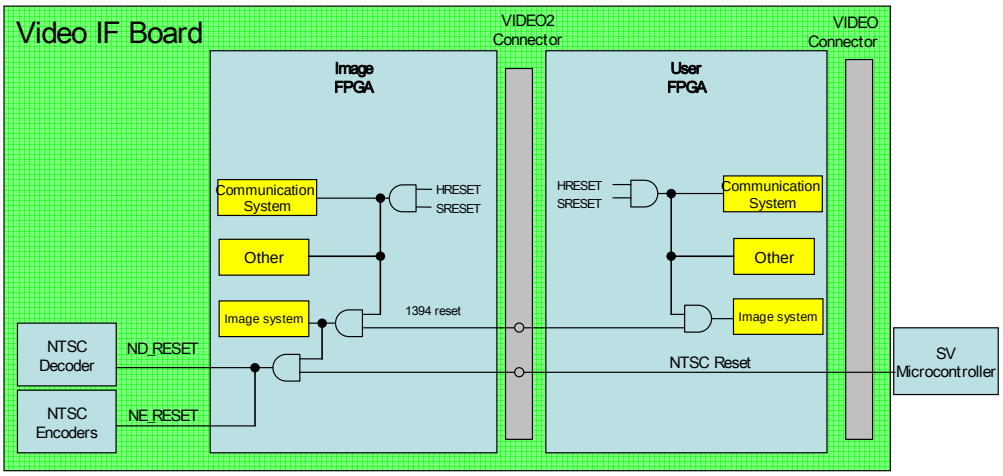


Internal composition of FPGA chart (I2C/ RS485 communication system)

5.1.3 Reset block

The reset signal is generated in FPGA as follows.

- HRESET is an equivalent signal to DX_DONE.



5.1.4 Pin assignment

The following tables describes the user FPGA pin assign

A1	GND	C1	TDI	E1	NE_STANDBY	G1	ND_HVALID	J1	2.5V
A2	2.5V	C2	HSWAP_EN	E2	ND_RESET_L	G2	ND_VVALID	J2	LVR1_LOCK
A3	NE_SDA	C3	GND	E3	ND_SCL	G3	3.3V	J3	LVR0_LOCK
A4	NE_SCL	C4	NE_CD9	E4	ND_SDA	G4	ND_VSYNC_L	J4	LVR3_LOCK
A5	ND_CSYNC_SCALR	C5	NE_CD8	E5	ND_C9	G5	ND_HSYNC_L	J5	LVR2_LOCK
A6	ND_VHVAL_SCALW	C6	NE_CD7	E6	ND_C8	G6	ND_ODD_EVENB	J6	LVT1_SYNC0
A7	VIDEO2_B13	C7	3.3V	E7	ND_C7	G7	ND_CLKX0	J7	LVT3_SYNC1
A8	VIDEO2_B11	C8	NE_CD6	E8	ND_C6	G8	VIDEO2_B12	J8	3.3V
A9	2.5V	C9	NE_CD5	E9	ND_C5	G9	VIDEO2_B10	J9	1.2V
A10	VIDEO2_B1	C10	NE_CD4	E10	ND_C4	G10	VIDEO2_B23	J10	1.2V
A11	ND_STATUS1	C11	3.3V	E11	ND_C3	G11	ND_CLKX20	J11	3.3V
A12	NE_RESET_L	C12	NE_CD3	E12	ND_C2	G12	LVT0_SYNC0	J12	3.3V
A13	SYS_CLK_P	C13	NE_CD2	E13	ND_C1	G13	NE_CLK	J13	3.3V
A14	NE_VSYNC_L	C14	NE_CD1	E14	ND_C0	G14	GROBAL_SRESET	J14	3.3V
A15	VIDEO2_A38	C15	VIDEO2_A57	E15	NE_OLR	G15	P_TEST_LED8	J15	3.3V
A16	P_TEST_LED6	C16	3.3V	E16	P_TEST_LED4	G16	P_TEST_LED2	J16	3.3V
A17	P_TEST_SW16	C17	*Reserved*	E17	P_TEST_SW15	G17	P_TEST_SW13	J17	1.2V
A18	2.5V	C18	P_TEST_SW11	E18	RESERVED_B3	G18	VIDEO2_A46	J18	1.2V
A19	P_TEST_SW8	C19	P_TEST_SW6	E19	P_TEST_SW4	G19	*Reserved*	J19	3.3V
A20	P_TEST_SW2	C20	3.3V	E20	P_TEST_SW1	G20	*Reserved*	J20	*Reserved*
A21	VIDEO2_A55	C21	*Reserved*	E21	*Reserved*	G21	*Reserved*	J21	*Reserved*
A22	RESERVED_B0	C22	*Reserved*	E22	*Reserved*	G22	*Reserved*	J22	*Reserved*
A23	RESERVED_B1	C23	*Reserved*	E23	RESERVED_C1	G23	*Reserved*	J23	*Reserved*
A24	TMS	C24	GND	E24	RESERVED_C2	G24	3.3V	J24	*Reserved*
A25	2.5V	C25	RESERVED_C0	E25	RESERVED_C4	G25	*Reserved*	J25	*Reserved*
A26	GND	C26	VIDEO2_A36	E26	VIDEO2_A34	G26	VIDEO2_A23	J26	2.5V
B1	2.5V	D1	NE_CD0	F1	ND_B5	H1	LVT2_SYNC1	K1	LVR0_SYNC0
B2	GND	D2	NE_BD9	F2	ND_B4	H2	LVT2_SYNC2	K2	LVR0_SYNC1
B3	NE_HSYNC_L	D3	PROG_B	F3	ND_B3	H3	LVT1_SYNC2	K3	LVR0_SYNC2
B4	NE_BLANK_L	D4	GND	F4	ND_B2	H4	LVT2_SYNC0	K4	LVR1_SYNC0
B5	NE_YD9	D5	NE_BD8	F5	ND_Y0	H5	LVT1_SYNC1	K5	LVR1_SYNC1
B6	NE_YD8	D6	NE_BD7	F6	ND_Y1	H6	LVT0_SYNC1	K6	LVT3_SYNC2
B7	NE_YD7	D7	NE_BD6	F7	ND_Y2	H7	LVT0_SYNC2	K7	LVT3_SYNC0
B8	NE_YD6	D8	NE_BD5	F8	ND_Y3	H8	1.2V	K8	3.3V
B9	NE_YD5	D9	NE_BD4	F9	ND_Y4	H9	3.3V	K9	1.2V
B10	NE_YD4	D10	NE_BD3	F10	ND_Y5	H10	3.3V	K10	1.2V
B11	NE_YD3	D11	NE_BD2	F11	ND_Y6	H11	VIDEO2_B34	K11	GND
B12	NE_YD2	D12	GND	F12	ND_Y7	H12	VIDEO2_B24	K12	GND
B13	NE_YD1	D13	NE_BD1	F13	ND_Y8	H13	ND_CLK	K13	3.3V
B14	NE_YD0	D14	NE_BD0	F14	ND_Y9	H14	NE_OLB	K14	3.3V
B15	VIDEO2_A37	D15	GND	F15	NE_OLG	H15	NE_OLC	K15	GND
B16	P_TEST_LED7	D16	RESERVED_B2	F16	P_TEST_LED5	H16	P_TEST_LED3	K16	GND
B17	P_TEST_LED1	D17	P_TEST_SW14	F17	P_TEST_SW12	H17	3.3V	K17	1.2V
B18	P_TEST_SW10	D18	VIDEO2_A56	F18	VIDEO2_A54	H18	3.3V	K18	1.2V
B19	P_TEST_SW9	D19	P_TEST_SW7	F19	P_TEST_SW5	H19	1.2V	K19	3.3V
B20	P_TEST_SW3	D20	CAR2_CSITX	F20	RESERVED_B4	H20	*Reserved*	K20	*Reserved*
B21	CAR2_CSIRX	D21	CAR2_CSICLK	F21	*Reserved*	H21	*Reserved*	K21	*Reserved*
B22	*Reserved*	D22	*Reserved*	F22	N.C.	H22	*Reserved*	K22	*Reserved*
B23	*Reserved*	D23	GND	F23	*Reserved*	H23	*Reserved*	K23	*Reserved*
B24	TCK	D24	TDO	F24	*Reserved*	H24	*Reserved*	K24	*Reserved*
B25	GND	D25	RESERVED_C3	F25	*Reserved*	H25	*Reserved*	K25	*Reserved*
B26	2.5V	D26	VIDEO2_A35	F26	VIDEO2_A24	H26	VIDEO2_A14	K26	VIDEO2_A13

L1	LVR1_SYNC2	N1	LVT0_D13	R1	LVR0_D9	U1	LVT1_D2
L2	LVR2_SYNC0	N2	LVT0_D12	R2	LVR0_D10	U2	LVT1_D1
L3	3.3V	N3	LVT0_D11	R3	LVR0_D11	U3	LVT1_D0
L4	LVR2_SYNC1	N4	LVT0_D10	R4	GND	U4	LVT1_DE
L5	LVR2_SYNC2	N5	LVT0_D9	R5	LVR0_D12	U5	LVR0_DE
L6	LVR3_SYNC0	N6	LVT0_D8	R6	LVR0_D13	U6	LVR0_D0
L7	LVR3_SYNC1	N7	LVT0_D7	R7	LVR0_D14	U7	LVR0_D1
L8	LVR3_SYNC2	N8	LVT0_D6	R8	LVR0_D15	U8	3.3V
L9	3.3V	N9	3.3V	R9	3.3V	U9	1.2V
L10	GND	N10	3.3V	R10	GND	U10	1.2V
L11	GND	N11	GND	R11	GND	U11	GND
L12	GND	N12	GND	R12	GND	U12	GND
L13	GND	N13	GND	R13	GND	U13	3.3V
L14	GND	N14	GND	R14	GND	U14	3.3V
L15	GND	N15	GND	R15	GND	U15	GND
L16	GND	N16	GND	R16	GND	U16	GND
L17	GND	N17	3.3V	R17	GND	U17	1.2V
L18	3.3V	N18	3.3V	R18	3.3V	U18	1.2V
L19	*Reserved*	N19	VIDEO2_B54	R19	VIDEO2_A9	U19	3.3V
L20	*Reserved*	N20	VIDEO2_B37	R20	VIDEO2_B2	U20	VIDEO2_A20
L21	*Reserved*	N21	*Reserved*	R21	VIDEO2_B3	U21	VIDEO2_A21
L22	VIDEO2_A12	N22	VIDEO2_B36	R22	VIDEO2_B4	U22	VIDEO2_A22
L23	*Reserved*	N23	*Reserved*	R23	GND	U23	VIDEO2_B14
L24	3.3V	N24	*Reserved*	R24	VIDEO2_B5	U24	VIDEO2_B15
L25	*Reserved*	N25	*Reserved*	R25	VIDEO2_B6	U25	VIDEO2_B16
L26	VIDEO2_A11	N26	VIDEO2_B35	R26	VIDEO2_B7	U26	VIDEO2_B17
M1	LVT0_D5	P1	LVR0_D16	T1	LVR0_D2	V1	2.5V
M2	LVT0_D4	P2	LVR0_D17	T2	LVR0_D3	V2	LVT1_D8
M3	LVT0_D3	P3	LVR0_CLKOUT	T3	3.3V	V3	LVT1_D7
M4	GND	P4	LVT0_CLKIN	T4	LVR0_D4	V4	LVT1_D6
M5	LVT0_D2	P5	LVT0_D17	T5	LVR0_D5	V5	LVT1_D5
M6	LVT0_D1	P6	LVT0_D16	T6	LVR0_D6	V6	LVT1_D4
M7	LVT0_D0	P7	LVT0_D15	T7	LVR0_D7	V7	LVT1_D3
M8	LVT0_DE	P8	LVT0_D14	T8	LVR0_D8	V8	3.3V
M9	3.3V	P9	3.3V	T9	3.3V	V9	1.2V
M10	GND	P10	3.3V	T10	GND	V10	1.2V
M11	GND	P11	GND	T11	GND	V11	3.3V
M12	GND	P12	GND	T12	GND	V12	3.3V
M13	GND	P13	GND	T13	GND	V13	3.3V
M14	GND	P14	GND	T14	GND	V14	3.3V
M15	GND	P15	GND	T15	GND	V15	3.3V
M16	GND	P16	GND	T16	GND	V16	3.3V
M17	GND	P17	3.3V	T17	GND	V17	1.2V
M18	3.3V	P18	3.3V	T18	3.3V	V18	1.2V
M19	*Reserved*	P19	VIDEO2_A1	T19	VIDEO2_B8	V19	3.3V
M20	*Reserved*	P20	VIDEO2_A2	T20	VIDEO2_B9	V20	VIDEO2_B18
M21	*Reserved*	P21	VIDEO2_A3	T21	VIDEO2_A15	V21	VIDEO2_B19
M22	VIDEO2_A10	P22	VIDEO2_A4	T22	VIDEO2_A16	V22	VIDEO2_B20
M23	GND	P23	VIDEO2_A5	T23	VIDEO2_A17	V23	VIDEO2_B21
M24	*Reserved*	P24	VIDEO2_A6	T24	3.3V	V24	VIDEO2_B22
M25	*Reserved*	P25	VIDEO2_A7	T25	VIDEO2_A18	V25	VIDEO2_A25
M26	VIDEO2_B55	P26	VIDEO2_A8	T26	VIDEO2_A19	V26	2.5V

W1	LVT1_D15	AA1	LVR1_D12	AC1	LVR1_D4	AE1	2.5V
W2	LVT1_D14	AA2	LVR1_D13	AC2	LVR1_D5	AE2	GND
W3	LVT1_D13	AA3	LVR1_D14	AC3	M1	AE3	M0
W4	LVT1_D12	AA4	LVR1_D15	AC4	GND	AE4	LVR1_D0
W5	LVT1_D11	AA5	ND_STATUS2	AC5	LVR1_D6	AE5	LVT2_D0
W6	LVT1_D10	AA6	LVT2_D2	AC6	LVT2_D4	AE6	LVT2_D6
W7	LVT1_D9	AA7	LVT2_D8	AC7	LVT2_D10	AE7	LVT2_D11
W8	1.2V	AA8	LVT2_D14	AC8	LVT2_D16	AE8	LVT2_CLKIN
W9	3.3V	AA9	LVR2_D16	AC9	LVR2_D14	AE9	LVR2_D12
W10	3.3V	AA10	LVR2_D10	AC10	LVR2_D8	AE10	LVR2_D6
W11	LVR2_D4	AA11	LVR2_D2	AC11	LVR2_D0	AE11	LVR2_DE
W12	LVT3_D0	AA12	LVT3_D2	AC12	GND	AE12	LVT3_D5
W13	LVT3_D7	AA13	LVT3_D9	AC13	LVT3_D11	AE13	LVT3_D13
W14	LVT3_D15	AA14	LVT3_D17	AC14	INT_B/	AE14	LVR3_CLKOUT
W15	LVR3_D16	AA15	LVR3_D15	AC15	GND	AE15	LVR3_D12
W16	LVR3_D10	AA16	LVR3_D8	AC16	LVR3_D6	AE16	LVR3_D5
W17	3.3V	AA17	LVR3_D2	AC17	LVR3_D0	AE17	UART3_EN
W18	3.3V	AA18	UART1_EN	AC18	UART2_EN	AE18	UART3_DI
W19	1.2V	AA19	UART0_EN	AC19	UART2_DI	AE19	VIDEO2_B51
W20	VIDEO2_A26	AA20	VIDEO2_B30	AC20	VIDEO2_B41	AE20	VIDEO2_B52
W21	VIDEO2_A27	AA21	VIDEO2_B31	AC21	VIDEO2_B42	AE21	VIDEO2_B53
W22	VIDEO2_A28	AA22	VIDEO2_B32	AC22	VIDEO2_B43	AE22	VIDEO2_A47
W23	VIDEO2_A29	AA23	VIDEO2_B33	AC23	GND	AE23	VIDEO2_A48
W24	VIDEO2_A30	AA24	VIDEO2_A39	AC24	DONE	AE24	VIDEO2_A49
W25	VIDEO2_A31	AA25	VIDEO2_A40	AC25	VIDEO2_B44	AE25	GND
W26	VIDEO2_A32	AA26	VIDEO2_A41	AC26	VIDEO2_B45	AE26	2.5V
Y1	LVR1_D16	AB1	LVR1_D7	AD1	LVR1_D1	AF1	GND
Y2	LVR1_D17	AB2	LVR1_D8	AD2	LVR1_D2	AF2	2.5V
Y3	3.3V	AB3	LVR1_D9	AD3	GND	AF3	M2
Y4	LVR1_CLKOUT	AB4	LVR1_D10	AD4	LVR1_D3	AF4	LVR1_DE
Y5	LVT1_CLKIN	AB5	LVR1_D11	AD5	LVT2_DE	AF5	LVT2_D1
Y6	LVT1_D17	AB6	LVT2_D3	AD6	LVT2_D5	AF6	LVT2_D7
Y7	LVT1_D16	AB7	LVT2_D9	AD7	3.3V	AF7	LVT2_D12
Y8	LVT2_D13	AB8	LVT2_D15	AD8	LVT2_D17	AF8	LVR2_CLKOUT
Y9	LVR2_D17	AB9	LVR2_D15	AD9	LVR2_D13	AF9	2.5V
Y10	LVR2_D11	AB10	LVR2_D9	AD10	LVR2_D7	AF10	LVR2_D5
Y11	LVR2_D3	AB11	LVR2_D1	AD11	3.3V	AF11	LVT3_DE
Y12	LVT3_D1	AB12	LVT3_D3	AD12	LVT3_D4	AF12	LVT3_D6
Y13	LVT3_D8	AB13	LVT3_D10	AD13	LVT3_D12	AF13	LVT3_D14
Y14	LVT3_D16	AB14	LVT3_CLKIN	AD14	DX_DONE	AF14	LVR3_D17
Y15	DIN/D0/	AB15	LVR3_D14	AD15	LVR3_D13	AF15	LVR3_D11
Y16	LVR3_D9	AB16	LVR3_D7	AD16	3.3V	AF16	LVR3_D4
Y17	LVR3_D3	AB17	LVR3_D1	AD17	LVR3_DE	AF17	UART3_RO
Y18	UART1_DI	AB18	UART1_RO	AD18	UART2_RO	AF18	2.5V
Y19	UART0_DI	AB19	UART0_RO	AD19	VIDEO2_B46	AF19	VIDEO2_A50
Y20	VIDEO2_A33	AB20	VIDEO2_A42	AD20	3.3V	AF20	VIDEO2_A51
Y21	VIDEO2_B25	AB21	VIDEO2_A43	AD21	VIDEO2_B47	AF21	VIDEO2_A52
Y22	VIDEO2_B26	AB22	VIDEO2_A44	AD22	VIDEO2_B48	AF22	VIDEO2_A53
Y23	VIDEO2_B27	AB23	VIDEO2_A45	AD23	VIDEO2_B49	AF23	VIDEO2_B56
Y24	3.3V	AB24	VIDEO2_B38	AD24	GND	AF24	VIDEO2_B57
Y25	VIDEO2_B28	AB25	VIDEO2_B39	AD25	VIDEO2_B50	AF25	2.5V
Y26	VIDEO2_B29	AB26	VIDEO2_B40	AD26	CCLK	AF26	GND

A1	GND	C1	TDI	E1	A2	G1	VIDEO2_B1	J1	2.5V
A2	2.5V	C2	HSWAP_EN	E2	A6	G2	A4	J2	VIDEO2_B5
A3	A11	C3	GND	E3	A9	G3	3.3V	J3	VIDEO2_A5
A4	A17	C4	A15	E4	A14	G4	A12	J4	VIDEO2_B6
A5	A24	C5	A22	E5	A20	G5	A18	J5	VIDEO2_A6
A6	D3	C6	D1	E6	A27	G6	A25	J6	VIDEO2_B7
A7	D9	C7	3.3V	E7	D4	G7	D2	J7	VIDEO2_A7
A8	D14	C8	D12	E8	D10	G8	D8	J8	3.3V
A9	2.5V	C9	WAIT_B1	E9	WAIT_B0	G9	RD_B	J9	1.2V
A10	CAR2_PORT01	C10	YOBIPORT3	E10	YOBIBUSBUSY	G10	WAIT_B2	J10	1.2V
A11	CAR2_PORT08	C11	3.3V	E11	CAR2_PORT05	G11	CAR2_PORT03	J11	3.3V
A12	CAR2_PORT15	C12	CAR2_PORT13	E12	CAR2_PORT12	G12	CAR2_PORT10	J12	3.3V
A13	SYS_CLK	C13	CAR2_CSITX	E13	CAR2_CSICLK	G13	CAR2_INTP1	J13	3.3V
A14	YOBIPORT2	C14	*RESERVED_B1*	E14	GROBAL_SRESET	G14	CAR2_ERROROUT	J14	3.3V
A15	PIO_VIO0	C15	PIO_VIO4	E15	ODDEVEN10	G15	HSYNCIB0	J15	3.3V
A16	CH0_ID1	C16	3.3V	E16	CH0_ID2	G16	CH0_ID4	J16	3.3V
A17	CH0_ID6	C17	CH0_ID8	E17	CH0_ID10	G17	CH0_ID12	J17	1.2V
A18	2.5V	C18	CH0_ID14	E18	ODDEVEN11	G18	PIO_VIO3	J18	1.2V
A19	VSYNCIB1	C19	SCLK211	E19	CH1_ID1	G19	CH1_ID3	J19	3.3V
A20	CH1_ID2	C20	3.3V	E20	CH1_ID7	G20	CH1_ID9	J20	CH1_ID11
A21	PIO_VIO8	C21	VSYNCIB2	E21	SCLK212	G21	CH2_ID1	J21	CH2_ID3
A22	CH2_ID6	C22	CH2_ID8	E22	CH2_ID10	G22	CH2_ID13	J22	CH2_ID15
A23	ODDEVEN00	C23	HSYNC00_B	E23	SCLK200	G23	CH0_OD1	J23	CH0_OD3
A24	TMS	C24	GND	E24	CH0_OD7	G24	3.3V	J24	CH1_OD0
A25	2.5V	C25	CH1_OD4	E25	CH1_OD6	G25	CH2_OD0	J25	CH2_OD2
A26	GND	C26	PIO_VIO12	E26	PIO_VIO14	G26	PIO_VIO16	J26	2.5V
B1	2.5V	D1	A3	F1	A1	H1	VIDEO2_A1	K1	VIDEO2_B8
B2	GND	D2	A7	F2	A5	H2	VIDEO2_B2	K2	VIDEO2_A8
B3	A10	D3	PROG_B	F3	A8	H3	VIDEO2_A2	K3	VIDEO2_B9
B4	A16	D4	GND	F4	A13	H4	VIDEO2_B3	K4	VIDEO2_A9
B5	A23	D5	A21	F5	A19	H5	VIDEO2_A3	K5	VIDEO2_B10
B6	D0	D6	A28	F6	A26	H6	VIDEO2_B4	K6	VIDEO2_A10
B7	D6	D7	D7	F7	D5	H7	VIDEO2_A4	K7	VIDEO2_B11
B8	D15	D8	D13	F8	D11	H8	1.2V	K8	3.3V
B9	CS_B1	D9	CS_B0	F9	WR_B	H9	3.3V	K9	1.2V
B10	CAR2_PORT00	D10	YOBIBUSREQ	F10	CS_B2	H10	3.3V	K10	1.2V
B11	CAR2_PORT07	D11	CAR2_PORT06	F11	CAR2_PORT04	H11	CAR2_PORT02	K11	GND
B12	CAR2_PORT14	D12	GND	F12	CAR2_PORT11	H12	CAR2_PORT09	K12	GND
B13	*RESERVED_A0*	D13	CAR2_CSIRX	F13	CAR2_INTP2	H13	CAR2_INTP0	K13	3.3V
B14	*RESERVED_B0*	D14	YOBIPORT1	F14	CAR2_CSICS	H14	SCLK10	K14	3.3V
B15	PIO_VIO2	D15	GND	F15	VSYNCIB0	H15	SCLK210	K15	GND
B16	CH0_ID0	D16	CH0_ID3	F16	CH0_ID5	H16	CH0_ID7	K16	GND
B17	CH0_ID9	D17	CH0_ID11	F17	CH0_ID13	H17	3.3V	K17	1.2V
B18	CH0_ID15	D18	PIO_VIO5	F18	PIO_VIO1	H18	3.3V	K18	1.2V
B19	HSYNCIB1	D19	SCLK11	F19	CH1_ID0	H19	1.2V	K19	3.3V
B20	CH1_ID5	D20	CH1_ID4	F20	CH1_ID6	H20	CH1_ID8	K20	CH1_ID10
B21	ODDEVEN12	D21	HSYNCIB2	F21	SCLK12	H21	CH2_ID0	K21	CH2_ID2
B22	CH2_ID9	D22	CH2_ID11	F22	*RESERVED_C0*	H22	CH2_ID12	K22	CH2_ID14
B23	VSYNC00_B	D23	GND	F23	SCLK00	H23	CH0_OD0	K23	CH0_OD2
B24	TCK	D24	TDO	F24	CH0_OD6	H24	CH1_OD1	K24	CH1_OD3
B25	GND	D25	CH1_OD7	F25	CH2_OD1	H25	CH2_OD3	K25	CH2_OD5
B26	2.5V	D26	PIO_VIO13	F26	PIO_VIO15	H26	PIO_VIO17	K26	PIO_VIO18

L1	VIDEO2_A11	N1	VIDEO2_A18	R1	VIDEO2_A26	U1	VIDEO2_A33
L2	VIDEO2_B12	N2	VIDEO2_B19	R2	VIDEO2_B27	U2	VIDEO2_B34
L3	3.3V	N3	VIDEO2_A19	R3	VIDEO2_A27	U3	VIDEO2_A34
L4	VIDEO2_A12	N4	VIDEO2_B20	R4	GND	U4	VIDEO2_B35
L5	VIDEO2_B13	N5	VIDEO2_A20	R5	VIDEO2_B28	U5	VIDEO2_A35
L6	VIDEO2_A13	N6	VIDEO2_B21	R6	VIDEO2_A28	U6	VIDEO2_B36
L7	VIDEO2_B14	N7	VIDEO2_A21	R7	VIDEO2_B29	U7	VIDEO2_A36
L8	VIDEO2_A14	N8	VIDEO2_B22	R8	VIDEO2_A29	U8	3.3V
L9	3.3V	N9	3.3V	R9	3.3V	U9	1.2V
L10	GND	N10	3.3V	R10	GND	U10	1.2V
L11	GND	N11	GND	R11	GND	U11	GND
L12	GND	N12	GND	R12	GND	U12	GND
L13	GND	N13	GND	R13	GND	U13	3.3V
L14	GND	N14	GND	R14	GND	U14	3.3V
L15	GND	N15	GND	R15	GND	U15	GND
L16	GND	N16	GND	R16	GND	U16	GND
L17	GND	N17	3.3V	R17	GND	U17	1.2V
L18	3.3V	N18	3.3V	R18	3.3V	U18	1.2V
L19	CH1_ID12	N19	PIO_VIO10	R19	TEST_LED1	U19	3.3V
L20	CH1_ID13	N20	PIO_VIO6	R20	TEST_LED2	U20	TEST_LED8
L21	CH2_ID5	N21	CH2_ID7	R21	TEST_LED3	U21	SV_BUSBUSY
L22	PIO_VIO7	N22	PIO_VIO9	R22	TEST_LED4	U22	SV_BUSREQ
L23	CH0_OD5	N23	CH0_OD4	R23	GND	U23	SV_BUSSTAT
L24	3.3V	N24	CH1_OD5	R24	TEST_LED5	U24	SV_BUSRESET
L25	CH2_OD4	N25	CH2_OD6	R25	TEST_LED6	U25	DX_DONE
L26	PIO_VIO19	N26	PIO_VIO21	R26	TEST_LED7	U26	SV_BURST
M1	VIDEO2_B15	P1	VIDEO2_A22	T1	VIDEO2_B30	V1	2.5V
M2	VIDEO2_A15	P2	VIDEO2_B23	T2	VIDEO2_A30	V2	VIDEO2_B37
M3	VIDEO2_B16	P3	VIDEO2_A23	T3	3.3V	V3	VIDEO2_A37
M4	GND	P4	VIDEO2_B24	T4	VIDEO2_B31	V4	VIDEO2_B38
M5	VIDEO2_A16	P5	VIDEO2_A24	T5	VIDEO2_A31	V5	VIDEO2_A38
M6	VIDEO2_B17	P6	VIDEO2_B25	T6	VIDEO2_B32	V6	VIDEO2_B39
M7	VIDEO2_A17	P7	VIDEO2_A25	T7	VIDEO2_A32	V7	VIDEO2_A39
M8	VIDEO2_B18	P8	VIDEO2_B26	T8	VIDEO2_B33	V8	3.3V
M9	3.3V	P9	3.3V	T9	3.3V	V9	1.2V
M10	GND	P10	3.3V	T10	GND	V10	1.2V
M11	GND	P11	GND	T11	GND	V11	3.3V
M12	GND	P12	GND	T12	GND	V12	3.3V
M13	GND	P13	GND	T13	GND	V13	3.3V
M14	GND	P14	GND	T14	GND	V14	3.3V
M15	GND	P15	GND	T15	GND	V15	3.3V
M16	GND	P16	GND	T16	GND	V16	3.3V
M17	GND	P17	3.3V	T17	GND	V17	1.2V
M18	3.3V	P18	3.3V	T18	3.3V	V18	1.2V
M19	CH1_ID14	P19	TEST_SW1	T19	TEST_SW9	V19	3.3V
M20	CH1_ID15	P20	TEST_SW2	T20	TEST_SW10	V20	TEST_SW16
M21	CH2_ID4	P21	TEST_SW3	T21	TEST_SW11	V21	TP48
M22	PIO_VIO11	P22	TEST_SW4	T22	TEST_SW12	V22	TP50
M23	GND	P23	TEST_SW5	T23	TEST_SW13	V23	TP49
M24	CH1_OD2	P24	TEST_SW6	T24	3.3V	V24	TP52
M25	CH2_OD7	P25	TEST_SW7	T25	TEST_SW14	V25	*RESERVED_D10*
M26	PIO_VIO20	P26	TEST_SW8	T26	TEST_SW15	V26	2.5V

W1	VIDEO2_B40	AA1	VIDEO2_B48	AC1	VIDEO2_A56	AE1	2.5V
W2	VIDEO2_A40	AA2	VIDEO2_A48	AC2	VIDEO2_B57	AE2	GND
W3	VIDEO2_B41	AA3	VIDEO2_B49	AC3	M1	AE3	M0
W4	VIDEO2_A41	AA4	VIDEO2_A49	AC4	GND	AE4	SR0_A6
W5	VIDEO2_B42	AA5	*RESERVED_G0*	AC5	VIDEO2_A57	AE5	SR0_IO8
W6	VIDEO2_A42	AA6	VIDEO2_B50	AC6	SR0_IO6	AE6	SR0_IO4
W7	VIDEO2_B43	AA7	VIDEO2_A50	AC7	SR0_IO2	AE7	SR0_IO1
W8	1.2V	AA8	VIDEO2_B51	AC8	SR0_A4	AE8	SR0_A2
W9	3.3V	AA9	VIDEO2_A51	AC9	SR0_A0	AE9	SR0_A16
W10	3.3V	AA10	SR0_A15	AC10	SRAM0_UBB	AE10	SR0_IO16
W11	SR0_IO14	AA11	SR0_IO12	AC11	SR0_IO10	AE11	SR0_IO9
W12	SR0_A13	AA12	SR0_A11	AC12	GND	AE12	SR1_A8
W13	SR1_A6	AA13	SRAM1_WEB	AC13	SR1_IO7	AE13	SR1_IO5
W14	SR1_IO3	AA14	SR1_IO1	AC14	X_INT	AE14	SR1_A4
W15	SR1_A2	AA15	SR1_A1	AC15	GND	AE15	SR1_A16
W16	SRAM1_OEB	AA16	SRAM1_LBB	AC16	SR1_IO15	AE16	SR1_IO14
W17	3.3V	AA17	SR1_IO11	AC17	SR1_IO9	AE17	SR1_A13
W18	3.3V	AA18	SR1_A10	AC18	SR2_A8	AE18	SR2_A6
W19	1.2V	AA19	SRAM2_WEB	AC19	SR2_IO7	AE19	SR2_IO5
W20	*RESERVED_D7*	AA20	SR1_IO2	AC20	SRAM2_CSB	AE20	SR2_A4
W21	*RESERVED_D6*	AA21	SR2_A1	AC21	SR2_A17	AE21	SR2_A15
W22	CAR2_HDRSTB	AA22	SRAM2_LBB	AC22	SR2_IO15	AE22	SR2_IO13
W23	CAR2_DCON19	AA23	SR2_IO10	AC23	GND	AE23	SR2_A13
W24	CAR2_DCON10	AA24	SR2_A11	AC24	DONE	AE24	*RESERVED_E1*
W25	CAR2_FAILDC	AA25	*RESERVED_D5*	AC25	*RESERVED_D1*	AE25	GND
W26	CAR2_REGON25	AA26	*RESERVED_D4*	AC26	*RESERVED_D0*	AE26	2.5V
Y1	VIDEO2_A43	AB1	VIDEO2_B52	AD1	SR0_A9	AF1	GND
Y2	VIDEO2_B44	AB2	VIDEO2_A52	AD2	SR0_A8	AF2	2.5V
Y3	3.3V	AB3	VIDEO2_B53	AD3	GND	AF3	M2
Y4	VIDEO2_A44	AB4	VIDEO2_A53	AD4	SR0_A7	AF4	SR0_A5
Y5	VIDEO2_B45	AB5	VIDEO2_B54	AD5	SRAM0_WEB	AF5	SR0_IO7
Y6	VIDEO2_A45	AB6	VIDEO2_A54	AD6	SR0_IO5	AF6	SR0_IO3
Y7	VIDEO2_B46	AB7	VIDEO2_B55	AD7	3.3V	AF7	SRAM0_CSB
Y8	VIDEO2_A46	AB8	VIDEO2_A55	AD8	SR0_A3	AF8	SR0_A1
Y9	VIDEO2_B47	AB9	VIDEO2_B56	AD9	SR0_A17	AF9	2.5V
Y10	VIDEO2_A47	AB10	SRAM0_OEB	AD10	SRAM0_LBB	AF10	SR0_IO15
Y11	SR0_IO13	AB11	SR0_IO11	AD11	3.3V	AF11	SR0_A14
Y12	SR0_A12	AB12	SR0_A10	AD12	SR1_A9	AF12	SR1_A7
Y13	SR1_A5	AB13	SR1_IO8	AD13	SR1_IO6	AF13	SR1_IO4
Y14	SR2_IO2	AB14	SRAM1_CSB	AD14	*RESERVED_E3*	AF14	SR1_A3
Y15	OP_DO	AB15	SR1_A0	AD15	SR1_A17	AF15	SR1_A15
Y16	SRAM1_UBB	AB16	SR1_IO16	AD16	3.3V	AF16	SR1_IO13
Y17	SR1_IO12	AB17	SR1_IO10	AD17	SR1_A14	AF17	SR1_A12
Y18	SR1_A11	AB18	SR2_A9	AD18	SR2_A7	AF18	2.5V
Y19	SR2_A5	AB19	SR2_IO8	AD19	SR2_IO6	AF19	SR2_IO4
Y20	SR2_IO3	AB20	SR2_IO1	AD20	3.3V	AF20	SR2_A3
Y21	SR2_A2	AB21	SR2_A0	AD21	SR2_A16	AF21	SRAM2_OEB
Y22	SRAM2_UBB	AB22	SR2_IO16	AD22	SR2_IO14	AF22	SR2_IO12
Y23	SR2_IO11	AB23	SR2_IO9	AD23	SR2_A14	AF23	SR2_A12
Y24	3.3V	AB24	SR2_A10	AD24	GND	AF24	*RESERVED_E2*
Y25	*RESERVED_D9*	AB25	*RESERVED_D3*	AD25	*RESERVED_E0*	AF25	2.5V
Y26	*RESERVED_D8*	AB26	*RESERVED_D2*	AD26	CCLK	AF26	GND

5.2 FPGA ROM configuration

Supplier : Xilinx

Model : XCF08PVOG48C 48pinTSOP

For more information, please refer to the Platform Flash In-System Programmable Configuration PROMS data sheet.

5.3 High speed status random access memory

Supplier : NEC

Model : ML86V7655 μPD444016LG5-A8-7JF-A 44pinTSOP

Features

- 262,144 words by 16 bits organization
- Fast access time : 8, 10, 12 ns (MAX.)
- Byte data control : /LB (I/O1 – I/O8), /UB (I/O9 – I/O16)
- Output Enable input for easy application
- 3.3 V single power supply

For more information, please refer to the uPD444016L data sheet.

5.4 LVDS

Supplier : Thine

Model : THCV213 48pinTQFP / THCV214 48pinTQFP

Features

- Transmit 18bit data and 4bit control data through a
- single differential cable
- Wide frequency range: 5MHz to 40MHz
- Support INIT pattern and LOCK indicator
- Pre Emphasis Mode
- Clock Edge Selectable
- Dual Display Mode
- Power Down Mode
- Low power single 3.3V CMOS design
- 48pin TQFP/QFN

For more information, please refer to the THCV213/THC214 data sheet.

5.5 NTSC decoder/encoder

Supplier : OKI

Model : ML86V7655 / ML86V7656 100pinTQFP

Features

- Supported video type: NTSC/PAL
- Scanning method: Interlace/Progressive/Single-field signals
- Input data format
  - o ITU-R BT.656-4 type (Y/CbCr 4:2:2 10-bit multiplexing, synchronization signal information added)
  - o ITU-R BT.601 (Y/CbCr 4:2:2 20-bit non-multiplexing (Y/CbCr 4:1:1 20-bit non-multiplexing)
  - o Y/CbCr 4:2:2 10-bit multiplexing, without synchronization signal
  - o YCbCr 4:2:2 20-bit non-multiplexing (progressive)
  - o YCbCr 4:4:4 30-bit/24-bit non-multiplexing (interlaced/progressive)
  - o RGB 4:4:4 30-bit/24-bit non-multiplexing (interlaced/progressive)
- Input pixel frequency (Input double-speed clock frequency)
  - o 12.272727 MHz (24.545454 MHz): NTSC Square Pixel
  - o 13.5 MHz (27 MHz): NTSC/PAL ITU-R BT.601
  - o 14.318182 MHz (28.636364 MHz): NTSC 4fsc
  - o 14.75 MHz (29.5 MHz): PAL Square Pixel
  - o 18 MHz (36 MHz): NTSC/PAL ITU-R BT.601 wide
- Output format
  - o Composite (CVBS)
  - o S-Video (Y/C separate signals)
  - o RGB (Interlace/Progressive)
  - o YCbCr component (Interlace/Progressive)
- Scan type conversion function / Color space conversion function
  - o Interlace to Progressive / Progressive to Interlace
  - o YCbCr to RGB / RGB to YCbCr
- Built-in 6ch 11-bit DAC: Capable of simultaneous output of composite, S-video, YCbCr or RGB
- Output load resistance: 300 Ohm (A video amp is required when a TV monitor is connected.)
- Master/Slave operation (Slave only for ITU-R BT.656 mode)
- Color bar output
- 3-bit title graphic input interface
- Luminance adjustment
- RGB gain adjustment
- Expanded luminance range mode

- Synchronization signal level adjustment
- CGMS/WSS information adding function
- Supports Macrovision copyguard function (only available in the ML86V7656)
  - o Conforms to version 7.1.L1 for interlace
  - o Conforms to version 1.2 for progressive
- I2C-bus type serial interface
- Supply voltage: 3.3 V (I/O supply)/2.5 V (core supply) (SCL and SDA pins only, 5 V tolerant)
- Package: 100-pin plastic TQFP (TQFP100-P-1414-0.5-K) (ML86V7655TB/ML86V7656TB)

For more information, please refer to the ML86V7666/ ML86V7665 data sheet.

5.6 RS485 transceivers

Supplier : Linear Technology

Model : LTC2850CS8 8-LEAD PLASTIC MSOP

Features

- 3.3V Supply Voltage
- 20Mbps Maximum Data Rate
- No Damage or Latchup Up to ±15kV HBM
- High Input Impedance Supports 256 Nodes (C, I-Grade)
- Operation Up to 125°C (H-Grade)
- Current Limited Drivers and Thermal Shutdown
- Delayed Micropower Shutdown: 5µA Maximum (C, I-Grade)
- Power Up/Down Glitch-Free Driver Outputs
- Low Operating Current: 370µA Typical in Receive Mode
- Compatible with TIA/EIA-485-A Specifications

For more information, please refer to the LTC2850 data sheet.

5.7 Equipment connection cable

NEC recommends using a category 7 Ethernet cable 7(600MHz/10GBASE-T)

6 Revision history

Version	Date	Document Number	Description
1.0	July 2009	U19880EE1V0UM00	First version

The following revision list shows all functional changes compared to the previous version.

Chapter	Page	Description