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April 1st, 2010
Renesas Electronics Corporation

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Technical Note

RELIABILITY QUALITY CONTROL OF SILICON POWER FET DEVICE

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Major Revisions in This Edition

Page	Description
Throughout	Review of descriptions in conjunction with merger of NEC Compound Semiconductor Devices, Ltd. with NEC Electronics Corporation.

CONTENTS

1. CONCEPT OF RELIABILITY QUALITY CONTROL

NEC Electronics Corporation has been certified for ISO 9001 and ISO 14001. The company is intent on continually improving its quality system to provide high-quality/environment-friendly products that will satisfy the customer.

The reliability quality control of our microwave semiconductor devices is based on improving the reliability in individual processes, from development design to mass production design, by reflecting customers' needs identified through market research and customer feedback. We also aim to achieve production that maintains a balance between reliability quality and price by adopting effective management methods suitable for the application of individual products, and will devote our full efforts to manufacturing products that will meet our customers' expectations. Toward this realization, shipment and after-sales service are controlled under a coherent system in each process from material procurement to product delivery as follows:

(1) Selection and procurement of environment-friendly material as well as components/parts
(2) Quality control and inspection of the product in individual processes up to mass-production
(3) Confirmation of the quality of the product by reliability testing

In addition, with the expansion and development of the application fields of microwave semiconductor devices such as mobile phones, the number of applications is drastically increasing and the quality expected of our products is steadily growing. In response to these expectations, NEC Electronics Corporation considers the following items key points:

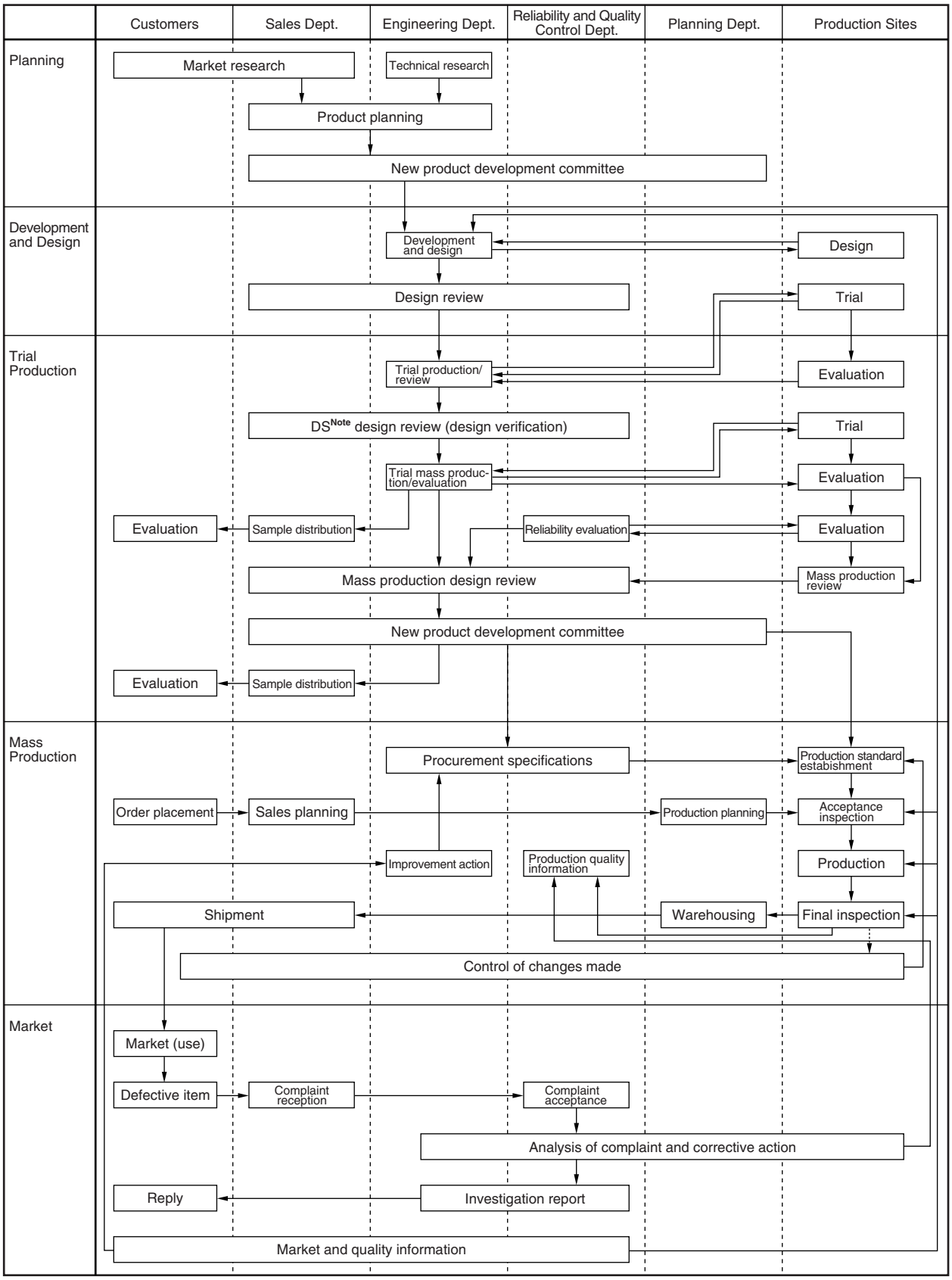
(a) improvement of design quality,
(b) improvement and maintenance of the quality in the production phase, and
(c) removal of potential defects by setting quality gates in each process.

Aspects to be emphasized include
(i) establishment of reliability by standardization of design rules,
(ii) identification of non-reliability causes by design review,
(iii) thorough evaluation of characteristics and reliability testing in development/trial production phase,
(iv) automation of production facilities and product variation control by facility maintenance,
(v) enhancement of staff awareness of the quality by small group activities such as QC circle,
(vi) analysis, feedback and feedforward of quality information including field data, and
(vii) prevention of defective products by PC (Process Check) in each process and feedback of results to the corresponding process.

By implementing these actions, we commit ourselves to providing semiconductor devices that satisfy the high quality/low price needs of the customer. Moreover, we also pledge to continue our efforts to improve product quality.

The flowchart of the quality (Q) and reliability (R) system is shown in Figure 1-1.

Figure 1-1 The flowchart of the quality (Q) and reliability (R) system



Note DS : Design Sample

2. QUALITY CONTROL OF PRODUCTION PROCESS

NEC Electronics Corporation manufactures and releases microwave semiconductor devices focusing on further improvement of the required product reliability by assessing customer requirements as well as the application environment of the product, and incorporating the results into the original design. To realize the reliability quality intended in the design, a production control system is required to obviate any defective elements caused by variations in individual production processes.

Therefore, emphasis is placed on the quality control of parts, components or secondary materials that will determine the reliability quality upon production and on related aspects such as the production environment. Further, by incorporating checking functions in the production processes, half-finished products in each process are checked with optimum frequency against the key control items.

A flowchart example of production process control is shown in Figure 2-1 and 2-2. Components, materials or secondary materials are controlled as described below.

Components, materials and secondary materials such as chemicals or high-purity gas are procured through the specified vendors. Acceptance testing is performed largely by sampling based on JIS Z 9015 or other procurement standards used by NEC Electronics Corporation. The result of the acceptance test is monitored, and if necessary, corrective action is taken or factory inspections are conducted at the specified vendors to stabilize the quality of the purchased products.

Figure 2-1 An example of production process control flowchart of Silicon Power FET (hollow plastic package)

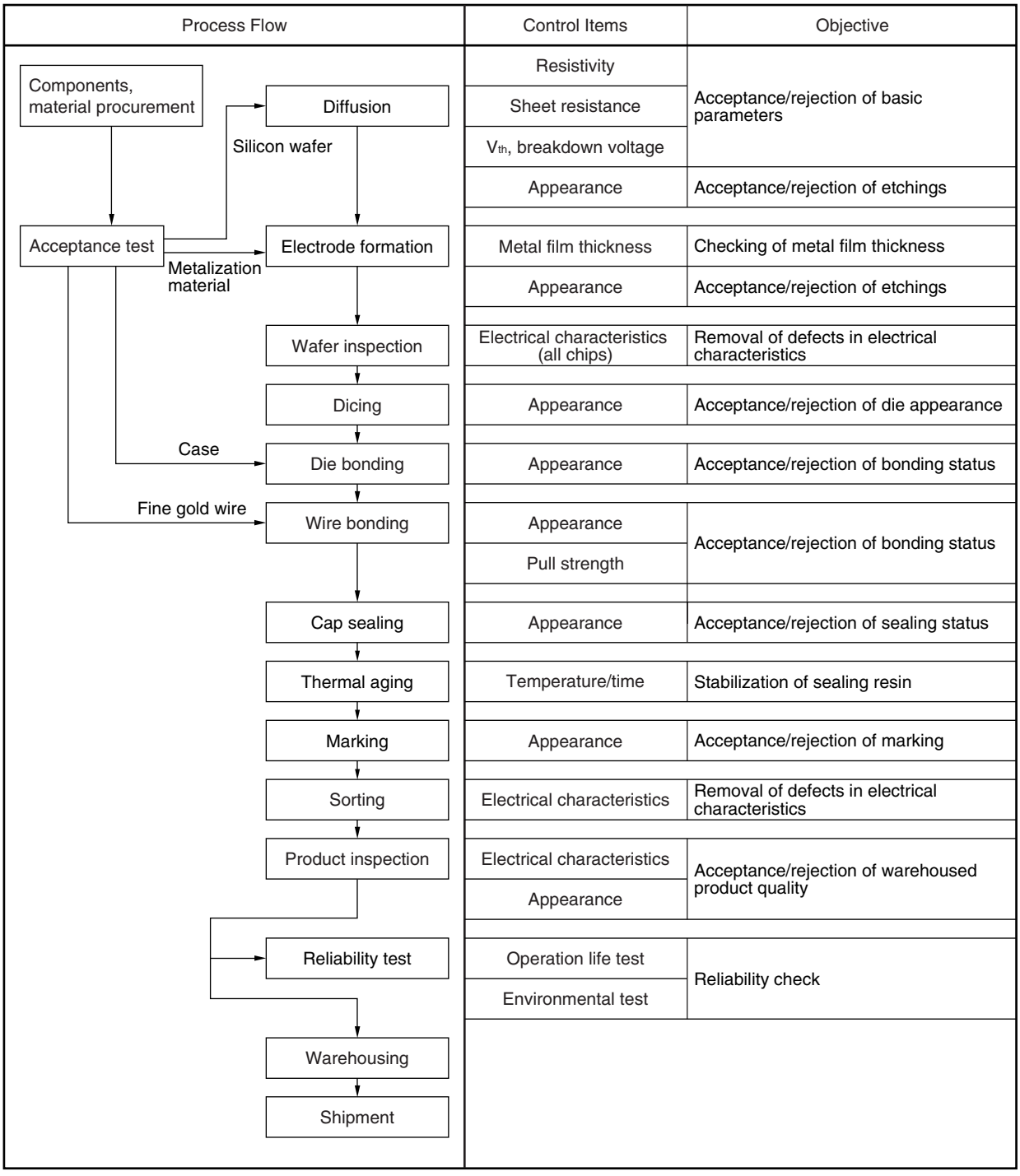
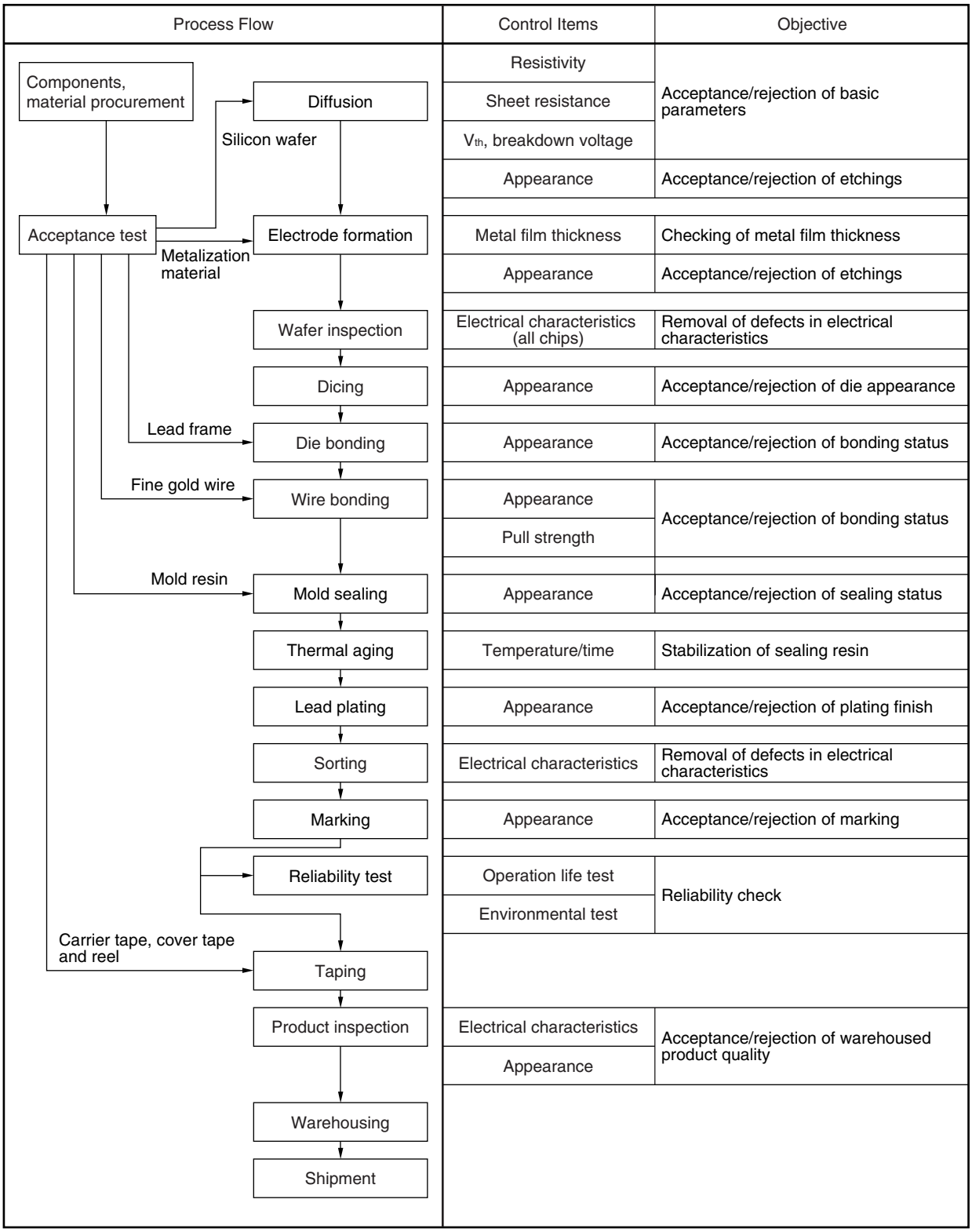


Figure 2-2 An example of production process control flowchart of Silicon Power FET (plastic package)



3. PRODUCTION INSPECTION

Product inspections are conducted by sampling to determine whether or not the package appearance and electrical characteristics of products that have already passed the sorting inspection meet the specified standard.

An example of this inspection is shown below.

(1) Silicon Power FET (hollow plastic package)

Item	Parameter	Sampling Inspection		
		LTPD	Number of Samples	Number Passed Inspection
Open/Short	Open, Short	10%	22	0
DC Items	BV_{GSS}, BV_{DSS}, I_{GSS}, I_{DSS}, g_m, V_{th} ($V_{GS\ (off)}$)	10%	22	0
RF Items	P_{out}, η_d, G_L	10%	22	0
Critical Package Appearance	Resin cracking, Lead deformation, Bent leads, No lead plating, Missing markings	1%	231	0
Moderate Package Appearance	Defective resin molding/Chipping, Defective lead plating, Illegible markings	1%	231	0

(2) Silicon Power FET (plastic package)

Item	Parameter	Sampling Inspection		
		LTPD	Number of Samples	Number Passed Inspection
Open/Short	Open, Short	10%	22	0
DC Items	BV_{GSS}, BV_{DSS}, I_{GSS}, I_{DSS}, g_m, V_{th} ($V_{GS\ (off)}$)	10%	22	0
RF Items	P_{out}, η_d	10%	22	0
Critical Package Appearance	Resin cracking, Lead deformation, Bent leads, No soldering, Missing markings	1%	231	0
Moderate Package Appearance	Defective resin molding/Chipping, Defective soldering, Illegible markings	1%	231	0

4. RELIABILITY TEST

Reliability tests are conducted regularly based upon EIAJ ED-4701, MIL-STD-750 and other standards. Examples of the tests and of the failure criteria are shown in 4. 1 and 4. 2 below.

4. 1 Test Contents

(1) An example of Silicon Power FET (hollow plastic package) is shown below.

Test Item	Test Conditions	Number of Samples	Related Standards
Solderability	215±5°C or 245±5°C, 5 seconds	10	MIL-STD-750 2026
Soldering Heat	260±5°C, 10 seconds	10	MIL-STD-750 2031
Temperature Cycle	T_{stg} min.[Note1] to T_{stg} max.[Note1] 30 minutes each, 100 cycles	10	MIL-STD-750 1051
High-temperature Storage	T_{stg} max.[Note1], 1 000 hours	10	MIL-STD-750 1031
Steady State Operation Life	$T_{ch} = T_{ch}$ max.[Note1], $V_{DS} = V_{DS}$ max.[Note2], $I_{DS} = I_{DS}$ max.[Note2], 1 000 hours	8	MIL-STD-750 1026
High-temperature High-humidity Bias	T_A = 85°C, Rh = 85%, $V_{GS} = \pm V_{GS}$ max.[Note1], 1 000 hours	8	EIAJ ED-4701 102
High-temperature Bias	$T_A = T_{stg}$ max.[Note1], $V_{GS} = \pm V_{GS}$ max.[Note1], 1 000 hours	8	EIAJ ED-4701 102
Terminal Strength (pulling)	Apply the specified weight, Keep for 10 seconds	3	MIL-STD-750 2036
Terminal Strength (bending)	Apply the specified weight, 0° → 90° → 0°, 3 times	3	MIL-STD-750 2036
Electrostatic Discharge Sensitivity	C = 200 pF, R = 0 Ω, Once, Between the weakest terminals	10	EIAJ ED-4701 304

Notes 1. Absolute maximum ratings

2. Recommended operating conditions

Remark Acceptance/rejection is determined by (0, 1) regardless of the number of samples.

(2) An example of Silicon Power FET (plastic package) is shown below.

Test Item	Test Conditions	Number of Samples	Related Standards
Solderability	215±5°C or 245±5°C, 5 seconds	22	MIL-STD-750 2026
Soldering Heat	260±5°C, 10 seconds	22	MIL-STD-750 2031
Temperature Cycle [Note1]	T_{stg} min. [Note2] to T_{stg} max. [Note2] 30 minutes each, 100 cycles	22	MIL-STD-750 1051
High-temperature Storage	T_{stg} max. [Note2], 1 000 hours	22	MIL-STD-750 1031
Steady State Operation Life	$T_{ch} = T_{ch}$ max. [Note2], $V_{DS} = V_{DS}$ max. [Note3], $I_{DS} = I_{DS}$ max. [Note3], 1 000 hours	22	MIL-STD-750 1026
High-temperature High-humidity Bias [Note1]	T_A = 85°C, Rh = 85%, $V_{GS} = \pm V_{GS}$ max. [Note2], 1 000 hours	22	EIAJ ED-4701 102
High-temperature Bias	$T_A = T_{stg}$ max. [Note2], $V_{GS} = \pm V_{GS}$ max. [Note2], 1 000 hours	22	EIAJ ED-4701 102
Autoclave (Pressure Cooker) [Note1]	T_A = 125°C, Rh = 100%, P = 223 kPa, 96 hours	22	–
Terminal Strength (pulling)	Apply the specified weight, Keep for 10 seconds	11	MIL-STD-750 2036
Terminal Strength (bending)	Apply the specified weight, 0° → 90° → 0°, 3 times	11	MIL-STD-750 2036
Electrostatic Discharge Sensitivity	C = 200 pF, R = 0 Ω, Once, Between the weakest terminals	20	EIAJ ED-4701 304

Notes 1. Preconditioning: High-temperature storage (125°C, 24 hours) + High-temperature high-humidity storage (85°C, 85%, 24 hours) + SH (260°C, 10 seconds, 3 times)

2. Absolute maximum ratings

3. Recommended operating conditions

Remark Acceptance/rejection is determined by (0, 1) regardless of the number of samples.

4. 2 Failure Criteria

(1) An example of Silicon Power FET (hollow plastic package) is shown below.

Test Item	Failure Criteria		
	Parameter	Lower	Upper
Soldering Heat, Temperature Cycle, High-temperature Storage, Steady State Operation Life, High-temperature High-humidity Bias, High-temperature Bias, Electrostatic Discharge Sensitivity	Gate to source leak current (I_{GSS})	–	U
	Saturated drain current (Zero gate voltage drain current) (I_{DSS})	–	U
	Transconductance (g_m)	S × 0.8	S × 1.2
	Threshold voltage (V_{th})	S × 0.8	S × 1.2
Terminal Strength	Lead appearance	No evidence of breakage or loosening	
Solderability		Solder covers 95% or more of the surface	

Remark U : Upper value of the product standard
S : Initial value

(2) An example of Silicon Power FET (plastic package) is shown below.

Test Item	Failure Criteria		
	Parameter	Lower	Upper
Soldering Heat, Temperature Cycle, High-temperature Storage, Steady State Operation Life, High-temperature High-humidity Bias, High-temperature Bias, PCT, Electrostatic Discharge Sensitivity	Gate to source leak current (I_{GSS})	–	U
	Saturated drain current (Zero gate voltage drain current) (I_{DSS})	–	U
	Transconductance (g_m)	S × 0.8	S × 1.2
	Threshold voltage (V_{th})	S × 0.8	S × 1.2
Terminal Strength (bending)	Lead appearance	No evidence of breakage or loosening	
Solderability		Solder covers 95% or more of the surface	

Remark U : Upper value of the product standard
S : Initial value

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