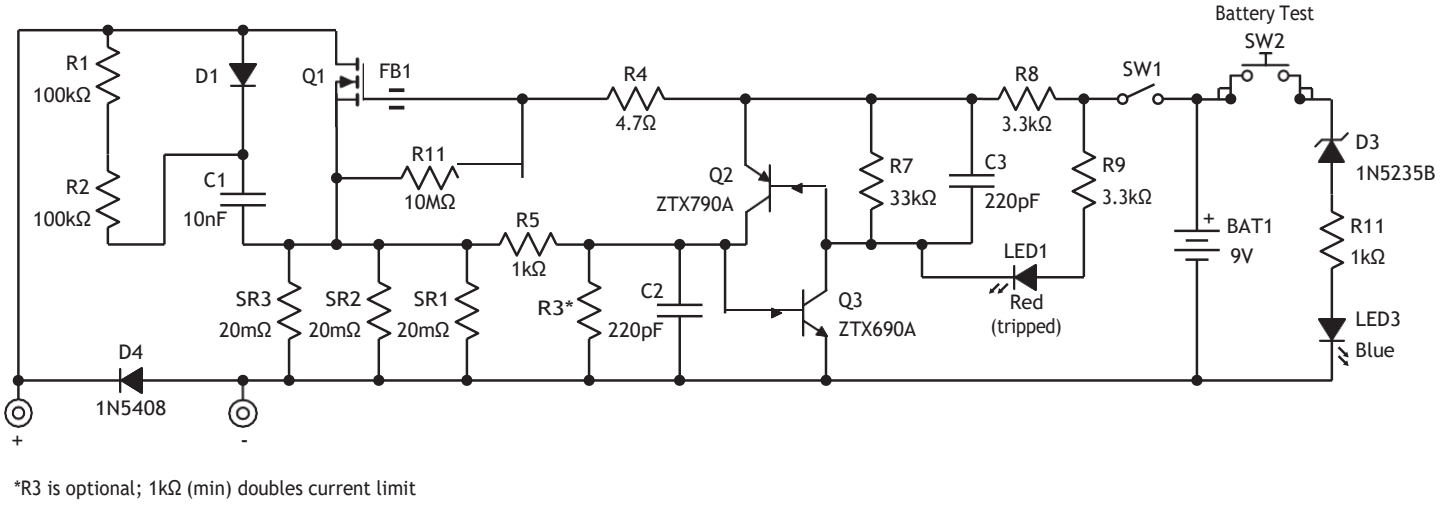
Ultrafast Overcurrent Breaker Circuit for Prototyping



*R3 is optional; 1kΩ (min) doubles current limit

Figure 1. Complete schematic of the ultrafast breaker circuit

Introduction

This Design Guide presents a simple, fast (<1µs) resettable electronic circuit breaker that can help protect GaN transistors, and save repair time by reducing collateral damage from an overcurrent condition due to a malfunction during development of a power electronics system.

PBC layout, schematic, and BOM files can be downloaded at Renesasusa.com/dg005df.

How it works

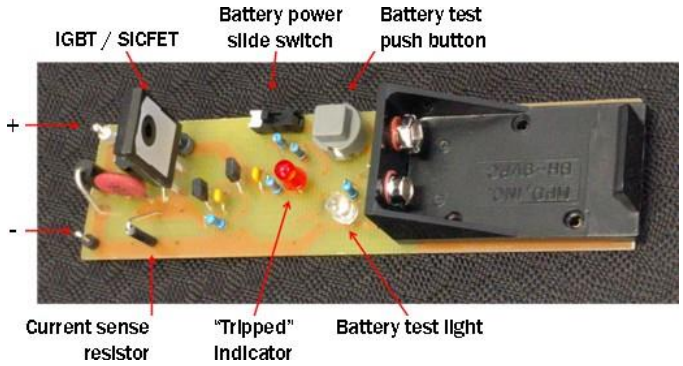


Figure 2. Ultrafast breaker board

During normal operation, the gate of Q1 is driven high through R8 and R4, allowing Q1 to conduct current. During an overcurrent condition, the voltage drop on current sense resistors SR1 - SR3 will trigger the 2-transistor SCR (Q2 and Q3), discharging the gate of Q1. The sense resistors are calculated to provide approximately 0.6V of drop at the desired current threshold. R4 limits the gate discharge current through the SCR to prevent damage. The red LED (LED1) is illuminated when the breaker has tripped.

A 9V battery provides power with isolation from the rest of the Circuit Under Test. A push-to-test button (SW2) connects a blue LED (LED3) through Zener diode D3 to provide a "battery good" indicator. Slide switch (SW1) is the main battery power switch to prevent battery drain when the board is not being used. The switch is also used to reset the system by turning off, then on. After a fault event the Circuit Under Test should be checked for issues prior to turning the breaker back on. The breaker should not be used to power down the Circuit Under Test via SW1. This produces a very slow turn-off that may overheat Q1.

In the tripped state the board will block voltage in one direction. Voltage can be blocked in both directions by adding a diode bridge to the circuit (Figure 3). Note that without the bridge the main FET Q1 can conduct current in either direction but the board will only detect overcurrent in one direction.

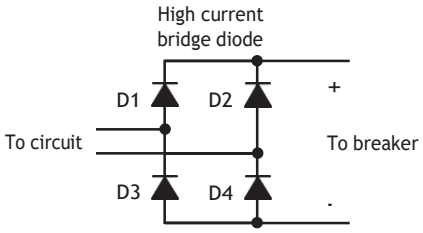


Figure 3. Bridge rectifier to use breaker on AC currents

Resistor R3 is optional, and can be installed to quickly increase the current limit without changing the sense resistors. Note this method will cause additional dissipation in SR1~SR3. FET Q1 will require heatsinking for a Circuit Under Test that requires more than 3A RMS. Likewise the power rating of SR1~SR3 should be selected carefully.

D1, R1, R2, and C1 form an RCD turn-off snubber to prevent safe operating area (SOA) failure of the FET and prevent ringing by reducing dv/dt. D4 prevents reverse current from turning off the Q2/Q3 SCR pair, which would reactivate the breaker. FB1 is a slip-on ferrite bead to prevent FET high frequency oscillation.

Where to insert the breaker

In many applications, the breaker is placed between the bulk capacitor (C1) and the bypass capacitor (C2) which are close to the GaN devices (Figure 4). The breaker will prevent the bulk capacitors from dumping all their energy into the GaN FETs, causing catastrophic failure in the event of a worst-case malfunction wherein both high and low side devices turn on simultaneously (i.e. Q1 and Q2 both on, or Q3 and Q4 both on). The small bypass capacitor(s) (C2) should remain close to the half-bridges to reduce loop inductance and limit voltage overshoots on the GaN FETs. If C2 is small enough the stored energy will be incapable of damaging the GaN FETs. 100nF max is acceptable for TO-220 devices, and 470nF max for TO-247 devices. The MOV between C1 and C2 will absorb energy from inductors L1 and L2 after the breaker opens which can charge C2 and cause an overvoltage. A short twisted-wire pair should be used to connect the breaker board to the application. Care should be taken with polarity in DC applications. The breaker should never be inserted in series with a large inductive element because Q1 will be subjected to overvoltage when the breaker opens.

In some applications two breakers are required. The full bridge in Figure 4 is connected to the grid or an AC motor, which can source a large overcurrent into the GaN FETs. A 2nd breaker, with a bridge rectifier, is added between the inverter and the output. The MOV next to C3 absorbs the energy in L1 and L2 when the breaker opens, and the right-most MOV absorbs energy in the case of a motor load.

For additional examples, see the Multi-pulse Testing for GaN Layout Verification Design Guide.

For a full-bridge inverter, the controller or DSP must shut all gate drives during a fault; otherwise, power may continue to flow into the leftmost MOV, causing it to fail.

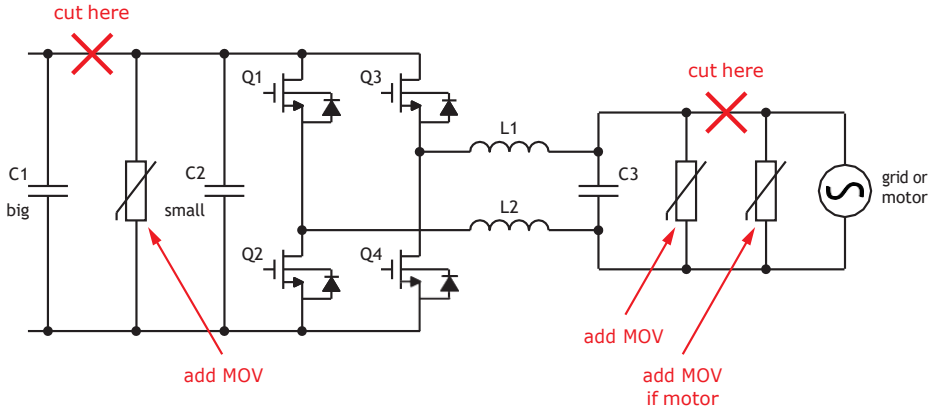


Figure 4. Full-bridge inverter example – place breaker at "cut here"

References and further reading

Design Files (Renesasusa.com/dg005df)

Design Guide DG004: Multi-pulse Testing for GaN Layout Verification (Renesasusa.com/dg004)