Tsi381™
Board Design Guidelines

60E1000_AN001_06

September 2009

Contents

About this Document

This section discusses the following topics:

Scope

The *Tsi381 Board Design Guidelines* provides hardware reference information for the Tsi381, such as layout guidelines and schematic review information. It is intended for hardware designers who are designing system interconnect applications with the Tsi381.

Document Conventions

This document uses the following conventions.

Non-differential Signal Notation

Non-differential signals are either active-low or active-high. An active-low signal has an active state of logic 0 (or the lower voltage level), and is denoted by a lowercase "n". An active-high signal has an active state of logic 1 (or the higher voltage level), and is not denoted by a special character. The following table illustrates the non-differential signal naming convention.

State	Single-line signal	Multi-line signal
Active low	NAMEn	NAMEn[3]
Active high	NAME	NAME[3]

Differential Signal Notation

Differential signals consist of pairs of complement positive and negative signals that are measured at the same time to determine a signal's active or inactive state (they are denoted by "_p" and "_n", respectively). The following table illustrates the differential signal naming convention.

State	Single-line signal	Multi-line signal
Inactive	NAME_p = 0 NAME_n = 1	NAME_p[3] = 0 NAME_n[3] =1
Active	NAME_p = 1 NAME_n = 0	NAME_p[3] is 1 NAME_n[3] is 0

Numeric Notation

- Hexadecimal numbers are denoted by the prefix *0x* (for example, 0x04).

- Binary numbers are denoted by the prefix *0b* (for example, 0b010).

- Registers that have multiple iterations are denoted by {x..y} in their names; where *x* is first register and address, and *y* is the last register and address. For example, REG{0..1} indicates there are two versions of the register at different addresses: REG0 and REG1.

Symbols

This symbol indicates a basic design concept or information considered helpful.

This symbol indicates important configuration information or suggestions.

This symbol indicates procedures or operating levels that may result in misuse or damage to the device.

Revision History

60E1000_AN001_06, Formal, September 2009

This document was rebranded as IDT. It does not include any technical changes.

60E1000_AN001_05, Formal, March 2009

- Removed a previous recommendation to use capacitors with the "PCIe_REFCLK" circuit

- Revised the description of "Polarity Reversal"

60E1000_AN001_04, Formal, July 2008

- Added a brief description about "Polarity Reversal"

- Moved the schematic checklist content to the "Signal Descriptions" chapter of the *Tsi381 User Manual*

60E1000_AN001_03, Formal, December 2007

Redefined the description of the TEST_SPARE[2:0] signals (see *Tsi381 User Manual*)

60E1000_AN001_02, Formal, September 2007

- Revised the PCI bus routing rules:
    - See "Clock length matching" in Table 8
    - See "Skew with clock" in Table 9
- Revised the descriptions of various signals

60E1000_AN001_01, Formal, August 2007

This is the irst version of the document.

1. Designing a PCB for PCIe Signals

Topics discussed include the following:

- "PCIe Signals"
- "Transmission Line Terms"
- "Trace Geometry"
- "Trace Length Matching"
- "Reference Planes"
- "Bends in PCIe Differential Pairs"
- "Device Breakout Area"
- "Vias in Differential Traces"
- "Routing Guidelines Summary"
- "PCIe Tx Capacitors"
- "PCIe_REFCLK"
- "Polarity Reversal"

Dimensions in this chapter are given in British imperial units. Use this conversion ratio for Metric units:

- 1 inch = 25.4 mm
- 1 mil = 0.0254 mm

1.1 PCIe Signals

The following table lists the Tsi381's PCIe signals that are subject to the layout guidelines.

Table 1: Tsi381 PCIe Signals

Signal Name	Pin Number
PCIE_TXD_p	B5
PCIE_TXD_n	A4
PCIE_RXD_p	A8
PCIE_RXD_n	B7
PCIE_REFCLK_P	A6
PCIE_REFCLK_n	B6

1.2 Transmission Line Terms

- Microstrips – Traces that are adjacent to a continuous reference plane. In a PCB stackup, the microstrips are on the primary and secondary layers.

- Striplines – Traces routed in inner layers and have two reference planes. In a PCB stack-up, striplines are on internal layers

1.3 Trace Geometry

The PCIe protocol uses differential pair routing, which requires greater care to meet the impedance targets on these signals versus other single-ended interfaces. Variations in the impedance of these signals will impact the overall jitter and loss within the system.

The main areas of concern for board trace routing of PCIe data and clock signals include:

- Spacing within the differential pair

- Coupling to an adjacent reference plane

- Thickness of the traces within the pair

Close coupling or relatively close physical spacing within the differential pairs, along with increased spacing to unrelated differential pairs and other signals, help to minimize crosstalk and EMI effects.

The width and spacing guidelines of the PCIe differential signals determines the impedance of the traces and helps to insure that interconnect loss and jitter budgets are met. Signal integrity within the system is also impacted by whether or not appropriate spacing exists between differential pairs and adjacent traces.

Edge-coupled microstrip traces of each differential pair within the PCIe Interface should have a differential impedance of 100 Ohms. When using common PCB material, the target impedance can be achieved with trace widths of 5-mils with a 7-mil space within the pair. This 5/7/5 routing method provides the best compromise between impedance targets, loss impacts, crosstalk immunity, and routing flexibility. If stripline traces are used, they should maintain a 5/5/5 routing geometry with 5-mil trace widths combined with a 5-mil spacing within the pair.

A 20-mil edge-to-edge spacing should be used between traces of adjacent differential pairs in order to minimize negative crosstalk effects. A 20-mil spacing should also be maintained between differential pairs and non-PCIe signals. If unrelated signals have significantly higher voltage levels or edge rates when compared to PCIe, then a minimum 30-mil spacing should be used to avoid coupling issues.

Figure 1 displays an example of the width and spacing recommendations for PCIe differential pairs.

If board constraints require routing sections of a differential pair uncoupled where the intrapair spacing exceeds the 7-mil requirement, then the width of the uncoupled section of trace can be increased to 7-mils, as displayed in the figure. This applies to uncoupled sections that exceed 100 mils in distance. Using a 7-mil trace versus 5-mils within the uncoupled sections helps to maintain the correct differential impedance across the uncoupled region.

Figure 1: PCIe Board Trace Width and Spacings Example

PCIe Microstrip Board Traces

PCIe Stripline Board Traces
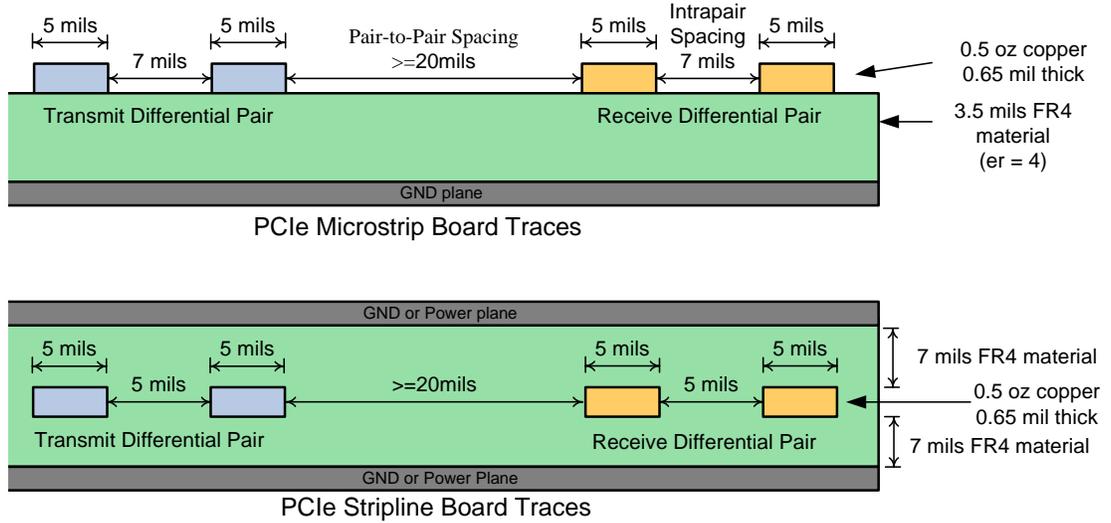
Note: PCB parameter examples are approximate. Use PCB parameters as provided by your PCB manufacturer.

1.4   Trace Length Matching

PCIe signals have constraints with respect to trace lengths and matching in order to meet jitter and loss budgets within a system. Each inch of board trace within a differential pair can add 1ps of jitter and up to 0.35dB of loss. Typically, the PCIe specification can be met with a chip-to-chip routing length up to 15 inches. When routing differential pairs connecting the finger connector pad to a Tsi381 pin on an add-in card, traces can be routed up to 3.5 inches.

Pair-to-pair length matching within the PCIe Interface is normally not required due to the large skew allowed at the receiver; however, it should be minimized in order to reduce the overall latency of the system. Intrapair skew is much more important and requires that the length of the traces within a differential pair be matched to within 5-mils of one another. Length matching within a differential pair should be performed on a segment-by-segment basis rather than only as an overall measurement.

1.5   Reference Planes

High quality reference planes within the PCIe Interface improve signal integrity, reduce EMI effects, and minimize AC common-mode noise within the differential pairs. It is recommended that the differential signal pairs reference the main ground plane within the PCB stackup, and reference only a single plane along the entire routing path. Differential traces should not be routed across or near any discontinuities in the reference plane. A 20-mil spacing should be maintained when routing near and parallel to the edge of a reference plane.

1.6   Bends in PCIe Differential Pairs

Bends or turns within the PCIe differential pairs should be kept to a minimum. The angles between
traces should be greater than or equal to 135 degrees, and there should never be any 90 degree turns or
bends along a trace. The inner spacing within a bend of a differential pair should equal or exceed the
minimum pair-to-pair spacing of 20-mils in order to minimize the introduction of common-mode noise
within the system (see Figure 1). Segments within a bend should have a length equal to or greater than
1.5x the width of the trace, and if possible the number of left- and right-hand bends should be matched
as closely as possible to minimize length skew differences within a differential pair.

1.7   Device Breakout Area

Within the breakout areas of the Tsi381, the PCIe signal pairs should maximize the differential routing
while minimizing any discontinuities or trace length skew (see Figure 2). Length matching of the
differential traces should occur as close as possible to the pad or pin while avoiding the addition of
"tight" bends within the traces. The breakout areas should not exceed 250-mils in length for the
PCIe Interface. Within the breakout areas, the trace routing guidelines of the differential pairs can be
slightly relaxed — if absolutely necessary — to facilitate successful breakout of the signals. A width
and spacing geometry of 5/5/5 can be used with a minimum spacing to other signals of 7-mils.

Figure 2: Tsi381 PCIe Differential Trace Breakout
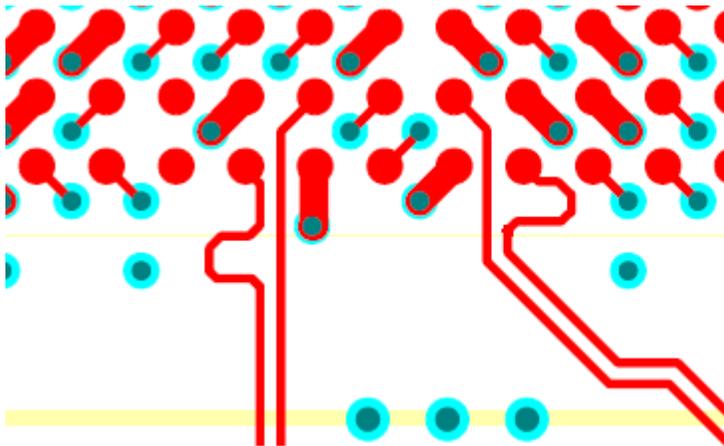
1.8   Vias in Differential Traces

Use of vias within the differential traces of the PCIe signals can have an adverse effect on system performance. If vias must be used, they should have a pad size of less than 25-mils with a finished hole size of less than 14-mils. Vias should always be placed in pairs at the same relative location and should be symmetrical between the differential traces. A maximum of four via pairs can be used within each transmit differential pair of the PCIe link. Each receive differential pair can have a maximum of two vias along its path. A maximum of six via pairs are allowed along the entire PCIe interconnect path.

When traces change layers in a PCB, the reference plane for the differential traces also changes. It is recommended to introduce a stitching via close to the differential trace vias (see Figure 3). The stitching via connects all the ground planes together, and allows return current to flow easily from one ground plane to another.

Figure 3: Differential Pair Vias and Stitching Via
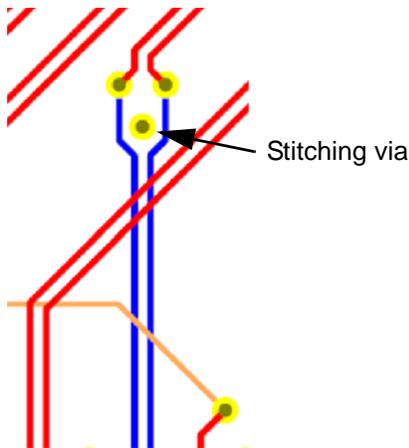
1.9   Routing Guidelines Summary

The routing guidelines should be used for board routing of the transmit and receive data. The guidelines are summarized in Table 2.

Table 2: PCIe Interface Routing Guidelines

| Parameter	Main Route System Board	Special Breakout Area
Differential Impedance Target	100 ohms $\pm$15 %	
Single-ended Impedance Target	60 ohms $\pm$15 %	
Trace Width	5 mils	7 mils if uncoupled length ≥ 100 mils
Differential Pair (within pair) Spacing	7 mils	5-mil spacing is acceptable
Pair-to-Pair Spacing	≥ 20 mils	7-mil spacing is acceptable
Trace Length Restrictions	≤ 15 " chip-to-chip ≤ 3.5 " chip-to-add-in card edge Connectors	Breakout is limited to ≤ 250 mils (included in overall trace length recommendations for main routes)
Length Matching within Pair	5 mils	
Length Matching Pair-to-Pair	Keep moderate for latency. 1.25ns maximum lane-to-lane skew.	
Reference Plane	GND plane recommended. Use stitching vias when changing layers. If a power plane is used as a reference plane, place decoupling capacitors close to the vias where the traces change layers.	GND islands on PWR layer are acceptable as long as the connection to the main ground planes is local.
Splits/Voids	No routing over splits or voids.	No more than half the trace width should be over via anti-pad.
Via Usage (maximum) (6 total, entire path)	Four vias per Tx trace. Two vias per Rx trace.	Acceptable to include one via in breakout area.
Bends	Match left and right turn bends where possible. No 90-degree or "tight" bends.	Avoid "tight" bends when routing in breakout area.

1.10 PCIe Tx Capacitors

The PCIe specification requires that each lane of the link be AC coupled between its corresponding transmitter and receiver. The AC coupling capacitors for the Tsi381 are discrete components located along each transmitter link on the PCB. These AC coupling capacitors allow the transmitter and receiver on a link to be biased at separate voltages. Table 3 summarizes the guidelines for implementing the PCIe AC coupling capacitors on a system board. Recommended capacitor layout and placement are provided in Figures 4 and 5.

**Table 3: PCIe Interface AC Coupling Capacitor Guidelines**

Parameter	Implementation Guideline
AC Coupling	AC coupling capacitors are required on the Tx pairs originating from the Tsi381.
Capacitor Value	$75nF \leq C_{AC\text{-}COUPLING} \leq 200nF$
Capacitor Tolerance	Specified minimum/maximum range must be met when capacitor tolerance is considered along with effects due to temperature and voltage.
Capacitor Type	Size 603 ceramic capacitors are acceptable; however, size 402 capacitors are strongly encouraged. The smaller the package size, the less ESL is introduced into the topology. The same package and capacitor size should be used for each signal in a differential pair. Do not use capacitor packs for PCIe AC coupling.
Capacitor Pad Size	To minimize parasitic impacts, pad sizes for each capacitor should be the minimum allowed per PCB manufacturer.
Capacitor Placement	AC coupling capacitors should be located at the same place within the differential pair. They should not be staggered in distance from one trace of the differential pair to the other. Capacitors should be placed as close to each other as possible to avoid creating large uncoupled sections within the differential pair traces. Relative location from one differential pair to another is not important.
Capacitor Location – Chip-to-Connector Routing	Capacitors should be placed such that they are not located in the center point of a trace route (for example, capacitors should be placed next to the connector or 1/3 the distance between the connector and the Tsi381).
Capacitor Location – Chip-to-Chip Routing	Capacitors should be located off-center within the interconnect (for example, placing the capacitors next to the Rx pins of one device is generally better than locating the capacitors in the midpoint of the interconnect).

Figure 4: PCIe AC Coupling Capacitor Symmetric Layout

Preferred Symmetric Placement

Avoid Asymmetric Placement
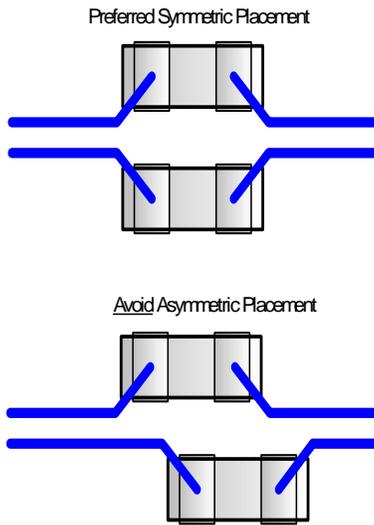
**Figure 5: PCIe AC Coupling Capacitor Recommended Board Placement**
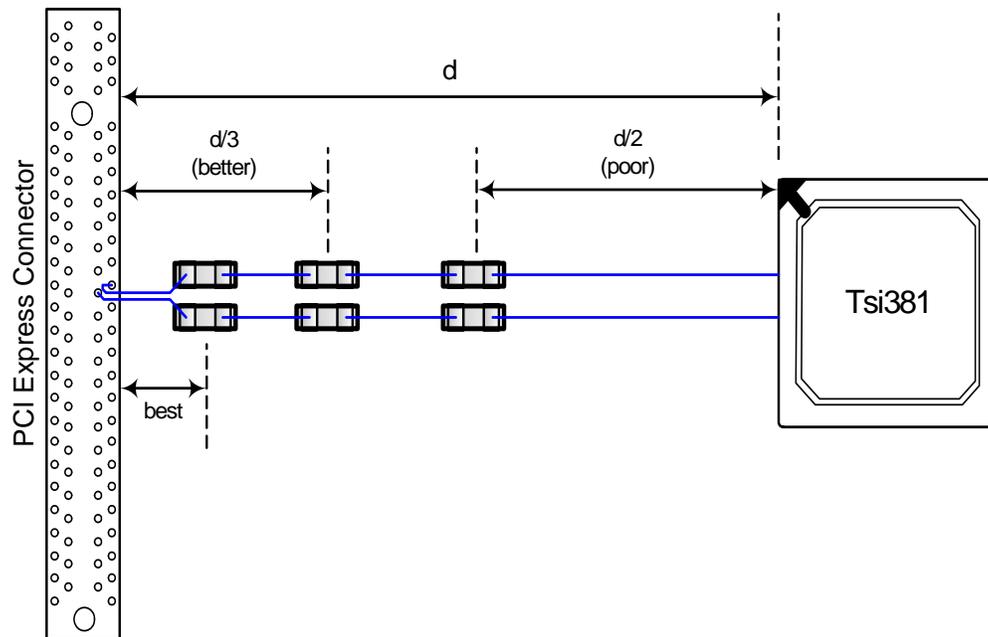
1.11   PCIe_REFCLK

The Tsi381 must receive a 100-MHz differential reference clock on its PCIE_REFCLK_p/n input pins. This clock can be generated from an on-board oscillator if a PCIe system clock is not available. The clock generator should provide an HCSL output-level clock that meets the PCIE_REFCLK duty cycle and jitter requirement, as specified in the *Tsi381 User Manual*. Figure 6 shows a simplified schematic of an HCSL PCIE_REFCLK circuit. The HCSL source termination is specified by the HCSL clock device vendor.

Figure 6: Simplified PCIE_REFCLK Circuit
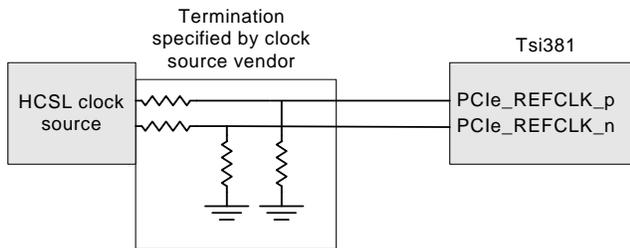
Table 4: PCIE_REFCLK Layout Guidelines

Parameter	Implementation Guidelines
PCIE_REFCLK Differential Trace Impedance	100 Ohms
PCIE_REFCLK Length Restriction for Add-in Card	From finger connector to Tsi381 (or any other device): 4 inches
Length Matching within Pair	≤ 10 mils

1.12   Polarity Reversal

Lane polarity reversal support is required as per the *PCI Express Specification*. This feature can be used to ease routing of differential pairs of the express link to and from the bridge. As such, the following are recommended:

- To connect the _p to the _n of a differential pair instead of crossing the _p and _n traces through an extra PCB layer

- To connect the _p to the _n of a differential pair instead of un-crossing traces around vias or through-holes in a break-out area

2. Power Supply Filtering and Decoupling

Topics discussed include the following:

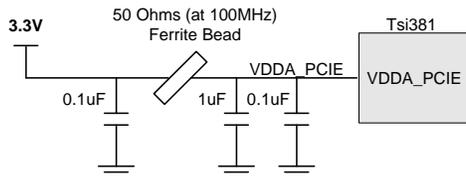- "Analog Power Supply Filtering"

- "Decoupling Capacitors"

2.1 Analog Power Supply Filtering

2.1.1 VDDA_PCIE

The VDDA_PCIE power pin is noise sensitive. Noise on this pin may translate into unwanted jitter on the serial bit streams. The VDDA_PCIE pin should be connected to a filtered 3.3V supply (for an example filter circuit, see Figure 7).

Based on the circuit in the figure, the VDDA_PCIE net can be implemented as a local plane located under the BGA. Ideally, the 0.1uF capacitor is located under the BGA within the breakout vias. If this is not possible, the capacitor should be very close to the edge of the package. The net from the ferrite bead to the VDDA_PCIE pins can be implemented as a trace from the ferrite bead to the VDDA_PCIE pin breakout via, as long as the decoupling capacitor is located under the BGA and connected to the breakout via with short traces (see Figure 8).

Figure 7: Supply Filter Circuit for VDDA_PCIE

Figure 8: VDDA_PCIE Filter Layout Example

Red: Top layer
Blue: Bottom layer
Turquoise: Filtered 3.3V plane (VDDA_PCIe) on a power layer.
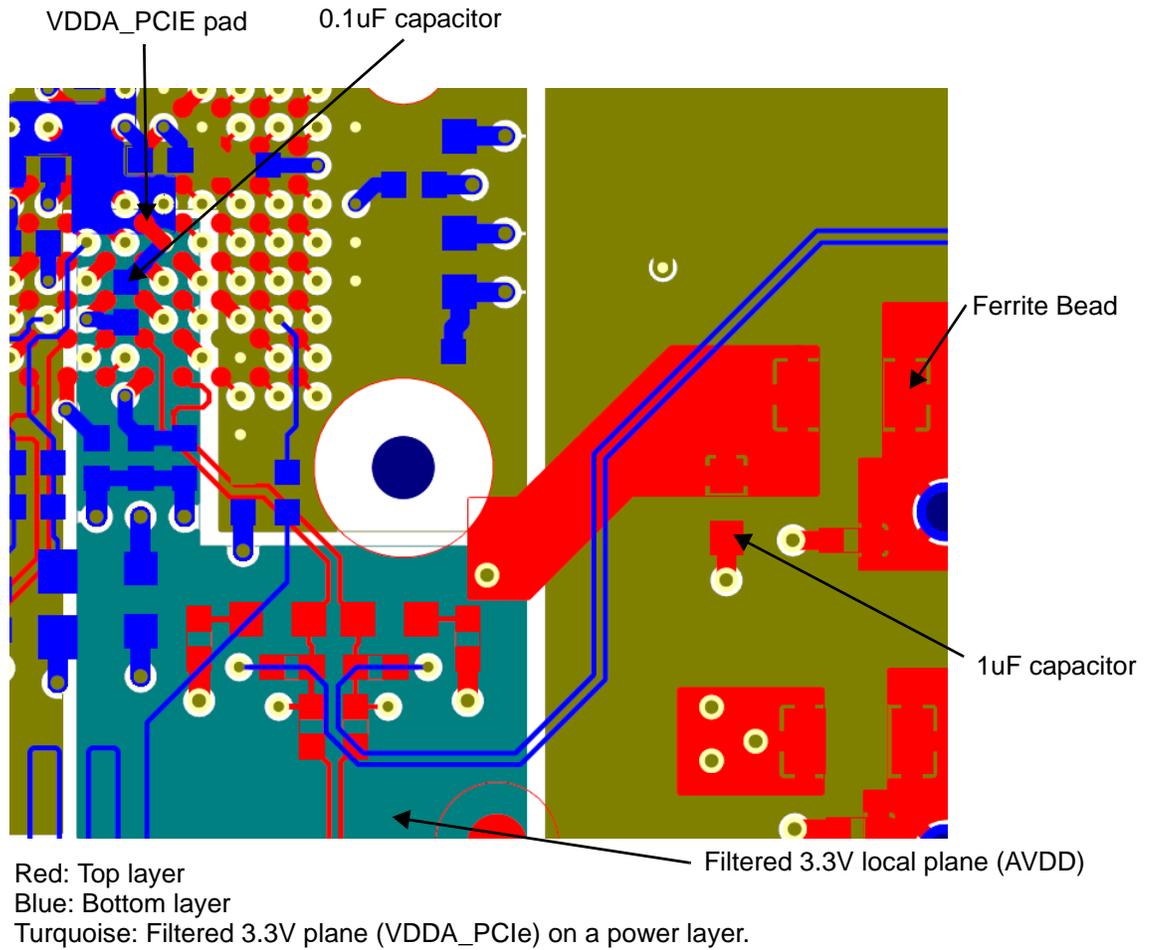
2.1.2   VDD_PCIE

VDD_PCIE pins supply 1.2V to the SerDes circuit internal to Tsi381. The noise restriction on VDD_PCIE is 50mV peak-to-peak. A filter circuit, as displayed in Figure 9, can be used to reduce the noise from the main 1.2V supply. Ideally, the 0.1uF capacitors are located under the BGA within the breakout vias. If this is not possible, the capacitors should be very close to the edge of the package. Preferably, the VDD_PCIE net is implemented as a local power plane under the BGA. Figure 10 shows the VDD_PCIE net implemented with a local power plane.

Figure 9: Supply Filter Circuit for VDD_PCIE

© 2019 Renesas Electronics Corporation
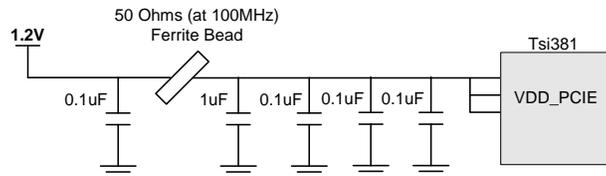
Figure 10: VDD_PCIE Filter Layout Example

VDD_PCIE pads

0.1uF caps   1uF cap   VDD_PCIE plane   Ferrite bead

Red: Top layer
Blue: Bottom layer
Turquoise: Filtered 1.2V plane (VDD_PCIe) on a power layer.
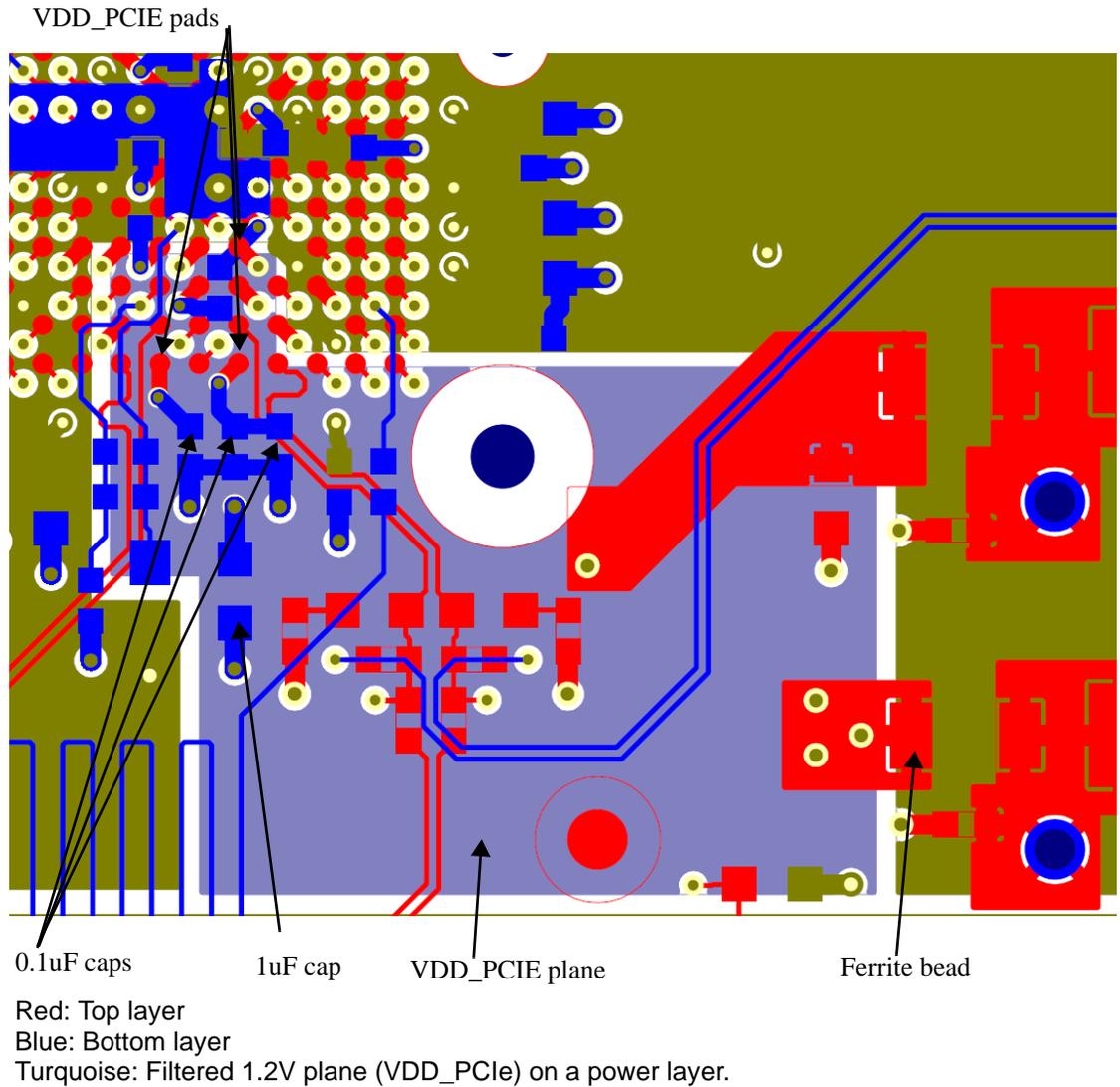
2.1.3 VDDA_PLL

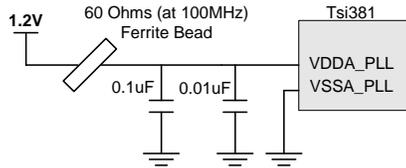The VDDA_PLL supply pin provides power to the internal clock PLL circuit inside the Tsi381. Use a filter circuit similar to the one in Figure 11. Place the 0.1uF and 0.01uF capacitors in the via breakout under the BGA.

**Figure 11: Supply Filter Circuit for VDDA_PLL**

2.2 Decoupling Capacitors

The Tsi381 decoupling recommendation is provided in Table 5. Other components, including PCI connectors, must also be adequately decoupled.

Table 5: Decoupling Capacitor Recommendations

Rail	Capacitor value	Quantity	Placement	Description
VDD	0.1uF	6	Ideally several are placed within the BGA breakout. Others are placed close to the BGA.	Ceramic (X5R or X7R) Surface mount Case size 0402 or 0603
VDD	1uF	2	Close to Tsi381	
VDD_PCI	0.1uF	7	Close to Tsi381	
VDD_PCI	1uF	7	Close to Tsi381	
VIO_PCI	0.1uF	3	Close to Tsi381	

The layout example in Figure 12 shows one method for inserting decoupling capacitors within the BGA breakout. Not all decoupling capacitor from Table 5 are placed in the breakout. The remaining capacitors are located near the chip.

Figure 12: Top View of Bottom Layer, Decoupling Capacitors in Via Field
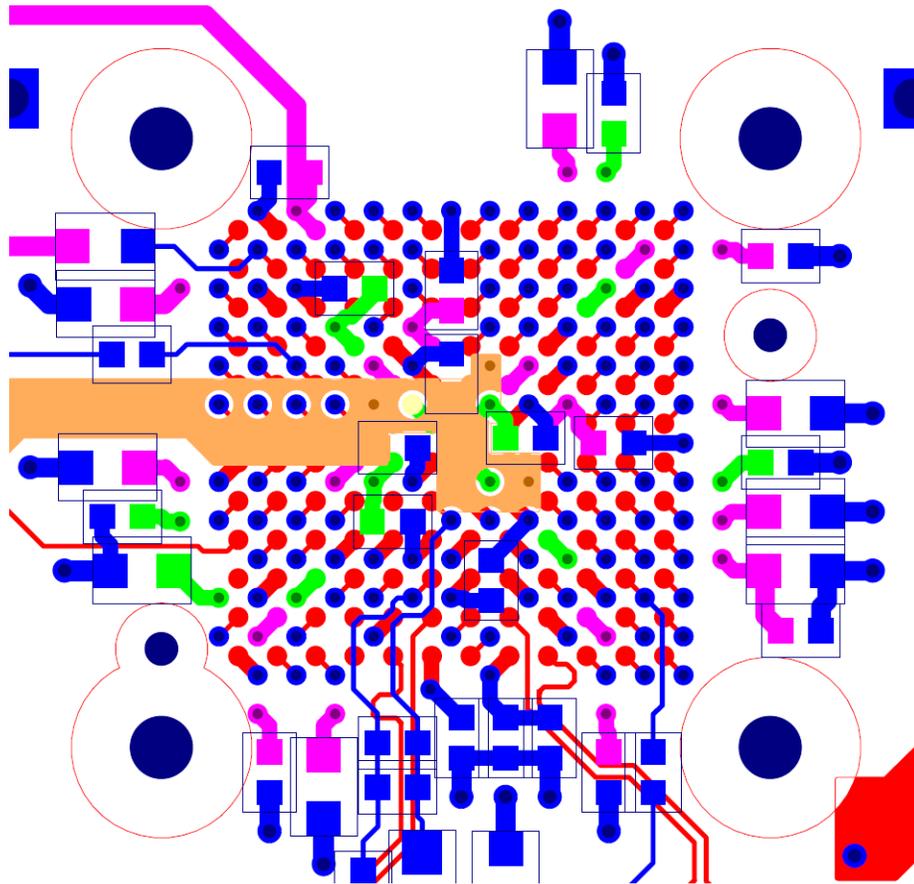
Purple: VDD_PCI rail (3.3V)
Green: VDD rail (1.2)
Blue: Ground and other
Tan: VIO_PCI

3. PCI Bus Design Notes

Topics discussed include the following:

- "PCI Clocking Modes"
- "Bus Routing Rules"

3.1 PCI Clocking Modes

The Tsi381 supports two clocking modes: Master and Slave. These clocking modes are discussed in the following sections.

3.1.1 PCI Slave Mode Clocking

Slave mode clocking requires an external PCI clock source (see Figure 13). The clock source must connect to the Tsi381 PCI_CLK, as well as to all other PCI devices on the same bus. Clock signal trace lengths should all be matched.

Figure 13: Slave Mode Clocking
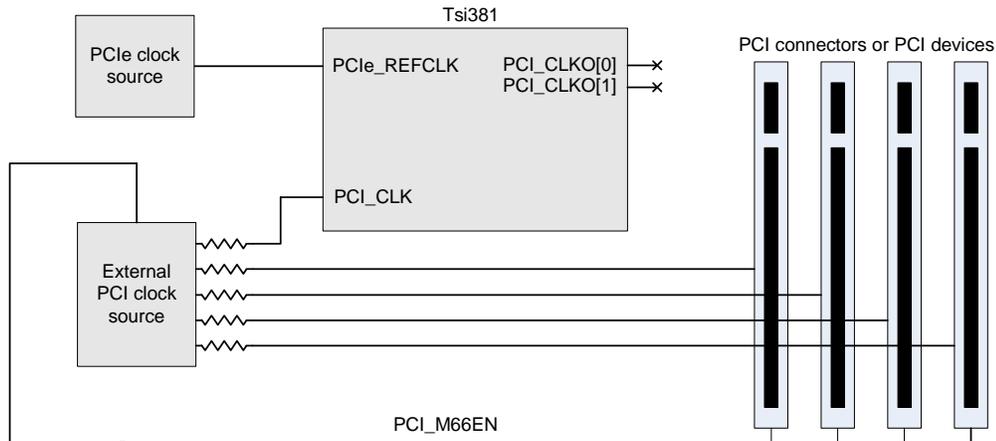
Table 6: Slave Mode Setup

Signal	Setting
PWRUP_PLL_BYPASS	Don't care
PCI_M66EN	Don't care

3.1.2   PCI Master Mode Clocking

Master mode clocking uses the PCIe input clock to generate the PCI clock outputs (see Figure 14).
PCI_CLKO[1] should be connected to PCI_CLK for PCB trace and internal delay compensation. In
Master mode, it is important to set PCI_M66EN at the appropriate level because this signal is used to
set the output clock frequency.

Figure 14: Master Mode Clocking – PCI Clock for All Frequencies
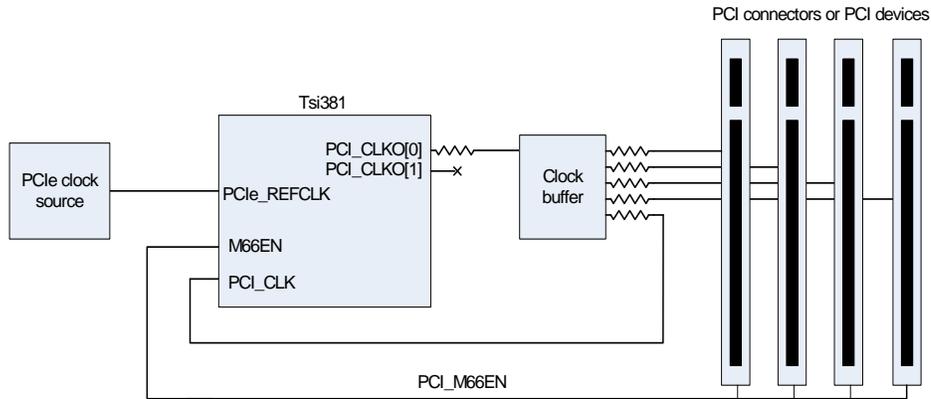
Table 7: Master Mode Setup

Signal	Setting
PWRUP_PLL_BYPASS	0

3.2　　　Bus Routing Rules

The PCB trace parameters outlined in Tables 8 and 9 are derived from the *PCI Specification's* System Timing Budget and the Tsi381's setup and hold timing parameters.

Table 8: PCI Clock Trace Routing Parameters

Parameter	Implementation Guideline
Clock length matching	Clock traces from the clock source to each PCI device should be length matched, including the trace to Tsi381's PCI_CLK. When routing the clock signal to a PCI connector, the path through the connector and through the plug-in card finger-connector to the PCI device should be taken into account when calculating the Tsi381's PCI_CLK trace length. The connector + plug-in card clock path length is 2.5 inches + connector delay. [a]
Trace impedance	60 Ohms +/- 15%
Minimum spacing	Three times the trace width from any other traces.
Resistor	Place 33-Ohm resistors close to Tsi381's clock outputs.

a. Delay through the connector varies with the connector type. Consider adding 0.3" to 0.7" depending on the connector.

Table 9: PCI Bus Routing Parameters

Parameter	Implementation Guideline
Maximum bus length	For 66-MHz operation: 27 inches from the Tsi381 to the last load on the bus, including connectors and plug-in card trace lengths.
Skew with clock	The clock traces should be matched in length. When all PCI devices see the clock rising edges at the same time, PCI bus timing budget specifies the propagation delay for the PCI bus signals between all the devices to be: 6ns for 66 MHz and 12ns for 33 MHz. However, the propagation delay must also includes delays due to slow edge rates and other waveform distortion such as overshoots and undershoots. This propagation delay varies significantly depending on the bus topology and signaling level. As a general guideline the PCI bus skew with clock should be kept within: • 15" for 66-MHz operation • 30" for 33-MHz operation
Trace impedance	60 Ohms +/- 15%

PCI Pull ups

As per the PCI specification, pull-up resistors are required on the signals listed in Table 10. PCI bus signals should be pulled up to the VIO rail.

Table 10: PCI Signal Requiring pull up resistor

Signal Name	Resistor value
PCI_FRAMEn	8.2K
PCI_TRDYn	8.2K
PCI_IRDYn	8.2K
PCI_DEVSELn	8.2K
PCI_STOPn	8.2K
PCI_SERRn	8.2K
PCI_PERRn	8.2K
PCI_LOCKn	8.2K
PCI_INTAn	8.2K
PCI_INTBn	8.2K
PCI_INTCn	8.2K
PCI_INTDn	8.2K
PCI_REQn[3:1] PCI_REQ[0]	8.2K 8.2K only when internal arbiter is used.
PCI_GNTn[0]	8.2K only when an external arbiter is used.
M66EN (when Tsi381 is used on a system board)	10K

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.