RZ/T2H and RZ/N2H Group Hardware Design Guide

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Introduction

This application note is a summary of the items serving as design points as reference materials for use when designing hardware which incorporates RZ/T2H and RZ/N2H group LSIs.

Target Device

- RZ/T2H Group
- RZ/N2H Group

Trademark

Table of Contents

Introduction 1

Target Device 1

Trademark 1

Table of Contents 2

1. Power Supply 5
   - 1.1 Power Supply 5
   - 1.2 Power-On/Off Sequence 6
     - 1.2.1 Example of a Power Supply Circuit Using GreenPAK 8
     - 1.2.2 Example of a Power Supply Circuit Using PMIC 10
     - 1.2.3 Reset Circuit 12

2. Operating Mode 14
   - 2.1 Overview 14
   - 2.2 Types and Selection of Operating Mode 14
     - 2.2.1 Operating Modes (MDn) 14
     - 2.2.2 Operating Voltage of Separated I/O Domain (MDV) 15
     - 2.2.3 Selection of JTAG Authentication by Hash (MDD) 15
     - 2.2.4 Selection of ATCM Wait Cycle (MDWn) 15
   - 2.3 Mode Input Voltage and Timing 16
   - 2.4 Notes 17

3. Oscillator Circuit 18
   - 3.1 Clock Pins 18
   - 3.2 External Clock Connection 18
   - 3.3 Crystal Resonator Connection 19
     - 3.3.1 Example PCB Layouts 20

4. Flash Memory 22
   - 4.1 xSPIn (n = 0, 1) Boot Mode (x1 Boot Serial Flash Mode) 22
     - 4.1.1 For Serial Flash With Hardware Reset 23
     - 4.1.2 For Serial Flash Without Hardware Reset 24
   - 4.2 xSPI0 Boot Mode (x8 Boot Serial Flash Mode) 25

5. Ethernet 26
   - 5.1 Ethernet PHY 26
     - 5.1.1 Notes on the Ethernet PHY Layout 29

5.2 EtherCAT 30
5.2.1 PHY Addresses 30
5.2.2 Connection with PHY 30
5.2.3 Connection with EEPROM 31
5.2.4 Connection with LEDs 32

6. eMMC and SD 33
6.1 eMMC 34
6.2 SD 35

7. PCIe 37
7.1 PCB Specifications and Layout 37
7.1.1 Thickness and Number of Layers of PCB 37
7.1.2 Notes on PCB Layout 37
7.1.3 Recommended Power Filter Configuration 38
7.2 Example Circuits 39
7.2.1 Root Complex 39
7.2.2 End Point 40

8. LPDDR4 41

9. USB2.0 42
9.1 Notes on PCB Layout 42
9.2 Recommended Power Filter Configuration 43
9.3 Example Circuits 44
9.3.1 Host Controller Circuit Example 44
9.3.2 Function Controller Circuit Example 45
9.3.3 OTG System Circuit Example 46

10. ADC 47
10.1 Notes on PCB Layout 47
10.2 Recommended Power Filter Configuration 47

11. PLL 48
11.1 Notes on PCB Layout 48
11.2 Recommended Power Filter Configuration 48

12. OTP 49
12.1 Notes on PCB Layout 49
12.2 Recommended Power Filter Configuration 49

13. TSU 50
13.1 Notes on PCB Layout 50
13.2 Recommended Power Filter Configuration 50
14. Handling of Unused Pins 52
15. Other Bypass Capacitors 53
15.1 Bypass Capacitors for I/O Power 53
15.2 Bypass Capacitors for Core Power 53
REVISION HISTORY 55
General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products 56
Notice 57

1. Power Supply

1.1 Power Supply

RZ/T2H and RZ/N2H group LSIs have the power supplies shown in **Table 1.1**.

- When designing a board, separate the digital power supply and the analog power supply as far away as possible to prevent switching noise from the digital power supply.
- Connect all power supply and ground pins. Operation of the LSI is not guaranteed if there are open pins.

Table 1.1 Power Supply

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage (3.3-V I/O)	VDD33, VDD1833_0 to VDD1833_7 (3.3-V mode)	3.135	3.3	3.465	V
Power supply voltage (1.8-V I/O)	VDD1833_0 to VDD1833_7 (1.8-V mode), VDDP_18_33, VDDP_18_0 to VDDP_18_7	1.71	1.8	1.89	V
Power supply voltage (Core)	VDD08	0.76	0.8	0.84	V
Ground	VSS	—	0	—	V
Oscillator power supply voltage	VDD33_X	3.135	3.3	3.465	V
	VDDP_18_X	1.71	1.8	1.89	V
PLL power supply voltage	VDD18_PLL0 to VDD18_PLL4	1.71	1.8	1.89	V
	VDD08_PLL0 to VDD08_PLL4	0.76	0.8	0.84	V
	VSS_PLL0 to VSS_PLL4	—	0	—	V
TSU power supply voltage	AVDD18A_TSU	1.71	1.8	1.89	V
	DVDD08A_TSU	0.76	0.8	0.84	V
OTP power supply voltage	OTPVDD18	1.71	1.8	1.89	V
	OTPVDD08	0.76	0.8	0.84	V
USB power supply voltage	USB_USVDD33	3.135	3.3	3.465	V
	USB_USVDD18	1.71	1.8	1.89	V
	USB_USDVDD	0.76	0.8	0.84	V
PCI Express power supply voltage	PCIE_VDD18A_CMN, PCIE_VDD18A_L0, PCIE_VDD18A_L1	1.71	1.8	1.89	V
	PCIE_VDD08A_L0, PCIE_VDD08A_L1	0.76	0.8	0.84	V
LPDDR4 power supply voltage	DDR_VAA	1.71	1.8	1.89	V
	DDR_VDDQ	1.06	1.1	1.17	V
ADC12 power supply voltage	AVDDIO_ADC0 to AVDDIO_ADC2	1.71	1.8	1.89	V
	AVDD_ADC0 to AVDD_ADC2	0.76	0.8	0.84	V
	AVSSIO_ADC0 to AVSSIO_ADC2	—	0	—	V
	AVSS_ADC0 to AVSS_ADC2	—	0	—	V

1.2 Power-On/Off Sequence

The power-on/off sequence and its timing are shown in **Figure 1.1** and **Table 1.2**.

Turning power on requires supplying 0.8-V power (VDD08) first, then 1.8-V power (VDD18, AVDD), 1.1-V power, and 3.3-V power (DDR_VDDQ, VDD33), in that order. The power-on sequence must be completed within 100 ms. A reset signal (RES#) must be held at the low level during power-on.

Turning power off requires powering down 1.1-V and 3.3-V power (DDR_VDDQ, VDD33) first, and then 0.8-V and 1.8-V power (VDD08, VDD18, and AVDD). The power-off sequence must be completed within 100 ms.

The rise time of each power supply at power-on must be longer than 40 µs, and the fall time at power-off must be longer than 10 µs.

The power supply voltages and reset signal must rise monotonically.

Do not apply a negative voltage to the power supply voltages.

A stable clock must be supplied to the EXTAL/XTAL or EXTCLKIN pin when the reset signal (RES#) is driven high.

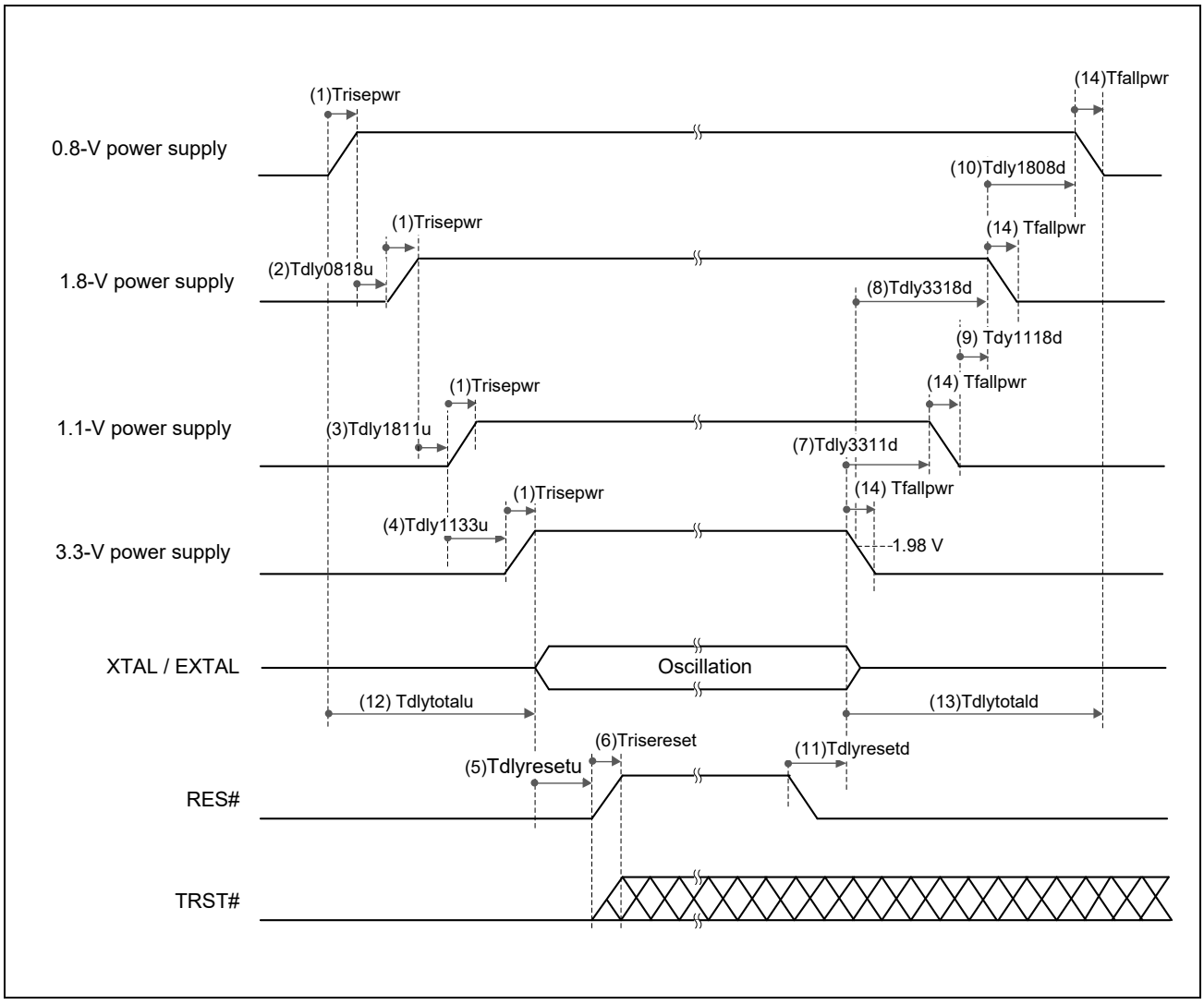

Figure 1.1 Power-On/Off Sequence

Table 1.2 Power-On/Off Sequence Timing

No	Symbol	Description	Value		
			Min.	Typ.	Max.
(1)	Trisepwr	Rising time of the power supply voltage	40 µs	—	30 ms
(2)	Tdly0818u	Delay time from the completion of the rising of the 0.8-V power supply voltage to the start of the rising of the 1.8-V power supply voltage	1 µs	—	100 ms
(3)	Tdly1811u	Delay time from the completion of the rising of the 1.8-V power supply voltage to the start of the rising of the 1.1-V power supply voltage	0	—	100 ms
(4)	Tdly1133u	Delay time from the start of the rising of the 1.1-V power supply voltage to the start of the rising of the 3.3-V power supply voltage	0	—	100 ms
(5)	Tdlyresetu	Delay time from the completion of the rising of the 3.3-V power supply voltage to the start of the rising of RES#	10 ms	—	—
(6)	Trisereset	Rising time of RES#	—	—	150 µs
(7)	Tdly3311d	Delay time from the start of the falling of the 3.3-V power supply voltage to the start of the falling of the 1.1-V power supply voltage	0	—	100 ms
(8)	Tdly3318d	Delay time from the time when the 3.3-V power supply voltage drops below 1.98 V to the start of the falling of the 1.8-V power supply voltage	0	—	100 ms
(9)	Tdly1118d	Delay time from the completion of the falling of the 1.1-V power supply voltage to the start of the falling of the 1.8-V power supply voltage	0	—	100 ms
(10)	Tdly1808d	Delay time from the start of the falling of the 1.8-V power supply voltage to the start of the falling of the 0.8-V power supply voltage	0	—	100 ms
(11)	Tdlyresetd	Delay time from the start of the falling of RES# to the start of the falling of the 3.3-V power supply voltage	10 µs	—	—
(12)	Tdlytotalu	Startup time of all power supply voltages	0	—	100 ms
(13)	Tdlytotald	Shutdown time of all power supply voltages	0	—	100 ms
(14)	Tfallpwr	Falling time of the power supply voltage	10 µs	—	30 ms

1.2.1 Example of a Power Supply Circuit Using GreenPAK

Figure 1.2 shows an example of a power supply circuit using GreenPAK™ (SLG7RN47598). **Figure 1.3** shows the timing chart of this power supply circuit example.

This circuit realizes the power on/off sequence by controlling the enable signal of each regulator. Note that this example circuit omits the regulator peripheral circuit. Refer to each regulator's datasheet for details. When the power is turned off (switched off), the fall time of each regulator output differs depending on the system configuration (circuit load), so add a discharge resistor as required. Note that it does not support the instantaneous power outage of the main power source.

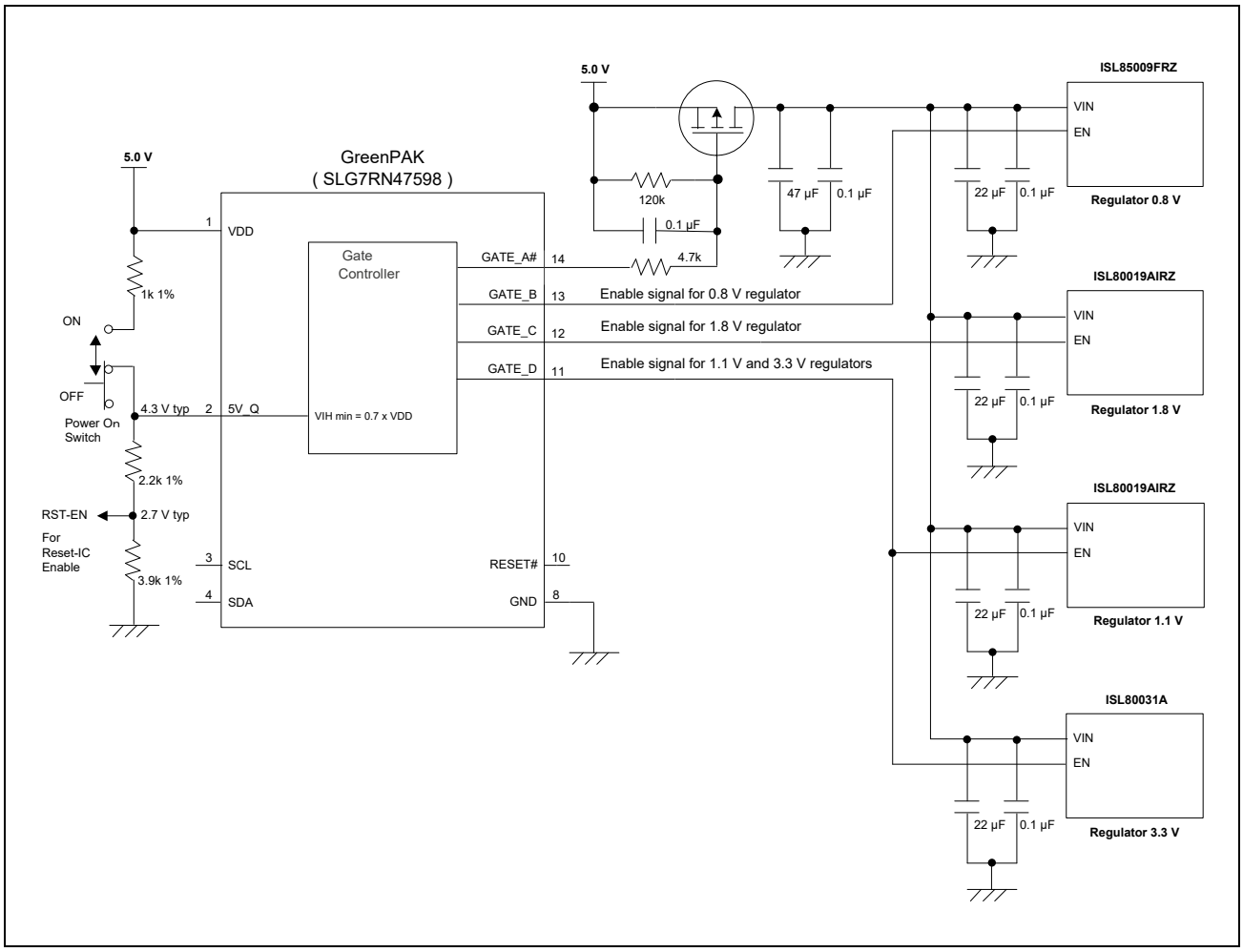

Figure 1.2 Example of a Power Supply Circuit Using GreenPAK

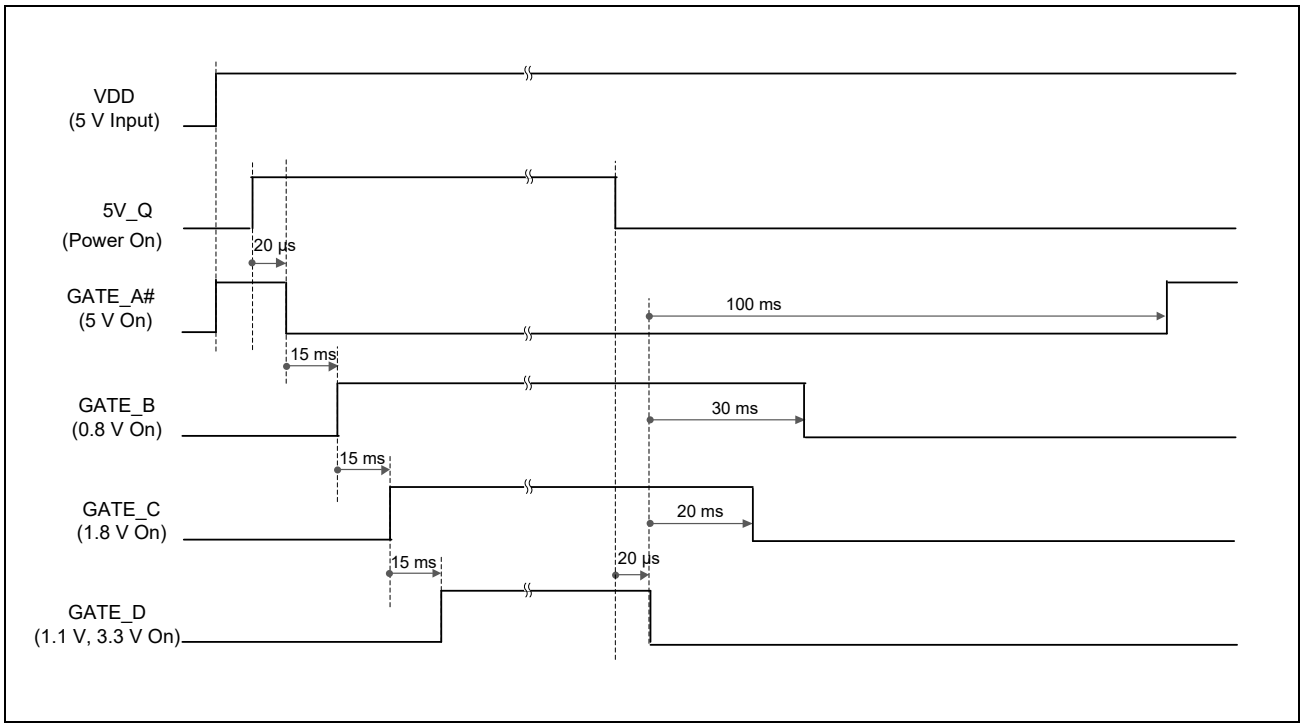

Figure 1.3 Timing Chart of a Power Supply Circuit Using GreenPAK (SLG7RN47598)

1.2.2 Example of a Power Supply Circuit Using PMIC

Figure 1.4 shows an example of a power supply circuit using DA9080-66FCBx. It realizes the power on/off sequence of this LSI. **Figure 1.5** shows a timing chart for this power supply circuit example. When the power（EN terminal of DA9080）is turned off , the fall time of each regulator output differs depending on the system configuration (circuit load), so add a discharge resistor as required. Note that it does not support the instantaneous power outage of the main power source.

In addition, note that DA9080-66FCBx are custom products with OTP settings for RZ/T2H and RZ/N2H. For more information, please refer to the application note AN-PM-212.

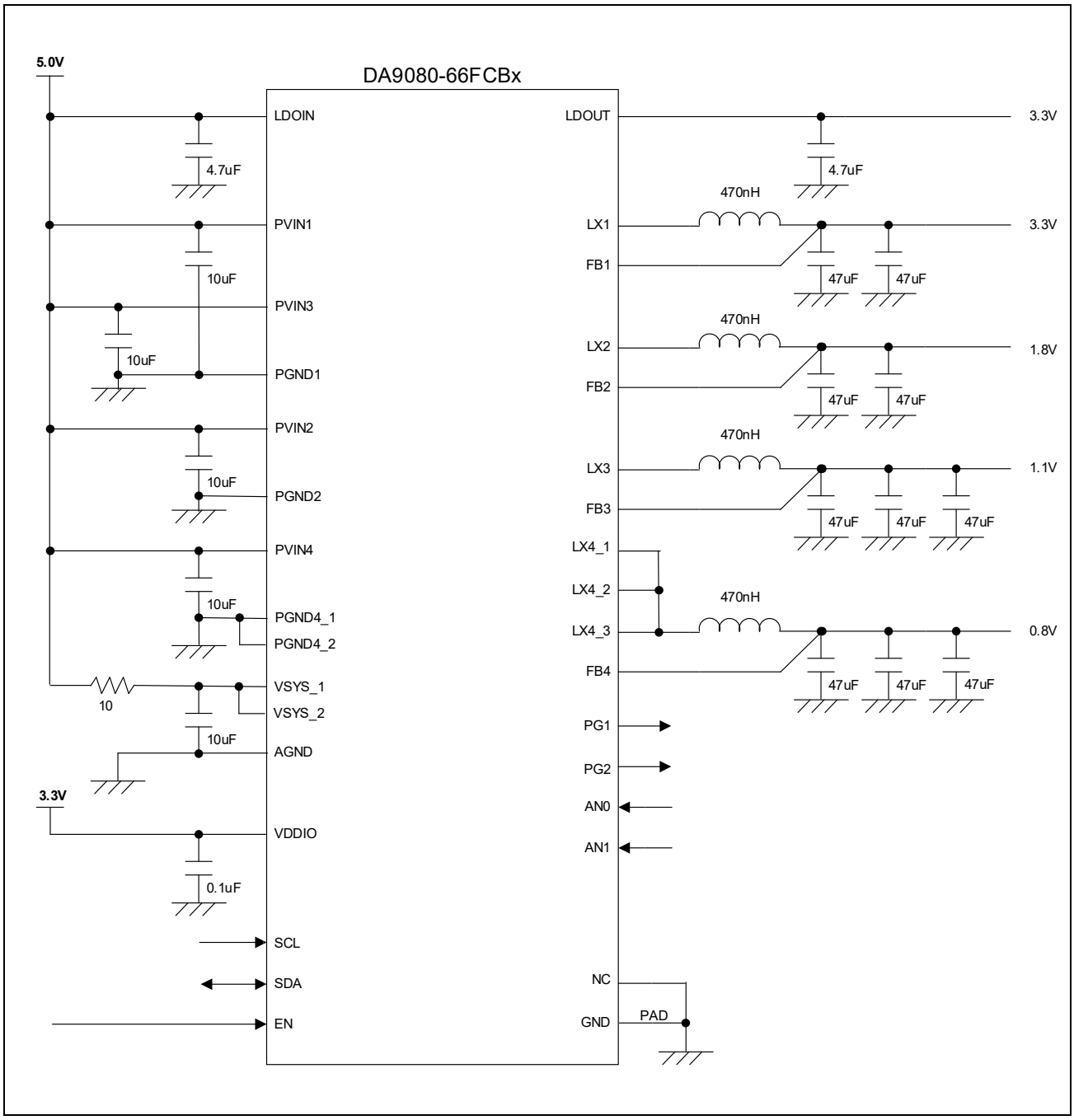

Figure 1.4 Example of a Power Supply Circuit Using DA9080-66FCBx

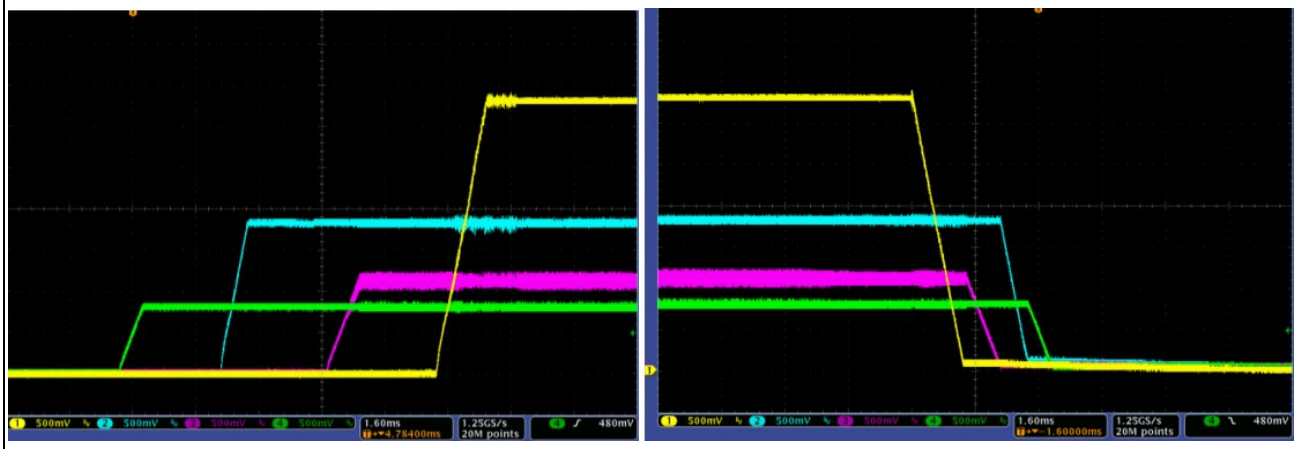

Figure 1.5 Timing Chart of Power Supply Circuit Using DA9080-66FCBx

1.2.3 Reset Circuit

Figure 1.6 shows an example reset circuit. In this example, the reset circuit including the JTAG interface can be easily configured by using GreenPAK (SLG7RN46360). The EXTRST pin is an optional function, so there is no problem with having a pull-up resistor only. **Figure 1.7** shows an example of the timing of the reset circuit.

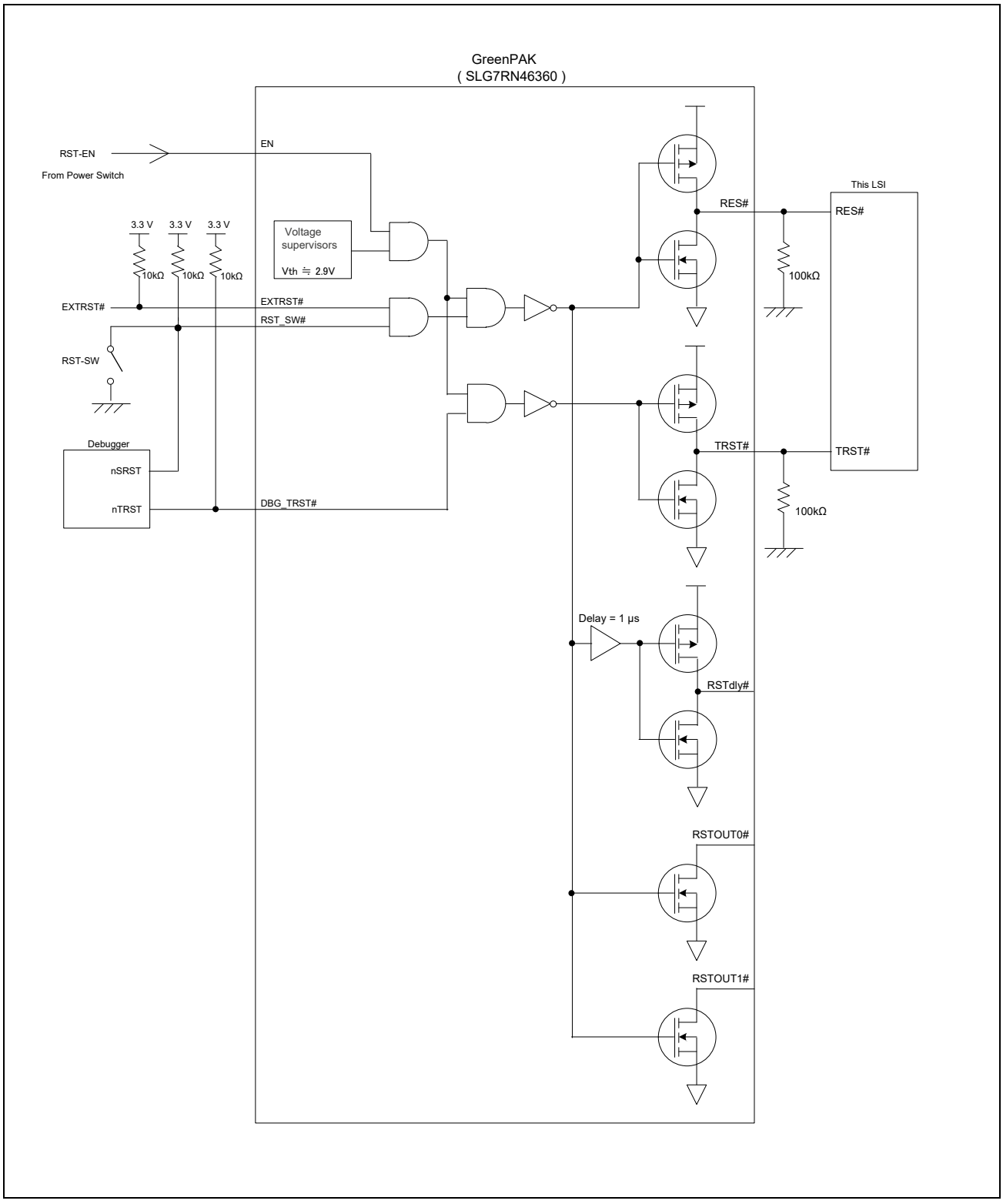

Figure 1.6 Reset Circuit

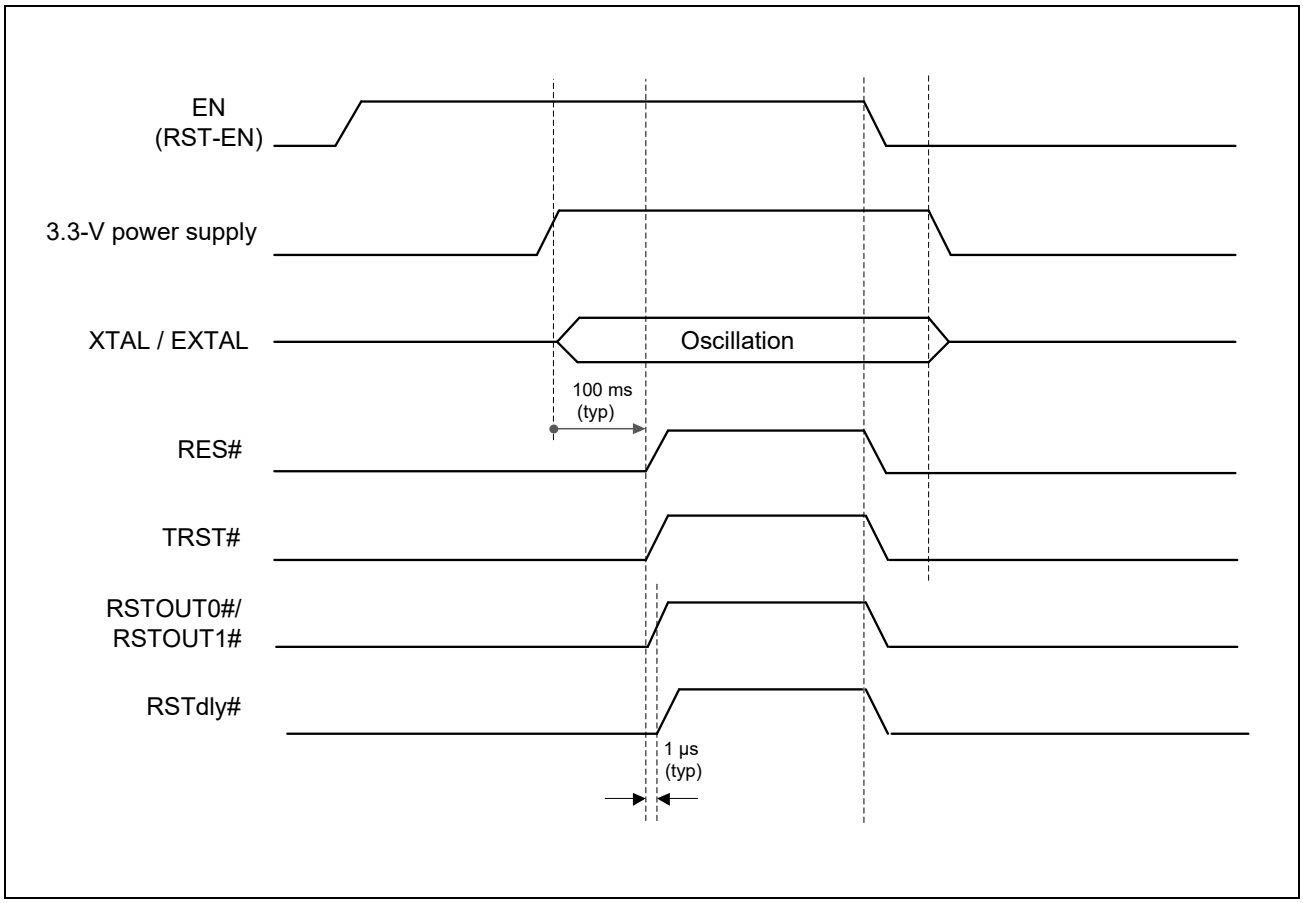

Figure 1.7 Example of Timing of the Reset Circuit

2. Operating Mode

2.1 Overview

This LSI is intended for booting up from an external flash memory. In the mode for booting from flash memory, booting processing is executed by starting from the user program stored in the supported external flash memory. Secure boot mode, which protects the user program with encryption, is also selectable for products that support security functions.

2.2 Types and Selection of Operating Mode

2.2.1 Operating Modes (MDn)

Seven types of operating mode are selectable with the method of connecting the external flash memory and device. The operating mode is selected by the input levels on the mode setting pins (MD2 to MD0) when the pin reset (except a software reset) is released.

Table 2.1 shows the relationship between the input levels of the mode setting pins (MD2 to MD0) at the time of reset release and the operating mode to be selected. The values on the pins (MD2 to MD0) are latched to the registers at reset release.

Table 2.1 MDn Setting Pin Settings

Mode Setting Pins			
MD2	MD1	MD0	Operating Mode
Low	Low	Low	xSPI0 boot mode (x1 boot serial flash) Boots a program from x1 boot serial flash memory connected to the xSPI0 CS0 space. Supporting voltage (3.3 V or 1.8 V)
Low	Low	High	xSPI0 boot mode (x8 boot serial flash) Boots a program from x8 boot serial flash memory such as HyperFlash™ memory connected to the xSPI0 CS0 space. Supporting voltage (3.3 V or 1.8 V)
Low	High	Low	xSPI1 boot mode (x1 boot serial flash) Boots a program from x1 boot serial flash memory connected to the xSPI1 CS0 space. Supporting voltage (3.3 V or 1.8 V)
Low	High	High	eSD boot mode Boots a program from eSD connected to SDHI1. Supporting voltage (3.3 V)
High	Low	Low	eMMC boot mode Boots a program from eMMC connected to SDHI0. Supporting voltage (3.3 V or 1.8 V)
High	Low	High	SCI (UART) boot mode Boots a program from a host PC through UART communication connected to SCI0. For flash writer use.
High	High	Low	USB boot mode Boots a program from a host PC through USB. For flash writer use.
High	High	High	Reserved (setting prohibited)

2.2.2 Operating Voltage of Separated I/O Domain (MDV)

The IO voltage of boot peripherals supporting 3.3 V or 1.8 V is selected based on the input level of the voltage setting pin (MDV). **Table 2.2** shows the selection of the IO voltage of boot peripherals supporting 3.3 V or 1.8 V. The value on the pin (MDV) is latched to the register at reset release. The target operating mode is xSPI0 boot mode (x1, x8), xSPI1 boot mode (x1), or eMMC boot mode. In eSD boot mode, SCI boot mode, or USB boot mode, the MDV setting has no effect.

Table 2.2 Selection of IO Voltage of Boot Peripherals Supporting 3.3 V or 1.8 V

MDV	Power Supply Pin
Low	1.8 V
High	3.3 V

2.2.3 Selection of JTAG Authentication by Hash (MDD)

JTAG authentication by hash is handled by the boot ROM. The boot ROM must identify whether JTAG is connected through the boot sequence. JTAG authentication by the hash enabling pin (MDD) is used to notify the CPU of whether JTAG is connected securely. The value on this pin is latched to the register at reset release in the same way as for the other mode setting pins. This pin is valid for products that support security functions.

Table 2.3 Selection of JTAG Authentication by Hash

MDD	JTAG Mode
Low	Normal mode JTAG authentication by hash is disabled
High	JTAG authentication by hash mode

2.2.4 Selection of ATCM Wait Cycle (MDWn)

The ATCM wait cycle for Cortex-R52 is selectable from no waiting or one-wait cycle only during the reset. Therefore, the ATCM wait cycle setting pins (MDW0 for CPU0; MDW1 for CPU1) are used to capture the value. The value on these pins is latched to the register at reset release in the same way as for MDn and MDV.

Table 2.4 Selection of ATCM Wait Cycle

MDW0/1	ATCM Wait Cycle
Low	No waiting. Valid when the CPU operating frequency is 500 MHz.
High	One wait cycle. Valid when the CPU operating frequency is 500 MHz or 1000 MHz. When using 1000 MHz, select this setting.

2.3 Mode Input Voltage and Timing

For the operating mode pins MDn, MDV, MDD, and MDWn, input a voltage of the appropriate level (V_{IH33}, V_{IL33}) that satisfies **Table 2.5** or **Table 2.6** according to the VDD1833_n_domain voltage until the operating mode transition is completed. Also, the mode hold time in **Table 2.7** must be satisfied (see **Figure 2.1**). The mode pins are multiplexed with the peripheral functions of this LSI, so take care when implementing them. Especially when the peripheral functions are input pins, you must also take into consideration the signal input from outside.

Table 2.5 Input Level Voltage (VDD1833_n_domain) (3.3-V Mode)

Item	Symbol	Condition	Min	Typ	Max	Unit
Input high-level voltage	V_{IH33}	—	VDD1833 × 0.7	—	VDD1833 + 0.3	V
Input low-level voltage	V_{IL33}	—	-0.3	—	VDD1833 × 0.3	V

Table 2.6 Input Level Voltage (VDD1833_n_domain) (1.8-V Mode)

Item	Symbol	Condition	Min	Typ	Max	Unit
Input high-level voltage	V_{IH18}	—	VDD1833 × 0.7	—	VDD1833 + 0.3	V
Input low-level voltage	V_{IL18}	—	-0.3	—	VDD1833 × 0.3	V

Table 2.7 Mode Hold Time

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Mode hold time (from RES#)	t_{MDH}	—	250	—	—	ns

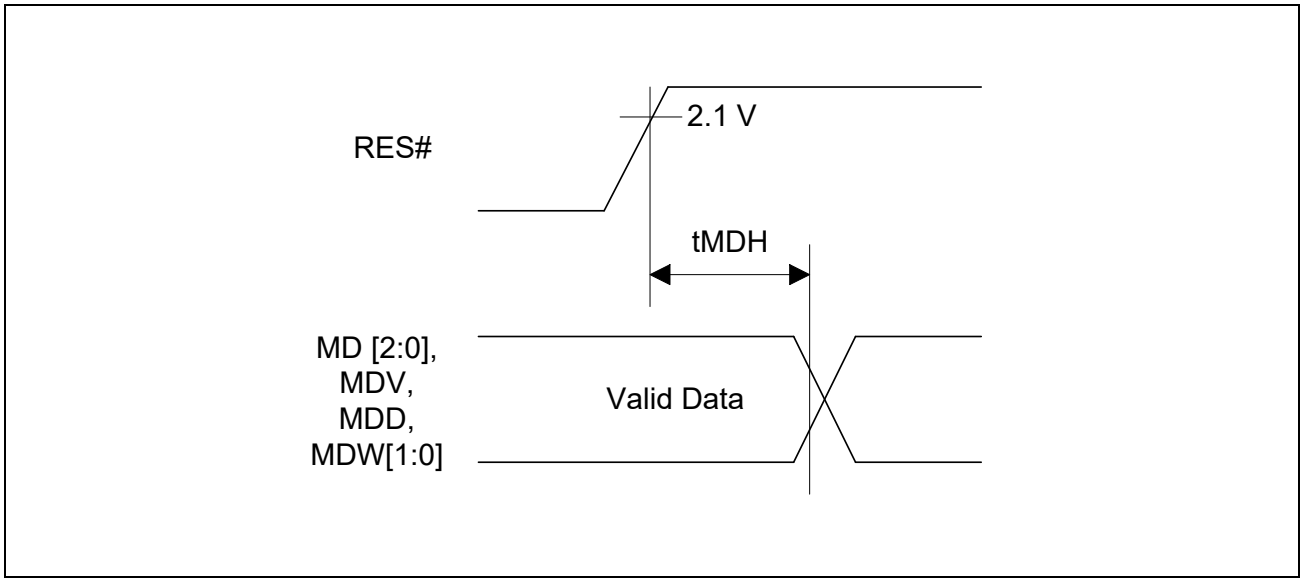

Figure 2.1 Mode Input Timing

2.4 Notes

Some of the mode setting pins MDn, MDV, MDD, and MDWn are used in common as Ethernet-related pins. Especially when using RGMII mode with Ethernet, care should be taken because the signal frequency becomes higher.

In order to suppress unnecessary reflections, place the mode setting circuit components (pull-up/pull-down resistors) as close to the LSI as possible. We recommend that the wiring length from the LSI to the components be within 1.5 cm.

3. Oscillator Circuit

3.1 Clock Pins

RZ/T2H and RZ/N2H have the method of inputting an external clock and the method of connecting a crystal resonator as a main clock.

Table 3.1 shows the pins to which a crystal resonator can be connected, or a clock can be input, and their frequencies. Using EtherCAT® requires satisfying the accuracy of ±25 ppm.

Table 3.1 Clock Pins

Xin Pin	Xout Pin	Description	Conditions	Frequency
EXTAL	XTAL	EXTAL clock input frequency	—	25.00 MHz ±50 ppm
			EtherCAT in use	25.00 MHz ±25 ppm

3.2 External Clock Connection

Figure 3.1 shows an example of connection of external clock input. Connect EXTAL to VSS via a resistor and leave XTAL open. Additionally, connect XTALSEL to VSS via a resistor.

If a crystal oscillator is used, it should be placed as close as possible to the EXTCLKIN pin. Shield the clock signal pattern for input to EXTCKIN with a circuit GND pattern of the crystal oscillator. The GND traces used for shielding should be at least 0.3 mm wide and there should be a space of 0.3 mm to 2.0 mm between them and adjacent traces.

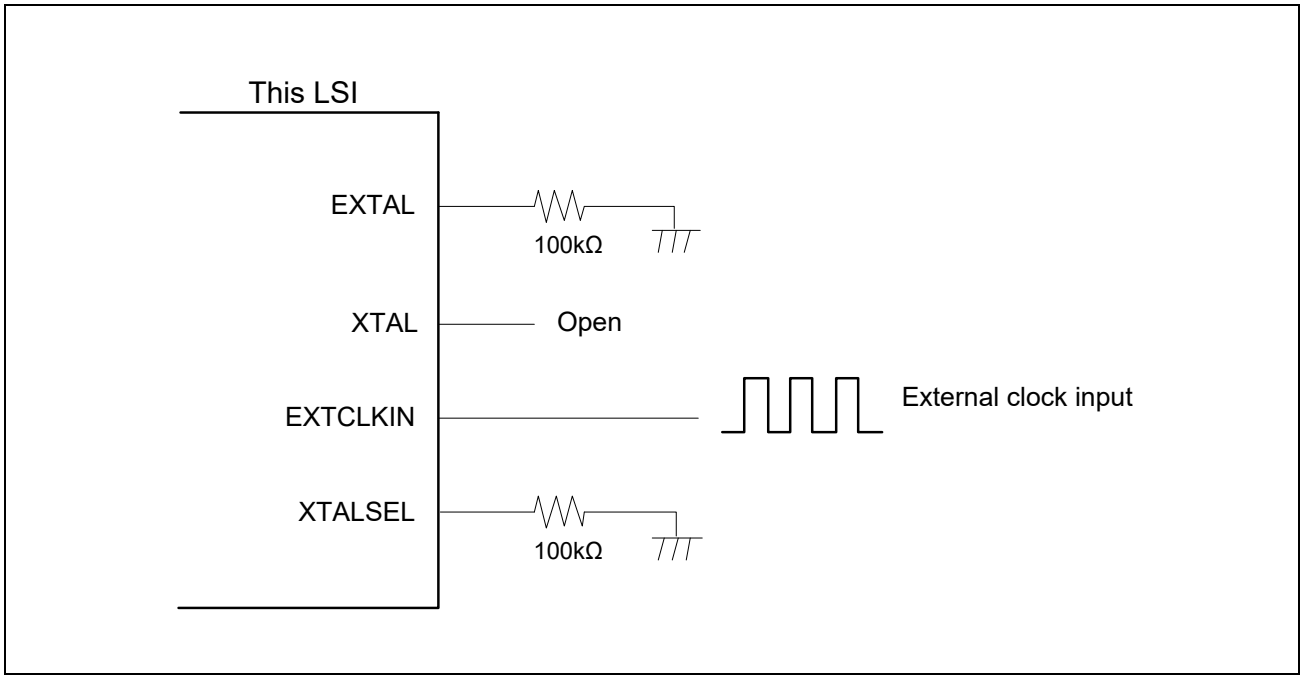

Figure 3.1 Example of External Clock Connection

3.3 Crystal Resonator Connection

Figure 3.2 shows an example of crystal resonator connection. Be sure to connect EXTCLKIN to VSS via a resistor and XTALSEL to VDD33 via a resistor.

When using a crystal resonator, which increases susceptibility to the effects of environmental temperature and noise, take special care with the layout.

It is recommended that preproduction printed-circuit board (PCB) designs include the two optional resistors Rf and Rd in case they are required for proper oscillator operation when combined with crystal circuit components.

RZ/T2H and RZ/N2H do not have a built-in feedback resistor Rif, so an external feedback resistor Rf is required. The limiting resistor Rd is recommended to be 0Ω, so it is not necessary to implement it on the PCB.

However, depending on the characteristics of the crystal resonator, an optional external resistor (Rd) may be required. The CL1 and CL2 constants shown in **Figure 3.2** are reference values and the optimum values differ depending on the characteristics of the crystal resonator. If you need the optimum oscillator circuit constants for your system, contact your crystal resonator manufacturer.

These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.

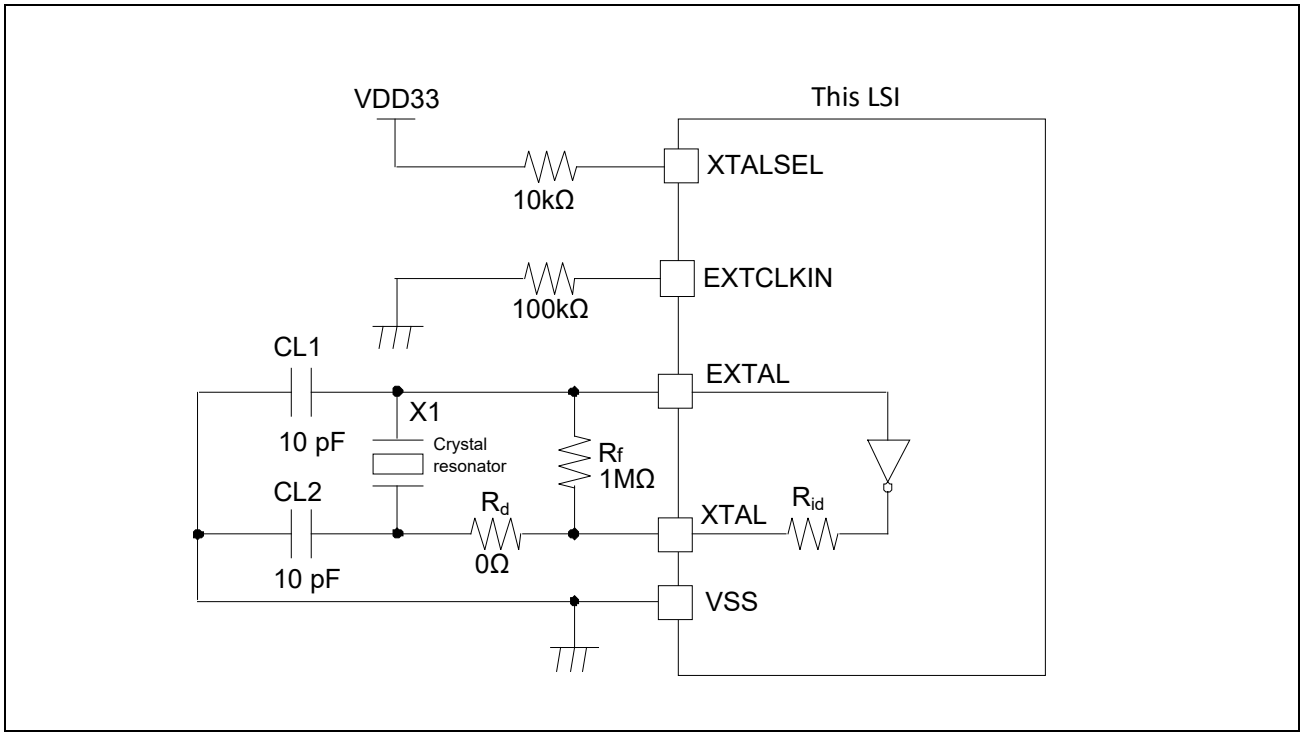

Figure 3.2 Example of Crystal Resonator Connection

3.3.1 Example PCB Layouts

This section shows example PCB layouts of the crystal resonator peripheral circuit.

If noise enters the clock I/O pins, the clock waveforms may become distorted, possibly causing an MCU malfunction or program runaway. In addition, accurate clock signals cannot be input to the MCU if there is a potential difference between the VSS inputs to the MCU and the resonator.

Figure 3.3 shows an example of PCB layout of layer 1 for the crystal connection.

Note the following points:

- The crystal resonator and capacitors CL1 and CL2 should be placed as close as possible to the Xin (EXTAL) pin and the Xout (XTAL) pin.
- To avoid inductance and to oscillate properly, use a common grounding point for the crystal resonator and additional capacitors, and do not place wiring patterns near these parts.
- Shield the wiring pattern for the clock I/O pins with the GND pattern of the crystal resonator peripheral circuit and do not arrange the traces for the clock I/O pins in parallel with or across other traces that have large current flows or rapid level changes.
- The GND traces used for shielding should be at least 0.3 mm wide and there should be a space of 0.3 mm to 2.0 mm between them and adjacent traces.

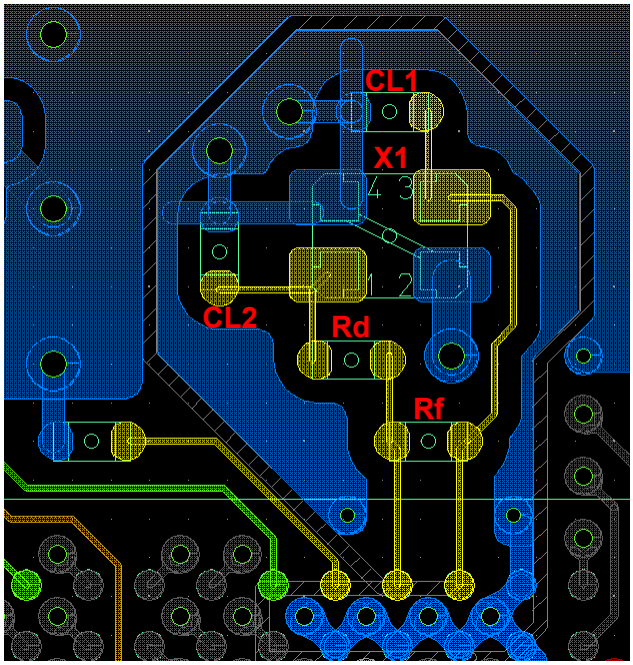

Figure 3.3 Example Layout of the First Layer (Layer 1) of the PCB

Figure 3.4 shows an example layout of the layer farthest from the oscillator circuit on the PCB.

Intermediate layer pattern wiring in the area where the crystal resonator peripheral circuit is located is prohibited as it will affect other GNDs and signals. Be sure to use the area of the layer farthest from the crystal resonator peripheral circuit as the GND of the crystal resonator peripheral circuit.

- Separate the crystal resonator GND from the digital GND (DGND).
- Connect the crystal resonator GND at one point with the GND near the LSI.

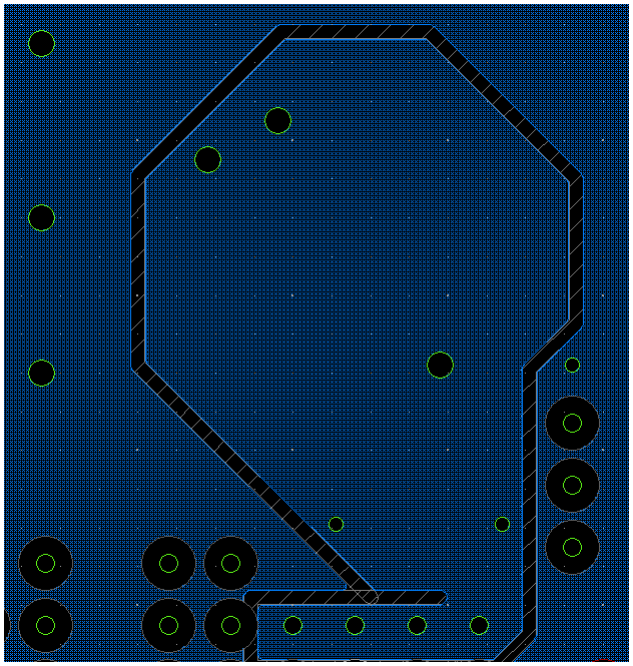

Figure 3.4 Example Layout of the Layer Farthest from the Oscillator Circuit

4. Flash Memory

Booting will fail if booting of the LSI does not coincide with the operating mode of flash memory. This section describes the points which should be taken into account for connection with flash memory.

It is necessary to switch the power supply voltage of VDD1833 depending on the power supply specification (3.3 V or 1.8 V) of the selected flash memory. **Table 4.1** shows the I/O domains and the VDD1833 voltage settings.

Table 4.1 I/O Domain and VDD1833 Voltage Setting

I/O Domain	Power Pin	Power Supply Voltage
xSPI0	VDD1833_4	3.3 V or 1.8 V
xSPI1	VDD1833_5	3.3 V or 1.8 V

4.1 xSPIn (n = 0, 1) Boot Mode (x1 Boot Serial Flash Mode)

This LSI has an xSPI controller and is designed so that external serial flash can be booted in either xSPI0 boot or xSPI1 boot (x1 boot serial flash) mode. At startup, the serial flash is accessed in protocol mode 1S-1S-1S and the system software is reset. See **Table 2.1** for this boot mode setting.

After the reset is released, processing is executed immediately after boot processing starts in xSPI n (n = 0, 1) boot mode (x1 boot serial flash) until the loader parameters are transferred.

NOTE

In x1 boot serial flash mode, if the serial flash protocol mode is switched from 1S-1S-1S to another mode by the application program, it is necessary to pay attention to the serial flash protocol mode setting after reset. If only this LSI is reset, then serial flash cannot receive the 1S command at the time of booting and cannot boot normally. The countermeasures are explained in the following sections.

4.1.1 For Serial Flash With Hardware Reset

When changing the serial flash protocol mode to other than 1S-1S-1S by the application program, implement the following software and hardware countermeasures.

(1) Switch the serial flash protocol mode to 1S-xx-xx (the command is 1S mode) before a software reset.

(2) Apply a hardware reset to the serial flash when the system is reset.

Figure 4.1 shows an example of connection of the quad serial flash with the reset pin. Applying a hardware reset to the quad serial flash also resets the protocol mode setting for the quad serial flash.

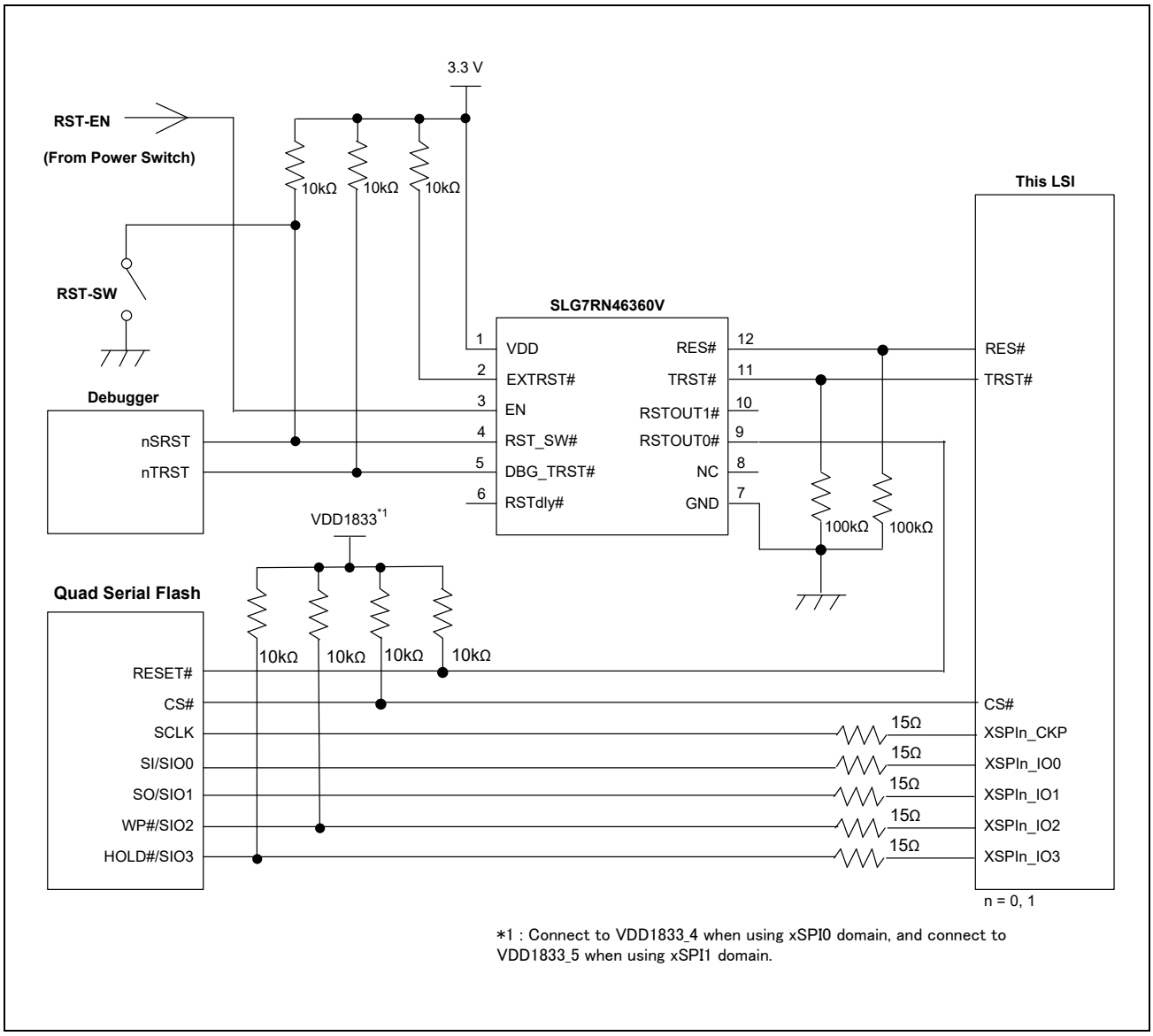

Figure 4.1 Connection Example of Quad Serial Flash with Reset Pin

4.1.2 For Serial Flash Without Hardware Reset

When using serial flash memory without a hardware reset pin, if this LSI is reset after the serial flash protocol setting has been changed from 1S-1S-1S protocol to another protocol mode by the user program, the protocol mode of the boot program does not coincide with the protocol mode of the serial flash memory, which causes a boot error. To avoid this, take the following measures:

(1) Leave the protocol mode of the serial flash as 1S-1S-1S.

(2) Use 1S-xx-xx (command is 1S).

Figure 4.2 shows an example of connection of the quad serial flash without the reset pin.

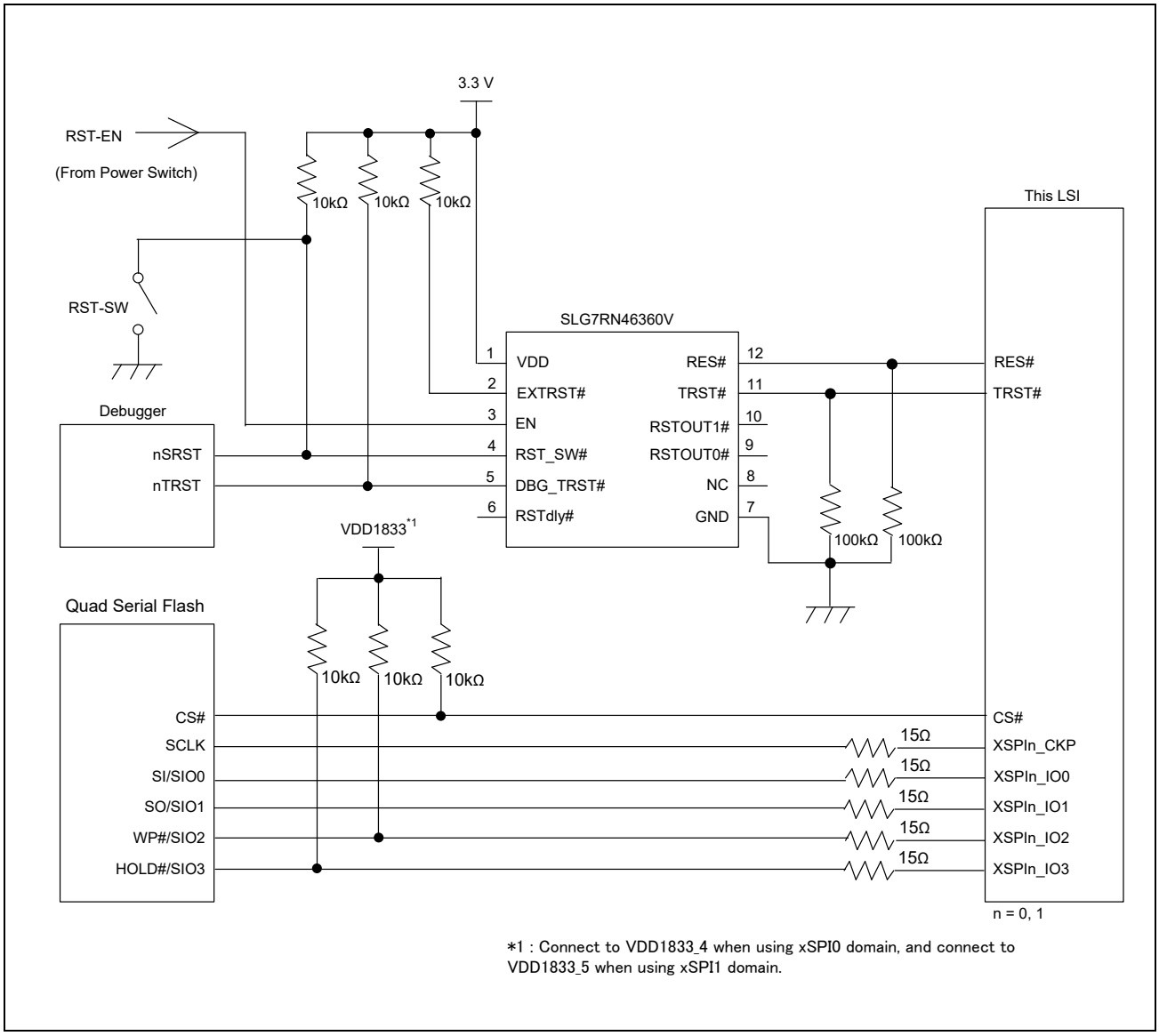

Figure 4.2 Connection Example of Quad Serial Flash without Reset Pin

4.2 xSPI0 Boot Mode (x8 Boot Serial Flash Mode)

Figure 4.3 shows an example of connection of x8 boot serial flash.

In xSPI0 boot (x8 boot serial flash) mode, the serial flash is accessed in protocol mode 8D-8D-8D profile 2.0 at startup, and a hardware reset is applied by the XSPIO_RESET#0 pin. See **Table 2.1** for this boot mode setting.

NOTE

Select a serial flash that supports protocol mode 8D-8D-8D Profile 2.0.

Data is read from HyperFlash with a read latency cycle of 10 at the time of booting. Use HyperFlash with a read latency cycle of 10.

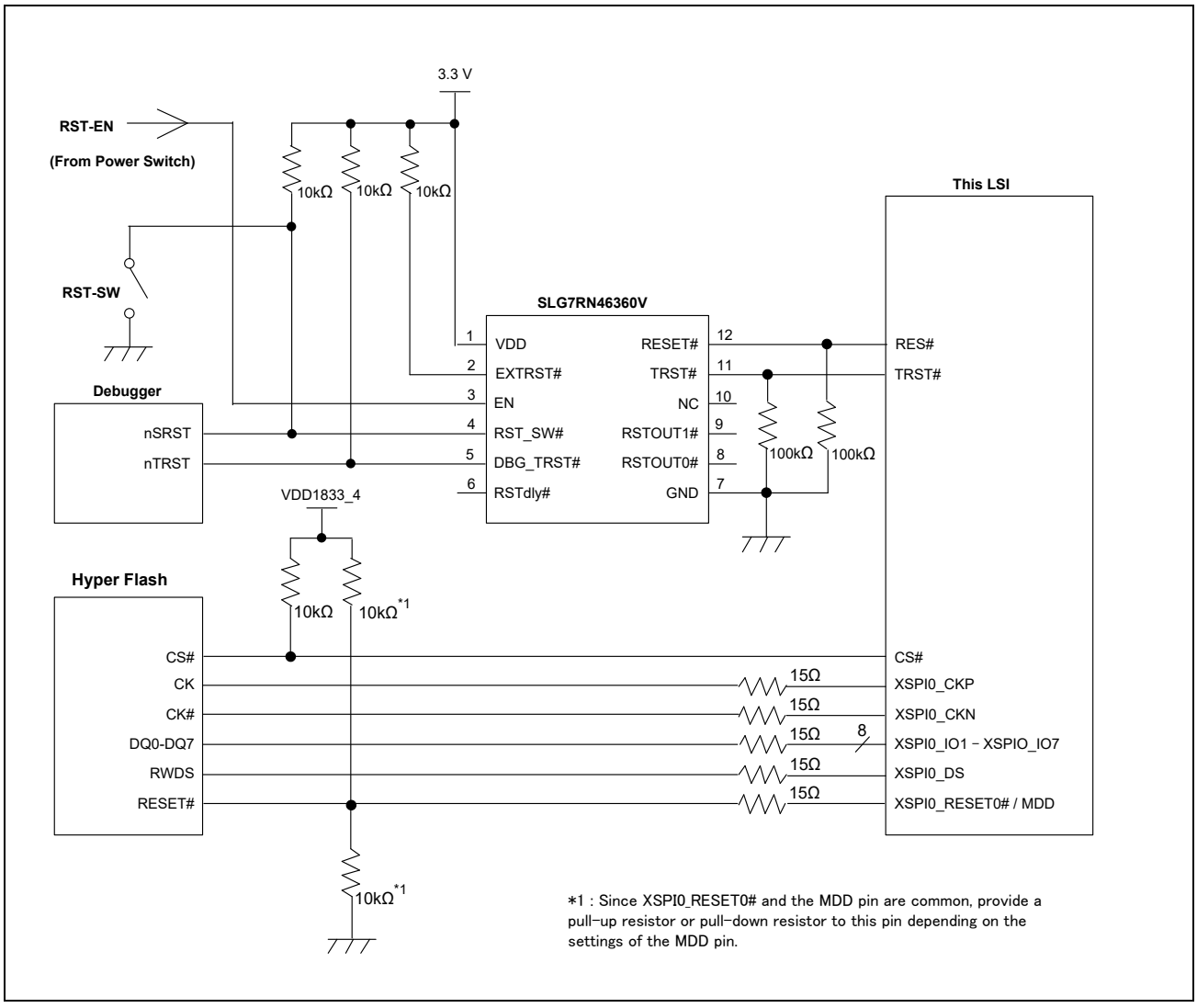

Figure 4.3 Connection Example of x8 Boot Serial Flash

5. Ethernet

5.1 Ethernet PHY

In this LSI, three Ethernet PHY interfaces are available: MII which supports 10 Mbps and 100 Mbps, RMII which has a reduced number of signals, and RGMII which supports Gigabit Ethernet. **Figure 5.1** to **Figure 5.3** show example circuits for the respective Ethernet modes. The damping resistance values for the example circuits are only examples, and the values should be determined by checking the waveforms.

Depending on the selected MII mode, the power voltage of VDD1833 must be switched. **Table 5.1** lists the MII modes and VDD1833 voltage settings.

Table 5.1 MII Modes and VDD1833 Voltage Settings

I/O Domain	Power Domain	MII / RMII	RGMII
ETH0	VDD1833_0	3.3 V	1.8 V
ETH1	VDD1833_1	3.3 V	1.8 V
ETH2	VDD1833_2	3.3 V	1.8 V
ETH3	VDD1833_3	3.3 V	1.8 V

Figure 5.1 shows an example of MII connections with Ethernet PHY.

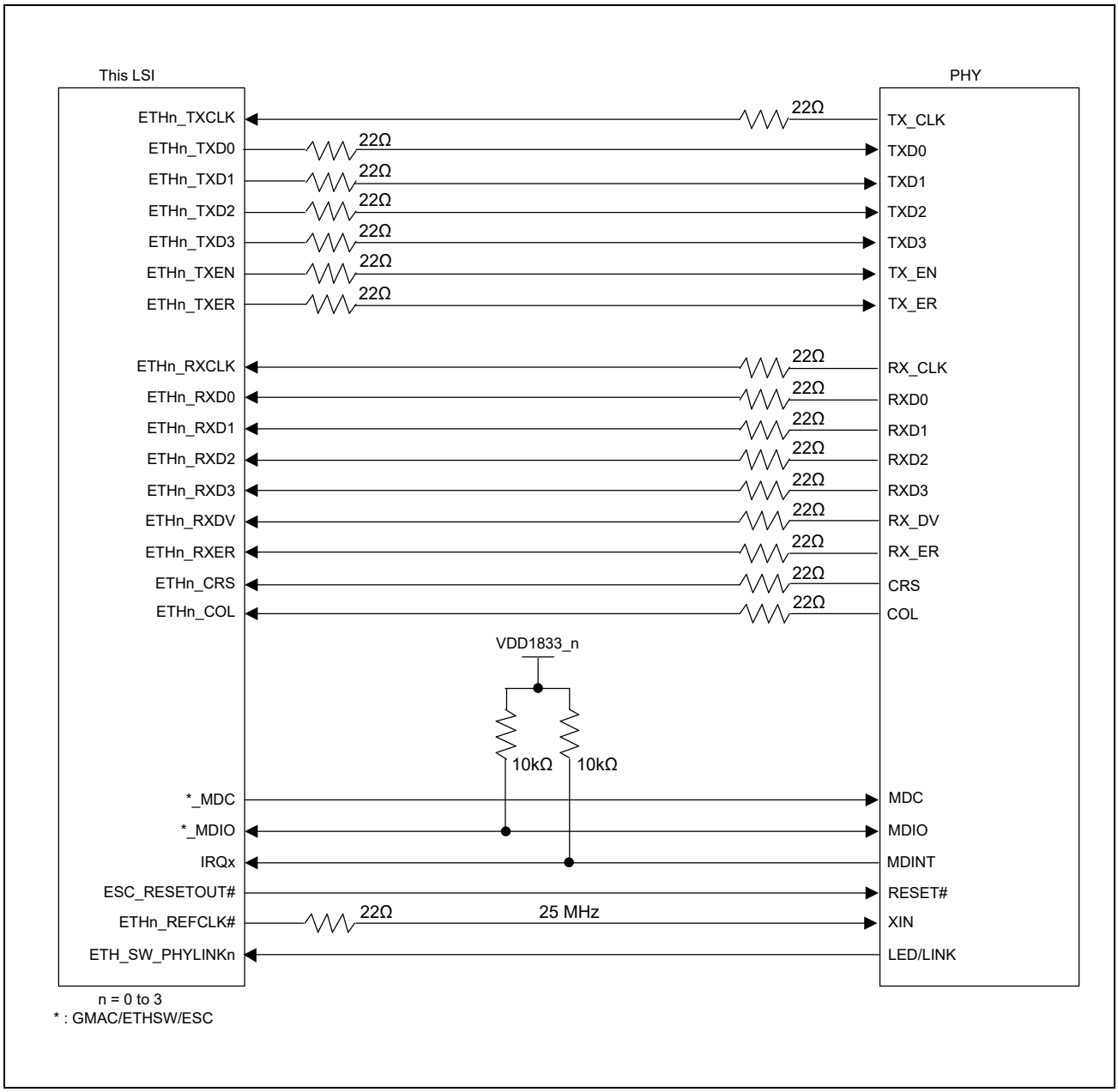

Figure 5.1 Example of MII Connections with Ethernet PHY

Figure 5.2 shows an example of RGMII connections with Ethernet PHY.

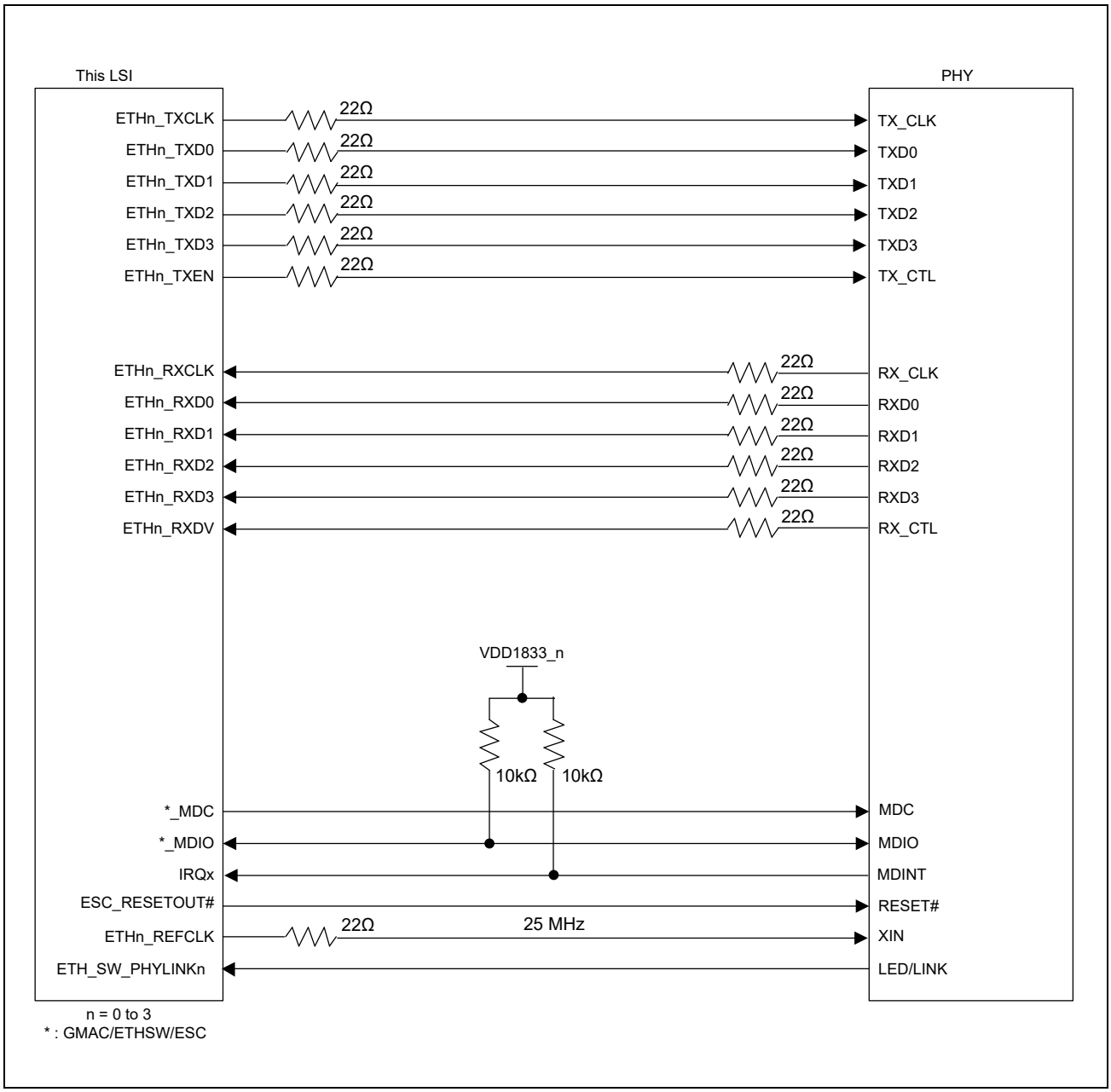

Figure 5.2 Example of RGMII Connections with Ethernet PHY

Figure 5.3 shows an example of RMII connections with Ethernet PHY.

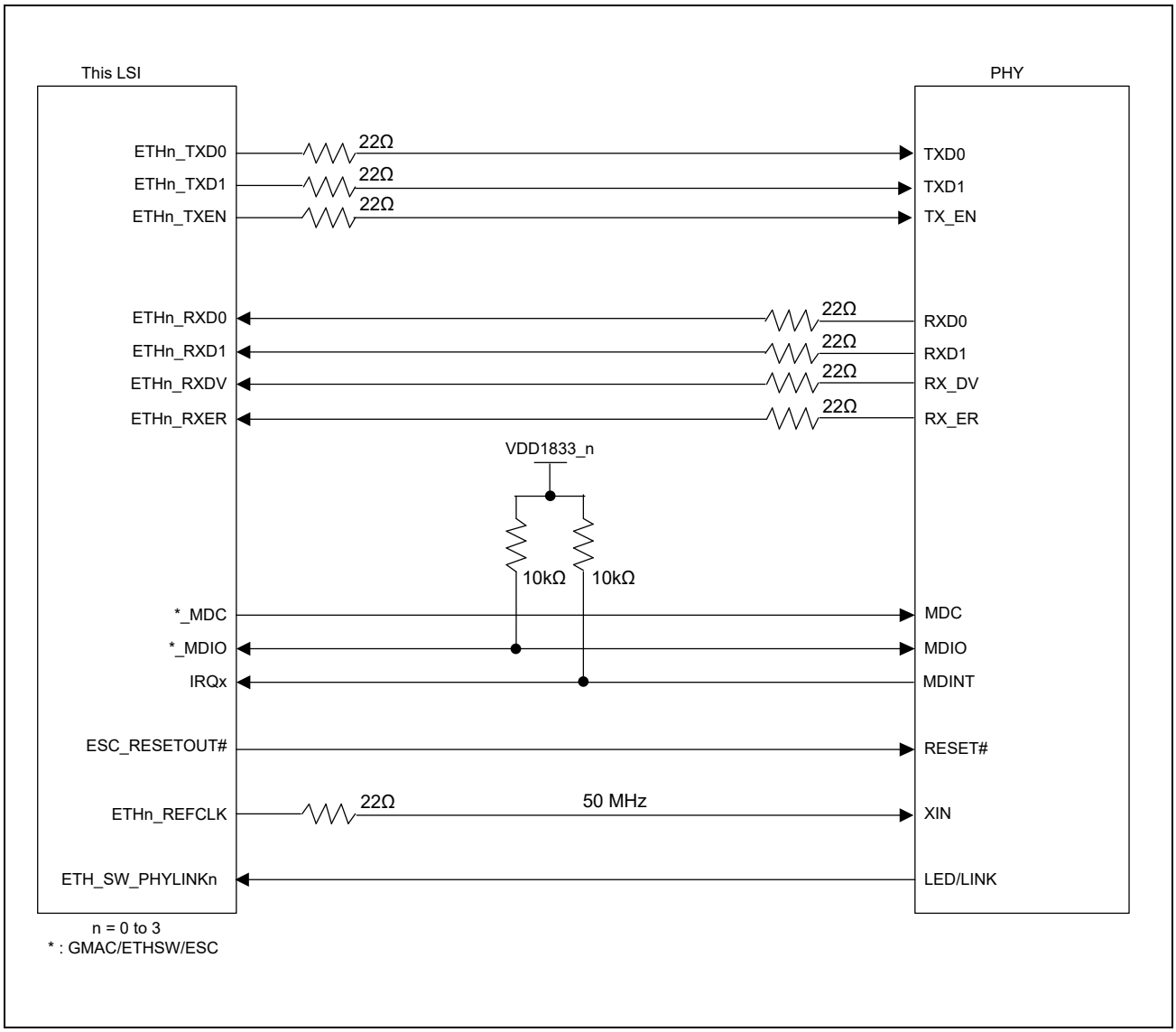

Figure 5.3 Example of RMII Connections with Ethernet PHY (when 50-MHz Clock is Output)

5.1.1 Notes on the Ethernet PHY Layout

The writing between ETHn_TXCLK and ETHn_TXD[3:0] and between ETHn_RXCLK and ETHn_RXD[3:0] should be of equal length.

5.2 EtherCAT

The following describes the connections that require attention when EtherCAT is in use. In order to obtain EtherCAT Technology Group (ETG) certification, however, be sure to refer to the related documents from the ETG.

For details of the hardware functions, refer to the Beckhoff document “EtherCAT IP Core for Xilinx FPGAs (v2.04e)”.

5.2.1 PHY Addresses

The addresses of the PHY devices should be consecutive from ESC port 0, 1 and 2 in that order. The ESC automatically accesses the PHY registers for some functions such as enhanced link detection.

The PHY base address to be detected by the ESC can be changed by using the EtherCAT PHY Offset Address Setting Register (ECATOFFADR). In the initial state, the base address is 0.

5.2.2 Connection with PHY

5.2.2.1 MAC-PHY Interface

Though this LSI supports MII, RMII, and RGMII as a MAC-PHY interface, MII is recommended in the related documents from the ETG. This is because RMII or RGMII may be inferior to MII in accuracy of EtherCAT communications due to an internal delay in the PHY. For details, contact the PHY manufacturing vendor or ETG.

5.2.2.2 Connection with the Link LED Pin of PHY

Connect the link LED of the PHY to the input signal ESC_PHYLINK0/1/2. The ESC monitors the state of the physical link by using this signal.

The active level of the signal can be changed by using the Ethernet PHY Link Mode Register (PHYLNK). The signal is active low in the initial state.

5.2.2.3 Connection with the PHY Reset Pin

When the ESC is reset, if you want to also reset the PHY synchronously, connect ESC_RESETOUT# to the reset pin of the PHY. This allows resetting the PHY at the same time as when the ESC is reset by a command from the EtherCAT master.

NOTE

In the initial reset state of the ESC, the ESC_RESETOUT# signal is in GPIO mode, so the reset pin of the PHY cannot be asserted in the initial state. After setting the corresponding pin to the output mode of GPIO to control the reset of the PHY, change PinMux to ESC_RESETOUT# mode.

5.2.2.4 REFCLK and TXCLK Signals

With EtherCAT, it is ideal that the operating clock of the PHY and that of the ESC are in the same phase, so the 25-MHz clock from the ETHn_REFCLK signal is connected to the 25-MHz clock input of the PHY.

Though TXCLK of the ESC is an optional pin, we recommend connecting TXCLK of the PHY to enable automatic TX shift compensation of the ESC. When the main clock is used as the reference clock of ETHn_REFCLK, the automatic TX CLK shift function must be used.

For the combinations of REFCLK and TXCLK, see **Table 5.2**.

Table 5.2 Automatic TX Shift Compensation Settings

Connection of REFCLK and PHY	Connection of TXCLK	Non-Connection of TXCLK
REFCLK with 25 MHz is connected to the PHY. PHYSEL = 0 (REFCLK is based on PLL)	Automatic TX shift is enabled. Phase adjustment by the ECATDBGC register is not required.	Automatic TX shift is disabled. Phase adjustment by the ECATDBGC register is required.
REFCLK with 25 MHz is connected to the PHY. PHYSEL = 1 (REFCLK is based on OSC)	Automatic TX shift is enabled. Phase adjustment by the ECATDBGC register is required.	Not available
REFCLK with 25 MHz is not connected to the PHY.	Automatic TX shift is enabled. Phase adjustment by the ECATDBGC register is required.	Not available

5.2.2.5 CRS and COL Signals

Since the ESC only supports full-duplex mode, it ignores the ETHn_CRS (n = 0 to 2) and ETHn_COL (n = 0 to 2) signals when the MII is connected. Accordingly, when these are only used by the ESC, the CRS and COL pins are not required.

5.2.3 Connection with EEPROM

Connect the ESC_I2CCLK and ESC_I2DATA signals to the EEPROM. The ESC loads the configuration information from the EEPROM at the time of startup.

NOTE

The communications protocol changes when the EEPROM is larger than 16 Kbits. In the initial state, the EEPROM is set for 16 Kbits or less. When the EEPROM larger than this size is connected, release the ESC from the reset after changing the setting of the EtherCAT Operation Mode Register (ECATOPMOD).

5.2.4 Connection with LEDs

Connect the ESC_LEDRUN, ESC_LEDERR, and ESC_LEDSTER (optional) signals, which indicate the operating state of the ESC, to the LEDs.

Connect the ESC_LINKACTn (n = 0 to 2) signals, which indicate the communications state of the ESC, to the LEDs. Add buffer circuits such as transistors as necessary.

Figure 5.4 shows an example of LED connections of the ESC. For details, refer to the ETG document “ETG.1300 Indicator and Labeling”.

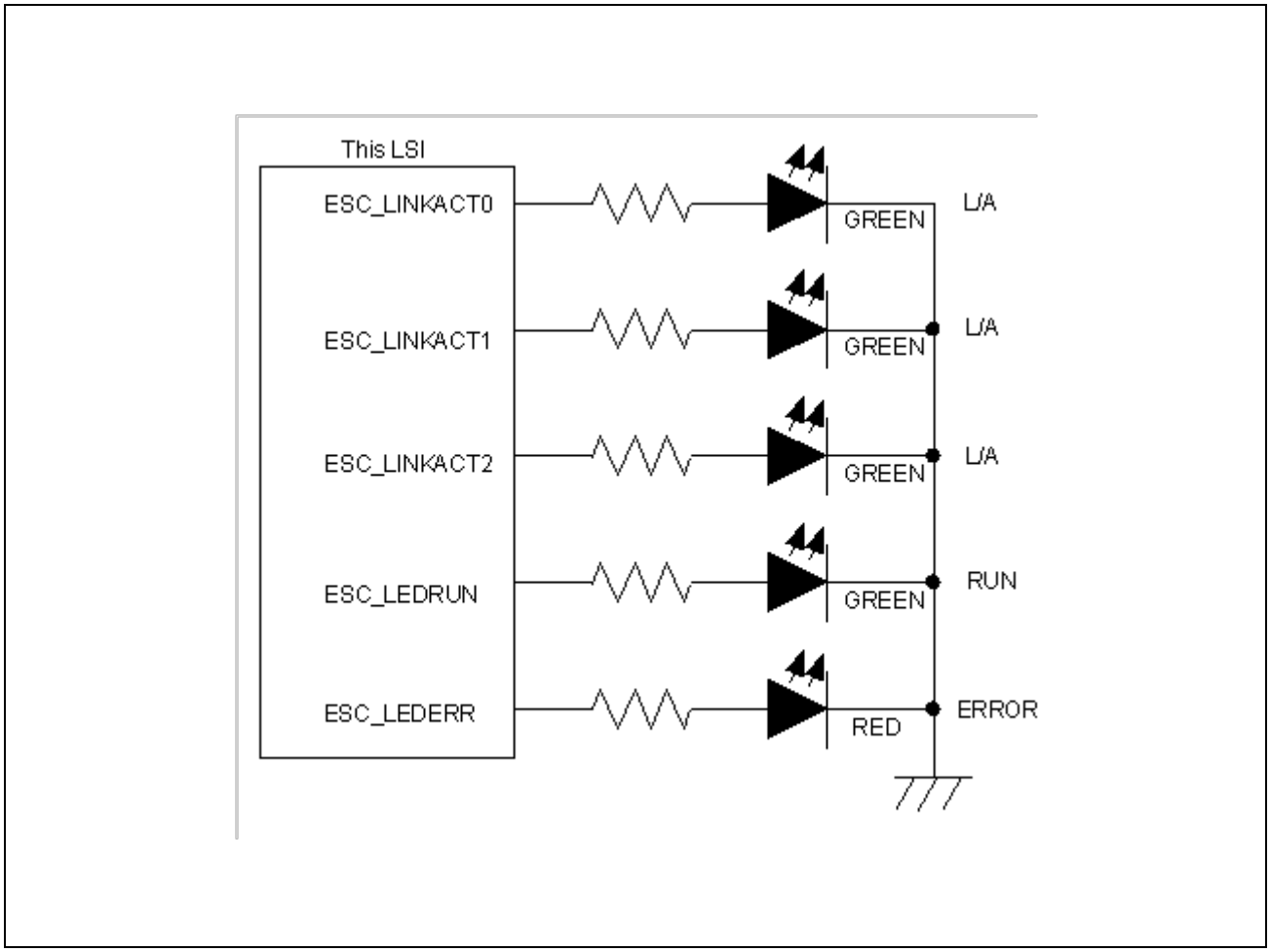

Figure 5.4 Example of LED Connections of the ESC

6. eMMC and SD

This LSI has 2 channels, SDHI0 and SDHI1, as eMMC/SD host interface.

As shown in **Table 6.1**, SDHI0 supports the eMMC or SD interface. SDHI1 only supports the SD interface.

Note the following points:

- eMMC is assigned to the SDHI0 channel only.
- eSD boot is automatically assigned to the port on the SDHI1 channel and cannot be changed.
- LVS (Low Voltage Signals) cards must support power supply switching between 3.3 V and 1.8 V. Note that power supply switching between 3.3 V and 1.8 V also occurs for general-purpose ports ((*) in **Table 6.1**) in the same power supply domain (VDD1833_6 or VDD1833_7) which are not used as SD ports.

Table 6.1 eMMC and SD Functions Assignment

Voltage Domain	Channel	Allocation Port	SD Port	eMMC Port
VDD1833_6	SDHI0	P12_0	SD0_CLK	SD0_CLK
		P12_1	SD0_CMD	SD0_CMD
		P12_2	SD0_DATA0	SD0_DATA0
		P12_3	SD0_DATA1	SD0_DATA1
		P12_4	SD0_DATA2	SD0_DATA2
		P12_5	SD0_DATA3	SD0_DATA3
		P12_6	(*)	SD0_DATA4
		P12_7	(*)	SD0_DATA5
		P13_0	(*)	SD0_DATA6
		P13_1	(*)	SD0_DATA7
		P13_2	(*)	SD0_RST#
	Other than SDHI0	P13_3	(*)	—
		P13_4	(*)	—
		P13_5	(*)	—
		P13_6	(*)	—
		P13_7	(*)	—
		P14_0	(*)	—
VDD_1833_7	SDHI1	P16_5	SD1_CLK	—
		P16_6	SD1_CMD	—
		P16_7	SD1_DATA0	—
		P17_0	SD1_DATA1	—
		P17_1	SD1_DATA2	—
		P17_2	SD1_DATA3	—
	Other than SDHI1	P17_3	(*)	—

6.1 eMMC

Figure 6.1 shows an example connection diagram between this LSI and an eMMC device.

The damping resistor and pull-up resistor values in each example circuit are only examples, and the actual values should be determined after checking the eMMC device specifications and waveforms. Note that this example circuit does not include a bypass capacitor required for the power supply, so add it as required.

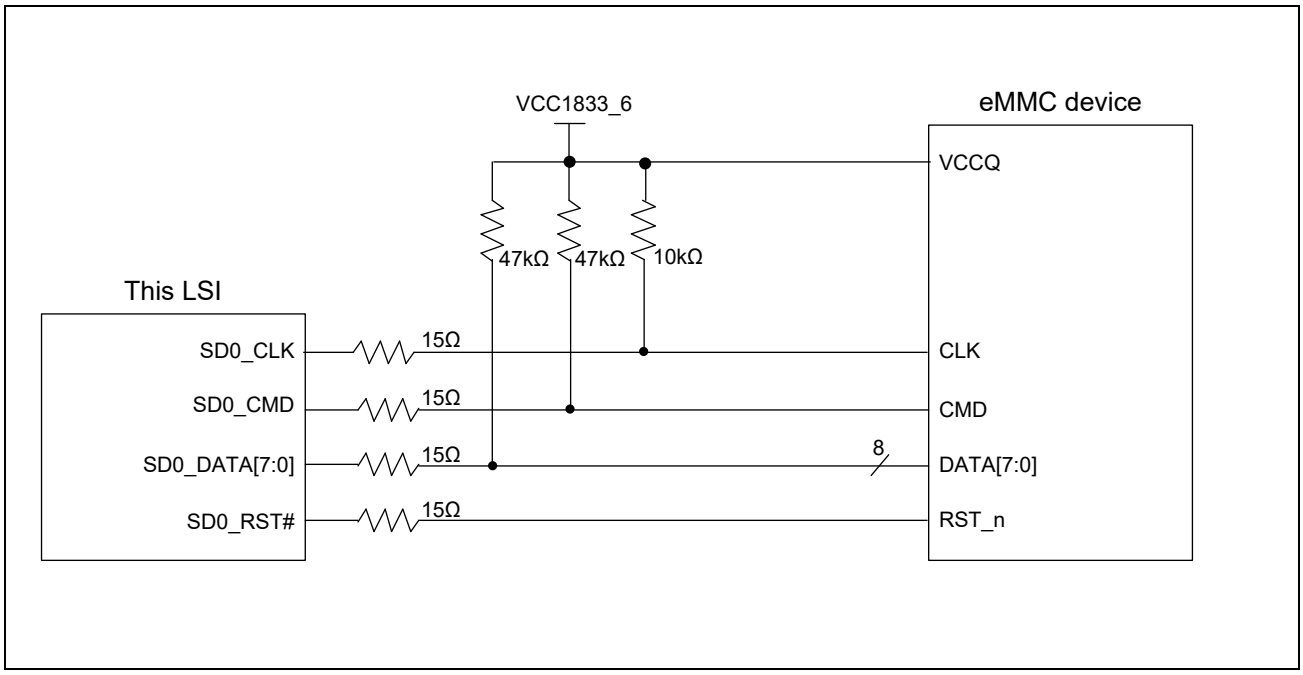

Figure 6.1 Connection Diagram of This LSI with eMMC Device

6.2 SD

Figure 6.2 shows an example of connection when using eSD boot. **Figure 6.3** shows an example of connection between this LSI and the SD slot when using the SDHI1 channel with VDD1833_7.

Regarding SDn_PWEN, use it to switch the power supplied to the SD card when the SD card needs to be initialized. In this example circuit, with the LVS (low voltage signaling) card taken into consideration, the circuit is configured to cut off the power to the SD card when it is reset.

Note that this example circuit does not include a bypass capacitor required for the power supply, so add it as required.

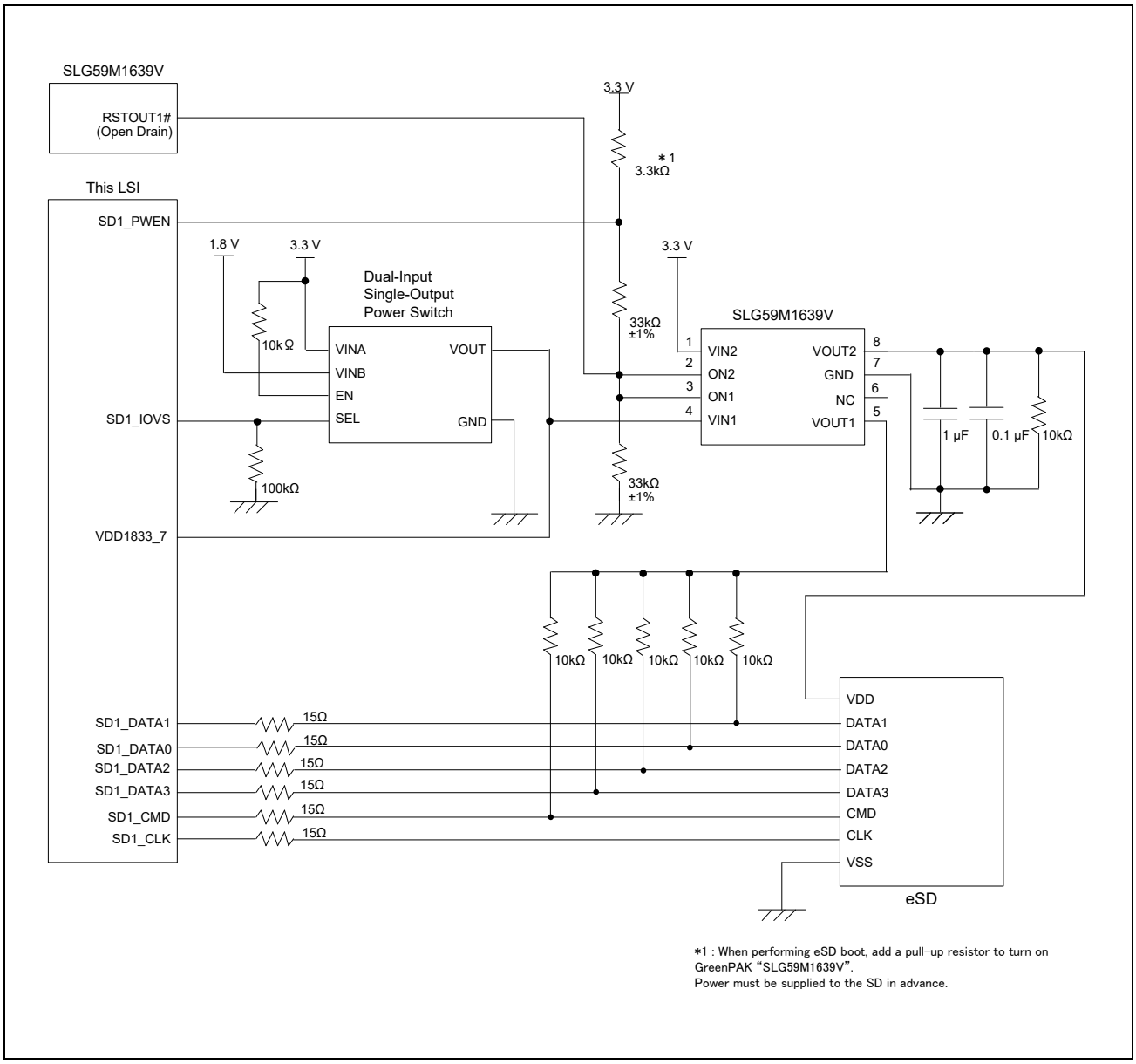

Figure 6.2 Connection Diagram of This LSI and eSD during eSD Boot

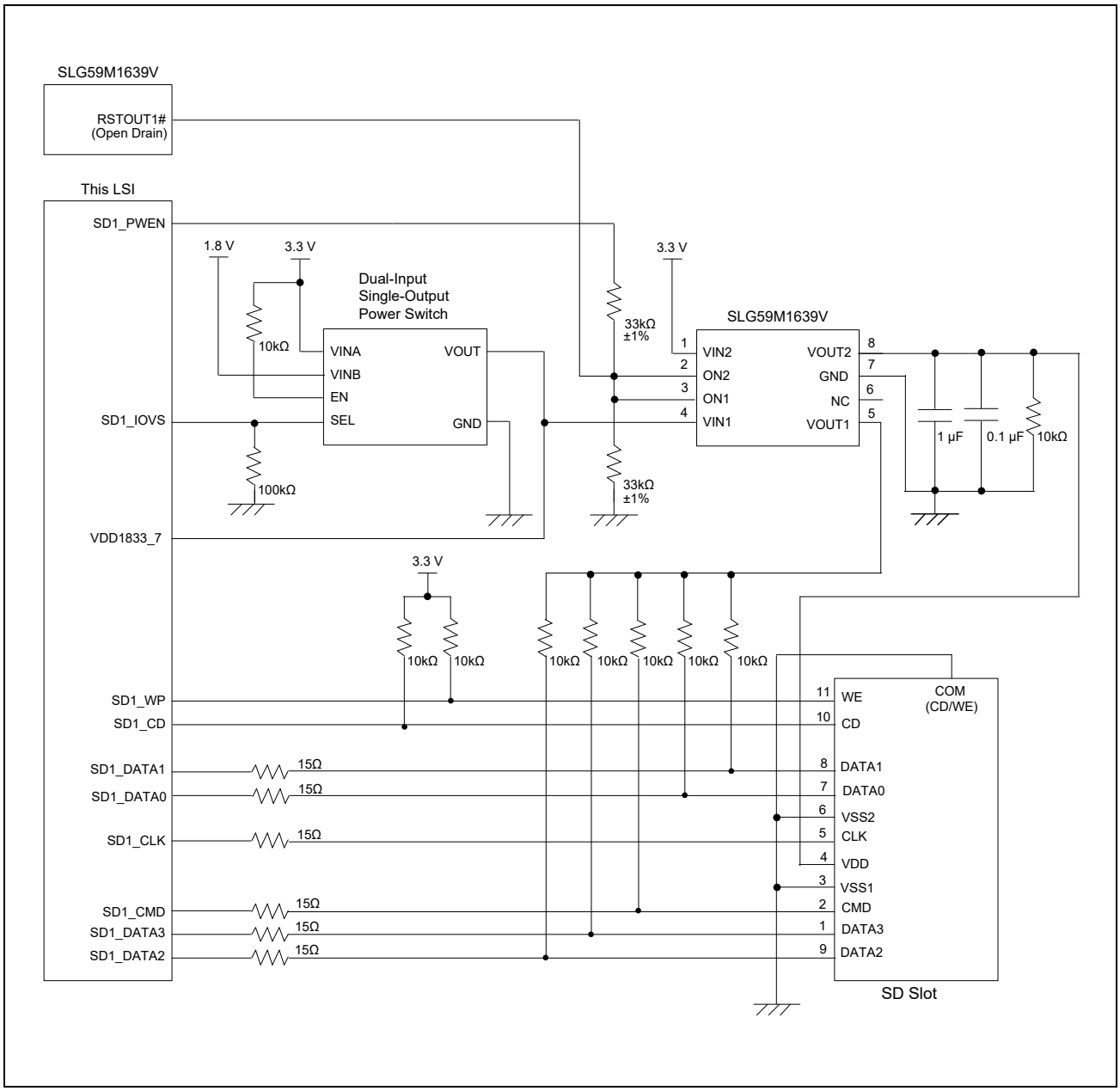

Figure 6.3 Connection Diagram of This LSI with SD Slot

7. PCIe

7.1 PCB Specifications and Layout

7.1.1 Thickness and Number of Layers of PCB

Boards without edge connectors can be designed with any number of layers or thickness, but with edges, the board must be designed with an overall thickness of 1.57 mm (0.062 inch).

7.1.2 Notes on PCB Layout

When wiring on the board, note the following:

- Place an AC coupling capacitor of 0.22 µF near the TX terminal.
- Wire the differential signals with equal length to avoid skew in the differential signals.
- It is recommended to design DP/DN wiring with differential impedance of TYP 100Ω (±5%) and single-end impedance of TYP 50Ω (±5%). It is also possible to design a differential impedance of TYP 85Ω (±5%) and a single-end impedance of TYP 42.5Ω (±5%).
- When using vias to trace differential signals, each differential signal must have the same number of vias. Avoid changing vias and layers for traces as much as possible.
- There are two types of test fixture CLB3 used in the compliance test: x4/x8 and x1/x16. Regarding PCIe® slot selection, 1 lane (only 1 lane supported) or 4 lanes is recommended.
- All unconnected lanes must be terminated during the compliance test.
- The PCIe standard assumes the insertion loss budget for PCB. Make the pattern wiring from the CPU to the PCIe slot or edge as short as possible to reduce the insertion loss.

7.1.3 Recommended Power Filter Configuration

Figure 7.1 shows the recommended filter configuration for the power supply.

To reduce the influence of noise, configure a filter for the power supply terminal. We recommend using ferrite beads (FB) between the board power supply and the PCIe power supply to avoid noise interference. Place the decoupling capacitor as close as possible to the power supply terminal.

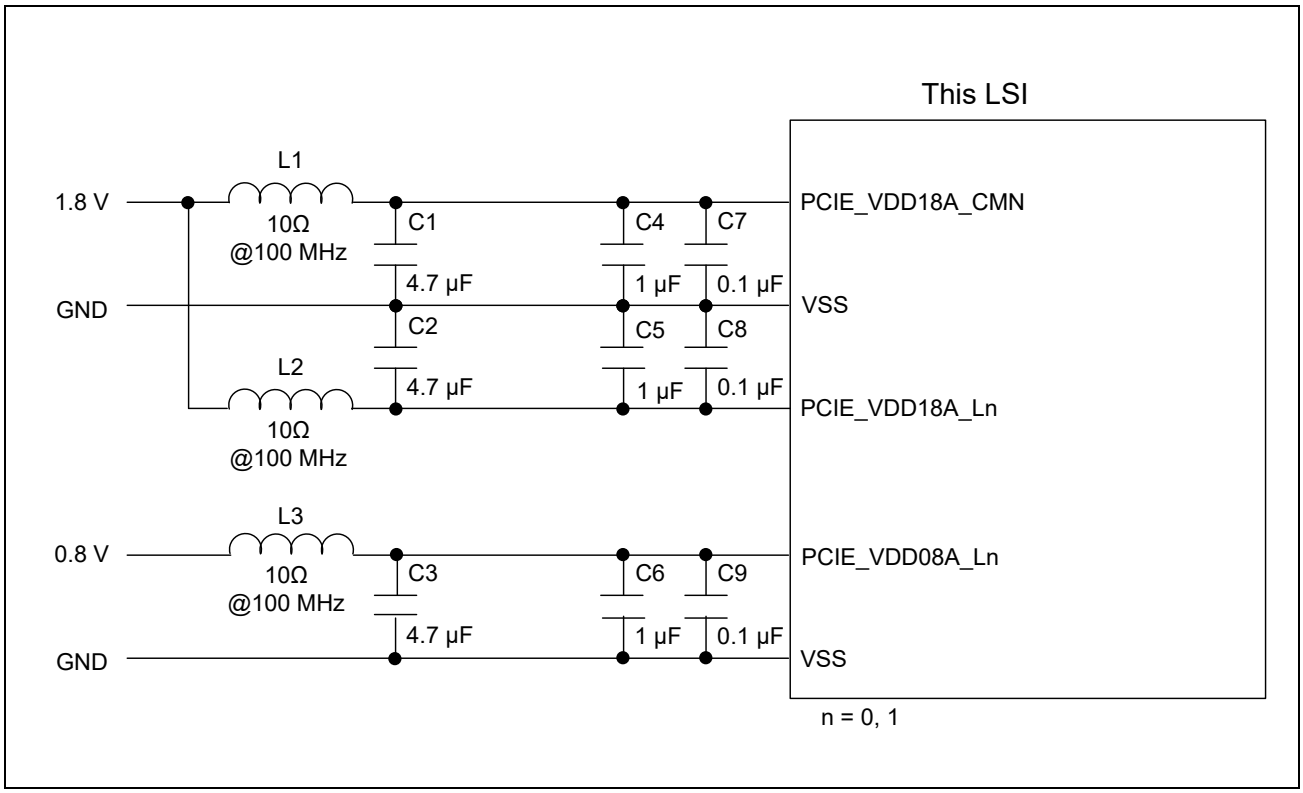

Figure 7.1 Recommended Power Filter Configuration for PCIe

Table 7.1 List of Recommended Components

Components	Type	Characteristic	Recommended Components
L1, L2, L3	Ferrite beads (FB)	10Ω@100 MHz	BLM15AX100SN1D
C1, C2, C3	Ceramic capacitor	4.7 µF ±10%	GRM188C71A475KE11D
C4, C5, C6	Ceramic capacitor	1.0 µF ±20%	GRM033D70G105ME01
C7, C8, C9	Ceramic capacitor	0.1 µF ±10%	GRM033C71A104KE14

7.2 Example Circuits

This section shows example PCIe circuits. The PERST# and WAKE# pins require pull-up resistors to be added on the system board for open-drain output. There is no VOH specification for these pins. The example circuits show example designs for DP/DN wiring with differential impedance of TYP 100Ω (±5%) and single-end impedance of TYP 50Ω (±5%).

7.2.1 Root Complex

Figure 7.2 shows an example circuit for the PCIe Root Complex. All PCI Express add-in card connectors require two power rails: +12V and +3.3V, with a third, optional 3.3Vaux rail.

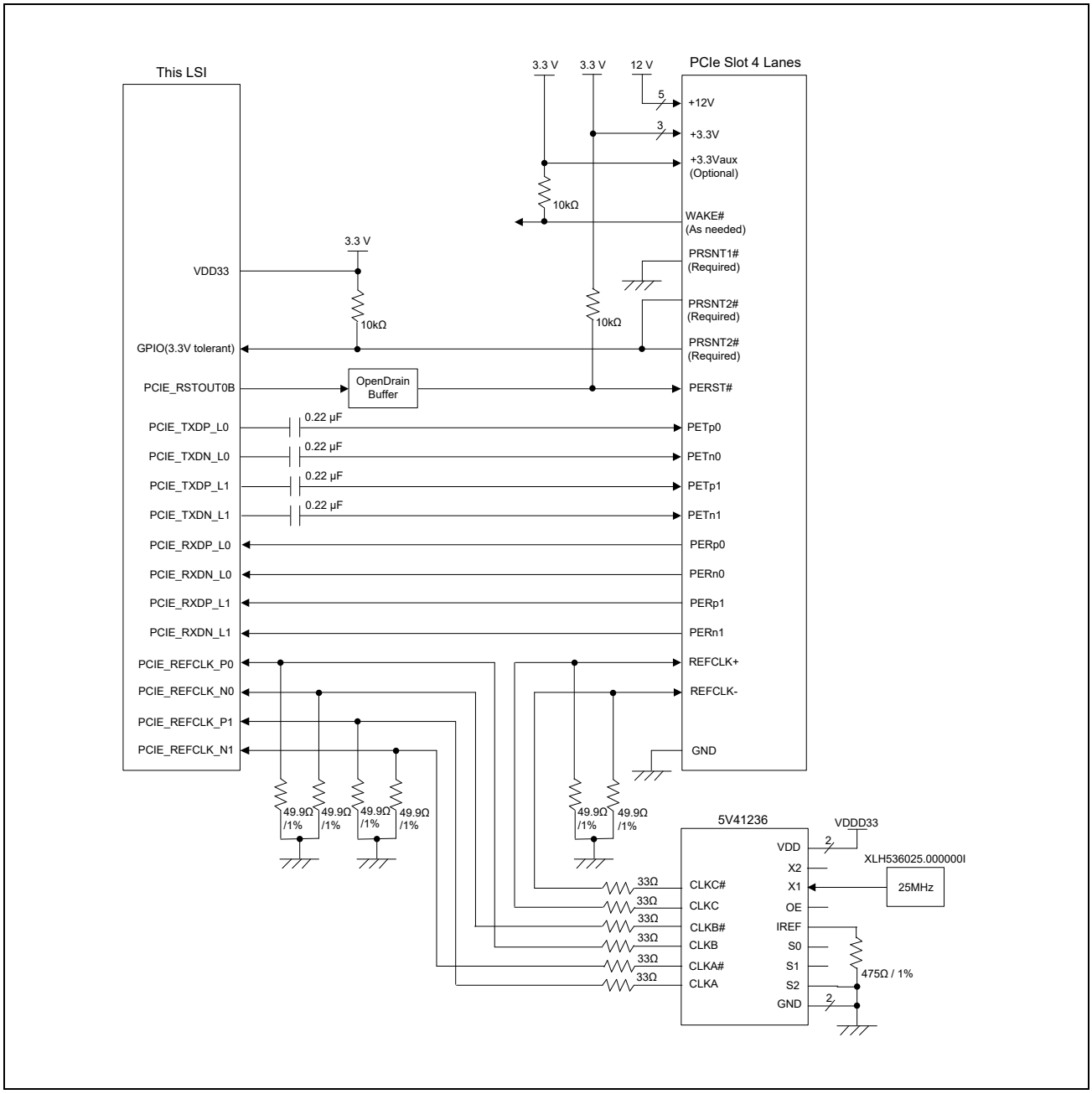

Figure 7.2 Example Circuit for PCIe Root Complex

7.2.2 End Point

Figure 7.3 shows an example circuit for the PCIe End Point.

The PRSNT1# signal should be connected to the farthest PRSNT2# signal with one trace. For example, when using a 4-lane connector, connect PRSNT1# of the A1 pin to PRSNT2# of the B31 pin.

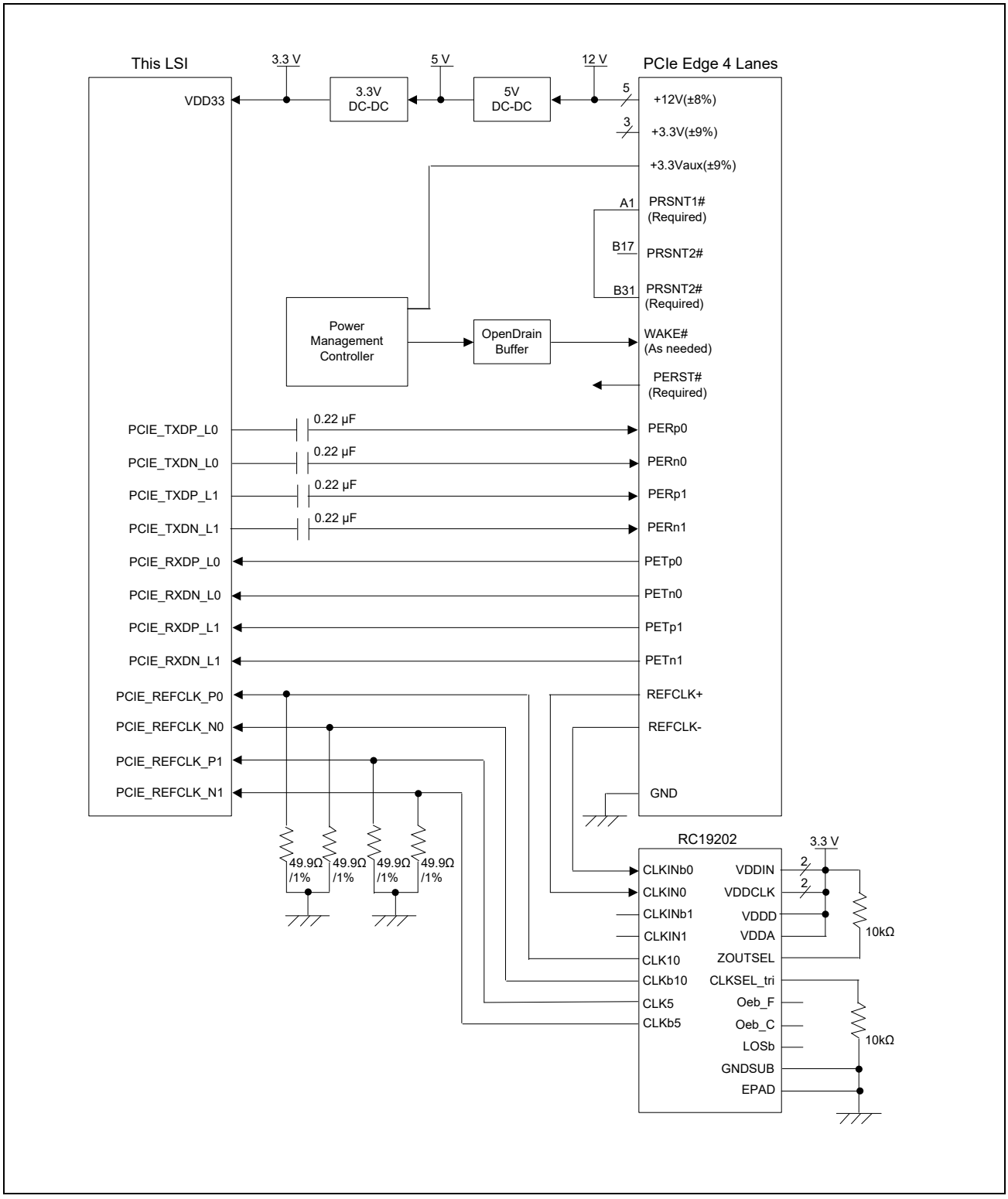

Figure 7.3 Example Circuit for PCIe End Point

8. LPDDR4

The following documents apply to LPDDR4 for this LSI. Make sure to refer to the latest versions of these documents. Last four digits of document number (described as ****) indicate version information of each document. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Table 8.1 List of LPDDR4 Documents

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, peripheral function specifications, electrical characteristics, timing charts) and operation description	RZ/T2H and RZ/N2H Group User's Manual: Hardware	R01UH1039EJ****
Application Note	PCB verification guide for LPDDR4	RZ/T2H and RZ/N2H Group PCB Verification Guide for LPDDR4	R01AN7260EJ****
Application Note	PCB design guide for LPDDR4	RZ/T2H and RZ/N2H Group PCB Design Guideline for LPDDR4	R01AN7268EJ****

9. USB2.0

9.1 Notes on PCB Layout

When wiring on the print circuit board, note the following:

- Separate digital power planes from analog power planes.
- Decoupling capacitors are required for all power supplies. Place a small capacitor (0.1 to 2.2 µF) around the chip and a large capacitor (10 to 47 µF) on the regulator side.
- The total value of L/C/R must be no greater than the value below.
  - Inductance: 4 nH or less
  - Capacitance: 5 pF or less
  - Resistance: 1Ω or less
- When each power supply (USB_USVDD33, USB_USVDD18, USB_USDVDD) is shared with other power supplies, use ferrite beads to separate the power supplies.
- Place the external resistors of USB_VUBUSIN and USB_TXRTUNE near the respective pins.
- Separate signals that generate noise (such as clocks) from USB_TXRTUNE or shield them with ground. (No crossing allowed)
- Do not place capacitors in parallel with external resistors of USB_TXRTUNE.
- The lower layer of the external resistors of USB_TXRTUNE and wiring must be a GND plane.
- It is recommended to design the DP/DM wiring with differential impedance of TYP 90Ω (±10%) and single-end impedance of TYP 45Ω (±10%). Give priority to the differential impedance in terms of characteristics.
- Keep the wiring for USB DP/DM between this LSI and connector short. The USB specification defines that the delay must be no more than 3 ns for the function and hub downstream, and no more than 1 ns for the host and hub upstream. Note that the delay value per length differs with the quality of the material of PCB.
- The DP/DM wiring must be of equal length and width, run parallel, and be on the same layer (the target value for the difference in wiring length: up to 1 mm).
- Do not cross the DP/DM wiring with the writing for other signals. When crossing, insert the digital power plane or GND plane between them.
- To prevent noise intrusion, minimize bends and through-holes for the USB DP/DM wiring, and use a GND plane for the lower layer of the DP/DM wiring (the number of vias must be the same, and it is recommended to avoid changing vias and layers as much as possible and to use the top or bottom layer).
- Isolate the USB DP/DM wiring from other signal wiring. Take particular care with signals that are subject to sharp changes, such as clocks and data buses.
- Shield GND on both sides of the DP/DM wiring.
- Place GND return vias adjacent to DP/DM vias.
- The return path must be continuous with GND.

9.2 Recommended Power Filter Configuration

Figure 9.1 shows the recommended filter configuration for the power supply. To reduce the influence of noise, configure a filter for the power supply terminal.

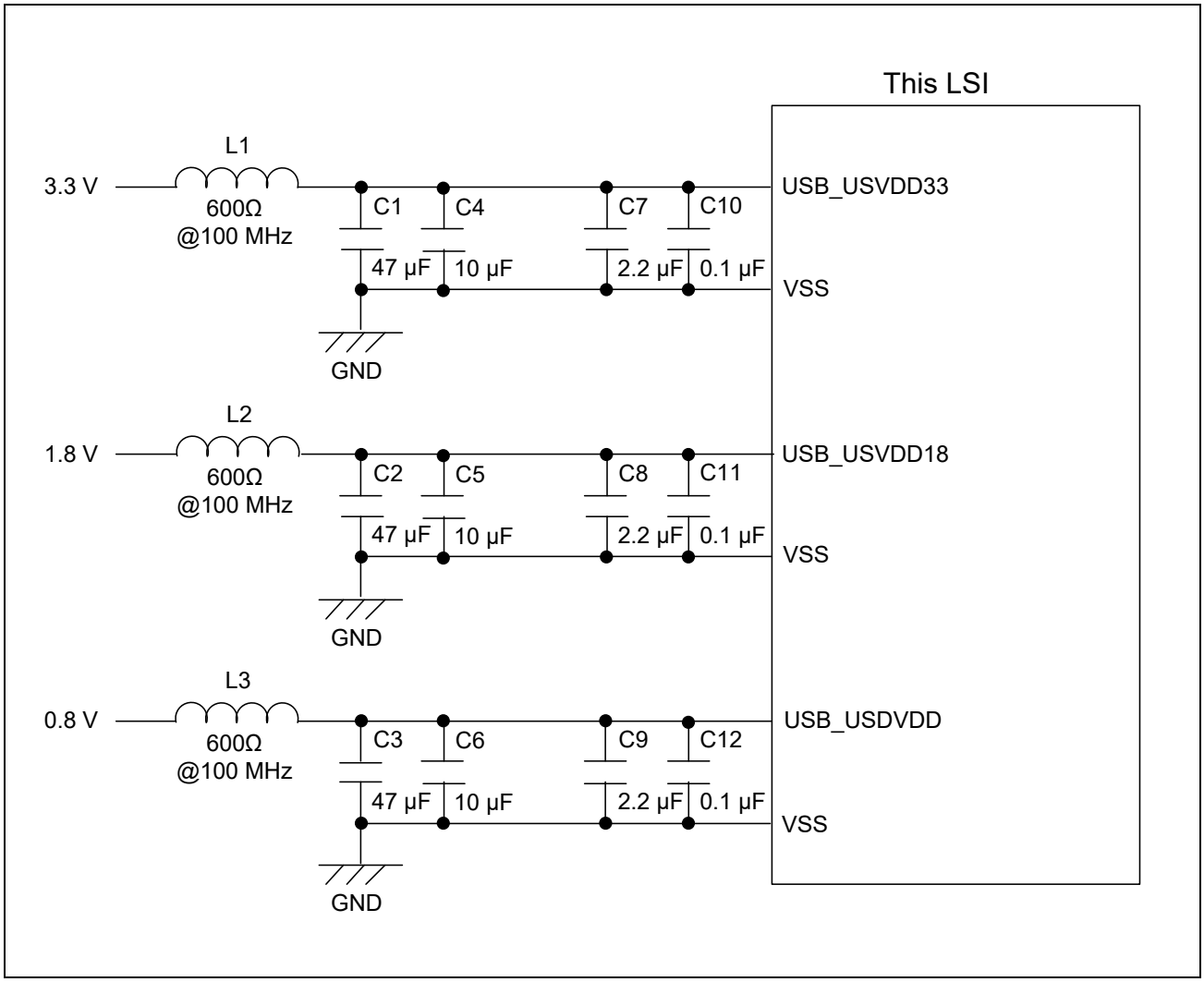

Figure 9.1 USB2.0 Recommended Filter Configuration

Table 9.1 List of USB2.0 Recommended Components

Components	Type	Characteristic	Recommended Components
L1, L2, L3	Ferrite beads (FB)	600Ω@100 MHz	BLM15AX601SZ1D
C1, C2, C3	Ceramic capacitor	47 µF	GRM32ER71A476ME15L
C4, C5, C6	Ceramic capacitor	10 µF	GRM188D71A106MA73D
C7, C8, C9	Ceramic capacitor	2.2 µF	GRM155Z71A225KE44D
C10, C11, C12	Ceramic capacitor	0.1 µF	GRM033C71A104KE14

9.3 Example Circuits

This section shows example USB circuits. Since an overshoot may occur on the VBUS line due to a mismatch in impedance when the USB cable is connected, add a TVS diode or similar to protect the USB_VBUSIN port. Also, protect the DM and DP signals with the TVS diode, etc.

9.3.1 Host Controller Circuit Example

Figure 9.2 shows an example circuit for supporting the host controller. When used as the host controller, it is necessary to supply VBUS power to the function device. To control the VBUS power supply, we recommend using a USB port power controller IC with an overcurrent limiting function, such as the ISL6186 manufactured by Renesas Electronics. Design the VBUS line so that its additional capacitance is 120 µF or more. (In this circuit example, it is set to 150 µF.) Also, in the following example, design the power domain of USB_VBUSEN to be 3.3 V. The rising threshold voltage of the EN pin of the ISL6186 must be sufficient. Add a pull-up resistor according to the power domain voltage of USB_OVRCUR.

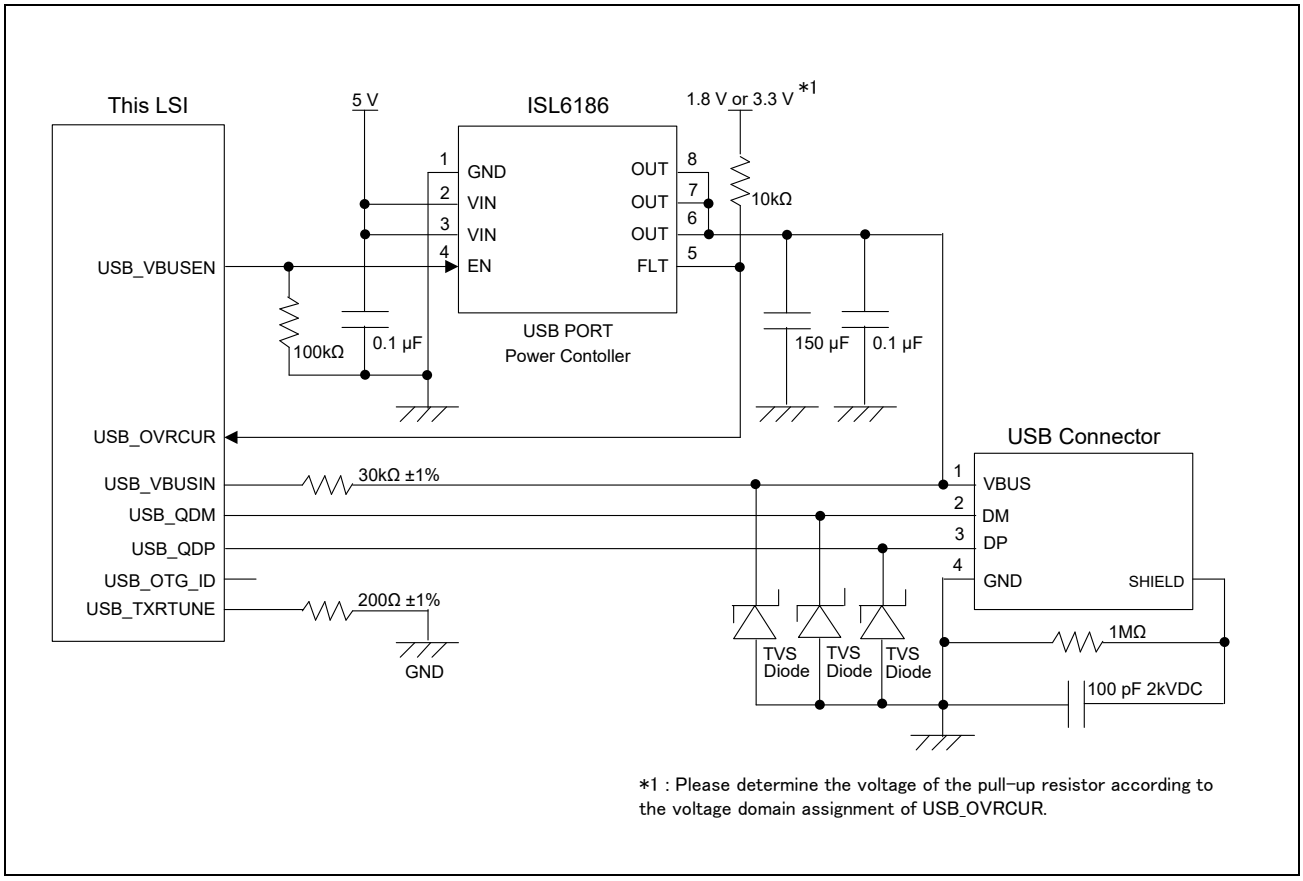

Figure 9.2 Host Controller Circuit Example

9.3.2 Function Controller Circuit Example

Figure 9.3 shows an example circuit for supporting the function controller.

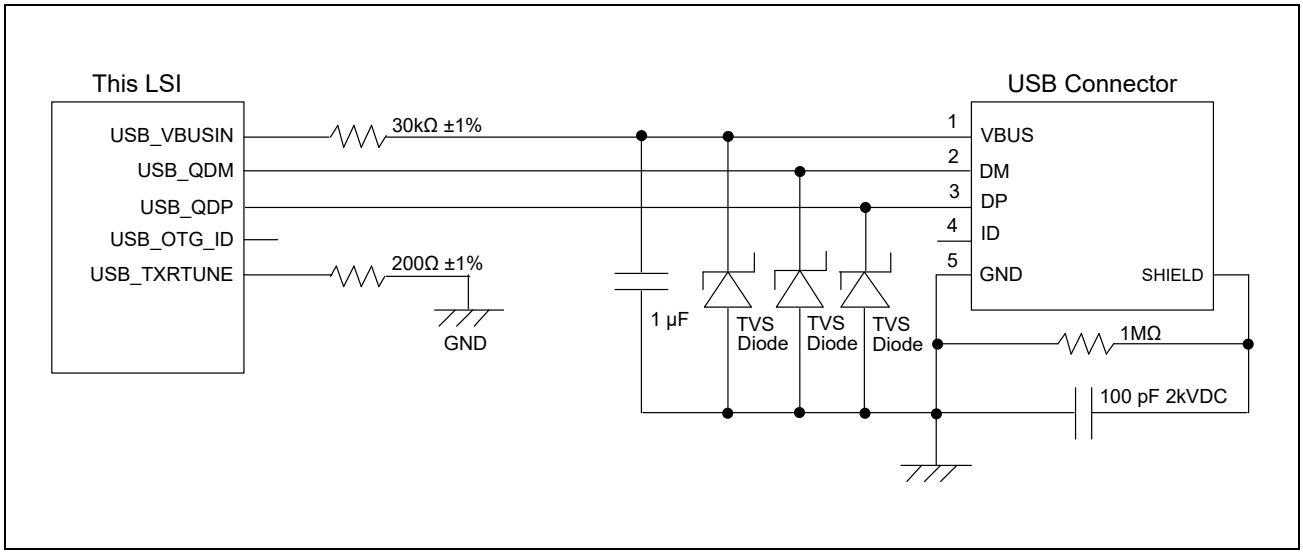

Figure 9.3 Function Controller Circuit Example

9.3.3 OTG System Circuit Example

Figure 9.4 shows an example circuit for supporting the OTG system. This configuration is an example using an external OTG transceiver. When OFFVBUS# is set to low, the charge pump of VBUS and the USB OTG transceiver is disabled. For normal VBUS operation, set OFFVBUS to low. When SHDN is set to low, the USB OTG transceiver enters shutdown mode. In shutdown mode, the charge pump and comparator of the USB OTG transceiver are disabled.

- Design the VBUS line so that its additional capacitance is 120 µF or more. (In this circuit example, it is set to 150 µF.)
- In this example circuit, design the power domains of USB_VBUSEN, USB_EXICEN, and USB_OVRCUR so that they are set to 3.3 V.

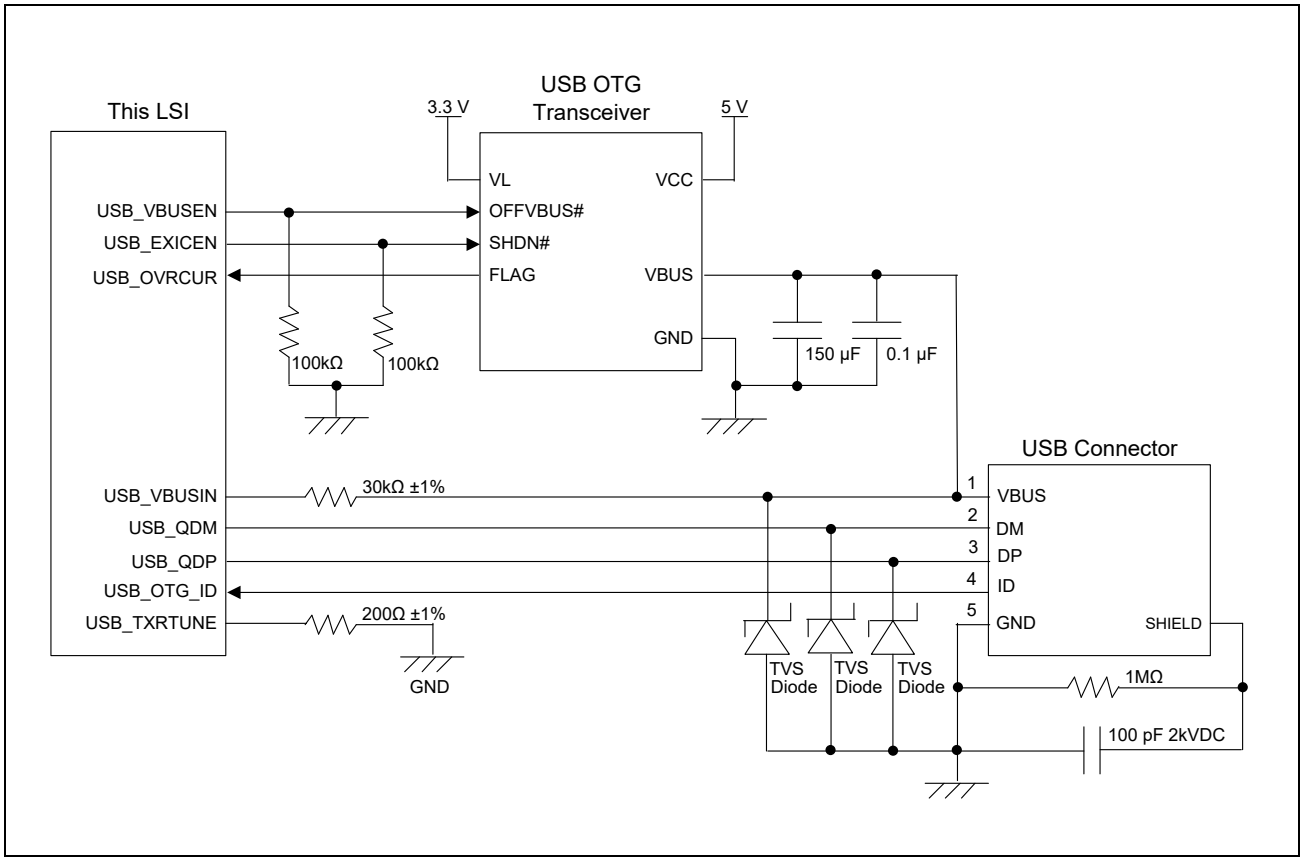

Figure 9.4 OTG System Circuit Example

10. ADC

10.1 Notes on PCB Layout

When wiring on the board, note the following:

- Decoupling capacitors are required for all power supplies. Place a small capacitor (0.1 to 2.2 µF) around the chip and a large capacitor (10 to 47 µF) on the regulator side.
- When each power supply (AVDDIO_ADCn, AVDDREF_ADCnD) is shared with other power supplies, use ferrite beads to separate the power supplies.
- It is highly recommended to shield the input signals to AN200 to AN214 with AVSSIO_ADCn on the PCB.
- Do not cross AN200 to AN214 or run parallel to high-speed signals such as digital signals or clock inputs.

10.2 Recommended Power Filter Configuration

Figure 10.1 shows the recommended filter configuration for the power supply. To reduce the influence of noise, configure a filter for the power supply terminal.

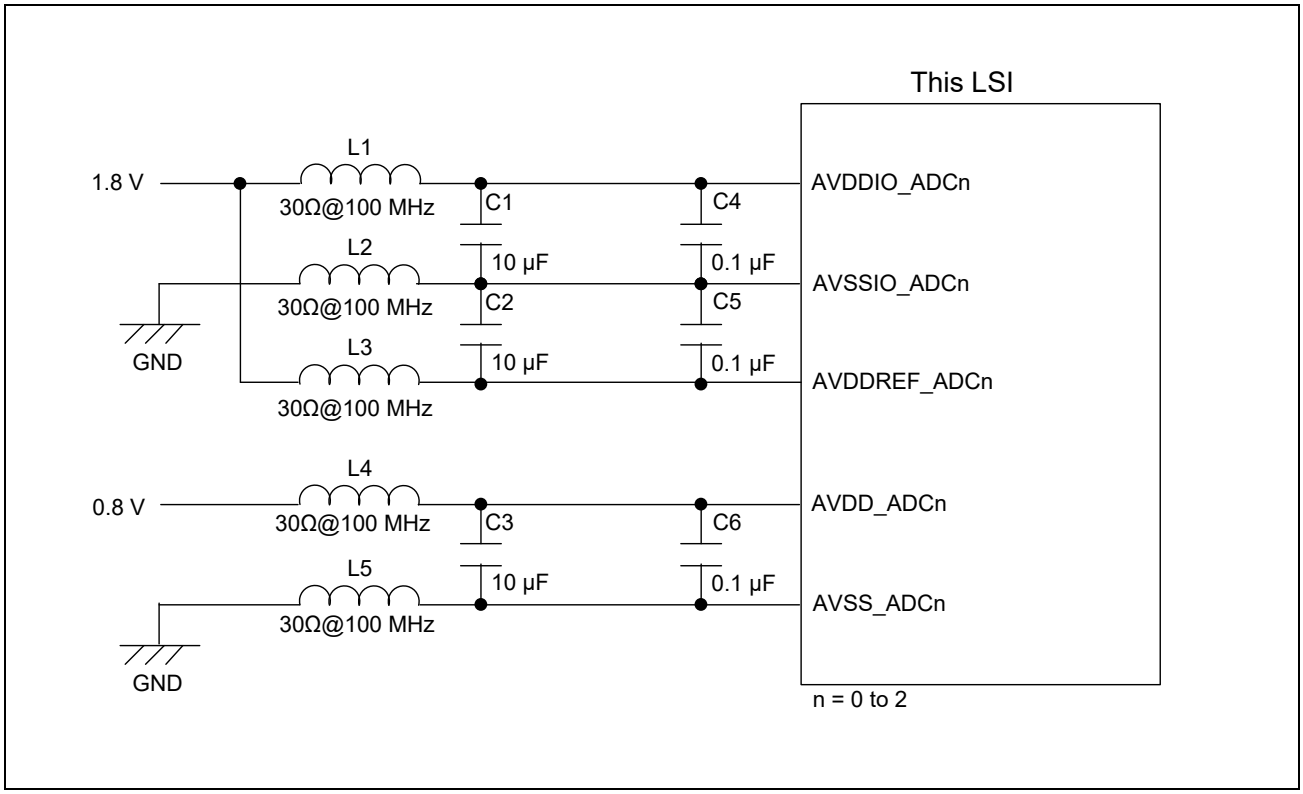

Figure 10.1 ADC Recommended Filter Configuration

Table 10.1 List of ADC Recommended Components

Components	Type	Characteristic	Recommended Components
L1, L2, L3	Ferrite beads (FB)	30Ω@100 MHz	BLM15AX300SZ1
C1, C2, C3	Ceramic capacitor	10 µF	GRM188D71A106MA73D
C4, C5, C6	Ceramic capacitor	0.1 µF	GRM033C71A104KE14

11. PLL

11.1 Notes on PCB Layout

When wiring on the board, note the following:

- Decoupling capacitors are required for all power supplies. Place a small capacitor (0.1 to 2.2 µF) around the chip and a large capacitor (10 to 47 µF) on the regulator side.
- When each power supply (VDD18_PLLn, VDD08_PLLn) is shared with other power supplies, use ferrite beads to separate the power supplies.

11.2 Recommended Power Filter Configuration

Figure 11.1 shows the recommended filter configuration for the power supply. To reduce the influence of noise, configure a filter for the power supply terminal.

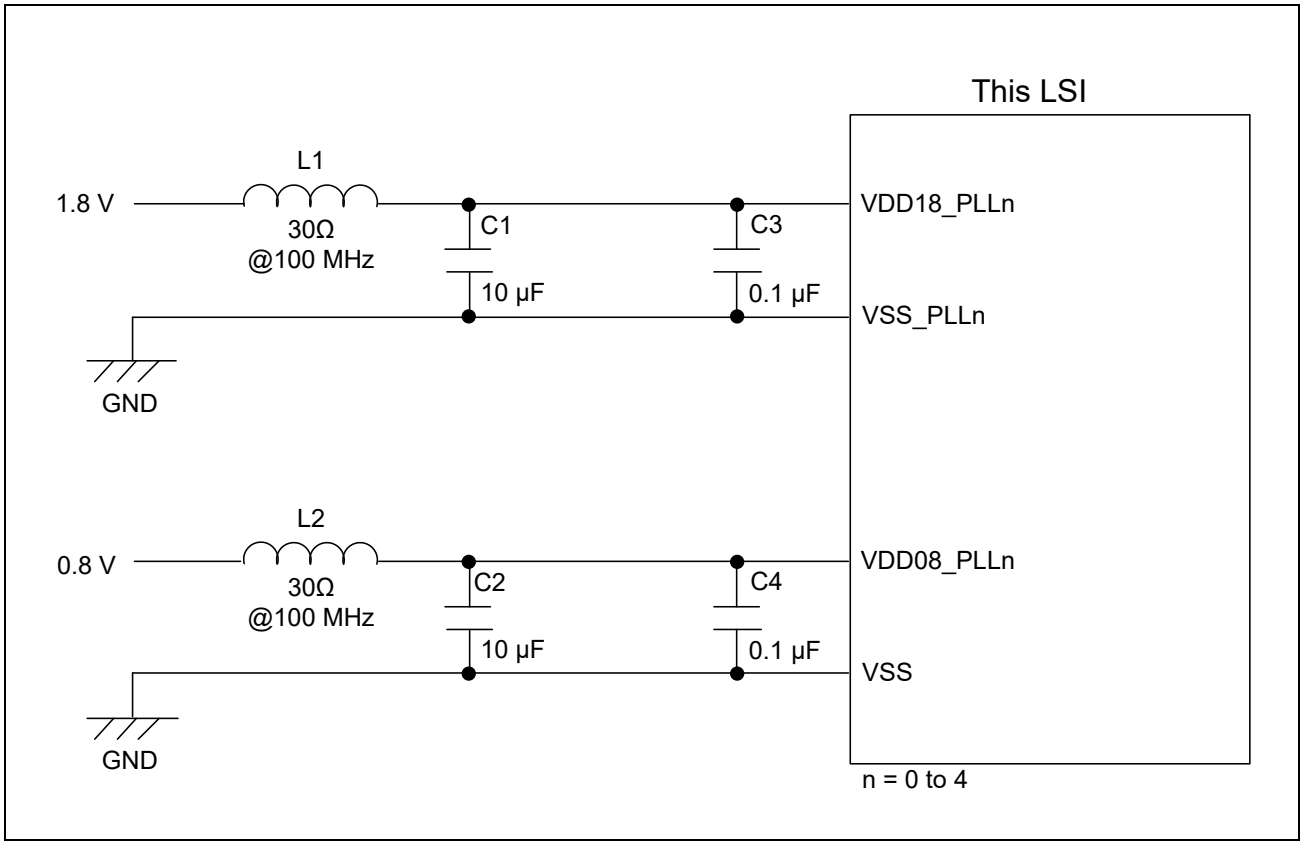

Figure 11.1 PLL Recommended Filter Configuration

Table 11.1 List of PLL Recommended Components

Components	Type	Characteristic	Recommended Components
L1, L2	Ferrite beads (FB)	30Ω@100 MHz	BLM15AX300SZ1
C1, C2	Ceramic capacitor	10 µF	GRM188D71A106MA73D
C3, C4	Ceramic capacitor	0.1 µF	GRM033C71A104KE14

12. OTP

12.1 Notes on PCB Layout

When wiring on the board, note the following:

- Decoupling capacitors are required for all power supplies. Place a small capacitor (0.1 to 2.2 µF) around the chip and a large capacitor (10 to 47 µF) on the regulator side.

12.2 Recommended Power Filter Configuration

Figure 12.1 shows the recommended filter configuration for the power supply.

To reduce the influence of noise, configure a filter for the power supply terminal.

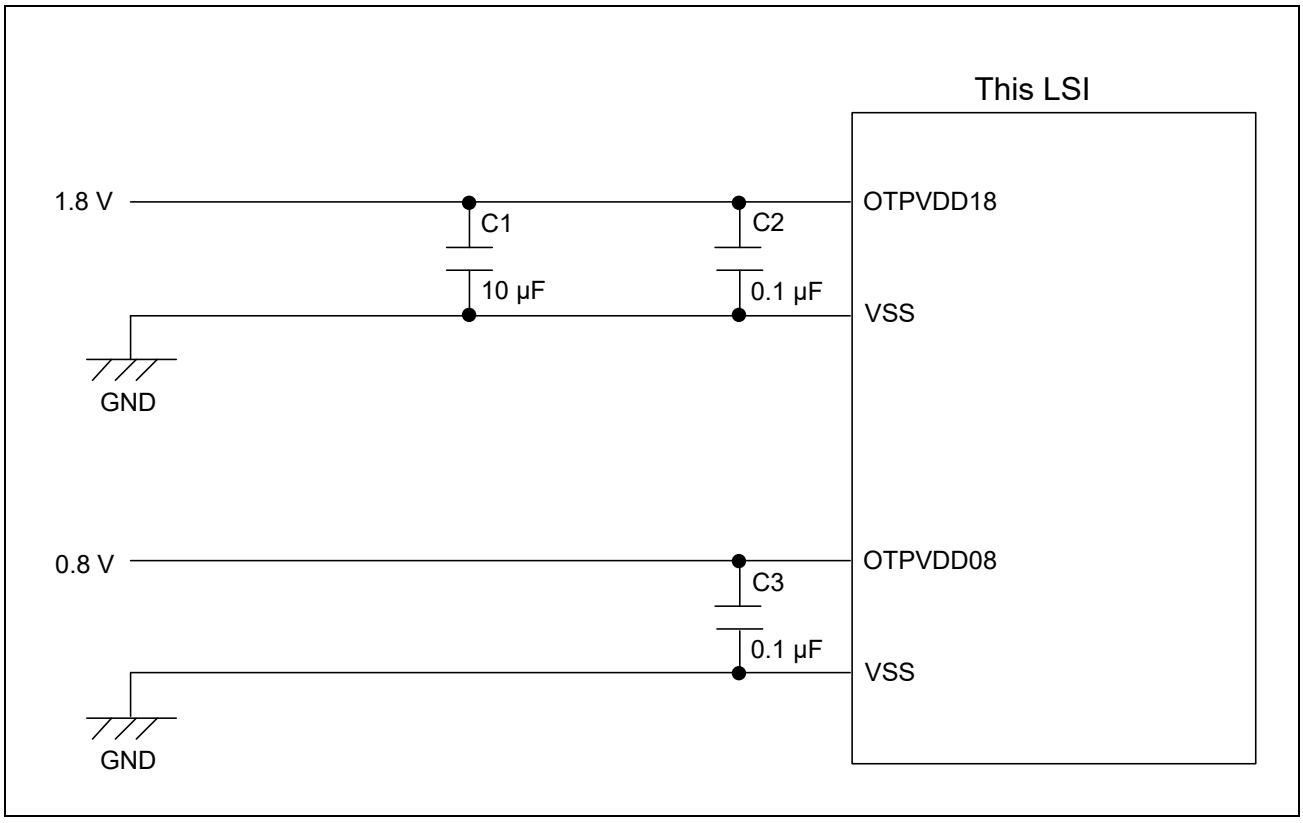

Figure 12.1 OTP Recommended Filter Configuration

Table 12.1 List of OTP Recommended Components

Components	Type	Characteristic	Recommended Components
C1	Ceramic capacitor	10 µF	GRM188D71A106MA73D
C2, C3	Ceramic capacitor	0.1 µF	GRM033C71A104KE14

13. TSU

13.1 Notes on PCB Layout

When wiring on the board, note the following:

- Decoupling capacitors are required for all power supplies. Place a small capacitor (0.1 to 2.2 µF) around the chip and a large capacitor (10 to 47 µF) on the regulator side.
- The total value of L/R of the board power supply wiring (AVDD18A_TSU, DVDD08A_TSU) must be no greater than the value below.
  - Inductance: 3 nH or less
  - Resistance: 300mΩ or less

13.2 Recommended Power Filter Configuration

Figure 13.1 shows the recommended filter configuration for the power supply.

To reduce the influence of noise, configure a filter for the power supply terminal.

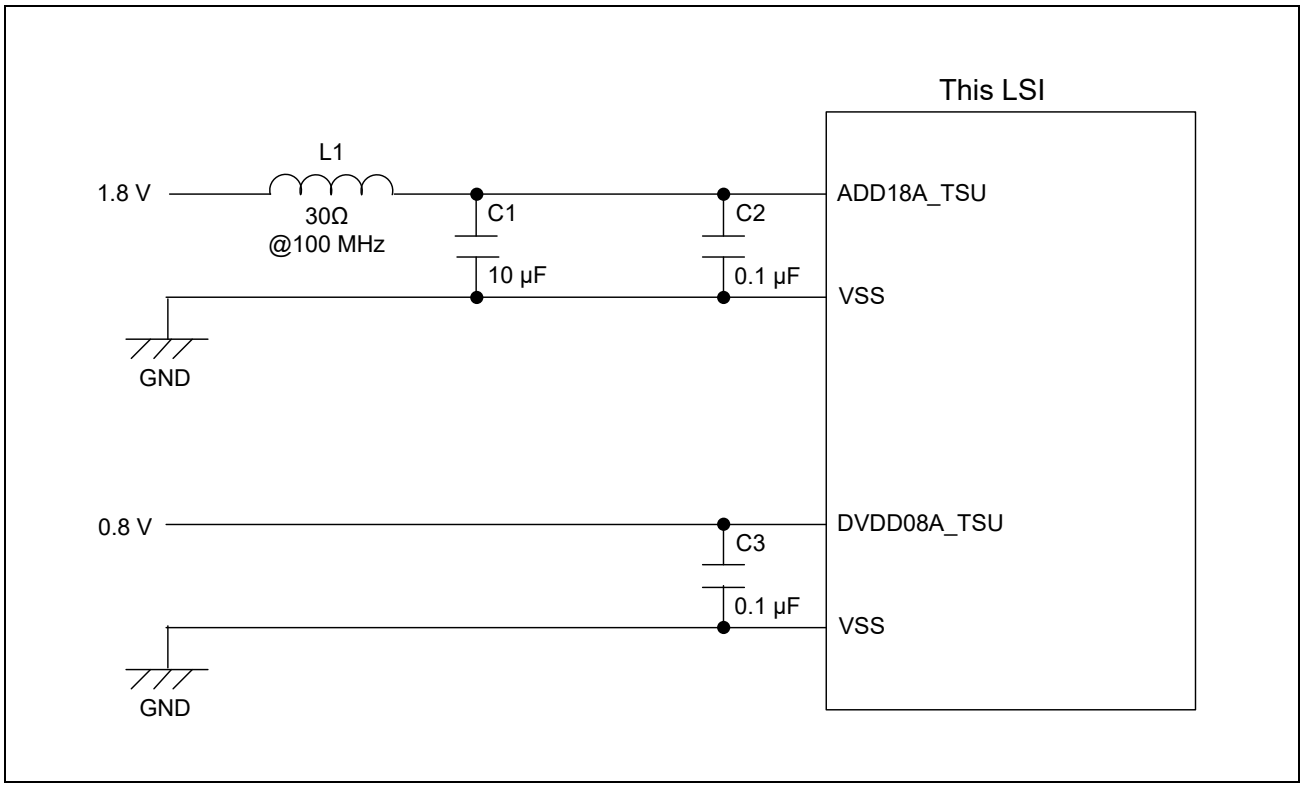

Figure 13.1 TSU Recommended Filter Configuration

Table 13.1 List of TSU Recommended Components

Components	Type	Characteristic	Recommended Components
L1	Ferrite beads (FB)	30Ω@100 MHz	BLM15AX300SZ1D
C1	Ceramic capacitor	10 µF	GRM188D71A106MA73D
C2, C3	Ceramic capacitor	0.1 µF	GRM033C71A104KE14

14. Handling of Unused Pins

Note the following regarding the handling of unused pins. The details on the handling of unused pins are given in **Table 14.1**.

- Connect the dedicated power supply pins of unused modules to the power supply as well.

Table 14.1 Handling of Unused Pins

Item	Pin Name	Handling
Clock	XTAL	Keep this pin open when an external clock signal is used.
	EXTAL	Connect this pin to VSS via a resistor (pulling down) when an external clock signal is used.
	EXTCLKIN	Connect this pin to VSS via a resistor (pulling down) when a crystal resonator is connected.
Debug	TRST#	Connect these pins to VSS via a resistor (pulling down), or input the same signal as that on the RES# pin.
	TCK (P08_3)	Connect this pin to VSS via a resistor (pulling down).
	TMS (P08_1)	Connect this pin to VDD33 via a resistor (pulling up).
	TDI (P08_2)	Connect this pin to VDD33 via a resistor (pulling up).
	TDO (P08_4)	Keep this pin open.
System	RSTOUT# (P08_5)	Keep this pin open.
	MDX*3	Connect this pin to VSS via a resistor (pulling down).
	BSCANP	Connect this pin to VSS via a resistor (pulling down).
ADC12*1	AN000 to AN003, AN100 to AN103, AN200 to AN214	Keep these pins open.
	AVDDREF_ADC0	Connect this pin to AVDDIO_ADC0.
	AVDDREF_ADC1	Connect this pin to AVDDIO_ADC1.
	AVDDREF_ADC2	Connect this pin to AVDDIO_ADC2.
USB*1	USB_QDP, USB_QDM, USB_OTG_ID	Keep these pins open.
	USB_VUBUSIN, USB_TXRTUNE	Connect these pins to VSS via a resistor (pulling down) or keep these pins open.
PCIE*1	PCIE_REFCLK_P0, PCIE_REFCLK_N0, PCIE_REFCLK_P1, PCIE_REFCLK_N1, PCIE_RXDP_L0, PCIE_RXDN_L0, PCIE_RXDP_L1, PCIE_RXDN_L1, PCIE_TXDP_L0, PCIE_TXDN_L0, PCIE_TXDP_L1, PCIE_TXDN_L1	Keep these pins open.
DDRSS*1	DDR_ZN	Connect this pin to DDR_VDDQ.
	DDR_DTEST, DDR_ATEST, DDR_RESET_N, DDR_CKA_T, DDR_CKA_C, DDR_CKB_T, DDR_CKB_C, DDR_CKEA[1:0], DDR_CKEB[1:0], DDR_CSA[1:0], DDR_CSB[1:0], DDR_CAA[5:0], DDR_CAB[5:0], DDR_DQA[15:0], DDR_DQB[15:0], DDR_DMIA[1:0], DDR_DMIB[1:0], DDR_DQSA_T[1:0], DDR_DQSB_T[1:0], DDR_DQSA_C[1:0], DDR_DQSB_C[1:0]	Keep these pins open.
Other	Other pins*2	Keep these pins open, connect them to VDD33 via a resistor (pulling up), or connect them to VSS via a resistor (pulling down).

Note 1. Set the module to the standby or low power mode. The module is placed in this state after reset release. Do not change the state of the module.

Note 2. When handling them as unused pins, set the corresponding bits of Port m Mode Register (PMm: m = 00 to 35) to “Non-use (Hi-Z input protection)” which is the value after reset release.

Note 3. Always use unused processing for MDX.

15. Other Bypass Capacitors

15.1 Bypass Capacitors for I/O Power

- For VDD1833_n (n = 0 to 7), place a bypass capacitor of about 0.1 µF for each two VDD1833_n balls as close to the LSI as possible.
- For VDD33, place a bypass capacitor of about 0.1 µF for each two balls as close to the LSI as possible.

15.2 Bypass Capacitors for Core Power

For the core power supply VDD08, place a bypass capacitor so that the target impedance in **Figure 15.2** is satisfied for the LSI model in **Table 15.1** and the topology in **Figure 15.1**.

Table 15.2 shows an example of recommended bypass capacitors for VDD08. Place capacitors at the bottom of the package with priority given to smaller capacitance.

Table 15.1 LSI Model

	Cchip [nF]	Rpkg [mΩ]	Lpkg [nH]
VDD08 (RZ/N2H)	174.49	0.613	0.0335
VDD08 (RZ/T2H)	174.49	0.515	0.0281

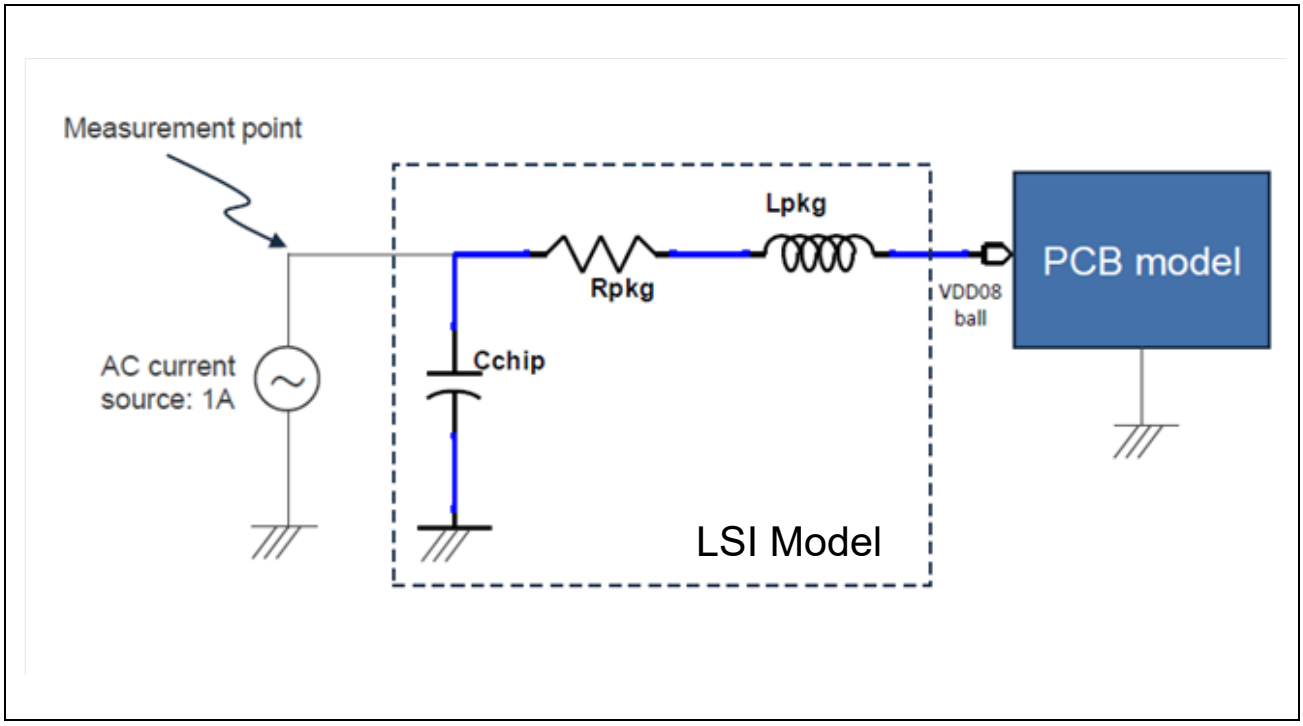

Figure 15.1 Topology

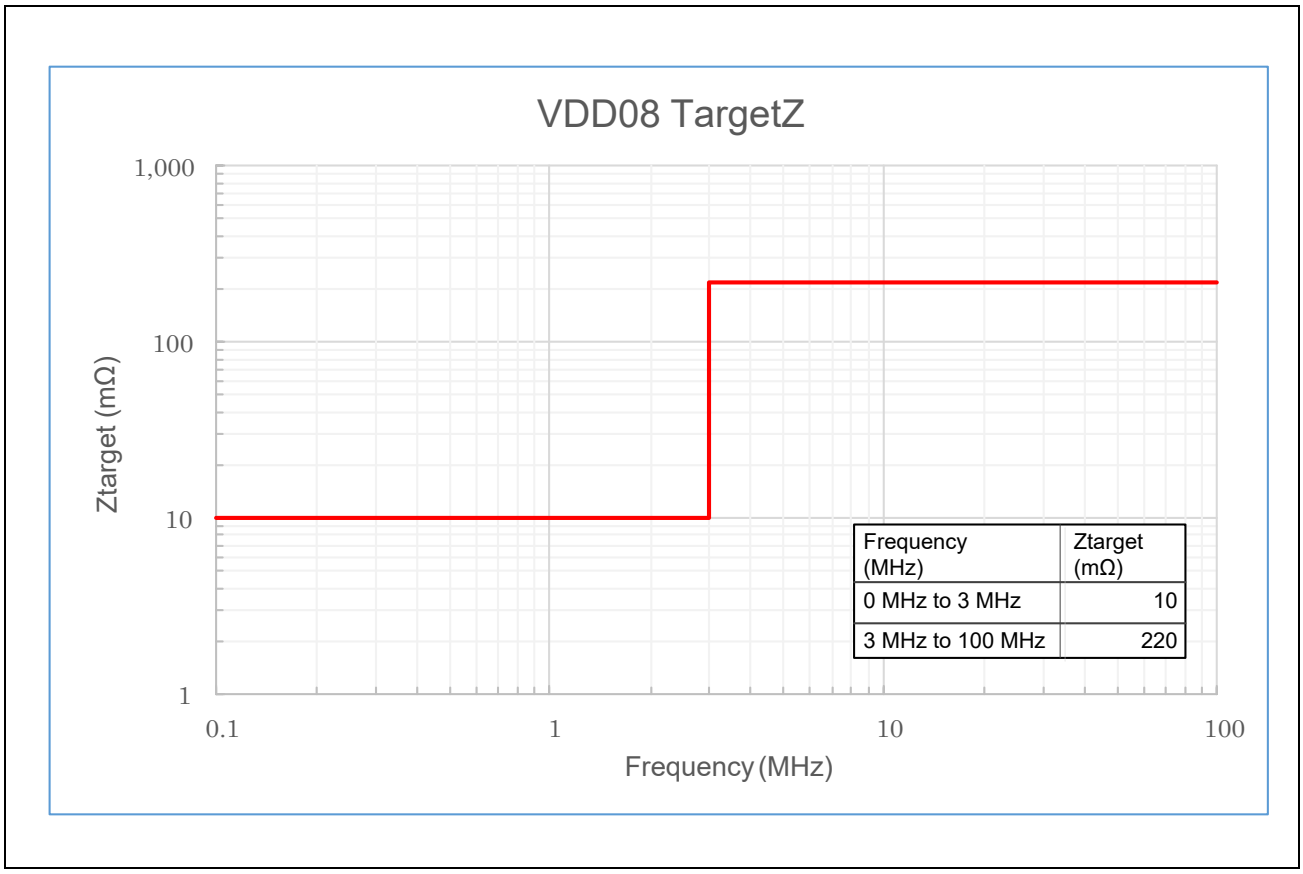

Figure 15.2 VDD08 Target Impedance

Table 15.2 VDD08 Reference Bypass Capacitor Recommendation Example

Characteristic	Quantity
6800 pF	1
0.01 µF	6
0.1 µF	5

REVISION HISTORY	RZ/T2H and RZ/N2H Group Hardware Design Guide

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 08, 2024	—	First edition issued
1.10	Oct. 31, 2025	10	Changed "Chapter 1.2.2 Example of a Power Supply Circuit Using PMIC

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

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