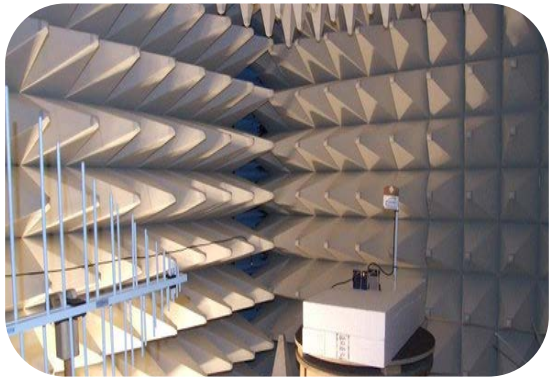
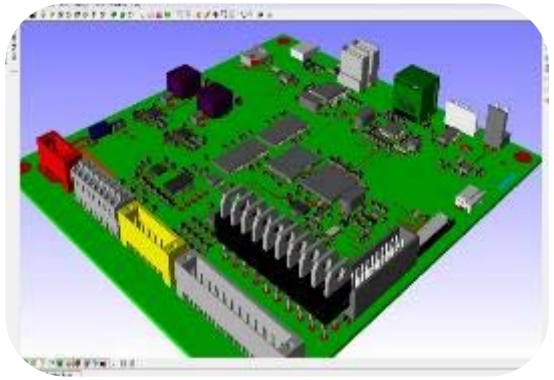
HOW COULD YOU AVOID FAILURES DURING EMC TESTS?

DISCOVER HOW RX23T MCU ADDRESS IT

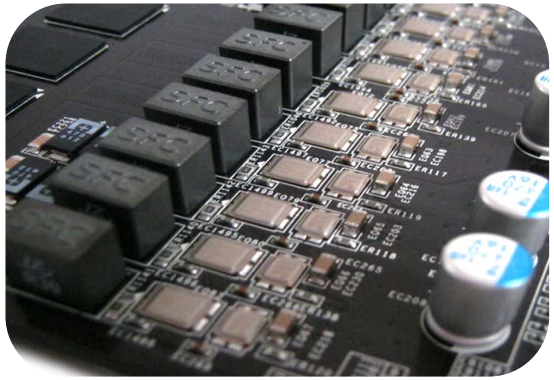
WHAT ARE THE COSTS IMPACTS OF FAILED EMC TESTS?



€ 300/hour for tests in anechoic chamber, high learning curve



For each iteration: PCB layout re-design, simulation, add PCB layers…



Components count & PCB cost due to ferrites, chokes, noise-cancelling ICs, etc.

Deadline missed, project overdue, product launch delay, ESD level too weak…

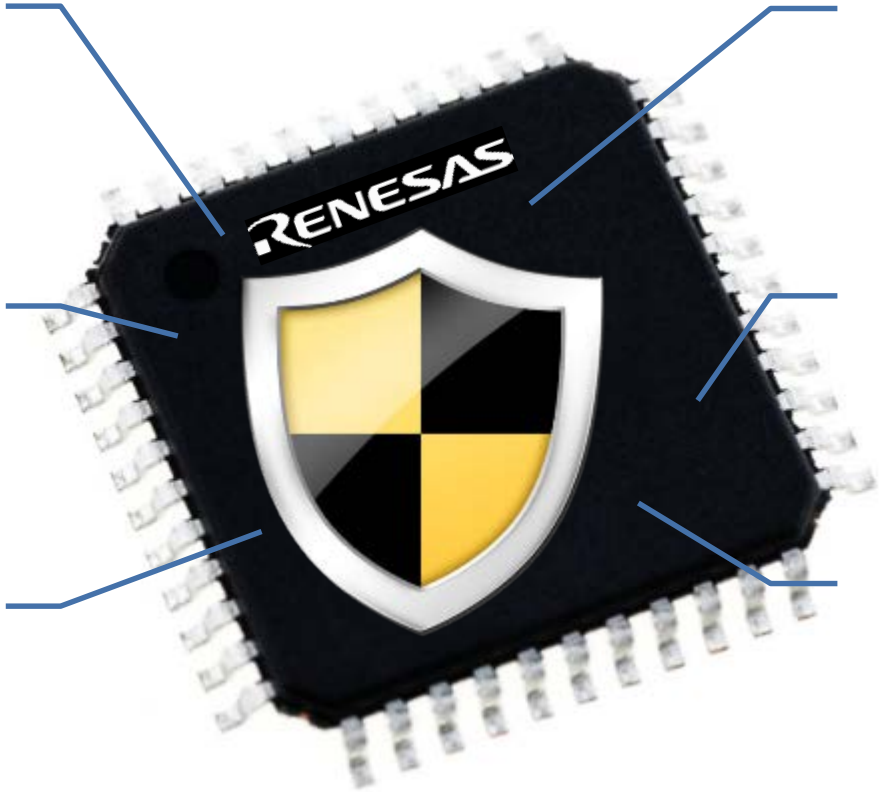
Cost Impact

RENESAS COMMITTED TO DESIGN SUPERIOR EMC MCUS

Clocks design optimized to remove any overshoots

Output buffers shaped to eliminate high current spikes

Innovative chip layout to ensure high noise absorption

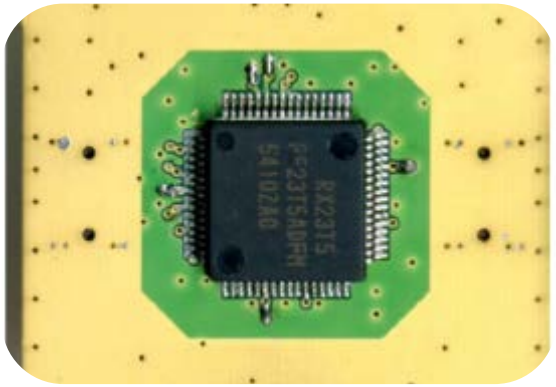


Optimal pin arrangement to minimize noise effects

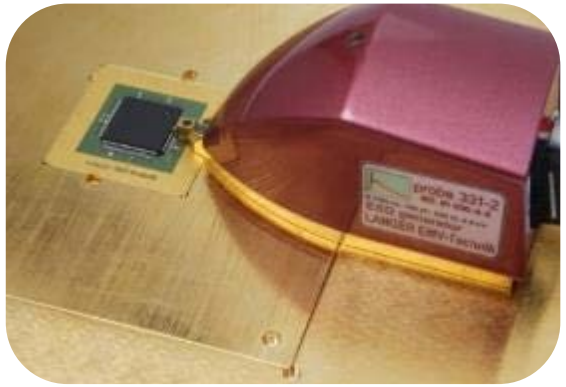
Separate Power and Ground paths to avoid mixing noise

Tough input pins protection to filter high frequency noise

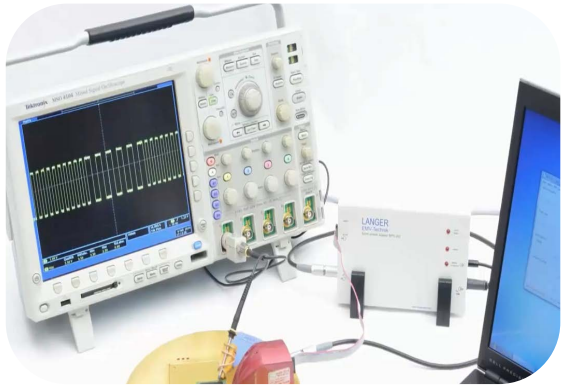
WHAT WAS DONE BY THE INDEPENDENT TESTING LAB?



Prepare RX23T samples on PCB with Self-test software running on the MCU



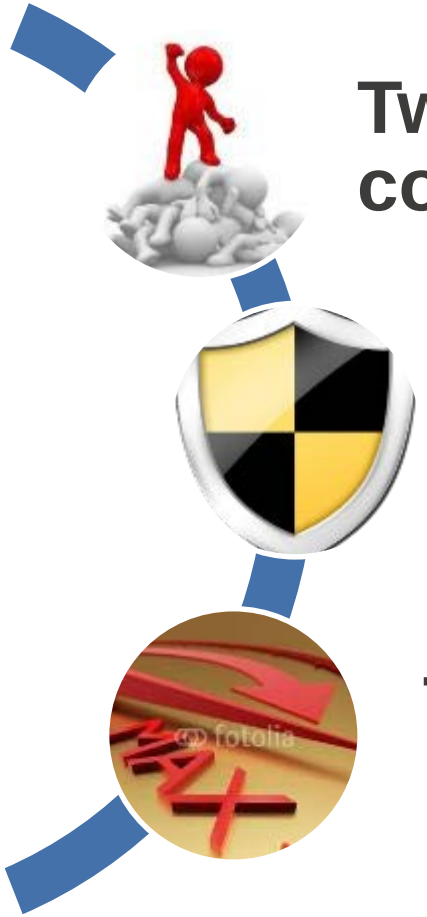
Apply voltages bursts on each pin until the MCU stops working and generates a Fault



Langer EMV lab tested the 64 pins of RX23T by applying disturbance pulse coupling

Display the results and analyse the MCU immunity level

TESTS MADE BY LANGER EMV SHOW HIGHEST ROBUSTNESS



Two times stronger than any competitor MCU

Highest level of noise immunity proven

Test limits reached without being disturbed

RX23T MCU FAMILY – SPARE TIME, EFFORTS & MONEY

MCU self-protected enable 2-layers PCB, faster PCB design layout, higher reliability

Remove by-pass capacitors, ferrites, damping resistors, chocks…

Line filter reduce by 30%, no oversized PCB, cost down-down BoM, PCB cost reduced

Pass highest ESD level the 1st time, meet project deadline, secure product launch

Download the complete RX23T Langer EMV report

Vincent.mignard@renesas.com