ProXO Register Descriptions and Programming

This document describes the behavior and function of the customer-programmable volatile-memory registers in the ProXO clock generator. For details of product operation, refer to the ProXO XP and XF series datasheets.

Contents

1. Overview

The ProXO device consists of an integrated 50MHz quartz crystal and PLL synthesizer IC to generate any clock frequency between 15MHz and 2.1GHz. The ProXO is pre-programmed at the factory for a certain output frequency and output logic type but can be re-programmed in the field to change any of its properties. The re-programming only affects volatile memory. Cycling the power supply will erase the re-programming and bring back the original factory settings.

The ProXO part number will describe the factory settings for output frequency and other properties.

2. ProXO Register Set

A ProXO device contains volatile (RAM) 8-bit registers and non-volatile 8-bit registers (Figure 1). The non-volatile registers are One-Time Programmable (OTP) and will be pre-programmed at the factory with a specific configuration in accordance with its part number.

The device operates according to settings in RAM registers. At power-up, a pre-programmed configuration is transferred from OTP to RAM registers and then a selected frequency configuration is passed to the device operation settings. There are 4 such frequency configurations, selectable with pins on the device. The device behavior can be modified by reprogramming the RAM registers through I2C and instructing the Active Trigger Control to pass the changes to the device settings.

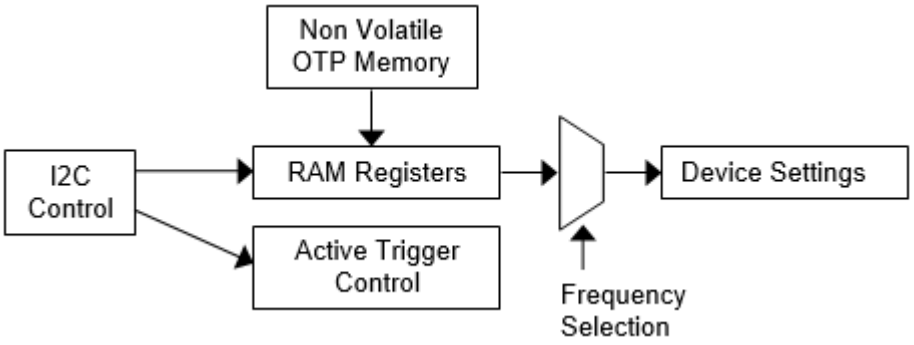

Figure 1. Register Maps

3. I²C Interface and Register Access

A ProXO device uses the SDA and SCL pins for a 2-wire serial interface that complies with the I2C bus standard. The I2C access protocol in the device is byte access (random access) only for writing settings to the device and both random and sequential access (block mode) for reading settings from the device.

A valid write operation must have a full 8-bit memory (register) address after the device address word from the master, which is followed by an acknowledge bit from the slave (SDA = 0/Low). The next 8 bits must contain the data word intended for the targeted register. After the data word is received, the slave responds with another acknowledgment bit and the master must end the write sequence with a STOP condition (see Figure 2).

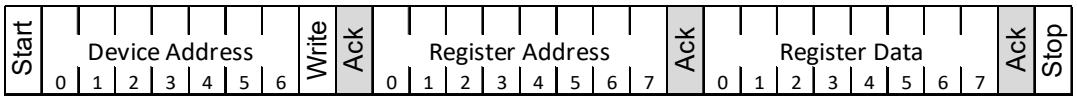

Figure 2. Random Write

Read operations are initiated the same way as write operations, except that the R/W bit of the slave address is set to '1' (High). There are two basic read operations: random read and sequential read. Figure 3 and Figure 4 illustrate these operations.

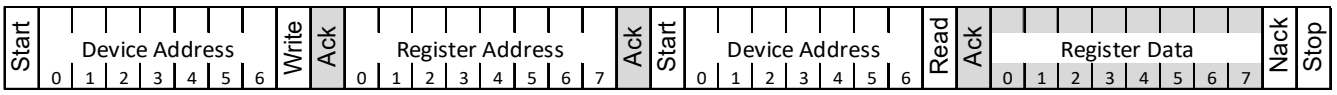

Figure 3. Random Read

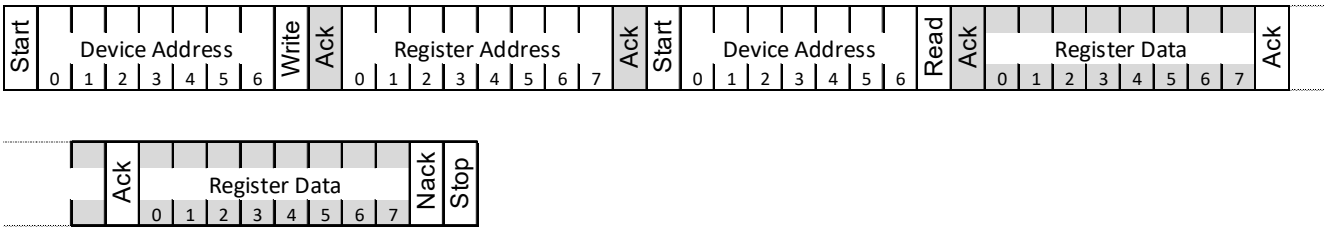

Figure 4. Sequential Read

Sequential read operations follow the same process as random reads, except that the master issues an acknowledgment instead of a STOP condition after transmission of the first 8-bit data word. This action results in an incrementing of the internal address pointer, and subsequently output of the next 8-bit data word. By continuing to issue acknowledges instead of STOP conditions, the master may serially read the entire contents of the slave.

All ProXO devices will come pre-programmed. However, if there is a need to change the configuration (supply voltage, frequency, output type, etc.), one may do so via I2C. The default I2C device address is 0xA0 (8-bit) or 0x50 (7-bit).

Table 1. RAM Overview

Register Address	Function Explanation
0x00 – 0x04	Reserved (trim settings & status info)
0x05 – 0x0F	Unused
0x10 – 0x15	Frequency 0 settings
0x16 – 0x1F	Unused
0x20 – 0x25	Frequency 1 settings
0x26 – 0x2F	Unused
0x30 – 0x35	Frequency 2 settings
0x36 – 0x3F	Unused
0x40 – 0x45	Frequency 3 settings
0x46 – 0x4F	Unused
0x50 – 0x57	▪ Output driver settings ▪ Crystal oscillator settings ▪ XO / VCXO function settings ▪ Miscellaneous settings
0x58 – 0x5F	Unused
0x60 – 0x63	▪ Programming commands ▪ OTP burn control ▪ Active Trigger Control
0x64 – 0x6F	Unused
0x70 and 0x71	Reserved (voltage regulator settings)
0x72 – 0x7F	Unused
0x80 – 0x83	Reserved (test settings)
0x84 – 0x8F	Unused
0x90 – 0xA3	Reserved (test settings)
0xA4 – 0xAF	Unused
0xB0 – 0xB4	Reserved (test settings)
0xB5 – 0xCC	Unused
0xCD – 0xCF	Reserved (test settings)
0xD0 – 0xDF	Reserved (miscellaneous)
0xE0 – 0xE9	Reserved (test settings)
0xEA – 0xEF	Unused
0xF0 – 0xFF	Reserved (test settings)

Table 2. RAM Register Map

Register Address		Register Bit	Default	Type	Function Explanation
Decimal	Hex				
00	0x00	[7..0]	51-hex	Read Only	Device ID
01	0x01	[7..0]	2A-hex	Read Only	Version ID
02	0x02	[7..0]	10-hex	R/W	Reserved
03	0x03	[7..0]	FF-hex	R/W	Reserved
04	0x04	[7..0]	00-hex	R/W	Reserved
16	0x10	[7..0]	37-hex	R/W	Frequency 0, Output Divider bits [7..0] (Default for Xtal = 50MHz, Out = 125MHz)
17	0x11	7	0	R/W	Frequency 0, Output Divider bit [8]
		[6..0]	100 0101	R/W	Frequency 0, Feedback Divider Integer bits [6..0]
18	0x12	7	0	R/W	Reserved
		6	0	R/W	Frequency 0, Charge Pump Offset Enable
		[5..4]	00	R/W	Frequency 0, Feedback Divider Integer bits [8..7]
		[3..1]	101	R/W	Frequency 0, Charge Pump Value
		0	0	R/W	Frequency 0, PLL Mode: 0 = Fractional Mode, 1 = Integer Mode
19	0x13	[7..0]	00-hex	R/W	Frequency 0, Feedback Divider Fraction bits [7..0]
20	0x14	[7..0]	00-hex	R/W	Frequency 0, Feedback Divider Fraction bits [15..8]
21	0x15	[7..0]	C0-hex	R/W	Frequency 0, Feedback Divider Fraction bits [23..16]
32	0x20	[7..0]	37-hex	R/W	Frequency 1, Output Divider bits [7..0] (Default for Xtal = 50MHz, Out = 125MHz)
33	0x21	7	0	R/W	Frequency 1, Output Divider bit [8]
		[6..0]	100 0101	R/W	Frequency 1, Feedback Divider Integer bits [6..0]
34	0x22	7	0	R/W	Reserved
		6	0	R/W	Frequency 1, Charge Pump Offset Enable
		[5..4]	00	R/W	Frequency 1, Feedback Divider Integer bits[8..7]
		[3..1]	101	R/W	Frequency 1, Charge Pump Value
		0	0	R/W	Frequency 1, PLL Mode: 0 = Fractional Mode, 1 = Integer Mode
35	0x23	[7..0]	00-hex	R/W	Frequency 1, Feedback Divider Fraction bits [7..0]
36	0x24	[7..0]	00-hex	R/W	Frequency 1, Feedback Divider Fraction bits [15..8]
37	0x25	[7..0]	C0-hex	R/W	Frequency 1, Feedback Divider Fraction bits [23..16]
48	0x30	[7..0]	37-hex	R/W	Frequency 2, Output Divider bits [7..0] (Default for Xtal = 50MHz, Out = 125MHz)
49	0x31	7	0	R/W	Frequency 2, Output Divider bit [8]
		[6..0]	100 0101	R/W	Frequency 2, Feedback Divider Integer bits [6..0]

Table 2. RAM Register Map (Cont.)

Register Address		Register Bit	Default	Type	Function Explanation
Decimal	Hex				
50	0x32	7	0	R/W	Reserved
		6	0	R/W	Frequency 2, Charge Pump Offset Enable
		[5..4]	00	R/W	Frequency 2, Feedback Divider Integer bits [8..7]
		[3..1]	101	R/W	Frequency 2, Charge Pump Value
		0	0	R/W	Frequency 2, PLL Mode: 0 = Fractional Mode, 1 = Integer Mode
51	0x33	[7..0]	00-hex	R/W	Frequency 2, Feedback Divider Fraction bits [7..0]
52	0x34	[7..0]	00-hex	R/W	Frequency 2, Feedback Divider Fraction bits [15..8]
53	0x35	[7..0]	C0-hex	R/W	Frequency 2, Feedback Divider Fraction bits [23..16]
64	0x40	[7..0]	37-hex	R/W	Frequency 3, Output Divider bits [7..0] (Default for Xtal = 50MHz, Out = 125MHz)
65	0x41	7	0	R/W	Frequency 3, Output Divider bit [8]
		[6..0]	100 0101	R/W	Frequency 3, Feedback Divider Integer bits [6..0]
66	0x42	7	0	R/W	Reserved
		6	0	R/W	Frequency 3, Charge Pump Offset Enable
		[5..4]	00	R/W	Frequency 3, Feedback Divider Integer bits [8..7]
		[3..1]	101	R/W	Frequency 3, Charge Pump Value
		0	0	R/W	Frequency 3, PLL Mode: 0 = Fractional Mode, 1 = Integer Mode
67	0x43	[7..0]	00-hex	R/W	Frequency 3, Feedback Divider Fraction bits [7..0]
68	0x44	[7..0]	00-hex	R/W	Frequency 3, Feedback Divider Fraction bits [15..8]
69	0x45	[7..0]	C0-hex	R/W	Frequency 3, Feedback Divider Fraction bits [23..16]
80	0x50	[7..5]	000	R/W	Reserved
		4	1	R/W	High Speed I^2C Enable: 0 = Standard Speed Mode, I^2C clock up to 400kHz 1 = High Speed Mode, I^2C clock up to 800kHz
		3	0	R/W	CMOS Output Enable
		[2..0]	101	R/W	Reserved
81	0x51	7	1	R/W	XO Frequency Doubler Disable: 0 = Doubler Enabled, 1 = Doubler Disabled
		[6..5]	10	R/W	Power Supply Voltage: 00 = 1.8V, 01 = 2.5V, 10 = 3.3V
		[4..3]	00	R/W	Reserved
		2	0	R/W	VCXO Disable: 0 = VCXO Mode, 1 = XO Mode
		[1..0]	00	R/W	VCXO Modulation Bandwidth: 00 = 10kHz, 01 = 20kHz, 10 = 5kHz
82	0x52	7	0	R/W	VCXO Gain Slope: 0 = Positive Gain Slope, 1 = Negative Gain Slope
		[6..4]	010	R/W	VCXO Gain Exponentially
		[3..0]	1010	R/W	VCXO Gain Scale
83	0x53	7	1	R/W	Output Enable Polarity: 0 = Active Low, 1 = Active High
		[6..4]	000	R/W	Output Logic Type: 000 = LVDS, 001 = LVPECL, 010 = CML, 011 = HCSL, 101 = LVPECL2 (No common mode offset current)
		[3..0]	0010	R/W	Reserved

Table 2. RAM Register Map (Cont.)

Register Address		Register Bit	Default	Type	Function Explanation
Decimal	Hex				
84	0x54	7	0	R/W	I²C Device Address Enable: 0 = Default 0x50, 1 = Use bits [6..0] value
		[6..0]	000 0000	R/W	I²C Device Address
85	0x55	[7..6]	10	R/W	XO Amplifier GM Overtone Value
		[5..0]	01 0100	R/W	XO Load Capacitance Trim Value, X1 pin
86	0x56	[7..4]	1000	R/W	XO Amplifier Slice
		3	0	R/W	Bypass the XO oscillator: 0 = Not bypassed, 1 = Bypass
		[2..0]	010	R/W	XO Load Capacitance Trim Value, X2 pin
87	0x57	7	0	R/W	Overtone Operation Disable: 0 = 3rd Overtone Mode, 1 = Fundamental Mode
		[6..4]	101	R/W	Overtone Filter Resistor Value
		[3..0]	1000	R/W	Reserved
96	0x60	7	0	R/W	0 → 1 = Copy OTP content to RAM Registers (follow up with 1 → 0 to reset).
		6	0	R/W	Reserved
		5	0	R/W	0 → 1 = Push RAM content to Device Settings (follow up with 1 → 0 to reset).
		[4..1]	0000	R/W	Reserved
		0	0	R/W	0 → 1 = Trigger Calibration to lock the PLL (follow up with 1 → 0 to reset).
97	0x61	[7..2]	0000 00	R/W	Reserved
		[1..0]	00	R/W	OTP Burn Control (see appendix 5)
98	0x62	[7..2]	0000 00	R/W	Reserved
		1	0	R/W	0 → 1: Push Small Change of RAM Registers to Device Settings (see Appendix C: Miscellaneous Settings Examples for Registers 0x50–0x57)
		0	0	R/W	0 → 1: Push Large Change of RAM Registers to Device Settings (see Appendix C: Miscellaneous Settings Examples for Registers 0x50–0x57)
99	0x63	[7..0]	00-hex	R/W	Reserved
112	0x70	[7..0]	0C-hex	R/W	Reserved
113	0x71	[7..0]	08-hex	R/W	Reserved
128	0x80	[7..0]	30-hex	R/W	Reserved
129	0x81	[7..0]	06-hex	R/W	Reserved
130	0x82	[7..0]	06-hex	R/W	Reserved
131	0x83	[7..0]	02-hex	R/W	Reserved
144	0x90	[7..0]	00-hex	R/W	Reserved
145	0x91	[7..0]	06-hex	R/W	Reserved
146	0x92	[7..0]	06-hex	R/W	Reserved
147	0x93	[7..0]	00-hex	R/W	Reserved
148	0x94	[7..0]	06-hex	R/W	Reserved
149	0x95	[7..0]	00-hex	R/W	Reserved
150	0x96	[7..0]	02-hex	R/W	Reserved
151	0x97	[7..0]	06-hex	R/W	Reserved

Table 2. RAM Register Map (Cont.)

Register Address		Register Bit	Default	Type	Function Explanation
Decimal	Hex				
152	0x98	[7..0]	06-hex	R/W	Reserved
153	0x99	[7..0]	00-hex	R/W	Reserved
154	0x9A	[7..0]	02-hex	R/W	Reserved
155	0x9B	[7..0]	00-hex	R/W	Reserved
156	0x9C	[7..0]	02-hex	R/W	Reserved
157	0x9D	[7..0]	03-hex	R/W	Reserved
158	0x9E	[7..0]	00-hex	R/W	Reserved
159	0x9F	[7..0]	C0-hex	R/W	Reserved
160	0xA0	[7..0]	01-hex	R/W	Reserved
161–163	0xA1–0xA3		00-hex	R/W	Reserved
176	0xB0	[7..0]	42-hex	R/W	Reserved
177	0xB1	[7..0]	03-hex	R/W	Reserved
178	0xB2	[7..0]	64-hex	R/W	Reserved
179	0xB3	[7..0]	14-hex	R/W	Reserved
180	0xB4	[7..0]	00-hex	R/W	Reserved
205–207	0xCD–0xCF		00-hex	R/W	Reserved
208–210	0xD0–0xD2		00-hex	R/W	Reserved
211	0xD3	[7..0]	03-hex	R/W	Reserved
212–213	0xD4–0xD5		00-hex	R/W	Reserved
214	0xD6	[7..0]	13-hex	R/W	Reserved
215	0xD7	[7..0]	1C-hex	R/W	Reserved
216–223	0xD8–0xDF		00-hex	R/W	Reserved
224–228	0xE0–0xE4		00-hex	R/W	Reserved
229	0xE5	[7..0]	30-hex	R/W	Reserved
230–233	0xE6–0xE9		00-hex	R/W	Reserved
240–254	0xF0–0xFE		00-hex	R/W	Reserved

4. XO and VCXO Operation

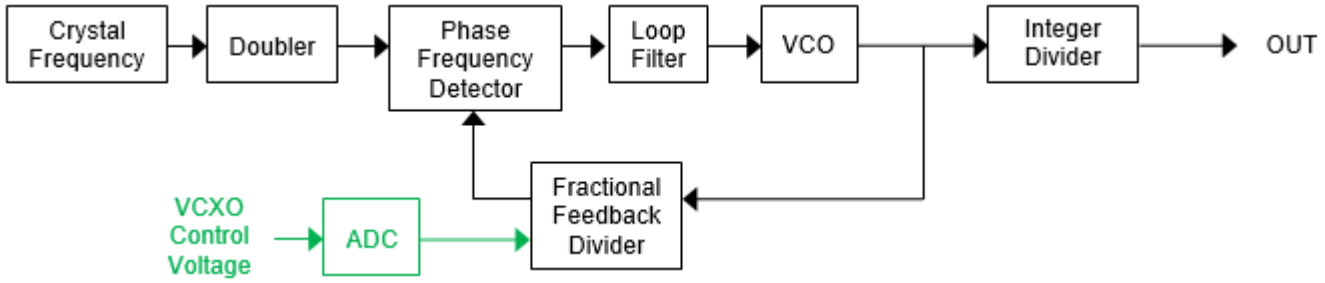

Figure 5. ProXO Block Diagram

The ProXO in the 12-pin 2.5 × 2.0 mm DFN package (XF style) can be configured both as a clock oscillator or "XO" and as a Voltage Controlled Xtal Oscillator or "VCXO". Other packages do not have the control voltage pin available. Traditionally, the control voltage for a VCXO affects the crystal, using a Varactor diode to tune the crystal frequency. The limitations of this approach are limited tuning range and relatively bad linearity of the tuning curve. The ProXO approach is digital with a perfectly linear tuning curve and programmable tuning range. Large tuning ranges are available that are not possible with the varactor diode approach.

XO and VCXO configuration is almost identical. For an XO, leave the VCXO function disabled: register 0x51 bit[2] = '1'. Other VCXO settings are ignored. The control voltage input is disabled and can be left open.

For a VCXO, set 0x51 bit[2] = '0' and make other settings to configure the VCXO function. More about setting up VCXO configurations in Appendix B: VCXO Configurations.

Equations:

$F_{VCO} = F_{CRYSTAL} \times$ Doubler × (Fractional Feedback Divider)
$F_{OUT} = F_{VCO}$ / (Integer Output Divider)
Doubler is ×2 when enabled and ×1 when disabled.

Limits:

$F_{CRYSTAL}$: 40MHz – 166MHz
F_{VCO}: 6860MHz – 8650MHz
$F_{DOUBLER}$: 40MHz – 80MHz (disable doubler when crystal > 80MHz)
Integer Output Divider: 4 – 511
Fractional Feedback Divider: 41 – 216

Table 3. Charge Pump Settings

VCO Frequency (MHz)	0x12 bits [3..1] or 0x22 bits [3..1] or 0x32 bits [3..1] or 0x42 bits [3..1]
VCO < 7000	101
7000 ≤ VCO < 7400	100
7400 ≤ VCO < 7800	011
7800 ≤ VCO	010

Table 4. Crystal Oscillator Settings

Crystal Frequency (MHz)	Oscillator Mode	XO Doubler 0x51 [7]	OT GM 0x55 [7..6]	XO Cap X1 0x55 [5..0]	XO Amp 0x56 [7..4]	XO Cap X2 0x56 [2..0]	OT Dis. 0x57 [7]	OT Res. 0x57 [6..4]
40 – 80[1]	Fun.	0	10	11 1100	0001	010	1	000
100 – 140	3rd OT	1	10	01 0101	1100	101	0	101
140 – 166	3rd OT	1	11	01 0101	1100	101	0	011

1. Most ProXO modules use a 50MHz fundamental mode crystal.

5. Revision History

Revision	Date	Description
1.02	Mar 24, 2025	Updated Register Address 84 / 0x54, register bit 7, to 0 = Default 0x50 from 0 = Default 0x55 in Table 2.
1.01	Jul 23, 2021	Updated text in section I2C Interface and Register Access.
1.00	Apr 8, 2021	Initial release.

Appendix A: Output Frequency Settings

In most cases, there will be multiple solutions to make a specific output frequency. The recommended solution is the one with the lowest VCO frequency above the VCO low limit of 6860MHz. There is one exception to that rule, when this lowest VCO frequency requires a fraction setting in the feedback counter, while there is an alternative solution with a higher VCO frequency where the feedback counter can be an integer value.

Equation 1: Output Divider = INT(1 + 6860 / F_{OUT})
Equation 2: F_{VCO} = F_{OUT} × Output Divider
Equation 3: Feedback Divider = F_{VCO} / ($F_{CRYSTAL}$ × Doubler) (Doubler = 2 when enabled, Doubler = 1 when disabled)

Check for potential integer Feedback Divider value by increasing the Output Divider value until FVCO passes above 8650MHz. For each Output Divider value, check if the Feedback Divider value is an integer value. In case there are no solutions where the Feedback Divider is an integer value, use the solution with the lowest VCO frequency above 6860MHz. In case there are solutions where the Feedback Divider value is an integer value, use the solution with the lowest VCO frequency and where the Feedback Divider is an integer value.

The Feedback Divider has an Integer and a Fraction setting, “FBInt” and “FBFrac” in the following equations:

Equation 4: FBInt = INT(Feedback Divider)
Equation 5: FBFrac = Feedback Divider - INT(Feedback Divider)
Equation 6: FBFrac bits = INT(0.5 + FBFrac × 2^{24})

For each frequency setting there are bits called “Feedback Divider Integer bits [8..0]” and Feedback Divider Fraction bits [23..0]”. The “FBFrac bits” value calculated in equation 6 can be written to the “Feedback Divider Fraction bits” in the registers. For the “FBInt” value from equation 4 we need one more check:

- When FBFrac < 0.5 → Write “Feedback Divider Integer bits” = FBInt value.
- When FBFrac ≥ 0.5 → Write “Feedback Divider Integer bits” = FBInt value + 1.

Example 1: $F_{CRYSTAL}$ = 50MHz, F_{OUT} = 125MHz

Output Divider = INT(1 + 6860 / 125) = 55
FVCO = 125 × 55 = 6875MHz
Feedback Divider = 6875 / (50 × 2) = 68.75

The Feedback Divider is a fractional value. When increasing the Output Divider to 56, the VCO frequency increases to 56 × 125 = 7000MHz and now the Feedback Divider is an integer value: Feedback Divider = 7000 / (50 × 2) = 70. This means that we will use an Output Divider value of 56 and a Feedback Divider value of 70 for this case.

Register 0x10 = 38-hex (Output Divider = 56)
Register 0x11 = 46-hex (Feedback Divider Integer = 70)
Register 0x12 = 09-hex (Charge Pump value = 4, see Table 3. Integer Mode is enabled)
Register 0x13 = 0x14 = 0x15 = 00-hex (The Feedback Divider Fraction is 0)

Example 2: $F_{CRYSTAL}$ = 50MHz, F_{OUT} = 148.5MHz

Output Divider = INT(1 + 6860 / 148.5) = 47
FVCO = 148.5 × 47 = 6979.5MHz
Feedback Divider = 6979.5 / (50 × 2) = 69.795

The Feedback Divider is a fractional value. When increasing the Output Divider value, no integer values are found for the Feedback Divider so we will work with Output Divider = 47.

FBInt = INT(69.795) = 69
FBFrac = 69.795 - INT(69.795) = 0.795
FBFrac bits = INT(0.5 + 0.795 × 224) = INT(0.5 + 13,337,886.72) = 13,337,887 = CB 85 1F hex

The FBFrac value is above 0.5 so we need to set the “Feedback Divider Integer bits” to 69+1 = 70.

Register 0x10 = 2F-hex (Output Divider = 47)
Register 0x11 = 46-hex (Feedback Divider Integer = 70)
Register 0x12 = 0A-hex (Charge Pump value = 5, see Table 3. Integer Mode is disabled)
Register 0x13 = 1F-hex
Register 0x14 = 85-hex
Register 0x15 = CB-hex

Appendix B: VCXO Configurations

All VCXO specific settings can be found in registers 0x51 and 0x52. General output frequency settings as explained in Appendix 1 are valid for VCXOs as well.

Register 0x51 Bit[2]

Enable the VCXO function. Bit[2] = 0. For use as a Clock Oscillator or XO, set Bit[2] = 1 and all other VCXO settings will be ignored.

Register 0x51 Bits[1..0]

Set the modulation bandwidth. A signal on the control voltage is essentially frequency modulating the output clock. The modulation bandwidth is a low pass filter for the control voltage.

00 sets 10kHz bandwidth.

01 sets 20kHz bandwidth (default).

10 sets 5kHz bandwidth.

11 is not used.

Register 0x52 Bit[7]

0 = Positive tuning slope: Control voltage is going up → output frequency is going up (default).

1 = Negative tuning slope: Control voltage is going up → output frequency is going down.

Register 0x52 Bits[6..0]

Set the VCXO gain. This setting influences how much the frequency of the output clock will tune when changing the control voltage between 0V and the VDD voltage. This block of 7 bits consists of two settings:

Bits[6..4] is the “Exponential” value. With every +1 change, the frequency tuning range for the output clock doubles. This can be considered the “gross setting”.

Bits[3..0] is the “Scale” value. This is the “fine setting” for the tuning range.

Below is an equation that estimates the frequency tuning range of the VCXO, based upon “Scale” and “Exponential” value settings.

Equation: Tuning Range (+ / - ppm) = $K * (Scale + 1) * 2^{Exponential}$

K = 2.767 is determined from measurements and fits the results best across all settings.

For example we want ±100ppm of pulling range: Scale = 8, Exponential = 2 gets closest to the ±100ppm requirement.

2.767 * (8 + 1) * 2^2 = ±99.6 ppm of tuning range

APR is a popular specification for a VCXO. It stands for “Absolute Pulling Range”. APR is a minimum achievable tuning range of the VCXO over the life of the device and all conditions like temperature variation. The combination of all instabilities and inaccuracies for the typical ProXO device is 50ppm. To find the required ‘±’ tuning range, add

50ppm to the required APR specification. For example, with a 50ppm APR requirement we can use the settings mentioned in the example above, resulting in ±100ppm of tuning range. Table 5 lists Scale and Exponential settings for a number of APR requirements.

Table 5. Recommended Register Settings for APR Requirements

APR	Tuning Range Required	Scale Setting	Exponential Setting	Actual Tuning Range
0ppm[1]	±50ppm	8	1	±49.8ppm
50ppm[2]	±100ppm	8	2	±99.6ppm
75ppm	±125ppm	11	2	±132.8ppm
100ppm	±150ppm	13	2	±150.0ppm

1. This is the minimum setting required to be able to tune out a frequency error from inaccuracy or other variations. In other words, this is the minimum setting required to always be able to lock to a perfectly accurate reference clock.
2. 50ppm APR is the most popular requirement. It is often used for DSL applications where one clock needs to lock to another clock and both can have up to a 50ppm error.

The plot in Figure 6 shows a few example VCXO tuning curves of output frequency deviation in ppm versus the voltage on the control voltage pin.

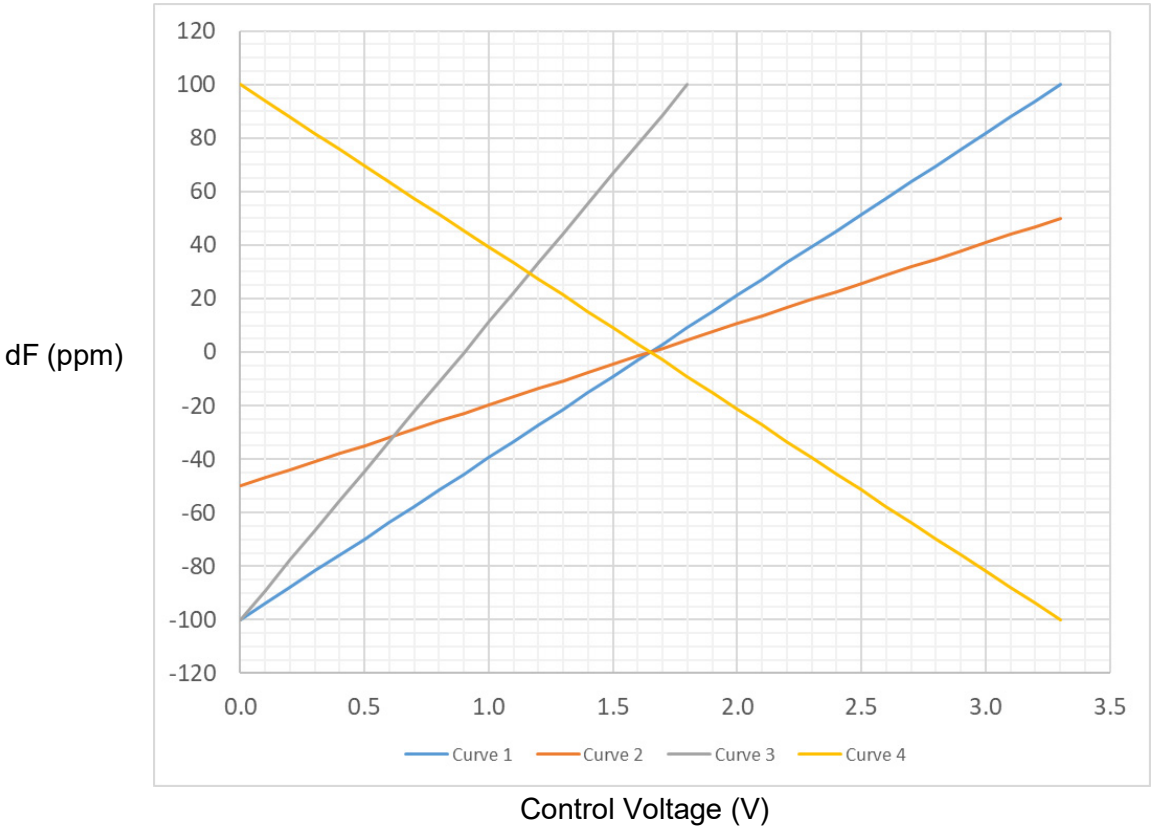

Figure 6. VCXO Tuning Curve Examples

Curve 1: ±100ppm tuning range with positive slope for VDD = 3.3V.

Curve 2: ±50ppm tuning range with positive slope for VDD = 3.3V.

Curve 3: ±100ppm tuning range with positive slope for VDD = 1.8V.

Curve 4: ±100ppm tuning range with negative slope for VDD = 3.3V.

Additional Recommendations:

Even though the register settings allow you to set up much bigger tuning ranges, it is not recommended to use a larger than ±1000ppm tuning range. The reason is that the Control Voltage essentially tunes the PLL VCO frequency and there is a limited margin to guarantee the PLL remains locked under all conditions. A tuning range of ±1000ppm or smaller is safe.

The feedback counter value needs to be a fractional number for the VCXO to perform well. For an XO, the performance is best with an integer feedback counter value, but with a VCXO you want the opposite and avoid the integer value. For example, with a 50MHz crystal and 156.25MHz output, we select a VCO frequency of 7500MHz with an XO so the feedback counter can be an integer value of 75. When this is a VCXO, it is recommended to use VCO = 6875MHz with a feedback counter value of 68.75. Sometimes an integer value for the feedback counter cannot be avoided, for example, when the output is 100MHz. For these cases we have alternative ProXO modules with a 61.44MHz crystal inside.

Appendix C: Miscellaneous Settings Examples for Registers 0x50–0x57

0x50 = 15-hex → This enables High-Speed I2C and disables the CMOS output. 0x50 can always be 15-hex.

0x51 → Important bits are XO Doubler control in bit 7 and power supply settings in bits 6 and 5.

Examples:

- 50MHz crystal and VDD = 3.3V → 0x51 = 40-hex (bit[7] = 0 for Doubler enabled, bits[6..5] = 10 for VDD = 3.3V)
- 100MHz crystal and VDD = 2.5V → 0x51 = A0-hex (bit[7] = 1 for Doubler disabled, bits[6..5] = 01 for VDD = 2.5V)

0x52 = 2A-hex → This register can always be 2A-hex for Clock Oscillator or XO operation. See Appendix B: VCXO Configurations for VCXO settings.

0x53 → Important bits are OE Polarity control in bit 7 and Output Logic settings in bits [6..4].

Examples:

- Positive OE Polarity and LVDS Logic → 0x53 = 82-hex (bit[7] = 1 for Pos. OE Pol., bits[6..4] = 000 for LVDS)
- Negative OE Polarity and LVPECL Logic → 0x53 = 12-hex (bit[7] = 0 for Neg. OE Pol., bits[6..4] = 001 for LVPECL)

0x54 → Bit[7] enables an alternative I2C address and the address value is in bits [6..0].

Examples:

- Use default device address 0x55 → 0x54 = 00-hex
- Change device address to 0x43 → 0x54 = C3-hex

0x55, 0x56 and 0x57 have crystal oscillator settings. SeeTable 4.

Examples:

- 50MHz fundamental mode crystal → 0x55 – 57 = BC-12-88 hex
- 114.285MHz 3rd overtone mode crystal → 0x55 – 57 = 95-C5-58 hex
- 156.25MHz 3rd overtone mode crystal → 0x55 – 57 = D5-C5-38 hex

Appendix D: I²C Active Trigger Control Commands in Registers 0x60 and 0x62

Setting Up the Device:

After writing all settings to registers 0x10 – 0x57, I2C commands are needed to push the settings to the Device Settings.

Write 0x60 = 00-hex → Make sure 0x60 is zero at the start.
Write 0x60 = 20-hex → Push all RAM Register settings to the Device settings.
Write 0x60 = 00-hex → Reset the command
Write 0x60 = 01-hex → Trigger the PLL calibration to make the PLL lock.
Write 0x60 = 00-hex → Reset the command

The ProXO device should now have its output enabled and toggling with the desired frequency.

Updating the Frequency:

After updating frequency settings in registers 0x10 – 0x15, these updates can be activated with one I2C command:

Write 0x62 = 01-hex → Activate the updates. We assume that 0x62 is 00-hex at the start.
Write 0x62 = 00-hex → Reset the command.

This is the command for the “Large Frequency Change”. After the change, a PLL calibration is triggered to make sure that the PLL locks again, independent of how large the change is. The disadvantage of triggering the calibration is that the output clock is interrupted for as long as it takes to calibrate the PLL. In case of a small frequency adjustment, a different command can be used that will not trigger a calibration. This frequency adjustment or “Small Frequency Change” will be glitch free.

Write 0x62 = 02-hex → Activate the updates without a PLL calibration (“Small Frequency Change”).
Write 0x62 = 00-hex → Reset the command.

The total amount of small changes accumulated since the last PLL calibration cannot increase over 1,000ppm, to make sure the PLL remains locked.

The “Large Frequency Change” and “Small Frequency Change” commands also work with devices where a configuration was programmed into OTP memory. When powered up, a device like this will transfer its OTP settings through the RAM registers to the device settings and start operating according to those settings. During operation, the RAM registers can be modified through I2C and the modifications can be pushed to the device settings, using a Small/Large Frequency Change command. This is useful for frequency margining or frequency fine tuning.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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