LLC Resonant Tank Design for 3.3kW Electric Vehicle On-board Charger with Wide-range Output Voltage

Introduction

This Design Guide is intended to assist the experienced designer with some prior knowledge of LLC design and operation by providing a starting point for the resonant tank values, and methods for calculating transformer ferrite and high-frequency copper losses.

Today's electric vehicle (EV) on-board chargers (OBC) require low weight and small size. High efficiency and high frequency operation help to achieve this, benefits offered by Renesas GaN FETs and the LLC topology.

Renesas GaN FETs are particularly well-suited for LLCand other high-frequency resonant applications for the following reasons:

- Fast switching
- Low drain charge ($Q_{OSS} = C_{OSS(tr)} * V_{DS}$)
- Very fast body diode (low Q_{RR})
- Low gate drive current requirement

Superjunction (SJ) MOSFETs tend to exhibit very large drain capacitance at low voltage (i.e. < 30V), typically 10x more than that of Renesas GaN FETs, resulting in a very large total drain charge (Q_{OSS}) at 400V. This greatly increases the required magnetizing current in an LLC transformer to enable proper zero-voltage switching (ZVS) operation, thereby increasing losses.

Additionally, SJ MOSFETs with relatively fast body diodes still exhibit large Q_{RR} (50x - 200x of Renesas GaN FETs),and may fail after only a few hard reverse-recovery events. Even though proper LLC operation does not subject the body diode to hard reverse-recovery, it is difficult to ensure that it does not occur during transient conditions such as power-up, where hard-switching typically occurs for several cycles before proper resonant operation commences.

The LLC resonant topology (Figure 1) is a popular topology for high efficiency applications. Its advantages include:

- ZVS provides high efficiency despite high switching frequency, reducing the transformer size
- Limited dv/dt and di/dt, which reduce ringing, spikes, and radiated EMI problems

Using an "integrated transformer" structure (where the transformer leakage inductance is deliberately made large to implement the series inductance L_{SER}) offers advantages such as:

- A single magnetic structure which reduces cost and size and improves efficiency over a standard transformer plus a discrete series inductor
- The required spacing between primary and secondary windings to achieve the desired leakage inductance reduces common-mode EMI due to displacement currents through the reduced capacitance between primary and secondary

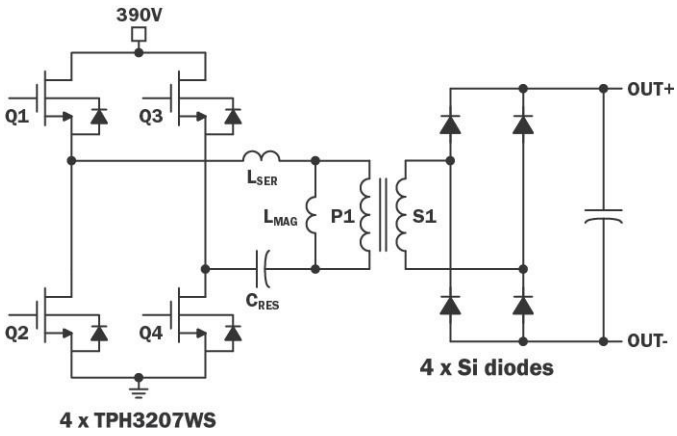

Figure 1. LLC topology and simulation schematic with full-bridge primary and secondary

In Figure 1, GaN FETs Q1 and Q4, and Q2 and Q3 are driven simultaneously. The two pairs are driven with a near50% duty cycle, 180º out of phase, with a short (~150ns) dead-time wherein all FETs are off.

LLC optimization

The LLC is typically most efficient when operating at the series resonant frequency (f_{SER}). When an LLC with a full-bridge primary and secondary is operating at f_{SER}, the input and output voltages are related simply by the transformer turns ratio:

$$\frac{V_{OUT}}{V_{IN}} = \frac{N_{SEC}}{N_{PRI}}$$

The operating frequency is used to control the output voltage. However, operating away from f_{SER} tends to reduce efficiency. EV OBC designs have an output (battery) voltage max to min ratio requirement between approximately 1.5:1 and 2:1, with constant power over that range.

The LLC topology's resonant powertrain has multiple variables: Magnetizing inductance, series inductance, resonant capacitance, and turns ratio. These four variables need to be optimized based on the extremes of output voltage. Non-optimal values will reduce efficiency and/or require a large expensive transformer. Multiple degrees of freedom can make design optimization very difficult. This Design Guide provides a methodology for establishing a starting point that will be reasonably close to optimum. SIMPLIS'™ "POP" (Periodic Operation Point which is steady-state switching), was used to find the optimal values and generate plots of RMS currents and frequency vs. output voltage (Figures 2-4.)

For a given combination of resonant frequency, rated power, input voltage, and max/min output voltage ratio, there is an optimum value of total (magnetizing + series) primary inductance (L_{PRI}). There is a large range of series inductance that will work (> 2.5:1). The resonant capacitor value is chosen to achieve the desired series resonant frequency f_{SER}. The operating frequency will vary above and below f_{SER} as output voltage varies. The turns ratio is adjusted to place operation at f_{SER} somewhere between min and max output voltage. The exact point is determined from the plots.

The simulations were performed with the following assumptions:

- Full-bridge primary and full-bridge diode secondary (See Figure 1)
- 390V_{DC} input (boost PFC pre-regulated front-end)
- 3.3kW load
- 1:1 turns ratio (this will be scaled according to the desired minimum output voltage)
- f_{SER}=250kHz: This provides a good compromise between core size, Litz wire gauge, and frequency capability of available LLC controllers, such as the NCP1399 (which operates in current mode with automatic dead-time)
- Three plots are presented: *K=4, 6.5, and 10*, where *$K=L_{MAG}/L_{SER}$; $L_{SER}=L_{MAG}/(K-1)$*; and *$L_{PRI}=L_{MAG}+L_{SER}$* This range of values of K yields reasonable results
- Uses 4 x TPH3207WS: 35mΩ (typ), TO-247, 650V (cont), 800V (transient)
- Output diodes have 75pF capacitance each (note diode capacitance increases magnetizing current requirements)
- Output diodes have V_F=0.8V

Sample time-domain simulation waveforms for K=6.5 and three different output voltages are shown in Figures 5-7.

Switching frequency, primary current, magnetizing current, and secondary current as a function of output voltage are shown in the frequency and RMS current plots (Figures 2-4.)

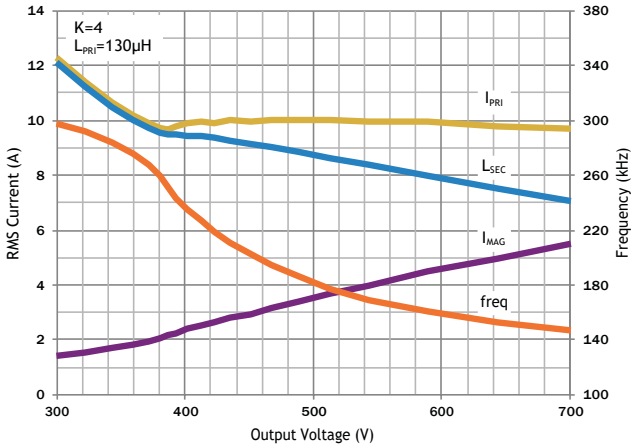

Figure 2. Frequency and currents vs. output voltage K=4, L_{PRI}=130µH

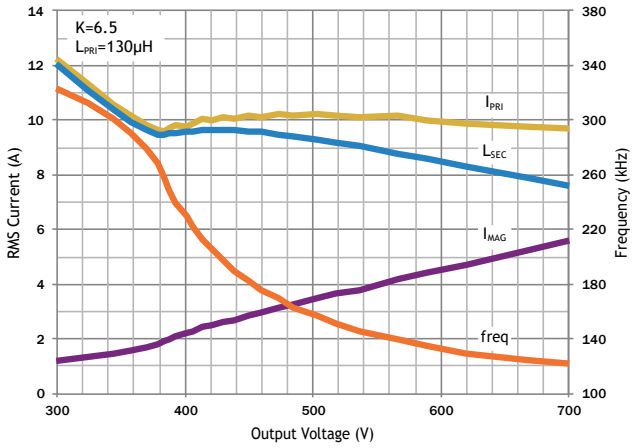

Figure 3. Frequency and currents vs. output voltage K=6.5, L_{PRI}=130µH

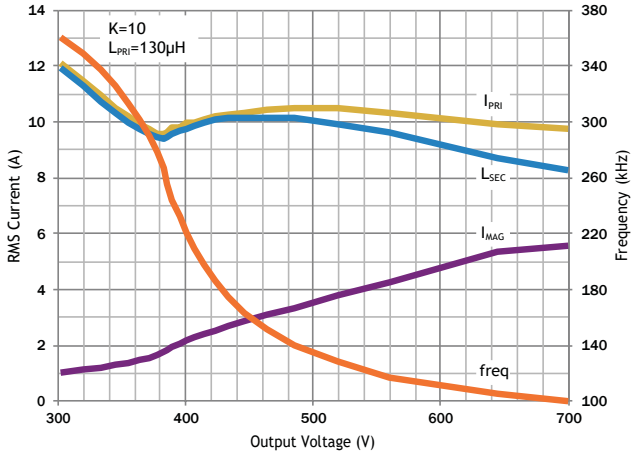

Figure 4. Frequency and currents vs. output voltage K=10, L_{PRI}=130µH

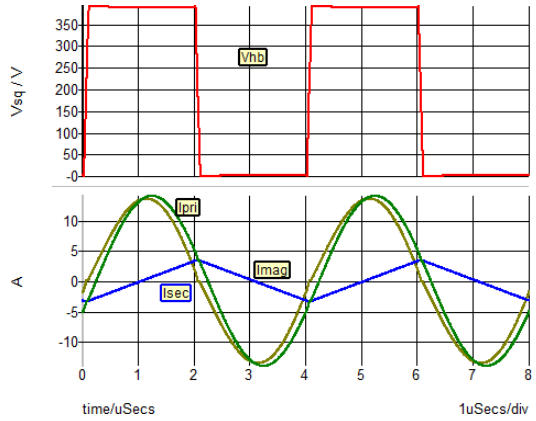

Figure 5. Operating waveforms at f_{RES} (V_{OUT}=V_{IN} with 1:1 turns ratio); note sinusoidal primary and secondary currents; V_{HS} (half-bridge voltage) is the drain voltage of Q1 in Figure 1

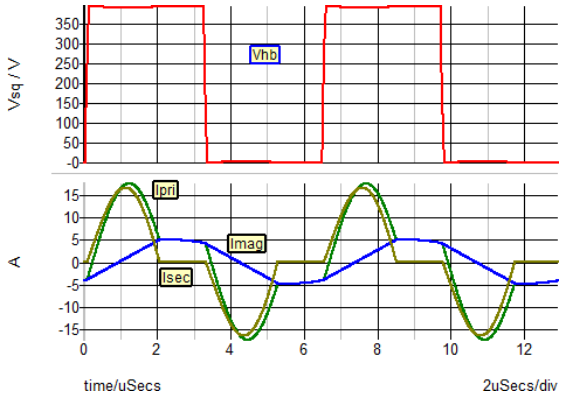

Figure 6. Operating waveforms at maximum output voltage (f_{MIN}=155kHz), K=6.5

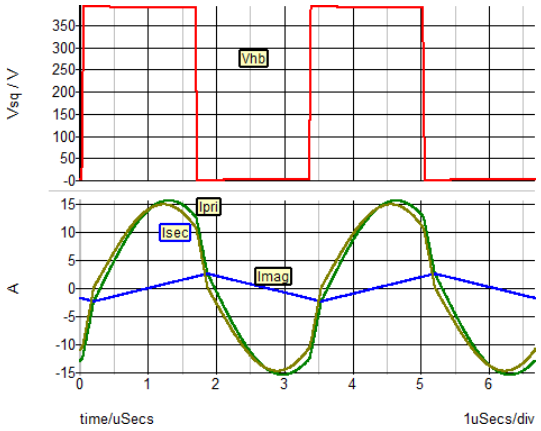

Figure 7. Operating waveforms at minimum output voltage (maximum frequency), K=6.5

The simulations in Figures 2-4 used L_{PRI}=130µH which is the maximum total primary inductance that enables proper ZVS throughout the output voltage range (see Figure 8.) A higher LPRI (or higher FET Q_{OSS}) will cause loss of ZVS at maximum output voltage (see Figure 9.) Excessive diode capacitance tends to cause loss of ZVS in the middle of the voltage range. A lower L_{MAG} will remedy this but increases magnetizing current and thus losses, especially within the windings that are situated near the core gap, from the flux concentration.

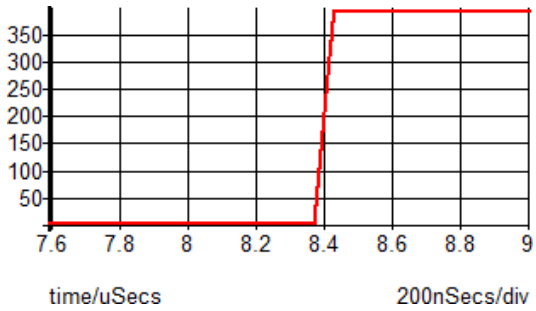

Figure 8. Switching edge (Q2 drain voltage) showing normal ZVS transition; the dv/dt is determined by the primary current and the capacitances

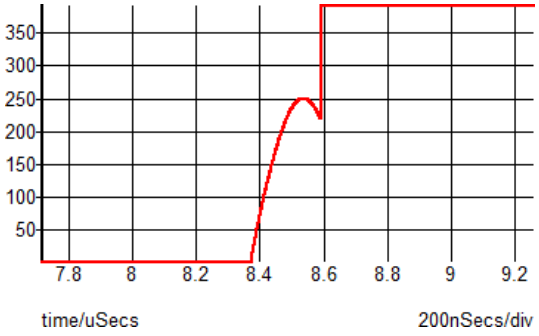

Figure 9. Switching edge (Q2 drain voltage) showing loss of ZVS when L_{MAG} is too high; there is insufficient magnetizing energy to completely charge/discharge the parasitic capacitances (from C_{OSS}, diode, and winding self-resonances), and the upper FET Q1 does not see ZVS

A small series resonant inductance (high K value) increases the frequency max/min ratio that is needed to regulate the output voltage over the output voltage range. However, with an integrated transformer, a lower K value increases the spacing required between primary and secondary, reducing available space for copper. With a non-integrated-magnetics design, a higher K value results in a smaller discrete series inductor.

However, the lower f_{MIN} (frequency at maximum output voltage) requires more turns per volt (in both primary and secondary) or a larger transformer core, increasing losses which may outweigh the benefit from the reduced spacing (or reduced size of the discrete inductor if one is used). With an integrated-transformer, the series inductance can be the value that results from the core and bobbin geometry and the turns resulting from the core loss calculations at maximum output voltage, provided it is within the acceptable K value range (4-10.)

Increasing turns will increase the leakage inductance, proportional to the square of the primary turns. Increasing the spacing between primary and secondary will also increase leakage inductance. Alternatively, a small additional discrete inductor can be used to add to the series inductance.

Observations on the RMS current plots

The plots (Figures 2-4) of primary current I_{PRI} show a dip where the output voltage is slightly below 390V, where it operates at resonance, V_O=V_{IN} with a 1:1 transformer turns ratio. The slight deviation from 390V is due to conduction losses in the FETs and diodes. Note that for higher output voltages, the frequency must go below f_{RES} for the LLC resonant tank to "amplify" the voltage. Below 390V the frequency must go above f_{RES} for the LLC resonant tank to reduce the output voltage. A useful minimum voltage is around 340V. Below that, I_{PRI} goes up sharply. For all designs use a minimum voltage of 340V. (This will later be scaled to your actual minimum voltage.) f_{MIN} will be the frequency at V_{MAX} (maximum output voltage) for the chosen value of K. For intermediate values of K, the values for RMS current and frequency can be interpolated from the appropriate plots. The maximum voltage can be 510V (for output max/min=1.5), or 680V (for max/min=2), or any value within the range of the plots. There is margin outside this range to accommodate 100/120Hz ripple voltage at the input. Note that a larger output voltage ratio requires a lower f_{MIN} and thus a larger core.

Other Design Considerations

To scale the design to a different output voltage

$$turns\_ratio_{ne9} = \frac{340\ V}{V_{MIN\_NEW}}$$

where

$$turns\_ratio = \frac{N_{PRI}}{N_{SEC}}$$

The new secondary RMS current will be

$$I_{SEC_{NEC}} = \frac{I_{SEC_{PLFT}}}{turns_{ratio_{NEW}}}$$

I_{SEC_PLOT} is I_{SEC} read from Figures 2-4.

To scale to a different input voltage

Calculate

$$\text{Vscaler} = \text{V}_{\text{NEW}} / 390\ \text{V}$$

The inductances will scale inversely with *Vscaler²*

$$\text{L}_{\text{NEW}} = \text{L}_{\text{OLD}} * \text{Vscaler}^2$$

To scale to a different resonant frequency

Calculate fscaler

$$fscaler = f_{RES\_NEW} / 250\ kHz$$

The new inductances will be

$$\text{L}_{\text{NEW}} = \text{L}_{\text{OLD}} / \text{fscaler}$$

The resonant capacitor C_{RES} is always calculated via

$$f_{RES} = \frac{1}{2 * \pi * \sqrt{L_{SER} * C_{RES}}}$$

To calculate the flux density

Look up f_{MIN} from Figures 2-4.

$$B_{P-P} = \frac{V_{IN}}{2 * N_{PRI} * f_{MIN} * A_C}$$

where A_C is the core area; use SI units

Note that typical core manufacturers provide loss curves that use B_{PK}, the peak value of flux where

$$B_{PK} = \frac{B_{P-P}}{2}$$

To determine the number of turns

Consider operation at f_{MIN}, where flux density and thus core losses will be highest. Look up the candidate core specifications (e.g. PQ4040), and calculate the acceptable total transformer loss in watts based on temperature rise, convection/forced-air liquid cooling, and surface area. Assign a percentage to core loss. Assuming 50% of total transformer loss coming from the core is a good starting point. Calculate the specific loss in mW per cm^3 based on the core volume. Then refer to the core loss curves and find the B_{PK} value that yields this loss at f_{MIN}. Use the earlier flux density equations to calculate N_{PRI}. N_{SEC} is then calculated from the turns ratio.

To calculate conduction losses in each GaN FET

$$P_{FET} = \frac{I^{\text{r}}_{PRI\ RMS} * R_{0N}}{2}$$

Calculating winding losses

The general equation for losses in a winding with no DC current is

$$P_{9indinu} = I^{\text{r}}_{ACRMS} * R_{DC} * (1 + F_E)$$

F_E is the eddy current loss factor due to skin and proximity effects, which can go from zero to infinity; use SI units.

Secondary winding losses

The copper losses are:

$$P_{Cu_{SE\sim}} = I^{\text{r}}_{sec} * R_{\ DC_{SE\sim}} * \left(1 + F_{E_{SE\sim}}\right)$$

Where I_{SEC} is the secondary RMS current, and DC resistance is

$$R_{DC\_SEC}(m\Omega) = \frac{N_{SEC} * mlt}{33.8 * n_{SEC} * d^{\text{r}}}$$

This is at a copper temperature of 100°C; *mlt* is the mean length per turn in mm; *d* is strand diameter in mm; n_{SEC} is the number of strands in the Litz wire in the secondary; N_{SEC} is secondary turns; F_{E_SEC} is the eddy current loss factor

$$F_{E_{SE\sim}} = \frac{1}{610} * \left(\frac{f_{E\acute{a}_{SE\sim}} * N_{SEC} * n_{SEC}}{w} \right)^{r} * d_{SEC}^{\hat{a}}$$

Also at 100°C; d_{SEC} is the strand copper diameter in mm; *w* is the winding "breadth" in mm (see Figure 10), and f_{EQ_SEC} is the equivalent frequency of the secondary current in kHz, read from "f_{EQ_MAIN}" in the plots in Figures 11-13. The equivalent frequency is higher than the actual frequency due to the harmonics in the current waveforms, which increases losses.

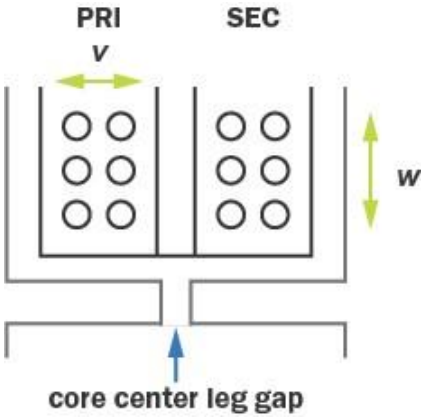

Figure 10. Partial cross-section of integrated transformer; the core gap is adjusted to achieve the desired L_{MAG}, the spacing between primary and secondary windings produces the leakage inductance and 'w' and 'v' are used for calculating eddy current losses

Primary winding losses are a little more complicated because the magnetizing and coupled currents' fields come from different directions. The magnetizing field comes from the gap, and the main coupled field from the secondary. They need to be considered separately. The total primary copper loss is:

$$P_{Cu_{PRI}} = R_{DC_{PRI}} * \left(I^{r}_{PRI} + I^{r}_{MAIN} * F_{E_{M\varsigma IN}} + I^{r}_{MAG} * F_{E_{M\varsigma G}} \right)$$

R_{DC_PRI} is the primary DC resistance (DCR) calculated similarly to the secondary DCR described earlier; I_{PRI} is the primary RMS current; I_{MAIN} is the main coupled current between primary and secondary current, and is equal to I_{SEC} in Figures 2-4 scaled by V_{scaler} above; F_{E_MAIN} is the eddy current factor of the main coupled current's field; I_{MAG} is the magnetizing current; F_{E_MAG} is the eddy current factor of the magnetizing current's field.

The eddy current factors are

$$F_{E\_MAIN} = \frac{1}{610} * \left(\frac{f_{E\acute{a}\_MAIN} * N_{PRI} * n_{PRI}}{w} \right)^{r} * d_{PRI}^{\hat{a}}$$

$$F_{E\_MAG} = \frac{1}{610} * \left(\frac{f_{E\acute{a}\_MAG} * N_{PRI} * n_{PRI}}{v} \right)^{r} * d_{PRI}^{\hat{a}}$$

f_{EQ_MAIN} and f_{EQ_MAG} are the equivalent frequencies of the main and magnetizing currents respectively, in kHz, from the plots in Figures 11-13. Dimensions *w* and *v* are in mm – they are shown in Figure 10. d_{PRI} is the copper strand diameter in mm; n_{PRI} is the number of Litz strands, and N_{PRI} is the number of turns.

Optimizing Litz wire gauge and number of strands

For a given strand diameter there is an optimum number of strands that minimizes copper loss, given by

$$n_{0PT} = \frac{24.7 * w}{N * d^{\acute{i}} * f_{E\acute{a}}}$$

Note that:

- The optimum number of strands may either not fit or may not fill up the entire available window. In the latter case, increasing the numbers of strands will ***increase*** losses despite reduced DC resistance, due to the increased number of *equivalent layers* which will sharply increase proximity losses. Note that with Litz, the equivalent number of layers is proportional to $layers * \sqrt{n}$ where *n* is the number of strands and *layers* is the physical number of winding layers.
- A thinner strand diameter with the optimal number of strands will tend to fill up more of the winding window (at higher cost); the thinnest wire at the optimum strands, that fills up the available window, is the lowest loss solution
- An acceptable strand diameter for a ~250kHz, 3.3kW LLC is 0.03 - 0.05mm. Strand diameter must be a fraction of the skin depth. AWG #38 (0.1mm), which is common, is too lossy, unless the frequency is reduced (which will increase the core size), or two transformers are used, either in series or parallel. Parallel

transformers (both primary and secondary in parallel) use fewer-strand Litz wire which costs less and is easier to terminate and solder. Current sharing accuracy will be mainly a function of L_{SER} accuracy.

- If thin enough Litz wire is not available, the operating frequency needs to be reduced

Dynamic adjustment of PFC output/LLC input voltage

When the output voltage is low and the switching frequency is below f_{RES}, the PFC output voltage should be adjusted down when possible to bring the LLC operation closer to f_{RES}. This will improve the efficiency of both the PFC and LLC stages.

Output diode reverse recovery

Even in diode-continuous-current mode (operation above f_{RES}), the di/dt during turn-off of the output diodes is controlled. The di/dt is limited by L_{SER} and thus losses related to diode reverse-recovery are relatively limited. The use of SiC output diodes will have modest benefits.

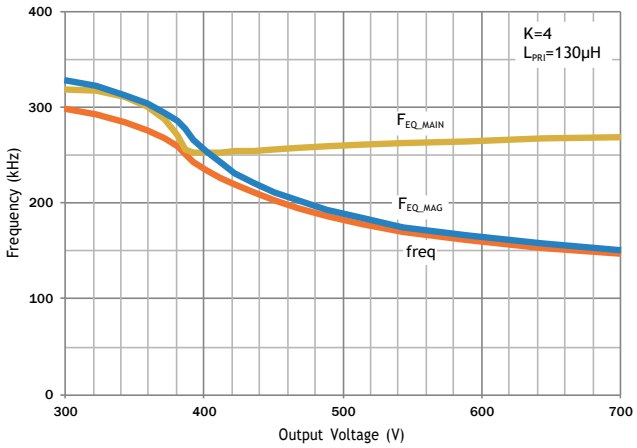

Figure 11. Plots of switching frequency and equivalent frequencies of the main coupled current and the magnetizing current for K=4, L_{PRI}=130µH; the equivalent frequencies are used for calculating eddy current losses in the windings

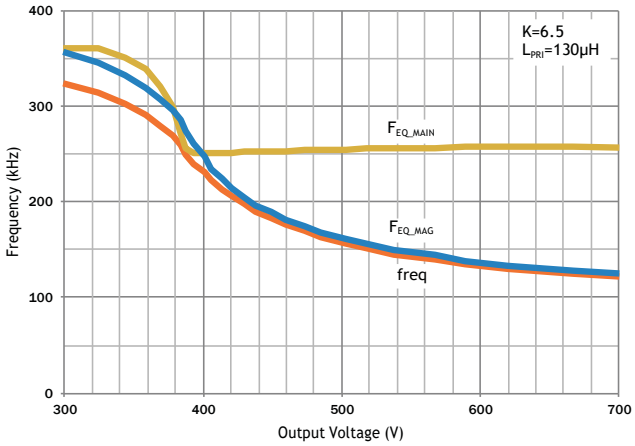

Figure 12. Plots of switching frequency and equivalent frequencies of the main coupled current and the magnetizing current for K=6.5, L_{PRI}=130µH

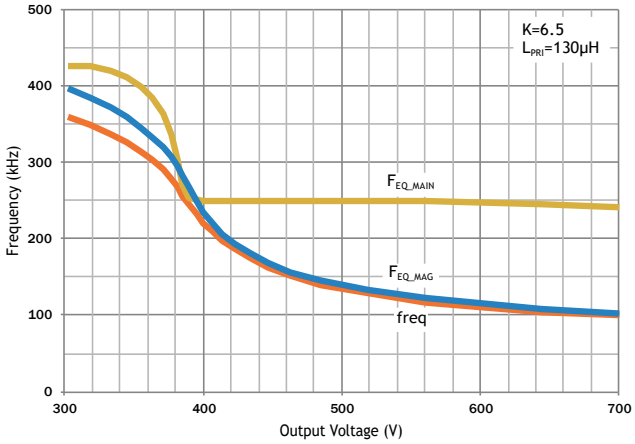

Figure 13. Plots of switching frequency and equivalent frequencies of the main coupled current and the magnetizing current for K=10, L_{PRI}=130µH

Further reading

The equations for Litz wire losses can be found here. (www.dartmouth.edu/~sullivan/litzwire/skin.html)