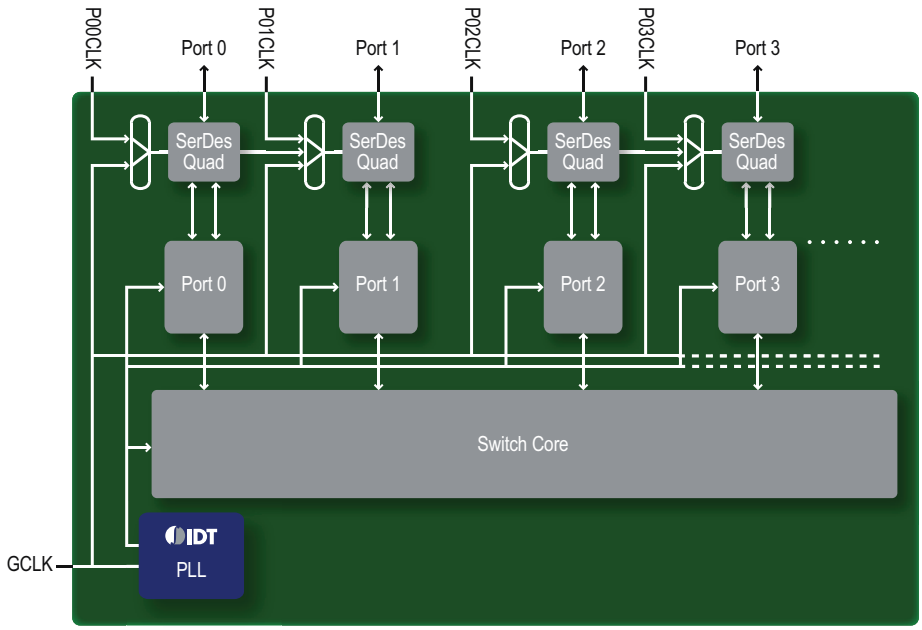
# Design tip: Clocking Architecture in IDT PCIe® Gen2 Switches

## Description

The PCI Express® (PCIe®) Base Specification states that the reference clocks for ports at the two ends of a PCI Express Link must be modulated such that they never exceed a total of 600 ppm (parts per million) difference. PCI Express specifications also permit use of SSC (Spread Spectrum Clocking) with +0 to -5000 ppm modulation of clock frequency at a modulation rate not to exceed 33 kHz.

Let's take a quick look at the clocking architecture in the IDT PCIe Gen2 switches.

The clocking architecture within the IDT Gen2 PCIe system interconnect switches has two differential Global Reference Clock inputs (GCLKP[1:0]/GCLKN[1:0]) and differential Port Reference Clock inputs (PxCLK) for ports that support local port clocking. For the Global Reference Clock inputs, none must be left unconnected and both must be connected to the same source. Unused Port Reference Clock inputs must be connected to Vss.



The Global Reference Clock inputs to the PLL are used to generate all of the clocks required by the internal switch logic and the SerDes. The Local Port Reference Clock input associated with a port (or a group of ports in the Gen2 Inter-Domain Switches) is used by the SerDes only when a port (or a group of ports in the Gen2 Inter-Domain Switches) is configured to function in local port clocked mode. Local Port Clock refers to the clock that a port uses to receive and transmit serial data.

The differential clock inputs require the signal source to drive 0V common-mode, and the REFCLK signal must meet the electrical specifications defined in the PCI Express Base 2.0 specification and the IDT device datasheet.

The Port Reference Clock inputs support Spread Spectrum Clocking (SSC) for reduced EMI and allow isolation of this SSC from the rest of the switch. The PCI Express Base 2.0 specification permits an SSC down-spread technique, which only allows from +0% to -0.5% (+0 to -5000 ppm) of the nominal data rate frequency at a modulation rate not to exceed 30 kHz - 33 kHz while still meeting ±300 ppm requirement (link partners cannot exceed a total of 600 ppm difference).

If SSC is used by the global reference clock, the same clock source or generator must be used for all link partners of the switch, both upstream and downstream.

There are no skew requirements between the Global Clock input and a Port Reference Clock input or between any of the Port Reference Clock inputs. A constant phase difference is acceptable.

The switch supports both 100 MHz and 125 MHz reference Global Clock inputs and the frequency selection is made via the Global Clock Frequency Select (GCLKFSEL) pin.

## Conclusion

A large variety of server, storage, communication and other embedded applications can be realized using IDT PCIe switches. For more information, visit http://www.idt.com/go/PCIe-Clocks.

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