ClockMatrix™ GUI Step-by-Step

This user guide is intended to familiarize new users on how to set up ClockMatrix (FW4.8.7) using the Timing Commander interface and to offer instructions on how to generate a basic configuration file.

Contents

1. Timing Commander

Figure 1. Timing Commander Launch Window

- Timing Commander serves as the platform that all Renesas' family of timing devices operate on.
- Download link: https://www.renesas.com/us/en/products/clocks-timing/clockmatrix-timing-solutions
- Open the Timing Commander GUI.

2. ClockMatrix GUI

A family of devices such as ClockMatrix contains a personality file and a settings file.The ClockMatrix personality files shown in Figure 2 covers devices 8A34000, 8A34001, and 8A34002.

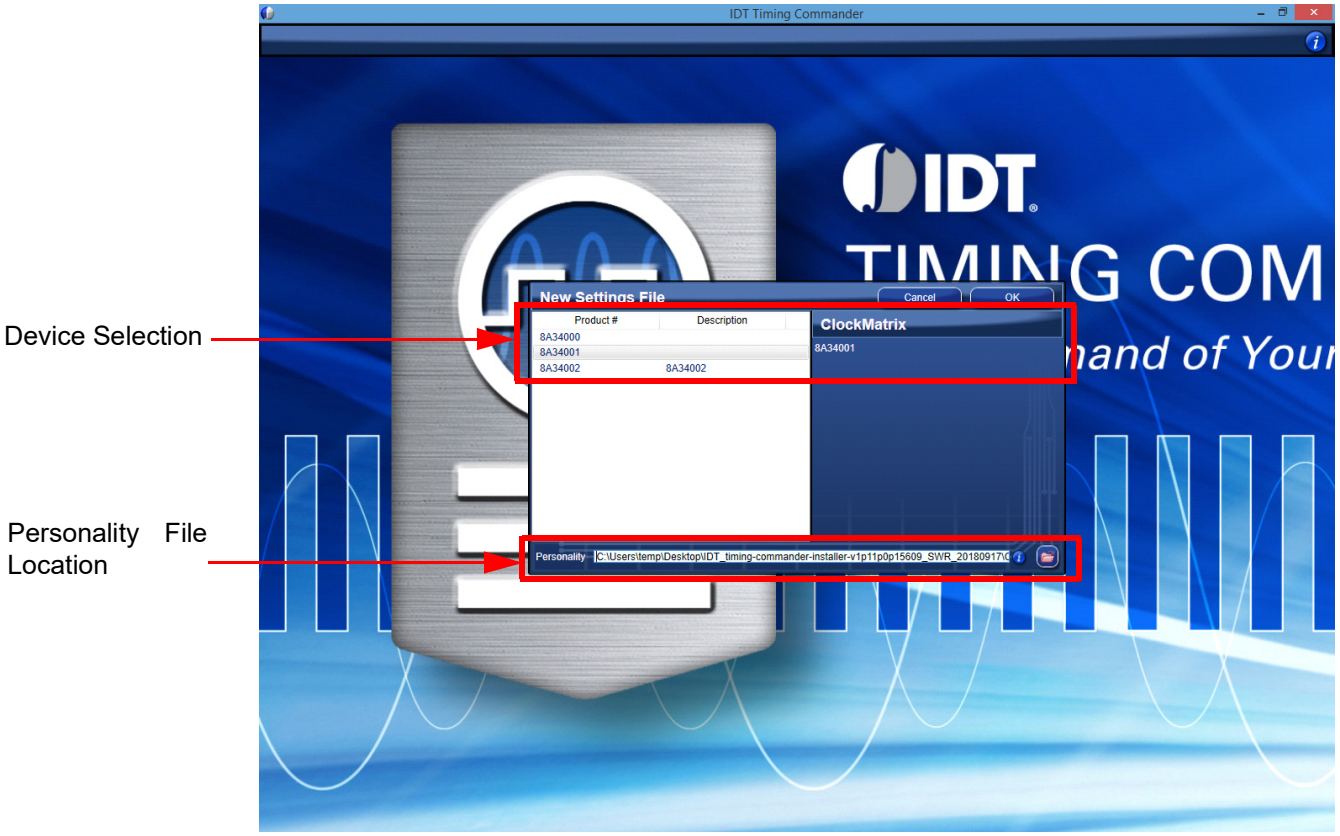


Figure 2. ClockMatrix New Settings File Window

The settings file is either loaded or created. A settings file will be created in this presentation. The user selects the desired device to create a settings file for using the ClockMatrix personality file.

2.1 Main Window

The ClockMatrix main window (see Figure 3) contains blocks (Input Stages, DPLL, System DPLL, System APLL, Output Stages, etc.). These are described throughout the following corresponding sections.

These blocks can be used/combined to create many different modes of operation (Synthesizer, Clock Generator, Jitter Attenuator, DCO, Combo Bus mode). See datasheet section “Basic Operating Modes”.

All grey or blue boxes are active and clickable (open sub-windows). White boxes allow the user to enter a valid value or to select a value. Some white boxes also provide information about the acceptable values or a register description when pointed at with a mouse. Tabs at the top of the screen allow the user to access bits/registers directly. See Figure 4.

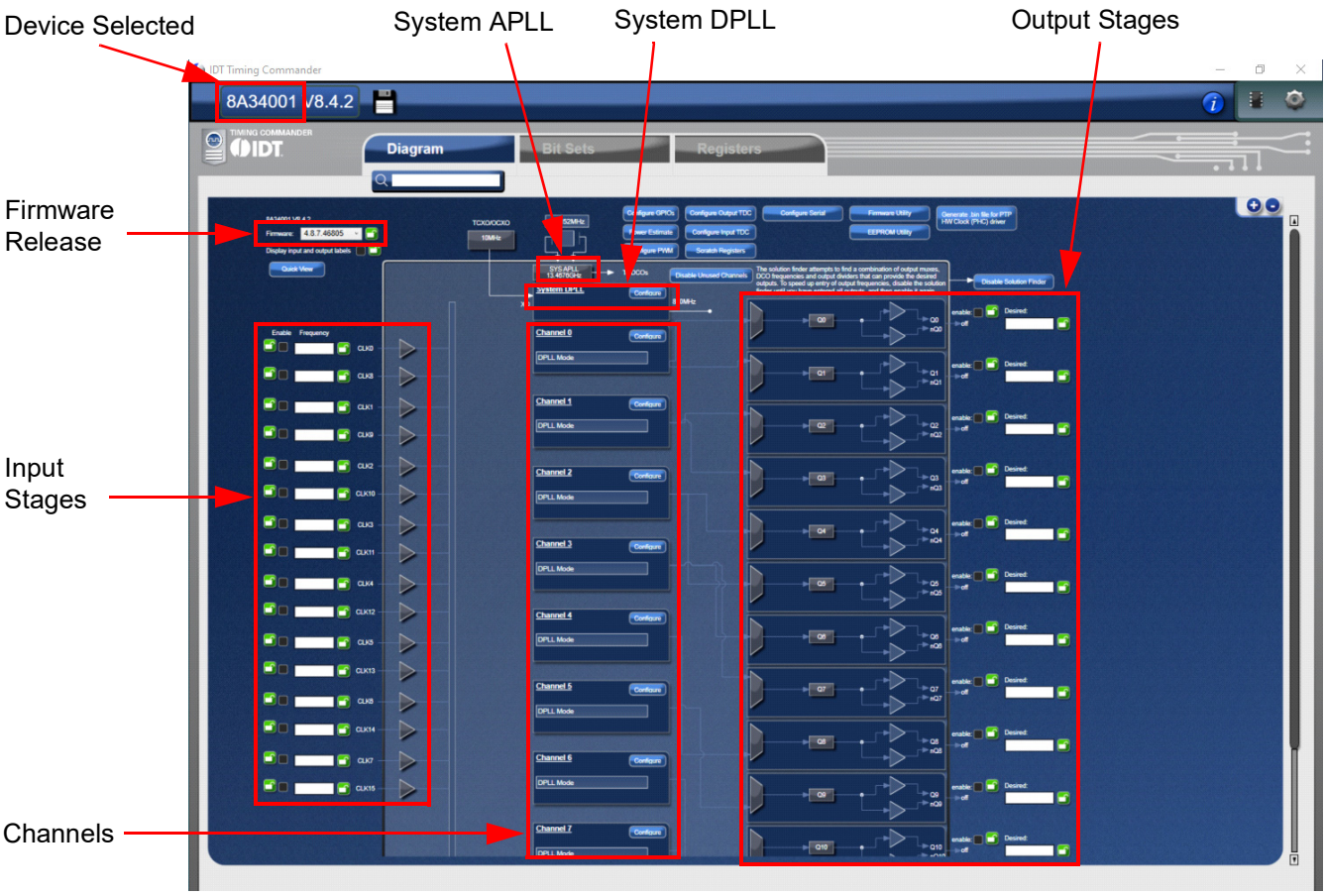


Figure 3. Main Window

Figure 4. Main Window (cont.)

2.2 Input Stages

- Up to 8/16 individually configurable inputs, either differential (PECL, LVDS, HCSL, and CML) or single-ended CMOS.
- Support frequencies from 0.5Hz to 1GHz (250MHz single-ended)
- Accepts either 1.8V, 2.5V, or 3.3V inputs depending on type (see “Input Stage Setting” table in datasheet)
- Accepts reference plus sync/frame pair
- Different types of reference monitoring:
  - **Loss of Signal (LOS)** monitor can be configured for either normal single cycle or gapped clock
  - **Activity** monitor coarsely measures the frequency accuracy (selectable between +0.1% to +20%)
  - **Frequency offset** monitor precisely measures the frequency accuracy (selectable between +9.2ppm to +130ppm)
  - Masks enable or disable a monitor

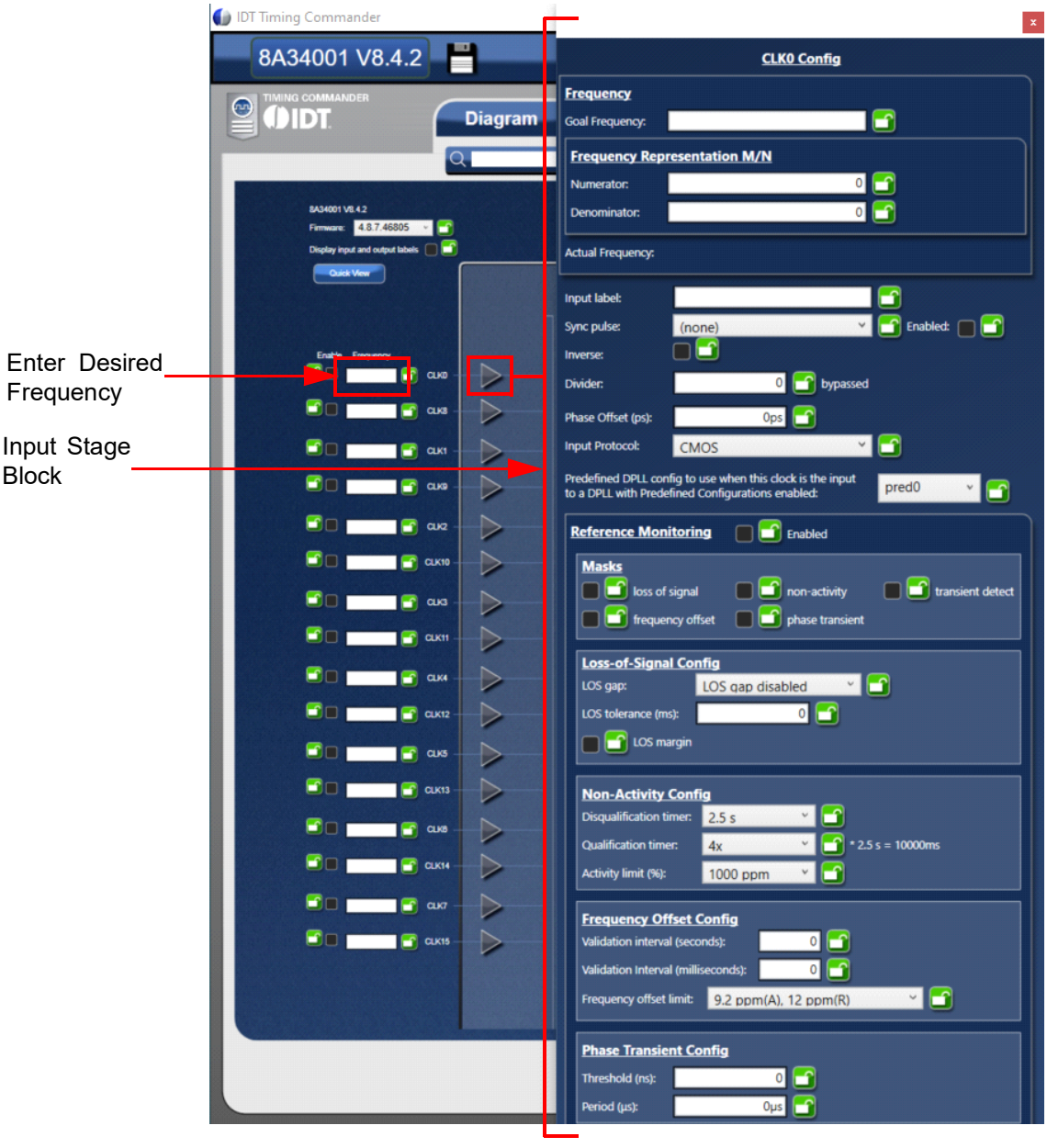


Figure 5. Input Stage Block Window

2.3 Channel Block

- Up to 8 independent channels depending on variant (see Figure 6)
- Each channel can be configured (see Figure 6) for:
  - DPLL mode (used in jitter attenuators)
  - DCO mode (used for 1588)
  - Synthesizer mode (rate conversion or clock generation)
  - Phase measurement mode
- Predefined standards can be loaded (e.g., G.8262) which load the appropriate digital loop filter settings and the lock criteria fields
- Grey boxes can be clicked to define other settings:
  - Filter: Bandwidth and PSL
  - DCO: Output frequency
  - Master Divider
  - TODx: Accumulator
- Other features such as external feedback and hitless reference switching are defined throughout this section.

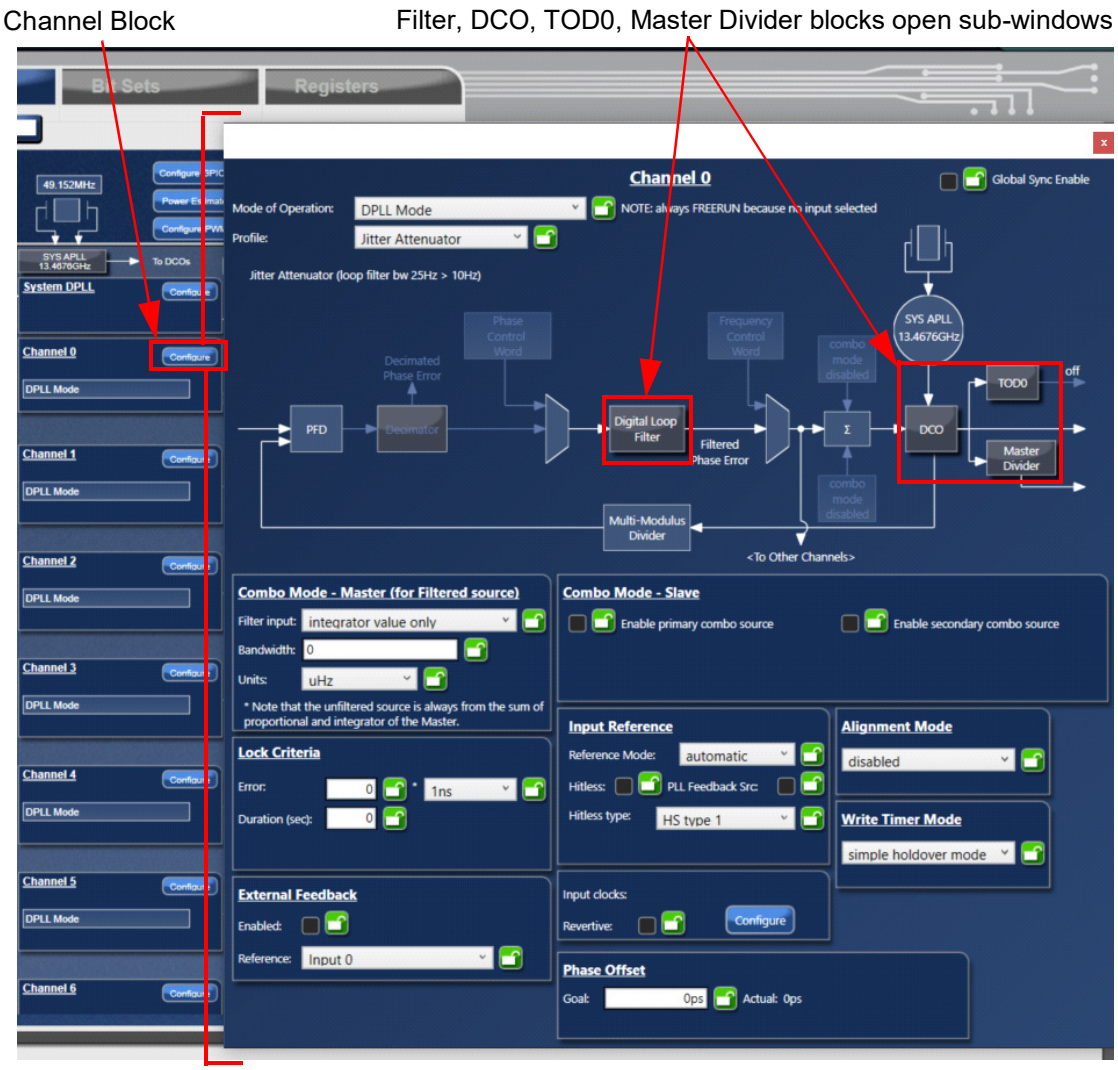


Figure 6. Channel Block Window

- Depending on the mode of the channel, certain blocks become active/inactive (see Figure 7)
- Combo bus allows channels to interact with each another:
  - Channels are connected via the summation block before the DCO (see Figure 7)
  - Used in SyncE and 1588: one channel serves as the SyncE clock and the other channel serves as the 1588 DCO
  - Used for stability compensation with use of a TCXO/OCXO and the system DPLL
  - Frequency adjustments can be applied to DCO of any channel and is available to all channels
  - Up to two slave channels can be defined for each master channel
  - See *ClockMatrix Auto-Alignment of Outputs Application Note*
- The output of each channel (output of DCO) feeds a respective output stage (see Figure 7)
- Output of DCO is a fractional divider

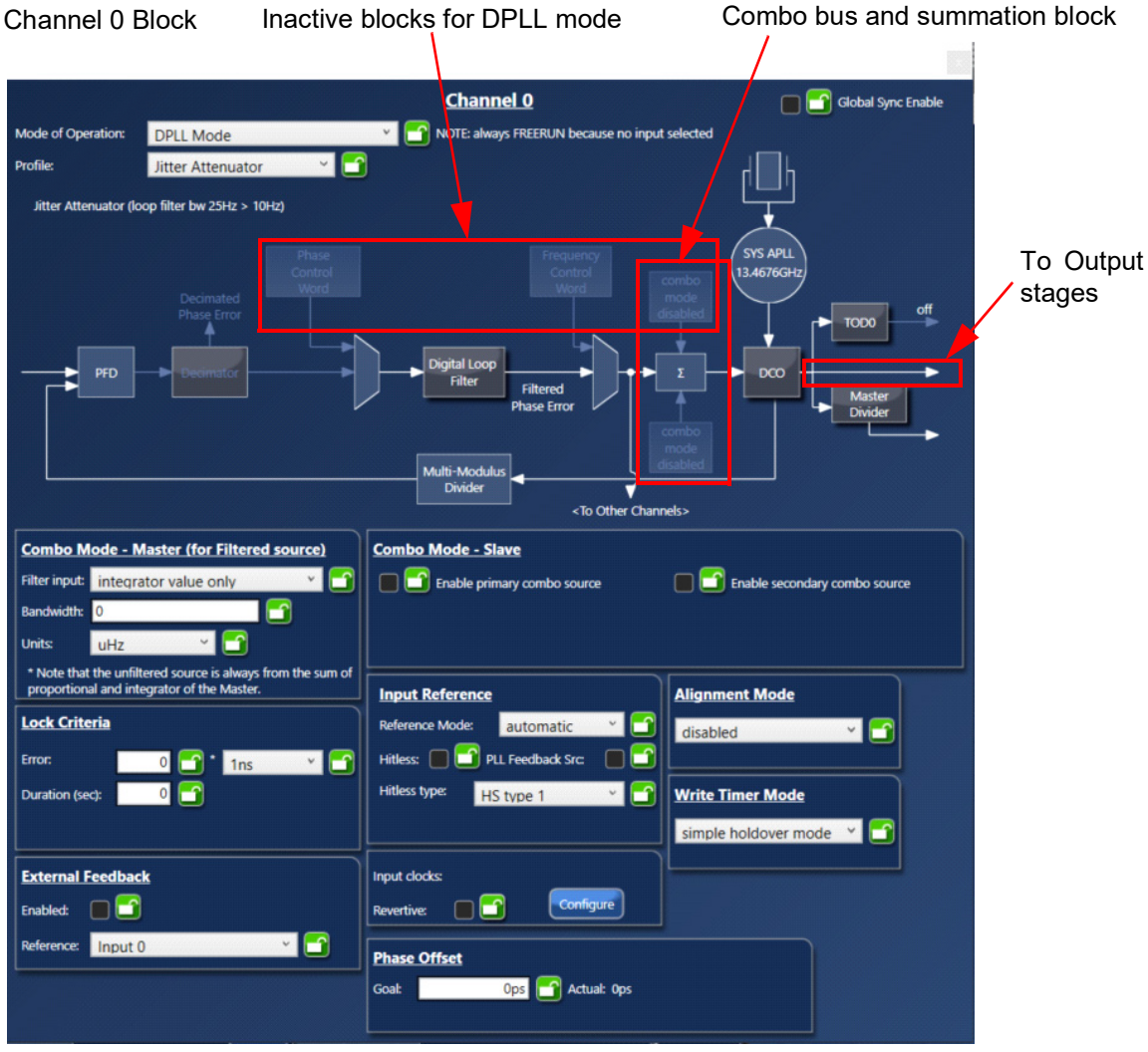


Figure 7. Channel Block Window (cont.)

2.4 Channel Modes

DPLL Mode:

- Acts as a jitter/wander attenuator
- Noisy input is filtered by a digital filter
- Output has low jitter/wander

DCO Mode:

- Used in 1588 applications
- PLL is open loop
- Can be controlled by a frequency step or a phase control word

Synthesizer Mode:

- Used for clock generation
- Only APLL/combo bus feeds the DCO
- No reference inputs, just crystal/XO input

Phase Measurement Mode:

- Measures the phase difference between two different reference inputs
- Channel still operates in synthesizer mode

2.4.1 DPLL Mode

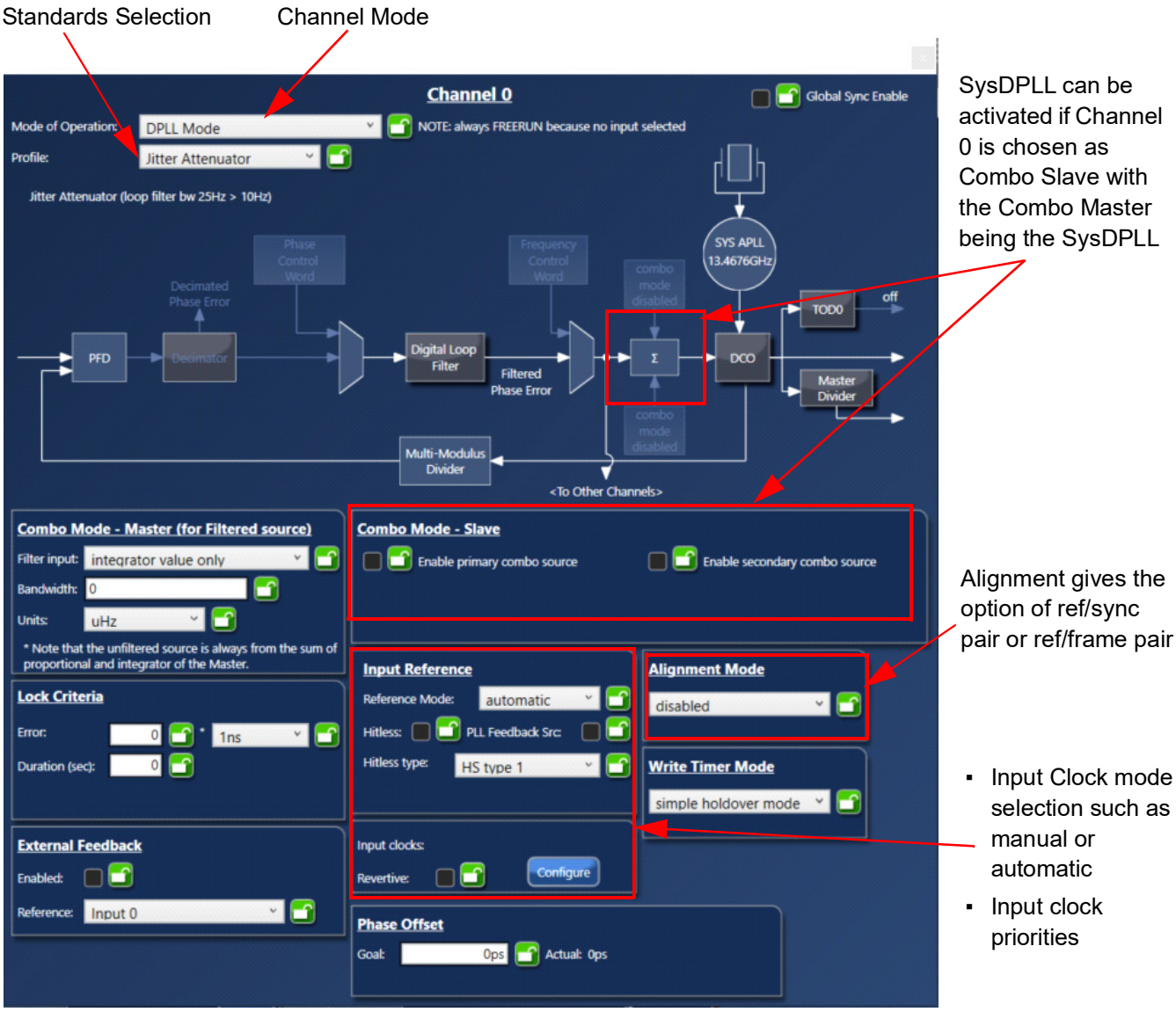


Figure 8. Channel Block Window – DPLL Mode

2.4.2 DCO Mode

DCO Mode

DCO control can be GPIO/Phase/ Frequency controlled

DCO control blocks are activated/ deactivated depending on selection

In 1588 mode, one channel can be in DCO mode (combo slave) and another channel in SyncE DPLL mode (combo master)

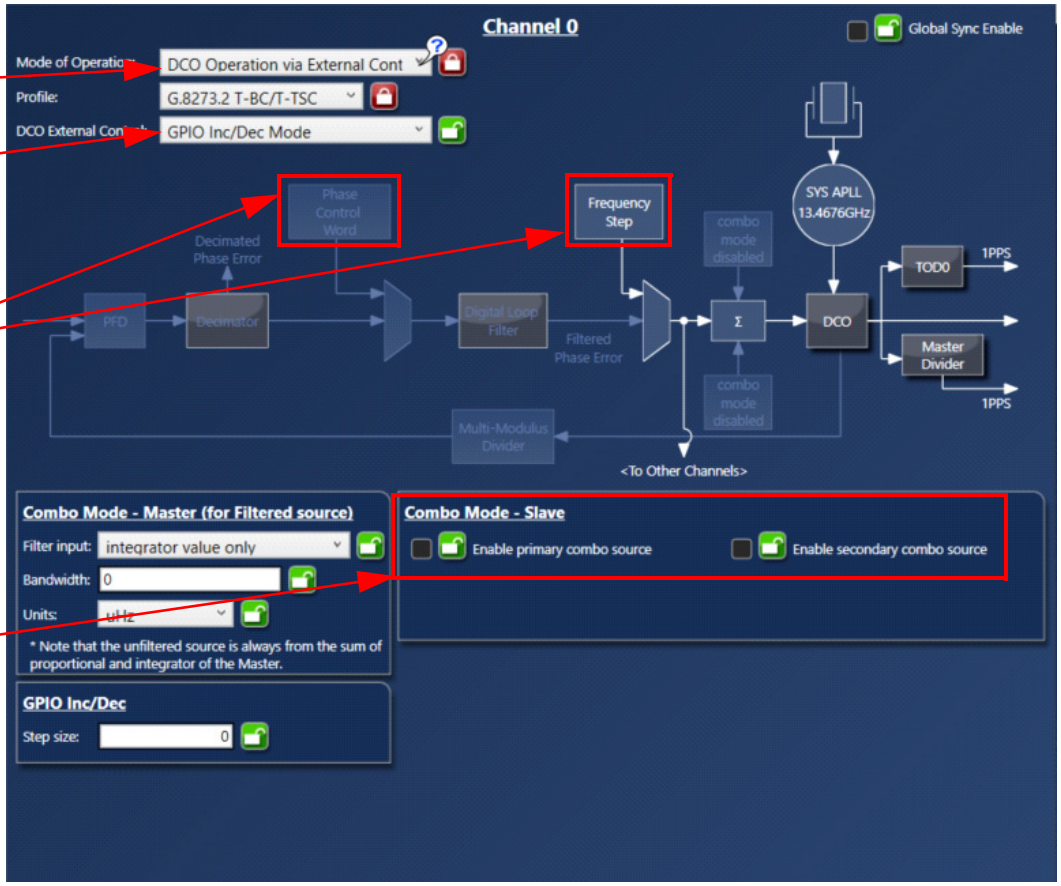


Figure 9. Channel Block Window – DCO Mode

2.4.3 Synthesizer Mode

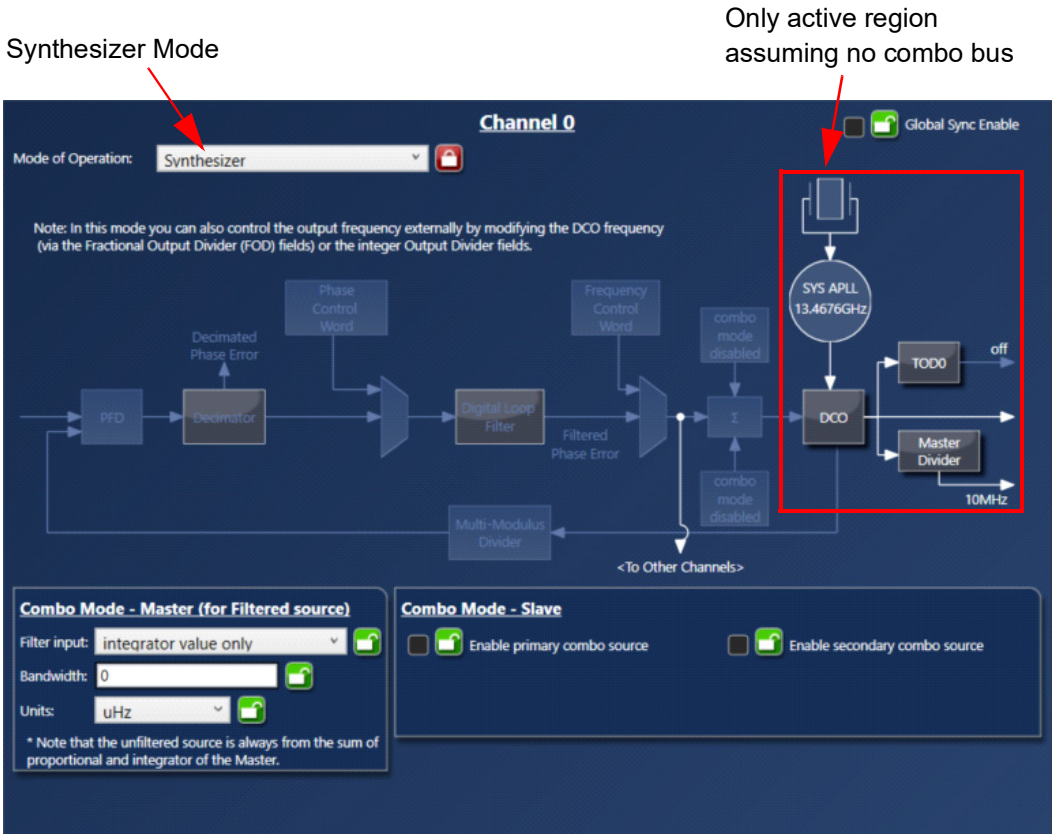


Figure 10. Channel Block Window – Synthesizer Mode

2.4.4 Phase Measurement Mode

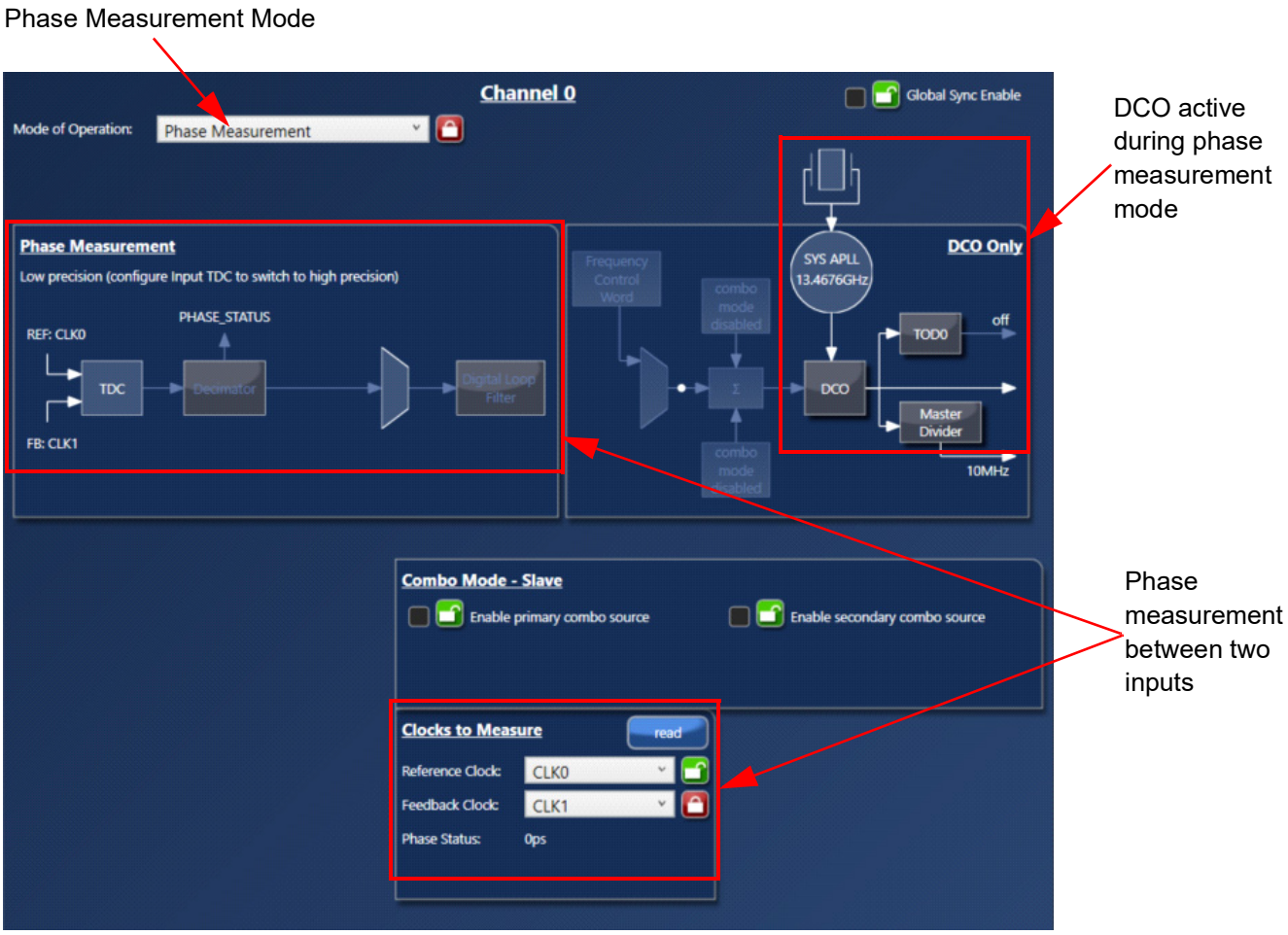


Figure 11. Channel Block Window – Phase Measurement Mode

2.5 System DPLL

- The output of this DPLL is the system clock (800MHz) that feeds the internal digital circuitry of the device (see Figure 12)
- The DCO output (800MHz) is not programmable
- System DPLL can be used as a frequency compensation DPLL for other DPLL channels using the combo bus
- By using a system DPLL as a combo master with a slave DPLL, the slave DPLL can use a lower loop bandwidth, thereby generating less jitter/wander
- It can only be a master using the combo bus
- Three modes are available:
  - TCXO/OCXO mode: TCXO/OCXO is the input reference of the System DPLL
  - System APLL mode: System DPLL is disabled and only the System APLL is active
  - Automatic mode: A non-TCXO/OCXO can be the reference of the System DPLL

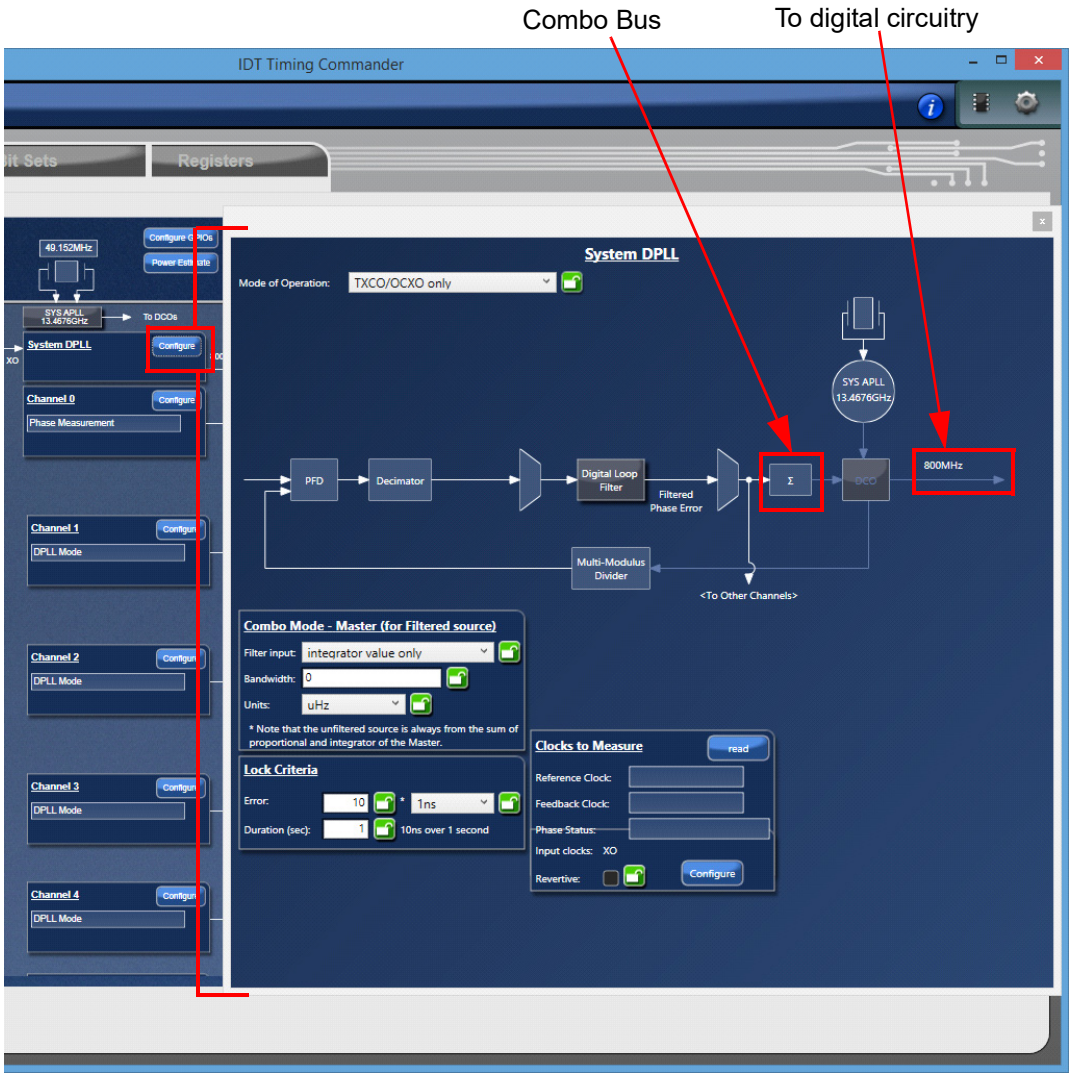


Figure 12. System DPLL Window

2.6 System APLL

- System APLL is an integer-N APLL (see Figure 13)
- The VCO can operate from 13.2GHz to 13.8GHz
- The crystal input ranges from 25MHz to 54MHz
- An input doubler is available making the possible input range from 50MHz to 108MHz
- Operating voltages are 3.3V and 2.5V
- The output of the system APLL feeds the DCOs and is used for clock synthesis by all of the Fractional Output Dividers (FODs) in the device
- To avoid integer boundary spurs on FODs, a user can adjust the FOD ratio, the doubler, or the feedback divider

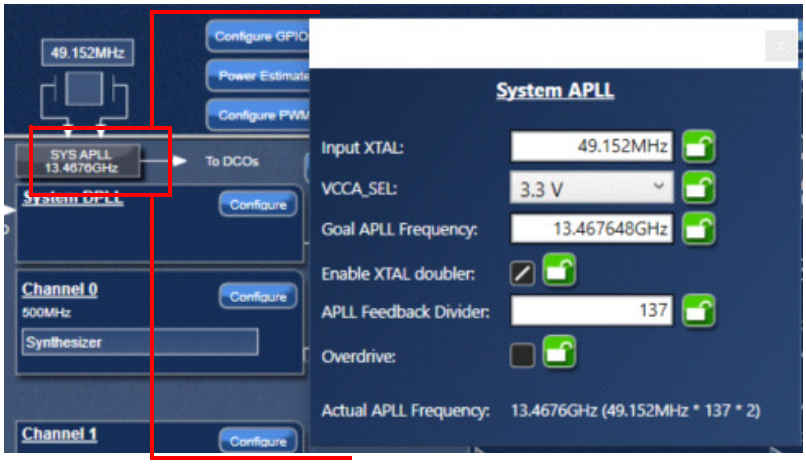


Figure 13. System APLL Window

2.7 Output Stages

- Up to 8 output stages, one stage for each channel (see Figure 14)
- Output stages 0:3 can drive two differential or four LVCMOS signals; LVCMOS P and N signals can be either in-phase or inverted
- Output stages 4:7 can drive one differential or two LVCMOS signals
- Output stages 4:5 or 6:7 can be driven by a single channel or they can be driven individually
- Frequencies from 0.5Hz to 1GHz (250MHz for LVCMOS)
- Output stage has an integer N divider
- The user must enter the desired output frequency (FOUT) first, then select differential or LVCMOS from the individual output boxes (Q0, Q1, Q2, etc)
- Once FOUT is entered, the internal frequency solver will adjust the DCO fractional divider and the integer divider from this stage to see if a solution exists

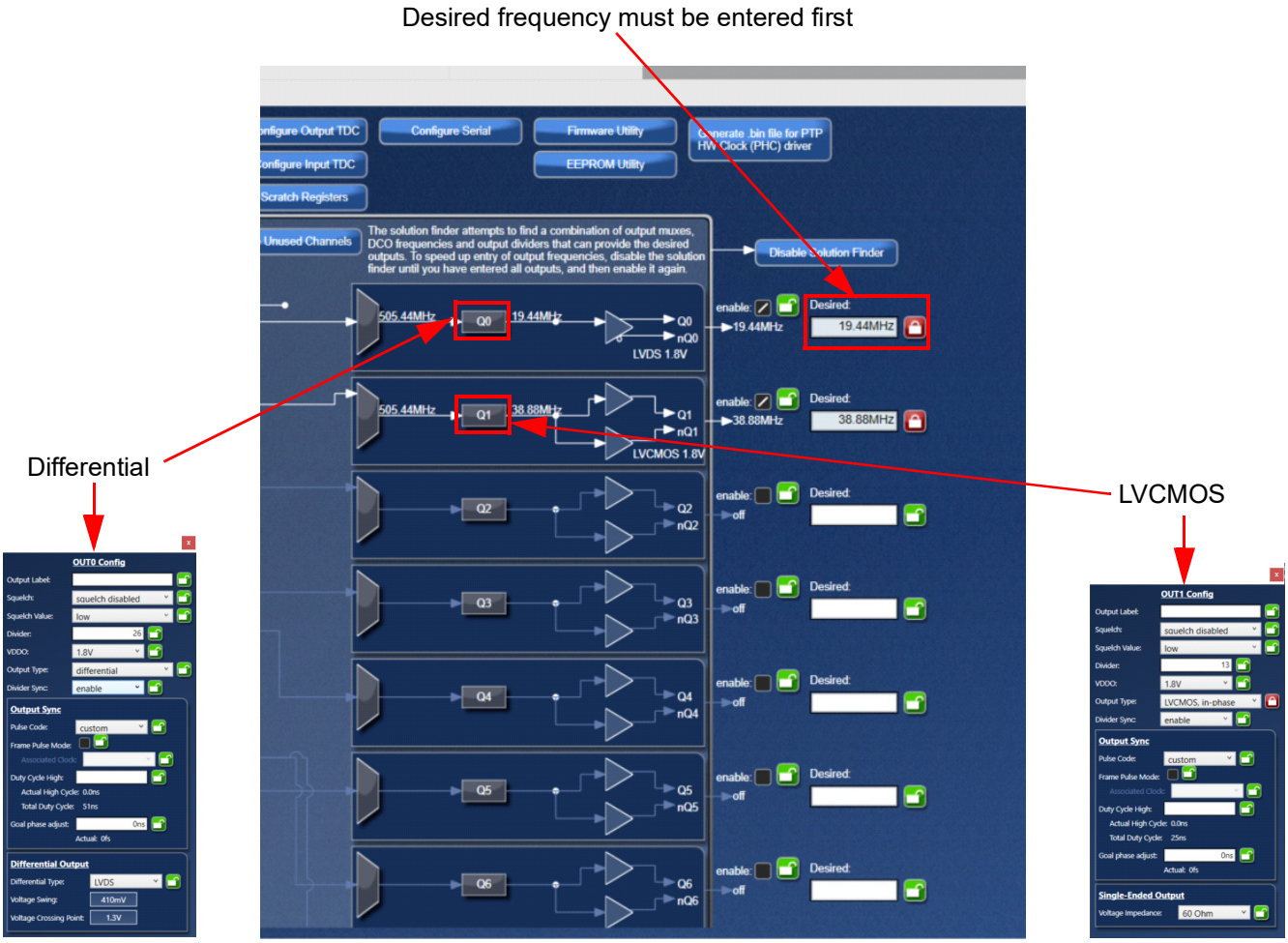


Figure 14. Output Stages Window

Refer to Figure 15 for the following Differential and LVCMOS signals configurations.

- Rail voltages can be 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V
- LVCMOS signals have a selection of different output impedance values (23Ω, 29Ω, 40Ω, or 60Ω)
- Differential signals have a selection of different output types (LVPECL, LVDS, or user defined)

- User-defined differential signals have access to different common-mode DC levels (0.9V to 2.3V in increments of 0.2V) and to different voltage swings (410mV, 600mV, 750mV, or 900mV) thereby supporting other output types such as SSTL, CML, HCSL, and HSTL
- Phase adjustment (ns granularity) and automatic output synchronization functions exist
- Duty cycle can be adjusted as a fraction of the Fractional Output Divider Frequency
- Squelch mode can be used to finish a clock cycle before maintaining a high or low level signal

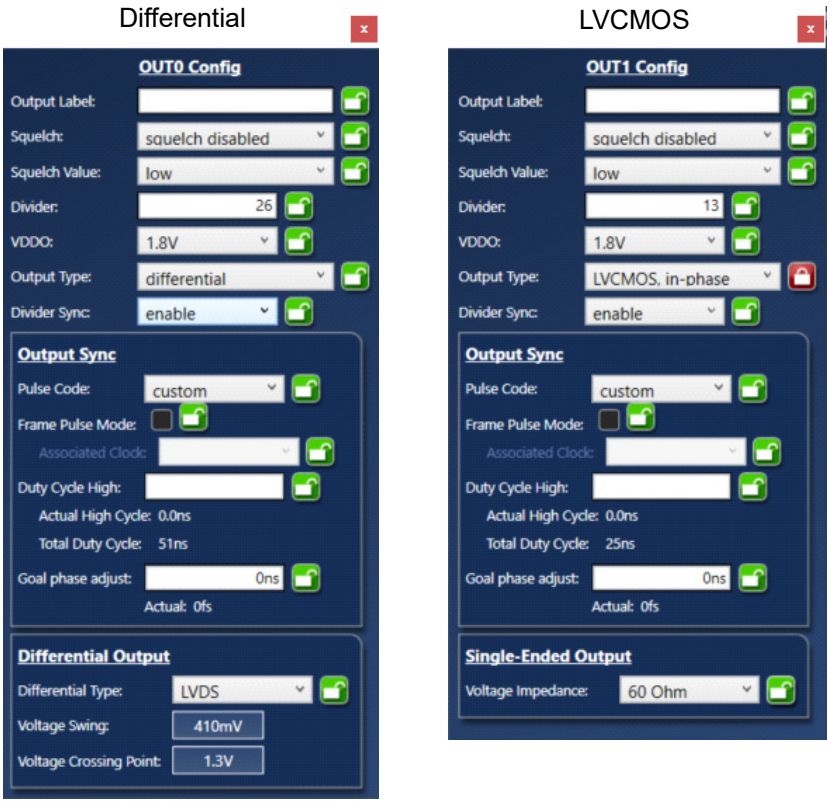


Figure 15. Output Stages – Differential and LVCMOS Signals Windows

2.8 Quick View Button

- This button enables quick access to all of the inputs, channels, and outputs (see Figure 16)
- Channel modes can be changed here
- Combo mode can be accessed here as well
- Input and output types are accessible
- DCO frequency and loop filter bandwidths are exposed here
- A copy function exists here that enables copying the contents of one DPLL to another DPLL

Figure 16. Quick View Button Window

2.9 Output Time-to-Digital Converter

- Output Timing-to-Digital Converters (TDCs) are digital phase detectors that have numerous applications (see Figure 17)
- One common application is output phase alignment between DPLLs
- For more information, see the *ClockMatrix Auto-Alignment of Outputs Application Note*

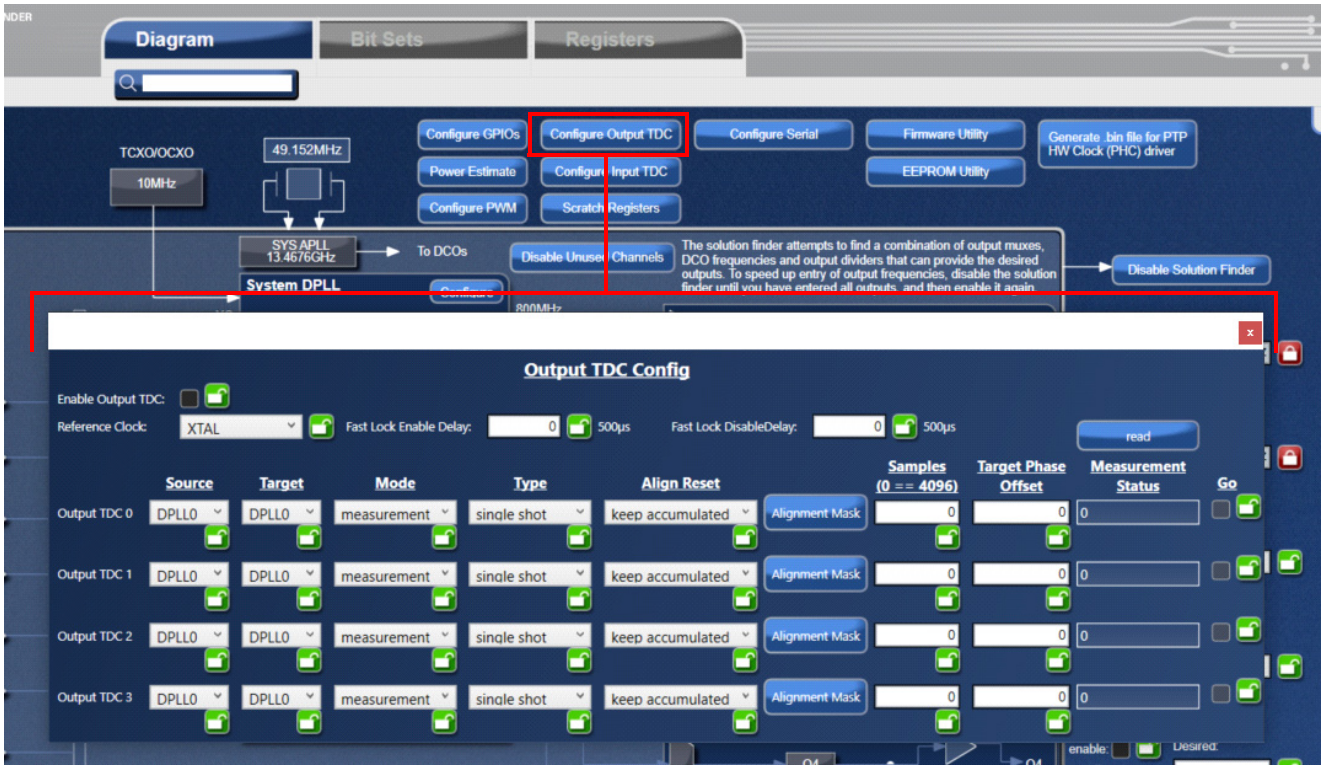


Figure 17. Output Timing-to-Digital Converter (TDC) Configuration Window

2.10 Configure GPIOs

- GPIO = General-Purpose Input / Output
- GPIOs enable the user to input signals to configure the device; they also output signals that help debug the device
- Rail voltage choices are 1.5V, 1.8V, 2.5V, or 3.3V
- I/O types are CMOS or Open Drain
- A maximum of 16 GPIOs are possible
- How to set up GPIO0 to control the clock selection for DPLL1 (see Figure 18):
  1. Click on the *Configure GPIOs* button to open the “GPIO CONFIG” dialog window.
  2. Enable a GPIO function.
  3. Click on the *edit* button to bring up the GPIO0 CONFIG dialog window. The GPIO Function is enabled.
  4. From the “GPIO Function” pull-down, select “manual clock select (in)”.
  5. Select the Clocks. CLK2 will be selected when GPIO0 is “High”.
  6. Select the affected DPLL.

Figure 18. GPIO Configuration Window

2.11 Power Estimate

- Power (current) calculator exists in the GUI to help estimate the power (see Figure 19)
- Both typical and maximum currents are included
- Current is separated by the different voltage pins and rails
- Voltage rails can be selected for even more accurate power calculations
- Power calculated is power dissipated on-chip only; off-chip power is not included

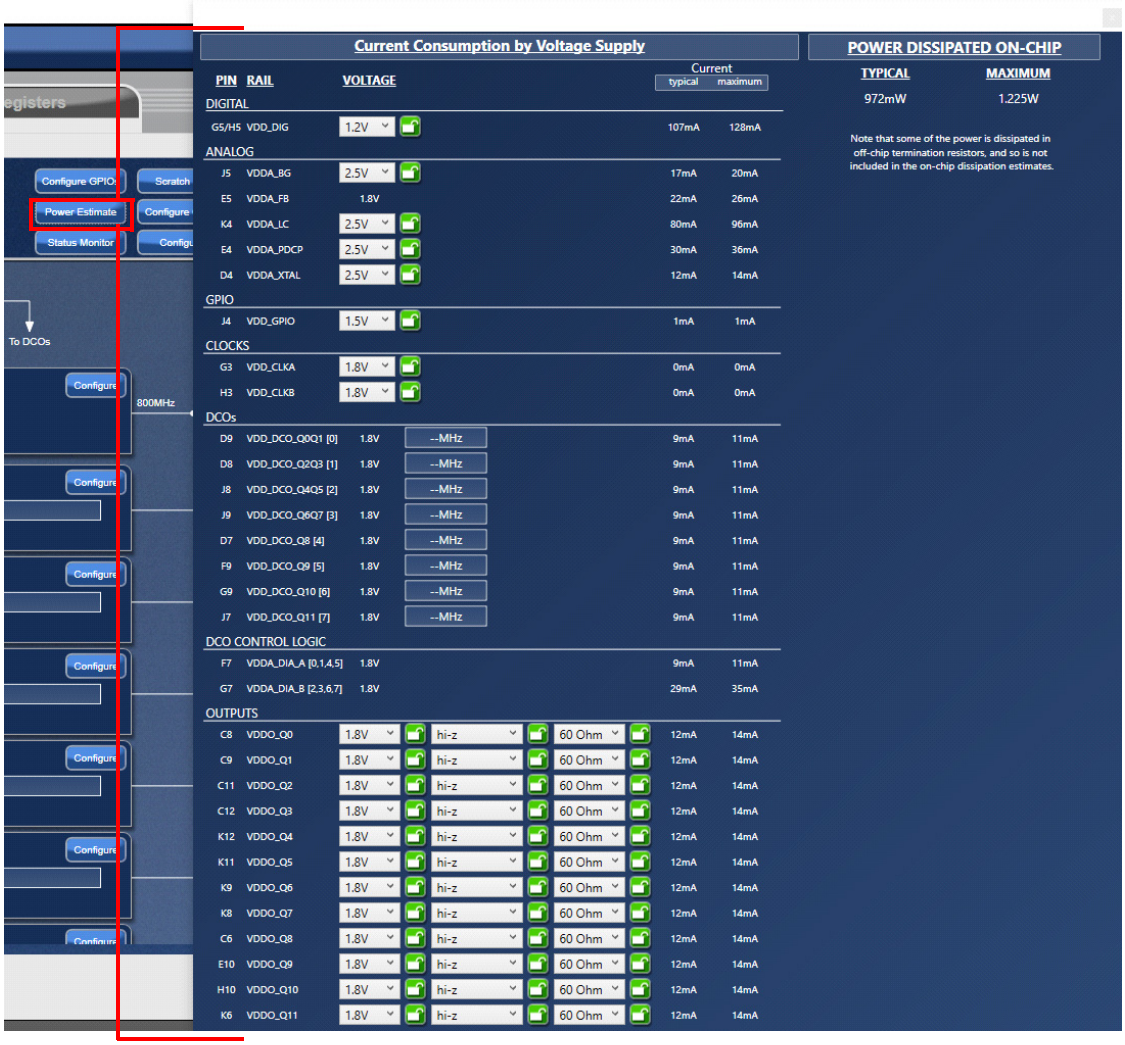


Figure 19. Power Estimate Window

2.12 Show Monitors

- Status Monitor button only appears when GUI is connected to the device (see Figure 20)
- Monitors exist for Inputs, DPLLs, System APLL, GPIOs, and Output TDCs
- Device must be polled to show monitor status (see Figure 20); auto-polling is possible but is not recommended due to the slow speed of the GUI
- Device provides both a “live” and a “sticky” status for each potential alarm condition
- A “live” bit shows the status of that alarm signal at the moment it is read; a “sticky” bit will assert when an alarm condition changes state and will remain asserted until the user clears it by writing to the appropriate clear bit

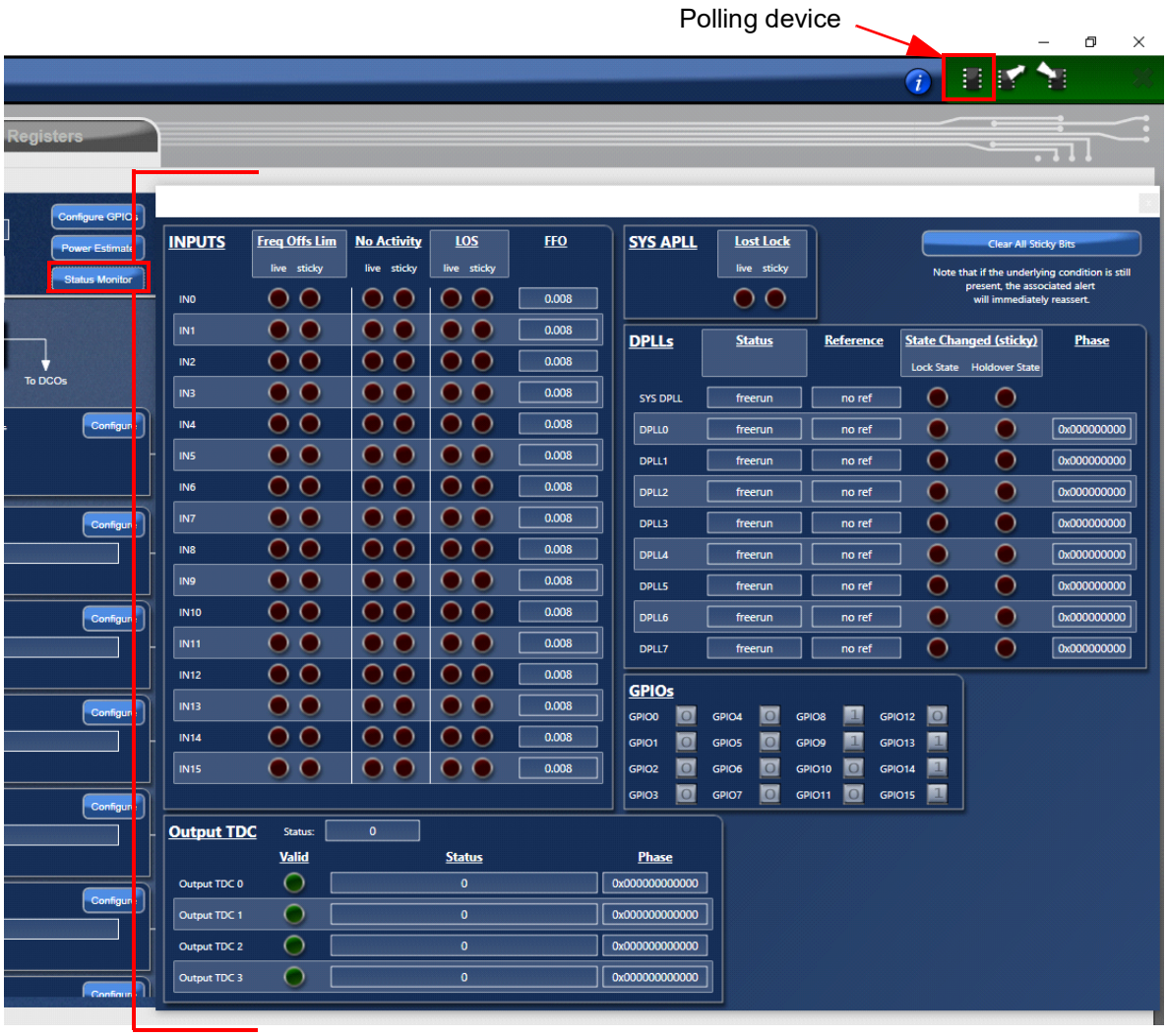


Figure 20. Show Monitors Window

2.13 Pulse Width Modulation (PWM)

- ClockMatrix has a feature called Pulse Width Modulation (PWM)
- It enables a clock signal to be pulse width modulated and also demodulated, so there are encoders and decoders (see Figure 21)
- One common application is to embed a 1Hz pulse on a clock signal (send one signal as opposed to two signals)
- See *ClockMatrix Pulse Width Modulation Overview Application Note*

Figure 21. Pulse Width Modulation Configuration Window

2.14 Time of Day (ToD)

- DPLL0 to DPLL3 are connected to a ToD counter, which is used to time-stamp external events (see Figure 22)
- Main application is for IEEE 1588
- See *Using an External Trigger for Loading/Latching ToD Application Note*

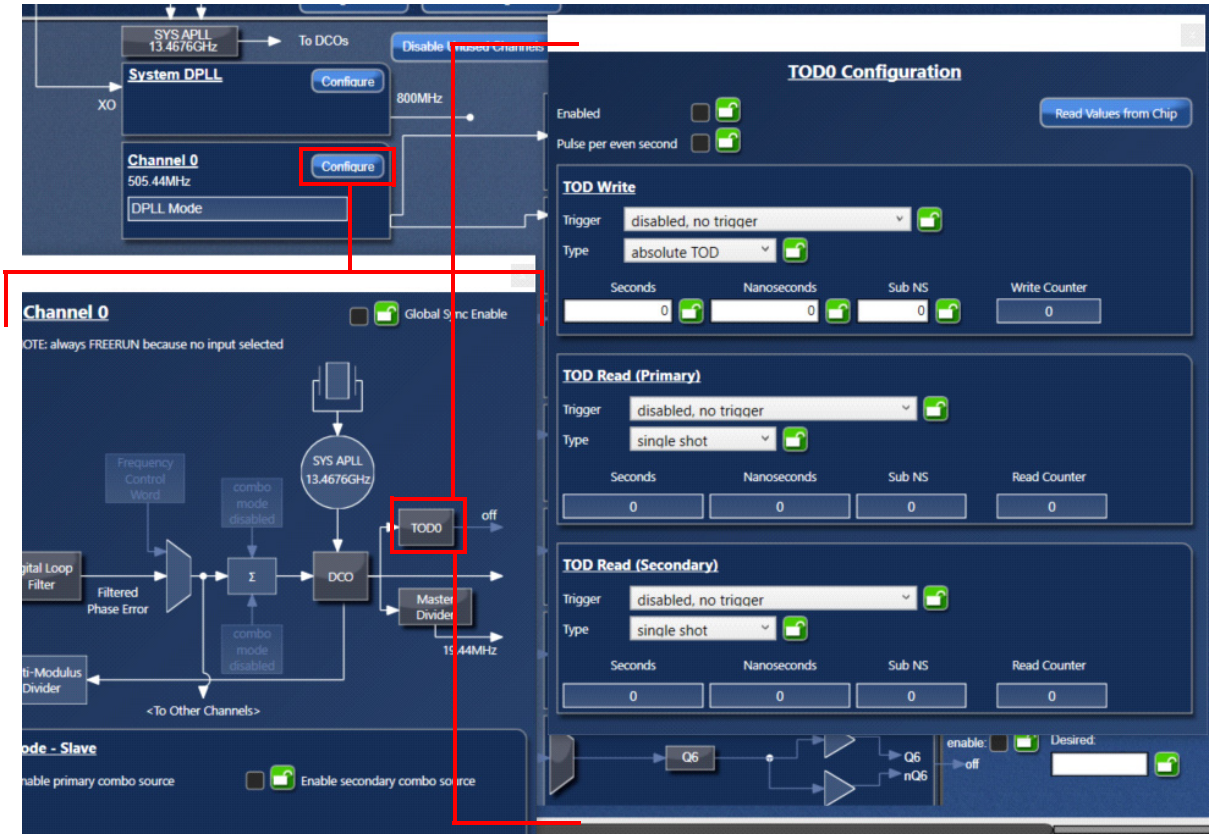


Figure 22. Time of Day (ToD) Configuration Window

2.15 Configure Serial Access

- Two serial ports exist in the device (see Figure 23)
- The device mode can be I2C or SPI or no change
- The address size is either 1-byte or 2-byte access
- All of the above information is saved in the TCS file and changes the device serial port access once a confirm code of 0x0A is written
- If the confirm code is not written, the device serial access will remain the default serial access based on the startup value of GPIO9
- **Warning**: If the serial port access is inadvertently changed, communication to the device will be lost

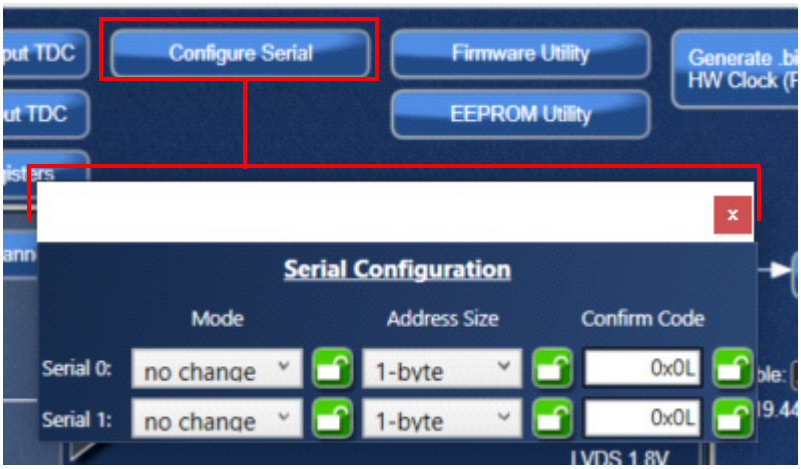


Figure 23. Serial Configuration Window

2.16 Firmware Utility and EEPROM

- Current firmware version of the device is output here (see Figure 24)
- If the firmware expected from the personality file loaded is different than the firmware version on the device, the device firmware can be updated by updating the RAM
- The external EEPROM on the board can be programmed here, given a HEX file
- Two types of EEPROM are possible (24×1024 and 24×1025)
- The *Generate EEPROM File* button can output a HEX file containing the config (.tcs) and the current firmware, which can then be used to program an EEPROM

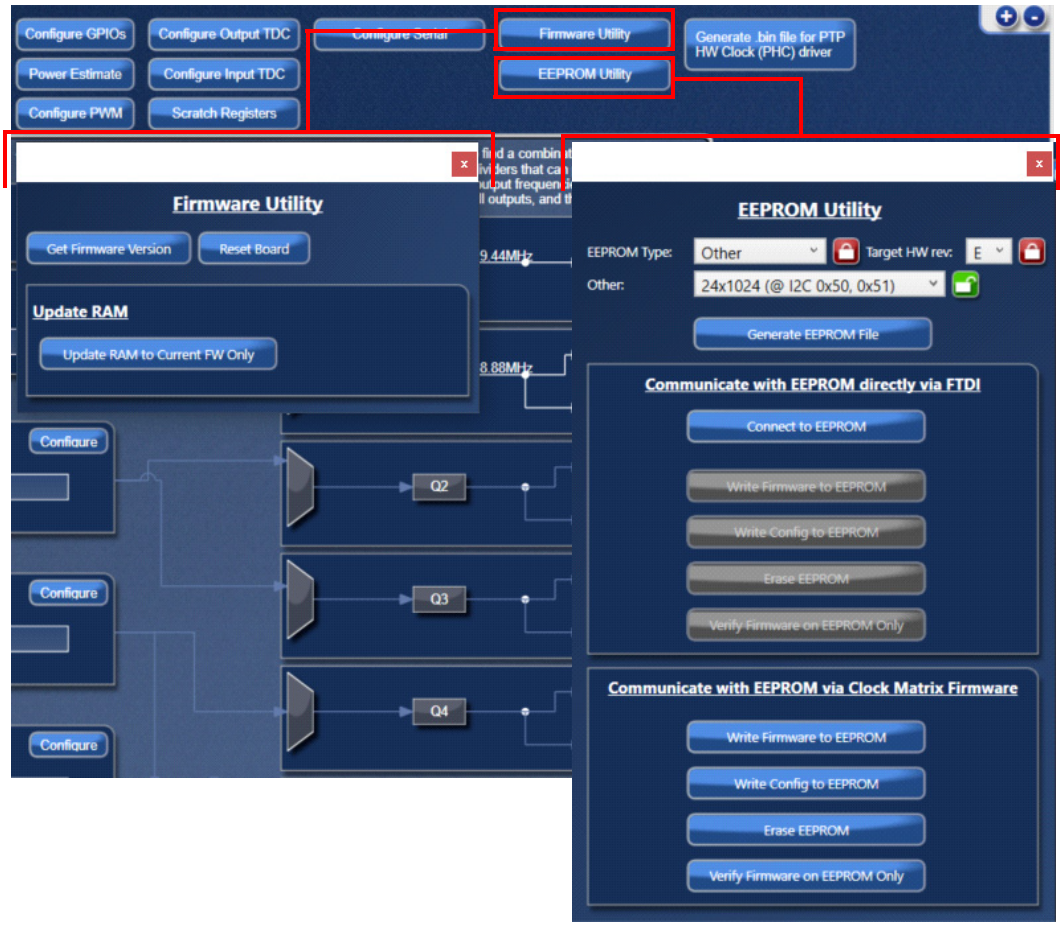


Figure 24. Firmware and EEPROM Utilities Windows

2.17 Bit Sets Tab

- The Bit Sets tab shows all of the customer visible register names and values (see Figure 25)
- Register descriptions are also shown on the right when a specific register name is clicked
- List view shows the register list alphabetically while tree view displays the register list by function
- Register list is searchable

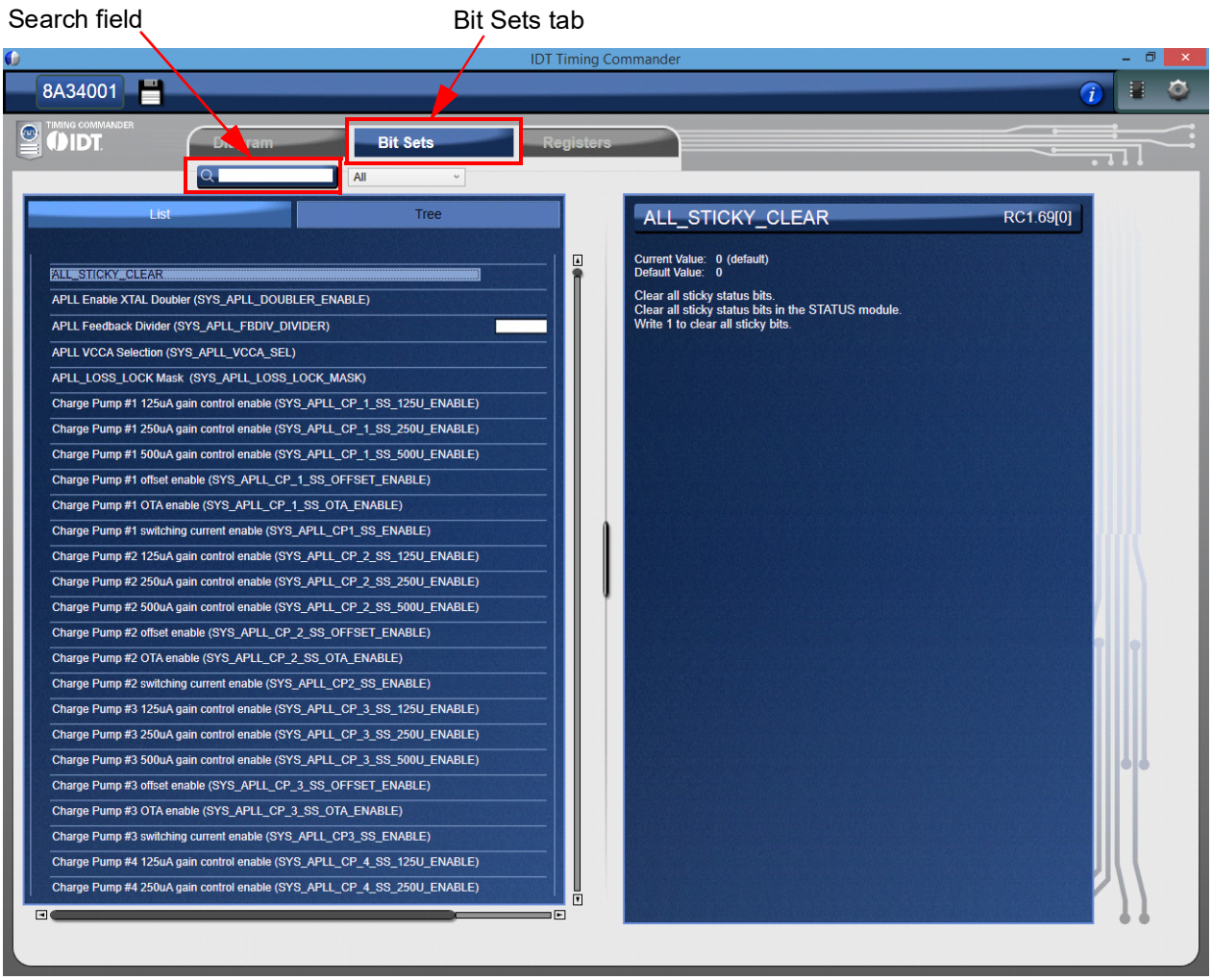


Figure 25. Bit Sets Tab Window

2.18 Registers Tab

- The Registers tab can be used to find a particular register by page and offset (see Figure 26)
- The individual bits and bytes can be modified here
- An entire register map can be imported here as well from a text file
- For proper addressing, see the 8A3xxxx Family Programming Guide

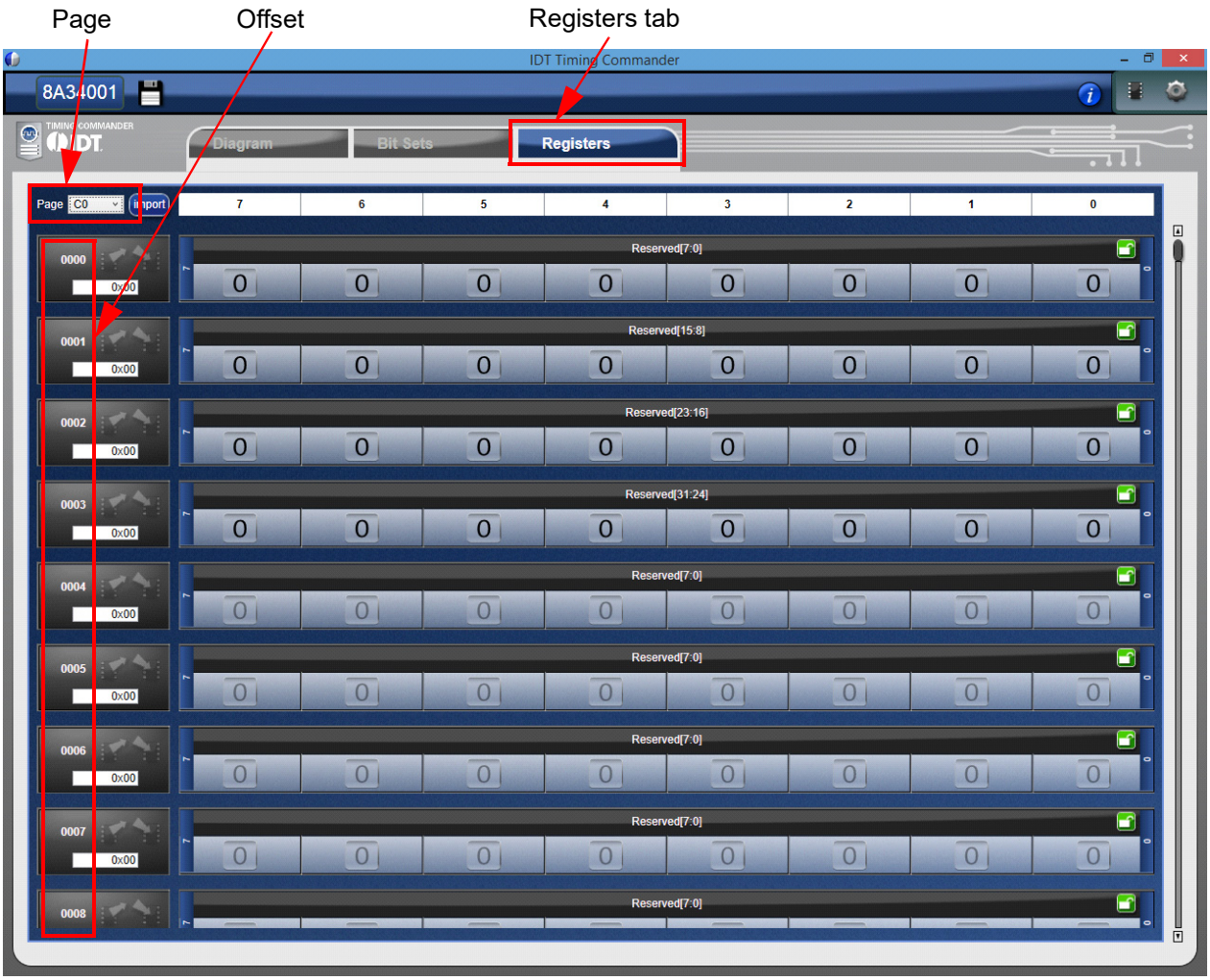


Figure 26. Registers Tab Window

2.19 File Management

- A configuration (.tcs) file can be loaded here or a new one can be created (see Figure 27)
- Both *Save* and *Save As* functions exist
- The entire register map can be exported in a table format
- Additionally, a programming file can be generated to be used by an Aardvark I2C or SPI controller

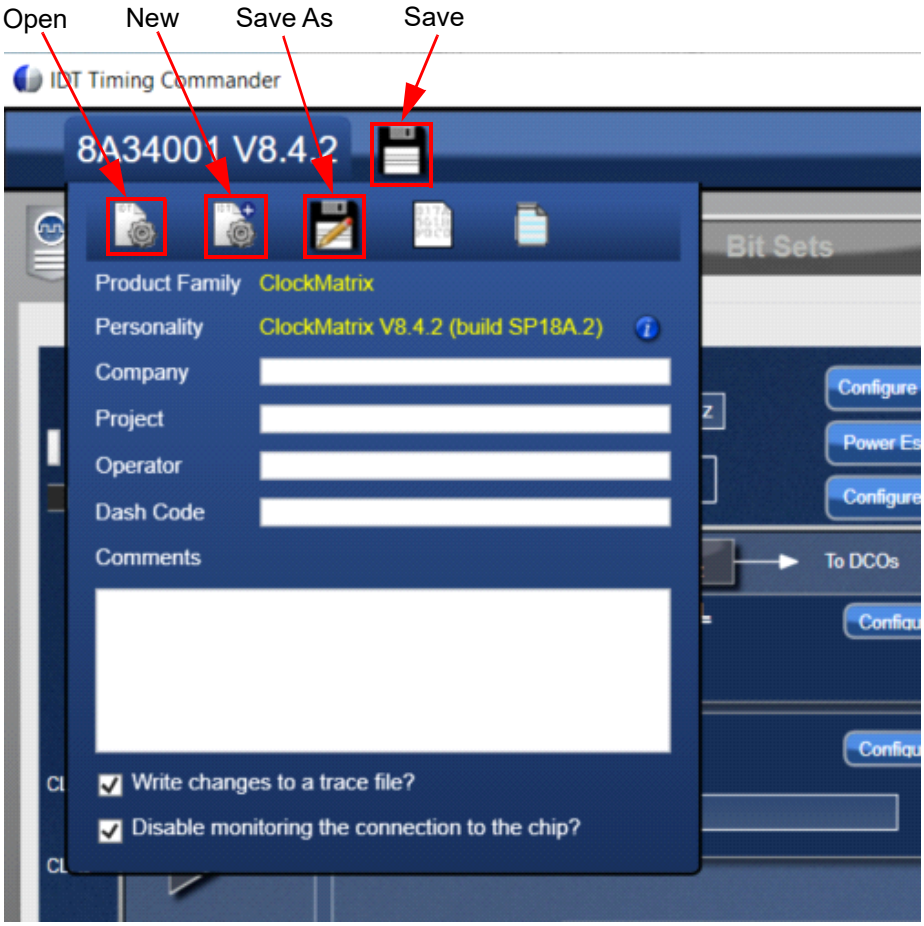


Figure 27. File Management Buttons

2.20 Exporting a Serial Stream

- Use the Export button of the GUI (see Figure 28)
  1. Browse for a location for the export.
  2. Choose the format (Generic, Register Map, or Aardvark).
  3. Choose “SPI” or “I2C”.
  4. Choose “Non Default” to only show modified registers.
  5. Choose either “One Byte” or “Two Byte” addressing.
  6. Check the box to include trigger registers.
  7. Click *OK*.

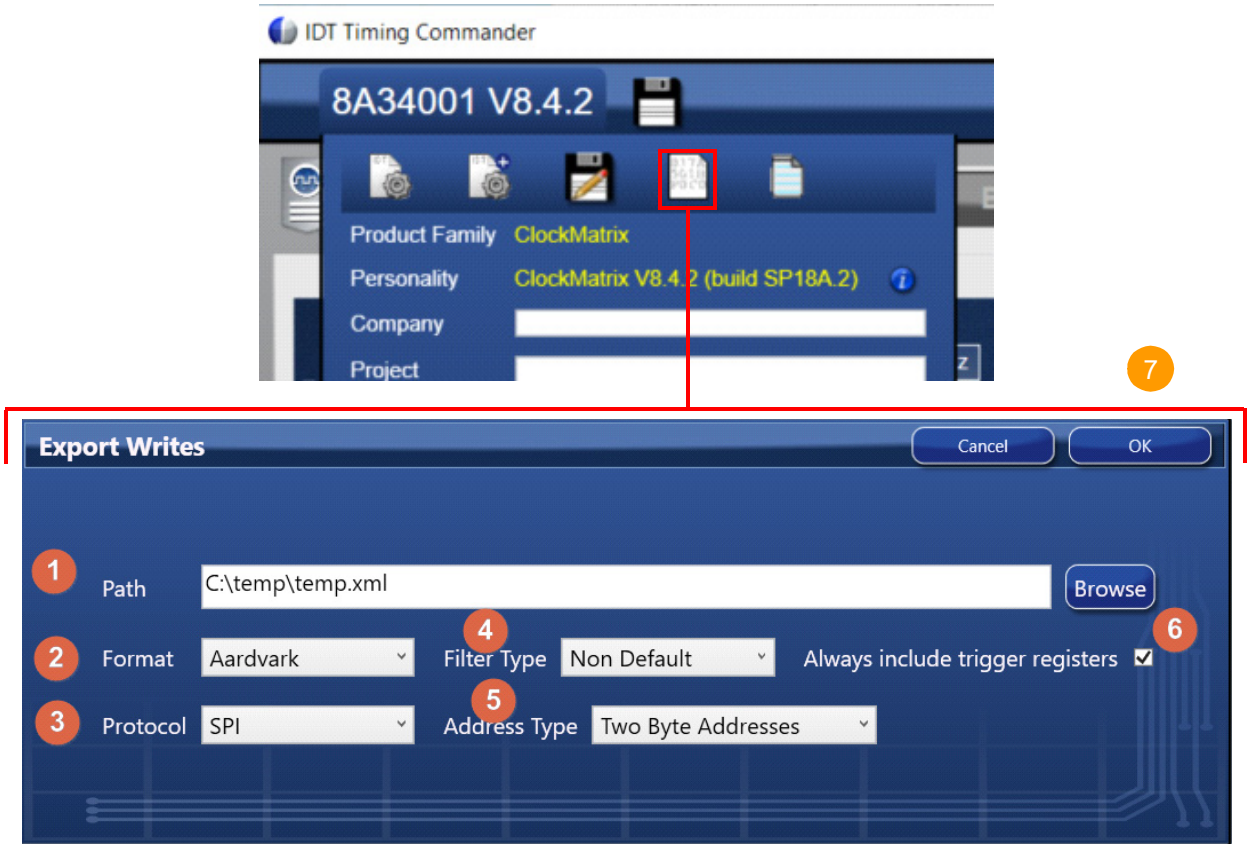


Figure 28. Export Button and Export Writes Window

2.21 Connection Settings

- The device can be communicated via I2C or SPI (see Figure 29)
  - One byte or two byte addressing is supported through the GUI
- The microchip button must be pushed to write or read from the device (see Figure 29)
  - Auto-polling is possible when reading the device, but is not recommended due to the slow speed of the GUI
- The "*i*" button gives version and build info of the GUI. It also outputs logging information (see Figure 29):
  - Logging information is stored in an .sil file
  - The .sil file contains all GUI error messages. It also contains logging information about what the user did to create the .tcs file

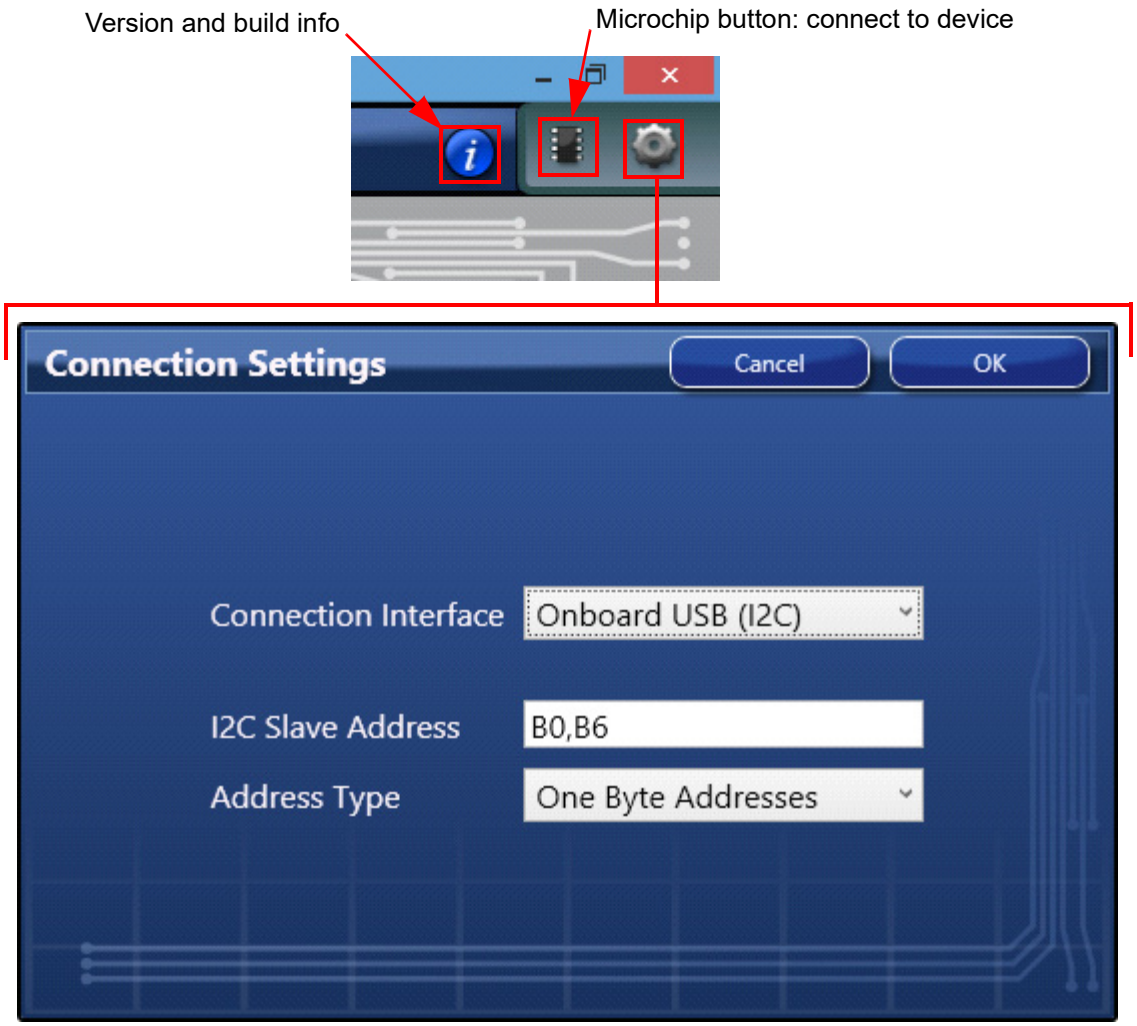


Figure 29. Connection Settings Window

3. Configuring a Channel – Example

The example in this section will demonstrate the step-by-step process of configuring a channel in jitter attenuator mode with the following:

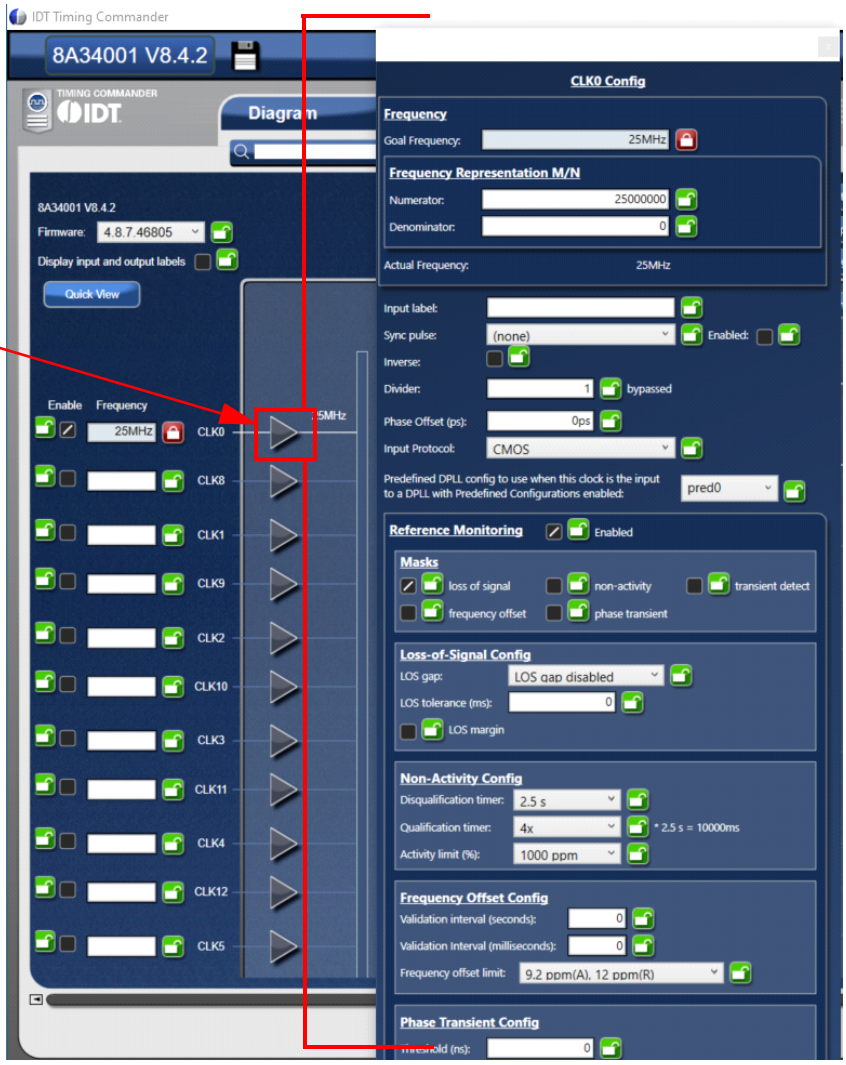
- 25MHz input LVPECL
- Loop bandwidth of 10Hz
- 156.25MHz output LVPECL

3.1 Step 1: Input Frequency

- Point to CLK0 white box with mouse
- Enter 25MHz in the white box
- Push Enter

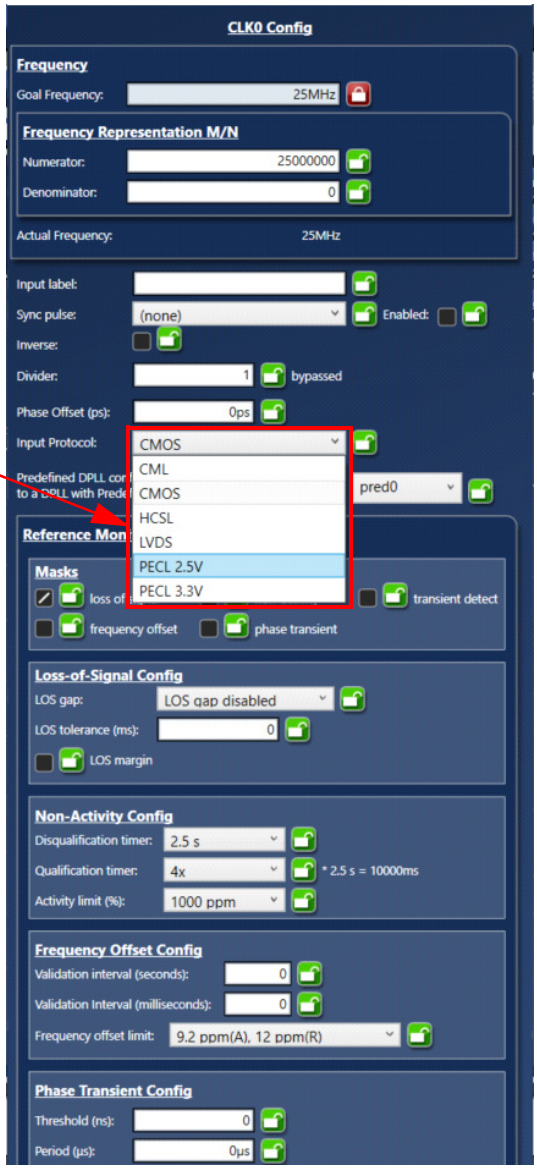
3.2 Step 2: Input Stage

Click on input stage to open sub-window



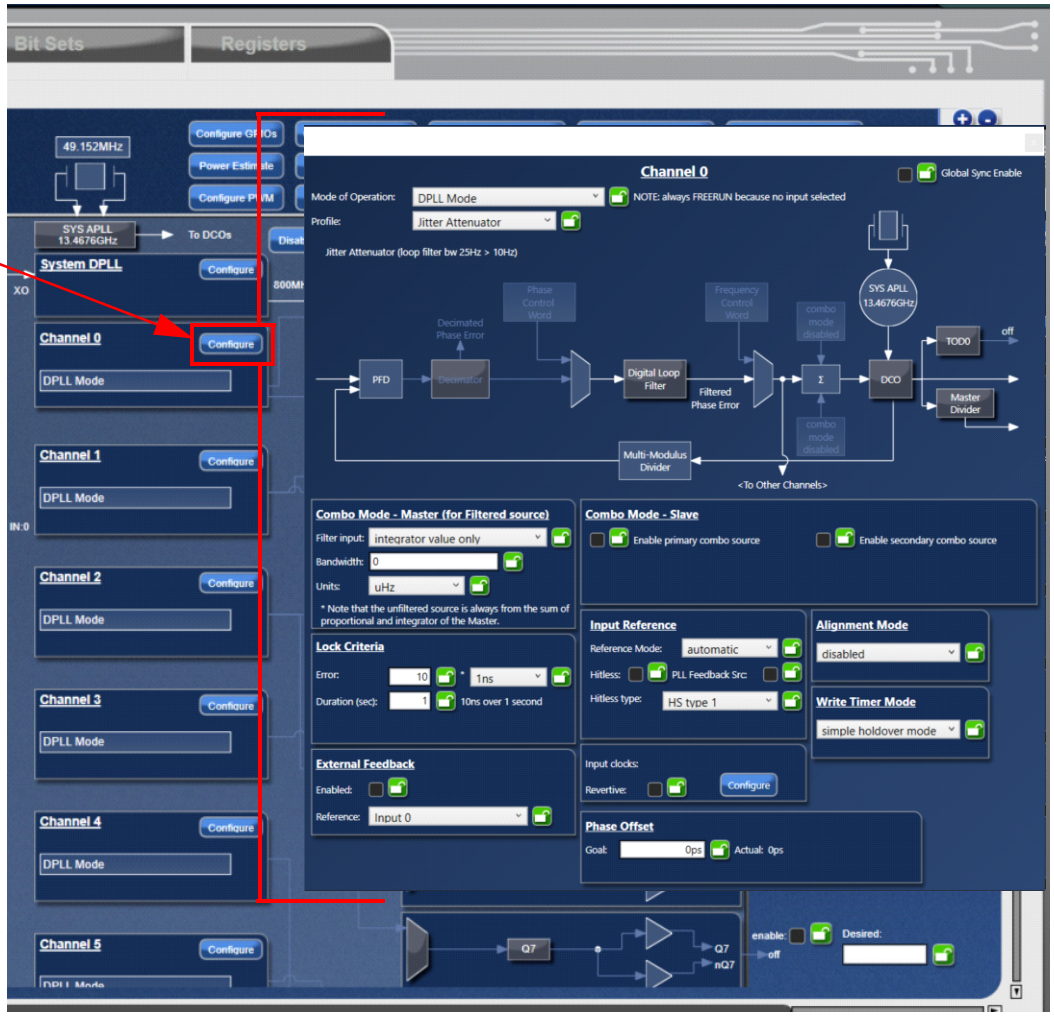
3.3 Step 3: LVPECL Input

- Choose PECL 2.5V from the drop-down menu
- Close window



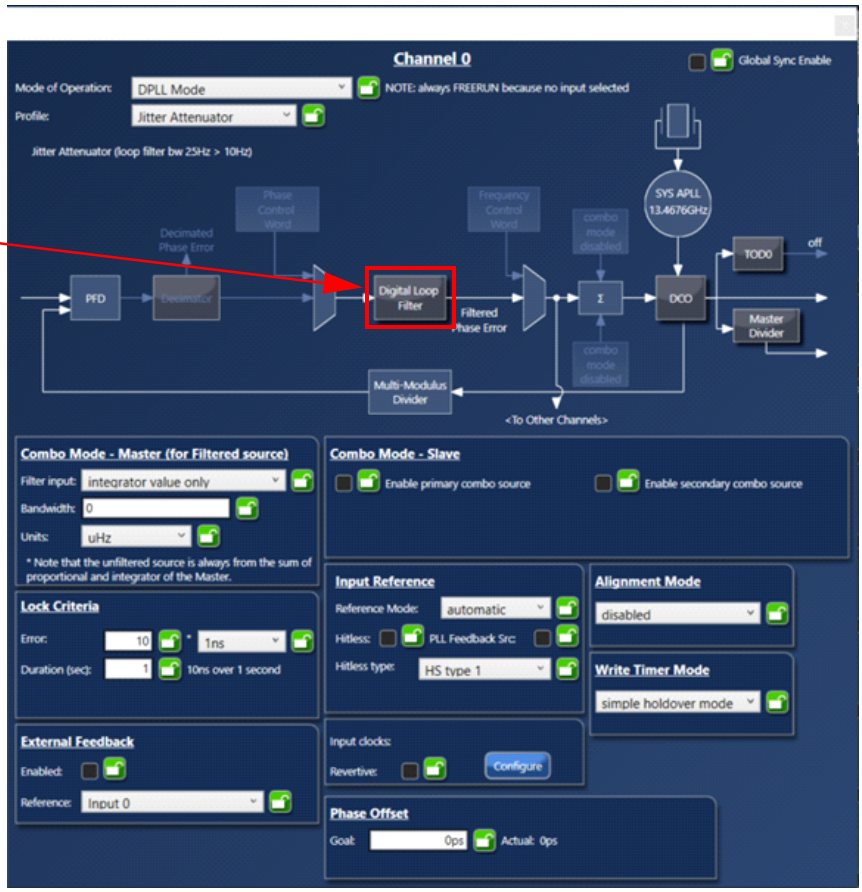
3.4 Step 4: Channel 0

Click on Channel 0 Configure button to open the Channel Block sub-window



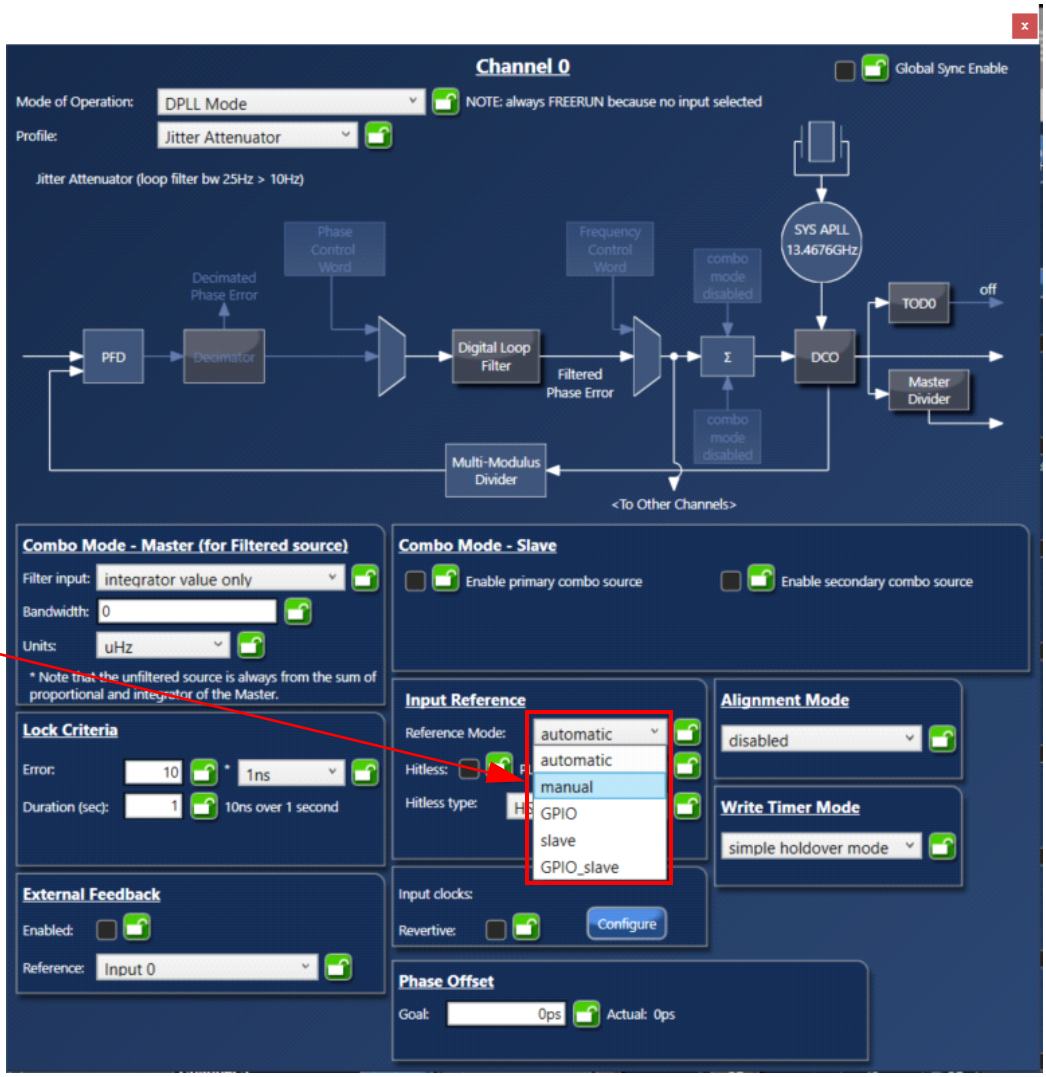
3.5 Step 5: Digital Loop Filter

Click on Digital Loop Filter button



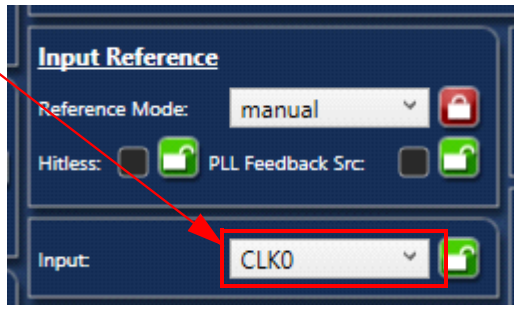
Change Loop Bandwidth to 10Hz

3.6 Step 6: Input Reference Mode

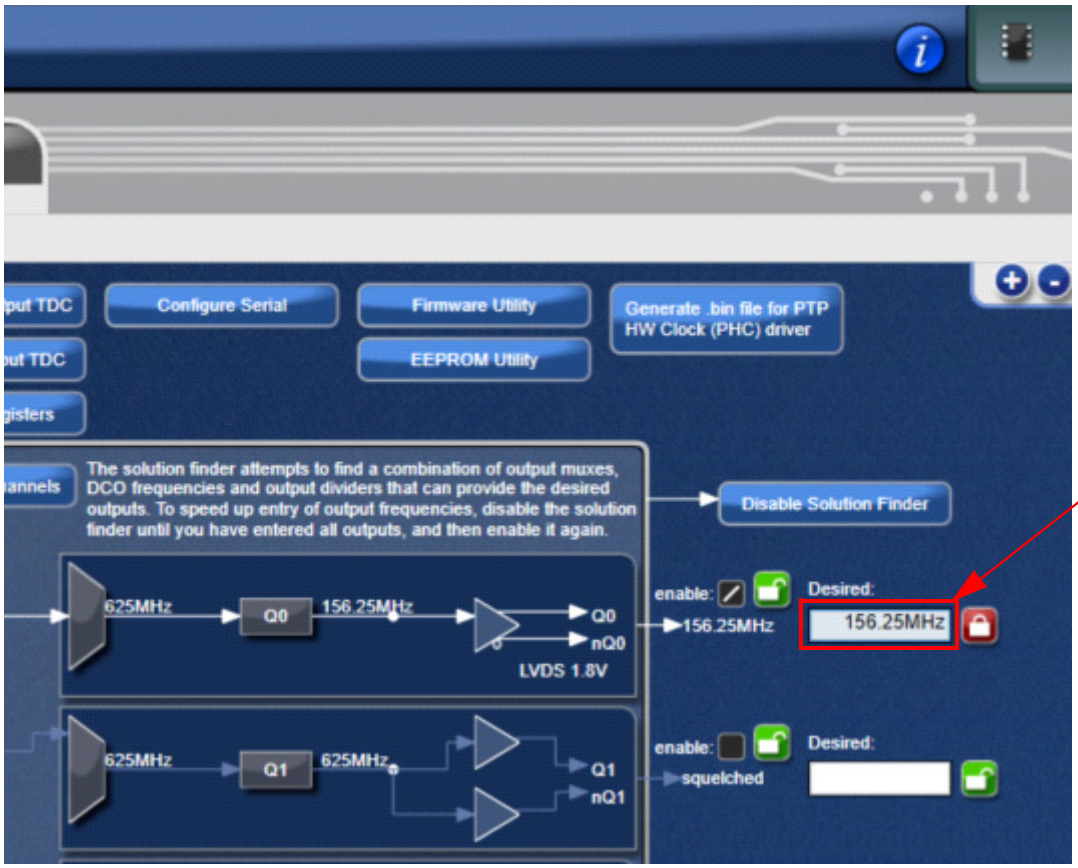


Change to manual

- Select CLK0
- Close sub-windows



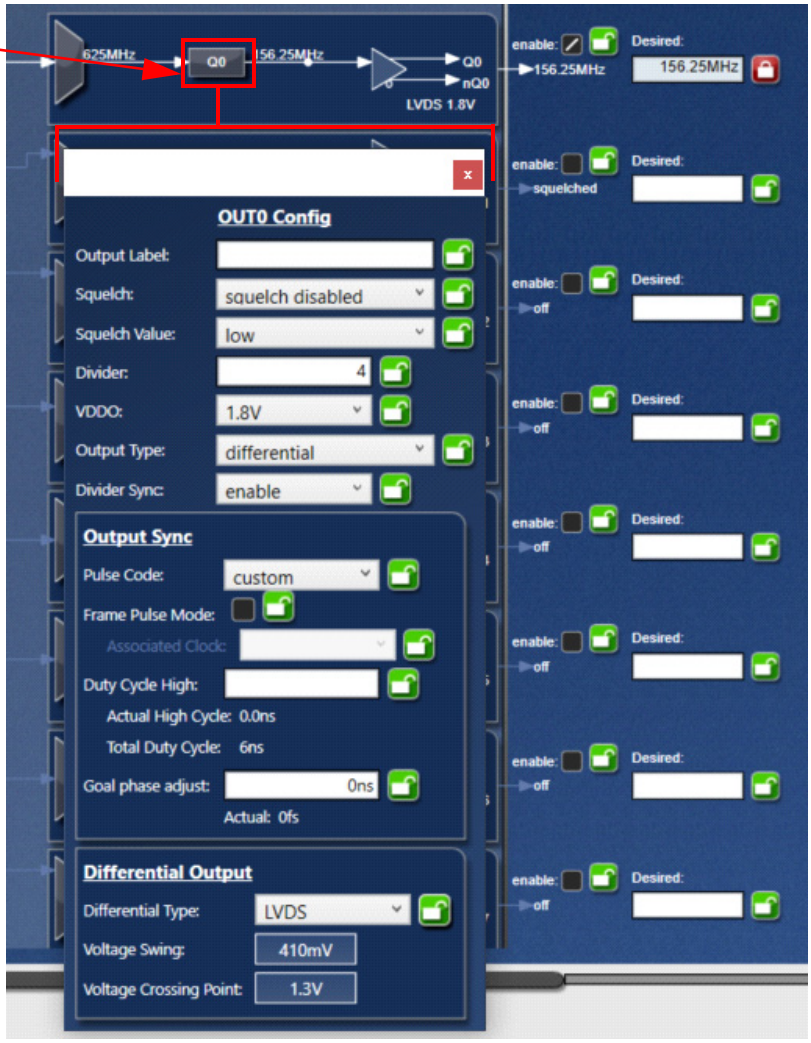
3.7 Step 7: Output Frequency



- Point to Q0 white box with mouse
- Enter 156.25 MHz in the white box
- Push Enter

3.8 Step 8: Output Stage

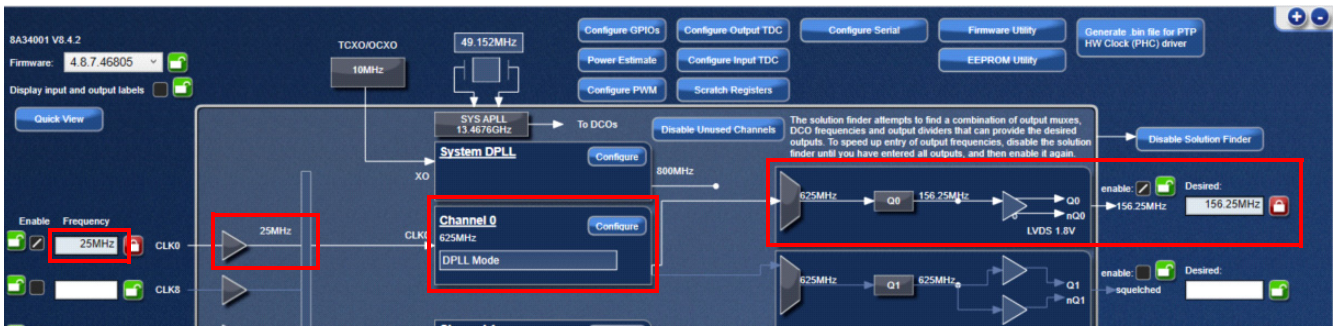
Click on output stage to open OUT0 Config sub-window



3.9 Step 9: LVPECL Output

- Choose LVPECL 2.5V from the drop-down menu
- Close window

3.10 Step 10: Channel Configuration Completed



4. Revision History

Revision	Date	Description
1.0	Jun 29, 2021	Initial release.

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