## How to Use this Document

The 8A3xxxx Family Programming Guide contains information on how to access internal registers and what those registers do in detail for all devices in the 8A3xxxx family. Not all devices in the family support all the same features or quantities of logic blocks, however the register blocks all behave and are addressed at the same locations in all device. Some devices will not make use of all register blocks since the associated feature or block of circuitry may not be available in that particular device. A Programming Guide Addendum for each specific device will indicate which register modules are support in that device.

In addition, there are several other pieces of documentation that describe specific functions or details for the family or individual devices. Table 1 shows related documents.

Table 1: Related Documentation for Devices in the 8A3xxxx Family

| Document Title | Document Description |
|---|---|
| <device name> Datasheet | Contains a functional overview of the device and hardware-design related details including pinouts, AC & DC specifications and applications information related to power filtering and terminations. |
| <device name>-<dash code> Datasheet Addendum | Indicates pre-programmed power-up / reset configurations of this specific 'dash code' part number |
| 8A3xxxx Family Programming Guide (v4.8) | Contains detailed register descriptions and address maps for all members of the family of devices. Please check the <device name> datasheet to check the version used by that device. All devices that use this version number use some subset of this register map, as indicated in their device-specific Programming Guide Addendum document.. |
| Evaluation Board Reference Manual | Describes the Evaluation Board. Evaluation boards are available for the 8A34001 (144BGA) or 8A34002 (72QFN) devices. These devices contain a superset of the functionality available in all other members of the 8A3xxxx Family. So they can serve as evaluation tools for any of the less fully-featured family members. |
| Timing Commander Personality User Manual | Detailed description of how to use IDT's Timing Commander configuration tool. At this time, a personality file is only available for 8A34001. This personality contains a superset of the functionality available in all other members of the 8A3xxxx family. Since all members of the 8A3xxxx family share register locations and resource numbering, configurations generated using the 8A34001 personality can be used in any member of the 8A3xxxx family. Functionality that is not available on the other family members will of course not respond to any configuration of it that is made. |

This document discusses the registers supported by a particular version of the Firmware (FW) running on the internal micro-controller within the 8A3xxxx family of devices. Register maps may change between major releases of the FW, so please check the Revision History section of this document to ensure this document aligns with the FW revision being used on the device. FW version numbering follows the format:

v<major release number>.<minor release number>.<hotfix number>

This document is divided into several sections:

- Introduction (this section) - describes documentation structure for the 8A3xxxx
- Serial Port Overview - repeating selected information from the 8A3xxxx Datasheet to discuss how the serial ports function, overall device memory map and register addresses
- I2C Slave Operation - discusses register accessing topics related to $I^2C$ operation on a serial port
- SPI Operation - discusses register accessing topics related to SPI operation on a serial port
- Register Table Overview - discusses register table format and abbreviations
- Register Set Descriptions - describes a set of registers that is made available for users to quickly and simply access the commonly-used features of the 8A3xxxx.
- Revision History
- IDT Contact information

# Serial Port Overview

The 8A3xxxx family supports up to three serial ports. One is a dedicated I²C Master port used for loading configuration data at reset, and the other two are configurable slave I²C or SPI ports that can be used at any time after the reset sequence has completed to monitor and/or configure the device. In some variants of the device, the I²C Master port share pins with an I²C slave port.

Operation of the I²C Master Port is only used by the device to access an external serial EEPROM and so this is not relevant to device programming.

Two slave ports have been provided to allow independent access to any of the device's internal registers. This allows high-priority accesses not to be queued behind lower priority ones on a shared external serial interface. Note that internal to the device, both slave serial ports access a single instance of each register over a shared internal bus. The device ensures that a burst access on one bus will complete atomically once begun, before the other port can gain access to the shared internal bus or registers. However it does not guarantee the order in which the two serial ports will be granted access to any shared resource.

Please refer to the appropriate section below for details on the operation of the slave I²C or SPI ports.

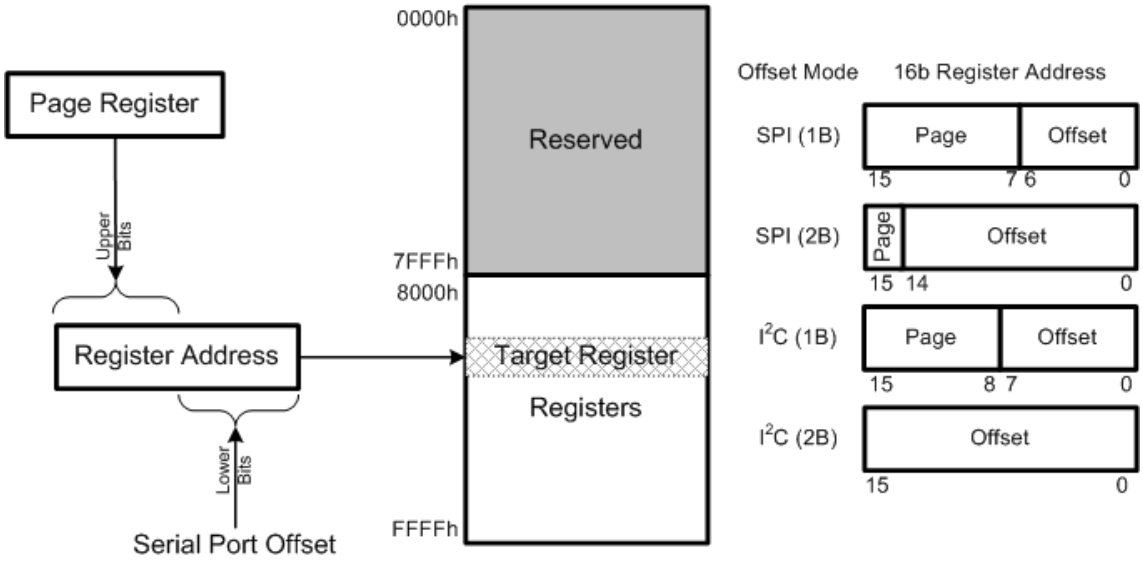
Either slave port can be reconfigured over either serial port at any time by accessing the appropriate registers. This includes both configuration options with each protocol or switching between protocols (I²C to SPI or vice versa). However it is recommended that the full operating mode configuration, including page sizes for registers, for each serial port be set in the initial configuration data read from OTP or external EEPROM (see Device Initial Configuration in the 8A3xxxx Datasheet for details).

## Addressing Registers within a Device

The address space that is externally accessible within the device is 64k bytes in size, and therefore needs 16-bits of address offset information to be provided during slave serial port accesses. Of that 64k bytes, only the upper 32k bytes contains user accessible registers.

The user may choose to operate either serial port providing the full offset address within each burst, or to operate in a paged mode where part of the address offset is provided in each transaction and the other part comes from an internal page register in each serial port. The decision may be made independently on each slave serial port and each slave serial port has its own page register to avoid conflicts. Figure 1 shows how page register and offset bytes from each serial transaction interact to address a register within the 8A3xxxx.

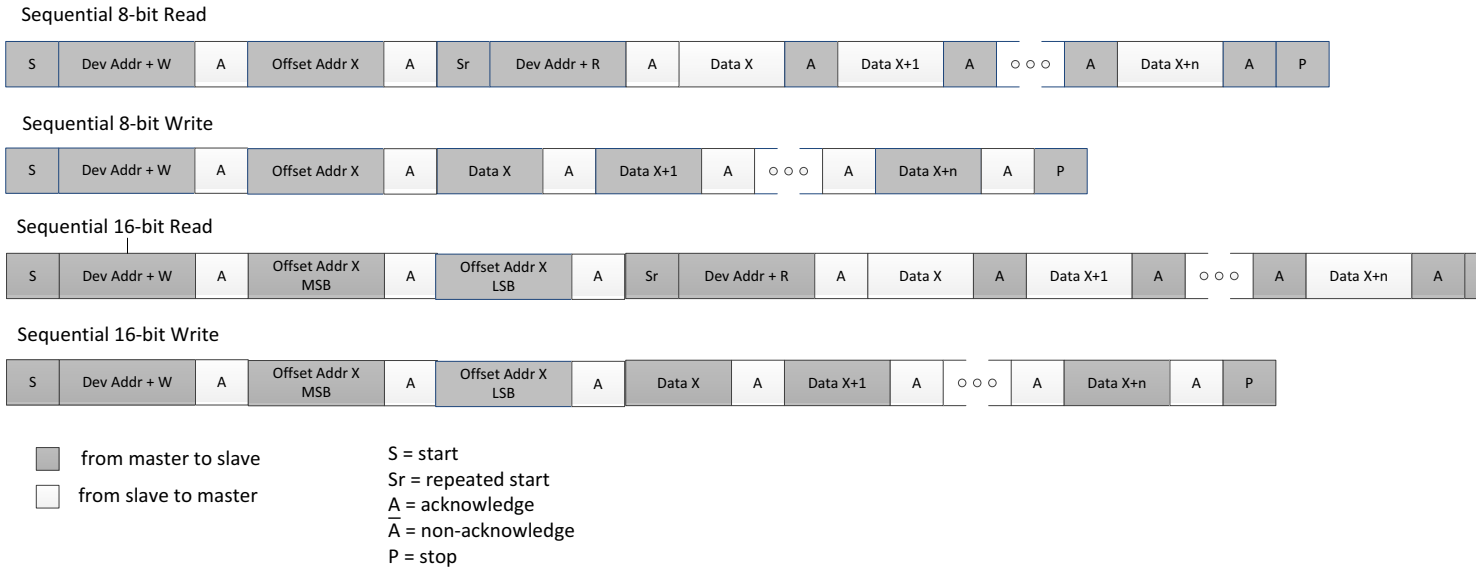
Figure 1: Register Addressing Modes via Serial Port




## I²C Slave Operation

The I²C slave protocol of the 8A3xxx family complies with Version 2.1 of the I²C specification. Figure 2 shows the sequence of states on the I²C SDATA signal for the supported modes of operation.

Figure 2: I²C Slave Sequencing Diagram




The Dev Addr shown in the figure represents the base address of the 8A3xxxx device. This 7-bit value can be set in an internal register which can have a user-defined value loaded at reset from internal OTP memory or an external EEPROM. The default value if those methods are not used is 1011000b (binary). Note that the levels on the S_A0 and S_A1 inputs can be used to control Bit 0 and Bit 1 (respectively) of this address. These pins are available independently for each serial port. In I²C operation these inputs are expected to remain static. They have different functions when the part is in SPI mode. The resulting base address is the I²C bus address that this device will respond to. The default address may be overwritten at any time.

When I²C operation is selected for either slave serial port, selection of 1-byte (1B) or 2-byte (2B) offset addressing must also be selected independently for each slave serial port. These offsets are used in conjunction with the page register for each serial port to access registers internal to the device. Because the I²C protocol already includes a read/write bit with the Dev Addr, all bits of the 1B or 2B offset field can be used to address internal registers.

- In 1B mode, the lower 8 bits of the register offset address come from the Offset Addr byte and the upper 8 bits come from the page register (see Table 2 for description of the 8-bit I²C Page Register).
  The page register can be accessed at any time, no matter what page the serial port is currently on, using an offset byte value of FCh. This 4-byte register must be written in a single burst write transaction. The page register is replicated on every register page to always be accessible.
- In 2B mode, the full 16-bit register address can be obtained from the Offset Addr bytes, so the page register only needs to be set once after reset using a 3-byte burst access starting from address FFFDh (see Table 3 for description of the 16-bit I²C Page Register).

Table 2: I²C 1B Mode Page Register Bit Field Locations and Descriptions

| Offset Address (Hex) | I²C 1B Mode Page Register Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| FC | PAGE_ADDR[7:0] | | | | | | | |
| FD | PAGE_ADDR[15:8] | | | | | | | |
| FE | PAGE_ADDR[23:16] | | | | | | | |
| FF | PAGE_ADDR[31:24] | | | | | | | |

| I²C 1B Mode Page Register Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PAGE_ADDR[7:0] | R/W | 00h | The values in this field are always replaced by the bits in I²C transaction itself and so have no meaning. |
| PAGE_ADDR[15:8] | R/W | 00h | Select which register page to access. Forms the upper 8-bits of the 16-bit register address. Only values of 80h or higher should be used. Lower addresses are not user-accessible |
| PAGE_ADDR[23:16] | R/W | 10h | Must be set to 10h in all cases |
| PAGE_ADDR[31:24] | R/W | 20h | Must be set to 20h in all cases |

Table 3: I²C 2B Mode Page Register Bit Field Locations and Descriptions

| Offset Address (Hex) | I²C 2B Mode Page Register Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| FFFD[1] | PAGE_ADDR[15:8] | | | | | | | |
| FFFE | PAGE_ADDR[23:16] | | | | | | | |
| FFFF | PAGE_ADDR[31:24] | | | | | | | |

1. Burst access must begin at this non-aligned offset and all 3 bytes must be written in the same I²C burst access. A burst beginning at the 32-bit aligned address of FFFCh will not correctly set this register.

| I²C 2B Mode Page Register Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PAGE_ADDR[15:8] | R/W | 00h | The values in this field are always replaced by the bits in I²C transaction itself and so have no meaning. |
| PAGE_ADDR[23:16] | R/W | 10h | Must be set to 10h in all cases |
| PAGE_ADDR[31:24] | R/W | 20h | Must be set to 20h in all cases |

I²C burst mode operation is required to ensure data integrity of multi-byte registers. When accessing a multi-byte register, all data bytes must be written or read in a single I²C burst access. Bursts may be of greater length if desired, but must not extend beyond the end of the register page (Offset Addr FFh in 1B mode, no limit in 2B mode). An internal address pointer is incremented automatically as each data byte is written or read.

*²C 1-byte (1B) Addressing Examples*

8A3xxxx I²C 7-bit I²C address is 0x5B with LSB=R/W

Example Write “0x50” to register 0xCBE4

```
B6* FC 00 CB 10 20      #Set Page Register, *I²C Address is left-shifted one bit.
B6 E4 50                #Write data 5B to CB E4
```

Example read from register 0xC024

| | |
|---|---|
| B6* FC 00 C0 10 20 | #Set Page Register, *I2C Address is left-shifted one bit. |
| B6 24* | #Set I2C pointer to 0xC024, *I2C instruction should use “No Stop” |
| B7 <read back data> | #Send address with Read bit set. |

*I2C 2-byte (2B) Addressing*

8A3xxxx I2C 7-bit I2C address is 0x5B with LSB=R/W

Example Write “50” to register 0xCBE4

| | |
|---|---|
| B6* FF FD 00 10 20 | #Set Page Register, *I2C Address is left-shifted one bit. |
| B6 CB E4 50 | #Write data to CB E4 |

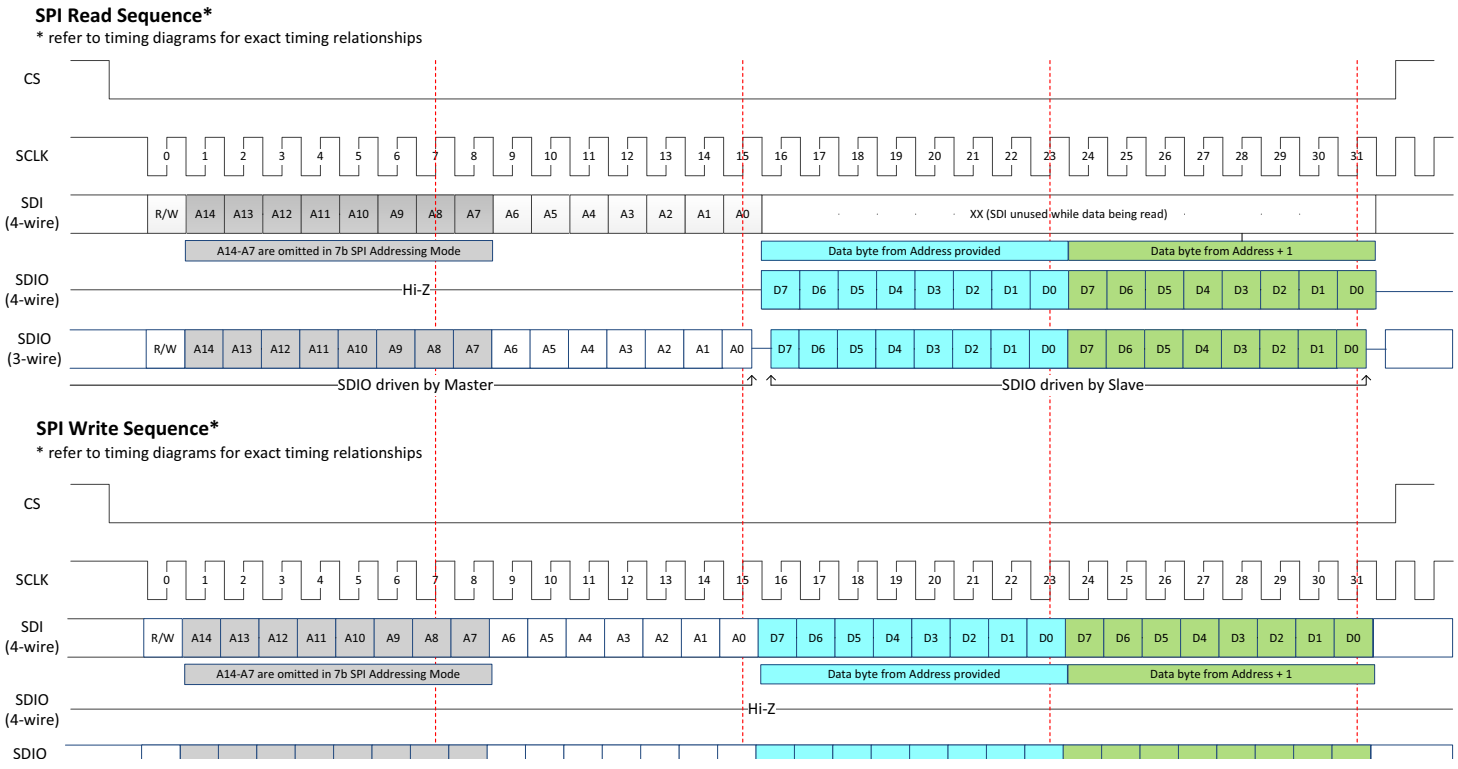
Example read from register 0xC024:

| | |
|---|---|
| B6* FF FD 00 10 20 | #Set Page Register (*I2C Address is left-shifted one bit.) |
| B6 C0 24* | #Set I2C pointer to 0xC024, *I2C instruction should use “No Stop” |
| B7 <read back data> | #Send address with Read bit set. |

## SPI Operation

The 8A3xxxx family of devices support SPI operation on their main and alternate serial ports. Figure 3 shows the sequencing of address and data on the serial port in SPI mode.

Figure 3: SPI Sequencing Diagram




Each serial port can be independently configured for the following settings. These settings can come from register defaults or from an internal OTP or external EEPROM configuration loaded at reset:

— 1-byte (1B) or 2-byte (2B) offset addressing (see Figure 1)

  - In 1B operation, the 16-bit register address is formed by using the 7 bits of address supplied in the SPI access and taking the upper 9 bits from the page register. The page register is accessed, no matter what page the serial port is currently on, using an Offset Address of 7Ch - 7Fh. It must be accessed in a single 4-byte burst write transaction. The page register is replicated on every register page to always be accessible.
  - In 2B operation, the 16-bit register address is formed by using the 15 bits of address supplied in the SPI access and taking the upper 1 bit from the page register. Note that this bit will always be '1' for register accesses, so the page register only needs to be set once in 2B operation. The page register can be accessed, no matter what page the serial port is currently on, using an Offset Address of 7FFDh - 7FFFh. It should be accessed in a single 3-byte burst write transaction to set it. The page register is replicated on every register page to always be accessible.
- Data sampling on falling or rising edge of SCLK
- Output (read) data positioning relative to active SCLK edge
- 4-wire (SCLK, SCSb, SDATA, SDO) or 3-wire (SCLK, SCSb, SDATA) operation
  - In 3-wire mode, SDATA is a bi-directional data pin.
- Output signal protocol compatibility / drive strength and termination voltage

Table 4: SPI 1B Mode Page Register Bit Field Locations and Descriptions

| Offset Address (Hex) | SPI 1B Mode Page Register Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 7C | PAGE_ADDR [7] | PAGE_ADDR[6:0] | | | | | | |
| 7D | PAGE_ADDR[15:8] | | | | | | | |
| 7E | PAGE_ADDR[23:16] | | | | | | | |
| 7F | PAGE_ADDR[31:24] | | | | | | | |

| SPI 1BMode Page Register Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PAGE_ADDR[6:0] | R/W | - | The values in this field are always replaced by the bits in SPI transaction itself and so have no meaning. |
| PAGE_ADDR[15:7] | R/W | 000000000b | Select which register page to access. Forms the upper 9-bits of the 16-bit register address. Only values of 100000000b or higher should be used. Lower addresses are not user-accessible |
| PAGE_ADDR[23:16] | R/W | 10h | Must be set to 10h in all cases |
| PAGE_ADDR[31:24] | R/W | 20h | Must be set to 20h in all cases |

Table 5: SPI 2B Mode Page Register Bit Field Locations and Descriptions

| Offset Address (Hex) | SPI 2B Mode Page Register Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 7FFD[1] | PAGE_ADDR [15] | PAGE_ADDR[14:8] | | | | | | |
| 7FFE | PAGE_ADDR[23:16] | | | | | | | |
| 7FFF | PAGE_ADDR[31:24] | | | | | | | |

1. Burst access must begin at this non-aligned offset and all 3 bytes must be written in the same SPI burst access. A burst beginning at the 32-bit aligned address of 7FFCh will not correctly set this register.

| SPI 2B Mode Page Register Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PAGE_ADDR[14:8] | R/W | 0000000b | The values in this field are always replaced by the bits in SPI transaction itself and so have no meaning. |
| PAGE_ADDR[15] | R/W | 0b | Select which register page to access. Forms the most-significant bit of the 16-bit register address. Only a value of 1b should be used. Lower addresses are not user-accessible |
| PAGE_ADDR[23:16] | R/W | 10h | Must be set to 10h in all cases |
| PAGE_ADDR[31:24] | R/W | 20h | Must be set to 20h in all cases |

SPI burst mode operation is required to ensure data integrity of multi-byte registers. When accessing a multi-byte register, all data bytes must be written or read in a single SPI burst access. Bursts may be of greater length if desired, but must not extend beyond the end of the register page. An internal address pointer is incremented automatically as each data byte is written or read.

*SPI 1-byte (1B) Addressing Example*

Example Write to “50” to register 0xCBE4

```
7C 80 CB 10 20          #Set Page register
64* 50                  #*MSB is 0 for write transactions
```

Example Read from 0xC024:

```
7C 00 C0 10 20          #Set Page register
A4* 00                  #*MSB is set, so this is a read command
```

*SPI 2-byte (2B) Addressing Example*

Example Write to “50” to register 0xCBE4

```
7F FD 80 10 20          #Set Page register
4B E4* 50               #*MSB is 0 for write transactions
```

Example Read from 0xC024:

```
7F FD 80 10 20          #Set Page register
C0* 24 00               #*MSB is set, so this is a read command
```

## Register Table Overview

When programming an 8A3xxxx family device, it is necessary to read or write values to one or more *bit-fields* within the device. A bit-field provides status and/or control information on a single aspect of a single feature. A bit field may be as small as a single-bit or many bytes in length. A bit-field should be treated as an indivisible entity and all bytes of each bit-field should be read or written in a single serial port burst.

Access to bit-fields is performed using byte-oriented addressing. A bit-field may take up multiple byte address and/or multiple bit-fields may occupy a single byte. When there are multiple bit-fields within a single byte, all bit fields are read from or written to during an access to that byte address over the serial port. When a bit-field spans multiple byte addresses, all bytes should be read or written in the same serial port burst transaction to ensure consistency. For bit-fields spanning multiple bytes, the least-significant bits of that bit-field are contained in the byte with the lowest address.

Bit-fields are grouped into *registers* and registers are in turn grouped into *modules*. In the documentation that follows, bit-fields are shown mapped into register bytes in a table called a *Bit-Field Location* table. The function of each bit-field is shown in an associated *Bit-Field Description* table. One or more bit-fields are grouped into a register. Registers show an address offset for each byte within that register.

A number of registers are grouped together into a module. In general a module contains all the registers needed to interact with a functional block within the device. Each module in the standard register set is listed in a Register Module Index table showing its module base address, a brief description of the module's function and a link to that module's location in the document. In each module's sub-section is a similar table listing all the registers within that module, a brief description of the register and a link to that register's detailed description. This is shown in Figure 4

Many register modules include a trigger register that must be written to cause register changes within that module to take effect; the trigger register must be written even if the contents of the trigger register are not changed. Where present, the trigger register is always the last register in the module so that the last write of a burst will trigger any changes in the module. After a trigger register is written the user should wait 200 microseconds before reading or writing any register in the device.

Figure 4: Finding a Register's Detailed Description in this Document

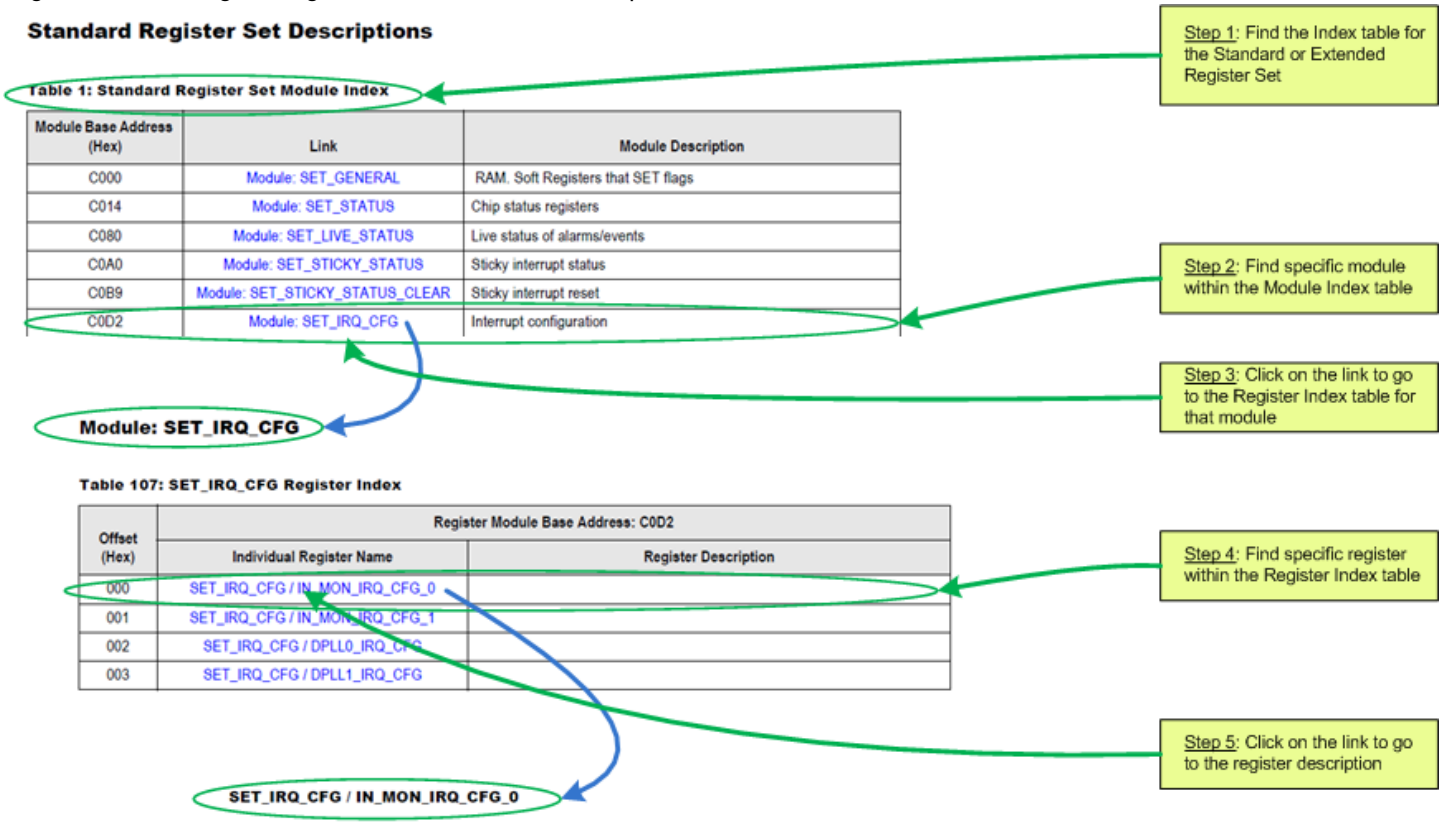



**Table 108: SET_IRQ_CFG / IN_MON_IRQ_CFG_0 Bit Field Locations and Descriptions**

| Offset Address (Hex) | SET_IRQ_CFG / IN_MON_IRQ_CFG_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000 | IN7_MON_EN | IN6_MON_EN | IN5_MON_EN | IN4_MON_EN | IN3_MON_EN | IN2_MON_EN | IN1_MON_EN | IN0_MON_EN |

| IN_MON_IRQ_CFG_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN7_MON_EN | R/W | 0 | 0 = disabled<br>1 = enabled |
| IN6_MON_EN | R/W | 0 | 0 = disabled<br>1 = enabled |
| IN5_MON_EN | R/W | 0 | 0 = disabled<br>1 = enabled |
| IN4_MON_EN | R/W | 0 | 0 = disabled<br>1 = enabled |

The device contains multiple copies of many functional blocks and each has its own associated register module for status and control. To keep the documentation clear and concise, only the first instance of a register module for a specific functional block will be shown in detail. The module table will show all instantiations of the module with their unique base addresses, but the links will all point to the same descriptive section (see blue arrows in Figure 5). Please ensure that when addressing a register that the base address of the correct instantiation of the module is used (see red arrows in Figure 5). Note that the base address indicated in the table description is for the first instantiation of the module only (see green arrow in Figure 5). For example, as shown below, to access the DPLL_MANUAL_HOLDOVER_VALUE bit-field for DPLL4, take the base address of that instantiation (C480h) and add the register offset of that specific register (008h). Note that since this bit-field is more than one byte, all bytes should be accessed in a single serial port burst transaction starting at C488h.

Figure 5: Determining the Address to Access a Specific Register.

**Table 1: Standard Register Set Module Index**

| Module Base Address (Hex) | Link | Module Description |
|---|---|---|
| C000 | Module: SET_GENERAL | RAM. Soft Registers that SET flags |
| C280 | Module: SET_DPLL | DPLL0 registers |
| C300 | Module: SET_DPLL | DPLL1 registers |
| C380 | Module: SET_DPLL | DPLL2 registers |
| C400 | Module: SET_DPLL | DPLL3 registers |
| C480 | Module: SET_DPLL | DPLL4 registers |
| C500 | Module: SET_DPLL | DPLL5 registers |
| C580 | Module: SET_DPLL | DPLL6 registers |
| C600 | Module: SET_DPLL | DPLL7 registers |
| C680 | Module: SET_SYS_DPLL | SYS_DPLL registers |

**Module: SET_DPLL**

**Table 142: SET_DPLL Register Index**

| Offset (Hex) | Register Module Base Address: C280[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000 | SET_DPLL / DPLL_COMBO_SW_VALUE_CNFG | |
| 008 | SET_DPLL / DPLL_MANUAL_HOLDOVER_VALUE | |
| 010 | SET_DPLL / DPLL_FOD_FREQ_B | |
| 012 | SET_DPLL / DPLL_FOD_FREQ_K | |

**Table 144: SET_DPLL / DPLL_MANUAL_HOLDOVER_VALUE Bit Field Locations and Descriptions**

| Offset Address (Hex) | SET_DPLL / DPLL_MANUAL_HOLDOVER_VALUE Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 008 | DPLL_MANUAL_HOLDOVER_VALUE[7:0] | | | | | | | |
| 009 | DPLL_MANUAL_HOLDOVER_VALUE[15:8] | | | | | | | |
| 00A | DPLL_MANUAL_HOLDOVER_VALUE[23:16] | | | | | | | |
| 00B | DPLL_MANUAL_HOLDOVER_VALUE[31:24] | | | | | | | |

Register Address = Module Base Address (for instance desired) + Register Offset

## Terminology

The following terminology and abbreviations are used in the register tables.

- If a bit-field has more than a single bit, the bit-field will be written as BIT_FIELD_NAME[msb:lsb] (e.g. DPLL_MANUAL_HOLDOVER_VALUE[39:0]
- Binary numbers will be written with a lowercase ‘b’ after them (e.g. 0101b )
- Hexadecimal numbers will be written with a lowercase ‘h’ after them (e.g. C480h).
- R/W indicates a register is readable and writable by the user
- R/O indicates that a register should only be read by the user. Writing to a R/O register has an undefined effect.
- W/O indicates that a register should only be written to by the user. The read value is undefined and has no associated meaning.
- RW1C indicates a register that can be read, but a ‘1’ needs to be written to the bit to clear it back to 0. This is generally used for ‘sticky’ status bits that are latched high whenever a transient condition occurs. The user will need to write to clear the latched status.
- N/A means Not Applicable. This is only used for Reserved bit-fields who’s behaviour is not defined.

# Register Set Descriptions

Table 6: Register Set Module Index

| Module Base Address (Hex) | Link | Module Description |
|---|---|---|
| 8180h | Module: HW_REVISION | Hardware Revision ID register. |
| C000h | Module: RESET_CTRL | General reset management. |
| C014h | Module: GENERAL_STATUS | Chip hardware status registers. |
| C03Ch | Module: STATUS | Live status of alarms and events. |
| C160h | Module: GPIO_USER_CONTROL | GPIO user control. |
| C164h | Module: STICKY_STATUS_CLEAR | Sticky status clear. |
| C16Ch | Module: GPIO_TOD_NOTIFICATION_CLEAR | Clear GPIO output Time of Day read notification. |
| C170h | RESERVED | This module must not be modified from the read value |
| C180h | RESERVED | This module must not be modified from the read value |
| C188h | Module: ALERT_CFG | Notification configuration. |
| C194h | Module: SYS_DPLL_XO | System DPLL XO configuration. |
| C19Ch | Module: SYS_APLL | System APLL configuration. |
| C1B0h | Module: INPUT_0 | Input 0 configuration. |
| C1C0h | INPUT_1 | Input 1 configuration.<br>Same as INPUT_0. |
| C1D0h | INPUT_2 | Input 2 configuration.<br>Same as INPUT_0. |
| C200h | INPUT_3 | Input 3 configuration.<br>Same as INPUT_0. |
| C210h | INPUT_4 | Input 4 configuration.<br>Same as INPUT_0. |
| C220h | INPUT_5 | Input 5 configuration.<br>Same as INPUT_0. |
| C230h | INPUT_6 | Input 6 configuration.<br>Same as INPUT_0. |
| C240h | INPUT_7 | Input 7 configuration.<br>Same as INPUT_0. |
| C250h | INPUT_8 | Input 8 configuration.<br>Same as INPUT_0. |
| C260h | INPUT_9 | Input 9 configuration.<br>Same as INPUT_0. |
| C280h | INPUT_10 | Input 10 configuration.<br>Same as INPUT_0. |

Table 6: Register Set Module Index

| Module Base Address (Hex) | Link | Module Description |
|---|---|---|
| C290h | INPUT_11 | Input 11 configuration.<br>Same as INPUT_0. |
| C2A0h | INPUT_12 | Input 12 configuration.<br>Same as INPUT_0. |
| C2B0h | INPUT_13 | Input 13 configuration.<br>Same as INPUT_0. |
| C2C0h | INPUT_14 | Input 14 configuration.<br>Same as INPUT_0. |
| C2D0h | INPUT_15 | Input 15 configuration.<br>Same as INPUT_0. |
| C2E0h | Module: REF_MON_0 | Reference monitor 0. |
| C2ECh | REF_MON_1 | Reference monitor 1.<br>Same as REF_MON_0. |
| C300h | REF_MON_2 | Reference monitor 2.<br>Same as REF_MON_0. |
| C30Ch | REF_MON_3 | Reference monitor 3.<br>Same as REF_MON_0. |
| C318h | REF_MON_4 | Reference monitor 4.<br>Same as REF_MON_0. |
| C324h | REF_MON_5 | Reference monitor 5.<br>Same as REF_MON_0. |
| C330h | REF_MON_6 | Reference monitor 6.<br>Same as REF_MON_0. |
| C33Ch | REF_MON_7 | Reference monitor 7.<br>Same as REF_MON_0. |
| C348h | REF_MON_8 | Reference monitor 8.<br>Same as REF_MON_0. |
| C354h | REF_MON_9 | Reference monitor 9.<br>Same as REF_MON_0. |
| C360h | REF_MON_10 | Reference monitor 10.<br>Same as REF_MON_0. |
| C36Ch | REF_MON_11 | Reference monitor 11.<br>Same as REF_MON_0. |
| C380h | REF_MON_12 | Reference monitor 12.<br>Same as REF_MON_0. |
| C38Ch | REF_MON_13 | Reference monitor 13.<br>Same as REF_MON_0. |
| C398h | REF_MON_14 | Reference monitor 14.<br>Same as REF_MON_0. |

Table 6: Register Set Module Index

| Module Base Address (Hex) | Link | Module Description |
|---|---|---|
| C3A4h | REF_MON_15 | Reference monitor 15.<br>Same as REF_MON_0. |
| C3B0h | Module: DPLL_0 | DPLL 0 configuration registers. |
| C400h | DPLL_1 | DPLL 1 registers.<br>Same as DPLL_0. |
| C438h | DPLL_2 | DPLL 2 registers.<br>Same as DPLL_0. |
| C480h | DPLL_3 | DPLL 3 registers.<br>Same as DPLL_0. |
| C4B8h | DPLL_4 | DPLL 4 registers.<br>Same as DPLL_0. |
| C500h | DPLL_5 | DPLL 5 registers.<br>Same as DPLL_0. |
| C538h | DPLL_6 | DPLL 6 registers.<br>Same as DPLL_0. |
| C580h | DPLL_7 | DPLL 7 registers.<br>Same as DPLL_0. |
| C5B8h | Module: SYS_DPLL | System DPLL registers. |
| C600h | Module: DPLL_CTRL_0 | DPLL 0 control registers. |
| C63Ch | DPLL_CTRL_1 | DPLL 1 control registers.<br>Same as DPLL_CTRL_0. |
| C680h | DPLL_CTRL_2 | DPLL 2 control registers.<br>Same as DPLL_CTRL_0. |
| C6BCh | DPLL_CTRL_3 | DPLL 3 control registers.<br>Same as DPLL_CTRL_0. |
| C700h | DPLL_CTRL_4 | DPLL 4 control registers.<br>Same as DPLL_CTRL_0. |
| C73Ch | DPLL_CTRL_5 | DPLL 5 control registers.<br>Same as DPLL_CTRL_0. |
| C780h | DPLL_CTRL_6 | DPLL 6 control registers.<br>Same as DPLL_CTRL_0. |
| C7BCh | DPLL_CTRL_7 | DPLL 7 control registers.<br>Same as DPLL_CTRL_0. |
| C800h | Module: SYS_DPLL_CTRL | System DPLL control registers. |
| C818h | Module: DPLL_PHASE_0 | DPLL 0 write phase. |
| C81Ch | DPLL_PHASE_1 | DPLL 1 write phase.<br>Same as DPLL_PHASE_0. |

Table 6: Register Set Module Index

| Module Base Address (Hex) | Link | Module Description |
|---|---|---|
| C820h | DPLL_PHASE_2 | DPLL 2 write phase.<br>Same as DPLL_PHASE_0. |
| C824h | DPLL_PHASE_3 | DPLL 3 write phase.<br>Same as DPLL_PHASE_0. |
| C828h | DPLL_PHASE_4 | DPLL 4 write phase.<br>Same as DPLL_PHASE_0. |
| C82Ch | DPLL_PHASE_5 | DPLL 5 write phase.<br>Same as DPLL_PHASE_0. |
| C830h | DPLL_PHASE_6 | DPLL 6 write phase.<br>Same as DPLL_PHASE_0. |
| C834h | DPLL_PHASE_7 | DPLL 7 write phase.<br>Same as DPLL_PHASE_0. |
| C838h | Module: DPLL_FREQ_0 | DPLL 0 write frequency. |
| C840h | DPLL_FREQ_1 | DPLL 1 write frequency.<br>Same as DPLL_FREQ_0. |
| C848h | DPLL_FREQ_2 | DPLL 2 write frequency.<br>Same as DPLL_FREQ_0. |
| C850h | DPLL_FREQ_3 | DPLL 3 write frequency.<br>Same as DPLL_FREQ_0. |
| C858h | DPLL_FREQ_4 | DPLL 4 write frequency.<br>Same as DPLL_FREQ_0. |
| C860h | DPLL_FREQ_5 | DPLL 5 write frequency.<br>Same as DPLL_FREQ_0. |
| C868h | DPLL_FREQ_6 | DPLL 6 write frequency.<br>Same as DPLL_FREQ_0. |
| C870h | DPLL_FREQ_7 | DPLL 7 write frequency.<br>Same as DPLL_FREQ_0. |
| C880h | Module: DPLL_PHASE_PULL_IN_0 | DPLL 0 phase pull-in control. |
| C888h | DPLL_PHASE_PULL_IN_1 | DPLL 1 phase pull-in control.<br>Same as DPLL_PHASE_PULL_IN_0. |
| C890h | DPLL_PHASE_PULL_IN_2 | DPLL 2 phase pull-in control.<br>Same as DPLL_PHASE_PULL_IN_0. |
| C898h | DPLL_PHASE_PULL_IN_3 | DPLL 3 phase pull-in control.<br>Same as DPLL_PHASE_PULL_IN_0. |
| C8A0h | DPLL_PHASE_PULL_IN_4 | DPLL 4 phase pull-in control.<br>Same as DPLL_PHASE_PULL_IN_0. |
| C8A8h | DPLL_PHASE_PULL_IN_5 | DPLL 5 phase pull-in control.<br>Same as DPLL_PHASE_PULL_IN_0. |

Table 6: Register Set Module Index

| Module Base Address (Hex) | Link | Module Description |
|---|---|---|
| C8B0h | DPLL_PHASE_PULL_IN_6 | DPLL 6 phase pull-in control.<br>Same as DPLL_PHASE_PULL_IN_0. |
| C8B8h | DPLL_PHASE_PULL_IN_7 | DPLL 7 phase pull-in control.<br>Same as DPLL_PHASE_PULL_IN_0. |
| C8C0h | Module: GPIO_CFG | GPIO global configuration. |
| C8C2h | Module: GPIO_0 | GPIO 0 registers. |
| C8D4h | GPIO_1 | GPIO 1 registers.<br>Same as GPIO_0. |
| C8E6h | GPIO_2 | GPIO 2 registers.<br>Same as GPIO_0. |
| C900h | GPIO_3 | GPIO 3 registers.<br>Same as GPIO_0. |
| C912h | GPIO_4 | GPIO 4 registers.<br>Same as GPIO_0. |
| C924h | GPIO_5 | GPIO 5 registers.<br>Same as GPIO_0. |
| C936h | GPIO_6 | GPIO 6 registers.<br>Same as GPIO_0. |
| C948h | GPIO_7 | GPIO 7 registers.<br>Same as GPIO_0. |
| C95Ah | GPIO_8 | GPIO 8 registers.<br>Same as GPIO_0. |
| C980h | GPIO_9 | GPIO 9 registers.<br>Same as GPIO_0. |
| C992h | GPIO_10 | GPIO 10 registers.<br>Same as GPIO_0. |
| C9A4h | GPIO_11 | GPIO 11 registers.<br>Same as GPIO_0. |
| C9B6h | GPIO_12 | GPIO 12 registers.<br>Same as GPIO_0. |
| C9C8h | GPIO_13 | GPIO 13 registers.<br>Same as GPIO_0. |
| C9DAh | GPIO_14 | GPIO 14 registers.<br>Same as GPIO_0. |
| CA00h | GPIO_15 | GPIO 15 registers.<br>Same as GPIO_0. |
| CA12h | Module: OUT_DIV_MUX | Output divider multiplexers. |
| CA14h | Module: OUTPUT_0 | Output 0 registers. |

Table 6: Register Set Module Index

| Module Base Address (Hex) | Link | Module Description |
|---|---|---|
| CA24h | OUTPUT_1 | Output 1 register.<br>Same as OUTPUT_0. |
| CA34h | OUTPUT_2 | Output 2 register.<br>Same as OUTPUT_0. |
| CA44h | OUTPUT_3 | Output 3 register.<br>Same as OUTPUT_0. |
| CA54h | OUTPUT_4 | Output 4 register.<br>Same as OUTPUT_0. |
| CA64h | OUTPUT_5 | Output 5 register.<br>Same as OUTPUT_0. |
| CA80h | OUTPUT_6 | Output 6 register.<br>Same as OUTPUT_0. |
| CA90h | OUTPUT_7 | Output 7 register.<br>Same as OUTPUT_0. |
| CAA0h | OUTPUT_8 | Output 8 register.<br>Same as OUTPUT_0. |
| CAB0h | OUTPUT_9 | Output 9 register.<br>Same as OUTPUT_0. |
| CAC0h | OUTPUT_10 | Output 10 register.<br>Same as OUTPUT_0. |
| CAD0h | OUTPUT_11 | Output 11 register.<br>Same as OUTPUT_0. |
| CAE0h | Module: SERIAL | Serial Interfaces registers. |
| CB00h | Module: PWM_ENCODER_0 | PWM 0 encoder registers. |
| CB08h | PWM_ENCODER_1 | PWM 1 encoder registers.<br>Same as PWM_ENCODER_0. |
| CB10h | PWM_ENCODER_2 | PWM 2 encoder registers.<br>Same as PWM_ENCODER_0. |
| CB18h | PWM_ENCODER_3 | PWM 3 encoder registers.<br>Same as PWM_ENCODER_0. |
| CB20h | PWM_ENCODER_4 | PWM 4 encoder registers.<br>Same as PWM_ENCODER_0. |
| CB28h | PWM_ENCODER_5 | PWM 5 encoder registers.<br>Same as PWM_ENCODER_0. |
| CB30h | PWM_ENCODER_6 | PWM 6 encoder registers.<br>Same as PWM_ENCODER_0. |
| CB38h | PWM_ENCODER_7 | PWM 7 encoder registers.<br>Same as PWM_ENCODER_0. |
| CB40h | Module: PWM_DECODER_0 | PWM 0 decoder registers. |

Table 6: Register Set Module Index

| Module Base Address (Hex) | Link | Module Description |
|---|---|---|
| CB48h | PWM_DECODER_1 | PWM 1 decoder registers.<br>Same as PWM_DECODER_0. |
| CB50h | PWM_DECODER_2 | PWM 2 decoder registers.<br>Same as PWM_DECODER_0. |
| CB58h | PWM_DECODER_3 | PWM 3 decoder registers.<br>Same as PWM_DECODER_0. |
| CB60h | PWM_DECODER_4 | PWM 4 decoder registers.<br>Same as PWM_DECODER_0. |
| CB68h | PWM_DECODER_5 | PWM 5 decoder registers.<br>Same as PWM_DECODER_0. |
| CB70h | PWM_DECODER_6 | PWM 6 decoder registers.<br>Same as PWM_DECODER_0. |
| CB80h | PWM_DECODER_7 | PWM 7 decoder registers.<br>Same as PWM_DECODER_0. |
| CB88h | PWM_DECODER_8 | PWM 8 decoder registers.<br>Same as PWM_DECODER_0. |
| CB90h | PWM_DECODER_9 | PWM 9 decoder registers.<br>Same as PWM_DECODER_0. |
| CB98h | PWM_DECODER_10 | PWM 10 decoder registers.<br>Same as PWM_DECODER_0. |
| CBA0h | PWM_DECODER_11 | PWM 11 decoder registers.<br>Same as PWM_DECODER_0. |
| CBA8h | PWM_DECODER_12 | PWM 12 decoder registers.<br>Same as PWM_DECODER_0. |
| CBB0h | PWM_DECODER_13 | PWM 13 decoder registers.<br>Same as PWM_DECODER_0. |
| CBB8h | PWM_DECODER_14 | PWM 14 decoder registers.<br>Same as PWM_DECODER_0. |
| CBC0h | PWM_DECODER_15 | PWM 15 decoder registers.<br>Same as PWM_DECODER_0. |
| CBC8h | Module: PWM_USER_DATA | PWM user data registers. |
| CBCCh | Module: TOD_0 | TOD 0 registers. |
| CBCEh | TOD_1 | TOD 1 registers.<br>Same as TOD_0. |
| CBD0h | TOD_2 | TOD 2 registers.<br>Same as TOD_0. |
| CBD2h | TOD_3 | TOD 3 registers.<br>Same as TOD_0. |
| CC00h | Module: TOD_WRITE_0 | Write TOD 0 registers. |

Table 6: Register Set Module Index

| Module Base Address (Hex) | Link | Module Description |
|---|---|---|
| CC10h | TOD_WRITE_1 | Write TOD 1 registers.<br>Same as TOD_WRITE_0. |
| CC20h | TOD_WRITE_2 | Write TOD 2 registers.<br>Same as TOD_WRITE_0. |
| CC30h | TOD_WRITE_3 | Write TOD 3 registers.<br>Same as TOD_WRITE_0. |
| CC40h | Module: TOD_READ_PRIMARY_0 | Read TOD 0 primary registers. |
| CC50h | TOD_READ_PRIMARY_1 | Read TOD 1 primary registers.<br>Same as TOD_READ_PRIMARY_0. |
| CC60h | TOD_READ_PRIMARY_2 | Read TOD 2 primary registers.<br>Same as TOD_READ_PRIMARY_0. |
| CC80h | TOD_READ_PRIMARY_3 | Read TOD 3 primary registers.<br>Same as TOD_READ_PRIMARY_0. |
| CC90h | Module: TOD_READ_SECONDARY_0 | Read TOD 0 secondary registers. |
| CCA0h | TOD_READ_SECONDARY_1 | Read TOD 1 secondary registers.<br>Same as TOD_READ_SECONDARY_0. |
| CCB0h | TOD_READ_SECONDARY_2 | Read TOD 2 secondary registers.<br>Same as TOD_READ_SECONDARY_0. |
| CCC0h | TOD_READ_SECONDARY_3 | Read TOD 3 secondary registers.<br>Same as TOD_READ_SECONDARY_0. |
| CCD0h | Module: OUTPUT_TDC_CFG | Output TDC global configuration. |
| CD00h | Module: OUTPUT_TDC_0 | Output TDC 0. |
| CD08h | OUTPUT_TDC_1 | Output TDC 1.<br>Same as OUTPUT_TDC_0. |
| CD10h | OUTPUT_TDC_2 | Output TDC 2.<br>Same as OUTPUT_TDC_0. |
| CD18h | OUTPUT_TDC_3 | Output TDC 3.<br>Same as OUTPUT_TDC_0. |
| CD20h | Module: INPUT_TDC | Input TDC |
| CF40h | RESERVED | This module must not be modified from the read value |
| CF50h | Module: SCRATCH | User multipurpose registers. |
| CF60h | RESERVED | This module must not be modified from the read value |
| CF68h | Module: EEPROM | EEPROM. |
| CF70h | Module: OTP | OTP. |
| CF80h | Module: BYTE | OTP registers. |
| D000h | RESERVED | This module must not be modified from the read value |

## Module: HW_REVISION

Hardware Revision Information.Note that while this register can be accessed directly from the serial port by software, in IDT's Timing Commander GUI tool, it must be accessed indirectly since it is located in the hardware only register space.

Table 7: RESET_CTRL Register Index

| Offset (Hex) | Register Module Base Address: 8180h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 07Ah | HW_REVISION.REV_ID | Device Hardware Revision Number |

### HW_REVISION.REV_ID

Device Hardware Revision Number..

Table 8: HW_REVISION.REV_ID Bit Field Locations and Descriptions

| Offset Address (Hex) | HW_REVISION.REV_ID Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 07Ah | REV_ID[7:0] | | | | | | | |

| HW_REVISION.REV_ID Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| REV_ID[7:0] | R/O | 5 | Hardware Revision Register<br>1: RevA<br>2: RevB<br>3: RevC<br>4: RevD<br>5: RevE |

## Module: RESET_CTRL

Reset configuration.

Table 9: RESET_CTRL Register Index

| Offset (Hex) | Register Module Base Address: C000h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | RESERVED | This register must not be modified from the read value |
| 001h | RESERVED | This register must not be modified from the read value |
| 002h | RESERVED | This register must not be modified from the read value |
| 003h | RESERVED | This register must not be modified from the read value |
| 004h | RESERVED | This register must not be modified from the read value |
| 005h | RESERVED | This register must not be modified from the read value |
| 006h | RESERVED | This register must not be modified from the read value |

Table 9: RESET_CTRL Register Index

| Offset (Hex) | Register Module Base Address: C000h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 007h | RESERVED | This register must not be modified from the read value |
| 008h | RESERVED | This register must not be modified from the read value |
| 009h | RESERVED | This register must not be modified from the read value |
| 00Ah | RESERVED | This register must not be modified from the read value |
| 00Bh | RESERVED | This register must not be modified from the read value |
| 00Ch | RESERVED | This register must not be modified from the read value |
| 00Dh | RESERVED | This register must not be modified from the read value |
| 00Eh | RESERVED | This register must not be modified from the read value |
| 00Fh | RESERVED | This register must not be modified from the read value |
| 010h | RESERVED | This register must not be modified from the read value |
| 011h | RESERVED | This register must not be modified from the read value |
| 012h | RESET_CTRL.SM_RESET | Reset state machine. |

### RESET_CTRL.SM_RESET

Enable state machine reset.

TRIGGER: Writing to this byte triggers a read and activation in hardware of all the bytes of the RESET_CTRL module.

Table 10: RESET_CTRL.SM_RESET Bit Field Locations and Descriptions

| Offset Address (Hex) | RESET_CTRL.SM_RESET Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 012h | RESET[7:0] | | | | | | | |

| RESET_CTRL.SM_RESET Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESET[7:0] | R/W | 0 | Reset state machine.<br>0x5a = initiate state machine reset<br>Write 0x5A to perform state machine reset. All other values are ignored. Self clearing.<br>During a state machine reset, all registers starting from GENERAL_STATUS returns to reset values and the device proceeds with the start-up sequence as if the device was just powered on. The digital core is not reset. |

## Module: GENERAL_STATUS

Notification for hardware status.

Table 11: GENERAL_STATUS Register Index

| Offset (Hex) | Register Module Base Address: C014h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | RESERVED | This register must not be modified from the read value |
| 001h | RESERVED | This register must not be modified from the read value |
| 002h | RESERVED | This register must not be modified from the read value |
| 003h | RESERVED | This register must not be modified from the read value |
| 004h | GENERAL_STATUS.OTP_STATUS | Current status of OTP. |
| 008h | GENERAL_STATUS.EEPROM_STATUS | Current status of EEPROM. |
| 00Ah | RESERVED | This register must not be modified from the read value |
| 00Bh | RESERVED | This register must not be modified from the read value |
| 00Ch | RESERVED | This register must not be modified from the read value |
| 00Dh | RESERVED | This register must not be modified from the read value |
| 00Eh | RESERVED | This register must not be modified from the read value |
| 00Fh | RESERVED | This register must not be modified from the read value |
| 010h | GENERAL_STATUS.MAJ_REL | Major release number. |
| 011h | GENERAL_STATUS.MIN_REL | Minor release number. |
| 012h | GENERAL_STATUS.HOTFIX_REL | Hotfix release number. |
| 014h | RESERVED | This register must not be modified from the read value |
| 015h | RESERVED | This register must not be modified from the read value |
| 016h | RESERVED | This register must not be modified from the read value |
| 017h | RESERVED | This register must not be modified from the read value |
| 018h | RESERVED | This register must not be modified from the read value |
| 019h | RESERVED | This register must not be modified from the read value |
| 01Ah | RESERVED | This register must not be modified from the read value |
| 01Bh | RESERVED | This register must not be modified from the read value |
| 01Ch | GENERAL_STATUS.JTAG_DEVICE_ID | JTAG device identity. |
| 01Eh | GENERAL_STATUS.PRODUCT_ID | Product identity. |
| 020h | RESERVED | This register must not be modified from the read value |
| 021h | RESERVED | This register must not be modified from the read value |
| 022h | GENERAL_STATUS.OTP_SCSR_CONFIG_SELECT | Selected soft CSR configuration loaded from OTP. |

Table 11: GENERAL_STATUS Register Index

| Offset (Hex) | Register Module Base Address: C014h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 023h | GENERAL_STATUS.OTP_CONFIG_STATUS | OTP soft CSR configuration status. |
| 024h | GENERAL_STATUS.OTP_CSR_CONFIG_STATUS | OTP hard CSR configuration status. |
| 025h | RESERVED | This register must not be modified from the read value |
| 026h | GENERAL_STATUS.EEPROM_CONFIG_STATUS | EEPROM soft CSR configuration status. |

## GENERAL_STATUS.OTP_STATUS

Indicates status of OTP.

Table 12: GENERAL_STATUS.OTP_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | GENERAL_STATUS.OTP_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | OTP_STATUS[7:0] | | | | | | | |
| 005h | OTP_STATUS[15:8] | | | | | | | |
| 006h | OTP_STATUS[23:16] | | | | | | | |
| 007h | OTP_STATUS[31:24] | | | | | | | |

| GENERAL_STATUS.OTP_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| OTP_STATUS[31:0] | R/O | 0 | Current status of OTP.<br>0x0000000 = no status<br>0x1000000 = success<br>0x1000001 = corrupted header<br>0x1000002 = address out of range<br>0x1000003 = corrupted section<br>0x1000004 = invalid cluster index<br>0x1000005 = redundant cluster not available<br>0x1000006 = redundant cluster invalid index<br>0x1000007 = redundant cluster program fail<br>0x1000008 = cluster program fail<br>0x1000009 = cluster read fail<br>0x100000A = main memory program fail<br>0x100000B = no header available<br>0x100000C = not enough space<br>0x100000D = header fail<br>0x100000E = invalid boot row index<br>0x100000F = invalid header index<br>0x1000010 = header not found<br>0x1000011 = more data available<br>0x1000012 = wrong confirmation code<br>0x1000013 = OTP programming locked<br>0x10000FE = OTP access mode is disabled<br>0x10000FF = unknown command |

### GENERAL_STATUS.EEPROM_STATUS

Indicates status of EEPROM.

Table 13: GENERAL_STATUS.EEPROM_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | GENERAL_STATUS.EEPROM_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 008h | EEPROM_STATUS[7:0] | | | | | | | |
| 009h | EEPROM_STATUS[15:8] | | | | | | | |

| GENERAL_STATUS.EEPROM_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| EEPROM_STATUS[15:0] | R/O | 0 | Current status of EEPROM.<br>0x0000 = no status<br>0x8000 = ok<br>0x8001 = unknown command<br>0x8002 = wrong size<br>0x8003 = out of range<br>0x8004 = read failed<br>0x8005 = write failed<br>0x8006 = verification failed |

### GENERAL_STATUS.MAJ_REL

Major release number. e.g.. X.0.0

Table 14: GENERAL_STATUS.MAJ_REL Bit Field Locations and Descriptions

| Offset Address (Hex) | GENERAL_STATUS.MAJ_REL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 010h | MAJOR[7:1] | | | | | | | PR_BUILD[0] |

| GENERAL_STATUS.MAJ_REL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| MAJOR[7:1] | R/O | 0100b | Numeric major release. e.g.. X.0.0 |
| PR_BUILD[0] | R/O | 0001b | Product release status.<br>1 if a product release or 0 if a development release.. |

### GENERAL_STATUS.MIN_REL

Minor release number. e.g.. 1.Y.0

Table 15: GENERAL_STATUS.MIN_REL Bit Field Locations and Descriptions

| Offset Address (Hex) | GENERAL_STATUS.MIN_REL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 011h | MINOR[7:0] | | | | | | | |

| GENERAL_STATUS.MIN_REL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| MINOR[7:0] | R/O | 1000b | Minor release number. e.g.. 1.Y.0 |

### GENERAL_STATUS.HOTFIX_REL

Hotfix release number. e.g.. 1.2.Z

Table 16: GENERAL_STATUS.HOTFIX_REL Bit Field Locations and Descriptions

| Offset Address (Hex) | GENERAL_STATUS.HOTFIX_REL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 012h | HOTFIX[7:0] | | | | | | | |

| GENERAL_STATUS.HOTFIX_REL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| HOTFIX[7:0] | R/O | 0111b | Hotfix release number. e.g.. 1.2.Z |

### GENERAL_STATUS.JTAG_DEVICE_ID

16-bit subset of JTAG ID as determined by BOND_ID.

Table 17: GENERAL_STATUS.JTAG_DEVICE_ID Bit Field Locations and Descriptions

| Offset Address (Hex) | GENERAL_STATUS.JTAG_DEVICE_ID Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Ch | JTAG_DEVICE_ID[7:0] | | | | | | | |
| 01Dh | JTAG_DEVICE_ID[15:8] | | | | | | | |

| GENERAL_STATUS.JTAG_DEVICE_ID Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| JTAG_DEVICE_ID[15:0] | R/O | 0 | 16-bit ID code for this specific device, please refer to the Programming Guide Addendum for the specific device for expected value here. |

### GENERAL_STATUS.PRODUCT_ID

16-bit numeric value that correlates to the part number.

Table 18: GENERAL_STATUS.PRODUCT_ID Bit Field Locations and Descriptions

| Offset Address (Hex) | GENERAL_STATUS.PRODUCT_ID Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Eh | PRODUCT_ID[7:0] | | | | | | | |
| 01Fh | PRODUCT_ID[15:8] | | | | | | | |

| GENERAL_STATUS.PRODUCT_ID Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRODUCT_ID[15:0] | R/O | 0 | 16-bit Product ID code for this specific device, please refer to the Programming Guide Addendum for the specific device for expected value here. |

### GENERAL_STATUS.OTP_SCSR_CONFIG_SELECT

The index of the soft CSR configuration loaded from OTP.

Table 19: GENERAL_STATUS.OTP_SCSR_CONFIG_SELECT Bit Field Locations and Descriptions

| Offset Address (Hex) | GENERAL_STATUS.OTP_SCSR_CONFIG_SELECT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 022h | OTP_SCSR_CONFIG_SELECTION[7:0] | | | | | | | |

| GENERAL_STATUS.OTP_SCSR_CONFIG_SELECT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| OTP_SCSR_CONFIG_SELECTION[7:0] | R/O | 0 | Index of OTP SCSR configuration currently selected via startup GPIO function. |

### GENERAL_STATUS.OTP_CONFIG_STATUS

Status of soft CSR configuration loaded from OTP.

Table 20: GENERAL_STATUS.OTP_CONFIG_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | GENERAL_STATUS.OTP_CONFIG_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 023h | OTP_SCSR_CONFIG_STATUS[7:0] | | | | | | | |

| GENERAL_STATUS.OTP_CONFIG_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| OTP_SCSR_CONFIG_STATUS[7:0] | R/O | 0 | Status code.<br>0 = success<br>1 = not found<br>2 = incomplete<br>3 = wrong offset<br>4 = wrong length<br>5 = SCSR out of range<br>6 = CRC error |

### GENERAL_STATUS.OTP_CSR_CONFIG_STATUS

Status of hard CSR configuration loaded from OTP.

Table 21: GENERAL_STATUS.OTP_CSR_CONFIG_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | GENERAL_STATUS.OTP_CSR_CONFIG_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 024h | OTP_CSR_CONFIG_STATUS[7:0] | | | | | | | |

| GENERAL_STATUS.OTP_CSR_CONFIG_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| OTP_CSR_CONFIG_STATUS[7:0] | R/O | 0 | Status code.<br>0 = success<br>1 = not found<br>2 = incomplete<br>3 = wrong offset<br>4 = wrong length<br>5 = CSR out of range<br>6 = CRC error<br>7 = serializer wrong length<br>8 = serializer write fail |

### GENERAL_STATUS.EEPROM_CONFIG_STATUS

Status of configuration loaded from EEPROM.

Table 22: GENERAL_STATUS.EEPROM_CONFIG_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | GENERAL_STATUS.EEPROM_CONFIG_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 026h | EEPROM_CONFIG_STATUS[7:0] | | | | | | | |

| GENERAL_STATUS.EEPROM_CONFIG_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| EEPROM_CONFIG_STATUS[7:0] | R/O | 0 | Status code.<br>0x0 = success<br>0x1 = not found<br>0x2 = incomplete<br>0x3 = wrong offset<br>0x4 = wrong length<br>0x5 = SCSR out of range<br>0x6 = CRC error<br>0xA = corrupt header<br>0xB = EEPROM out of range |

## Module: STATUS

Live status of alarms and events.

Table 23: STATUS Register Index

| Offset (Hex) | Register Module Base Address: C03Ch | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | STATUS.I2CM_STATUS | I2C master status. |
| 001h | RESERVED | This register must not be modified from the read value |
| 002h | STATUS.SER0_STATUS | Status of serial interface 0 (main serial port). |
| 003h | STATUS.SER0_SPI_STATUS | Status of serial interface 0 (main serial port) SPI. |
| 004h | STATUS.SER0_I2C_STATUS | Status of serial interface 0 (main serial port) I2C. |
| 005h | STATUS.SER1_STATUS | Status of serial interface 1 (auxiliary serial port). |
| 006h | STATUS.SER1_SPI_STATUS | Status of serial interface 1 (auxiliary serial port) SPI. |
| 007h | STATUS.SER1_I2C_STATUS | Status of serial interface 1 (auxiliary serial port) I2C. |
| 008h | STATUS.IN0_MON_STATUS | Input 0 reference monitor status. |
| 009h | STATUS.IN1_MON_STATUS | Input 1 reference monitor status. |
| 00Ah | STATUS.IN2_MON_STATUS | Input 2 reference monitor status. |
| 00Bh | STATUS.IN3_MON_STATUS | Input 3 reference monitor status. |
| 00Ch | STATUS.IN4_MON_STATUS | Input 4 reference monitor status. |
| 00Dh | STATUS.IN5_MON_STATUS | Input 5 reference monitor status. |
| 00Eh | STATUS.IN6_MON_STATUS | Input 6 reference monitor status. |
| 00Fh | STATUS.IN7_MON_STATUS | Input 7 reference monitor status. |
| 010h | STATUS.IN8_MON_STATUS | Input 8 reference monitor status. |
| 011h | STATUS.IN9_MON_STATUS | Input 9 reference monitor status. |
| 012h | STATUS.IN10_MON_STATUS | Input 10 reference monitor status. |
| 013h | STATUS.IN11_MON_STATUS | Input 11 reference monitor status. |
| 014h | STATUS.IN12_MON_STATUS | Input 12 reference monitor status. |
| 015h | STATUS.IN13_MON_STATUS | Input 13 reference monitor status. |
| 016h | STATUS.IN14_MON_STATUS | Input 14 reference monitor status. |
| 017h | STATUS.IN15_MON_STATUS | Input 15 reference monitor status. |
| 018h | STATUS.DPLL0_STATUS | DPLL 0 status. |
| 019h | STATUS.DPLL1_STATUS | DPLL 1 status. |
| 01Ah | STATUS.DPLL2_STATUS | DPLL 2 status. |
| 01Bh | STATUS.DPLL3_STATUS | DPLL 3 status. |
| 01Ch | STATUS.DPLL4_STATUS | DPLL 4 status. |
| 01Dh | STATUS.DPLL5_STATUS | DPLL 5 status. |

Table 23: STATUS Register Index

| Offset (Hex) | Register Module Base Address: C03Ch | |
|---|---|---|
| | Individual Register Name | Register Description |
| 01Eh | STATUS.DPLL6_STATUS | DPLL 6 status. |
| 01Fh | STATUS.DPLL7_STATUS | DPLL 7 status. |
| 020h | STATUS.DPLL_SYS_STATUS | System DPLL status. |
| 021h | STATUS.SYS_APLL_STATUS | System APLL status. |
| 022h | STATUS.DPLL0_REF_STAT | DPLL 0 input reference status. |
| 023h | STATUS.DPLL1_REF_STAT | DPLL 1 input reference status. |
| 024h | STATUS.DPLL2_REF_STAT | DPLL 2 input reference status. |
| 025h | STATUS.DPLL3_REF_STAT | DPLL 3 input reference status. |
| 026h | STATUS.DPLL4_REF_STAT | DPLL 4 input reference status. |
| 027h | STATUS.DPLL5_REF_STAT | DPLL 5 input reference status. |
| 028h | STATUS.DPLL6_REF_STAT | DPLL 6 input reference status. |
| 029h | STATUS.DPLL7_REF_STAT | DPLL 7 input reference status. |
| 02Ah | STATUS.DPLL_SYS_REF_STAT | System DPLL input reference status. |
| 044h | STATUS.DPLL0_FILTER_STATUS | DPLL 0 loop filter status. |
| 04Ch | STATUS.DPLL1_FILTER_STATUS | DPLL 1 loop filter status. |
| 054h | STATUS.DPLL2_FILTER_STATUS | DPLL 2 loop filter status. |
| 05Ch | STATUS.DPLL3_FILTER_STATUS | DPLL 3 loop filter status. |
| 064h | STATUS.DPLL4_FILTER_STATUS | DPLL 4 loop filter status. |
| 06Ch | STATUS.DPLL5_FILTER_STATUS | DPLL 5 loop filter status. |
| 074h | STATUS.DPLL6_FILTER_STATUS | DPLL 6 loop filter status. |
| 07Ch | STATUS.DPLL7_FILTER_STATUS | DPLL 7 loop filter status. |
| 084h | STATUS.DPLL_SYS_FILTER_STATUS | System DPLL loop filter status. |
| 08Ah | STATUS.USER_GPIO0_TO_7_STATUS | User controlled GPIO level. |
| 08Bh | STATUS.USER_GPIO8_TO_15_STATUS | User controlled GPIO level. |
| 08Ch | STATUS.IN0_MON_FREQ_STATUS | Input 0 reference monitor frequency status and unit. |
| 08Eh | STATUS.IN1_MON_FREQ_STATUS | Input 1 reference monitor frequency status and unit. |
| 090h | STATUS.IN2_MON_FREQ_STATUS | Input 2 reference monitor frequency status and unit. |
| 092h | STATUS.IN3_MON_FREQ_STATUS | Input 3 reference monitor frequency status and unit. |
| 094h | STATUS.IN4_MON_FREQ_STATUS | Input 4 reference monitor frequency status and unit. |
| 096h | STATUS.IN5_MON_FREQ_STATUS | Input 5 reference monitor frequency status and unit. |
| 098h | STATUS.IN6_MON_FREQ_STATUS | Input 6 reference monitor frequency status and unit. |
| 09Ah | STATUS.IN7_MON_FREQ_STATUS | Input 7 reference monitor frequency status and unit. |

Table 23: STATUS Register Index

| Offset (Hex) | Register Module Base Address: C03Ch | |
|---|---|---|
| | Individual Register Name | Register Description |
| 09Ch | STATUS.IN8_MON_FREQ_STATUS | Input 8 reference monitor frequency status and unit. |
| 09Eh | STATUS.IN9_MON_FREQ_STATUS | Input 9 reference monitor frequency status and unit. |
| 0A0h | STATUS.IN10_MON_FREQ_STATUS | Input 10 reference monitor frequency status and unit. |
| 0A2h | STATUS.IN11_MON_FREQ_STATUS | Input 11 reference monitor frequency status and unit. |
| 0A4h | STATUS.IN12_MON_FREQ_STATUS | Input 12 reference monitor frequency status and unit. |
| 0A6h | STATUS.IN13_MON_FREQ_STATUS | Input 13 reference monitor frequency status and unit. |
| 0A8h | STATUS.IN14_MON_FREQ_STATUS | Input 14 reference monitor frequency status and unit. |
| 0AAh | STATUS.IN15_MON_FREQ_STATUS | Input 15 reference monitor frequency status and unit. |
| 0ACh | STATUS.OUTPUT_TDC_CFG_STATUS | Output TDC global status. |
| 0ADh | STATUS.OUTPUT_TDC0_STATUS | Output TDC 0 status. |
| 0AEh | STATUS.OUTPUT_TDC1_STATUS | Output TDC 1 status. |
| 0AFh | STATUS.OUTPUT_TDC2_STATUS | Output TDC 2 status. |
| 0B0h | STATUS.OUTPUT_TDC3_STATUS | Output TDC 3 status. |
| 0B4h | STATUS.OUTPUT_TDC0_MEASUREMENT | Output TDC 0 measurement status. |
| 0BAh | RESERVED | This register must not be modified from the read value |
| 0BBh | RESERVED | This register must not be modified from the read value |
| 0C4h | STATUS.OUTPUT_TDC1_MEASUREMENT | Output TDC 1 measurement status. |
| 0CAh | RESERVED | This register must not be modified from the read value |
| 0CBh | RESERVED | This register must not be modified from the read value |
| 0CCh | STATUS.OUTPUT_TDC2_MEASUREMENT | Output TDC 2 measurement status. |
| 0D2h | RESERVED | This register must not be modified from the read value |
| 0D3h | RESERVED | This register must not be modified from the read value |
| 0D4h | STATUS.OUTPUT_TDC3_MEASUREMENT | Output TDC 3 measurement status. |
| 0DAh | RESERVED | This register must not be modified from the read value |
| 0DBh | RESERVED | This register must not be modified from the read value |
| 0DCh | STATUS.DPLL0_PHASE_STATUS | Phase offset at output of decimator. |
| 0E1h | RESERVED | This register must not be modified from the read value |
| 0E2h | RESERVED | This register must not be modified from the read value |
| 0E3h | RESERVED | This register must not be modified from the read value |
| 0E4h | STATUS.DPLL1_PHASE_STATUS | Phase offset at output of decimator. |
| 0E9h | RESERVED | This register must not be modified from the read value |
| 0EAh | RESERVED | This register must not be modified from the read value |

Table 23: STATUS Register Index

| Offset (Hex) | Register Module Base Address: C03Ch | |
|---|---|---|
| | Individual Register Name | Register Description |
| 0EBh | RESERVED | This register must not be modified from the read value |
| 0ECh | STATUS.DPLL2_PHASE_STATUS | Phase offset at output of decimator. |
| 0F1h | RESERVED | This register must not be modified from the read value |
| 0F2h | RESERVED | This register must not be modified from the read value |
| 0F3h | RESERVED | This register must not be modified from the read value |
| 0F4h | STATUS.DPLL3_PHASE_STATUS | Phase offset at output of decimator. |
| 0F9h | RESERVED | This register must not be modified from the read value |
| 0FAh | RESERVED | This register must not be modified from the read value |
| 0FBh | RESERVED | This register must not be modified from the read value |
| 0FCh | STATUS.DPLL4_PHASE_STATUS | Phase offset at output of decimator. |
| 101h | RESERVED | This register must not be modified from the read value |
| 102h | RESERVED | This register must not be modified from the read value |
| 103h | RESERVED | This register must not be modified from the read value |
| 104h | STATUS.DPLL5_PHASE_STATUS | Phase offset at output of decimator. |
| 109h | RESERVED | This register must not be modified from the read value |
| 10Ah | RESERVED | This register must not be modified from the read value |
| 10Bh | RESERVED | This register must not be modified from the read value |
| 10Ch | STATUS.DPLL6_PHASE_STATUS | Phase offset at output of decimator. |
| 111h | RESERVED | This register must not be modified from the read value |
| 112h | RESERVED | This register must not be modified from the read value |
| 113h | RESERVED | This register must not be modified from the read value |
| 114h | STATUS.DPLL7_PHASE_STATUS | Phase offset at output of decimator. |
| 119h | RESERVED | This register must not be modified from the read value |
| 11Ah | RESERVED | This register must not be modified from the read value |
| 11Bh | RESERVED | This register must not be modified from the read value |
| 11Ch | STATUS.DPLL0_PHASE_PULL_IN_STATUS | DPLL0 phase pull-in status |
| 11Dh | STATUS.DPLL1_PHASE_PULL_IN_STATUS | DPLL1 phase pull-in status |
| 11Eh | STATUS.DPLL2_PHASE_PULL_IN_STATUS | DPLL2 phase pull-in status |
| 11Fh | STATUS.DPLL3_PHASE_PULL_IN_STATUS | DPLL3 phase pull-in status |

Table 23: STATUS Register Index

| Offset (Hex) | Register Module Base Address: C03Ch | |
|---|---|---|
| | Individual Register Name | Register Description |
| 120h | STATUS.DPLL4_PHASE_PULL_IN_STATUS | DPLL4 phase pull-in status |
| 121h | STATUS.DPLL5_PHASE_PULL_IN_STATUS | DPLL5 phase pull-in status |
| 122h | STATUS.DPLL6_PHASE_PULL_IN_STATUS | DPLL6 phase pull-in status |
| 123h | STATUS.DPLL7_PHASE_PULL_IN_STATUS | DPLL7 phase pull-in status |

### STATUS.I2CM_STATUS

Status of the I2C master (port selection and speed).

Table 24: STATUS.I2CM_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.I2CM_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | RESERVED[7:4] | | | | I2CM_SPEED[3:2] | | I2CM_PORT_SEL[1:0] | |

| STATUS.I2CM_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| I2CM_SPEED[3:2] | R/O | 0 | I2C Master speed.<br>Indicates the I2C speed.<br>0 = 100 KHz<br>1 = 400 KHz<br>2 = 1 MHz |
| I2CM_PORT_SEL[1:0] | R/O | 0 | I2C Master port pin selection.<br>Indicates the pins the I2C master is connected to.<br>0 = I2C master<br>1 = serial interface 0<br>2 = serial interface 1 |

### STATUS.SER0_STATUS

Status of serial interface 0 (main serial port).

Table 25: STATUS.SER0_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.SER0_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | RESERVED[7:3] | | | | | ADDRESS_SIZE[2] | MODE[1:0] | |

| STATUS.SER0_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| ADDRESS_SIZE[2] | R/O | 0 | Serial Interface 0 (main serial port) address size.<br>Indicates the SSI address size.<br>0 = 1-byte<br>1 = 2-byte |
| MODE[1:0] | R/O | 0 | Serial interface 0 (main serial port) mode.<br>Indicates the SSI protocol.<br>0 = undefined<br>1 = I2C<br>2 = SPI<br>3 = disabled |

### STATUS.SER0_SPI_STATUS

Status of serial interface 0 (main serial port) SPI.

Table 26: STATUS.SER0_SPI_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.SER0_SPI_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 003h | RESERVED[7:5] | | | SPI_SDO_DELAY[4] | SPI_CLOCK_SELECTION[3] | SPI_DUPLEX_MODE[2] | RESERVED[1:0] | |

| STATUS.SER0_SPI_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SPI_SDO_DELAY[4] | R/O | 0 | SPI delay SDO driving edge.<br>0 = driving edge used for SDO<br>1 = SDO driving edge delayed half-cycle of SCLK |
| SPI_CLOCK_SELECTION[3] | R/O | 0 | SPI Clock Selection for SDI sampling.<br>Indicates if the SPI clock selection is on a rising or falling edge.<br>0 = rising edge<br>1 = falling edge |
| SPI_DUPLEX_MODE[2] | R/O | 0 | SPI 4-wire or 3-wire.<br>Indicates if the SPI is in full duplex or half duplex mode.<br>0 = full duplex<br>1 = half duplex |
| RESERVED | N/A | - | This field must not be modified from the read value |

### STATUS.SER0_I2C_STATUS

Status of serial interface 0 (main serial port) I2C.

Table 27: STATUS.SER0_I2C_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.SER0_I2C_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | RESERVED[7] | DEVICE_ADDRESS[6:0] | | | | | | |

| STATUS.SER0_I2C_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DEVICE_ADDRESS[6:0] | R/O | 0 | I2C address of this I2C slave.<br>7-bit I2C address. |

### STATUS.SER1_STATUS

Status of serial interface 1 (auxiliary serial port).

Table 28: STATUS.SER1_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.SER1_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 005h | RESERVED[7:3] | | | | | ADDRESS_SIZE[2] | MODE[1:0] | |

| STATUS.SER1_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| ADDRESS_SIZE[2] | R/O | 0 | Serial interface 1 (auxiliary serial port) address size.<br>Indicates the SSI address size.<br>0 = 1-byte<br>1 = 2-byte |
| MODE[1:0] | R/O | 0 | Serial interface 1 (auxiliary serial port) mode.<br>Indicates the SSI protocol.<br>0 = undefined<br>1 = I2C<br>2 = SPI<br>3 = disabled |

### STATUS.SER1_SPI_STATUS

Status of serial interface 1 (auxiliary serial port) SPI.

Table 29: STATUS.SER1_SPI_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.SER1_SPI_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 006h | RESERVED[7:5] | | | SPI_SDO_DELAY[4] | SPI_CLOCK_SELECTION[3] | SPI_DUPLEX_MODE[2] | RESERVED[1:0] | |

| STATUS.SER1_SPI_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SPI_SDO_DELAY[4] | R/O | 0 | SPI delay SDO driving edge.<br>0 = driving edge used for SDO<br>1 = SDO driving edge delayed half-cycle of SCLK |
| SPI_CLOCK_SELECTION[3] | R/O | 0 | SPI Clock Selection for SDI sampling.<br>Indicates if the SPI clock selection is on a rising or falling edge.<br>0 = rising edge<br>1 = falling edge |
| SPI_DUPLEX_MODE[2] | R/O | 0 | SPI 4-wire or 3-wire.<br>Indicates if the SPI is in full duplex or half duplex mode.<br>0 = full duplex<br>1 = half duplex |
| RESERVED | N/A | - | This field must not be modified from the read value |

### STATUS.SER1_I2C_STATUS

Status of serial interface 1 (auxiliary serial port) I2C.

Table 30: STATUS.SER1_I2C_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.SER1_I2C_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 007h | RESERVED[7] | DEVICE_ADDRESS[6:0] | | | | | | |

| STATUS.SER1_I2C_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DEVICE_ADDRESS[6:0] | R/O | 0 | I2C address of this I2C slave.<br>7-bit I2C address. |

### STATUS.IN0_MON_STATUS

Input 0 reference monitor status.

Table 31: STATUS.IN0_MON_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN0_MON_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 008h | IN0_TRANS_DETECT_STICKY[7] | IN0_FREQ_OFFS_LIM_STICKY[6] | IN0_NO_ACTIVITY_STICKY[5] | IN0_LOS_STICKY[4] | IN0_TRANS_DETECT_LIVE[3] | IN0_FREQ_OFFS_LIM_LIVE[2] | IN0_NO_ACTIVITY_LIVE[1] | IN0_LOS_LIVE[0] |

| STATUS.IN0_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN0_TRANS_DETECT_STICKY[7] | R/O | 0 | Transient detector sticky bit.<br>Indicates a change of in0_trans_detect_live bit.<br>0 = no change<br>1 = live status changed |
| IN0_FREQ_OFFS_LIM_STICKY[6] | R/O | 0 | Frequency offset limit sticky bit.<br>Indicates a change of in0_freq_offs_lim_live bit.<br>0 = no change<br>1 = live status changed |
| IN0_NO_ACTIVITY_STICKY[5] | R/O | 0 | No activity sticky bit.<br>Indicates a change of in0_no_activity_live bit.<br>0 = no change<br>1 = live status changed |
| IN0_LOS_STICKY[4] | R/O | 0 | LOS sticky bit.<br>Indicates a change of in0_los_live bit.<br>0 = no change<br>1 = live status changed |
| IN0_TRANS_DETECT_LIVE[3] | R/O | 0 | Transient detector live bit.<br>Indicates that a transient is detected for input 0.<br>0 = inactive<br>1 = active |
| IN0_FREQ_OFFS_LIM_LIVE[2] | R/O | 0 | Frequency offset limit live status.<br>Indicates that the current frequency offset exceeds the limit for input 0.<br>0 = inactive<br>1 = active |
| IN0_NO_ACTIVITY_LIVE[1] | R/O | 0 | No activity live status.<br>Indicates no activity on input 0.<br>0 = inactive<br>1 = active |
| IN0_LOS_LIVE[0] | R/O | 0 | LOS live status.<br>Indicates loss of signal on input 0.<br>0 = inactive<br>1 = active |

### STATUS.IN1_MON_STATUS

Input 1 reference monitor status.

Table 32: STATUS.IN1_MON_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN1_MON_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 009h | IN1_TRANS_DETECT_STICKY[7] | IN1_FREQ_OFFS_LIM_STICKY[6] | IN1_NO_ACTIVITY_STICKY[5] | IN1_LOS_STICKY[4] | IN1_TRANS_DETECT_LIVE[3] | IN1_FREQ_OFFS_LIM_LIVE[2] | IN1_NO_ACTIVITY_LIVE[1] | IN1_LOS_LIVE[0] |

| STATUS.IN1_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN1_TRANS_DETECT_STICKY[7] | R/O | 0 | Transient detector sticky bit.<br>Indicates a change of in1_trans_detect_live bit.<br>0 = no change<br>1 = live status changed |
| IN1_FREQ_OFFS_LIM_STICKY[6] | R/O | 0 | Frequency offset limit sticky bit.<br>Indicates a change of in1_freq_offs_lim_live bit.<br>0 = no change<br>1 = live status changed |
| IN1_NO_ACTIVITY_STICKY[5] | R/O | 0 | No activity sticky bit.<br>Indicates a change of in1_no_activity_live bit.<br>0 = no change<br>1 = live status changed |
| IN1_LOS_STICKY[4] | R/O | 0 | LOS sticky bit.<br>Indicates a change of in1_los_live bit.<br>0 = no change<br>1 = live status changed |
| IN1_TRANS_DETECT_LIVE[3] | R/O | 0 | Transient detector live bit.<br>Indicates that a transient is detected for input 1.<br>0 = inactive<br>1 = active |
| IN1_FREQ_OFFS_LIM_LIVE[2] | R/O | 0 | Frequency offset limit live status.<br>Indicates that the current frequency offset exceeds the limit for input 1.<br>0 = inactive<br>1 = active |
| IN1_NO_ACTIVITY_LIVE[1] | R/O | 0 | No activity live status.<br>Indicates no activity on input 1.<br>0 = inactive<br>1 = active |
| IN1_LOS_LIVE[0] | R/O | 0 | LOS live status.<br>Indicates loss of signal on input 1.<br>0 = inactive<br>1 = active |

### STATUS.IN2_MON_STATUS

Input 2 reference monitor status.

Table 33: STATUS.IN2_MON_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN2_MON_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ah | IN2_TRANS_DETECT_STICKY[7] | IN2_FREQ_OFFS_LIM_STICKY[6] | IN2_NO_ACTIVITY_STICKY[5] | IN2_LOS_STICKY[4] | IN2_TRANS_DETECT_LIVE[3] | IN2_FREQ_OFFS_LIM_LIVE[2] | IN2_NO_ACTIVITY_LIVE[1] | IN2_LOS_LIVE[0] |

| STATUS.IN2_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN2_TRANS_DETECT_STICKY[7] | R/O | 0 | Transient detector sticky bit.<br>Indicates a change of in2_trans_detect_live bit.<br>0 = no change<br>1 = live status changed |
| IN2_FREQ_OFFS_LIM_STICKY[6] | R/O | 0 | Frequency offset limit sticky bit.<br>Indicates a change of in2_freq_offs_lim_live bit.<br>0 = no change<br>1 = live status changed |
| IN2_NO_ACTIVITY_STICKY[5] | R/O | 0 | No activity sticky bit.<br>Indicates a change of in2_no_activity_live bit.<br>0 = no change<br>1 = live status changed |
| IN2_LOS_STICKY[4] | R/O | 0 | LOS sticky bit.<br>Indicates a change of in2_los_live bit.<br>0 = no change<br>1 = live status changed |
| IN2_TRANS_DETECT_LIVE[3] | R/O | 0 | Transient detector live bit.<br>Indicates that a transient is detected for input 2.<br>0 = inactive<br>1 = active |
| IN2_FREQ_OFFS_LIM_LIVE[2] | R/O | 0 | Frequency offset limit live status.<br>Indicates that the current frequency offset exceeds the limit for input 2.<br>0 = inactive<br>1 = active |
| IN2_NO_ACTIVITY_LIVE[1] | R/O | 0 | No activity live status.<br>Indicates no activity on input 2.<br>0 = inactive<br>1 = active |
| IN2_LOS_LIVE[0] | R/O | 0 | LOS live status.<br>Indicates loss of signal on input 2.<br>0 = inactive<br>1 = active |

### STATUS.IN3_MON_STATUS

Input 3 reference monitor status.

Table 34: STATUS.IN3_MON_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN3_MON_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Bh | IN3_TRANS_DETECT_STICKY[7] | IN3_FREQ_OFFS_LIM_STICKY[6] | IN3_NO_ACTIVITY_STICKY[5] | IN3_LOS_STICKY[4] | IN3_TRANS_DETECT_LIVE[3] | IN3_FREQ_OFFS_LIM_LIVE[2] | IN3_NO_ACTIVITY_LIVE[1] | IN3_LOS_LIVE[0] |

| STATUS.IN3_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN3_TRANS_DETECT_STICKY[7] | R/O | 0 | Transient detector sticky bit.<br>Indicates a change of in3_trans_detect_live bit.<br>0 = no change<br>1 = live status changed |
| IN3_FREQ_OFFS_LIM_STICKY[6] | R/O | 0 | Frequency offset limit sticky bit.<br>Indicates a change of in3_freq_offs_lim_live bit.<br>0 = no change<br>1 = live status changed |
| IN3_NO_ACTIVITY_STICKY[5] | R/O | 0 | No activity sticky bit.<br>Indicates a change of in3_no_activity_live bit.<br>0 = no change<br>1 = live status changed |
| IN3_LOS_STICKY[4] | R/O | 0 | LOS sticky bit.<br>Indicates a change of in3_los_live bit.<br>0 = no change<br>1 = live status changed |
| IN3_TRANS_DETECT_LIVE[3] | R/O | 0 | Transient detector live bit.<br>Indicates that a transient is detected for input 3.<br>0 = inactive<br>1 = active |
| IN3_FREQ_OFFS_LIM_LIVE[2] | R/O | 0 | Frequency offset limit live status.<br>Indicates that the current frequency offset exceeds the limit for input 3.<br>0 = inactive<br>1 = active |
| IN3_NO_ACTIVITY_LIVE[1] | R/O | 0 | No activity live status.<br>Indicates no activity on input 3.<br>0 = inactive<br>1 = active |
| IN3_LOS_LIVE[0] | R/O | 0 | LOS live status.<br>Indicates loss of signal on input 3.<br>0 = inactive<br>1 = active |

### STATUS.IN4_MON_STATUS

Input 4 reference monitor status.

Table 35: STATUS.IN4_MON_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN4_MON_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ch | IN4_TRANS_DETECT_STICKY[7] | IN4_FREQ_OFFS_LIM_STICKY[6] | IN4_NO_ACTIVITY_STICKY[5] | IN4_LOS_STICKY[4] | IN4_TRANS_DETECT_LIVE[3] | IN4_FREQ_OFFS_LIM_LIVE[2] | IN4_NO_ACTIVITY_LIVE[1] | IN4_LOS_LIVE[0] |

| STATUS.IN4_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN4_TRANS_DETECT_STICKY[7] | R/O | 0 | Transient detector sticky bit.<br>Indicates a change of in4_trans_detect_live bit.<br>0 = no change<br>1 = live status changed |
| IN4_FREQ_OFFS_LIM_STICKY[6] | R/O | 0 | Frequency offset limit sticky bit.<br>Indicates a change of in4_freq_offs_lim_live bit.<br>0 = no change<br>1 = live status changed |
| IN4_NO_ACTIVITY_STICKY[5] | R/O | 0 | No activity sticky bit.<br>Indicates a change of in4_no_activity_live bit.<br>0 = no change<br>1 = live status changed |
| IN4_LOS_STICKY[4] | R/O | 0 | LOS sticky bit.<br>Indicates a change of in4_los_live bit.<br>0 = no change<br>1 = live status changed |
| IN4_TRANS_DETECT_LIVE[3] | R/O | 0 | Transient detector live bit.<br>Indicates that a transient is detected for input 4.<br>0 = inactive<br>1 = active |
| IN4_FREQ_OFFS_LIM_LIVE[2] | R/O | 0 | Frequency offset limit live status.<br>Indicates that the current frequency offset exceeds the limit for input 4.<br>0 = inactive<br>1 = active |
| IN4_NO_ACTIVITY_LIVE[1] | R/O | 0 | No activity live status.<br>Indicates no activity on input 4.<br>0 = inactive<br>1 = active |
| IN4_LOS_LIVE[0] | R/O | 0 | LOS live status.<br>Indicates loss of signal on input 4.<br>0 = inactive<br>1 = active |

### STATUS.IN5_MON_STATUS

Input 5 reference monitor status.

Table 36: STATUS.IN5_MON_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN5_MON_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Dh | IN5_TRANS_DETECT_STICKY[7] | IN5_FREQ_OFFS_LIM_STICKY[6] | IN5_NO_ACTIVITY_STICKY[5] | IN5_LOS_STICKY[4] | IN5_TRANS_DETECT_LIVE[3] | IN5_FREQ_OFFS_LIM_LIVE[2] | IN5_NO_ACTIVITY_LIVE[1] | IN5_LOS_LIVE[0] |

| STATUS.IN5_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN5_TRANS_DETECT_STICKY[7] | R/O | 0 | Transient detector sticky bit.<br>Indicates a change of in5_trans_detect_live bit.<br>0 = no change<br>1 = live status changed |
| IN5_FREQ_OFFS_LIM_STICKY[6] | R/O | 0 | Frequency offset limit sticky bit.<br>Indicates a change of in5_freq_offs_lim_live bit.<br>0 = no change<br>1 = live status changed |
| IN5_NO_ACTIVITY_STICKY[5] | R/O | 0 | No activity sticky bit.<br>Indicates a change of in5_no_activity_live bit.<br>0 = no change<br>1 = live status changed |
| IN5_LOS_STICKY[4] | R/O | 0 | LOS sticky bit.<br>Indicates a change of in5_los_live bit.<br>0 = no change<br>1 = live status changed |
| IN5_TRANS_DETECT_LIVE[3] | R/O | 0 | Transient detector live bit.<br>Indicates that a transient is detected for input 5.<br>0 = inactive<br>1 = active |
| IN5_FREQ_OFFS_LIM_LIVE[2] | R/O | 0 | Frequency offset limit live status.<br>Indicates that the current frequency offset exceeds the limit for input 5.<br>0 = inactive<br>1 = active |
| IN5_NO_ACTIVITY_LIVE[1] | R/O | 0 | No activity live status.<br>Indicates no activity on input 5.<br>0 = inactive<br>1 = active |
| IN5_LOS_LIVE[0] | R/O | 0 | LOS live status.<br>Indicates loss of signal on input 5.<br>0 = inactive<br>1 = active |

### STATUS.IN6_MON_STATUS

Input 6 reference monitor status.

Table 37: STATUS.IN6_MON_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN6_MON_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Eh | IN6_TRANS_DETECT_STICKY[7] | IN6_FREQ_OFFS_LIM_STICKY[6] | IN6_NO_ACTIVITY_STICKY[5] | IN6_LOS_STICKY[4] | IN6_TRANS_DETECT_LIVE[3] | IN6_FREQ_OFFS_LIM_LIVE[2] | IN6_NO_ACTIVITY_LIVE[1] | IN6_LOS_LIVE[0] |

| STATUS.IN6_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN6_TRANS_DETECT_STICKY[7] | R/O | 0 | Transient detector sticky bit.<br>Indicates a change of in6_trans_detect_live bit.<br>0 = no change<br>1 = live status changed |
| IN6_FREQ_OFFS_LIM_STICKY[6] | R/O | 0 | Frequency offset limit sticky bit.<br>Indicates a change of in6_freq_offs_lim_live bit.<br>0 = no change<br>1 = live status changed |
| IN6_NO_ACTIVITY_STICKY[5] | R/O | 0 | No activity sticky bit.<br>Indicates a change of in6_no_activity_live bit.<br>0 = no change<br>1 = live status changed |
| IN6_LOS_STICKY[4] | R/O | 0 | LOS sticky bit.<br>Indicates a change of in6_los_live bit.<br>0 = no change<br>1 = live status changed |
| IN6_TRANS_DETECT_LIVE[3] | R/O | 0 | Transient detector live bit.<br>Indicates that a transient is detected for input 6.<br>0 = inactive<br>1 = active |
| IN6_FREQ_OFFS_LIM_LIVE[2] | R/O | 0 | Frequency offset limit live status.<br>Indicates that the current frequency offset exceeds the limit for input 6.<br>0 = inactive<br>1 = active |
| IN6_NO_ACTIVITY_LIVE[1] | R/O | 0 | No activity live status.<br>Indicates no activity on input 6.<br>0 = inactive<br>1 = active |
| IN6_LOS_LIVE[0] | R/O | 0 | LOS live status.<br>Indicates loss of signal on input 6.<br>0 = inactive<br>1 = active |

### STATUS.IN7_MON_STATUS

Input 7 reference monitor status.

Table 38: STATUS.IN7_MON_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN7_MON_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Fh | IN7_TRANS_DETECT_STICKY[7] | IN7_FREQ_OFFS_LIM_STICKY[6] | IN7_NO_ACTIVITY_STICKY[5] | IN7_LOS_STICKY[4] | IN7_TRANS_DETECT_LIVE[3] | IN7_FREQ_OFFS_LIM_LIVE[2] | IN7_NO_ACTIVITY_LIVE[1] | IN7_LOS_LIVE[0] |

| STATUS.IN7_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN7_TRANS_DETECT_STICKY[7] | R/O | 0 | Transient detector sticky bit.<br>Indicates a change of in7_trans_detect_live bit.<br>0 = no change<br>1 = live status changed |
| IN7_FREQ_OFFS_LIM_STICKY[6] | R/O | 0 | Frequency offset limit sticky bit.<br>Indicates a change of in7_freq_offs_lim_live bit.<br>0 = no change<br>1 = live status changed |
| IN7_NO_ACTIVITY_STICKY[5] | R/O | 0 | No activity sticky bit.<br>Indicates a change of in7_no_activity_live bit.<br>0 = no change<br>1 = live status changed |
| IN7_LOS_STICKY[4] | R/O | 0 | LOS sticky bit.<br>Indicates a change of in7_los_live bit.<br>0 = no change<br>1 = live status changed |
| IN7_TRANS_DETECT_LIVE[3] | R/O | 0 | Transient detector live bit.<br>Indicates that a transient is detected for input 7.<br>0 = inactive<br>1 = active |
| IN7_FREQ_OFFS_LIM_LIVE[2] | R/O | 0 | Frequency offset limit live status.<br>Indicates that the current frequency offset exceeds the limit for input 7.<br>0 = inactive<br>1 = active |
| IN7_NO_ACTIVITY_LIVE[1] | R/O | 0 | No activity live status.<br>Indicates no activity on input 7.<br>0 = inactive<br>1 = active |
| IN7_LOS_LIVE[0] | R/O | 0 | LOS live status.<br>Indicates loss of signal on input 7.<br>0 = inactive<br>1 = active |

### STATUS.IN8_MON_STATUS

Input 8 reference monitor status.

Table 39: STATUS.IN8_MON_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN8_MON_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 010h | IN8_TRANS_DETECT_STICKY[7] | IN8_FREQ_OFFS_LIM_STICKY[6] | IN8_NO_ACTIVITY_STICKY[5] | IN8_LOS_STICKY[4] | IN8_TRANS_DETECT_LIVE[3] | IN8_FREQ_OFFS_LIM_LIVE[2] | IN8_NO_ACTIVITY_LIVE[1] | IN8_LOS_LIVE[0] |

| STATUS.IN8_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN8_TRANS_DETECT_STICKY[7] | R/O | 0 | Transient detector sticky bit.<br>Indicates a change of in8_trans_detect_live bit.<br>0 = no change<br>1 = live status changed |
| IN8_FREQ_OFFS_LIM_STICKY[6] | R/O | 0 | Frequency offset limit sticky bit.<br>Indicates a change of in8_freq_offs_lim_live bit.<br>0 = no change<br>1 = live status changed |
| IN8_NO_ACTIVITY_STICKY[5] | R/O | 0 | No activity sticky bit.<br>Indicates a change of in8_no_activity_live bit.<br>0 = no change<br>1 = live status changed |
| IN8_LOS_STICKY[4] | R/O | 0 | LOS sticky bit.<br>Indicates a change of in8_los_live bit.<br>0 = no change<br>1 = live status changed |
| IN8_TRANS_DETECT_LIVE[3] | R/O | 0 | Transient detector live bit.<br>Indicates that a transient is detected for input 8.<br>0 = inactive<br>1 = active |
| IN8_FREQ_OFFS_LIM_LIVE[2] | R/O | 0 | Frequency offset limit live status.<br>Indicates that the current frequency offset exceeds the limit for input 8.<br>0 = inactive<br>1 = active |
| IN8_NO_ACTIVITY_LIVE[1] | R/O | 0 | No activity live status.<br>Indicates no activity on input 8.<br>0 = inactive<br>1 = active |
| IN8_LOS_LIVE[0] | R/O | 0 | LOS live status.<br>Indicates loss of signal on input 8.<br>0 = inactive<br>1 = active |

### STATUS.IN9_MON_STATUS

Input 9 reference monitor status.

Table 40: STATUS.IN9_MON_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN9_MON_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 011h | IN9_TRANS_DETECT_STICKY[7] | IN9_FREQ_OFFS_LIM_STICKY[6] | IN9_NO_ACTIVITY_STICKY[5] | IN9_LOS_STICKY[4] | IN9_TRANS_DETECT_LIVE[3] | IN9_FREQ_OFFS_LIM_LIVE[2] | IN9_NO_ACTIVITY_LIVE[1] | IN9_LOS_LIVE[0] |

| STATUS.IN9_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN9_TRANS_DETECT_STICKY[7] | R/O | 0 | Transient detector sticky bit.<br>Indicates a change of in9_trans_detect_live bit.<br>0 = no change<br>1 = live status changed |
| IN9_FREQ_OFFS_LIM_STICKY[6] | R/O | 0 | Frequency offset limit sticky bit.<br>Indicates a change of in9_freq_offs_lim_live bit.<br>0 = no change<br>1 = live status changed |
| IN9_NO_ACTIVITY_STICKY[5] | R/O | 0 | No activity sticky bit.<br>Indicates a change of in9_no_activity_live bit.<br>0 = no change<br>1 = live status changed |
| IN9_LOS_STICKY[4] | R/O | 0 | LOS sticky bit.<br>Indicates a change of in9_los_live bit.<br>0 = no change<br>1 = live status changed |
| IN9_TRANS_DETECT_LIVE[3] | R/O | 0 | Transient detector live bit.<br>Indicates that a transient is detected for input 9.<br>0 = inactive<br>1 = active |
| IN9_FREQ_OFFS_LIM_LIVE[2] | R/O | 0 | Frequency offset limit live status.<br>Indicates that the current frequency offset exceeds the limit for input 9.<br>0 = inactive<br>1 = active |
| IN9_NO_ACTIVITY_LIVE[1] | R/O | 0 | No activity live status.<br>Indicates no activity on input 9.<br>0 = inactive<br>1 = active |
| IN9_LOS_LIVE[0] | R/O | 0 | LOS live status.<br>Indicates loss of signal on input 9.<br>0 = inactive<br>1 = active |

### STATUS.IN10_MON_STATUS

Input 10 reference monitor status.

Table 41: STATUS.IN10_MON_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN10_MON_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 012h | IN10_TRANS_DETECT_STICKY[7] | IN10_FREQ_OFFS_LIM_STICKY[6] | IN10_NO_ACTIVITY_STICKY[5] | IN10_LOS_STICKY[4] | IN10_TRANS_DETECT_LIVE[3] | IN10_FREQ_OFFS_LIM_LIVE[2] | IN10_NO_ACTIVITY_LIVE[1] | IN10_LOS_LIVE[0] |

| STATUS.IN10_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN10_TRANS_DETECT_STICKY[7] | R/O | 0 | Transient detector sticky bit.<br>Indicates a change of in10_trans_detect_live bit.<br>0 = no change<br>1 = live status changed |
| IN10_FREQ_OFFS_LIM_STICKY[6] | R/O | 0 | Frequency offset limit sticky bit.<br>Indicates a change of in10_freq_offs_lim_live bit.<br>0 = no change<br>1 = live status changed |
| IN10_NO_ACTIVITY_STICKY[5] | R/O | 0 | No activity sticky bit.<br>Indicates a change of in10_no_activity_live bit.<br>0 = no change<br>1 = live status changed |
| IN10_LOS_STICKY[4] | R/O | 0 | LOS sticky bit.<br>Indicates a change of in10_los_live bit.<br>0 = no change<br>1 = live status changed |
| IN10_TRANS_DETECT_LIVE[3] | R/O | 0 | Transient detector live bit.<br>Indicates that a transient is detected for input 10.<br>0 = inactive<br>1 = active |
| IN10_FREQ_OFFS_LIM_LIVE[2] | R/O | 0 | Frequency offset limit live status.<br>Indicates that the current frequency offset exceeds the limit for input 10.<br>0 = inactive<br>1 = active |
| IN10_NO_ACTIVITY_LIVE[1] | R/O | 0 | No activity live status.<br>Indicates no activity on input 10.<br>0 = inactive<br>1 = active |
| IN10_LOS_LIVE[0] | R/O | 0 | LOS live status.<br>Indicates loss of signal on input 10.<br>0 = inactive<br>1 = active |

### STATUS.IN11_MON_STATUS

Input 11 reference monitor status.

Table 42: STATUS.IN11_MON_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN11_MON_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 013h | IN11_TRANS_DETECT_STICKY[7] | IN11_FREQ_OFFS_LIM_STICKY[6] | IN11_NO_ACTIVITY_STICKY[5] | IN11_LOS_STICKY[4] | IN11_TRANS_DETECT_LIVE[3] | IN11_FREQ_OFFS_LIM_LIVE[2] | IN11_NO_ACTIVITY_LIVE[1] | IN11_LOS_LIVE[0] |

| STATUS.IN11_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN11_TRANS_DETECT_STICKY[7] | R/O | 0 | Transient detector sticky bit.<br>Indicates a change of in11_trans_detect_live bit.<br>0 = no change<br>1 = live status changed |
| IN11_FREQ_OFFS_LIM_STICKY[6] | R/O | 0 | Frequency offset limit sticky bit.<br>Indicates a change of in11_freq_offs_lim_live bit.<br>0 = no change<br>1 = live status changed |
| IN11_NO_ACTIVITY_STICKY[5] | R/O | 0 | No activity sticky bit.<br>Indicates a change of in11_no_activity_live bit.<br>0 = no change<br>1 = live status changed |
| IN11_LOS_STICKY[4] | R/O | 0 | LOS sticky bit.<br>Indicates a change of in11_los_live bit.<br>0 = no change<br>1 = live status changed |
| IN11_TRANS_DETECT_LIVE[3] | R/O | 0 | Transient detector live bit.<br>Indicates that a transient is detected for input 11.<br>0 = inactive<br>1 = active |
| IN11_FREQ_OFFS_LIM_LIVE[2] | R/O | 0 | Frequency offset limit live status.<br>Indicates that the current frequency offset exceeds the limit for input 11.<br>0 = inactive<br>1 = active |
| IN11_NO_ACTIVITY_LIVE[1] | R/O | 0 | No activity live status.<br>Indicates no activity on input 11.<br>0 = inactive<br>1 = active |
| IN11_LOS_LIVE[0] | R/O | 0 | LOS live status.<br>Indicates loss of signal on input 11.<br>0 = inactive<br>1 = active |

### STATUS.IN12_MON_STATUS

Input 12 reference monitor status.

Table 43: STATUS.IN12_MON_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN12_MON_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 014h | IN12_TRANS_DETECT_STICKY[7] | IN12_FREQ_OFFS_LIM_STICKY[6] | IN12_NO_ACTIVITY_STICKY[5] | IN12_LOS_STICKY[4] | IN12_TRANS_DETECT_LIVE[3] | IN12_FREQ_OFFS_LIM_LIVE[2] | IN12_NO_ACTIVITY_LIVE[1] | IN12_LOS_LIVE[0] |

| STATUS.IN12_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN12_TRANS_DETECT_STICKY[7] | R/O | 0 | Transient detector sticky bit.<br>Indicates a change of in12_trans_detect_live bit.<br>0 = no change<br>1 = live status changed |
| IN12_FREQ_OFFS_LIM_STICKY[6] | R/O | 0 | Frequency offset limit sticky bit.<br>Indicates a change of in12_freq_offs_lim_live bit.<br>0 = no change<br>1 = live status changed |
| IN12_NO_ACTIVITY_STICKY[5] | R/O | 0 | No activity sticky bit.<br>Indicates a change of in12_no_activity_live bit.<br>0 = no change<br>1 = live status changed |
| IN12_LOS_STICKY[4] | R/O | 0 | LOS sticky bit.<br>Indicates a change of in12_los_live bit.<br>0 = no change<br>1 = live status changed |
| IN12_TRANS_DETECT_LIVE[3] | R/O | 0 | Transient detector live bit.<br>Indicates that a transient is detected for input 12.<br>0 = inactive<br>1 = active |
| IN12_FREQ_OFFS_LIM_LIVE[2] | R/O | 0 | Frequency offset limit live status.<br>Indicates that the current frequency offset exceeds the limit for input 12.<br>0 = inactive<br>1 = active |
| IN12_NO_ACTIVITY_LIVE[1] | R/O | 0 | No activity live status.<br>Indicates no activity on input 12.<br>0 = inactive<br>1 = active |
| IN12_LOS_LIVE[0] | R/O | 0 | LOS live status.<br>Indicates loss of signal on input 12.<br>0 = inactive<br>1 = active |

### STATUS.IN13_MON_STATUS

Input 13 reference monitor status.

Table 44: STATUS.IN13_MON_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN13_MON_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 015h | IN13_TRANS_DETECT_STICKY[7] | IN13_FREQ_OFFS_LIM_STICKY[6] | IN13_NO_ACTIVITY_STICKY[5] | IN13_LOS_STICKY[4] | IN13_TRANS_DETECT_LIVE[3] | IN13_FREQ_OFFS_LIM_LIVE[2] | IN13_NO_ACTIVITY_LIVE[1] | IN13_LOS_LIVE[0] |

| STATUS.IN13_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN13_TRANS_DETECT_STICKY[7] | R/O | 0 | Transient detector sticky bit.<br>Indicates a change of in13_trans_detect_live bit.<br>0 = no change<br>1 = live status changed |
| IN13_FREQ_OFFS_LIM_STICKY[6] | R/O | 0 | Frequency offset limit sticky bit.<br>Indicates a change of in13_freq_offs_lim_live bit.<br>0 = no change<br>1 = live status changed |
| IN13_NO_ACTIVITY_STICKY[5] | R/O | 0 | No activity sticky bit.<br>Indicates a change of in13_no_activity_live bit.<br>0 = no change<br>1 = live status changed |
| IN13_LOS_STICKY[4] | R/O | 0 | LOS sticky bit.<br>Indicates a change of in13_los_live bit.<br>0 = no change<br>1 = live status changed |
| IN13_TRANS_DETECT_LIVE[3] | R/O | 0 | Transient detector live bit.<br>Indicates that a transient is detected for input 13.<br>0 = inactive<br>1 = active |
| IN13_FREQ_OFFS_LIM_LIVE[2] | R/O | 0 | Frequency offset limit live status.<br>Indicates that the current frequency offset exceeds the limit for input 13.<br>0 = inactive<br>1 = active |
| IN13_NO_ACTIVITY_LIVE[1] | R/O | 0 | No activity live status.<br>Indicates no activity on input 13.<br>0 = inactive<br>1 = active |
| IN13_LOS_LIVE[0] | R/O | 0 | LOS live status.<br>Indicates loss of signal on input 13.<br>0 = inactive<br>1 = active |

### STATUS.IN14_MON_STATUS

Input 14 reference monitor status.

-

Table 45: STATUS.IN14_MON_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN14_MON_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 016h | IN14_TRANS_DETECT_STICKY[7] | IN14_FREQ_OFFS_LIM_STICKY[6] | IN14_NO_ACTIVITY_STICKY[5] | IN14_LOS_STICKY[4] | IN14_TRANS_DETECT_LIVE[3] | IN14_FREQ_OFFS_LIM_LIVE[2] | IN14_NO_ACTIVITY_LIVE[1] | IN14_LOS_LIVE[0] |

| STATUS.IN14_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN14_TRANS_DETECT_STICKY[7] | R/O | 0 | Transient detector sticky bit.<br>Indicates a change of in14_trans_detect_live bit.<br>0 = no change<br>1 = live status changed |
| IN14_FREQ_OFFS_LIM_STICKY[6] | R/O | 0 | Frequency offset limit sticky bit.<br>Indicates a change of in14_freq_offs_lim_live bit.<br>0 = no change<br>1 = live status changed |
| IN14_NO_ACTIVITY_STICKY[5] | R/O | 0 | No activity sticky bit.<br>Indicates a change of in14_no_activity_live bit.<br>0 = no change<br>1 = live status changed |
| IN14_LOS_STICKY[4] | R/O | 0 | LOS sticky bit.<br>Indicates a change of in14_los_live bit.<br>0 = no change<br>1 = live status changed |
| IN14_TRANS_DETECT_LIVE[3] | R/O | 0 | Transient detector live bit.<br>Indicates that a transient is detected for input 14.<br>0 = inactive<br>1 = active |
| IN14_FREQ_OFFS_LIM_LIVE[2] | R/O | 0 | Frequency offset limit live status.<br>Indicates that the current frequency offset exceeds the limit for input 14.<br>0 = inactive<br>1 = active |

| STATUS.IN14_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN14_NO_ACTIVITY_LIVE [1] | R/O | 0 | No activity live status.<br>Indicates no activity on input 14.<br>0 = inactive<br>1 = active |
| IN14_LOS_LIVE[0] | R/O | 0 | LOS live status.<br>Indicates loss of signal on input 14.<br>0 = inactive<br>1 = active |

### STATUS.IN15_MON_STATUS

Input 15 reference monitor status.

Table 46: STATUS.IN15_MON_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN15_MON_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 017h | IN15_TRANS_DETECT_STICKY[7] | IN15_FREQ_OFFS_LIM_STICKY[6] | IN15_NO_ACTIVITY_STICKY[5] | IN15_LOS_STICKY[4] | IN15_TRANS_DETECT_LIVE[3] | IN15_FREQ_OFFS_LIM_LIVE[2] | IN15_NO_ACTIVITY_LIVE[1] | IN15_LOS_LIVE[0] |

| STATUS.IN15_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN15_TRANS_DETECT_STICKY[7] | R/O | 0 | Transient detector sticky bit.<br>Indicates a change of in15_trans_detect_live bit.<br>0 = no change<br>1 = live status changed |
| IN15_FREQ_OFFS_LIM_STICKY[6] | R/O | 0 | Frequency offset limit sticky bit.<br>Indicates a change of in15_freq_offs_lim_live bit.<br>0 = no change<br>1 = live status changed |
| IN15_NO_ACTIVITY_STICKY[5] | R/O | 0 | No activity sticky bit.<br>Indicates a change of in15_no_activity_live bit.<br>0 = no change<br>1 = live status changed |
| IN15_LOS_STICKY[4] | R/O | 0 | LOS sticky bit.<br>Indicates a change of in15_los_live bit.<br>0 = no change<br>1 = live status changed |
| IN15_TRANS_DETECT_LIVE[3] | R/O | 0 | Transient detector live bit.<br>Indicates that a transient is detected for input 15.<br>0 = inactive<br>1 = active |

| STATUS.IN15_MON_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN15_FREQ_OFFS_LIM_LIVE[2] | R/O | 0 | Frequency offset limit live status.<br>Indicates that the current frequency offset exceeds the limit for input 15.<br>0 = inactive<br>1 = active |
| IN15_NO_ACTIVITY_LIVE[1] | R/O | 0 | No activity live status.<br>Indicates no activity on input 15.<br>0 = inactive<br>1 = active |
| IN15_LOS_LIVE[0] | R/O | 0 | LOS live status.<br>Indicates loss of signal on input 15.<br>0 = inactive<br>1 = active |

### STATUS.DPLL0_STATUS

DPLL 0 status.

Table 47: STATUS.DPLL0_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL0_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 018h | RESERVED[7:6] | | DPLL0_HOLDOVER_STATE_CHANGE_STICKY[5] | DPLL0_LOCK_STATE_CHANGE_STICKY[4] | DPLL0_STATE[3:0] | | | |

| STATUS.DPLL0_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL0_HOLDOVER_STATE_CHANGE_STICKY[5] | R/O | 0 | Holdover state change sticky bit.<br>Indicates whether any transition to or from Holdover state occurred.<br>0 = no transition to or from Holdover state<br>1 = transition to or from Holdover state |

| STATUS.DPLL0_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL0_LOCK_STATE_CHANGE_STICKY[4] | R/O | 0 | Lock state change sticky bit.<br>Indicates whether any transition to or from Locked state occurred.<br>0 = no transition to or from Locked state<br>1 = transition to or from Locked state |
| DPLL0_STATE[3:0] | R/O | 0 | Current state of DPLL0.<br>0 = freerun<br>1 = lockacq<br>2 = lockrec<br>3 = locked<br>4 = holdover<br>5 = open loop<br>6 = disabled |

### STATUS.DPLL1_STATUS

DPLL 1 status.

Table 48: STATUS.DPLL1_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL1_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 019h | RESERVED[7:6] | | DPLL1_HOLDOVER_STATE_CHANGE_STICKY[5] | DPLL1_LOCK_STATE_CHANGE_STICKY[4] | DPLL1_STATE[3:0] | | | |

| STATUS.DPLL1_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL1_HOLDOVER_STATE_CHANGE_STICKY[5] | R/O | 0 | Holdover state change sticky bit.<br>Indicates whether any transition to or from Holdover state occurred.<br>0 = no transition to or from Holdover state<br>1 = transition to or from Holdover state |

| STATUS.DPLL1_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL1_LOCK_STATE_CHANGE_STICKY[4] | R/O | 0 | Lock state change sticky bit.<br>Indicates whether any transition to or from Locked state occurred.<br>0 = no transition to or from Locked state<br>1 = transition to or from Locked state |
| DPLL1_STATE[3:0] | R/O | 0 | Current state of DPLL1.<br>0 = freerun<br>1 = lockacq<br>2 = lockrec<br>3 = locked<br>4 = holdover<br>5 = open loop<br>6 = disabled |

### STATUS.DPLL2_STATUS

DPLL 2 status.

Table 49: STATUS.DPLL2_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL2_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Ah | RESERVED[7:6] | | DPLL2_HOLDOVER_STATE_CHANGE_STICKY[5] | DPLL2_LOCK_STATE_CHANGE_STICKY[4] | DPLL2_STATE[3:0] | | | |

| STATUS.DPLL2_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL2_HOLDOVER_STATE_CHANGE_STICKY[5] | R/O | 0 | Holdover state change sticky bit.<br>Indicates whether any transition to or from Holdover state occurred.<br>0 = no transition to or from Holdover state<br>1 = transition to or from Holdover state |

| STATUS.DPLL2_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL2_LOCK_STATE_CHANGE_STICKY[4] | R/O | 0 | Lock state change sticky bit.<br>Indicates whether any transition to or from Locked state occurred.<br>0 = no transition to or from Locked state<br>1 = transition to or from Locked state |
| DPLL2_STATE[3:0] | R/O | 0 | Current state of DPLL2.<br>0 = freerun<br>1 = lockacq<br>2 = lockrec<br>3 = locked<br>4 = holdover<br>5 = open loop<br>6 = disabled |

### STATUS.DPLL3_STATUS

DPLL 3 status.

Table 50: STATUS.DPLL3_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL3_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Bh | RESERVED[7:6] | | DPLL3_HOLDOVER_STATE_CHANGE_STICKY[5] | DPLL3_LOCK_STATE_CHANGE_STICKY[4] | DPLL3_STATE[3:0] | | | |

| STATUS.DPLL3_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL3_HOLDOVER_STATE_CHANGE_STICKY[5] | R/O | 0 | Holdover state change sticky bit.<br>Indicates whether any transition to or from Holdover state occurred.<br>0 = no transition to or from Holdover state<br>1 = transition to or from Holdover state |

| STATUS.DPLL3_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL3_LOCK_STATE_CHANGE_STICKY[4] | R/O | 0 | Lock state change sticky bit.<br>Indicates whether any transition to or from Locked state occurred.<br>0 = no transition to or from Locked state<br>1 = transition to or from Locked state |
| DPLL3_STATE[3:0] | R/O | 0 | Current state of DPLL3.<br>0 = freerun<br>1 = lockacq<br>2 = lockrec<br>3 = locked<br>4 = holdover<br>5 = open loop<br>6 = disabled |

### STATUS.DPLL4_STATUS

DPLL 4 status.

Table 51: STATUS.DPLL4_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL4_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Ch | RESERVED[7:6] | | DPLL4_HOLDOVER_STATE_CHANGE_STICKY[5] | DPLL4_LOCK_STATE_CHANGE_STICKY[4] | DPLL4_STATE[3:0] | | | |

| STATUS.DPLL4_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL4_HOLDOVER_STATE_CHANGE_STICKY[5] | R/O | 0 | Holdover state change sticky bit.<br>Indicates whether any transition to or from Holdover state occurred.<br>0 = no transition to or from Holdover state<br>1 = transition to or from Holdover state |

| STATUS.DPLL4_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL4_LOCK_STATE_CHANGE_STICKY[4] | R/O | 0 | Lock state change sticky bit.<br>Indicates whether any transition to or from Locked state occurred.<br>0 = no transition to or from Locked state<br>1 = transition to or from Locked state |
| DPLL4_STATE[3:0] | R/O | 0 | Current state of DPLL4.<br>0 = freerun<br>1 = lockacq<br>2 = lockrec<br>3 = locked<br>4 = holdover<br>5 = open loop<br>6 = disabled |

### STATUS.DPLL5_STATUS

DPLL 5 status.

Table 52: STATUS.DPLL5_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL5_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Dh | RESERVED[7:6] | | DPLL5_HOLDOVER_STATE_CHANGE_STICKY[5] | DPLL5_LOCK_STATE_CHANGE_STICKY[4] | DPLL5_STATE[3:0] | | | |

| STATUS.DPLL5_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL5_HOLDOVER_STATE_CHANGE_STICKY[5] | R/O | 0 | Holdover state change sticky bit.<br>Indicates whether any transition to or from Holdover state occurred.<br>0 = no transition to or from Holdover state<br>1 = transition to or from Holdover state |

| STATUS.DPLL5_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL5_LOCK_STATE_CHANGE_STICKY[4] | R/O | 0 | Lock state change sticky bit.<br>Indicates whether any transition to or from Locked state occurred.<br>0 = no transition to or from Locked state<br>1 = transition to or from Locked state |
| DPLL5_STATE[3:0] | R/O | 0 | Current state of DPLL5.<br>0 = freerun<br>1 = lockacq<br>2 = lockrec<br>3 = locked<br>4 = holdover<br>5 = open loop<br>6 = disabled |

### STATUS.DPLL6_STATUS

DPLL 6 status.

Table 53: STATUS.DPLL6_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL6_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Eh | RESERVED[7:6] | | DPLL6_HOLDOVER_STATE_CHANGE_STICKY[5] | DPLL6_LOCK_STATE_CHANGE_STICKY[4] | DPLL6_STATE[3:0] | | | |

| STATUS.DPLL6_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL6_HOLDOVER_STATE_CHANGE_STICKY[5] | R/O | 0 | Holdover state change sticky bit.<br>Indicates whether any transition to or from Holdover state occurred.<br>0 = no transition to or from Holdover state<br>1 = transition to or from Holdover state |

| STATUS.DPLL6_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL6_LOCK_STATE_CHANGE_STICKY[4] | R/O | 0 | Lock state change sticky bit.<br>Indicates whether any transition to or from Locked state occurred.<br>0 = no transition to or from Locked state<br>1 = transition to or from Locked state |
| DPLL6_STATE[3:0] | R/O | 0 | Current state of DPLL6.<br>0 = freerun<br>1 = lockacq<br>2 = lockrec<br>3 = locked<br>4 = holdover<br>5 = open loop<br>6 = disabled |

### STATUS.DPLL7_STATUS

DPLL 7 status.

Table 54: STATUS.DPLL7_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL7_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Fh | RESERVED[7:6] | | DPLL7_HOLDOVER_STATE_CHANGE_STICKY[5] | DPLL7_LOCK_STATE_CHANGE_STICKY[4] | DPLL7_STATE[3:0] | | | |

| STATUS.DPLL7_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL7_HOLDOVER_STATE_CHANGE_STICKY[5] | R/O | 0 | Holdover state change sticky bit.<br>Indicates whether any transition to or from Holdover state occurred.<br>0 = no transition to or from Holdover state<br>1 = transition to or from Holdover state |

| STATUS.DPLL7_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL7_LOCK_STATE_CHANGE_STICKY[4] | R/O | 0 | Lock state change sticky bit.<br>Indicates whether any transition to or from Locked state occurred.<br>0 = no transition to or from Locked state<br>1 = transition to or from Locked state |
| DPLL7_STATE[3:0] | R/O | 0 | Current state of DPLL7.<br>0 = freerun<br>1 = lockacq<br>2 = lockrec<br>3 = locked<br>4 = holdover<br>5 = open loop<br>6 = disabled |

### STATUS.DPLL_SYS_STATUS

System DPLL status.

Table 55: STATUS.DPLL_SYS_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL_SYS_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 020h | RESERVED[7:6] | | DPLL_SYS_HOLDOVER_STATE_CHANGE_STICKY[5] | DPLL_SYS_LOCK_STATE_CHANGE_STICKY[4] | DPLL_SYS_STATE[3:0] | | | |

| STATUS.DPLL_SYS_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL_SYS_HOLDOVER_STATE_CHANGE_STICKY[5] | R/O | 0 | Holdover state change sticky bit.<br>Indicates whether any transition to or from Holdover state occurred.<br>0 = no transition to or from Holdover state<br>1 = transition to or from Holdover state |

| STATUS.DPLL_SYS_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL_SYS_LOCK_STATE_CHANGE_STICKY[4] | R/O | 0 | Lock state change sticky bit.<br>Indicates whether any transition to or from Locked state occurred.<br>0 = no transition to or from Locked state<br>1 = transition to or from Locked state |
| DPLL_SYS_STATE[3:0] | R/O | 0 | Current state of SYS_DPLL.<br>0 = freerun<br>1 = lockacq<br>2 = lockrec<br>3 = locked<br>4 = holdover<br>5 = open loop |

### STATUS.SYS_APLL_STATUS

System APLL status.

Table 56: STATUS.SYS_APLL_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.SYS_APLL_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 021h | RESERVED[7:5] | | | SYS_APLL_LOSS_LOCK_STICKY[4] | RESERVED[3:1] | | | SYS_APLL_LOSS_LOCK_LIVE[0] |

| STATUS.SYS_APLL_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SYS_APLL_LOSS_LOCK_STICKY[4] | R/O | 0 | System APLL loss lock sticky bit.<br>Indicates that loss of lock was detected for system APLL.<br>0 = no change<br>1 = live status changed |
| RESERVED | N/A | - | This field must not be modified from the read value |
| SYS_APLL_LOSS_LOCK_LIVE[0] | R/O | 0 | System APLL loss lock live status.<br>Indicates that loss of lock is currently detected for system APLL.<br>0 = locked<br>1 = unlocked |

### STATUS.DPLL0_REF_STAT

Indicates which reference is currently selected for tracking.

Table 57: STATUS.DPLL0_REF_STAT Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL0_REF_STAT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 022h | RESERVED[7:5] | | | DPLL0_INPUT[4:0] | | | | |

| STATUS.DPLL0_REF_STAT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL0_INPUT[4:0] | R/O | 0 | Current reference input for DPLL 0.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL<br>0x13 = fb clk of DPLL0 (CLK19)<br>0x14 = fb clk of DPLL1 (CLK20)<br>0x15 = fb clk of DPLL2 (CLK21)<br>0x16 = fb clk of DPLL3 (CLK22)<br>0x17 = fb clk of DPLL4 (CLK23)<br>0x18 = fb clk of DPLL5 (CLK24)<br>0x19 = fb clk of DPLL6 (CLK25)<br>0x1A = fb clk of DPLL7 (CLK26)<br>0x1B = fb clk of SYS DPLL (CLK27)<br>0x1F = no reference |

### STATUS.DPLL1_REF_STAT

Indicates which reference is currently selected for tracking.

Table 58: STATUS.DPLL1_REF_STAT Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL1_REF_STAT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 023h | RESERVED[7:5] | | | DPLL1_INPUT[4:0] | | | | |

| STATUS.DPLL1_REF_STAT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL1_INPUT[4:0] | R/O | 0 | Current reference input for DPLL 1.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL<br>0x13 = fb clk of DPLL0 (CLK19)<br>0x14 = fb clk of DPLL1 (CLK20)<br>0x15 = fb clk of DPLL2 (CLK21)<br>0x16 = fb clk of DPLL3 (CLK22)<br>0x17 = fb clk of DPLL4 (CLK23)<br>0x18 = fb clk of DPLL5 (CLK24)<br>0x19 = fb clk of DPLL6 (CLK25)<br>0x1A = fb clk of DPLL7 (CLK26)<br>0x1B = fb clk of SYS DPLL (CLK27)<br>0x1F = no reference |

### STATUS.DPLL2_REF_STAT

Indicates which reference is currently selected for tracking.

Table 59: STATUS.DPLL2_REF_STAT Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL2_REF_STAT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 024h | RESERVED[7:5] | | | DPLL2_INPUT[4:0] | | | | |

| STATUS.DPLL2_REF_STAT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL2_INPUT[4:0] | R/O | 0 | Current reference input for DPLL 2.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL<br>0x13 = fb clk of DPLL0 (CLK19)<br>0x14 = fb clk of DPLL1 (CLK20)<br>0x15 = fb clk of DPLL2 (CLK21)<br>0x16 = fb clk of DPLL3 (CLK22)<br>0x17 = fb clk of DPLL4 (CLK23)<br>0x18 = fb clk of DPLL5 (CLK24)<br>0x19 = fb clk of DPLL6 (CLK25)<br>0x1A = fb clk of DPLL7 (CLK26)<br>0x1B = fb clk of SYS DPLL (CLK27)<br>0x1F = no reference |

### STATUS.DPLL3_REF_STAT

Indicates which reference is currently selected for tracking.

Table 60: STATUS.DPLL3_REF_STAT Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL3_REF_STAT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 025h | RESERVED[7:5] | | | DPLL3_INPUT[4:0] | | | | |

| STATUS.DPLL3_REF_STAT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL3_INPUT[4:0] | R/O | 0 | Current reference input for DPLL 3.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL<br>0x13 = fb clk of DPLL0 (CLK19)<br>0x14 = fb clk of DPLL1 (CLK20)<br>0x15 = fb clk of DPLL2 (CLK21)<br>0x16 = fb clk of DPLL3 (CLK22)<br>0x17 = fb clk of DPLL4 (CLK23)<br>0x18 = fb clk of DPLL5 (CLK24)<br>0x19 = fb clk of DPLL6 (CLK25)<br>0x1A = fb clk of DPLL7 (CLK26)<br>0x1B = fb clk of SYS DPLL (CLK27)<br>0x1F = no reference |

### STATUS.DPLL4_REF_STAT

Indicates which reference is currently selected for tracking.

Table 61: STATUS.DPLL4_REF_STAT Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL4_REF_STAT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 026h | RESERVED[7:5] | | | DPLL4_INPUT[4:0] | | | | |

| STATUS.DPLL4_REF_STAT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL4_INPUT[4:0] | R/O | 0 | Current reference input for DPLL 4.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL<br>0x13 = fb clk of DPLL0 (CLK19)<br>0x14 = fb clk of DPLL1 (CLK20)<br>0x15 = fb clk of DPLL2 (CLK21)<br>0x16 = fb clk of DPLL3 (CLK22)<br>0x17 = fb clk of DPLL4 (CLK23)<br>0x18 = fb clk of DPLL5 (CLK24)<br>0x19 = fb clk of DPLL6 (CLK25)<br>0x1A = fb clk of DPLL7 (CLK26)<br>0x1B = fb clk of SYS DPLL (CLK27)<br>0x1F = no reference |

### STATUS.DPLL5_REF_STAT

Indicates which reference is currently selected for tracking.

Table 62: STATUS.DPLL5_REF_STAT Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL5_REF_STAT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 027h | RESERVED[7:5] | | | DPLL5_INPUT[4:0] | | | | |

| STATUS.DPLL5_REF_STAT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL5_INPUT[4:0] | R/O | 0 | Current reference input for DPLL 5.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL<br>0x13 = fb clk of DPLL0 (CLK19)<br>0x14 = fb clk of DPLL1 (CLK20)<br>0x15 = fb clk of DPLL2 (CLK21)<br>0x16 = fb clk of DPLL3 (CLK22)<br>0x17 = fb clk of DPLL4 (CLK23)<br>0x18 = fb clk of DPLL5 (CLK24)<br>0x19 = fb clk of DPLL6 (CLK25)<br>0x1A = fb clk of DPLL7 (CLK26)<br>0x1B = fb clk of SYS DPLL (CLK27)<br>0x1F = no reference |

### STATUS.DPLL6_REF_STAT

Indicates which reference is currently selected for tracking.

Table 63: STATUS.DPLL6_REF_STAT Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL6_REF_STAT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 028h | RESERVED[7:5] | | | DPLL6_INPUT[4:0] | | | | |

| STATUS.DPLL6_REF_STAT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL6_INPUT[4:0] | R/O | 0 | Current reference input for DPLL 6.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL<br>0x13 = fb clk of DPLL0 (CLK19)<br>0x14 = fb clk of DPLL1 (CLK20)<br>0x15 = fb clk of DPLL2 (CLK21)<br>0x16 = fb clk of DPLL3 (CLK22)<br>0x17 = fb clk of DPLL4 (CLK23)<br>0x18 = fb clk of DPLL5 (CLK24)<br>0x19 = fb clk of DPLL6 (CLK25)<br>0x1A = fb clk of DPLL7 (CLK26)<br>0x1B = fb clk of SYS DPLL (CLK27)<br>0x1F = no reference |

### STATUS.DPLL7_REF_STAT

Indicates which reference is currently selected for tracking.

Table 64: STATUS.DPLL7_REF_STAT Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL7_REF_STAT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 029h | RESERVED[7:5] | | | DPLL7_INPUT[4:0] | | | | |

| STATUS.DPLL7_REF_STAT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL7_INPUT[4:0] | R/O | 0 | Current reference input for DPLL 7.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL<br>0x13 = fb clk of DPLL0 (CLK19)<br>0x14 = fb clk of DPLL1 (CLK20)<br>0x15 = fb clk of DPLL2 (CLK21)<br>0x16 = fb clk of DPLL3 (CLK22)<br>0x17 = fb clk of DPLL4 (CLK23)<br>0x18 = fb clk of DPLL5 (CLK24)<br>0x19 = fb clk of DPLL6 (CLK25)<br>0x1A = fb clk of DPLL7 (CLK26)<br>0x1B = fb clk of SYS DPLL (CLK27)<br>0x1F = no reference |

### STATUS.DPLL_SYS_REF_STAT

Indicates which reference is currently selected for tracking.

Table 65: STATUS.DPLL_SYS_REF_STAT Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL_SYS_REF_STAT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 02Ah | RESERVED[7:5] | | | DPLL_SYS_INPUT[4:0] | | | | |

| STATUS.DPLL_SYS_REF_STAT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL_SYS_INPUT[4:0] | R/O | 0 | Current reference input for system DPLL.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL<br>0x13 = fb clk of DPLL0 (CLK19)<br>0x14 = fb clk of DPLL1 (CLK20)<br>0x15 = fb clk of DPLL2 (CLK21)<br>0x16 = fb clk of DPLL3 (CLK22)<br>0x17 = fb clk of DPLL4 (CLK23)<br>0x18 = fb clk of DPLL5 (CLK24)<br>0x19 = fb clk of DPLL6 (CLK25)<br>0x1A = fb clk of DPLL7 (CLK26)<br>0x1B = fb clk of SYS DPLL (CLK27)<br>0x1F = no reference |

### STATUS.DPLL0_FILTER_STATUS

DPLL 0 loop filter status.

Table 66: STATUS.DPLL0_FILTER_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL0_FILTER_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 044h | FILTER_STATUS[7:0] | | | | | | | |
| 045h | FILTER_STATUS[15:8] | | | | | | | |
| 046h | FILTER_STATUS[23:16] | | | | | | | |
| 047h | FILTER_STATUS[31:24] | | | | | | | |
| 048h | FILTER_STATUS[39:32] | | | | | | | |
| 049h | FILTER_STATUS[47:40] | | | | | | | |

| STATUS.DPLL0_FILTER_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FILTER_STATUS[47:0] | R/O | 0 | DPLL loop filter status.<br>If FILTER_STATUS_UPDATE_EN = "1", then FILTER_STATUS is a signed 48-bit FFO value in units of 2^(-53).<br>If the DPLL is in phase measurement mode and the input TDC is configured for fine phase measurement, then the FILTER_STATUS is a signed 48-bit phase value in units of 50/128 picoseconds. |

### STATUS.DPLL1_FILTER_STATUS

DPLL 1 loop filter status.

Table 67: STATUS.DPLL1_FILTER_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL1_FILTER_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 04Ch | FILTER_STATUS[7:0] | | | | | | | |
| 04Dh | FILTER_STATUS[15:8] | | | | | | | |
| 04Eh | FILTER_STATUS[23:16] | | | | | | | |
| 04Fh | FILTER_STATUS[31:24] | | | | | | | |
| 050h | FILTER_STATUS[39:32] | | | | | | | |
| 051h | FILTER_STATUS[47:40] | | | | | | | |

| STATUS.DPLL1_FILTER_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FILTER_STATUS[47:0] | R/O | 0 | DPLL loop filter status.<br>If FILTER_STATUS_UPDATE_EN = "1", then FILTER_STATUS is a signed 48-bit FFO value in units of 2^(-53).<br>If the DPLL is in phase measurement mode and the input TDC is configured for fine phase measurement, then the FILTER_STATUS is a signed 48-bit phase value in units of 50/128 picoseconds. |

### STATUS.DPLL2_FILTER_STATUS

DPLL 2 loop filter status.

Table 68: STATUS.DPLL2_FILTER_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL2_FILTER_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 054h | FILTER_STATUS[7:0] | | | | | | | |
| 055h | FILTER_STATUS[15:8] | | | | | | | |
| 056h | FILTER_STATUS[23:16] | | | | | | | |
| 057h | FILTER_STATUS[31:24] | | | | | | | |
| 058h | FILTER_STATUS[39:32] | | | | | | | |
| 059h | FILTER_STATUS[47:40] | | | | | | | |

| STATUS.DPLL2_FILTER_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FILTER_STATUS[47:0] | R/O | 0 | DPLL loop filter status.<br>If FILTER_STATUS_UPDATE_EN = "1", then FILTER_STATUS is a signed 48-bit FFO value in units of 2^(-53).<br>If the DPLL is in phase measurement mode and the input TDC is configured for fine phase measurement, then the FILTER_STATUS is a signed 48-bit phase value in units of 50/128 picoseconds. |

### STATUS.DPLL3_FILTER_STATUS

DPLL 3 loop filter status.

Table 69: STATUS.DPLL3_FILTER_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL3_FILTER_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 05Ch | FILTER_STATUS[7:0] | | | | | | | |
| 05Dh | FILTER_STATUS[15:8] | | | | | | | |
| 05Eh | FILTER_STATUS[23:16] | | | | | | | |
| 05Fh | FILTER_STATUS[31:24] | | | | | | | |
| 060h | FILTER_STATUS[39:32] | | | | | | | |
| 061h | FILTER_STATUS[47:40] | | | | | | | |

| STATUS.DPLL3_FILTER_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FILTER_STATUS[47:0] | R/O | 0 | DPLL loop filter status.<br>If FILTER_STATUS_UPDATE_EN = "1", then FILTER_STATUS is a signed 48-bit FFO value in units of 2^(-53).<br>If the DPLL is in phase measurement mode and the input TDC is configured for fine phase measurement, then the FILTER_STATUS is a signed 48-bit phase value in units of 50/128 picoseconds. |

### STATUS.DPLL4_FILTER_STATUS

DPLL 4 loop filter status.

Table 70: STATUS.DPLL4_FILTER_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL4_FILTER_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 064h | FILTER_STATUS[7:0] | | | | | | | |
| 065h | FILTER_STATUS[15:8] | | | | | | | |
| 066h | FILTER_STATUS[23:16] | | | | | | | |
| 067h | FILTER_STATUS[31:24] | | | | | | | |
| 068h | FILTER_STATUS[39:32] | | | | | | | |
| 069h | FILTER_STATUS[47:40] | | | | | | | |

| STATUS.DPLL4_FILTER_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FILTER_STATUS[47:0] | R/O | 0 | DPLL loop filter status.<br>If FILTER_STATUS_UPDATE_EN = "1", then FILTER_STATUS is a signed 48-bit FFO value in units of 2^(-53).<br>If the DPLL is in phase measurement mode and the input TDC is configured for fine phase measurement, then the FILTER_STATUS is a signed 48-bit phase value in units of 50/128 picoseconds. |

### STATUS.DPLL5_FILTER_STATUS

DPLL 5 loop filter status.

Table 71: STATUS.DPLL5_FILTER_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL5_FILTER_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 06Ch | FILTER_STATUS[7:0] | | | | | | | |
| 06Dh | FILTER_STATUS[15:8] | | | | | | | |
| 06Eh | FILTER_STATUS[23:16] | | | | | | | |
| 06Fh | FILTER_STATUS[31:24] | | | | | | | |
| 070h | FILTER_STATUS[39:32] | | | | | | | |
| 071h | FILTER_STATUS[47:40] | | | | | | | |

| STATUS.DPLL5_FILTER_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FILTER_STATUS[47:0] | R/O | 0 | DPLL loop filter status.<br>If FILTER_STATUS_UPDATE_EN = "1", then FILTER_STATUS is a signed 48-bit FFO value in units of 2^(-53).<br>If the DPLL is in phase measurement mode and the input TDC is configured for fine phase measurement, then the FILTER_STATUS is a signed 48-bit phase value in units of 50/128 picoseconds. |

### STATUS.DPLL6_FILTER_STATUS

DPLL 6 loop filter status.

Table 72: STATUS.DPLL6_FILTER_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL6_FILTER_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 074h | FILTER_STATUS[7:0] | | | | | | | |
| 075h | FILTER_STATUS[15:8] | | | | | | | |
| 076h | FILTER_STATUS[23:16] | | | | | | | |
| 077h | FILTER_STATUS[31:24] | | | | | | | |
| 078h | FILTER_STATUS[39:32] | | | | | | | |
| 079h | FILTER_STATUS[47:40] | | | | | | | |

| STATUS.DPLL6_FILTER_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FILTER_STATUS[47:0] | R/O | 0 | DPLL loop filter status.<br>If FILTER_STATUS_UPDATE_EN = "1", then FILTER_STATUS is a signed 48-bit FFO value in units of 2^(-53).<br>If the DPLL is in phase measurement mode and the input TDC is configured for fine phase measurement, then the FILTER_STATUS is a signed 48-bit phase value in units of 50/128 picoseconds. |

### STATUS.DPLL7_FILTER_STATUS

DPLL 7 loop filter status.

Table 73: STATUS.DPLL7_FILTER_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL7_FILTER_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 07Ch | FILTER_STATUS[7:0] | | | | | | | |
| 07Dh | FILTER_STATUS[15:8] | | | | | | | |
| 07Eh | FILTER_STATUS[23:16] | | | | | | | |
| 07Fh | FILTER_STATUS[31:24] | | | | | | | |
| 080h | FILTER_STATUS[39:32] | | | | | | | |
| 081h | FILTER_STATUS[47:40] | | | | | | | |

| STATUS.DPLL7_FILTER_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FILTER_STATUS[47:0] | R/O | 0 | DPLL loop filter status.<br>If FILTER_STATUS_UPDATE_EN = "1", then FILTER_STATUS is a signed 48-bit FFO value in units of 2^(-53).<br>If the DPLL is in phase measurement mode and the input TDC is configured for fine phase measurement, then the FILTER_STATUS is a signed 48-bit phase value in units of 50/128 picoseconds. |

### STATUS.DPLL_SYS_FILTER_STATUS

Loop filter status of system DPLL .

Table 74: STATUS.DPLL_SYS_FILTER_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL_SYS_FILTER_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 084h | FILTER_STATUS[7:0] | | | | | | | |
| 085h | FILTER_STATUS[15:8] | | | | | | | |
| 086h | FILTER_STATUS[23:16] | | | | | | | |
| 087h | FILTER_STATUS[31:24] | | | | | | | |
| 088h | FILTER_STATUS[39:32] | | | | | | | |
| 089h | FILTER_STATUS[47:40] | | | | | | | |

| STATUS.DPLL_SYS_FILTER_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FILTER_STATUS[47:0] | R/O | 0 | System DPLL loop filter status.<br>If FILTER_STATUS_UPDATE_EN = "1", then FILTER_STATUS is a signed 48-bit FFO value in units of 2^(-53). |

### STATUS.USER_GPIO0_TO_7_STATUS

GPIO 0 - 7 level status.

Table 75: STATUS.USER_GPIO0_TO_7_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.USER_GPIO0_TO_7_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 08Ah | GPIO7_LEVEL[7] | GPIO6_LEVEL[6] | GPIO5_LEVEL[5] | GPIO4_LEVEL[4] | GPIO3_LEVEL[3] | GPIO2_LEVEL[2] | GPIO1_LEVEL[1] | GPIO0_LEVEL[0] |

| STATUS.USER_GPIO0_TO_7_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| GPIO7_LEVEL[7] | R/O | 0 | Level of GPIO pin 7.<br>0 = low<br>1 = high |
| GPIO6_LEVEL[6] | R/O | 0 | Level of GPIO pin 6.<br>0 = low<br>1 = high |
| GPIO5_LEVEL[5] | R/O | 0 | Level of GPIO pin 5.<br>0 = low<br>1 = high |
| GPIO4_LEVEL[4] | R/O | 0 | Level of GPIO pin 4.<br>0 = low<br>1 = high |
| GPIO3_LEVEL[3] | R/O | 0 | Level of GPIO pin 3.<br>0 = low<br>1 = high |
| GPIO2_LEVEL[2] | R/O | 0 | Level of GPIO pin 2.<br>0 = low<br>1 = high |
| GPIO1_LEVEL[1] | R/O | 0 | Level of GPIO pin 1.<br>0 = low<br>1 = high |
| GPIO0_LEVEL[0] | R/O | 0 | Level of GPIO pin 0.<br>0 = low<br>1 = high |

### STATUS.USER_GPIO8_TO_15_STATUS

GPIO 8 - 15 level status.

Table 76: STATUS.USER_GPIO8_TO_15_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.USER_GPIO8_TO_15_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 08Bh | GPIO15_LEVEL[7] | GPIO14_LEVEL[6] | GPIO13_LEVEL[5] | GPIO12_LEVEL[4] | GPIO11_LEVEL[3] | GPIO10_LEVEL[2] | GPIO9_LEVEL[1] | GPIO8_LEVEL[0] |

| STATUS.USER_GPIO8_TO_15_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| GPIO15_LEVEL[7] | R/O | 0 | Level of GPIO pin 15.<br>0 = low<br>1 = high |
| GPIO14_LEVEL[6] | R/O | 0 | Level of GPIO pin 14.<br>0 = low<br>1 = high |
| GPIO13_LEVEL[5] | R/O | 0 | Level of GPIO pin 13.<br>0 = low<br>1 = high |
| GPIO12_LEVEL[4] | R/O | 0 | Level of GPIO pin 12.<br>0 = low<br>1 = high |
| GPIO11_LEVEL[3] | R/O | 0 | Level of GPIO pin 11.<br>0 = low<br>1 = high |
| GPIO10_LEVEL[2] | R/O | 0 | Level of GPIO pin 10.<br>0 = low<br>1 = high |
| GPIO9_LEVEL[1] | R/O | 0 | Level of GPIO pin 9.<br>0 = low<br>1 = high |
| GPIO8_LEVEL[0] | R/O | 0 | Level of GPIO pin 8.<br>0 = low<br>1 = high |

### STATUS.IN0_MON_FREQ_STATUS

Input 0 reference monitor frequency status and unit.

Table 77: STATUS.IN0_MON_FREQ_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN0_MON_FREQ_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 08Ch | FFO[7:0] | | | | | | | |
| 08Dh | FFO_UNIT[15:14] | | FFO[13:8] | | | | | |

| STATUS.IN0_MON_FREQ_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[15:14] | R/O | 0 | Input clock FFO unit enumeration.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO[13:0] | R/O | 0 | Signed 14-bit input clock fractional frequency offset. |

### STATUS.IN1_MON_FREQ_STATUS

Input 1 reference monitor frequency status and unit.

Table 78: STATUS.IN1_MON_FREQ_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN1_MON_FREQ_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 08Eh | FFO[7:0] | | | | | | | |
| 08Fh | FFO_UNIT[15:14] | | FFO[13:8] | | | | | |

| STATUS.IN1_MON_FREQ_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[15:14] | R/O | 0 | Input clock FFO unit enumeration.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO[13:0] | R/O | 0 | Signed 14-bit input clock fractional frequency offset. |

### STATUS.IN2_MON_FREQ_STATUS

Input 2 reference monitor frequency status and unit.

Table 79: STATUS.IN2_MON_FREQ_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN2_MON_FREQ_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 090h | FFO[7:0] | | | | | | | |
| 091h | FFO_UNIT[15:14] | | FFO[13:8] | | | | | |

| STATUS.IN2_MON_FREQ_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[15:14] | R/O | 0 | Input clock FFO unit enumeration.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO[13:0] | R/O | 0 | Signed 14-bit input clock fractional frequency offset. |

### STATUS.IN3_MON_FREQ_STATUS

Input 3 reference monitor frequency status and unit.

Table 80: STATUS.IN3_MON_FREQ_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN3_MON_FREQ_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 092h | FFO[7:0] | | | | | | | |
| 093h | FFO_UNIT[15:14] | | FFO[13:8] | | | | | |

| STATUS.IN3_MON_FREQ_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[15:14] | R/O | 0 | Input clock FFO unit enumeration.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO[13:0] | R/O | 0 | Signed 14-bit input clock fractional frequency offset. |

### STATUS.IN4_MON_FREQ_STATUS

Input 4 reference monitor frequency status and unit.

Table 81: STATUS.IN4_MON_FREQ_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN4_MON_FREQ_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 094h | FFO[7:0] | | | | | | | |
| 095h | FFO_UNIT[15:14] | | FFO[13:8] | | | | | |

| STATUS.IN4_MON_FREQ_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[15:14] | R/O | 0 | Input clock FFO unit enumeration.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO[13:0] | R/O | 0 | Signed 14-bit input clock fractional frequency offset. |

### STATUS.IN5_MON_FREQ_STATUS

Input 5 reference monitor frequency status and unit.

Table 82: STATUS.IN5_MON_FREQ_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN5_MON_FREQ_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 096h | FFO[7:0] | | | | | | | |
| 097h | FFO_UNIT[15:14] | | FFO[13:8] | | | | | |

| STATUS.IN5_MON_FREQ_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[15:14] | R/O | 0 | Input clock FFO unit enumeration.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO[13:0] | R/O | 0 | Signed 14-bit input clock fractional frequency offset. |

### STATUS.IN6_MON_FREQ_STATUS

Input 6 reference monitor frequency status and unit.

Table 83: STATUS.IN6_MON_FREQ_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN6_MON_FREQ_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 098h | FFO[7:0] | | | | | | | |
| 099h | FFO_UNIT[15:14] | | FFO[13:8] | | | | | |

| STATUS.IN6_MON_FREQ_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[15:14] | R/O | 0 | Input clock FFO unit enumeration.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO[13:0] | R/O | 0 | Signed 14-bit input clock fractional frequency offset. |

### STATUS.IN7_MON_FREQ_STATUS

Input 7 reference monitor frequency status and unit.

Table 84: STATUS.IN7_MON_FREQ_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN7_MON_FREQ_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 09Ah | FFO[7:0] | | | | | | | |
| 09Bh | FFO_UNIT[15:14] | | FFO[13:8] | | | | | |

| STATUS.IN7_MON_FREQ_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[15:14] | R/O | 0 | Input clock FFO unit enumeration.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO[13:0] | R/O | 0 | Signed 14-bit input clock fractional frequency offset. |

### STATUS.IN8_MON_FREQ_STATUS

Input 8 reference monitor frequency status and unit.

Table 85: STATUS.IN8_MON_FREQ_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN8_MON_FREQ_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 09Ch | FFO[7:0] | | | | | | | |
| 09Dh | FFO_UNIT[15:14] | | FFO[13:8] | | | | | |

| STATUS.IN8_MON_FREQ_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[15:14] | R/O | 0 | Input clock FFO unit enumeration.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO[13:0] | R/O | 0 | Signed 14-bit input clock fractional frequency offset. |

### STATUS.IN9_MON_FREQ_STATUS

Input 9 reference monitor frequency status and unit.

Table 86: STATUS.IN9_MON_FREQ_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN9_MON_FREQ_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 09Eh | FFO[7:0] | | | | | | | |
| 09Fh | FFO_UNIT[15:14] | | FFO[13:8] | | | | | |

| STATUS.IN9_MON_FREQ_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[15:14] | R/O | 0 | Input clock FFO unit enumeration.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO[13:0] | R/O | 0 | Signed 14-bit input clock fractional frequency offset. |

### STATUS.IN10_MON_FREQ_STATUS

Input 10 reference monitor frequency status and unit.

Table 87: STATUS.IN10_MON_FREQ_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN10_MON_FREQ_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0A0h | FFO[7:0] | | | | | | | |
| 0A1h | FFO_UNIT[15:14] | | FFO[13:8] | | | | | |

| STATUS.IN10_MON_FREQ_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[15:14] | R/O | 0 | Input clock FFO unit enumeration.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO[13:0] | R/O | 0 | Signed 14-bit input clock fractional frequency offset. |

### STATUS.IN11_MON_FREQ_STATUS

Input 11 reference monitor frequency status and unit.

Table 88: STATUS.IN11_MON_FREQ_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN11_MON_FREQ_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0A2h | FFO[7:0] | | | | | | | |
| 0A3h | FFO_UNIT[15:14] | | FFO[13:8] | | | | | |

| STATUS.IN11_MON_FREQ_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[15:14] | R/O | 0 | Input clock FFO unit enumeration.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO[13:0] | R/O | 0 | Signed 14-bit input clock fractional frequency offset. |

### STATUS.IN12_MON_FREQ_STATUS

Input 12 reference monitor frequency status and unit.

Table 89: STATUS.IN12_MON_FREQ_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN12_MON_FREQ_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0A4h | FFO[7:0] | | | | | | | |
| 0A5h | FFO_UNIT[15:14] | | FFO[13:8] | | | | | |

| STATUS.IN12_MON_FREQ_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[15:14] | R/O | 0 | Input clock FFO unit enumeration.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO[13:0] | R/O | 0 | Signed 14-bit input clock fractional frequency offset. |

### STATUS.IN13_MON_FREQ_STATUS

Input 13 reference monitor frequency status and unit.

Table 90: STATUS.IN13_MON_FREQ_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN13_MON_FREQ_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0A6h | FFO[7:0] | | | | | | | |
| 0A7h | FFO_UNIT[15:14] | | FFO[13:8] | | | | | |

| STATUS.IN13_MON_FREQ_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[15:14] | R/O | 0 | Input clock FFO unit enumeration.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO[13:0] | R/O | 0 | Signed 14-bit input clock fractional frequency offset. |

### STATUS.IN14_MON_FREQ_STATUS

Input 14 reference monitor frequency status and unit.

Table 91: STATUS.IN14_MON_FREQ_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN14_MON_FREQ_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0A8h | FFO[7:0] | | | | | | | |
| 0A9h | FFO_UNIT[15:14] | | FFO[13:8] | | | | | |

| STATUS.IN14_MON_FREQ_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[15:14] | R/O | 0 | Input clock FFO unit enumeration.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO[13:0] | R/O | 0 | Signed 14-bit input clock fractional frequency offset. |

### STATUS.IN15_MON_FREQ_STATUS

Input 15 reference monitor frequency status and unit.

Table 92: STATUS.IN15_MON_FREQ_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.IN15_MON_FREQ_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0AAh | FFO[7:0] | | | | | | | |
| 0ABh | FFO_UNIT[15:14] | | FFO[13:8] | | | | | |

| STATUS.IN15_MON_FREQ_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[15:14] | R/O | 0 | Input clock FFO unit enumeration.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO[13:0] | R/O | 0 | Signed 14-bit input clock fractional frequency offset. |

### STATUS.OUTPUT_TDC_CFG_STATUS

Indicates when the output TDC is ready for use.

Table 93: STATUS.OUTPUT_TDC_CFG_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.OUTPUT_TDC_CFG_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0ACh | RESERVED[7:2] | | | | | | STATE[1:0] | |

| STATUS.OUTPUT_TDC_CFG_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| STATE[1:0] | R/O | 0 | Indicates whether the output TDC is ready to be used.<br>Output TDC is by default disabled.<br>Need to enable with OUTPUT_TDC_CFG_GBL_2.enable. After enabling, it takes time for the output TDC clock to stabilize.<br>Output TDC is ready for use when in Ready state.<br>0 = disabled<br>1 = initializing<br>2 = ready |

### STATUS.OUTPUT_TDC0_STATUS

Indicates the hardware output TDC instance assigned and the status code.

Table 94: STATUS.OUTPUT_TDC0_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.OUTPUT_TDC0_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0ADh | VALID[7] | RESERVED[6:4] | | | STATUS[3:0] | | | |

| STATUS.OUTPUT_TDC0_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| VALID[7] | R/O | 0 | Indicates a valid measurement or alignment has met target phase offset.<br>When go bit is set, valid is cleared.<br>Measurement mode: Indicates when OUTPUT_TDCn_MEASUREMENT is valid.<br>Alignment mode: Indicates when all the alignment targets are within the OUTPUT_TDC_CTRL_1.TARGET_PHASE_OFFSET.<br>0 = invalid<br>1 = valid |

| STATUS.OUTPUT_TDC0_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| STATUS[3:0] | R/O | 0 | Status code.<br>When output TDC is not enabled, this shows 'Disabled'.<br>When OUTPUT_TDC_CTRL_4.GO is set and the configuration is valid, this transitions to 'In progress'. When the operation completes successfully, status transitions back to 'Idle' and OUTPUT_TDC_CTRL_4.GO will be cleared.<br>When OUTPUT_TDC_CTRL_4.GO is set and there is an invalid configuration, then OUTPUT_TDC_CTRL_4.GO will be cleared and this will indicate the error condition encountered.<br>0 = disabled<br>1 = idle<br>2 = in progress<br>3 = error - invalid source/target<br>4 = error - non-uniform master divider freq<br>5 = error - start failed<br>6 = error - measurement timeout |

### STATUS.OUTPUT_TDC1_STATUS

Indicates the hardware output TDC instance assigned and the status code.

Table 95: STATUS.OUTPUT_TDC1_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.OUTPUT_TDC1_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0AEh | VALID[7] | RESERVED[6:4] | | | STATUS[3:0] | | | |

| STATUS.OUTPUT_TDC1_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| VALID[7] | R/O | 0 | Indicates a valid measurement or alignment has met target phase offset. When go bit is set, valid is cleared.<br>Measurement mode: Indicates when OUTPUT_TDCn_MEASUREMENT is valid.<br>Alignment mode: Indicates when all the alignment targets are within the OUTPUT_TDC_CTRL_1.TARGET_PHASE_OFFSET.<br>0 = invalid<br>1 = valid |

| STATUS.OUTPUT_TDC1_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| STATUS[3:0] | R/O | 0 | Status code.<br>When output TDC is not enabled, this shows 'Disabled'.<br>When OUTPUT_TDC_CTRL_4.GO is set and the configuration is valid, this transitions to 'In progress'. When the operation completes successfully, status transitions back to 'Idle' and OUTPUT_TDC_CTRL_4.GO will be cleared.<br>When OUTPUT_TDC_CTRL_4.GO is set and there is an invalid configuration, then OUTPUT_TDC_CTRL_4.GO will be cleared and this will indicate the error condition encountered.<br>0 = disabled<br>1 = idle<br>2 = in progress<br>3 = error - invalid source/target<br>4 = error - non-uniform master divider freq<br>5 = error - start failed<br>6 = error - measurement timeout |

### STATUS.OUTPUT_TDC2_STATUS

Indicates the hardware output TDC instance assigned and the status code.

Table 96: STATUS.OUTPUT_TDC2_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.OUTPUT_TDC2_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0AFh | VALID[7] | RESERVED[6:4] | | | STATUS[3:0] | | | |

| STATUS.OUTPUT_TDC2_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| VALID[7] | R/O | 0 | Indicates a valid measurement or alignment has met target phase offset. When go bit is set, valid is cleared.<br>Measurement mode: Indicates when OUTPUT_TDCn_MEASUREMENT is valid.<br>Alignment mode: Indicates when all the alignment targets are within the OUTPUT_TDC_CTRL_1.TARGET_PHASE_OFFSET.<br>0 = invalid<br>1 = valid |

| STATUS.OUTPUT_TDC2_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| STATUS[3:0] | R/O | 0 | Status code.<br>When output TDC is not enabled, this shows 'Disabled'.<br>When OUTPUT_TDC_CTRL_4.GO is set and the configuration is valid, this transitions to 'In progress'. When the operation completes successfully, status transitions back to 'Idle' and OUTPUT_TDC_CTRL_4.GO will be cleared.<br>When OUTPUT_TDC_CTRL_4.GO is set and there is an invalid configuration, then OUTPUT_TDC_CTRL_4.GO will be cleared and this will indicate the error condition encountered.<br>0 = disabled<br>1 = idle<br>2 = in progress<br>3 = error - invalid source/target<br>4 = error - non-uniform master divider freq<br>5 = error - start failed<br>6 = error - measurement timeout |

### STATUS.OUTPUT_TDC3_STATUS

Indicates the hardware output TDC instance assigned and the status code.

Table 97: STATUS.OUTPUT_TDC3_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.OUTPUT_TDC3_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0B0h | VALID[7] | RESERVED[6:4] | | | STATUS[3:0] | | | |

| STATUS.OUTPUT_TDC3_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| VALID[7] | R/O | 0 | Indicates a valid measurement or alignment has met target phase offset. When go bit is set, valid is cleared.<br>Measurement mode: Indicates when OUTPUT_TDCn_MEASUREMENT is valid.<br>Alignment mode: Indicates when all the alignment targets are within the OUTPUT_TDC_CTRL_1.TARGET_PHASE_OFFSET.<br>0 = invalid<br>1 = valid |

| STATUS.OUTPUT_TDC3_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| STATUS[3:0] | R/O | 0 | Status code.<br>When output TDC is not enabled, this shows 'Disabled'.<br>When OUTPUT_TDC_CTRL_4.GO is set and the configuration is valid, this transitions to 'In progress'. When the operation completes successfully, status transitions back to 'Idle' and OUTPUT_TDC_CTRL_4.GO will be cleared.<br>When OUTPUT_TDC_CTRL_4.GO is set and there is an invalid configuration, then OUTPUT_TDC_CTRL_4.GO will be cleared and this will indicate the error condition encountered.<br>0 = disabled<br>1 = idle<br>2 = in progress<br>3 = error - invalid source/target<br>4 = error - non-uniform master divider freq<br>5 = error - start failed<br>6 = error - measurement timeout |

### STATUS.OUTPUT_TDC0_MEASUREMENT

Indicates output TDC 0 measurement.

Table 98: STATUS.OUTPUT_TDC0_MEASUREMENT Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.OUTPUT_TDC0_MEASUREMENT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0B4h | PHASE[7:0] | | | | | | | |
| 0B5h | PHASE[15:8] | | | | | | | |
| 0B6h | PHASE[23:16] | | | | | | | |
| 0B7h | PHASE[31:24] | | | | | | | |
| 0B8h | PHASE[39:32] | | | | | | | |
| 0B9h | PHASE[47:40] | | | | | | | |

| STATUS.OUTPUT_TDC0_MEASUREMENT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PHASE[47:0] | R/O | 0 | Output TDC measurement.<br>Signed 48-bit integer in picoseconds.<br>Measurement = sum of samples / number of samples<br>A sample is collected every 100us.<br>Positive value indicates the target edge leads the source edge.<br>i.e.. source edge is to the left of the target edge |

### STATUS.OUTPUT_TDC1_MEASUREMENT

Indicates output TDC 1 measurement.

Table 99: STATUS.OUTPUT_TDC1_MEASUREMENT Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.OUTPUT_TDC1_MEASUREMENT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0C4h | PHASE[7:0] | | | | | | | |
| 0C5h | PHASE[15:8] | | | | | | | |
| 0C6h | PHASE[23:16] | | | | | | | |
| 0C7h | PHASE[31:24] | | | | | | | |
| 0C8h | PHASE[39:32] | | | | | | | |
| 0C9h | PHASE[47:40] | | | | | | | |

| STATUS.OUTPUT_TDC1_MEASUREMENT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PHASE[47:0] | R/O | 0 | Output TDC measurement.<br>Signed 48-bit integer in picoseconds.<br>Measurement = sum of samples / number of samples<br>A sample is collected every 100us.<br>Positive value indicates the target edge leads the source edge.<br>i.e.. source edge is to the left of the target edge |

### STATUS.OUTPUT_TDC2_MEASUREMENT

Indicates output TDC 2 measurement.

Table 100: STATUS.OUTPUT_TDC2_MEASUREMENT Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.OUTPUT_TDC2_MEASUREMENT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0CCh | PHASE[7:0] | | | | | | | |
| 0CDh | PHASE[15:8] | | | | | | | |
| 0CEh | PHASE[23:16] | | | | | | | |
| 0CFh | PHASE[31:24] | | | | | | | |
| 0D0h | PHASE[39:32] | | | | | | | |
| 0D1h | PHASE[47:40] | | | | | | | |

| STATUS.OUTPUT_TDC2_MEASUREMENT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PHASE[47:0] | R/O | 0 | Output TDC measurement.<br>Signed 48-bit integer in picoseconds.<br>Measurement = sum of samples / number of samples<br>A sample is collected every 100us.<br>Positive value indicates the target edge leads the source edge.<br>i.e.. source edge is to the left of the target edge |

### STATUS.OUTPUT_TDC3_MEASUREMENT

Indicates output TDC 3 measurement.

Table 101: STATUS.OUTPUT_TDC3_MEASUREMENT Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.OUTPUT_TDC3_MEASUREMENT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0D4h | PHASE[7:0] | | | | | | | |
| 0D5h | PHASE[15:8] | | | | | | | |
| 0D6h | PHASE[23:16] | | | | | | | |
| 0D7h | PHASE[31:24] | | | | | | | |
| 0D8h | PHASE[39:32] | | | | | | | |
| 0D9h | PHASE[47:40] | | | | | | | |

| STATUS.OUTPUT_TDC3_MEASUREMENT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PHASE[47:0] | R/O | 0 | Output TDC measurement.<br>Signed 48-bit integer in picoseconds.<br>Measurement = sum of samples / number of samples<br>A sample is collected every 100us.<br>Positive value indicates the target edge leads the source edge.<br>i.e.. source edge is to the left of the target edge |

### STATUS.DPLL0_PHASE_STATUS

Phase offset at output of decimator.

Table 102: STATUS.DPLL0_PHASE_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL0_PHASE_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0DCh | DPLL0_PHASE_STATUS[7:0] | | | | | | | |
| 0DDh | DPLL0_PHASE_STATUS[15:8] | | | | | | | |
| 0DEh | DPLL0_PHASE_STATUS[23:16] | | | | | | | |
| 0DFh | DPLL0_PHASE_STATUS[31:24] | | | | | | | |
| 0E0h | RESERVED[39:36] | | | | DPLL0_PHASE_STATUS[35:32] | | | |

| STATUS.DPLL0_PHASE_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL0_PHASE_STATUS[35:0] | R/O | 0 | Signed 36-bit phase offset in ITDC_UIs. |

### STATUS.DPLL1_PHASE_STATUS

Phase offset at output of decimator.

Table 103: STATUS.DPLL1_PHASE_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL1_PHASE_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0E4h | DPLL1_PHASE_STATUS[7:0] | | | | | | | |
| 0E5h | DPLL1_PHASE_STATUS[15:8] | | | | | | | |
| 0E6h | DPLL1_PHASE_STATUS[23:16] | | | | | | | |
| 0E7h | DPLL1_PHASE_STATUS[31:24] | | | | | | | |
| 0E8h | RESERVED[39:36] | | | | DPLL1_PHASE_STATUS[35:32] | | | |

| STATUS.DPLL1_PHASE_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL1_PHASE_STATUS[35:0] | R/O | 0 | Signed 36-bit phase offset in ITDC_UIs. |

### STATUS.DPLL2_PHASE_STATUS

Phase offset at output of decimator.

Table 104: STATUS.DPLL2_PHASE_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL2_PHASE_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0ECh | DPLL2_PHASE_STATUS[7:0] | | | | | | | |
| 0EDh | DPLL2_PHASE_STATUS[15:8] | | | | | | | |
| 0EEh | DPLL2_PHASE_STATUS[23:16] | | | | | | | |
| 0EFh | DPLL2_PHASE_STATUS[31:24] | | | | | | | |
| 0F0h | RESERVED[39:36] | | | | DPLL2_PHASE_STATUS[35:32] | | | |

| STATUS.DPLL2_PHASE_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL2_PHASE_STATUS[35:0] | R/O | 0 | Signed 36-bit phase offset in ITDC_UIs. |

### STATUS.DPLL3_PHASE_STATUS

Phase offset at output of decimator.

Table 105: STATUS.DPLL3_PHASE_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL3_PHASE_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0F4h | DPLL3_PHASE_STATUS[7:0] | | | | | | | |
| 0F5h | DPLL3_PHASE_STATUS[15:8] | | | | | | | |
| 0F6h | DPLL3_PHASE_STATUS[23:16] | | | | | | | |
| 0F7h | DPLL3_PHASE_STATUS[31:24] | | | | | | | |
| 0F8h | RESERVED[39:36] | | | | DPLL3_PHASE_STATUS[35:32] | | | |

| STATUS.DPLL3_PHASE_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL3_PHASE_STATUS[35:0] | R/O | 0 | Signed 36-bit phase offset in ITDC_UIs. |

### STATUS.DPLL4_PHASE_STATUS

Phase offset at output of decimator.

Table 106: STATUS.DPLL4_PHASE_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL4_PHASE_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0FCh | DPLL4_PHASE_STATUS[7:0] | | | | | | | |
| 0FDh | DPLL4_PHASE_STATUS[15:8] | | | | | | | |
| 0FEh | DPLL4_PHASE_STATUS[23:16] | | | | | | | |
| 0FFh | DPLL4_PHASE_STATUS[31:24] | | | | | | | |
| 100h | RESERVED[39:36] | | | | DPLL4_PHASE_STATUS[35:32] | | | |

| STATUS.DPLL4_PHASE_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL4_PHASE_STATUS[35:0] | R/O | 0 | Signed 36-bit phase offset in ITDC_UIs. |

### STATUS.DPLL5_PHASE_STATUS

Phase offset at output of decimator.

Table 107: STATUS.DPLL5_PHASE_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL5_PHASE_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 104h | DPLL5_PHASE_STATUS[7:0] | | | | | | | |
| 105h | DPLL5_PHASE_STATUS[15:8] | | | | | | | |
| 106h | DPLL5_PHASE_STATUS[23:16] | | | | | | | |
| 107h | DPLL5_PHASE_STATUS[31:24] | | | | | | | |
| 108h | RESERVED[39:36] | | | | DPLL5_PHASE_STATUS[35:32] | | | |

| STATUS.DPLL5_PHASE_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL5_PHASE_STATUS[35:0] | R/O | 0 | Signed 36-bit phase offset in ITDC_UIs. |

### STATUS.DPLL6_PHASE_STATUS

Phase offset at output of decimator.

Table 108: STATUS.DPLL6_PHASE_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL6_PHASE_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 10Ch | DPLL6_PHASE_STATUS[7:0] | | | | | | | |
| 10Dh | DPLL6_PHASE_STATUS[15:8] | | | | | | | |
| 10Eh | DPLL6_PHASE_STATUS[23:16] | | | | | | | |
| 10Fh | DPLL6_PHASE_STATUS[31:24] | | | | | | | |
| 110h | RESERVED[39:36] | | | | DPLL6_PHASE_STATUS[35:32] | | | |

| STATUS.DPLL6_PHASE_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL6_PHASE_STATUS[35:0] | R/O | 0 | Signed 36-bit phase offset in ITDC_UIs. |

### STATUS.DPLL7_PHASE_STATUS

Phase offset at output of decimator.

Table 109: STATUS.DPLL7_PHASE_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL7_PHASE_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 114h | DPLL7_PHASE_STATUS[7:0] | | | | | | | |
| 115h | DPLL7_PHASE_STATUS[15:8] | | | | | | | |
| 116h | DPLL7_PHASE_STATUS[23:16] | | | | | | | |
| 117h | DPLL7_PHASE_STATUS[31:24] | | | | | | | |
| 118h | RESERVED[39:36] | | | | DPLL7_PHASE_STATUS[35:32] | | | |

| STATUS.DPLL7_PHASE_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL7_PHASE_STATUS[35:0] | R/O | 0 | Signed 36-bit phase offset in ITDC_UIs. |

### STATUS.DPLL0_PHASE_PULL_IN_STATUS

DPLL0 phase pull-in status

Table 110: STATUS.DPLL0_PHASE_PULL_IN_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL0_PHASE_PULL_IN_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 11Ch | REMAINING_TIME[7:0] | | | | | | | |

| STATUS.DPLL0_PHASE_PULL_IN_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| REMAINING_TIME[7:0] | R/O | 0 | Unsigned 8-bit phase pull-in time to finish in seconds.<br>If the value of this field < 255, the actual remaining time is between (remaining_time) and (remaining_time + 1) seconds. If the value = 255, it implies the actual remaining time >= 255 seconds. |

### STATUS.DPLL1_PHASE_PULL_IN_STATUS

DPLL1 phase pull-in status

Table 111: STATUS.DPLL1_PHASE_PULL_IN_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL1_PHASE_PULL_IN_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 11Dh | REMAINING_TIME[7:0] | | | | | | | |

| STATUS.DPLL1_PHASE_PULL_IN_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| REMAINING_TIME[7:0] | R/O | 0 | Unsigned 8-bit phase pull-in time to finish in seconds.<br>If the value of this field < 255, the actual remaining time is between (remaining_time) and (remaining_time + 1) seconds. If the value = 255, it implies the actual remaining time >= 255 seconds. |

### STATUS.DPLL2_PHASE_PULL_IN_STATUS

DPLL2 phase pull-in status

Table 112: STATUS.DPLL2_PHASE_PULL_IN_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL2_PHASE_PULL_IN_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 11Eh | REMAINING_TIME[7:0] | | | | | | | |

| STATUS.DPLL2_PHASE_PULL_IN_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| REMAINING_TIME[7:0] | R/O | 0 | Unsigned 8-bit phase pull-in time to finish in seconds.<br>If the value of this field < 255, the actual remaining time is between (remaining_time) and (remaining_time + 1) seconds. If the value = 255, it implies the actual remaining time >= 255 seconds. |

### STATUS.DPLL3_PHASE_PULL_IN_STATUS

DPLL3 phase pull-in status

Table 113: STATUS.DPLL3_PHASE_PULL_IN_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL3_PHASE_PULL_IN_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 11Fh | REMAINING_TIME[7:0] | | | | | | | |

| STATUS.DPLL3_PHASE_PULL_IN_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| REMAINING_TIME[7:0] | R/O | 0 | Unsigned 8-bit phase pull-in time to finish in seconds.<br>If the value of this field < 255, the actual remaining time is between (remaining_time) and (remaining_time + 1) seconds. If the value = 255, it implies the actual remaining time >= 255 seconds. |

### STATUS.DPLL4_PHASE_PULL_IN_STATUS

DPLL4 phase pull-in status

Table 114: STATUS.DPLL4_PHASE_PULL_IN_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL4_PHASE_PULL_IN_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 120h | REMAINING_TIME[7:0] | | | | | | | |

| STATUS.DPLL4_PHASE_PULL_IN_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| REMAINING_TIME[7:0] | R/O | 0 | Unsigned 8-bit phase pull-in time to finish in seconds.<br>If the value of this field < 255, the actual remaining time is between (remaining_time) and (remaining_time + 1) seconds. If the value = 255, it implies the actual remaining time >= 255 seconds. |

### STATUS.DPLL5_PHASE_PULL_IN_STATUS

DPLL5 phase pull-in status

Table 115: STATUS.DPLL5_PHASE_PULL_IN_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL5_PHASE_PULL_IN_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 121h | REMAINING_TIME[7:0] | | | | | | | |

| STATUS.DPLL5_PHASE_PULL_IN_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| REMAINING_TIME[7:0] | R/O | 0 | Unsigned 8-bit phase pull-in time to finish in seconds.<br>If the value of this field < 255, the actual remaining time is between (remaining_time) and (remaining_time + 1) seconds. If the value = 255, it implies the actual remaining time >= 255 seconds. |

### STATUS.DPLL6_PHASE_PULL_IN_STATUS

DPLL6 phase pull-in status

Table 116: STATUS.DPLL6_PHASE_PULL_IN_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL6_PHASE_PULL_IN_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 122h | REMAINING_TIME[7:0] | | | | | | | |

| STATUS.DPLL6_PHASE_PULL_IN_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| REMAINING_TIME[7:0] | R/O | 0 | Unsigned 8-bit phase pull-in time to finish in seconds.<br>If the value of this field < 255, the actual remaining time is between (remaining_time) and (remaining_time + 1) seconds. If the value = 255, it implies the actual remaining time >= 255 seconds. |

### STATUS.DPLL7_PHASE_PULL_IN_STATUS

DPLL7 phase pull-in status

Table 117: STATUS.DPLL7_PHASE_PULL_IN_STATUS Bit Field Locations and Descriptions

| Offset Address (Hex) | STATUS.DPLL7_PHASE_PULL_IN_STATUS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 123h | REMAINING_TIME[7:0] | | | | | | | |

| STATUS.DPLL7_PHASE_PULL_IN_STATUS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| REMAINING_TIME[7:0] | R/O | 0 | Unsigned 8-bit phase pull-in time to finish in seconds.<br>If the value of this field < 255, the actual remaining time is between (remaining_time) and (remaining_time + 1) seconds. If the value = 255, it implies the actual remaining time >= 255 seconds. |

## Module: GPIO_USER_CONTROL

Configures the controls of the GPIO .

Table 118: GPIO_USER_CONTROL Register Index

| Offset (Hex) | Register Module Base Address: C160h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | GPIO_USER_CONTROL.GPIO0_TO_7_OUT | GPIO output control. |
| 001h | GPIO_USER_CONTROL.GPIO8_TO_15_OUT | GPIO output control. |

### GPIO_USER_CONTROL.GPIO0_TO_7_OUT

Write these bits to define the level on a GPIO output pin when configured for user output control.

Table 119: GPIO_USER_CONTROL.GPIO0_TO_7_OUT Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_USER_CONTROL.GPIO0_TO_7_OUT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | GPIO7_DRIVE_LEVEL[7] | GPIO6_DRIVE_LEVEL[6] | GPIO5_DRIVE_LEVEL[5] | GPIO4_DRIVE_LEVEL[4] | GPIO3_DRIVE_LEVEL[3] | GPIO2_DRIVE_LEVEL[2] | GPIO1_DRIVE_LEVEL[1] | GPIO0_DRIVE_LEVEL[0] |

| GPIO_USER_CONTROL.GPIO0_TO_7_OUT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| GPIO7_DRIVE_LEVEL[7] | R/W | 0 | GPIO pin 7 drive level.<br>Valid only if GPIO_FUNCTION is disabled and 'gpio_control_dir' is output.<br>0 = drive low<br>1 = drive high |
| GPIO6_DRIVE_LEVEL[6] | R/W | 0 | GPIO pin 6 drive level.<br>Valid only if GPIO_FUNCTION is disabled and 'gpio_control_dir' is output.<br>0 = drive low<br>1 = drive high |
| GPIO5_DRIVE_LEVEL[5] | R/W | 0 | GPIO pin 5 drive level.<br>Valid only if GPIO_FUNCTION is disabled and 'gpio_control_dir' is output.<br>0 = drive low<br>1 = drive high |

| GPIO_USER_CONTROL.GPIO0_TO_7_OUT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| GPIO4_DRIVE_LEVEL[4] | R/W | 0 | GPIO pin 4 drive level.<br>Valid only if GPIO_FUNCTION is disabled and 'gpio_control_dir' is output.<br>0 = drive low<br>1 = drive high |
| GPIO3_DRIVE_LEVEL[3] | R/W | 0 | GPIO pin 3 drive level.<br>Valid only if GPIO_FUNCTION is disabled and 'gpio_control_dir' is output.<br>0 = drive low<br>1 = drive high |
| GPIO2_DRIVE_LEVEL[2] | R/W | 0 | GPIO pin 2 drive level.<br>Valid only if GPIO_FUNCTION is disabled and 'gpio_control_dir' is output.<br>0 = drive low<br>1 = drive high |
| GPIO1_DRIVE_LEVEL[1] | R/W | 0 | GPIO pin 1 drive level.<br>Valid only if GPIO_FUNCTION is disabled and 'gpio_control_dir' is output.<br>0 = drive low<br>1 = drive high |
| GPIO0_DRIVE_LEVEL[0] | R/W | 0 | GPIO pin 0 drive level.<br>Valid only if GPIO_FUNCTION is disabled and 'gpio_control_dir' is output.<br>0 = drive low<br>1 = drive high |

### GPIO_USER_CONTROL.GPIO8_TO_15_OUT

Write these bits to define the level on a GPIO output pin when configured for user output control.

TRIGGER: Writing to this byte triggers a read and activation in hardware of all the bytes of the GPIO_USER_CONTROL module.

Table 120: GPIO_USER_CONTROL.GPIO8_TO_15_OUT Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_USER_CONTROL.GPIO8_TO_15_OUT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 001h | GPIO15_DRIVE_LEVEL[7] | GPIO14_DRIVE_LEVEL[6] | GPIO13_DRIVE_LEVEL[5] | GPIO12_DRIVE_LEVEL[4] | GPIO11_DRIVE_LEVEL[3] | GPIO10_DRIVE_LEVEL[2] | GPIO9_DRIVE_LEVEL[1] | GPIO8_DRIVE_LEVEL[0] |

| GPIO_USER_CONTROL.GPIO8_TO_15_OUT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| GPIO15_DRIVE_LEVEL[7] | R/W | 0 | GPIO pin 15 drive level.<br>Valid only if GPIO_FUNCTION is disabled and 'gpio_control_dir' is output.<br>0 = drive low<br>1 = drive high |
| GPIO14_DRIVE_LEVEL[6] | R/W | 0 | GPIO pin 14 drive level.<br>Valid only if GPIO_FUNCTION is disabled and 'gpio_control_dir' is output.<br>0 = drive low<br>1 = drive high |
| GPIO13_DRIVE_LEVEL[5] | R/W | 0 | GPIO pin 13 drive level.<br>Valid only if GPIO_FUNCTION is disabled and 'gpio_control_dir' is output.<br>0 = drive low<br>1 = drive high |
| GPIO12_DRIVE_LEVEL[4] | R/W | 0 | GPIO pin 12 drive level.<br>Valid only if GPIO_FUNCTION is disabled and 'gpio_control_dir' is output.<br>0 = drive low<br>1 = drive high |
| GPIO11_DRIVE_LEVEL[3] | R/W | 0 | GPIO pin 11 drive level.<br>Valid only if GPIO_FUNCTION is disabled and 'gpio_control_dir' is output.<br>0 = drive low<br>1 = drive high |
| GPIO10_DRIVE_LEVEL[2] | R/W | 0 | GPIO pin 10 drive level.<br>Valid only if GPIO_FUNCTION is disabled and 'gpio_control_dir' is output.<br>0 = drive low<br>1 = drive high |
| GPIO9_DRIVE_LEVEL[1] | R/W | 0 | GPIO pin 9 drive level.<br>Valid only if GPIO_FUNCTION is disabled and 'gpio_control_dir' is output.<br>0 = drive low<br>1 = drive high |
| GPIO8_DRIVE_LEVEL[0] | R/W | 0 | GPIO pin 8 drive level.<br>Valid only if GPIO_FUNCTION is disabled and 'gpio_control_dir' is output.<br>0 = drive low<br>1 = drive high |

## Module: STICKY_STATUS_CLEAR

TRIGGER: Every register in this module is a trigger register. In the case of a multibyte register the highest address register byte is the trigger byte.

-

Table 121: STICKY_STATUS_CLEAR Register Index

| Offset (Hex) | Register Module Base Address: C164h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | STICKY_STATUS_CLEAR.IN0_TO_7_MON_STICKY_STATUS_CLEAR | Clear sticky reference monitor status. |
| 001h | STICKY_STATUS_CLEAR.IN8_TO_15_MON_STICKY_STATUS_CLEAR | Clear sticky reference monitor status. |
| 002h | STICKY_STATUS_CLEAR.DPLL_STICKY_STATUS_CLEAR | Clear sticky DPLL status. |
| 003h | STICKY_STATUS_CLEAR.DPLL_SYS_STICKY_STATUS_CLEAR | Clear sticky system DPLL status. |
| 004h | STICKY_STATUS_CLEAR.SYS_APLL_STICKY_STATUS_CLEAR | Clear sticky system APLL status. |
| 005h | STICKY_STATUS_CLEAR.ALL_STICKY_STATUS_CLEAR | Clear all sticky status bits. |

## STICKY_STATUS_CLEAR.IN0_TO_7_MON_STICKY_STATUS_CLEAR

Clear sticky reference monitor bits for a particular input.

Table 122: STICKY_STATUS_CLEAR.IN0_TO_7_MON_STICKY_STATUS_CLEAR Bit Field Locations and Descriptions

| Offset Address (Hex) | STICKY_STATUS_CLEAR.IN0_TO_7_MON_STICKY_STATUS_CLEAR Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | IN7_MON_STICKY_CLEAR[7] | IN6_MON_STICKY_CLEAR[6] | IN5_MON_STICKY_CLEAR[5] | IN4_MON_STICKY_CLEAR[4] | IN3_MON_STICKY_CLEAR[3] | IN2_MON_STICKY_CLEAR[2] | IN1_MON_STICKY_CLEAR[1] | IN0_MON_STICKY_CLEAR[0] |

| STICKY_STATUS_CLEAR.IN0_TO_7_MON_STICKY_STATUS_CLEAR Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN7_MON_STICKY_CLEAR[7] | RW1C | 0 | Write 1 to clear the sticky bits of input 7. |
| IN6_MON_STICKY_CLEAR[6] | RW1C | 0 | Write 1 to clear the sticky bits of input 6. |
| IN5_MON_STICKY_CLEAR[5] | RW1C | 0 | Write 1 to clear the sticky bits of input 5. |
| IN4_MON_STICKY_CLEAR[4] | RW1C | 0 | Write 1 to clear the sticky bits of input 4. |
| IN3_MON_STICKY_CLEAR[3] | RW1C | 0 | Write 1 to clear the sticky bits of input 3. |

| STICKY_STATUS_CLEAR.IN0_TO_7_MON_STICKY_STATUS_CLEAR Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN2_MON_STICKY_CLEAR[2] | RW1C | 0 | Write 1 to clear the sticky bits of input 2. |
| IN1_MON_STICKY_CLEAR[1] | RW1C | 0 | Write 1 to clear the sticky bits of input 1. |
| IN0_MON_STICKY_CLEAR[0] | RW1C | 0 | Write 1 to clear the sticky bits of input 0. |

### STICKY_STATUS_CLEAR.IN8_TO_15_MON_STICKY_STATUS_CLEAR

Clear sticky reference monitor bits for a particular input.

Table 123: STICKY_STATUS_CLEAR.IN8_TO_15_MON_STICKY_STATUS_CLEAR Bit Field Locations and Descriptions

| Offset Address (Hex) | STICKY_STATUS_CLEAR.IN8_TO_15_MON_STICKY_STATUS_CLEAR Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 001h | IN15_MON_STICKY_CLEAR[7] | IN14_MON_STICKY_CLEAR[6] | IN13_MON_STICKY_CLEAR[5] | IN12_MON_STICKY_CLEAR[4] | IN11_MON_STICKY_CLEAR[3] | IN10_MON_STICKY_CLEAR[2] | IN9_MON_STICKY_CLEAR[1] | IN8_MON_STICKY_CLEAR[0] |

| STICKY_STATUS_CLEAR.IN8_TO_15_MON_STICKY_STATUS_CLEAR Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN15_MON_STICKY_CLEAR[7] | RW1C | 0 | Write 1 to clear the sticky bits of input 15. |
| IN14_MON_STICKY_CLEAR[6] | RW1C | 0 | Write 1 to clear the sticky bits of input 14. |
| IN13_MON_STICKY_CLEAR[5] | RW1C | 0 | Write 1 to clear the sticky bits of input 13. |
| IN12_MON_STICKY_CLEAR[4] | RW1C | 0 | Write 1 to clear the sticky bits of input 12. |
| IN11_MON_STICKY_CLEAR[3] | RW1C | 0 | Write 1 to clear the sticky bits of input 11. |
| IN10_MON_STICKY_CLEAR[2] | RW1C | 0 | Write 1 to clear the sticky bits of input 10. |
| IN9_MON_STICKY_CLEAR[1] | RW1C | 0 | Write 1 to clear the sticky bits of input 9. |
| IN8_MON_STICKY_CLEAR[0] | RW1C | 0 | Write 1 to clear the sticky bits of input 8. |

### STICKY_STATUS_CLEAR.DPLL_STICKY_STATUS_CLEAR

Clear sticky state change bits for a particular DPLL.

Table 124: STICKY_STATUS_CLEAR.DPLL_STICKY_STATUS_CLEAR Bit Field Locations and Descriptions

| Offset Address (Hex) | STICKY_STATUS_CLEAR.DPLL_STICKY_STATUS_CLEAR Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | DPLL7_STICKY_CLEAR[7] | DPLL6_STICKY_CLEAR[6] | DPLL5_STICKY_CLEAR[5] | DPLL4_STICKY_CLEAR[4] | DPLL3_STICKY_CLEAR[3] | DPLL2_STICKY_CLEAR[2] | DPLL1_STICKY_CLEAR[1] | DPLL0_STICKY_CLEAR[0] |

| STICKY_STATUS_CLEAR.DPLL_STICKY_STATUS_CLEAR Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL7_STICKY_CLEAR[7] | RW1C | 0 | Write 1 to clear the sticky bits of DPLL 7. |
| DPLL6_STICKY_CLEAR[6] | RW1C | 0 | Write 1 to clear the sticky bits of DPLL 6. |
| DPLL5_STICKY_CLEAR[5] | RW1C | 0 | Write 1 to clear the sticky bits of DPLL 5. |
| DPLL4_STICKY_CLEAR[4] | RW1C | 0 | Write 1 to clear the sticky bits of DPLL 4. |
| DPLL3_STICKY_CLEAR[3] | RW1C | 0 | Write 1 to clear the sticky bits of DPLL 3. |
| DPLL2_STICKY_CLEAR[2] | RW1C | 0 | Write 1 to clear the sticky bits of DPLL 2. |
| DPLL1_STICKY_CLEAR[1] | RW1C | 0 | Write 1 to clear the sticky bits of DPLL 1. |
| DPLL0_STICKY_CLEAR[0] | RW1C | 0 | Write 1 to clear the sticky bits of DPLL 0. |

### STICKY_STATUS_CLEAR.DPLL_SYS_STICKY_STATUS_CLEAR

Clear sticky state change bits for system DPLL.

Table 125: STICKY_STATUS_CLEAR.DPLL_SYS_STICKY_STATUS_CLEAR Bit Field Locations and Descriptions

| Offset Address (Hex) | STICKY_STATUS_CLEAR.DPLL_SYS_STICKY_STATUS_CLEAR Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 003h | RESERVED[7:1] | | | | | | | DPLL_SYS_STICKY_CLEAR[0] |

| STICKY_STATUS_CLEAR.DPLL_SYS_STICKY_STATUS_CLEAR Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL_SYS_STICKY_CLEAR[0] | RW1C | 0 | Write 1 to clear the sticky bits of system DPLL. |

### STICKY_STATUS_CLEAR.SYS_APLL_STICKY_STATUS_CLEAR

Clear sticky loss-of-lock bit for system APLL.

-

Table 126: STICKY_STATUS_CLEAR.SYS_APLL_STICKY_STATUS_CLEAR Bit Field Locations and Descriptions

| Offset Address (Hex) | STICKY_STATUS_CLEAR.SYS_APLL_STICKY_STATUS_CLEAR Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | RESERVED[7:1] | | | | | | | SYS_APLL_STICKY_CLEAR[0] |

| STICKY_STATUS_CLEAR.SYS_APLL_STICKY_STATUS_CLEAR Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| SYS_APLL_STICKY_CLEAR[0] | RW1C | 0 | Write 1 to clear the sticky bit of system APLL. |

### STICKY_STATUS_CLEAR.ALL_STICKY_STATUS_CLEAR

Clear all sticky status bits in the STATUS module.

Table 127: STICKY_STATUS_CLEAR.ALL_STICKY_STATUS_CLEAR Bit Field Locations and Descriptions

| Offset Address (Hex) | STICKY_STATUS_CLEAR.ALL_STICKY_STATUS_CLEAR Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 005h | RESERVED[7:1] | | | | | | | ALL_STICKY_CLEAR[0] |

| STICKY_STATUS_CLEAR.ALL_STICKY_STATUS_CLEAR Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| ALL_STICKY_CLEAR[0] | RW1C | 0 | Write 1 to clear all sticky bits. |

## Module: GPIO_TOD_NOTIFICATION_CLEAR

TRIGGER: Writing to this byte triggers a read and activation in hardware of all the bytes of the SYS_TOD_NOTIFICATION_CLEAR module.

Table 128: GPIO_TOD_NOTIFICATION_CLEAR Register Index

| Offset (Hex) | Register Module Base Address: C16Ch | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | GPIO_TOD_NOTIFICATION_CLEAR.GPIO0_TO_7_CLEAR | Clear GPIO output time of day read notification. |
| 001h | GPIO_TOD_NOTIFICATION_CLEAR.GPIO8_TO_15_CLEAR | Clear GPIO output time of day read notification. |

### GPIO_TOD_NOTIFICATION_CLEAR.GPIO0_TO_7_CLEAR

Clear GPIO output time of day read notification.

Table 129: GPIO_TOD_NOTIFICATION_CLEAR.GPIO0_TO_7_CLEAR Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_TOD_NOTIFICATION_CLEAR.GPIO0_TO_7_CLEAR Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | GPIO7_CLEAR[7] | GPIO6_CLEAR[6] | GPIO5_CLEAR[5] | GPIO4_CLEAR[4] | GPIO3_CLEAR[3] | GPIO2_CLEAR[2] | GPIO1_CLEAR[1] | GPIO0_CLEAR[0] |

| GPIO_TOD_NOTIFICATION_CLEAR.GPIO0_TO_7_CLEAR Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| GPIO7_CLEAR[7] | RW1C | 0 | Write 1 to clear GPIO7 assertion. |
| GPIO6_CLEAR[6] | RW1C | 0 | Write 1 to clear GPIO6 assertion. |
| GPIO5_CLEAR[5] | RW1C | 0 | Write 1 to clear GPIO5 assertion. |
| GPIO4_CLEAR[4] | RW1C | 0 | Write 1 to clear GPIO4 assertion. |
| GPIO3_CLEAR[3] | RW1C | 0 | Write 1 to clear GPIO3 assertion. |
| GPIO2_CLEAR[2] | RW1C | 0 | Write 1 to clear GPIO2 assertion. |
| GPIO1_CLEAR[1] | RW1C | 0 | Write 1 to clear GPIO1 assertion. |
| GPIO0_CLEAR[0] | RW1C | 0 | Write 1 to clear GPIO0 assertion. |

### GPIO_TOD_NOTIFICATION_CLEAR.GPIO8_TO_15_CLEAR

Clear GPIO output time of day read notification.

Table 130: GPIO_TOD_NOTIFICATION_CLEAR.GPIO8_TO_15_CLEAR Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_TOD_NOTIFICATION_CLEAR.GPIO8_TO_15_CLEAR Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 001h | GPIO15_CLEAR[7] | GPIO14_CLEAR[6] | GPIO13_CLEAR[5] | GPIO12_CLEAR[4] | GPIO11_CLEAR[3] | GPIO10_CLEAR[2] | GPIO9_CLEAR[1] | GPIO8_CLEAR[0] |

| GPIO_TOD_NOTIFICATION_CLEAR.GPIO8_TO_15_CLEAR Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| GPIO15_CLEAR[7] | RW1C | 0 | Write 1 to clear GPIO15 assertion. |
| GPIO14_CLEAR[6] | RW1C | 0 | Write 1 to clear GPIO14 assertion. |
| GPIO13_CLEAR[5] | RW1C | 0 | Write 1 to clear GPIO13 assertion. |
| GPIO12_CLEAR[4] | RW1C | 0 | Write 1 to clear GPIO12 assertion. |
| GPIO11_CLEAR[3] | RW1C | 0 | Write 1 to clear GPIO11 assertion. |
| GPIO10_CLEAR[2] | RW1C | 0 | Write 1 to clear GPIO10 assertion. |
| GPIO9_CLEAR[1] | RW1C | 0 | Write 1 to clear GPIO9 assertion. |
| GPIO8_CLEAR[0] | RW1C | 0 | Write 1 to clear GPIO8 assertion. |

## Module: ALERT_CFG

Global alert configuration.

Table 131: ALERT_CFG Register Index

| Offset (Hex) | Register Module Base Address: C188h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | ALERT_CFG.IN1_0_MON_ALERT_MASK | GPIO alert enable masks for reference monitors 0 and 1. |
| 001h | ALERT_CFG.IN3_2_MON_ALERT_MASK | GPIO alert enable masks for reference monitors 2 and 3. |
| 002h | ALERT_CFG.IN5_4_MON_ALERT_MASK | GPIO alert enable masks for reference monitors 4 and 5. |
| 003h | ALERT_CFG.IN7_6_MON_ALERT_MASK | GPIO alert enable masks for reference monitors 6 and 7. |
| 004h | ALERT_CFG.IN9_8_MON_ALERT_MASK | GPIO alert enable masks for reference monitors 8 and 9. |
| 005h | ALERT_CFG.IN11_10_MON_ALERT_MASK | GPIO alert enable masks for reference monitors 10 and 11. |
| 006h | ALERT_CFG.IN13_12_MON_ALERT_MASK | GPIO alert enable masks for reference monitors 12 and 13. |
| 007h | ALERT_CFG.IN15_14_MON_ALERT_MASK | GPIO alert enable masks for reference monitors 14 and 15. |
| 008h | ALERT_CFG.DPLL3_2_1_0_ALERT_MASK | GPIO alert enable masks for DPLL 0,1, 2 and 3. |
| 009h | ALERT_CFG.DPLL7_6_5_4_ALERT_MASK | GPIO alert enable masks for DPLLs 4, 5, 6 and 7. |
| 00Ah | ALERT_CFG.SYS_ALERT_MASK | GPIO alert enable masks for system DPLL and system APLL. |

### ALERT_CFG.IN1_0_MON_ALERT_MASK

GPIO alert enable masks (transient, frequency offset, no activity, loss of signal) for reference monitors 0 and 1.

Table 132: ALERT_CFG.IN1_0_MON_ALERT_MASK Bit Field Locations and Descriptions

| Offset Address (Hex) | ALERT_CFG.IN1_0_MON_ALERT_MASK Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | IN1_TRANS_DETECT_MASK[7] | IN1_FREQ_OFFS_LIM_MASK[6] | IN1_NO_ACTIVITY_MASK[5] | IN1_LOS_MASK[4] | IN0_TRANS_DETECT_MASK[3] | IN0_FREQ_OFFS_LIM_MASK[2] | IN0_NO_ACTIVITY_MASK[1] | IN0_LOS_MASK[0] |

| ALERT_CFG.IN1_0_MON_ALERT_MASK Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN1_TRANS_DETECT_MASK[7] | R/W | 0 | Input 1 transient detector mask.<br>If enabled, GPIO alert becomes active when in1_trans_detect_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN1_FREQ_OFFS_LIM_MASK[6] | R/W | 0 | Input 1 frequency offset limit enable mask.<br>If enabled, GPIO alert becomes active when in1_freq_offs_lim_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN1_NO_ACTIVITY_MASK[5] | R/W | 0 | Input 1 no activity enable mask.<br>If enabled, GPIO alert becomes active when in1_no_activity_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN1_LOS_MASK[4] | R/W | 0 | Input 1 LOS enable mask.<br>If enabled, GPIO alert becomes active when in1_los_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN0_TRANS_DETECT_MASK[3] | R/W | 0 | Input 0 transient detector mask.<br>If enabled, GPIO alert becomes active when in0_trans_detect_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN0_FREQ_OFFS_LIM_MASK[2] | R/W | 0 | Input 0 frequency offset limit enable mask.<br>If enabled, GPIO alert becomes active when in0_freq_offs_lim_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN0_NO_ACTIVITY_MASK[1] | R/W | 0 | Input 0 no activity enable mask.<br>If enabled, GPIO alert becomes active when in0_no_activity_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN0_LOS_MASK[0] | R/W | 0 | Input 0 LOS enable mask.<br>If enabled, GPIO alert becomes active when in0_los_sticky bit is set.<br>0 = disabled<br>1 = enabled |

### ALERT_CFG.IN3_2_MON_ALERT_MASK

GPIO alert enable masks (transient, frequency offset, no activity, loss of signal) for reference monitors 2 and 3.

Table 133: ALERT_CFG.IN3_2_MON_ALERT_MASK Bit Field Locations and Descriptions

| Offset Address (Hex) | ALERT_CFG.IN3_2_MON_ALERT_MASK Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 001h | IN3_TRANS_DETECT_MASK[7] | IN3_FREQ_OFFS_LIM_MASK[6] | IN3_NO_ACTIVITY_MASK[5] | IN3_LOS_MASK[4] | IN2_TRANS_DETECT_MASK[3] | IN2_FREQ_OFFS_LIM_MASK[2] | IN2_NO_ACTIVITY_MASK[1] | IN2_LOS_MASK[0] |

| ALERT_CFG.IN3_2_MON_ALERT_MASK Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN3_TRANS_DETECT_MASK[7] | R/W | 0 | Input 3 transient detector mask.<br>If enabled, GPIO alert becomes active when in3_trans_detect_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN3_FREQ_OFFS_LIM_MASK[6] | R/W | 0 | Input 3 frequency offset limit enable mask.<br>If enabled, GPIO alert becomes active when in3_freq_offs_lim_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN3_NO_ACTIVITY_MASK[5] | R/W | 0 | Input 3 no activity enable mask.<br>If enabled, GPIO alert becomes active when in3_no_activity_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN3_LOS_MASK[4] | R/W | 0 | Input 3 LOS enable mask.<br>If enabled, GPIO alert becomes active when in3_los_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN2_TRANS_DETECT_MASK[3] | R/W | 0 | Input 2 transient detector mask.<br>If enabled, GPIO alert becomes active when in2_trans_detect_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN2_FREQ_OFFS_LIM_MASK[2] | R/W | 0 | Input 2 frequency offset limit enable mask.<br>If enabled, GPIO alert becomes active when in2_freq_offs_lim_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN2_NO_ACTIVITY_MASK[1] | R/W | 0 | Input 2 no activity enable mask.<br>If enabled, GPIO alert becomes active when in2_no_activity_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN2_LOS_MASK[0] | R/W | 0 | Input 2 LOS enable mask.<br>If enabled, GPIO alert becomes active when in2_los_sticky bit is set.<br>0 = disabled<br>1 = enabled |

### ALERT_CFG.IN5_4_MON_ALERT_MASK

GPIO alert enable masks (transient, frequency offset, no activity, loss of signal) for reference monitors 4 and 5.

Table 134: ALERT_CFG.IN5_4_MON_ALERT_MASK Bit Field Locations and Descriptions

| Offset Address (Hex) | ALERT_CFG.IN5_4_MON_ALERT_MASK Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | IN5_TRANS_DETECT_MASK[7] | IN5_FREQ_OFFS_LIM_MASK[6] | IN5_NO_ACTIVITY_MASK[5] | IN5_LOS_MASK[4] | IN4_TRANS_DETECT_MASK[3] | IN4_FREQ_OFFS_LIM_MASK[2] | IN4_NO_ACTIVITY_MASK[1] | IN4_LOS_MASK[0] |

| ALERT_CFG.IN5_4_MON_ALERT_MASK Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN5_TRANS_DETECT_MASK[7] | R/W | 0 | Input 5 transient detector mask.<br>If enabled, GPIO alert becomes active when in5_trans_detect_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN5_FREQ_OFFS_LIM_MASK[6] | R/W | 0 | Input 5 frequency offset limit enable mask.<br>If enabled, GPIO alert becomes active when in5_freq_offs_lim_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN5_NO_ACTIVITY_MASK[5] | R/W | 0 | Input 5 no activity enable mask.<br>If enabled, GPIO alert becomes active when in5_no_activity_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN5_LOS_MASK[4] | R/W | 0 | Input 5 LOS enable mask.<br>If enabled, GPIO alert becomes active when in5_los_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN4_TRANS_DETECT_MASK[3] | R/W | 0 | Input 4 transient detector mask.<br>If enabled, GPIO alert becomes active when in4_trans_detect_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN4_FREQ_OFFS_LIM_MASK[2] | R/W | 0 | Input 4 frequency offset limit enable mask.<br>If enabled, GPIO alert becomes active when in4_freq_offs_lim_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN4_NO_ACTIVITY_MASK[1] | R/W | 0 | Input 4 no activity enable mask.<br>If enabled, GPIO alert becomes active when in4_no_activity_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN4_LOS_MASK[0] | R/W | 0 | Input 4 LOS enable mask.<br>If enabled, GPIO alert becomes active when in4_los_sticky bit is set.<br>0 = disabled<br>1 = enabled |

### ALERT_CFG.IN7_6_MON_ALERT_MASK

GPIO alert enable masks (transient, frequency offset, no activity, loss of signal) for reference monitors 7 and 6.

Table 135: ALERT_CFG.IN7_6_MON_ALERT_MASK Bit Field Locations and Descriptions

| Offset Address (Hex) | ALERT_CFG.IN7_6_MON_ALERT_MASK Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 003h | IN7_TRANS_DETECT_MASK[7] | IN7_FREQ_OFFS_LIM_MASK[6] | IN7_NO_ACTIVITY_MASK[5] | IN7_LOS_MASK[4] | IN6_TRANS_DETECT_MASK[3] | IN6_FREQ_OFFS_LIM_MASK[2] | IN6_NO_ACTIVITY_MASK[1] | IN6_LOS_MASK[0] |

| ALERT_CFG.IN7_6_MON_ALERT_MASK Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN7_TRANS_DETECT_MASK[7] | R/W | 0 | Input 7 transient detector mask.<br>If enabled, GPIO alert becomes active when in7_trans_detect_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN7_FREQ_OFFS_LIM_MASK[6] | R/W | 0 | Input 7 frequency offset limit enable mask.<br>If enabled, GPIO alert becomes active when in7_freq_offs_lim_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN7_NO_ACTIVITY_MASK[5] | R/W | 0 | Input 7 no activity enable mask.<br>If enabled, GPIO alert becomes active when in7_no_activity_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN7_LOS_MASK[4] | R/W | 0 | Input 7 LOS enable mask.<br>If enabled, GPIO alert becomes active when in7_los_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN6_TRANS_DETECT_MASK[3] | R/W | 0 | Input 6 transient detector mask.<br>If enabled, GPIO alert becomes active when in6_trans_detect_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN6_FREQ_OFFS_LIM_MASK[2] | R/W | 0 | Input 6 frequency offset limit enable mask.<br>If enabled, GPIO alert becomes active when in6_freq_offs_lim_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN6_NO_ACTIVITY_MASK[1] | R/W | 0 | Input 6 no activity enable mask.<br>If enabled, GPIO alert becomes active when in6_no_activity_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN6_LOS_MASK[0] | R/W | 0 | Input 6 LOS enable mask.<br>If enabled, GPIO alert becomes active when in6_los_sticky bit is set.<br>0 = disabled<br>1 = enabled |

### ALERT_CFG.IN9_8_MON_ALERT_MASK

GPIO alert enable masks (transient, frequency offset, no activity, loss of signal) for reference monitors 8 and 9.

Table 136: ALERT_CFG.IN9_8_MON_ALERT_MASK Bit Field Locations and Descriptions

| Offset Address (Hex) | ALERT_CFG.IN9_8_MON_ALERT_MASK Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | IN9_TRANS_DETECT_MASK[7] | IN9_FREQ_OFFS_LIM_MASK[6] | IN9_NO_ACTIVITY_MASK[5] | IN9_LOS_MASK[4] | IN8_TRANS_DETECT_MASK[3] | IN8_FREQ_OFFS_LIM_MASK[2] | IN8_NO_ACTIVITY_MASK[1] | IN8_LOS_MASK[0] |

| ALERT_CFG.IN9_8_MON_ALERT_MASK Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN9_TRANS_DETECT_MASK[7] | R/W | 0 | Input 9 transient detector mask.<br>If enabled, GPIO alert becomes active when in9_trans_detect_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN9_FREQ_OFFS_LIM_MASK[6] | R/W | 0 | Input 9 frequency offset limit enable mask.<br>If enabled, GPIO alert becomes active when in9_freq_offs_lim_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN9_NO_ACTIVITY_MASK[5] | R/W | 0 | Input 9 no activity enable mask.<br>If enabled, GPIO alert becomes active when in9_no_activity_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN9_LOS_MASK[4] | R/W | 0 | Input 9 LOS enable mask.<br>If enabled, GPIO alert becomes active when in9_los_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN8_TRANS_DETECT_MASK[3] | R/W | 0 | Input 8 transient detector mask.<br>If enabled, GPIO alert becomes active when in8_trans_detect_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN8_FREQ_OFFS_LIM_MASK[2] | R/W | 0 | Input 8 frequency offset limit enable mask.<br>If enabled, GPIO alert becomes active when in8_freq_offs_lim_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN8_NO_ACTIVITY_MASK[1] | R/W | 0 | Input 8 no activity enable mask.<br>If enabled, GPIO alert becomes active when in8_no_activity_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN8_LOS_MASK[0] | R/W | 0 | Input 8 LOS enable mask.<br>If enabled, GPIO alert becomes active when in08_los_sticky bit is set.<br>0 = disabled<br>1 = enabled |

### ALERT_CFG.IN11_10_MON_ALERT_MASK

GPIO alert enable masks (transient, frequency offset, no activity, loss of signal) for reference monitors 10 and 11.

Table 137: ALERT_CFG.IN11_10_MON_ALERT_MASK Bit Field Locations and Descriptions

| Offset Address (Hex) | ALERT_CFG.IN11_10_MON_ALERT_MASK Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 005h | IN11_TRANS_DETECT_MASK[7] | IN11_FREQ_OFFS_LIM_MASK[6] | IN11_NO_ACTIVITY_MASK[5] | IN11_LOS_MASK[4] | IN10_TRANS_DETECT_MASK[3] | IN10_FREQ_OFFS_LIM_MASK[2] | IN10_NO_ACTIVITY_MASK[1] | IN10_LOS_MASK[0] |

| ALERT_CFG.IN11_10_MON_ALERT_MASK Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN11_TRANS_DETECT_MASK[7] | R/W | 0 | Input 11 transient detector mask.<br>If enabled, GPIO alert becomes active when in11_trans_detect_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN11_FREQ_OFFS_LIM_MASK[6] | R/W | 0 | Input 11 frequency offset limit enable mask.<br>If enabled, GPIO alert becomes active when in11_freq_offs_lim_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN11_NO_ACTIVITY_MASK[5] | R/W | 0 | Input 11 no activity enable mask.<br>If enabled, GPIO alert becomes active when in11_no_activity_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN11_LOS_MASK[4] | R/W | 0 | Input 11 LOS enable mask.<br>If enabled, GPIO alert becomes active when in11_los_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN10_TRANS_DETECT_MASK[3] | R/W | 0 | Input 10 transient detector mask.<br>If enabled, GPIO alert becomes active when in10_trans_detect_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN10_FREQ_OFFS_LIM_MASK[2] | R/W | 0 | Input 10 frequency offset limit enable mask.<br>If enabled, GPIO alert becomes active when in10_freq_offs_lim_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN10_NO_ACTIVITY_MASK[1] | R/W | 0 | Input 10 no activity enable mask.<br>If enabled, GPIO alert becomes active when in10_no_activity_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN10_LOS_MASK[0] | R/W | 0 | Input 10 LOS enable mask.<br>If enabled, GPIO alert becomes active when in10_los_sticky bit is set.<br>0 = disabled<br>1 = enabled |

### ALERT_CFG.IN13_12_MON_ALERT_MASK

GPIO alert enable masks (transient, frequency offset, no activity, loss of signal) for reference monitors 12 and 13.

Table 138: ALERT_CFG.IN13_12_MON_ALERT_MASK Bit Field Locations and Descriptions

| Offset Address (Hex) | ALERT_CFG.IN13_12_MON_ALERT_MASK Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 006h | IN13_TRANS_DETECT_MASK[7] | IN13_FREQ_OFFS_LIM_MASK[6] | IN13_NO_ACTIVITY_MASK[5] | IN13_LOS_MASK[4] | IN12_TRANS_DETECT_MASK[3] | IN12_FREQ_OFFS_LIM_MASK[2] | IN12_NO_ACTIVITY_MASK[1] | IN12_LOS_MASK[0] |

| ALERT_CFG.IN13_12_MON_ALERT_MASK Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN13_TRANS_DETECT_MASK[7] | R/W | 0 | Input 13 transient detector mask.<br>If enabled, GPIO alert becomes active when in13_trans_detect_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN13_FREQ_OFFS_LIM_MASK[6] | R/W | 0 | Input 13 frequency offset limit enable mask.<br>If enabled, GPIO alert becomes active when in13_freq_offs_lim_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN13_NO_ACTIVITY_MASK[5] | R/W | 0 | Input 13 no activity enable mask.<br>If enabled, GPIO alert becomes active when in13_no_activity_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN13_LOS_MASK[4] | R/W | 0 | Input 13 LOS enable mask.<br>If enabled, GPIO alert becomes active when in13_los_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN12_TRANS_DETECT_MASK[3] | R/W | 0 | Input 12 transient detector mask.<br>If enabled, GPIO alert becomes active when in12_trans_detect_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN12_FREQ_OFFS_LIM_MASK[2] | R/W | 0 | Input 12 frequency offset limit enable mask.<br>If enabled, GPIO alert becomes active when in12_freq_offs_lim_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN12_NO_ACTIVITY_MASK[1] | R/W | 0 | Input 12 no activity enable mask.<br>If enabled, GPIO alert becomes active when in12_no_activity_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN12_LOS_MASK[0] | R/W | 0 | Input 12 LOS enable mask.<br>If enabled, GPIO alert becomes active when in12_los_sticky bit is set.<br>0 = disabled<br>1 = enabled |

### ALERT_CFG.IN15_14_MON_ALERT_MASK

GPIO alert enable masks (transient, frequency offset, no activity, loss of signal) for reference monitors 14 and 15.

Table 139: ALERT_CFG.IN15_14_MON_ALERT_MASK Bit Field Locations and Descriptions

| Offset Address (Hex) | ALERT_CFG.IN15_14_MON_ALERT_MASK Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 007h | IN15_TRANS_DETECT_MASK[7] | IN15_FREQ_OFFS_LIM_MASK[6] | IN15_NO_ACTIVITY_MASK[5] | IN15_LOS_MASK[4] | IN14_TRANS_DETECT_MASK[3] | IN14_FREQ_OFFS_LIM_MASK[2] | IN14_NO_ACTIVITY_MASK[1] | IN14_LOS_MASK[0] |

| ALERT_CFG.IN15_14_MON_ALERT_MASK Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN15_TRANS_DETECT_MASK[7] | R/W | 0 | Input 15 transient detector mask.<br>If enabled, GPIO alert becomes active when in15_trans_detect_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN15_FREQ_OFFS_LIM_MASK[6] | R/W | 0 | Input 15 frequency offset limit enable mask.<br>If enabled, GPIO alert becomes active when in15_freq_offs_lim_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN15_NO_ACTIVITY_MASK[5] | R/W | 0 | Input 15 no activity enable mask.<br>If enabled, GPIO alert becomes active when in15_no_activity_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN15_LOS_MASK[4] | R/W | 0 | Input 15 LOS enable mask.<br>If enabled, GPIO alert becomes active when in15_los_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN14_TRANS_DETECT_MASK[3] | R/W | 0 | Input 14 transient detector mask.<br>If enabled, GPIO alert becomes active when in14_trans_detect_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN14_FREQ_OFFS_LIM_MASK[2] | R/W | 0 | Input 14 frequency offset limit enable mask.<br>If enabled, GPIO alert becomes active when in14_freq_offs_lim_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN14_NO_ACTIVITY_MASK[1] | R/W | 0 | Input 14 no activity enable mask.<br>If enabled, GPIO alert becomes active when in14_no_activity_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| IN14_LOS_MASK[0] | R/W | 0 | Input 14 LOS enable mask.<br>If enabled, GPIO alert becomes active when in14_los_sticky bit is set.<br>0 = disabled<br>1 = enabled |

### ALERT_CFG.DPLL3_2_1_0_ALERT_MASK

GPIO alert enable masks (holdover, lock) for DPLL 0, 1, 2 and 3.

Table 140: ALERT_CFG.DPLL3_2_1_0_ALERT_MASK Bit Field Locations and Descriptions

| Offset Address (Hex) | ALERT_CFG.DPLL3_2_1_0_ALERT_MASK Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 008h | DPLL3_HOLDOVER_MASK[7] | DPLL3_LOCK_MASK[6] | DPLL2_HOLDOVER_MASK[5] | DPLL2_LOCK_MASK[4] | DPLL1_HOLDOVER_MASK[3] | DPLL1_LOCK_MASK[2] | DPLL0_HOLDOVER_MASK[1] | DPLL0_LOCK_MASK[0] |

| ALERT_CFG.DPLL3_2_1_0_ALERT_MASK Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL3_HOLDOVER_MASK[7] | R/W | 0 | DPLL 3 holdover state transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll3_holdover_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| DPLL3_LOCK_MASK[6] | R/W | 0 | DPLL 3 lock state transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll3_lock_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| DPLL2_HOLDOVER_MASK[5] | R/W | 0 | DPLL 2 holdover state transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll2_holdover_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| DPLL2_LOCK_MASK[4] | R/W | 0 | DPLL 2 lock state transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll2_lock_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| DPLL1_HOLDOVER_MASK[3] | R/W | 0 | DPLL 1 holdover state transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll1_holdover_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| DPLL1_LOCK_MASK[2] | R/W | 0 | DPLL 1 lock state transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll1_lock_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |

| ALERT_CFG.DPLL3_2_1_0_ALERT_MASK Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL0_HOLDOVER_MASK[1] | R/W | 0 | DPLL 0 holdover state transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll0_holdover_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| DPLL0_LOCK_MASK[0] | R/W | 0 | DPLL 0 lock state transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll0_lock_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |

### ALERT_CFG.DPLL7_6_5_4_ALERT_MASK

GPIO alert masks (holdover, lock) for DPLL 4, 5, 6 and 7.

Table 141: ALERT_CFG.DPLL7_6_5_4_ALERT_MASK Bit Field Locations and Descriptions

| Offset Address (Hex) | ALERT_CFG.DPLL7_6_5_4_ALERT_MASK Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 009h | DPLL7_HOLDOVER_MASK[7] | DPLL7_LOCK_MASK[6] | DPLL6_HOLDOVER_MASK[5] | DPLL6_LOCK_MASK[4] | DPLL5_HOLDOVER_MASK[3] | DPLL5_LOCK_MASK[2] | DPLL4_HOLDOVER_MASK[1] | DPLL4_LOCK_MASK[0] |

| ALERT_CFG.DPLL7_6_5_4_ALERT_MASK Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL7_HOLDOVER_MASK[7] | R/W | 0 | DPLL 7 holdover state transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll7_holdover_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| DPLL7_LOCK_MASK[6] | R/W | 0 | DPLL 7 lock state transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll7_lock_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| DPLL6_HOLDOVER_MASK[5] | R/W | 0 | DPLL 6 holdover state transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll6_holdover_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |

| ALERT_CFG.DPLL7_6_5_4_ALERT_MASK Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL6_LOCK_MASK[4] | R/W | 0 | DPLL 6 lock state transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll6_lock_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| DPLL5_HOLDOVER_MASK[3] | R/W | 0 | DPLL 5 holdover state transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll5_holdover_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| DPLL5_LOCK_MASK[2] | R/W | 0 | DPLL 5 lock state transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll5_lock_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| DPLL4_HOLDOVER_MASK[1] | R/W | 0 | DPLL 4 holdover state transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll4_holdover_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| DPLL4_LOCK_MASK[0] | R/W | 0 | DPLL 4 lock state transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll4_lock_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |

### ALERT_CFG.SYS_ALERT_MASK

GPIO alert enable masks (holdover, lock) for system DPLL, and loss-of-lock mask for system APLL.

TRIGGER: Writing to this byte triggers a read and activation in hardware of all the bytes of the SYS_ALERT_CFG module.

Table 142: ALERT_CFG.SYS_ALERT_MASK Bit Field Locations and Descriptions

| Offset Address (Hex) | ALERT_CFG.SYS_ALERT_MASK Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ah | RESERVED[7:3] | | | | | SYS_APLL_LOSS_LOCK_MASK[2] | DPLL_SYS_HOLDOVER_MASK[1] | DPLL_SYS_LOCK_MASK[0] |

| ALERT_CFG.SYS_ALERT_MASK Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| SYS_APLL_LOSS_LOCK_MASK[2] | R/W | 0 | System APLL loss lock event enable mask.<br>If enabled, GPIO alert becomes active when sys_apll_loss_lock_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| DPLL_SYS_HOLDOVER_MASK[1] | R/W | 0 | System DPLL holdover transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll_sys_holdover_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |
| DPLL_SYS_LOCK_MASK[0] | R/W | 0 | System DPLL locked transition event enable mask.<br>If enabled, GPIO alert becomes active when dpll_sys_lock_state_change_sticky bit is set.<br>0 = disabled<br>1 = enabled |

## Module: SYS_DPLL_XO

Configure the system DPLL oscillator XO_DPLL frequency.

Note: The order of configuring three SCSR modules, SCSR_SYS_DPLL_XO, SCSR_SYS_APLL, SCSR_SYS_DPLL, are critical. The correct configuration order should be: SCSR_SYS_DPLL_XO, SCSR_SYS_APLL, SCSR_SYS_DPLL, and followed by other modules. Each of these three SCSR modules should be configured completely before configuring the next module.

Table 143: SYS_DPLL_XO Register Index

| Offset (Hex) | Register Module Base Address: C194h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | SYS_DPLL_XO.XO_FREQ | XO_DPLL frequency in Hz. |

### SYS_DPLL_XO.XO_FREQ

System oscillator (XO_DPLL) Frequency in Hz is M / N.

Table 144: SYS_DPLL_XO.XO_FREQ Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_XO.XO_FREQ Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | M[7:0] | | | | | | | |
| 001h | M[15:8] | | | | | | | |
| 002h | M[23:16] | | | | | | | |
| 003h | M[31:24] | | | | | | | |

Table 144: SYS_DPLL_XO.XO_FREQ Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_XO.XO_FREQ Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | M[39:32] | | | | | | | |
| 005h | M[47:40] | | | | | | | |
| 006h | N[7:0] | | | | | | | |
| 007h | N[15:8] | | | | | | | |

| SYS_DPLL_XO.XO_FREQ Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| N[15:0] | R/W | 0 | XO_DPLL frequency N.<br>N is unsigned 16-bit. A value of 0 for this field will be interpreted as 1. |
| M[47:0] | R/W | 0 | XO_DPLL frequency M.<br>M is unsigned 48-bit. |

## Module: SYS_APLL

Configure the system APLL.

Note: The order of configuring three SCSR modules, SCSR_SYS_DPLL_XO, SCSR_SYS_APLL, SCSR_SYS_DPLL, are critical. The correct configuration order should be: SCSR_SYS_DPLL_XO, SCSR_SYS_APLL, SCSR_SYS_DPLL, and followed by other modules. Each of these three SCSR modules should be configured completely before configuring the next module.

Table 145: SYS_APLL Register Index

| Offset (Hex) | Register Module Base Address: C19Ch | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | SYS_APLL.SYS_APLL_CP_SS_CURRENT_1 | System APLL charge pump current register. |
| 001h | SYS_APLL.SYS_APLL_CP_SS_CURRENT_2 | System APLL charge pump current register. |
| 002h | SYS_APLL.SYS_APLL_CFG_1 | System APLL configuration register 1. |
| 003h | SYS_APLL.SYS_APLL_CFG_2 | System APLL configuration register 2. |
| 004h | SYS_APLL.SYS_APLL_VREG_CTRL | VREG control register. |
| 005h | SYS_APLL.SYS_APLL_CP_CTRL_0 | System APLL charge pump control register. |
| 006h | SYS_APLL.SYS_APLL_CP_CTRL_1 | System APLL charge pump control register. |
| 007h | SYS_APLL.SYS_APLL_CP_CTRL_2 | System APLL charge pump control register. |
| 008h | SYS_APLL.SYS_APLL_XTAL_FREQ | System APLL crystal frequency in Hz. |
| 010h | SYS_APLL.SYS_APLL_CTRL | System APLL control register. |

### SYS_APLL.SYS_APLL_CP_SS_CURRENT_1

Set the charge pump source switching currents and enable for config.

Table 146: SYS_APLL.SYS_APLL_CP_SS_CURRENT_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_APLL.SYS_APLL_CP_SS_CURRENT_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | GLOBAL_ENABLE[7] | RESERVED[6] | CP_1_SS_CURRENT[5:3] | | | CP_2_SS_CURRENT[2:0] | | |

| SYS_APLL.SYS_APLL_CP_SS_CURRENT_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| GLOBAL_ENABLE[7] | R/W | 0 | 0 = disabled,<br>1 = enabled.<br>Write '1' to this bit to apply the SCSR charge pump settings. No changes will be applied while this bit is disabled. |
| RESERVED | N/A | - | This field must not be modified from the read value |
| CP_1_SS_CURRENT[5:3] | R/W | 0 | 0x0 = 125uA,<br>0x3 = 500uA,<br>0x7 = 1000uA.<br>Reference current for Charge Pump #1. 125uA steps. For use in 3.3V VDDA operation. cp_1_ss_current + cp_2_ss_current + cp_3_ss_current + cp_4_ss_current = total cp current used to set APLL bandwidth. |
| CP_2_SS_CURRENT[2:0] | R/W | 0 | 0x0 = 125uA,<br>0x3 = 500uA,<br>0x7 = 1000uA.<br>Reference current for Charge Pump #2. 125uA steps. For use in 3.3V VDDA operation. cp_1_ss_current + cp_2_ss_current + cp_3_ss_current + cp_4_ss_current = total cp current used to set APLL bandwidth. |

### SYS_APLL.SYS_APLL_CP_SS_CURRENT_2

Set the charge pump source switching currents .

Table 147: SYS_APLL.SYS_APLL_CP_SS_CURRENT_2 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_APLL.SYS_APLL_CP_SS_CURRENT_2 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 001h | RESERVED[7:6] | | CP_3_SS_CURRENT[5:3] | | | CP_4_SS_CURRENT[2:0] | | |

| SYS_APLL.SYS_APLL_CP_SS_CURRENT_2 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| CP_3_SS_CURRENT[5:3] | R/W | 0 | 0x0 = 125uA,<br>0x3 = 500uA,<br>0x7 = 1000uA.<br>Reference current for Charge Pump #3. 125uA steps. For use in 3.3V VDDA operation. cp_1_ss_current + cp_2_ss_current + cp_3_ss_current + cp_4_ss_current = total cp current used to set APLL bandwidth. |
| CP_4_SS_CURRENT[2:0] | R/W | 0 | 0x0 = 125uA,<br>0x3 = 500uA,<br>0x7 = 1000uA.<br>Reference current for Charge Pump #4. 125uA steps. For use in 3.3V VDDA operation. cp_1_ss_current + cp_2_ss_current + cp_3_ss_current + cp_4_ss_current = total cp current used to set APLL bandwidth. |

### SYS_APLL.SYS_APLL_CFG_1

Sets APLL configuration register 1.

Table 148: SYS_APLL.SYS_APLL_CFG_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_APLL.SYS_APLL_CFG_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | PFD_FORCE_VC_LOW_CS[7] | PFD_FORCE_VC_HIGH_CS[6] | CP_CS_OFFSET_ENABLE[5] | XTAL_DOUBLE_CS[4] | CP_CS_OTA_ENABLE[3] | CP_CS_ENABLE[2] | PFD_RESET_CS[1] | PFD_RESET_SS_1[0] |

| SYS_APLL.SYS_APLL_CFG_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PFD_FORCE_VC_LOW_CS[7] | R/W | 0 | Force control voltage to low.<br>Used only as a test condition. |
| PFD_FORCE_VC_HIGH_CS[6] | R/W | 0 | Force control voltage to high.<br>Used only as a test condition. |
| CP_CS_OFFSET_ENABLE[5] | R/W | 0 | Enable current steering offset current in 2.5V VDDA mode.<br>Only used for trim. |
| XTAL_DOUBLE_CS[4] | R/W | 0 | Double XTAL frequency for 2.5V power supply.<br>Set high if doubler is enabled. For both 2.5V and 3.3V VDDA operation. |
| CP_CS_OTA_ENABLE[3] | R/W | 0 | Enable operational transconductance amplifier (OTA) in CP.<br>1 = 2.5V VDDA operation. 0 = 3.3V VDDA operation. |
| CP_CS_ENABLE[2] | R/W | 0 | Enable current steering charge pump.<br>Must be high for 2.5V VDDA operation, low for 3.3V VDDA operation. |

| SYS_APLL.SYS_APLL_CFG_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PFD_RESET_CS[1] | R/W | 0 | Reset to 2.5V current steering PFD.<br>Reset must be high for 3.3V VDDA operation, low for 2.5V VDDA operation. |
| PFD_RESET_SS_1[0] | R/W | 0 | Reset to 3.3V source switching PFD #1.<br>Reset must be high for 2.5V VDDA operation, low for 3.3V VDDA operation. |

### SYS_APLL.SYS_APLL_CFG_2

Sets APLL configuration register 2.

Table 149: SYS_APLL.SYS_APLL_CFG_2 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_APLL.SYS_APLL_CFG_2 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 003h | RESERVED[7] | PFD_RESET_SS_2[6] | CP_CS_500U_ENABLE[5] | CP_CS_250U_ENABLE[4] | CP_CS_125U_ENABLE[3] | CP_CS_CURRENT[2:0] | | |

| SYS_APLL.SYS_APLL_CFG_2 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| PFD_RESET_SS_2[6] | R/W | 0 | Reset to 3.3V source switching PFD #2.<br>Reset must be high for 2.5V VDDA operation, low for 3.3V VDDA operation. |
| CP_CS_500U_ENABLE[5] | R/W | 0 | Enable current steering charge pump 500uA gain control.<br>Enable 500uA current source for cs charge pump. For use in 2.5V VDDA operation. |
| CP_CS_250U_ENABLE[4] | R/W | 0 | Enable current steering charge pump 250uA gain control.<br>Enable 250uA current source for cs charge pump. For use in 2.5V VDDA operation |
| CP_CS_125U_ENABLE[3] | R/W | 0 | Enable current steering charge pump 125uA gain control.<br>Enable 125uA current source for cs charge pump. For use in 2.5V VDDA operation. |
| CP_CS_CURRENT[2:0] | R/W | 0 | Control bias current for current steering charge pump.<br>Reference current for 2.5V VDDA operation. 125uA steps. 0 = 125uA, 7 = 1000uA. |

### SYS_APLL.SYS_APLL_VREG_CTRL

VREG control register.

Table 150: SYS_APLL.SYS_APLL_VREG_CTRL Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_APLL.SYS_APLL_VREG_CTRL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | RESERVED[7:1] | | | | | | | VREG_VCAL_0[0] |

| SYS_APLL.SYS_APLL_VREG_CTRL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| VREG_VCAL_0[0] | R/W | 0 | VREG volt calibration control register bit 0.<br>When "1", PDCP and VCO regulators are set for 2.5V VDDA power supply application. When "0" PDCP and VCO regulators are set for 3.3V VDDA application. |

### SYS_APLL.SYS_APLL_CP_CTRL_0

Sets the charge pump and 500uA enables for control 0.

Table 151: SYS_APLL.SYS_APLL_CP_CTRL_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_APLL.SYS_APLL_CP_CTRL_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 005h | CP_4_SS_ENABLE[7] | CP_3_SS_ENABLE[6] | CP_2_SS_ENABLE[5] | CP_1_SS_ENABLE[4] | SYS_APLL_CP_4_SS_500U_ENABLE[3] | SYS_APLL_CP_3_SS_500U_ENABLE[2] | SYS_APLL_CP_2_SS_500U_ENABLE[1] | SYS_APLL_CP_1_SS_500U_ENABLE[0] |

| SYS_APLL.SYS_APLL_CP_CTRL_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| CP_4_SS_ENABLE[7] | R/W | 0 | Enable source switching charge pump #4.<br>Must be low for 2.5V VDDA.<br>0 = disabled<br>1 = enabled. |
| CP_3_SS_ENABLE[6] | R/W | 0 | Enable source switching charge pump #3.<br>Must be low for 2.5V VDDA.<br>0 = disabled<br>1 = enabled. |

| SYS_APLL.SYS_APLL_CP_CTRL_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| CP_2_SS_ENABLE[5] | R/W | 0 | Enable source switching charge pump #2.<br>Must be low for 2.5V VDDA.<br>0 = disabled<br>1 = enabled. |
| CP_1_SS_ENABLE[4] | R/W | 0 | Enable source switching charge pump #1.<br>Must be low for 2.5V VDDA.<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_4_SS_500U_ENABLE[3] | R/W | 0 | Enable source switching 500mA gain control for Charge Pump #4.<br>For use in 3.3V VDDA operation.<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_3_SS_500U_ENABLE[2] | R/W | 0 | Enable source switching 500mA gain control for Charge Pump #3.<br>For use in 3.3V VDDA operation.<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_2_SS_500U_ENABLE[1] | R/W | 0 | Enable source switching 500mA gain control for Charge Pump #2.<br>For use in 3.3V VDDA operation.<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_1_SS_500U_ENABLE[0] | R/W | 0 | Enable source switching 500mA gain control for Charge Pump #1.<br>For use in 3.3V VDDA operation.<br>0 = disabled<br>1 = enabled. |

### SYS_APLL.SYS_APLL_CP_CTRL_1

Sets the charge pump and 500uA enables for control 1.

Table 152: SYS_APLL.SYS_APLL_CP_CTRL_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_APLL.SYS_APLL_CP_CTRL_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 006h | SYS_APLL_CP_4_SS_125U_ENABLE[7] | SYS_APLL_CP_3_SS_125U_ENABLE[6] | SYS_APLL_CP_2_SS_125U_ENABLE[5] | SYS_APLL_CP_1_SS_125U_ENABLE[4] | SYS_APLL_CP_4_SS_250U_ENABLE[3] | SYS_APLL_CP_3_SS_250U_ENABLE[2] | SYS_APLL_CP_2_SS_250U_ENABLE[1] | SYS_APLL_CP_1_SS_250U_ENABLE[0] |

| SYS_APLL.SYS_APLL_CP_CTRL_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SYS_APLL_CP_4_SS_125U_ENABLE[7] | R/W | 0 | Enable source switching 125mA gain control for Charge Pump #4.<br>For use in 3.3V VDDA operation<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_3_SS_125U_ENABLE[6] | R/W | 0 | Enable source switching 125mA gain control for Charge Pump #3.<br>For use in 3.3V VDDA operation<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_2_SS_125U_ENABLE[5] | R/W | 0 | Enable source switching 125mA gain control for Charge Pump #2.<br>For use in 3.3V VDDA operation<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_1_SS_125U_ENABLE[4] | R/W | 0 | Enable source switching 125mA gain control for Charge Pump #1.<br>For use in 3.3V VDDA operation<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_4_SS_250U_ENABLE[3] | R/W | 0 | Enable source switching 250mA gain control for Charge Pump #4.<br>For use in 3.3V VDDA operation.<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_3_SS_250U_ENABLE[2] | R/W | 0 | Enable source switching 250mA gain control for Charge Pump #3.<br>For use in 3.3V VDDA operation.<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_2_SS_250U_ENABLE[1] | R/W | 0 | Enable source switching 250mA gain control for Charge Pump #2.<br>For use in 3.3V VDDA operation.<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_1_SS_250U_ENABLE[0] | R/W | 0 | Enable source switching 250mA gain control for Charge Pump #1.<br>For use in 3.3V VDDA operation.<br>0 = disabled<br>1 = enabled. |

### SYS_APLL.SYS_APLL_CP_CTRL_2

Sets the charge pump and 500uA enables for control 2.

Table 153: SYS_APLL.SYS_APLL_CP_CTRL_2 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_APLL.SYS_APLL_CP_CTRL_2 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 007h | SYS_APLL_CP_4_SS_OTA_ENABLE[7] | SYS_APLL_CP_3_SS_OTA_ENABLE[6] | SYS_APLL_CP_2_SS_OTA_ENABLE[5] | SYS_APLL_CP_1_SS_OTA_ENABLE[4] | SYS_APLL_CP_4_SS_OFFSET_ENABLE[3] | SYS_APLL_CP_3_SS_OFFSET_ENABLE[2] | SYS_APLL_CP_2_SS_OFFSET_ENABLE[1] | SYS_APLL_CP_1_SS_OFFSET_ENABLE[0] |

| SYS_APLL.SYS_APLL_CP_CTRL_2 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SYS_APLL_CP_4_SS_OTA_ENABLE[7] | R/W | 0 | Enable source switching ota for Charge Pump #4.<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_3_SS_OTA_ENABLE[6] | R/W | 0 | Enable source switching ota for Charge Pump #3.<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_2_SS_OTA_ENABLE[5] | R/W | 0 | Enable source switching ota for Charge Pump #2.<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_1_SS_OTA_ENABLE[4] | R/W | 0 | Enable source switching ota for Charge Pump #1.<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_4_SS_OFFSET_ENABLE[3] | R/W | 0 | Enable source switching offset current for Charge Pump #4.<br>Used only for trim.<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_3_SS_OFFSET_ENABLE[2] | R/W | 0 | Enable source switching offset current for Charge Pump #3.<br>Used only for trim.<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_2_SS_OFFSET_ENABLE[1] | R/W | 0 | Enable source switching offset current for Charge Pump #2.<br>Used only for trim.<br>0 = disabled<br>1 = enabled. |
| SYS_APLL_CP_1_SS_OFFSET_ENABLE[0] | R/W | 0 | Enable source switching offset current for Charge Pump #1.<br>Used only for trim.<br>0 = disabled<br>1 = enabled. |

### SYS_APLL.SYS_APLL_XTAL_FREQ

Crystal (XTAL) Frequency in Hz M/N.

Table 154: SYS_APLL.SYS_APLL_XTAL_FREQ Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_APLL.SYS_APLL_XTAL_FREQ Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 008h | M[7:0] | | | | | | | |
| 009h | M[15:8] | | | | | | | |
| 00Ah | M[23:16] | | | | | | | |
| 00Bh | M[31:24] | | | | | | | |
| 00Ch | M[39:32] | | | | | | | |
| 00Dh | M[47:40] | | | | | | | |
| 00Eh | N[7:0] | | | | | | | |
| 00Fh | N[15:8] | | | | | | | |

| SYS_APLL.SYS_APLL_XTAL_FREQ Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| N[15:0] | R/W | 0 | SYS_APLL crystal frequency N.<br>N is unsigned 16-bit. A value of 0 for this field will be interpreted as 1. |
| M[47:0] | R/W | 0 | SYS_APLL crystal frequency M.<br>M is unsigned 48-bit. |

### SYS_APLL.SYS_APLL_CTRL

System APLL control register.

Table 155: SYS_APLL.SYS_APLL_CTRL Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_APLL.SYS_APLL_CTRL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 010h | APLL_FBDIV_DIVIDER[7:0] | | | | | | | |
| 011h | VCCA_SEL[15] | DOUBLER_ENABLE[14] | APLL_FBDIV_DIVIDER[13:8] | | | | | |

| SYS_APLL.SYS_APLL_CTRL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| VCCA_SEL[15] | R/W | 0 | VCCA selection.<br>If SYS_APLL_CP_SS_CURRENT_1.GLOBAL_ENABLE is set to "0", this field selects 2.5V or 3.3V VDDA operation with default charge pump values. If SYS_APLL_CP_SS_CURRENT_1.GLOBAL_ENABLE is set to "1", this field will be ignored and the charge pump fields can be programmed to customized values.<br>0 = 3.3 V<br>1 = 2.5 V |
| DOUBLER_ENABLE[14] | R/W | 0 | Enable the crystal input frequency doubler. Enable = 1.<br>Doubles the Input frequency of the SYS_APLL.<br>0 = disabled<br>1 = enabled |
| APLL_FBDIV_DIVIDER[13:0] | R/W | 0 | Feedback divider value.<br>Sets the divider value of the feedback divider. |

## Module: INPUT_0

Input 0 configuration.

Table 156: INPUT_0 Register Index

| Offset (Hex) | Register Module Base Address: C1B0h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | INPUT_0.IN_FREQ | Input frequency in Hz. |
| 008h | INPUT_0.IN_DIV | Input divider value. |
| 00Ah | INPUT_0.IN_PHASE | Input phase offset configuration. |
| 00Ch | INPUT_0.IN_SYNC | Frame pulse and sync pulse configuration. |
| 00Dh | INPUT_0.IN_MODE | Input configuration. |

a. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

### INPUT_0.IN_FREQ

Input frequency in Hz is M / N.

Table 157: INPUT_0.IN_FREQ Bit Field Locations and Descriptions

| Offset Address (Hex) | INPUT_0.IN_FREQ Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | M[7:0] | | | | | | | |
| 001h | M[15:8] | | | | | | | |
| 002h | M[23:16] | | | | | | | |
| 003h | M[31:24] | | | | | | | |
| 004h | M[39:32] | | | | | | | |
| 005h | M[47:40] | | | | | | | |
| 006h | N[7:0] | | | | | | | |
| 007h | N[15:8] | | | | | | | |

| INPUT_0.IN_FREQ Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| N[15:0] | R/W | 0 | Input frequency N.<br>N is unsigned 16-bit. A value of 0 for this field will be interpreted as 1. |
| M[47:0] | R/W | 0 | Input frequency M.<br>M is unsigned 48-bit.<br>In differential mode, maximum speed is 1 GHz.<br>In CMOS mode (single-ended), maximum speed is 325 MHz. |

### INPUT_0.IN_DIV

Input divider value.

Table 158: INPUT_0.IN_DIV Bit Field Locations and Descriptions

| Offset Address (Hex) | INPUT_0.IN_DIV Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 008h | IN_DIV[7:0] | | | | | | | |
| 009h | IN_DIV[15:8] | | | | | | | |

| INPUT_0.IN_DIV Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN_DIV[15:0] | R/W | 0 | Divide IN_FREQ down to send to the DPLL.<br>Unsigned 16-bit number.<br>Maximum speed for the references sent to the DPLL is 150 MHz.<br>0 and 1 both indicate bypass. |

### INPUT_0.IN_PHASE

Input phase offset configuration.

Table 159: INPUT_0.IN_PHASE Bit Field Locations and Descriptions

| Offset Address (Hex) | INPUT_0.IN_PHASE Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ah | IN_PHASE[7:0] | | | | | | | |
| 00Bh | IN_PHASE[15:8] | | | | | | | |

| INPUT_0.IN_PHASE Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN_PHASE[15:0] | R/W | 0 | Phase offset value.<br>Signed 16-bit phase offset value in ITDC_UIs. |

### INPUT_0.IN_SYNC

Specify another input to be used as the frame pulse or sync pulse for the current input.

Table 160: INPUT_0.IN_SYNC Bit Field Locations and Descriptions

| Offset Address (Hex) | INPUT_0.IN_SYNC Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ch | FRAME_SYNC_PULSE_EN[7] | FRAME_SYNC_RESAMPLE_EDGE[6] | FRAME_SYNC_RESAMPLE_EN[5] | FRAME_SYNC_PULSE[4:0] | | | | |

| INPUT_0.IN_SYNC Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FRAME_SYNC_PULSE_EN[7] | R/W | 0 | Enable or disable the frame pulse or sync pulse mode for this input.<br>Mode selection is determined by frame_sync_mode in SCSR_DPLL_CTRL_2.<br>0 = disabled<br>1 = enabled |
| FRAME_SYNC_RESAMPLE_EDGE[6] | R/W | 0 | Re-sample edge selection.<br>0 = positive edge<br>1 = negative edge |

| INPUT_0.IN_SYNC Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FRAME_SYNC_RESAMPLE_EN[5] | R/W | 0 | Re-sample enable.<br>Enabling re-sample will have the frame/sync input signal being re-sampled by the input reference clock (refclk). It can help to re-align the frame/sync with respect to the refclk.<br>Ex. If the frame/sync input is aligned to the rising edge of the refclk, it might get into the situation where it is uncertain whether the phase detector sees the frame edge before or after the refclk edge. Re-sampling the frame/sync with the falling edge of the refclk will get the frame/sync out of this situation.<br>0 = disabled<br>1 = enabled |
| FRAME_SYNC_PULSE[4:0] | R/W | 0 | Select the reference input that is a frame or sync pulse to this input.<br>Selects either the input clock or PPS from the PWM decoder.<br>Selecting itself puts the DPLL back to normal tracking mode (i.e.. not in frame/pulse mode).<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = PPS from PWM Decoder 0<br>0x11 = PPS from PWM Decoder 1<br>0x12 = PPS from PWM Decoder 2<br>0x13 = PPS from PWM Decoder 3<br>0x14 = PPS from PWM Decoder 4<br>0x15 = PPS from PWM Decoder 5<br>0x16 = PPS from PWM Decoder 6<br>0x17 = PPS from PWM Decoder 7<br>0x18 = PPS from PWM Decoder 8<br>0x19 = PPS from PWM Decoder 9<br>0x1A = PPS from PWM Decoder 10<br>0x1B = PPS from PWM Decoder 11<br>0x1C = PPS from PWM Decoder 12<br>0x1D = PPS from PWM Decoder 13<br>0x1E = PPS from PWM Decoder 14<br>0x1F = PPS from PWM Decoder 15 |

### INPUT_0.IN_MODE

Configure the electrical properties of this input and select the predefined DPLL loop filter configuration.

TRIGGER: Writing to this byte triggers a read and activation in hardware of all the bytes of the INPUT module.

Table 161: INPUT_0.IN_MODE Bit Field Locations and Descriptions

| Offset Address (Hex) | INPUT_0.IN_MODE Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Dh | DPLL_PRED [7] | MUX_GPIO_ IN[6] | IN_DIFF[5] | IN_PNMODE [4] | IN_INVERSE [3] | RESERVED[2:1] | | IN_EN[0] |

| INPUT_0.IN_MODE Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL_PRED[7] | R/W | 0 | Select predefined configuration to be applied to DPLL when this input is selected, if predefined configuration is enabled in DPLL.<br>0 = pred0<br>1 = pred1 |
| MUX_GPIO_IN[6] | R/W | 0 | Select a GPIO pin to mux into the input divider instead of the input pin.<br>Only applicable to INPUT_8-15. When set to 1, the following mapping applies:<br>GPIO0 pin -> CLK8<br>GPIO15 pin -> CLK9<br>GPIO14 pin -> CLK10<br>GPIO13 pin -> CLK11<br>GPIO12 pin -> CLK12<br>GPIO11 pin -> CLK13<br>GPIO10 pin -> CLK14<br>GPIO3 pin -> CLK15<br>Applied only on a per input module basis (e.g. setting INPUT_8_INPUT_MODE_MUX_GPIO_IN results only in the GPIO0 pin being multiplexed into input divider 8).<br>0 = clock Input<br>1 = GPIO configured as input clock |

| INPUT_0.IN_MODE Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN_DIFF[5] | R/W | 0 | Select differential input.<br>Only applicable to INPUT_0-7. INPUT_8-15 are always in single-ended mode.<br>When 0, the input pin will be single-ended:<br>CLK[7:0] -> INPUT_[7:0]<br>nCLK0 = CLK8 -> INPUT_8<br>nCLK1 = CLK9 -> INPUT_9<br>nCLK2 = CLK10 -> INPUT_10<br>nCLK3 = CLK11 -> INPUT_11<br>nCLK4 = CLK12 -> INPUT_12<br>nCLK5 = CLK13 -> INPUT_13<br>nCLK6 = CLK14 -> INPUT_14<br>nCLK7 = CLK15 -> INPUT_15<br>When set to 1, the two input pins will be paired up as the differential inputs. For INPUT_8-15, this single ended input may come from GPIO (see MUX_GPIO_IN[6]):<br>CLK/nCLK[7:0] -> INPUT_[7:0]<br>0 = single-ended<br>1 = differential |
| IN_PNMODE[4] | R/W | 0 | Select PMOS or NMOS differential mode.<br>Only applicable in differential mode.<br>0 = NMOS<br>1 = PMOS |
| IN_INVERSE[3] | R/W | 0 | Invert input.<br>0 = normal<br>1 = inverse |
| RESERVED | N/A | - | This field must not be modified from the read value |
| IN_EN[0] | R/W | 0 | Enable input.<br>0 = disabled<br>1 = enabled |

## Module: REF_MON_0

Reference monitor 0.

Table 162: REF_MON_0 Register Index

| Offset (Hex) | Register Module Base Address: C2E0h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | REF_MON_0.IN_MON_FREQ_CFG | Reference monitor frequency configuration. |
| 001h | REF_MON_0.IN_MON_FREQ_VLD_INTV | Frequency validation short interval. |
| 002h | REF_MON_0.IN_MON_TRANS_THRESHOLD | Reference clock phase transient threshold. |
| 004h | REF_MON_0.IN_MON_TRANS_PERIOD | Reference clock phase transient detection period. |

Table 162: REF_MON_0 Register Index

| Offset (Hex) | Register Module Base Address: C2E0h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 006h | REF_MON_0.IN_MON_ACT_CFG | Activity limit, qualification and disqualification timers. |
| 008h | REF_MON_0.IN_MON_LOS_TOLERANCE | Loss of signal tolerance configuration. |
| 00Ah | REF_MON_0.IN_MON_LOS_CFG | Loss of signal configuration. |
| 00Bh | REF_MON_0.IN_MON_CFG | Reference monitor configuration. |

a. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

### REF_MON_0.IN_MON_FREQ_CFG

Frequency validation interval and frequency offset limit.

Table 163: REF_MON_0.IN_MON_FREQ_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | REF_MON_0.IN_MON_FREQ_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | RESERVED[7] | VLD_INTERVAL[6:3] | | | | FREQ_OFFS_LIM[2:0] | | |

| REF_MON_0.IN_MON_FREQ_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| VLD_INTERVAL[6:3] | R/W | 0 | Frequency validation interval.<br>Frequency validation interval in seconds.<br>The long term reference monitor uses VLD_INTERVAL as the period to measure the frequency offset.<br>0 means using IN_MON_FREQ_VLD_INTV.VLD_INTERVAL_SHORT as validation measurement interval. |
| FREQ_OFFS_LIM[2:0] | R/W | 0 | Frequency offset limit enumeration.<br>VLD_INTERVAL and FREQ_OFFS_LIM define the long term reference monitor parameters.<br>IN_MON_CFG.MASK_FREQ enables/disables the long term reference monitor.<br>0 = 9.2 ppm(A), 12 ppm(R)<br>1 = 13.8 ppm(A), 18 ppm(R)<br>2 = 24.6 ppm(A), 32 ppm(R)<br>3 = 36.6 ppm(A), 47.5 ppm(R)<br>4 = 40 ppm(A), 52 ppm(R)<br>5 = 52 ppm(A), 67.5 ppm(R)<br>6 = 64 ppm(A), 83 ppm(R)<br>7 = 100 pm(A), 130 ppm(R) |

### REF_MON_0.IN_MON_FREQ_VLD_INTV

Frequency validation interval in units of 10 milliseconds.

Table 164: REF_MON_0.IN_MON_FREQ_VLD_INTV Bit Field Locations and Descriptions

| Offset Address (Hex) | REF_MON_0.IN_MON_FREQ_VLD_INTV Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 001h | VLD_INTERVAL_SHORT[7:0] | | | | | | | |

| REF_MON_0.IN_MON_FREQ_VLD_INTV Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| VLD_INTERVAL_SHORT[7:0] | R/W | 0 | Reference frequency validation short interval in units of 10 milliseconds.<br>Used as freq measurement period when IN_MON_FREQ_CFG.VLD_INTERVAL = 0.<br>0 means 5 seconds. |

### REF_MON_0.IN_MON_TRANS_THRESHOLD

Unsigned 16-bit value in nanoseconds.

Table 165: REF_MON_0.IN_MON_TRANS_THRESHOLD Bit Field Locations and Descriptions

| Offset Address (Hex) | REF_MON_0.IN_MON_TRANS_THRESHOLD Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | IN_MON_TRANS_THRESHOLD[7:0] | | | | | | | |
| 003h | IN_MON_TRANS_THRESHOLD[15:8] | | | | | | | |

| REF_MON_0.IN_MON_TRANS_THRESHOLD Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN_MON_TRANS_THRESHOLD[15:0] | R/W | 0 | Reference phase transient detection threshold in nanoseconds. |

### REF_MON_0.IN_MON_TRANS_PERIOD

Unsigned 16-bit value in units of 100 microseconds.

Table 166: REF_MON_0.IN_MON_TRANS_PERIOD Bit Field Locations and Descriptions

| Offset Address (Hex) | REF_MON_0.IN_MON_TRANS_PERIOD Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | IN_MON_TRANS_PERIOD[7:0] | | | | | | | |
| 005h | IN_MON_TRANS_PERIOD[15:8] | | | | | | | |

| REF_MON_0.IN_MON_TRANS_PERIOD Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN_MON_TRANS_PERIOD[15:0] | R/W | 0 | Reference phase transient detection period in unit of 100 microseconds. |

### REF_MON_0.IN_MON_ACT_CFG

Activity limit, qualification and disqualification timers.

Table 167: REF_MON_0.IN_MON_ACT_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | REF_MON_0.IN_MON_ACT_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 006h | RESERVED[7] | QUAL_TIMER[6:5] | | DSQUAL_TIMER[4:3] | | ACT_LIM[2:0] | | |

| REF_MON_0.IN_MON_ACT_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| QUAL_TIMER[6:5] | R/W | 0 | Reference activity qualification timer enumeration.<br>Qualification timer value = qual_timer * dsqual_timer.<br>0 = 4x<br>1 = 2x<br>2 = 8x<br>3 = 16x |
| DSQUAL_TIMER[4:3] | R/W | 0 | Reference activity disqualification timer enumeration.<br>0 = 2.5 s<br>1 = 1.25 ms<br>2 = 25 ms<br>3 = 50 ms |
| ACT_LIM[2:0] | R/W | 0 | Activity limit +/- 1000 ppm to +/- 12 ppm.<br>0 = 1000 ppm<br>1 = 260 ppm<br>2 = 130 ppm<br>3 = 83 ppm<br>4 = 65 ppm<br>5 = 52 ppm<br>6 = 18 ppm<br>7 = 12 ppm |

### REF_MON_0.IN_MON_LOS_TOLERANCE

Loss of signal tolerance configuration.

Table 168: REF_MON_0.IN_MON_LOS_TOLERANCE Bit Field Locations and Descriptions

| Offset Address (Hex) | REF_MON_0.IN_MON_LOS_TOLERANCE Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 008h | IN_MON_LOS_TOLERANCE[7:0] | | | | | | | |
| 009h | IN_MON_LOS_TOLERANCE[15:8] | | | | | | | |

| REF_MON_0.IN_MON_LOS_TOLERANCE Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| IN_MON_LOS_TOLERANCE[15:0] | R/W | 0 | LOS tolerance.<br>Unsigned 16-bit value in milliseconds.<br>0 means a reference switch is triggered immediately upon reference LOS detection.<br>Non zero value means that if the reference LOS duration is less than IN_MON_LOS_TOLERANCE, the DPLL will not trigger a reference switch. |

### REF_MON_0.IN_MON_LOS_CFG

Gap and margin configuration.

Table 169: REF_MON_0.IN_MON_LOS_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | REF_MON_0.IN_MON_LOS_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ah | RESERVED[7:3] | | | | | LOS_GAP[2:1] | | LOS_MARGIN[0] |

| REF_MON_0.IN_MON_LOS_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| LOS_GAP[2:1] | R/W | 0 | Number consecutive missing clocks to declare LOS.<br>0 means short term monitor will use LOS_MARGIN to detect LOS.<br>0 = LOS gap disabled<br>1 = 1<br>2 = 2<br>3 = 5 |
| LOS_MARGIN[0] | R/W | 0 | Configure the LOS detection margin.<br>Tight margin aims for 1% freq error.<br>Loose margin aims for 25% freq error.<br>0 = tight margin<br>1 = loose margin |

REF_MON_0.IN_MON_CFG

Reference monitor configuration.

TRIGGER: Writing to this byte triggers a read and activation in hardware of all the bytes of the REF_MON module.

-

Table 170: REF_MON_0.IN_MON_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | REF_MON_0.IN_MON_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Bh | RESERVED[7:6] | | DIV_OR_NON_DIV_CLK_SELECT[5] | TRANS_DETECTOR_EN[4] | MASK_ACTIVITY[3] | MASK_FREQ[2] | MASK_LOS[1] | EN[0] |

| REF_MON_0.IN_MON_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DIV_OR_NON_DIV_CLK_SELECT[5] | R/W | 0 | Select the divided clock or the non-divided clock as an input for the reference monitor.<br>Only applies to reference monitors 2, 3, 10 and 11.<br>0 = divided clock<br>1 = non-divided clock |
| TRANS_DETECTOR_EN[4] | R/W | 0 | Phase transient detector enable/disable.<br>0 = disabled<br>1 = enabled |
| MASK_ACTIVITY[3] | R/W | 0 | Include or exclude activity monitor from reference qualification or disqualification.<br>0 = excluded<br>1 = included |
| MASK_FREQ[2] | R/W | 0 | Include or exclude frequency offset monitor from reference qualification or disqualification.<br>0 = excluded<br>1 = included |
| MASK_LOS[1] | R/W | 0 | Include or exclude LOS from reference qualification or disqualification.<br>0 = excluded<br>1 = included |
| EN[0] | R/W | 0 | Enable or disable reference monitor.<br>When disabled and the corresponding input clock is enabled, this input is always qualified to be a reference.<br>When enabled and MASK_ACTIVITY = 0, MASK_FREQ = 0, and MASK_LOS = 0, this input is always qualified to be a reference.<br>0 = disabled<br>1 = enabled |

## Module: DPLL_0

Configures the DPLL.

Table 171: DPLL_0 Register Index

| Offset (Hex) | Register Module Base Address: C3B0h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | DPLL_0.DPLL_DCO_INC_DEC_SIZE | Configure frequency step size for GPIO increment/decrement mode. |
| 002h | DPLL_0.DPLL_CTRL_0 | Reference switching configuration and forced lock reference selection. |
| 003h | DPLL_0.DPLL_CTRL_1 | Configure other hitless switch features and DPLL feedback as a reference. |
| 004h | DPLL_0.DPLL_CTRL_2 | External feedback and frame/sync pulse configuration. |
| 005h | DPLL_0.DPLL_UPDATE_RATE_CFG | DPLL loop filter update rate configuration. |
| 006h | DPLL_0.DPLL_FILTER_STATUS_UPDATE_CFG | DPLL loop filter status update configuration. |
| 007h | DPLL_0.DPLL_HO_ADVCD_HISTORY | Advanced holdover history configuration. |
| 008h | DPLL_0.DPLL_HO_ADVCD_BW | DPLL advanced holdover bandwidth configuration. |
| 00Ah | DPLL_0.DPLL_HO_CFG | Holdover configuration. |
| 00Bh | DPLL_0.DPLL_LOCK_0 | Phase lock threshold. |
| 00Ch | DPLL_0.DPLL_LOCK_1 | Phase lock monitor duration. |
| 00Dh | DPLL_0.DPLL_LOCK_2 | Frequency lock threshold. |
| 00Eh | DPLL_0.DPLL_LOCK_3 | Frequency lock monitor duration. |
| 00Fh | DPLL_0.DPLL_REF_PRIORITY_0 | Select input for highest (0) priority. |
| 010h | DPLL_0.DPLL_REF_PRIORITY_1 | Select input for priority 1. |
| 011h | DPLL_0.DPLL_REF_PRIORITY_2 | Select input for priority 2. |
| 012h | DPLL_0.DPLL_REF_PRIORITY_3 | Select input for priority 3. |
| 013h | DPLL_0.DPLL_REF_PRIORITY_4 | Select input for priority 4. |
| 014h | DPLL_0.DPLL_REF_PRIORITY_5 | Select input for priority 5. |
| 015h | DPLL_0.DPLL_REF_PRIORITY_6 | Select input for priority 6. |
| 016h | DPLL_0.DPLL_REF_PRIORITY_7 | Select input for priority 7. |
| 017h | DPLL_0.DPLL_REF_PRIORITY_8 | Select input for priority 8. |
| 018h | DPLL_0.DPLL_REF_PRIORITY_9 | Select input for priority 9. |
| 019h | DPLL_0.DPLL_REF_PRIORITY_10 | Select input for priority 10. |
| 01Ah | DPLL_0.DPLL_REF_PRIORITY_11 | Select input for priority 11. |
| 01Bh | DPLL_0.DPLL_REF_PRIORITY_12 | Select input for priority 12. |
| 01Ch | DPLL_0.DPLL_REF_PRIORITY_13 | Select input for priority 13. |
| 01Dh | DPLL_0.DPLL_REF_PRIORITY_14 | Select input for priority 14. |
| 01Eh | DPLL_0.DPLL_REF_PRIORITY_15 | Select input for priority 15. |
| 01Fh | DPLL_0.DPLL_REF_PRIORITY_16 | Select input for priority 16. |

Table 171: DPLL_0 Register Index

| Offset (Hex) | Register Module Base Address: C3B0h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 020h | DPLL_0.DPLL_REF_PRIORITY_17 | Select input for priority 17. |
| 021h | DPLL_0.DPLL_REF_PRIORITY_18 | Select input for priority 18. |
| 022h | DPLL_0.DPLL_TRANS_CTRL | Phase transient configuration. |
| 023h | DPLL_0.DPLL_FASTLOCK_CFG_0 | Fast lock configuration. |
| 024h | DPLL_0.DPLL_FASTLOCK_CFG_1 | Fast lock configuration. |
| 025h | DPLL_0.DPLL_MAX_FREQ_OFFSET | DPLL maximum frequency offset limit. |
| 026h | DPLL_0.DPLL_FASTLOCK_PSL | Fast lock phase slope limit. |
| 028h | DPLL_0.DPLL_FASTLOCK_FSL | Fast lock frequency slope limit. |
| 02Ah | DPLL_0.DPLL_FASTLOCK_BW | Fast lock loop filter bandwidth. |
| 02Ch | DPLL_0.DPLL_WRITE_FREQ_TIMER | Write frequency timer. |
| 02Eh | DPLL_0.DPLL_WRITE_PHASE_TIMER | Write phase timer. |
| 030h | DPLL_0.DPLL_PRED_CFG | Predefined configuration selection. |
| 031h | DPLL_0.DPLL_TOD_SYNC_CFG | DPLL ToD synchronization configuration. |
| 032h | DPLL_0.DPLL_COMBO_SLAVE_CFG_0 | Combo mode slave primary source configuration. |
| 033h | DPLL_0.DPLL_COMBO_SLAVE_CFG_1 | Combo mode slave secondary source configuration. |
| 034h | DPLL_0.DPLL_SLAVE_REF_CFG | Slave mode configuration. |
| 035h | DPLL_0.DPLL_REF_MODE | Reference selection configuration. |
| 036h | DPLL_0.DPLL_PHASE_MEASUREMENT_CFG | Phase measurement mode configuration. |
| 037h | DPLL_0.DPLL_MODE | DPLL operating modes. |

a. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

### DPLL_0.DPLL_DCO_INC_DEC_SIZE

Configure frequency step size for GPIO increment/decrement mode.

Table 172: DPLL_0.DPLL_DCO_INC_DEC_SIZE Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_DCO_INC_DEC_SIZE Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | DCO_INC_DEC_SIZE[7:0] | | | | | | | |
| 001h | DCO_INC_DEC_SIZE[15:8] | | | | | | | |

| DPLL_0.DPLL_DCO_INC_DEC_SIZE Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DCO_INC_DEC_SIZE[15:0] | R/W | 0 | Size of frequency increment/decrement in 0.01 ppb.<br>Unsigned 16-bit.<br>0 means no change.<br>GPIO increment/decrement mode is by setting GPIO_n.GPIO_CTRL.GPIO_FUNCTION = 0x4 increment / 0x5 decrement.<br>The DPLL to increment/decrement is configured in GPIO_n.GPIO_DCO_INC_DEC.DPLL_INDEX. |

### DPLL_0.DPLL_CTRL_0

Enable revertive switching, hitless switching and global sync mode.

Table 173: DPLL_0.DPLL_CTRL_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_CTRL_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | FORCE_LOCK_INPUT[7:3] | | | | | GLOBAL_SYNC_EN[2] | REVERTIVE_EN[1] | HITLESS_EN[0] |

| DPLL_0.DPLL_CTRL_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FORCE_LOCK_INPUT[7:3] | R/W | 0 | DPLL reference input index when force lock applied.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input (NA in this mode)<br>0x12 = XO_DPLL<br>0x13 = fb clk of DPLL 0<br>0x14 = fb clk of DPLL 1<br>0x15 = fb clk of DPLL 2<br>0x16 = fb clk of DPLL 3<br>0x17 = fb clk of DPLL 4<br>0x18 = fb clk of DPLL 5<br>0x19 = fb clk of DPLL 6<br>0x1A = fb clk of DPLL 7<br>0x1B = fb clk of SYS DPLL. |
| GLOBAL_SYNC_EN[2] | R/W | 0 | Enable global sync trigger to synchronize multiple DPLLs.<br>When this bit is set to 1, the phase of this DPLL's outputs will be aligned with the phase of other DPLLs' outputs, whose global_sync_en bit is also set to 1. When one of the DPLLs with this bit set to 1 requires phase synchronization, all DPLLs with this bit set to 1 will perform a phase synchronization procedure.<br>0 = disabled<br>1 = enabled |
| REVERTIVE_EN[1] | R/W | 0 | Enable revertive mode.<br>0 = disabled<br>1 = enabled |
| HITLESS_EN[0] | R/W | 0 | Enable hitless switch mode.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_CTRL_1

Enable other hitless switch features and select feedback clock.

Table 174: DPLL_0.DPLL_CTRL_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_CTRL_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 003h | RESERVED[7] | RESERVED[6] | HITLESS_TYPE[5] | FB_SELECT_REF[4:1] | | | | FB_SELECT_REF_EN[0] |

| DPLL_0.DPLL_CTRL_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| HITLESS_TYPE[5] | R/W | 0 | Select hitless switch type.<br>0 = HS type 1<br>1 = HS type 2 |
| FB_SELECT_REF[4:1] | R/W | 0 | Feedback from other DPLL selected as reference for this DPLL.<br>Select other DPLL feedback to be used as reference for this DPLL. If the other DPLL is in PLL mode and not in the LOCK state, then the feedback clock as a reference is disqualified. Upon disqualification, the DPLL will enter the configured holdover mode.<br>0 = fb clk of DPLL 0<br>1 = fb clk of DPLL 1<br>2 = fb clk of DPLL 2<br>3 = fb clk of DPLL 3<br>4 = fb clk of DPLL 4<br>5 = fb clk of DPLL 5<br>6 = fb clk of DPLL 6<br>7 = fb clk of DPLL 7<br>8 = fb clk of SYS DPLL |
| FB_SELECT_REF_EN[0] | R/W | 0 | Enable selected feedback as reference.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_CTRL_2

Configure external feedback and frame or sync pulse.

Table 175: DPLL_0.DPLL_CTRL_2 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_CTRL_2 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | FRAME_SYNC_PULSE_RESYNC_EN[7] | FRAME_SYNC_MODE[6:5] | | EXT_FB_REF_SELECT[4:1] | | | | EXT_FB_EN[0] |

| DPLL_0.DPLL_CTRL_2 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FRAME_SYNC_PULSE_RESYNC_EN[7] | R/W | 0 | Enable frame pulse or sync pulse periodic re-synchronization in locked state.<br>0 = disabled<br>1 = enabled |
| FRAME_SYNC_MODE[6:5] | R/W | 0 | Select frame pulse mode or sync pulse mode.<br>0 = disabled<br>1 = frame pulse mode<br>2 = sync pulse mode |
| EXT_FB_REF_SELECT[4:1] | R/W | 0 | Index of reference input selected as feedback for this DPLL.<br>External feedback must be the same frequency as ALL input references that this DPLL locks to.<br>If INPUT_n.IN_MODE.MUX_GPIO_IN = 1, then the corresponding GPIO to input pin mapping is in effect.<br>Ex. When INPUT_0.IN_MODE.MUX_GPIO_IN = 1, then CLK8 is replaced with the signal from GPIO 0.<br>0x0 = CLK0<br>0x1 = CLK1<br>0x2 = CLK2<br>0x3 = CLK3<br>0x4 = CLK4<br>0x5 = CLK5<br>0x6 = CLK6<br>0x7 = CLK7<br>0x8 = CLK8 (GPIO 0)<br>0x9 = CLK9 (GPIO 15)<br>0xA = CLK10 (GPIO 14)<br>0xB = CLK11 (GPIO 13)<br>0xC = CLK12 (GPIO 12)<br>0xD = CLK13 (GPIO 11)<br>0xE = CLK14 (GPIO 10)<br>0xF = CLK15 (GPIO 3) |
| EXT_FB_EN[0] | R/W | 0 | Enable external feedback mode.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_UPDATE_RATE_CFG

DPLL loop filter update rate configuration.

Table 176: DPLL_0.DPLL_UPDATE_RATE_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_UPDATE_RATE_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 005h | RESERVED[7:2] | | | | | | UPDATE_RATE_CFG[1:0] | |

| DPLL_0.DPLL_UPDATE_RATE_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| UPDATE_RATE_CFG[1:0] | R/W | 0 | DPLL loop filter update rate configuration.<br>Used to avoid spurs at a specific frequency.<br>0 = 2.777 MHz<br>1 = 694 kHz<br>2 = 174 kHz<br>3 = 43 kHz |

### DPLL_0.DPLL_FILTER_STATUS_UPDATE_CFG

DPLL loop filter status update configuration.

Table 177: DPLL_0.DPLL_FILTER_STATUS_UPDATE_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_FILTER_STATUS_UPDATE_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 006h | RESERVED[7:3] | | | | | FILTER_STATUS_UPDATE_EN[2] | FILTER_STATUS_SELECT_CNFG[1:0] | |

| DPLL_0.DPLL_FILTER_STATUS_UPDATE_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| FILTER_STATUS_UPDATE_EN[2] | R/W | 0 | DPLL loop filter status SCSR update enable.<br>0 = disabled<br>1 = enabled |
| FILTER_STATUS_SELECT_CNFG[1:0] | R/W | 0 | DPLL filter status SCSR source select configuration.<br>0 = integrator<br>1 = proportional + integrator<br>2 = holdover value<br>3 = delta_frequency (final ffo incl. combo mode additions) |

### DPLL_0.DPLL_HO_ADVCD_HISTORY

Advanced holdover history configuration.

Table 178: DPLL_0.DPLL_HO_ADVCD_HISTORY Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_HO_ADVCD_HISTORY Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 007h | RESERVED[7:6] | | HISTORY[5:0] | | | | | |

| DPLL_0.DPLL_HO_ADVCD_HISTORY Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| HISTORY[5:0] | R/W | 0 | Configure DPLL holdover history. |

### DPLL_0.DPLL_HO_ADVCD_BW

DPLL advanced holdover bandwidth configuration.

Table 179: DPLL_0.DPLL_HO_ADVCD_BW Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_HO_ADVCD_BW Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 008h | DPLL_HO_ADVCD_BW[7:0] | | | | | | | |
| 009h | BW_UNIT[15:14] | | DPLL_HO_ADVCD_BW[13:8] | | | | | |

| DPLL_0.DPLL_HO_ADVCD_BW Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| BW_UNIT[15:14] | R/W | 0 | DPLL advanced holdover bandwidth unit.<br>0 = uHz<br>1 = mHz<br>2 = Hz<br>3 = kHz |
| DPLL_HO_ADVCD_BW[13:0] | R/W | 0 | Unsigned 14 bit DPLL advanced holdover bandwidth value. |

### DPLL_0.DPLL_HO_CFG

Select type of holdover to be used.

Table 180: DPLL_0.DPLL_HO_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_HO_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ah | RESERVED[7:3] | | | | | HOLDOVER_MODE[2:0] | | |

| DPLL_0.DPLL_HO_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| HOLDOVER_MODE[2:0] | R/W | 0 | Holdover type configuration.<br>simple: holds DPLL with latest integrator value<br>manual: holds DPLL with value from DPLL_CTRL_n.DPLL_MANUAL_HOLDOVER_VALUE<br>advanced: holds DPLL with value derived from filtered DPLL frequency history<br>0 = simple<br>1 = manual<br>2 = advanced |

### DPLL_0.DPLL_LOCK_0

Phase lock threshold.

Table 181: DPLL_0.DPLL_LOCK_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_LOCK_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Bh | PHASE_UNIT[7:6] | | PHASE_LOCK_MAX_ERROR[5:0] | | | | | |

| DPLL_0.DPLL_LOCK_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PHASE_UNIT[7:6] | R/W | 0 | Phase lock threshold unit.<br>0 = 1 ns<br>1 = 10 ns<br>2 = 100 ns<br>3 = 1 us |
| PHASE_LOCK_MAX_ERROR[5:0] | R/W | 0 | Phase lock threshold value.<br>If 0, then phase check is disabled. |

### DPLL_0.DPLL_LOCK_1

Phase lock monitor duration.

Table 182: DPLL_0.DPLL_LOCK_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_LOCK_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ch | PHASE_MON_DUR[7:0] | | | | | | | |

| DPLL_0.DPLL_LOCK_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PHASE_MON_DUR[7:0] | R/W | 0 | Duration of phase error monitoring before lock is declared, in seconds.<br>0 means 4000 microseconds. |

### DPLL_0.DPLL_LOCK_2

Frequency lock threshold.

Table 183: DPLL_0.DPLL_LOCK_2 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_LOCK_2 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Dh | FFO_UNIT[7:6] | | FFO_LOCK_MAX_ERROR[5:0] | | | | | |

| DPLL_0.DPLL_LOCK_2 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[7:6] | R/W | 0 | FFO error unit.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO_LOCK_MAX_ERROR [5:0] | R/W | 0 | Integer maximum FFO error for lock criteria.<br>If 0, then Fractional Frequency Offset check is disabled. |

### DPLL_0.DPLL_LOCK_3

The duration in seconds the frequency has to be locked before declaring locked.

Table 184: DPLL_0.DPLL_LOCK_3 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_LOCK_3 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Eh | FFO_MON_DUR[7:0] | | | | | | | |

| DPLL_0.DPLL_LOCK_3 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_MON_DUR[7:0] | R/W | 0 | Duration of FFO error monitoring before lock declared (seconds).<br>0 means that the frequency is declared locked immediately after FFO lock criteria is met. |

### DPLL_0.DPLL_REF_PRIORITY_0

Lowest priority index is highest priority.

Table 185: DPLL_0.DPLL_REF_PRIORITY_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Fh | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 0.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 0.<br>Enable reference priority 0 for the automatic reference selection. Gaps in the priority table are supported.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_1

Lower priority index is higher priority.

Table 186: DPLL_0.DPLL_REF_PRIORITY_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 010h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 1.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 1.<br>Enable reference priority 1 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_2

Lower priority index is higher priority.

Table 187: DPLL_0.DPLL_REF_PRIORITY_2 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_2 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 011h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_2 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 2.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 2.<br>Enable reference priority 2 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_3

Lower priority index is higher priority.

Table 188: DPLL_0.DPLL_REF_PRIORITY_3 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_3 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 012h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_3 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 3.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 3.<br>Enable reference priority 3 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_4

Lower priority index is higher priority.

Table 189: DPLL_0.DPLL_REF_PRIORITY_4 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_4 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 013h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_4 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 4.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 4.<br>Enable reference priority 4 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_5

Lower priority index is higher priority.

Table 190: DPLL_0.DPLL_REF_PRIORITY_5 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_5 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 014h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_5 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 5.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 5.<br>Enable reference priority 5 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_6

Lower priority index is higher priority.

Table 191: DPLL_0.DPLL_REF_PRIORITY_6 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_6 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 015h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_6 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 6.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 6.<br>Enable reference priority 6 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_7

Lower priority index is higher priority.

Table 192: DPLL_0.DPLL_REF_PRIORITY_7 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_7 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 016h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_7 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 7.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 7.<br>Enable reference priority 7 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_8

Lower priority index is higher priority.

Table 193: DPLL_0.DPLL_REF_PRIORITY_8 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_8 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 017h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_8 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 8.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 8.<br>Enable reference priority 8 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_9

Lower priority index is higher priority.

Table 194: DPLL_0.DPLL_REF_PRIORITY_9 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_9 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 018h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_9 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 9.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 9.<br>Enable reference priority 9 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_10

Lower priority index is higher priority.

Table 195: DPLL_0.DPLL_REF_PRIORITY_10 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_10 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 019h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_10 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 10.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 10.<br>Enable reference priority 10 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_11

Lower priority index is higher priority.

Table 196: DPLL_0.DPLL_REF_PRIORITY_11 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_11 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Ah | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_11 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 11.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 11.<br>Enable reference priority 11 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_12

Lower priority index is higher priority.

Table 197: DPLL_0.DPLL_REF_PRIORITY_12 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_12 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Bh | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_12 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 12.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 12.<br>Enable reference priority 12 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_13

Lower priority index is higher priority.

Table 198: DPLL_0.DPLL_REF_PRIORITY_13 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_13 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Ch | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_13 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 13.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 13.<br>Enable reference priority 13 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_14

Lower priority index is higher priority.

Table 199: DPLL_0.DPLL_REF_PRIORITY_14 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_14 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Dh | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_14 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 14.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 14.<br>Enable reference priority 14 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_15

Lower priority index is higher priority.

Table 200: DPLL_0.DPLL_REF_PRIORITY_15 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_15 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Eh | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_15 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 15.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 15.<br>Enable reference priority 15 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_16

Lower priority index is higher priority.

Table 201: DPLL_0.DPLL_REF_PRIORITY_16 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_16 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Fh | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_16 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 16.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 16.<br>Enable reference priority 16 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_17

Highest priority index is lowest priority.

Table 202: DPLL_0.DPLL_REF_PRIORITY_17 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_17 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 020h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_17 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 17.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 17.<br>Enable reference priority 17 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_REF_PRIORITY_18

Highest priority index is lowest priority.

Table 203: DPLL_0.DPLL_REF_PRIORITY_18 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_PRIORITY_18 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 021h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| DPLL_0.DPLL_REF_PRIORITY_18 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>This parameter creates a priority group from two or more references when set to 1, 2, or 3. A priority group number is used to specify 2 or more input references having the same priority. References within the same priority group will use non-revertive switching, regardless of the revertive_en setting. When the priority group is set to zero (default), this reference does not belong to a priority group, and normal revertive switching will occur. The priority group should be continuous in the table and will inherit the priority of the lowest priority table entry that is part of the group number. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 18.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 18.<br>Enable reference priority 18 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_TRANS_CTRL

DPLL phase transient (phase build-out) configuration.

Table 204: DPLL_0.DPLL_TRANS_CTRL Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_TRANS_CTRL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 022h | RESERVED[7:2] | | | | | | TRANS_SUPPRESS_EN[1] | TRANS_DETECT_EN[0] |

| DPLL_0.DPLL_TRANS_CTRL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| TRANS_SUPPRESS_EN[1] | R/W | 0 | Transient suppress enable.<br>0 = disabled<br>1 = enabled |
| TRANS_DETECT_EN[0] | R/W | 0 | Transient detect enable.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_FASTLOCK_CFG_0

Enable different fast lock methods.

Fast lock stages in order:

1. Frequency snap
2. Phase snap
3. Pre-fast acquisition - bandwidth is set to maximum for PRE_FAST_ACQ_TIMER duration (LOCK_ACQ only)
4. Fast acquisition - bandwidth is set to DPLL_FASTLOCK_BW until lock achieved

Table 205: DPLL_0.DPLL_FASTLOCK_CFG_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_FASTLOCK_CFG_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 023h | LOCK_REC_OL_PULL_IN_EN[7] | LOCK_REC_FAST_ACQ_EN[6] | LOCK_REC_PHASE_SNAP_EN[5] | LOCK_REC_FREQ_SNAP_EN[4] | LOCK_ACQ_OL_PULL_IN_EN[3] | LOCK_ACQ_FAST_ACQ_EN[2] | LOCK_ACQ_PHASE_SNAP_EN[1] | LOCK_ACQ_FREQ_SNAP_EN[0] |

| DPLL_0.DPLL_FASTLOCK_CFG_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| LOCK_REC_OL_PULL_IN_EN[7] | R/W | 0 | Enable open loop pull_in for LOCKREC state.<br>Use SCSR_DPLL_MAX_FREQ_OFFSET_max_ffo to control the phase pull-in rate. To enable open loop pull-in, lock_rec_phase_snap_en must also be enabled.<br>0 = disabled<br>1 = enabled |
| LOCK_REC_FAST_ACQ_EN[6] | R/W | 0 | Enable fast acquisition stage for LOCKREC state.<br>During the fast acquisition stage, the bandwidth is temporarily set to DPLL_FASTLOCK_BW to facilitate faster lock acquisition.<br>0 = disabled<br>1 = enabled |
| LOCK_REC_PHASE_SNAP_EN[5] | R/W | 0 | Enable phase snap for LOCKREC state.<br>When lock_rec_ol_pull_in_en is also enabled, instead phase snap, open loop phase pull-in will be performed.<br>0 = disabled<br>1 = enabled |
| LOCK_REC_FREQ_SNAP_EN[4] | R/W | 0 | Enable frequency snap for LOCKREC state.<br>0 = disabled<br>1 = enabled |
| LOCK_ACQ_OL_PULL_IN_EN[3] | R/W | 0 | Enable open loop pull_in for LOCKACQ state.<br>Use SCSR_DPLL_MAX_FREQ_OFFSET_max_ffo to control the phase pull-in rate. To enable open loop pull-in, lock_acq_phase_snap_en must also be enabled.<br>0 = disabled<br>1 = enabled |
| LOCK_ACQ_FAST_ACQ_EN[2] | R/W | 0 | Enable fast acquisition stage for LOCKACQ state.<br>During the fast acquisition stage, the bandwidth is temporarily set to DPLL_FASTLOCK_BW to facilitate faster lock acquisition.<br>0 = disabled<br>1 = enabled |
| LOCK_ACQ_PHASE_SNAP_EN[1] | R/W | 0 | Enable phase snap for LOCKACQ state.<br>When lock_acq_ol_pull_in_en is also enabled, instead phase snap, open loop phase pull-in will be performed.<br>0 = disabled<br>1 = enabled |
| LOCK_ACQ_FREQ_SNAP_EN[0] | R/W | 0 | Enable frequency snap for LOCKACQ state.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_FASTLOCK_CFG_1

Configure pre fast acquisition timer, damping factor.

Table 206: DPLL_0.DPLL_FASTLOCK_CFG_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_FASTLOCK_CFG_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 024h | PRE_FAST_ACQ_TIMER[7:4] | | | | DAMP_FTR[3:0] | | | |

| DPLL_0.DPLL_FASTLOCK_CFG_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRE_FAST_ACQ_TIMER[7:4] | R/W | 0 | Pre-fast acquisition stage timer.<br>If the value n > 0, the DPLL opens up the bandwidth to the maximum for a duration of 2^(n-1) milliseconds.<br>If the value n = 0, then pre-fast-acquisition stage is disabled.<br>Only applied to LOCKACQ state. |
| DAMP_FTR[3:0] | R/W | 0 | DPLL damping factor for fast acquisition stage.<br>0 = 1.002, 0.02 dB, overdamp;<br>1 = 1.006, 0.05 dB, < 0.05dB;<br>2 = 1.008, 0.07 dB, < 1%;<br>3 = 1.012, 0.10 dB, < 0.1dB;<br>4 = 1.015 , 0.13 dB, < 2%;<br>5 = 1.022, 0.19 dB, < 0.2dB;<br>6 = 1.053 , 0.45 dB, < 0.5dB;<br>7 = 1.172 , 1.38 dB, underdamp; |

### DPLL_0.DPLL_MAX_FREQ_OFFSET

DPLL maximum frequency offset limit

Table 207: DPLL_0.DPLL_MAX_FREQ_OFFSET Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_MAX_FREQ_OFFSET Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 025h | MAX_FFO[7:0] | | | | | | | |

| DPLL_0.DPLL_MAX_FREQ_OFFSET Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| MAX_FFO[7:0] | R/W | 0 | Unsigned 8-bit maximum frequency offset limit in ppm.<br>Value 0 implies maximum of FFO limit of 244 ppm. |

### DPLL_0.DPLL_FASTLOCK_PSL

Fast lock phase slope limit.

Table 208: DPLL_0.DPLL_FASTLOCK_PSL Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_FASTLOCK_PSL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 026h | DPLL_FASTLOCK_PSL[7:0] | | | | | | | |
| 027h | DPLL_FASTLOCK_PSL[15:8] | | | | | | | |

| DPLL_0.DPLL_FASTLOCK_PSL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL_FASTLOCK_PSL[15:0] | R/W | 0 | Unsigned 16-bit phase slope limit in ns/s.<br>Value 0 implies no phase slope limit. Applied on both fast-acq and pre-fast acquisition stages. |

### DPLL_0.DPLL_FASTLOCK_FSL

Fast lock frequency slope limit.

Table 209: DPLL_0.DPLL_FASTLOCK_FSL Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_FASTLOCK_FSL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 028h | DPLL_FASTLOCK_FSL[7:0] | | | | | | | |
| 029h | DPLL_FASTLOCK_FSL[15:8] | | | | | | | |

| DPLL_0.DPLL_FASTLOCK_FSL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL_FASTLOCK_FSL[15:0] | R/W | 0 | Unsigned 16-bit frequency slope limit in ppb/s.<br>Value 0 implies no frequency slope limit. Applied only on frequency snap. |

### DPLL_0.DPLL_FASTLOCK_BW

Fast lock loop filter bandwidth.

Table 210: DPLL_0.DPLL_FASTLOCK_BW Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_FASTLOCK_BW Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 02Ah | DPLL_FASTLOCK_BW[7:0] | | | | | | | |
| 02Bh | BW_UNIT[15:14] | | DPLL_FASTLOCK_BW[13:8] | | | | | |

| DPLL_0.DPLL_FASTLOCK_BW Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| BW_UNIT[15:14] | R/W | 0 | Fast lock DPLL bandwidth unit.<br>0 = uHz<br>1 = mHz<br>2 = Hz<br>3 = kHz |
| DPLL_FASTLOCK_BW[13:0] | R/W | 0 | Unsigned 14-bit DPLL bandwidth value.<br>Applied only on fast acquisition stage. |

### DPLL_0.DPLL_WRITE_FREQ_TIMER

Write frequency timer.

Table 211: DPLL_0.DPLL_WRITE_FREQ_TIMER Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_WRITE_FREQ_TIMER Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 02Ch | WRITE_FREQ_TIMEOUT_CNFG[7:0] | | | | | | | |
| 02Dh | WRITE_FREQ_TIMEOUT_CNFG[15:8] | | | | | | | |

| DPLL_0.DPLL_WRITE_FREQ_TIMER Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| WRITE_FREQ_TIMEOUT_CNFG[15:0] | R/W | 0 | Unsigned 16-bit write frequency timeout value in milliseconds.<br>When in write frequency mode, the DPLL_WR_FREQ must be periodically written to within WRITE_FREQ_TIMEOUT_CNFG ms.<br>If the write frequency timer expires, the write frequency as a reference is disqualified. Upon disqualification, depending on the configuration, a reference switch may occur the DPLL may enter the configured holdover mode.<br>Value 0 implies no timeout. |

### DPLL_0.DPLL_WRITE_PHASE_TIMER

Write phase timer.

Table 212: DPLL_0.DPLL_WRITE_PHASE_TIMER Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_WRITE_PHASE_TIMER Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 02Eh | WRITE_PHASE_TIMEOUT_CNFG[7:0] | | | | | | | |
| 02Fh | WRITE_PHASE_TIMEOUT_CNFG[15:8] | | | | | | | |

| DPLL_0.DPLL_WRITE_PHASE_TIMER Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| WRITE_PHASE_TIMEOUT_CNFG[15:0] | R/W | 0 | Unsigned 16-bit write phase timeout value in milliseconds.<br>When in write phase mode, the DPLL_WRITE_PH must be periodically written to within WRITE_PHASE_TIMEOUT_CNFG ms.<br>If the write phase timer expires, the write phase as a reference is disqualified. Upon disqualification, depending on the configuration, a reference switch may occur the DPLL may enter the configured holdover mode.<br>Value 0 implies no timeout. |

### DPLL_0.DPLL_PRED_CFG

Predefined configuration selection.

Table 213: DPLL_0.DPLL_PRED_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_PRED_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 030h | RESERVED[7:2] | | | | | | WP_PRED[1] | PRED_EN[0] |

| DPLL_0.DPLL_PRED_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| WP_PRED[1] | R/W | 0 | Predefined configuration to be used for write phase input.<br>Write phase predefined configuration selection (0 or 1).<br>0 = pred0<br>1 = pred1 |
| PRED_EN[0] | R/W | 0 | Enable predefined configurations.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_TOD_SYNC_CFG

DPLL ToD synchronization configuration.

Table 214: DPLL_0.DPLL_TOD_SYNC_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_TOD_SYNC_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 031h | RESERVED[7:3] | | | | | TOD_SYNC_SOURCE[2:1] | | TOD_SYNC_EN[0] |

| DPLL_0.DPLL_TOD_SYNC_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| TOD_SYNC_SOURCE[2:1] | R/W | 0 | The ToD synchronization source.<br>The ToD index this DPLL synchronize to.<br>0 = ToD0<br>1 = ToD1<br>2 = ToD2<br>3 = ToD3 |
| TOD_SYNC_EN[0] | R/W | 0 | Enable the DPLL synchronizing to a ToD.<br>If enabled, when the source TOD write event happens, a phase snap on this DPLL will be triggered and the phase of the DPLL output will align with the ToD second boundary.<br>0 = disabled<br>1 = enabled |

### DPLL_0.DPLL_COMBO_SLAVE_CFG_0

Combo mode slave primary source configuration.

Table 215: DPLL_0.DPLL_COMBO_SLAVE_CFG_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_COMBO_SLAVE_CFG_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 032h | RESERVED[7:6] | | PRI_COMBO_SRC_EN[5] | PRI_COMBO_SRC_FILTERED_CNFG[4] | PRI_COMBO_SRC_ID[3:0] | | | |

| DPLL_0.DPLL_COMBO_SLAVE_CFG_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| PRI_COMBO_SRC_EN[5] | R/W | 0 | Enable this source.<br>0 = disabled<br>1 = enabled |
| PRI_COMBO_SRC_FILTERED_CNFG[4] | R/W | 0 | Use filtered source.<br>0 = use un-filtered source<br>1 = use filtered source |
| PRI_COMBO_SRC_ID[3:0] | R/W | 0 | Primary combo source DPLL index. |

### DPLL_0.DPLL_COMBO_SLAVE_CFG_1

Combo mode slave secondary source configuration.

Table 216: DPLL_0.DPLL_COMBO_SLAVE_CFG_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_COMBO_SLAVE_CFG_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 033h | RESERVED[7:6] | | SEC_COMBO_SRC_EN[5] | SEC_COMBO_SRC_FILTERED_CNFG[4] | SEC_COMBO_SRC_ID[3:0] | | | |

| DPLL_0.DPLL_COMBO_SLAVE_CFG_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| SEC_COMBO_SRC_EN[5] | R/W | 0 | Enable this source.<br>0 = disabled<br>1 = enabled |
| SEC_COMBO_SRC_FILTERED_CNFG[4] | R/W | 0 | Use filtered source.<br>0 = use un-filtered source<br>1 = use filtered source |
| SEC_COMBO_SRC_ID[3:0] | R/W | 0 | Secondary combo source DPLL index. |

### DPLL_0.DPLL_SLAVE_REF_CFG

Slave mode configuration.

Table 217: DPLL_0.DPLL_SLAVE_REF_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_SLAVE_REF_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 034h | RESERVED[7:5] | | | SLAVE_REFERENCE[4:0] | | | | |

| DPLL_0.DPLL_SLAVE_REF_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| SLAVE_REFERENCE[4:0] | R/W | 0 | Reference index used by DPLL when reference mode is 'slave' or 'GPIO_slave'.<br>0x0 = CLK0<br>0x1 = CLK1<br>0x2 = CLK2<br>0x3 = CLK3<br>0x4 = CLK4<br>0x5 = CLK5<br>0x6 = CLK6<br>0x7 = CLK7<br>0x8 = CLK8<br>0x9 = CLK9<br>0xA = CLK10<br>0xB = CLK11<br>0xC = CLK12<br>0xD = CLK13<br>0xE = CLK14<br>0xF = CLK15 |

### DPLL_0.DPLL_REF_MODE

Reference selection configuration.

Table 218: DPLL_0.DPLL_REF_MODE Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_REF_MODE Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 035h | RESERVED[7:4] | | | | MODE[3:0] | | | |

| DPLL_0.DPLL_REF_MODE Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| MODE[3:0] | R/W | 0 | Reference selection mode.<br>Automatic: DPLL_0.DPLL_REF_PRIORITY_[0:16]<br>Manual: DPLL_CTRL_0.DPLL_MANU_REF_CFG.MANUAL_REFERENCE<br>GPIO: GPIO_0.GPIO_MAN_CLK_SEL_0/1/2, GPIO_FUNCTION = 0x7 manual clock select<br>Slave: DPLL_0.DPLL_SLAVE_REF_CFG<br>GPIO_slave: DPLL_0.DPLL_SLAVE_REF_CFG, GPIO_FUNCTION = 0xC master/slave signal<br>0 = automatic<br>1 = manual<br>2 = GPIO<br>3 = slave<br>4 = GPIO_slave |

### DPLL_0.DPLL_PHASE_MEASUREMENT_CFG

Measure phase offset between two inputs using phase detector. Both single-ended and differential inputs are available for selection.

Coarse phase measurement or unfiltered reading (in ITDC_UI) is stored in DPLLx_PHASE_STATUS and is represented by 36-bit signed integer. Fine phase measurement or filtered reading (in ITDC_UI/128) is stored in DPLLx_FILTER_STATUS and is represented by 48-bit signed integer.

After selecting inputs, configure DPLL for phase measurement mode (i.e. set DPLL_MODE.pll_mode to 0x5).

If there is LOS condition present on either inputs selected, then said status registers will report error codes: DPLLx_PHASE_STATUS will report 0x7fffffffff value and DPLLx_FILTER_STATUS will report 0x7fffffffffff value.

Set INPUT_TDC_FBD_CTRL.fbd_integer_mode_en field to 0 to enable write frequency capability. Note that doing this will disable fine phase measurements. To stop supporting write frequency capability and start supporting fine phase measurements again, set said field to 1, retrigger INPUT_TDC module (i.e. write to INPUT_TDC_CTRL), and then retrigger DPLL module (i.e. write to DPLL_MODE).

Note: In cases where phase detector factors in one or more periods into phase measurement (e.g. when feedback clock drifts and phase detector takes one or more cycles to calculate phase offset), retrigger DPLL module (i.e. write to DPLL_MODE) to restart phase measurement.

Table 219: DPLL_0.DPLL_PHASE_MEASUREMENT_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_PHASE_MEASUREMENT_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 036h | PFD_FB_CLK_SEL[7:4] | | | | PFD_REF_CLK_SEL[3:0] | | | |

| DPLL_0.DPLL_PHASE_MEASUREMENT_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PFD_FB_CLK_SEL[7:4] | R/W | 0 | Select feedback clock going into phase detector.<br>Feedback clock selected must have same frequency as reference clock selected.<br>0x0 = CLK0<br>0x1 = CLK1<br>0x2 = CLK2<br>0x3 = CLK3<br>0x4 = CLK4<br>0x5 = CLK5<br>0x6 = CLK6<br>0x7 = CLK7<br>0x8 = CLK8<br>0x9 = CLK9<br>0xA = CLK10<br>0xB = CLK11<br>0xC = CLK12<br>0xD = CLK13<br>0xE = CLK14<br>0xF = CLK15 |
| PFD_REF_CLK_SEL[3:0] | R/W | 0 | Select reference clock going into phase detector.<br>Reference clock selected must have same frequency as feedback clock selected.<br>0x0 = CLK0<br>0x1 = CLK1<br>0x2 = CLK2<br>0x3 = CLK3<br>0x4 = CLK4<br>0x5 = CLK5<br>0x6 = CLK6<br>0x7 = CLK7<br>0x8 = CLK8<br>0x9 = CLK9<br>0xA = CLK10<br>0xB = CLK11<br>0xC = CLK12<br>0xD = CLK13<br>0xE = CLK14<br>0xF = CLK15 |

### DPLL_0.DPLL_MODE

Select state machine transition mode and DPLL operation mode.

TRIGGER: Writing to this byte triggers a read and activation in hardware of all the bytes of the DPLL module.

-

Table 220: DPLL_0.DPLL_MODE Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_0.DPLL_MODE Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 037h | RESERVED[7] | WRITE_TIMER_MODE[6] | PLL_MODE[5:3] | | | STATE_MODE[2:0] | | |

| DPLL_0.DPLL_MODE Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| WRITE_TIMER_MODE[6] | R/W | 0 | Write phase or write frequency timer mode.<br>This bit selects simple holdover or advanced holdover for DPLL once the write timer expires.<br>0 = simple holdover mode<br>1 = advanced holdover mode |
| PLL_MODE[5:3] | R/W | 0 | DPLL operation mode.<br>When switching from disabled mode to one of the other modes, appropriate trigger registers must be written to activate pertinent DPLL and output related SCSRs configurations.<br>0 = PLL mode<br>1 = write phase mode<br>2 = write frequency mode<br>3 = GPIO inc/dec mode<br>4 = synthesizer mode<br>5 = phase measurement mode<br>6 = disabled mode (reduced phase noise) |
| STATE_MODE[2:0] | R/W | 0 | DPLL state machine transition mode.<br>0 = automatic<br>1 = force lock<br>2 = force freerun<br>3 = force holdover |

## Module: SYS_DPLL

Configure the system DPLL.

Note: The order of configuring three SCSR modules, SCSR_SYS_DPLL_XO, SCSR_SYS_APLL, SCSR_SYS_DPLL, are critical. The correct configuration order should be: SCSR_SYS_DPLL_XO, SCSR_SYS_APLL, SCSR_SYS_DPLL, and followed by other modules. Each of these three SCSR modules should be configured completely before configuring the next module.

Table 221: SYS_DPLL Register Index

| Offset (Hex) | Register Module Base Address: C5B8h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | SYS_DPLL.SYS_DPLL_CTRL_0 | Reference switching configuration and forced lock reference selection. |
| 001h | SYS_DPLL.SYS_DPLL_UPDATE_RATE_CFG | System DPLL loop filter update rate configuration. |
| 002h | SYS_DPLL.SYS_DPLL_FILTER_STATUS_UPDATE_CFG | System DPLL loop filter status update configuration. |
| 003h | SYS_DPLL.SYS_DPLL_LOCK_0 | Phase lock threshold. |
| 004h | SYS_DPLL.SYS_DPLL_LOCK_1 | Phase lock monitor duration. |
| 005h | SYS_DPLL.SYS_DPLL_LOCK_2 | Frequency lock threshold. |
| 006h | SYS_DPLL.SYS_DPLL_LOCK_3 | Frequency lock monitor duration. |
| 007h | SYS_DPLL.SYS_DPLL_REF_PRIORITY_0 | Select input for highest (0) priority. |
| 008h | SYS_DPLL.SYS_DPLL_REF_PRIORITY_1 | Select input for priority 1. |
| 009h | SYS_DPLL.SYS_DPLL_REF_PRIORITY_2 | Select input for priority 2. |
| 00Ah | SYS_DPLL.SYS_DPLL_REF_PRIORITY_3 | Select input for priority 3. |
| 00Bh | SYS_DPLL.SYS_DPLL_REF_PRIORITY_4 | Select input for priority 4. |
| 00Ch | SYS_DPLL.SYS_DPLL_REF_PRIORITY_5 | Select input for priority 5. |
| 00Dh | SYS_DPLL.SYS_DPLL_REF_PRIORITY_6 | Select input for priority 6. |
| 00Eh | SYS_DPLL.SYS_DPLL_REF_PRIORITY_7 | Select input for priority 7. |
| 00Fh | SYS_DPLL.SYS_DPLL_REF_PRIORITY_8 | Select input for priority 8. |
| 010h | SYS_DPLL.SYS_DPLL_REF_PRIORITY_9 | Select input for priority 9. |
| 011h | SYS_DPLL.SYS_DPLL_REF_PRIORITY_10 | Select input for priority 10. |
| 012h | SYS_DPLL.SYS_DPLL_REF_PRIORITY_11 | Select input for priority 11. |
| 013h | SYS_DPLL.SYS_DPLL_REF_PRIORITY_12 | Select input for priority 12. |
| 014h | SYS_DPLL.SYS_DPLL_REF_PRIORITY_13 | Select input for priority 13. |
| 015h | SYS_DPLL.SYS_DPLL_REF_PRIORITY_14 | Select input for priority 14. |
| 016h | SYS_DPLL.SYS_DPLL_REF_PRIORITY_15 | Select input for priority 15. |
| 017h | SYS_DPLL.SYS_DPLL_REF_PRIORITY_16 | Select input for priority 16. |
| 018h | SYS_DPLL.SYS_DPLL_REF_PRIORITY_17 | Select input for priority 17. |
| 019h | SYS_DPLL.SYS_DPLL_REF_PRIORITY_18 | Select input for priority 18. |
| 01Ah | RESERVED | This register must not be modified from the read value |
| 01Bh | SYS_DPLL.SYS_DPLL_REF_MODE | Reference selection configuration. |
| 01Ch | SYS_DPLL.SYS_DPLL_MODE | System DPLL state machine transition mode. |

### SYS_DPLL.SYS_DPLL_CTRL_0

Reference switching configuration and forced lock reference selection.

Table 222: SYS_DPLL.SYS_DPLL_CTRL_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_CTRL_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | FORCE_LOCK_INPUT[7:3] | | | | | RESERVED[2] | REVERTIVE_EN[1] | RESERVED[0] |

| SYS_DPLL.SYS_DPLL_CTRL_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FORCE_LOCK_INPUT[7:3] | R/W | 0 | System DPLL reference input index when force lock applied.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL. |
| REVERTIVE_EN[1] | R/W | 0 | Enable revertive mode.<br>0 = disabled<br>1 = enabled |
| RESERVED | N/A | - | This field must not be modified from the read value |

### SYS_DPLL.SYS_DPLL_UPDATE_RATE_CFG

System DPLL loop filter update rate configuration.

Table 223: SYS_DPLL.SYS_DPLL_UPDATE_RATE_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_UPDATE_RATE_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 001h | RESERVED[7:2] | | | | | | UPDATE_RATE_CFG[1:0] | |

| SYS_DPLL.SYS_DPLL_UPDATE_RATE_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| UPDATE_RATE_CFG[1:0] | R/W | 0 | System DPLL loop filter update rate configuration.<br>Used to avoid spurs at a specific frequency.<br>0 = 2.777 MHz<br>1 = 694 kHz<br>2 = 174 kHz<br>3 = 43 kHz |

### SYS_DPLL.SYS_DPLL_FILTER_STATUS_UPDATE_CFG

System DPLL loop filter status update configuration.

Table 224: SYS_DPLL.SYS_DPLL_FILTER_STATUS_UPDATE_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_FILTER_STATUS_UPDATE_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | RESERVED[7:3] | | | | | FILTER_STATUS_UPDATE_EN[2] | FILTER_STATUS_SELECT_CNFG[1:0] | |

| SYS_DPLL.SYS_DPLL_FILTER_STATUS_UPDATE_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| FILTER_STATUS_UPDATE_EN[2] | R/W | 0 | System DPLL loop filter status SCSR update enable.<br>0 = disabled<br>1 = enabled |
| FILTER_STATUS_SELECT_CNFG[1:0] | R/W | 0 | System DPLL filter status SCSR source select configuration.<br>0 = integrator<br>1 = proportional + integrator<br>2 = holdover value<br>3 = delta_frequency (final ffo incl. combo mode additions) |

### SYS_DPLL.SYS_DPLL_LOCK_0

Phase lock threshold.

Table 225: SYS_DPLL.SYS_DPLL_LOCK_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_LOCK_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 003h | PHASE_UNIT[7:6] | | PHASE_LOCK_MAX_ERROR[5:0] | | | | | |

| SYS_DPLL.SYS_DPLL_LOCK_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PHASE_UNIT[7:6] | R/W | 0 | Phase lock threshold unit.<br>0 = 1 ns<br>1 = 10 ns<br>2 = 100 ns<br>3 = 1 us |
| PHASE_LOCK_MAX_ERROR[5:0] | R/W | 0 | Phase lock threshold value.<br>If 0, then Fractional Frequency Offset check is disabled. |

### SYS_DPLL.SYS_DPLL_LOCK_1

Phase lock monitor duration.

Table 226: SYS_DPLL.SYS_DPLL_LOCK_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_LOCK_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | PHASE_MON_DUR[7:0] | | | | | | | |

| SYS_DPLL.SYS_DPLL_LOCK_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PHASE_MON_DUR[7:0] | R/W | 0 | Duration of phase error monitoring before lock is declared, in seconds.<br>0 means 4000 microseconds. |

### SYS_DPLL.SYS_DPLL_LOCK_2

Frequency lock threshold.

Table 227: SYS_DPLL.SYS_DPLL_LOCK_2 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_LOCK_2 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 005h | FFO_UNIT[7:6] | | FFO_LOCK_MAX_ERROR[5:0] | | | | | |

| SYS_DPLL.SYS_DPLL_LOCK_2 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_UNIT[7:6] | R/W | 0 | FFO error unit.<br>0 = 1 ppb<br>1 = 10 ppb<br>2 = 100 ppb<br>3 = 1 ppm |
| FFO_LOCK_MAX_ERROR [5:0] | R/W | 0 | Integer maximum FFO error for lock criteria.<br>If 0, then Fractional Frequency Offset check is disabled. |

### SYS_DPLL.SYS_DPLL_LOCK_3

The duration in seconds the frequency has to be locked before declaring locked.

Table 228: SYS_DPLL.SYS_DPLL_LOCK_3 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_LOCK_3 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 006h | FFO_MON_DUR[7:0] | | | | | | | |

| SYS_DPLL.SYS_DPLL_LOCK_3 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FFO_MON_DUR[7:0] | R/W | 0 | Duration of FFO error monitoring before lock declared (seconds).<br>0 means that the frequency is declared locked immediately after FFO lock criteria is met. |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_0

Lowest priority index is highest priority.

Table 229: SYS_DPLL.SYS_DPLL_REF_PRIORITY_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 007h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>Used to group multiple clocks as equal priority.<br>References in the same priority group number use non-revertive switching. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 0.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 0.<br>Enable reference priority 0 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_1

Lower priority index is higher priority.

Table 230: SYS_DPLL.SYS_DPLL_REF_PRIORITY_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 008h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 1.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 1.<br>Enable reference priority 1 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_2

Lower priority index is higher priority.

Table 231: SYS_DPLL.SYS_DPLL_REF_PRIORITY_2 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_2 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 009h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_2 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 2.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 2.<br>Enable reference priority 2 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_3

Lower priority index is higher priority.

Table 232: SYS_DPLL.SYS_DPLL_REF_PRIORITY_3 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_3 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ah | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_3 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 3.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 3.<br>Enable reference priority 3 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_4

Lower priority index is higher priority.

Table 233: SYS_DPLL.SYS_DPLL_REF_PRIORITY_4 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_4 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Bh | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_4 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 4.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 4.<br>Enable reference priority 4 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_5

Lower priority index is higher priority.

Table 234: SYS_DPLL.SYS_DPLL_REF_PRIORITY_5 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_5 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ch | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_5 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 5.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 5.<br>Enable reference priority 5 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_6

Lower priority index is higher priority.

Table 235: SYS_DPLL.SYS_DPLL_REF_PRIORITY_6 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_6 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Dh | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_6 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 6.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 6.<br>Enable reference priority 6 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_7

Lower priority index is higher priority.

Table 236: SYS_DPLL.SYS_DPLL_REF_PRIORITY_7 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_7 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Eh | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_7 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 7.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 7.<br>Enable reference priority 7 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_8

Lower priority index is higher priority.

Table 237: SYS_DPLL.SYS_DPLL_REF_PRIORITY_8 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_8 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Fh | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_8 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 8.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 8.<br>Enable reference priority 8 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_9

Lower priority index is higher priority.

Table 238: SYS_DPLL.SYS_DPLL_REF_PRIORITY_9 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_9 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 010h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_9 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 9.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 9.<br>Enable reference priority 9 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_10

Lower priority index is higher priority.

Table 239: SYS_DPLL.SYS_DPLL_REF_PRIORITY_10 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_10 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 011h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_10 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 10.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 10.<br>Enable reference priority 10 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_11

Lower priority index is higher priority.

Table 240: SYS_DPLL.SYS_DPLL_REF_PRIORITY_11 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_11 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 012h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_11 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 11.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 11.<br>Enable reference priority 11 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_12

Lower priority index is higher priority.

Table 241: SYS_DPLL.SYS_DPLL_REF_PRIORITY_12 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_12 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 013h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_12 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 12.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 12.<br>Enable reference priority 12 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_13

Lower priority index is higher priority.

Table 242: SYS_DPLL.SYS_DPLL_REF_PRIORITY_13 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_13 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 014h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_13 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 13.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 13.<br>Enable reference priority 13 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_14

Lower priority index is higher priority.

Table 243: SYS_DPLL.SYS_DPLL_REF_PRIORITY_14 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_14 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 015h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_14 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 14.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 14.<br>Enable reference priority 14 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_15

Lower priority index is higher priority.

Table 244: SYS_DPLL.SYS_DPLL_REF_PRIORITY_15 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_15 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 016h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_15 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 15.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 15.<br>Enable reference priority 15 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_16

Lower priority index is higher priority.

Table 245: SYS_DPLL.SYS_DPLL_REF_PRIORITY_16 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_16 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 017h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_16 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 16.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 16.<br>Enable reference priority 16 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_17

Lower priority index is higher priority.

Table 246: SYS_DPLL.SYS_DPLL_REF_PRIORITY_17 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_17 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 018h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_17 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 17.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 17.<br>Enable reference priority 17 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_PRIORITY_18

Lower priority index is higher priority.

Table 247: SYS_DPLL.SYS_DPLL_REF_PRIORITY_18 Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_PRIORITY_18 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 019h | PRIORITY_GROUP_NUMBER[7:6] | | PRIORITY_REF[5:1] | | | | | PRIORITY_EN[0] |

| SYS_DPLL.SYS_DPLL_REF_PRIORITY_18 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PRIORITY_GROUP_NUMBER[7:6] | R/W | 0 | Priority group number.<br>For references in the same priority group, revertive switching is disabled. |
| PRIORITY_REF[5:1] | R/W | 0 | Input reference index for priority 18.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x12 = XO_DPLL |
| PRIORITY_EN[0] | R/W | 0 | Enable reference priority 18.<br>Enable reference priority 18 for the automatic reference selection.<br>0 = disabled<br>1 = enabled |

### SYS_DPLL.SYS_DPLL_REF_MODE

Reference selection configuration.

Table 248: SYS_DPLL.SYS_DPLL_REF_MODE Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_REF_MODE Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Bh | RESERVED[7:4] | | | | MODE[3:0] | | | |

| SYS_DPLL.SYS_DPLL_REF_MODE Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| MODE[3:0] | R/W | 0 | Reference selection mode.<br>Automatic: SYS_DPLL_0.DPLL_REF_PRIORITY_[0:16]<br>Manual: SYS_DPLL_MANU_REF_CFG.MANUAL_REFERENCE<br>0 = automatic<br>1 = manual |

### SYS_DPLL.SYS_DPLL_MODE

Select state machine transition mode.

TRIGGER: Writing to this byte triggers a read and activation in hardware of all the bytes of the system DPLL module.

-

Table 249: SYS_DPLL.SYS_DPLL_MODE Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL.SYS_DPLL_MODE Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Ch | RESERVED[7:6] | | RESERVED[5:3] | | | STATE_MODE[2:0] | | |

| SYS_DPLL.SYS_DPLL_MODE Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| STATE_MODE[2:0] | R/W | 0 | System DPLL state machine transition mode.<br>0 = automatic<br>1 = force lock<br>2 = force freerun<br>3 = force holdover |

## Module: DPLL_CTRL_0

TRIGGER: Every register in this module is a trigger register. In the case of a multibyte register the highest address register byte is the trigger byte.

Table 250: DPLL_CTRL_0 Register Index

| Offset (Hex) | Register Module Base Address: C600h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | DPLL_CTRL_0.DPLL_HS_TIE_RESET | Reset hitless switching time interval error. |
| 001h | DPLL_CTRL_0.DPLL_MANU_REF_CFG | Manual reference mode configuration. |
| 002h | DPLL_CTRL_0.DPLL_DAMPING | DPLL loop filter damping factor. |
| 003h | DPLL_CTRL_0.DPLL_DECIMATOR_BW_MULT | DPLL loop filter decimator bandwidth multiplier. |
| 004h | DPLL_CTRL_0.DPLL_BW | DPLL loop filter bandwidth. |
| 006h | DPLL_CTRL_0.DPLL_PSL | DPLL loop filter phase slope limit. |
| 008h | DPLL_CTRL_0.DPLL_PRED0_DAMPING | Predefined configuration 0 loop filter damping factor. |
| 009h | DPLL_CTRL_0.DPLL_PRED0_DECIMATOR_BW_MULT | Predefined configuration 0 loop filter decimator bandwidth multiplier. |
| 00Ah | DPLL_CTRL_0.DPLL_PRED0_BW | Predefined configuration 0 loop filter bandwidth. |
| 00Ch | DPLL_CTRL_0.DPLL_PRED0_PSL | Predefined configuration 0 loop filter phase slope limit. |
| 00Eh | DPLL_CTRL_0.DPLL_PRED1_DAMPING | Predefined configuration 1 loop filter damping factor. |

Table 250: DPLL_CTRL_0 Register Index

| Offset (Hex) | Register Module Base Address: C600h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 00Fh | DPLL_CTRL_0.DPLL_PRED1_DECIMATOR_BW_MULT | Predefined configuration 1 loop filter decimator bandwidth multiplier. |
| 010h | DPLL_CTRL_0.DPLL_PRED1_BW | Predefined configuration 1 loop filter bandwidth. |
| 012h | DPLL_CTRL_0.DPLL_PRED1_PSL | Predefined configuration 1 loop filter phase slope limit. |
| 014h | DPLL_CTRL_0.DPLL_PHASE_OFFSET_CFG | DPLL phase offset configuration. |
| 019h | DPLL_CTRL_0.DPLL_HO_HISTORY_RESET | Reset advanced holdover history. |
| 01Ah | DPLL_CTRL_0.DPLL_FINE_PHASE_ADV_CFG | DPLL fine phase advance adjustment configuration. |
| 01Ch | DPLL_CTRL_0.DPLL_FOD_FREQ | Fractional Output Divider (FOD) frequency in Hz. |
| 024h | DPLL_CTRL_0.DPLL_MASTER_DIV | Master divider value. |
| 028h | DPLL_CTRL_0.DPLL_COMBO_SW_VALUE_CNFG | DCO value to be added to the combo bus in SW combo mode. |
| 030h | DPLL_CTRL_0.DPLL_MANUAL_HOLDOVER_VALUE | DCO value to be used in manual holdover mode. |
| 036h | DPLL_CTRL_0.DPLL_DCD_FILTER_CNFG | DPLL DCD filter configuration. |
| 038h | DPLL_CTRL_0.DPLL_COMBO_MASTER_BW | DPLL combo filter bandwidth. |
| 03Ah | DPLL_CTRL_0.DPLL_COMBO_MASTER_CFG | DPLL combo master configuration. |
| 03Bh | DPLL_CTRL_0.DPLL_FRAME_PULSE_SYNC | Frame pulse sync trigger |

a. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

### DPLL_CTRL_0.DPLL_HS_TIE_RESET

Reset hitless switching time interval error.

Table 251: DPLL_CTRL_0.DPLL_HS_TIE_RESET Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_HS_TIE_RESET Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | RESERVED[7:1] | | | | | | | TIE_RESET[0] |

| DPLL_CTRL_0.DPLL_HS_TIE_RESET Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| TIE_RESET[0] | R/W | 0 | Hitless reference switch TIE reset.<br>1 = reset. This is a self clear bit. |

### DPLL_CTRL_0.DPLL_MANU_REF_CFG

Select reference to be used for manual reference selection mode.

Table 252: DPLL_CTRL_0.DPLL_MANU_REF_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_MANU_REF_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 001h | RESERVED[7:5] | | | MANUAL_REFERENCE[4:0] | | | | |

| DPLL_CTRL_0.DPLL_MANU_REF_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| MANUAL_REFERENCE[4:0] | R/W | 0 | Index of manually selected reference input when 'manual' reference mode is enabled.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = write-phase input<br>0x11 = write-frequency input<br>0x12 = XO_DPLL<br>0x13 = fb clk of DPLL 0<br>0x14 = fb clk of DPLL 1<br>0x15 = fb clk of DPLL 2<br>0x16 = fb clk of DPLL 3<br>0x17 = fb clk of DPLL 4<br>0x18 = fb clk of DPLL 5<br>0x19 = fb clk of DPLL 6<br>0x1A = fb clk of DPLL 7<br>0x1B = fb clk of SYS DPLL. |

### DPLL_CTRL_0.DPLL_DAMPING

DPLL loop filter damping factor.

Table 253: DPLL_CTRL_0.DPLL_DAMPING Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_DAMPING Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | RESERVED[7:4] | | | | DAMP_FTR[3:0] | | | |

| DPLL_CTRL_0.DPLL_DAMPING Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DAMP_FTR[3:0] | R/W | 0 | DPLL loop filter damping factor.<br>0 = 1.002, 0.02 dB, overdamp;<br>1 = 1.006, 0.05 dB, < 0.05 dB;<br>2 = 1.008, 0.07 dB, < 1%;<br>3 = 1.012, 0.10 dB, < 0.1 dB;<br>4 = 1.015 , 0.13 dB, < 2%;<br>5 = 1.022, 0.19 dB, < 0.2 dB;<br>6 = 1.053 , 0.45 dB, < 0.5 dB;<br>7 = 1.172 , 1.38 dB, underdamp |

### DPLL_CTRL_0.DPLL_DECIMATOR_BW_MULT

DPLL loop filter decimator bandwidth multiplier.

Table 254: DPLL_CTRL_0.DPLL_DECIMATOR_BW_MULT Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_DECIMATOR_BW_MULT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 003h | MULT[7:0] | | | | | | | |

| DPLL_CTRL_0.DPLL_DECIMATOR_BW_MULT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| MULT[7:0] | R/W | 0 | Unsigned 8-bit DPLL loop filter decimator bandwidth multiplier.<br>The decimator BW = decimator BW mult * DPLL BW. Value 0 implies maximum decimator bandwidth.<br>This is not the DPLL bandwidth. |

### DPLL_CTRL_0.DPLL_BW

DPLL loop filter bandwidth.

Table 255: DPLL_CTRL_0.DPLL_BW Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_BW Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | DPLL_BW[7:0] | | | | | | | |
| 005h | BW_UNIT[15:14] | | DPLL_BW[13:8] | | | | | |

| DPLL_CTRL_0.DPLL_BW Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| BW_UNIT[15:14] | R/W | 0 | DPLL loop filter bandwidth unit.<br>0 = uHz<br>1 = mHz<br>2 = Hz<br>3 = kHz |
| DPLL_BW[13:0] | R/W | 0 | Unsigned 14-bit DPLL loop filter bandwidth value. |

### DPLL_CTRL_0.DPLL_PSL

DPLL loop filter phase slope limit.

Table 256: DPLL_CTRL_0.DPLL_PSL Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_PSL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 006h | DPLL_PSL[7:0] | | | | | | | |
| 007h | DPLL_PSL[15:8] | | | | | | | |

| DPLL_CTRL_0.DPLL_PSL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL_PSL[15:0] | R/W | 0 | Unsigned 16-bit loop filter phase slope limit in ns/s. |

### DPLL_CTRL_0.DPLL_PRED0_DAMPING

Predefined configuration 0 loop filter damping factor.

Table 257: DPLL_CTRL_0.DPLL_PRED0_DAMPING Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_PRED0_DAMPING Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 008h | RESERVED[7:4] | | | | DAMP_FTR[3:0] | | | |

| DPLL_CTRL_0.DPLL_PRED0_DAMPING Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DAMP_FTR[3:0] | R/W | 0 | DPLL loop filter damping factor.<br>0 = 1.002, 0.02 dB, overdamp;<br>1 = 1.006, 0.05 dB, < 0.05 dB;<br>2 = 1.008, 0.07 dB, < 1%;<br>3 = 1.012, 0.10 dB, < 0.1 dB;<br>4 = 1.015 , 0.13 dB, < 2%;<br>5 = 1.022, 0.19 dB, < 0.2 dB;<br>6 = 1.053 , 0.45 dB, < 0.5 dB;<br>7 = 1.172 , 1.38 dB, underdamp |

### DPLL_CTRL_0.DPLL_PRED0_DECIMATOR_BW_MULT

Predefined configuration 0 loop filter decimator bandwidth multiplier.

Table 258: DPLL_CTRL_0.DPLL_PRED0_DECIMATOR_BW_MULT Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_PRED0_DECIMATOR_BW_MULT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 009h | MULT[7:0] | | | | | | | |

| DPLL_CTRL_0.DPLL_PRED0_DECIMATOR_BW_MULT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| MULT[7:0] | R/W | 0 | Unsigned 8-bit DPLL loop filter decimator bandwidth multiplier.<br>The decimator BW = decimator BW mult * DPLL BW. Value 0 implies maximum decimator bandwidth. |

### DPLL_CTRL_0.DPLL_PRED0_BW

Predefined configuration 0 loop filter bandwidth.

Table 259: DPLL_CTRL_0.DPLL_PRED0_BW Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_PRED0_BW Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ah | DPLL_PRED0_BW[7:0] | | | | | | | |
| 00Bh | BW_UNIT[15:14] | | DPLL_PRED0_BW[13:8] | | | | | |

| DPLL_CTRL_0.DPLL_PRED0_BW Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| BW_UNIT[15:14] | R/W | 0 | DPLL loop filter bandwidth unit.<br>0 = uHz<br>1 = mHz<br>2 = Hz<br>3 = kHz |
| DPLL_PRED0_BW[13:0] | R/W | 0 | Unsigned 14-bit DPLL loop filter bandwidth value. |

### DPLL_CTRL_0.DPLL_PRED0_PSL

Predefined configuration 0 loop filter phase slope limit.

Table 260: DPLL_CTRL_0.DPLL_PRED0_PSL Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_PRED0_PSL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ch | DPLL_PRED0_PSL[7:0] | | | | | | | |
| 00Dh | DPLL_PRED0_PSL[15:8] | | | | | | | |

| DPLL_CTRL_0.DPLL_PRED0_PSL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL_PRED0_PSL[15:0] | R/W | 0 | Unsigned 16-bit loop filter phase slope limit in ns/s.<br>Value 0 implies no phase slope limit. |

### DPLL_CTRL_0.DPLL_PRED1_DAMPING

Predefined configuration 1 loop filter damping factor.

Table 261: DPLL_CTRL_0.DPLL_PRED1_DAMPING Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_PRED1_DAMPING Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Eh | RESERVED[7:4] | | | | DAMP_FTR[3:0] | | | |

| DPLL_CTRL_0.DPLL_PRED1_DAMPING Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DAMP_FTR[3:0] | R/W | 0 | DPLL loop filter damping factor.<br>0 = 1.002, 0.02 dB, overdamp;<br>1 = 1.006, 0.05 dB, < 0.05 dB;<br>2 = 1.008, 0.07 dB, < 1%;<br>3 = 1.012, 0.10 dB, < 0.1 dB;<br>4 = 1.015 , 0.13 dB, < 2%;<br>5 = 1.022, 0.19 dB, < 0.2 dB;<br>6 = 1.053 , 0.45 dB, < 0.5 dB;<br>7 = 1.172 , 1.38 dB, underdamp |

### DPLL_CTRL_0.DPLL_PRED1_DECIMATOR_BW_MULT

Predefined configuration 1 loop filter decimator bandwidth multiplier.

Table 262: DPLL_CTRL_0.DPLL_PRED1_DECIMATOR_BW_MULT Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_PRED1_DECIMATOR_BW_MULT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Fh | MULT[7:0] | | | | | | | |

| DPLL_CTRL_0.DPLL_PRED1_DECIMATOR_BW_MULT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| MULT[7:0] | R/W | 0 | Unsigned 8-bit DPLL loop filter decimator bandwidth multiplier.<br>The decimator BW = decimator BW mult * DPLL BW. Value 0 implies maximum decimator bandwidth. |

### DPLL_CTRL_0.DPLL_PRED1_BW

Predefined configuration 1 loop filter bandwidth.

Table 263: DPLL_CTRL_0.DPLL_PRED1_BW Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_PRED1_BW Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 010h | DPLL_PRED1_BW[7:0] | | | | | | | |
| 011h | BW_UNIT[15:14] | | DPLL_PRED1_BW[13:8] | | | | | |

| DPLL_CTRL_0.DPLL_PRED1_BW Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| BW_UNIT[15:14] | R/W | 0 | DPLL loop filter bandwidth unit.<br>0 = uHz<br>1 = mHz<br>2 = Hz<br>3 = kHz |
| DPLL_PRED1_BW[13:0] | R/W | 0 | Unsigned 14-bit DPLL loop filter bandwidth value. |

### DPLL_CTRL_0.DPLL_PRED1_PSL

Predefined configuration 1 loop filter phase slope limit.

Table 264: DPLL_CTRL_0.DPLL_PRED1_PSL Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_PRED1_PSL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 012h | DPLL_PRED1_PSL[7:0] | | | | | | | |
| 013h | DPLL_PRED1_PSL[15:8] | | | | | | | |

| DPLL_CTRL_0.DPLL_PRED1_PSL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL_PRED1_PSL[15:0] | R/W | 0 | Unsigned 16-bit loop filter phase slope limit in ns/s.<br>Value 0 implies no phase slope limit. |

### DPLL_CTRL_0.DPLL_PHASE_OFFSET_CFG

DPLL phase offset configuration.

Table 265: DPLL_CTRL_0.DPLL_PHASE_OFFSET_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_PHASE_OFFSET_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 014h | DPLL_PHASE_OFFSET_CFG[7:0] | | | | | | | |
| 015h | DPLL_PHASE_OFFSET_CFG[15:8] | | | | | | | |
| 016h | DPLL_PHASE_OFFSET_CFG[23:16] | | | | | | | |
| 017h | DPLL_PHASE_OFFSET_CFG[31:24] | | | | | | | |
| 018h | RESERVED[39:36] | | | | DPLL_PHASE_OFFSET_CFG[35:32] | | | |

| DPLL_CTRL_0.DPLL_PHASE_OFFSET_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL_PHASE_OFFSET_CFG[35:0] | R/W | 0 | Signed 36-bit phase offset in ITDC_UIs.<br>ITDC_UI is input TDC unit interval. Please refer to the SCSR_INPUT_TDC module for details on input TDC settings and ITDC_UI value. The default input TDC settings yield 50ps ITDC_UI. A positive value here will cause an output clock phase delay relative to the input clock phase and a negative value will cause an output phase advance relative to the input clock phase.<br>Note that this phase offset configuration applies to both DPLL mode and write phase mode. |

### DPLL_CTRL_0.DPLL_HO_HISTORY_RESET

Reset advanced holdover history.

Table 266: DPLL_CTRL_0.DPLL_HO_HISTORY_RESET Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_HO_HISTORY_RESET Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 019h | RESERVED[7:1] | | | | | | | HO_HISTORY_RESET[0] |

| DPLL_CTRL_0.DPLL_HO_HISTORY_RESET Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| HO_HISTORY_RESET[0] | R/W | 0 | Reset advanced holdover history.<br>1 = enable reset, 0 = cancel reset. This bit is a self-clear bit. When the HO history is cleared, this bit will be cleared to 0 by FW. |

### DPLL_CTRL_0.DPLL_FINE_PHASE_ADV_CFG

Configure the fine phase advance to be applied to the DPLL.

Table 267: DPLL_CTRL_0.DPLL_FINE_PHASE_ADV_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_FINE_PHASE_ADV_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Ah | FINE_PHASE_ADVANCE[7:0] | | | | | | | |
| 01Bh | RESERVED[15:13] | | | FINE_PHASE_ADVANCE[12:8] | | | | |

| DPLL_CTRL_0.DPLL_FINE_PHASE_ADV_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| FINE_PHASE_ADVANCE[12:0] | R/W | 0 | Unsigned (i.e. positive) 13-bit fine phase advance.<br>Note: This register must be set to 0 if the DPLL feedback clock has a fractional component.<br>Resolution is in units of input TDC period/4096. The default input TDC clock is 625 MHz, so the default input TDC period is 1.6 ns which results in a resolution of approximately 391 fs.<br>Ex. 0x0002 translates to 782 fs (0.782 ps) phase advance applied to the DPLL. Conversely, 0x0000 means no phase advance is applied to the DPLL.<br>Note: Phase advance is defined as the phase of the output that is measured relative to another reference and the output clocks rising edge comes after the rising edge of the reference signal, by some amount X, then a phase advance on the output clock will result in a measurement of X - fine_phase_advance.<br>Note: The DPLL fractional feedback clock frequency correction is lost when a non zero phase advance is applied. To restore previous DPLL configuration, need to set 'fine_phase_advance' to 0 and re-trigger the DPLL configuration. |

### DPLL_CTRL_0.DPLL_FOD_FREQ

DPLL FOD frequency is determined by M / N.

Table 268: DPLL_CTRL_0.DPLL_FOD_FREQ Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_FOD_FREQ Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Ch | M[7:0] | | | | | | | |
| 01Dh | M[15:8] | | | | | | | |
| 01Eh | M[23:16] | | | | | | | |
| 01Fh | M[31:24] | | | | | | | |
| 020h | M[39:32] | | | | | | | |
| 021h | M[47:40] | | | | | | | |
| 022h | N[7:0] | | | | | | | |
| 023h | N[15:8] | | | | | | | |

| DPLL_CTRL_0.DPLL_FOD_FREQ Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| N[15:0] | R/W | 0 | Unsigned 16-bit frequency N field.<br>N is unsigned 16-bit. A value of 0 for this field will be interpreted as 1. |
| M[47:0] | R/W | 0 | Unsigned 48-bit frequency M field.<br>A setting of 0 will disable the FOD, but not other parts of the DPLL. This will significantly reduce the power consumption of this DPLL. As there is no clock output from the FOD when this field is set to 0, it is suggested to disable the outputs which are associated with this FOD by setting SCSR_OUTPUT_0.PAD_MODE to 0 (high-Z mode). |

### DPLL_CTRL_0.DPLL_MASTER_DIV

Master divider value.

Table 269: DPLL_CTRL_0.DPLL_MASTER_DIV Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_MASTER_DIV Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 024h | DPLL_MASTER_DIV[7:0] | | | | | | | |
| 025h | DPLL_MASTER_DIV[15:8] | | | | | | | |
| 026h | DPLL_MASTER_DIV[23:16] | | | | | | | |
| 027h | DPLL_MASTER_DIV[31:24] | | | | | | | |

| DPLL_CTRL_0.DPLL_MASTER_DIV Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL_MASTER_DIV[31:0] | R/W | 0 | Unsigned 32-bit master divider value.<br>For each of the 8 output channels, there is a master divider circuit that divides down the FOD clock. The purpose of this divider is to send sync signals to the output channel's important dividers, such as the integer output divider(s), the DPLL feedback divider, the DPLL feedback frame divider and the ToD (for those channels that have a ToD).<br>0 means the master divider is automatically set to a value that results in an 8 KHz signal coming out of the master divider block.<br>If any of the outputs are lower than 8kHz or any of the outputs/inputs are not a multiple of 8kHz, this needs to be updated to reflect the lowest common multiple (of all outputs/inputs).<br>If ToD[3:0] is being used (i.e. enabled), then the master divider for the associated DPLL[3:0] must be programmed to 1PPS (1Hz) or PPES (0.5Hz) (i.e. to match the ToD internal output). |

### DPLL_CTRL_0.DPLL_COMBO_SW_VALUE_CNFG

DCO value to be added to the combo bus in SW combo mode.

Table 270: DPLL_CTRL_0.DPLL_COMBO_SW_VALUE_CNFG Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_COMBO_SW_VALUE_CNFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 028h | DPLL_COMBO_SW_VALUE_CNFG[7:0] | | | | | | | |
| 029h | DPLL_COMBO_SW_VALUE_CNFG[15:8] | | | | | | | |
| 02Ah | DPLL_COMBO_SW_VALUE_CNFG[23:16] | | | | | | | |
| 02Bh | DPLL_COMBO_SW_VALUE_CNFG[31:24] | | | | | | | |
| 02Ch | DPLL_COMBO_SW_VALUE_CNFG[39:32] | | | | | | | |
| 02Dh | DPLL_COMBO_SW_VALUE_CNFG[47:40] | | | | | | | |

| DPLL_CTRL_0.DPLL_COMBO_SW_VALUE_CNFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL_COMBO_SW_VALUE_CNFG[47:0] | R/W | 0 | DPLL Combo SW value in units of 2^(-53). |

### DPLL_CTRL_0.DPLL_MANUAL_HOLDOVER_VALUE

DCO value to be used in manual holdover mode.

Table 271: DPLL_CTRL_0.DPLL_MANUAL_HOLDOVER_VALUE Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_MANUAL_HOLDOVER_VALUE Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 030h | DPLL_MANUAL_HOLDOVER_VALUE[7:0] | | | | | | | |
| 031h | DPLL_MANUAL_HOLDOVER_VALUE[15:8] | | | | | | | |
| 032h | DPLL_MANUAL_HOLDOVER_VALUE[23:16] | | | | | | | |
| 033h | DPLL_MANUAL_HOLDOVER_VALUE[31:24] | | | | | | | |
| 034h | DPLL_MANUAL_HOLDOVER_VALUE[39:32] | | | | | | | |
| 035h | RESERVED[47:42] | | | | | | DPLL_MANUAL_HOLDOVER_VALUE[41:40] | |

| DPLL_CTRL_0.DPLL_MANUAL_HOLDOVER_VALUE Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL_MANUAL_HOLDOVER_VALUE[41:0] | R/W | 0 | Signed 42-bit FFO in units of 2^(-53).<br>The holdover value used when DPLL_n.DPLL_HI_CFG.HOLDOVER_MODE is configured to manual holdover. |

### DPLL_CTRL_0.DPLL_DCD_FILTER_CNFG

DPLL DCD filter configuration.

Table 272: DPLL_CTRL_0.DPLL_DCD_FILTER_CNFG Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_DCD_FILTER_CNFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 036h | DCD_MANU_UPDATE_RATE_CNFG[7:6] | | DCD_MANU_GAIN_SHIFT[5:1] | | | | | DCD_MANU_EN[0] |
| 037h | RESERVED[15] | DCD_LPF_COE[14:10] | | | | | DCD_MANU_UPDATE_RATE_CNFG[9:8] | |

| DPLL_CTRL_0.DPLL_DCD_FILTER_CNFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DCD_LPF_COE[14:10] | R/W | 1010b | DCD low pass filter coefficient. |
| DCD_MANU_UPDATE_RATE_CNFG[9:6] | R/W | 202h | Configure DCD manual calibration mode updating rate.<br>Updating rate = 10000/(2^dcd_manu_update_rate_cnfg) in Hz. |
| DCD_MANU_GAIN_SHIFT[5:1] | R/W | 10h | DCD manual calibration mode gain down shift bits. |
| DCD_MANU_EN[0] | R/W | 0001b | Enable DCD manual calibration mode.<br>0 = disabled<br>1 = enabled |

### DPLL_CTRL_0.DPLL_COMBO_MASTER_BW

DPLL combo filter bandwidth.

Table 273: DPLL_CTRL_0.DPLL_COMBO_MASTER_BW Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_COMBO_MASTER_BW Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 038h | DPLL_COMBO_MASTER_BW[7:0] | | | | | | | |
| 039h | BW_UNIT[15:14] | | DPLL_COMBO_MASTER_BW[13:8] | | | | | |

| DPLL_CTRL_0.DPLL_COMBO_MASTER_BW Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| BW_UNIT[15:14] | R/W | 0 | Combo filter bandwidth unit.<br>0 = uHz<br>1 = mHz<br>2 = Hz<br>3 = kHz |
| DPLL_COMBO_MASTER_BW[13:0] | R/W | 0 | Unsigned 14-bit Combo filter bandwidth value. |

### DPLL_CTRL_0.DPLL_COMBO_MASTER_CFG

DPLL combo master configuration.

Table 274: DPLL_CTRL_0.DPLL_COMBO_MASTER_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_COMBO_MASTER_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 03Ah | RESERVED[7:2] | | | | | | FILTER_IN_SELECT[1] | HOLD_EN[0] |

| DPLL_CTRL_0.DPLL_COMBO_MASTER_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| FILTER_IN_SELECT[1] | R/W | 0 | Select filtered DCO value as combo source.<br>0 = integrator value only<br>1 = sum of proportional and integrator |
| HOLD_EN[0] | R/W | 0 | Combo bus output hold (freeze).<br>0 = no hold<br>1 = hold (freeze). |

### DPLL_CTRL_0.DPLL_FRAME_PULSE_SYNC

Frame pulse sync trigger

Table 275: DPLL_CTRL_0.DPLL_FRAME_PULSE_SYNC Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_CTRL_0.DPLL_FRAME_PULSE_SYNC Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 03Bh | RESERVED[7:1] | | | | | | | FRAME_PULSE_SYNC[0] |

| DPLL_CTRL_0.DPLL_FRAME_PULSE_SYNC Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| FRAME_PULSE_SYNC[0] | R/W | 0 | Trigger a frame pulse sync<br>Write 1 to trigger a frame pulse sync procedure. This bit will be self-cleared after the sync finished. Write 0 will have no effect.<br>0 = no effect<br>1 = trigger a frame pulse sync |

## Module: SYS_DPLL_CTRL

TRIGGER: Every register in this module is a trigger register. In the case of a multibyte register the highest address register byte is the trigger byte.

Table 276: SYS_DPLL_CTRL Register Index

| Offset (Hex) | Register Module Base Address: C800h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | SYS_DPLL_CTRL.SYS_DPLL_MANU_REF_CFG | Manual reference mode configuration. |
| 001h | SYS_DPLL_CTRL.SYS_DPLL_DAMPING | System DPLL loop filter damping factor. |
| 002h | SYS_DPLL_CTRL.SYS_DPLL_DECIMATOR_BW_MULT | System DPLL loop filter decimator bandwidth multiplier. |
| 004h | SYS_DPLL_CTRL.SYS_DPLL_BW | System DPLL loop filter bandwidth. |
| 006h | SYS_DPLL_CTRL.SYS_DPLL_PSL | System DPLL loop filter phase slope limit. |
| 008h | SYS_DPLL_CTRL.SYS_DPLL_PRED0_DAMPING | Predefined configuration 0 loop filter damping factor. |
| 009h | SYS_DPLL_CTRL.SYS_DPLL_PRED0_DECIMATOR_BW_MULT | Predefined configuration 0 loop filter decimator bandwidth multiplier. |
| 00Ah | SYS_DPLL_CTRL.SYS_DPLL_PRED0_BW | Predefined configuration 0 loop filter bandwidth. |
| 00Ch | SYS_DPLL_CTRL.SYS_DPLL_PRED0_PSL | Predefined configuration 0 loop filter  phase slope limit. |
| 00Eh | SYS_DPLL_CTRL.SYS_DPLL_PRED1_DAMPING | Predefined configuration 1 loop filter damping factor. |
| 00Fh | SYS_DPLL_CTRL.SYS_DPLL_PRED1_DECIMATOR_BW_MULT | Predefined configuration 1 loop filter decimator bandwidth multiplier. |
| 010h | SYS_DPLL_CTRL.SYS_DPLL_PRED1_BW | Predefined configuration 1 loop filter bandwidth. |
| 012h | SYS_DPLL_CTRL.SYS_DPLL_PRED1_PSL | Predefined configuration 1 loop filter phase slope limit. |
| 014h | SYS_DPLL_CTRL.SYS_DPLL_COMBO_MASTER_BW | System DPLL combo filter bandwidth. |
| 016h | SYS_DPLL_CTRL.SYS_DPLL_COMBO_MASTER_CFG | DPLL combo master configuration. |

### SYS_DPLL_CTRL.SYS_DPLL_MANU_REF_CFG

Select reference to be used for manual reference selection mode.

Table 277: SYS_DPLL_CTRL.SYS_DPLL_MANU_REF_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_CTRL.SYS_DPLL_MANU_REF_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | RESERVED[7:5] | | | MANUAL_REFERENCE[4:0] | | | | |

| SYS_DPLL_CTRL.SYS_DPLL_MANU_REF_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| MANUAL_REFERENCE[4:0] | R/W | 0 | Index of manually selected reference input when 'manual' reference mode is enabled.<br>0x00 = CLK0<br>0x01 = CLK1<br>0x02 = CLK2<br>0x03 = CLK3<br>0x04 = CLK4<br>0x05 = CLK5<br>0x06 = CLK6<br>0x07 = CLK7<br>0x08 = CLK8<br>0x09 = CLK9<br>0x0A = CLK10<br>0x0B = CLK11<br>0x0C = CLK12<br>0x0D = CLK13<br>0x0E = CLK14<br>0x0F = CLK15<br>0x10 = reserved<br>0x11 = reserved<br>0x12 = XO_DPLL |

### SYS_DPLL_CTRL.SYS_DPLL_DAMPING

System DPLL loop filter damping factor.

Table 278: SYS_DPLL_CTRL.SYS_DPLL_DAMPING Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_CTRL.SYS_DPLL_DAMPING Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 001h | RESERVED[7:4] | | | | DAMP_FTR[3:0] | | | |

| SYS_DPLL_CTRL.SYS_DPLL_DAMPING Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DAMP_FTR[3:0] | R/W | 0 | System DPLL loop filter damping factor<br>0 = 1.002, 0.02 dB, overdamp;<br>1 = 1.006, 0.05 dB, < 0.05 dB;<br>2 = 1.008, 0.07 dB, < 1%;<br>3 = 1.012, 0.10 dB, < 0.1 dB;<br>4 = 1.015 , 0.13 dB, < 2%;<br>5 = 1.022, 0.19 dB, < 0.2 dB;<br>6 = 1.053 , 0.45 dB, < 0.5 dB;<br>7 = 1.172 , 1.38 dB, underdamp |

### SYS_DPLL_CTRL.SYS_DPLL_DECIMATOR_BW_MULT

System DPLL loop filter decimator bandwidth multiplier.

Table 279: SYS_DPLL_CTRL.SYS_DPLL_DECIMATOR_BW_MULT Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_CTRL.SYS_DPLL_DECIMATOR_BW_MULT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | MULT[7:0] | | | | | | | |

| SYS_DPLL_CTRL.SYS_DPLL_DECIMATOR_BW_MULT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| MULT[7:0] | R/W | 0 | Unsigned 8-bit system DPLL loop filter decimator bandwidth multiplier.<br>The decimator BW = decimator BW mult * DPLL BW. Value 0 implies maximum decimator bandwidth.<br>This is not the system DPLL bandwidth. |

### SYS_DPLL_CTRL.SYS_DPLL_BW

System DPLL loop filter bandwidth.

Table 280: SYS_DPLL_CTRL.SYS_DPLL_BW Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_CTRL.SYS_DPLL_BW Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | SYS_DPLL_BW[7:0] | | | | | | | |
| 005h | BW_UNIT[15:14] | | SYS_DPLL_BW[13:8] | | | | | |

| SYS_DPLL_CTRL.SYS_DPLL_BW Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| BW_UNIT[15:14] | R/W | 0 | System DPLL loop filter bandwidth unit.<br>0 = uHz<br>1 = mHz<br>2 = Hz<br>3 = kHz |
| SYS_DPLL_BW[13:0] | R/W | 0 | Unsigned 14-bit system DPLL loop filter bandwidth value. |

### SYS_DPLL_CTRL.SYS_DPLL_PSL

System DPLL loop filter phase slope limit.

Table 281: SYS_DPLL_CTRL.SYS_DPLL_PSL Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_CTRL.SYS_DPLL_PSL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 006h | SYS_DPLL_PSL[7:0] | | | | | | | |
| 007h | SYS_DPLL_PSL[15:8] | | | | | | | |

| SYS_DPLL_CTRL.SYS_DPLL_PSL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SYS_DPLL_PSL[15:0] | R/W | 0 | Unsigned 16-bit loop filter phase slope limit in ns/s. |

### SYS_DPLL_CTRL.SYS_DPLL_PRED0_DAMPING

Predefined configuration 0 loop filter damping factor.

Table 282: SYS_DPLL_CTRL.SYS_DPLL_PRED0_DAMPING Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_CTRL.SYS_DPLL_PRED0_DAMPING Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 008h | RESERVED[7:4] | | | | DAMP_FTR[3:0] | | | |

| SYS_DPLL_CTRL.SYS_DPLL_PRED0_DAMPING Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DAMP_FTR[3:0] | R/W | 0 | System DPLL loop filter damping factor.<br>0 = 1.002, 0.02 dB, overdamp;<br>1 = 1.006, 0.05 dB, < 0.05 dB;<br>2 = 1.008, 0.07 dB, < 1%;<br>3 = 1.012, 0.10 dB, < 0.1 dB;<br>4 = 1.015 , 0.13 dB, < 2%;<br>5 = 1.022, 0.19 dB, < 0.2 dB;<br>6 = 1.053 , 0.45 dB, < 0.5 dB;<br>7 = 1.172 , 1.38 dB, underdamp |

### SYS_DPLL_CTRL.SYS_DPLL_PRED0_DECIMATOR_BW_MULT

Predefined configuration 0 loop filter decimator bandwidth multiplier.

Table 283: SYS_DPLL_CTRL.SYS_DPLL_PRED0_DECIMATOR_BW_MULT Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_CTRL.SYS_DPLL_PRED0_DECIMATOR_BW_MULT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 009h | MULT[7:0] | | | | | | | |

| SYS_DPLL_CTRL.SYS_DPLL_PRED0_DECIMATOR_BW_MULT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| MULT[7:0] | R/W | 0 | Unsigned 8-bit system DPLL loop filter decimator bandwidth multiplier.<br>The decimator BW = decimator BW mult * DPLL BW. Value 0 implies maximum decimator bandwidth. |

### SYS_DPLL_CTRL.SYS_DPLL_PRED0_BW

Predefined configuration 0 loop filter bandwidth.

Table 284: SYS_DPLL_CTRL.SYS_DPLL_PRED0_BW Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_CTRL.SYS_DPLL_PRED0_BW Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ah | SYS_DPLL_PRED0_BW[7:0] | | | | | | | |
| 00Bh | BW_UNIT[15:14] | | SYS_DPLL_PRED0_BW[13:8] | | | | | |

| SYS_DPLL_CTRL.SYS_DPLL_PRED0_BW Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| BW_UNIT[15:14] | R/W | 0 | System DPLL loop filter bandwidth unit.<br>0 = uHz<br>1 = mHz<br>2 = Hz<br>3 = kHz |
| SYS_DPLL_PRED0_BW[13:0] | R/W | 0 | Unsigned 14-bit system DPLL loop filter bandwidth value. |

### SYS_DPLL_CTRL.SYS_DPLL_PRED0_PSL

Predefined configuration 0 loop filter phase slope limit.

Table 285: SYS_DPLL_CTRL.SYS_DPLL_PRED0_PSL Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_CTRL.SYS_DPLL_PRED0_PSL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ch | SYS_DPLL_PRED0_PSL[7:0] | | | | | | | |
| 00Dh | SYS_DPLL_PRED0_PSL[15:8] | | | | | | | |

| SYS_DPLL_CTRL.SYS_DPLL_PRED0_PSL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SYS_DPLL_PRED0_PSL[15:0] | R/W | 0 | Unsigned 16-bit loop filter phase slope limit in ns/s.<br>Value 0 implies no phase slope limit. |

### SYS_DPLL_CTRL.SYS_DPLL_PRED1_DAMPING

Predefined configuration 1 loop filter damping factor.

Table 286: SYS_DPLL_CTRL.SYS_DPLL_PRED1_DAMPING Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_CTRL.SYS_DPLL_PRED1_DAMPING Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Eh | RESERVED[7:4] | | | | DAMP_FTR[3:0] | | | |

| SYS_DPLL_CTRL.SYS_DPLL_PRED1_DAMPING Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DAMP_FTR[3:0] | R/W | 0 | System DPLL loop filter damping factor.<br>0 = 1.002, 0.02 dB, overdamp;<br>1 = 1.006, 0.05 dB, < 0.05 dB;<br>2 = 1.008, 0.07 dB, < 1%;<br>3 = 1.012, 0.10 dB, < 0.1 dB;<br>4 = 1.015 , 0.13 dB, < 2%;<br>5 = 1.022, 0.19 dB, < 0.2 dB;<br>6 = 1.053 , 0.45 dB, < 0.5 dB;<br>7 = 1.172 , 1.38 dB, underdamp |

### SYS_DPLL_CTRL.SYS_DPLL_PRED1_DECIMATOR_BW_MULT

Predefined configuration 1 loop filter decimator bandwidth multiplier.

Table 287: SYS_DPLL_CTRL.SYS_DPLL_PRED1_DECIMATOR_BW_MULT Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_CTRL.SYS_DPLL_PRED1_DECIMATOR_BW_MULT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Fh | MULT[7:0] | | | | | | | |

| SYS_DPLL_CTRL.SYS_DPLL_PRED1_DECIMATOR_BW_MULT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| MULT[7:0] | R/W | 0 | Unsigned 8-bit system DPLL loop filter decimator bandwidth multiplier.<br>The decimator BW = decimator BW mult * DPLL BW. Value 0 implies maximum decimator bandwidth. |

### SYS_DPLL_CTRL.SYS_DPLL_PRED1_BW

Predefined configuration 1 loop filter bandwidth.

Table 288: SYS_DPLL_CTRL.SYS_DPLL_PRED1_BW Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_CTRL.SYS_DPLL_PRED1_BW Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 010h | SYS_DPLL_PRED1_BW[7:0] | | | | | | | |
| 011h | BW_UNIT[15:14] | | SYS_DPLL_PRED1_BW[13:8] | | | | | |

| SYS_DPLL_CTRL.SYS_DPLL_PRED1_BW Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| BW_UNIT[15:14] | R/W | 0 | System DPLL loop filter bandwidth unit.<br>0 = uHz<br>1 = mHz<br>2 = Hz<br>3 = kHz |
| SYS_DPLL_PRED1_BW[13:0] | R/W | 0 | Unsigned 14-bit system DPLL loop filter bandwidth value. |

### SYS_DPLL_CTRL.SYS_DPLL_PRED1_PSL

Predefined configuration 1 loop filter phase slope limit.

Table 289: SYS_DPLL_CTRL.SYS_DPLL_PRED1_PSL Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_CTRL.SYS_DPLL_PRED1_PSL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 012h | SYS_DPLL_PRED1_PSL[7:0] | | | | | | | |
| 013h | SYS_DPLL_PRED1_PSL[15:8] | | | | | | | |

| SYS_DPLL_CTRL.SYS_DPLL_PRED1_PSL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SYS_DPLL_PRED1_PSL[15:0] | R/W | 0 | Unsigned 16-bit loop filter phase slope limit in ns/s.<br>Value 0 implies no phase slope limit. |

### SYS_DPLL_CTRL.SYS_DPLL_COMBO_MASTER_BW

System DPLL combo filter bandwidth.

Table 290: SYS_DPLL_CTRL.SYS_DPLL_COMBO_MASTER_BW Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_CTRL.SYS_DPLL_COMBO_MASTER_BW Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 014h | SYS_DPLL_COMBO_MASTER_BW[7:0] | | | | | | | |
| 015h | BW_UNIT[15:14] | | SYS_DPLL_COMBO_MASTER_BW[13:8] | | | | | |

| SYS_DPLL_CTRL.SYS_DPLL_COMBO_MASTER_BW Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| BW_UNIT[15:14] | R/W | 0 | Combo filter bandwidth unit.<br>0 = uHz<br>1 = mHz<br>2 = Hz<br>3 = kHz |
| SYS_DPLL_COMBO_MASTER_BW[13:0] | R/W | 0 | Unsigned 14-bit Combo filter bandwidth value. |

### SYS_DPLL_CTRL.SYS_DPLL_COMBO_MASTER_CFG

DPLL combo master configuration.

Table 291: SYS_DPLL_CTRL.SYS_DPLL_COMBO_MASTER_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | SYS_DPLL_CTRL.SYS_DPLL_COMBO_MASTER_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 016h | RESERVED[7:2] | | | | | | FILTER_IN_SELECT[1] | HOLD_EN[0] |

| SYS_DPLL_CTRL.SYS_DPLL_COMBO_MASTER_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| FILTER_IN_SELECT[1] | R/W | 0 | Select filtered DCO value as combo source.<br>0 = integrator value only<br>1 = sum of proportional and integrator |
| HOLD_EN[0] | R/W | 0 | Combo bus output hold (freeze).<br>0 = no hold<br>1 = hold (freeze). |

## Module: DPLL_PHASE_0

Configures the DPLL phase.

Table 292: DPLL_PHASE_0 Register Index

| Offset (Hex) | Register Module Base Address: C818h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | DPLL_PHASE_0.DPLL_WRITE_PH | Set phase offset in write phase mode. |

a. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

### DPLL_PHASE_0.DPLL_WRITE_PH

Set phase offset in write phase mode.

Table 293: DPLL_PHASE_0.DPLL_WRITE_PH Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_PHASE_0.DPLL_WRITE_PH Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | DPLL_WRITE_PH[7:0] | | | | | | | |
| 001h | DPLL_WRITE_PH[15:8] | | | | | | | |
| 002h | DPLL_WRITE_PH[23:16] | | | | | | | |
| 003h | DPLL_WRITE_PH[31:24] | | | | | | | |

| DPLL_PHASE_0.DPLL_WRITE_PH Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL_WRITE_PH[31:0] | R/W | 0 | Signed 32-bit phase offset in ITDC_UIs.<br>When DPLL_n.DPLL_MODE.PLL_MODE = write phase mode, this value inputs to the loop filter and controls the DPLL phase. |

## Module: DPLL_FREQ_0

Configures the DPLL phase.

Table 294: DPLL_FREQ_0 Register Index

| Offset (Hex) | Register Module Base Address: C838h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | DPLL_FREQ_0.DPLL_WR_FREQ | Set DPLL frequency offset in write frequency mode. |
| 006h | RESERVED | This register must not be modified from the read value |
| 007h | RESERVED | This register must not be modified from the read value |

a. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

### DPLL_FREQ_0.DPLL_WR_FREQ

Set DPLL frequency offset in write frequency mode.

Table 295: DPLL_FREQ_0.DPLL_WR_FREQ Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_FREQ_0.DPLL_WR_FREQ Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | DPLL_WR_FREQ[7:0] | | | | | | | |
| 001h | DPLL_WR_FREQ[15:8] | | | | | | | |
| 002h | DPLL_WR_FREQ[23:16] | | | | | | | |
| 003h | DPLL_WR_FREQ[31:24] | | | | | | | |
| 004h | DPLL_WR_FREQ[39:32] | | | | | | | |
| 005h | RESERVED[47:42] | | | | | | DPLL_WR_FREQ[41:40] | |

| DPLL_FREQ_0.DPLL_WR_FREQ Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL_WR_FREQ[41:0] | R/W | 0 | Signed 42-bit FFO in units of 2^(-53).<br>Used when DPLL_n.DPLL_MODE.PLL_MODE = write frequency mode. |

## Module: DPLL_PHASE_PULL_IN_0

Configures the DPLL phase pull-in.

Table 296: DPLL_PHASE_PULL_IN_0 Register Index

| Offset (Hex) | Register Module Base Address: C880h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | DPLL_PHASE_PULL_IN_0.DPLL_PHASE_PULL_IN_OFFSET | Phase pull-in offset. |
| 004h | DPLL_PHASE_PULL_IN_0.DPLL_PHASE_PULL_IN_SLOPE_LIMIT | Phase pull-in slope limit. |
| 007h | DPLL_PHASE_PULL_IN_0.DPLL_PHASE_PULL_IN_CTRL | Phase pull-in configuration. |

a. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

### DPLL_PHASE_PULL_IN_0.DPLL_PHASE_PULL_IN_OFFSET

Phase pull-in offset.

Table 297: DPLL_PHASE_PULL_IN_0.DPLL_PHASE_PULL_IN_OFFSET Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_PHASE_PULL_IN_0.DPLL_PHASE_PULL_IN_OFFSET Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | DPLL_PHASE_PULL_IN_OFFSET[7:0] | | | | | | | |
| 001h | DPLL_PHASE_PULL_IN_OFFSET[15:8] | | | | | | | |
| 002h | DPLL_PHASE_PULL_IN_OFFSET[23:16] | | | | | | | |
| 003h | DPLL_PHASE_PULL_IN_OFFSET[31:24] | | | | | | | |

| DPLL_PHASE_PULL_IN_0.DPLL_PHASE_PULL_IN_OFFSET Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL_PHASE_PULL_IN_OFFSET[31:0] | R/W | 0 | Signed 32-bit phase pull-in offset in nanoseconds.<br>The phase offset for the phase pull-in operation. |

### DPLL_PHASE_PULL_IN_0.DPLL_PHASE_PULL_IN_SLOPE_LIMIT

Phase pull-in slope limit.

Table 298: DPLL_PHASE_PULL_IN_0.DPLL_PHASE_PULL_IN_SLOPE_LIMIT Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_PHASE_PULL_IN_0.DPLL_PHASE_PULL_IN_SLOPE_LIMIT Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | DPLL_PHASE_PULL_IN_SLOPE_LIMIT[7:0] | | | | | | | |
| 005h | DPLL_PHASE_PULL_IN_SLOPE_LIMIT[15:8] | | | | | | | |
| 006h | DPLL_PHASE_PULL_IN_SLOPE_LIMIT[23:16] | | | | | | | |

| DPLL_PHASE_PULL_IN_0.DPLL_PHASE_PULL_IN_SLOPE_LIMIT Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL_PHASE_PULL_IN_SLOPE_LIMIT[23:0] | R/W | 0 | Unsigned 24-bit max FFO in ppb.<br>The maximum FFO value for calculating phase pull-in time. This value should not exceed 244000 ppb. Value 0 implies that the maximum FFO 244000 ppb will be applied. |

### DPLL_PHASE_PULL_IN_0.DPLL_PHASE_PULL_IN_CTRL

Phase pull-in configuration.

Table 299: DPLL_PHASE_PULL_IN_0.DPLL_PHASE_PULL_IN_CTRL Bit Field Locations and Descriptions

| Offset Address (Hex) | DPLL_PHASE_PULL_IN_0.DPLL_PHASE_PULL_IN_CTRL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 007h | RESERVED[7:1] | | | | | | | PHASE_PULL_IN_REQUEST[0] |

| DPLL_PHASE_PULL_IN_0.DPLL_PHASE_PULL_IN_CTRL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| PHASE_PULL_IN_REQUEST[0] | R/W | 0 | Phase pull-in request.<br>Setting this bit to "1" starts a phase pull-in if there is no one in progress. Otherwise, it will be ignored. Setting this bit to "0" terminates the on-going phase pull-in. This request is only applicable to pll_mode: "write phase mode", "write frequency mode", "GPIO inc/dec mode", and "synthesizer mode". It will be ignored if the DPLL is in other modes. A pll-mode change will trigger a termination of on-going phase pull-in. This bit will be self-cleared after the phase pull-in finished. |

## Module: GPIO_CFG

Global GPIO configuration.

Table 300: GPIO_CFG Register Index

| Offset (Hex) | Register Module Base Address: C8C0h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | GPIO_CFG.GPIO_CFG_GBL | Global GPIO parameters. |

### GPIO_CFG.GPIO_CFG_GBL

Enable the GPIO drive supply mode.

TRIGGER: Writing to this byte triggers a read and activation in hardware of all the bytes of the GPIO_DC_CFG module.

Table 301: GPIO_CFG.GPIO_CFG_GBL Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_CFG.GPIO_CFG_GBL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | RESERVED[7:2] | | | | | | SUPPLY_MODE[1:0] | |

| GPIO_CFG.GPIO_CFG_GBL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| SUPPLY_MODE[1:0] | R/W | 0 | Select GPIO supply rail configuration.<br>Select GPIO drive voltage.<br>0 = 1.8 V<br>1 = 2.5 V/3.3 V<br>2 = 1.5 V |

## Module: GPIO_0

Configure the GPIO registers.

Table 302: GPIO_0 Register Index

| Offset (Hex) | Register Module Base Address: C8C2h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | GPIO_0.GPIO_DCO_INC_DEC | Increment/decrement DCO FFO configuration. |
| 001h | GPIO_0.GPIO_OUT_CTRL_0 | GPIO controlled output squelch for outputs 0-7. |
| 002h | GPIO_0.GPIO_OUT_CTRL_1 | GPIO controlled output squelch for outputs 8-11. |
| 003h | GPIO_0.GPIO_TOD_TRIG | GPIO controlled TOD trigger input. |
| 004h | GPIO_0.GPIO_DPLL_INDICATOR | GPIO indicator for DPLL lock and holdover states. |
| 005h | GPIO_0.GPIO_LOS_INDICATOR | GPIO loss of signal (LOS) indicator. |
| 006h | GPIO_0.GPIO_REF_INPUT_DSQ_0 | GPIO controlled input disqualification for inputs 0-7. |
| 007h | GPIO_0.GPIO_REF_INPUT_DSQ_1 | GPIO controlled input disqualification for inputs 8-15. |
| 008h | GPIO_0.GPIO_REF_INPUT_DSQ_2 | GPIO controlled input disqualification for DPLLs. |
| 009h | GPIO_0.GPIO_REF_INPUT_DSQ_3 | GPIO controlled input disqualification for system DPLL and disqualification level. |
| 00Ah | GPIO_0.GPIO_MAN_CLK_SEL_0 | Configure inputs for GPIO manual clock selection. |
| 00Bh | GPIO_0.GPIO_MAN_CLK_SEL_1 | Select DPLLs for GPIO manual clock selection. |
| 00Ch | GPIO_0.GPIO_MAN_CLK_SEL_2 | Select system DPLL for GPIO manual clock selection. |
| 00Dh | GPIO_0.GPIO_SLAVE | GPIO controlled device slave configuration. |
| 00Eh | GPIO_0.GPIO_ALERT_OUT_CFG | GPIO alert notification. |
| 00Fh | GPIO_0.GPIO_TOD_NOTIFICATION_CFG | GPIO configuration for DPLL TOD read notification. |
| 010h | GPIO_0.GPIO_CTRL | GPIO control. |

a. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

### GPIO_0.GPIO_DCO_INC_DEC

Increment/decrement DCO FFO configuration. Applies when GPIO_FUNCTION is equal to 'inc DCO FFO' or 'dec DCO FFO'. The squelch level is determined by the configuration per output by OUTPUT_n.OUT_CTR_1.SQUELCH_VALUE.

Table 303: GPIO_0.GPIO_DCO_INC_DEC Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_DCO_INC_DEC Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | RESERVED[7:3] | | | | | DPLL_INDEX[2:0] | | |

| GPIO_0.GPIO_DCO_INC_DEC Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL_INDEX[2:0] | R/W | 0 | DPLL index.<br>Select the DPLL to be controlled by this GPIO in incremental/decremental mode.<br>0 = DPLL0<br>1 = DPLL1<br>2 = DPLL2<br>3 = DPLL3<br>4 = DPLL4<br>5 = DPLL5<br>6 = DPLL6<br>7 = DPLL7 |

### GPIO_0.GPIO_OUT_CTRL_0

Define the set of outputs to be squelched by this GPIO input. Applies when GPIO_FUNCTION is equal to 'clock output control'. The squelch level is determined by OUTPUT_n.OUT_CTRL_1.SQUELCH_VALUE. One output cannot be controlled by more than one GPIO.

Table 304: GPIO_0.GPIO_OUT_CTRL_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_OUT_CTRL_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 001h | CTRL_OUT_7[7] | CTRL_OUT_6[6] | CTRL_OUT_5[5] | CTRL_OUT_4[4] | CTRL_OUT_3[3] | CTRL_OUT_2[2] | CTRL_OUT_1[1] | CTRL_OUT_0[0] |

| GPIO_0.GPIO_OUT_CTRL_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| CTRL_OUT_7[7] | R/W | 0 | Select output 7 to be controlled by this GPIO.<br>GPIO is used to disable (squelch) output 7.<br>0 = disabled<br>1 = enabled |
| CTRL_OUT_6[6] | R/W | 0 | Select output 6 to be controlled by this GPIO.<br>GPIO is used to disable (squelch) output 6.<br>0 = disabled<br>1 = enabled |
| CTRL_OUT_5[5] | R/W | 0 | Select output 5 to be controlled by this GPIO.<br>GPIO is used to disable (squelch) output 5.<br>0 = disabled<br>1 = enabled |
| CTRL_OUT_4[4] | R/W | 0 | Select output 4 to be controlled by this GPIO.<br>GPIO is used to disable (squelch) output 4.<br>0 = disabled<br>1 = enabled |
| CTRL_OUT_3[3] | R/W | 0 | Select output 3 to be controlled by this GPIO.<br>GPIO is used to disable (squelch) output 3.<br>0 = disabled<br>1 = enabled |
| CTRL_OUT_2[2] | R/W | 0 | Select output 2 to be controlled by this GPIO.<br>GPIO is used to disable (squelch) output 2.<br>0 = disabled<br>1 = enabled |
| CTRL_OUT_1[1] | R/W | 0 | Select output 1 to be controlled by this GPIO.<br>GPIO is used to disable (squelch) output 1.<br>0 = disabled<br>1 = enabled |
| CTRL_OUT_0[0] | R/W | 0 | Select output 0 to be controlled by this GPIO.<br>GPIO is used to disable (squelch) output 0.<br>0 = disabled<br>1 = enabled |

### GPIO_0.GPIO_OUT_CTRL_1

Define the set of outputs to be squelched by this GPIO input. Applies when GPIO_FUNCTION is equal to 'clock output control'. The squelch level is determined by OUTPUT_n.OUT_CTRL_1.SQUELCH_VALUE. One output cannot be controlled by more than one GPIO.

Table 305: GPIO_0.GPIO_OUT_CTRL_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_OUT_CTRL_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | RESERVED[7:4] | | | | CTRL_OUT_11[3] | CTRL_OUT_10[2] | CTRL_OUT_9[1] | CTRL_OUT_8[0] |

| GPIO_0.GPIO_OUT_CTRL_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| CTRL_OUT_11[3] | R/W | 0 | Select output 11 to be controlled by this GPIO.<br>GPIO is used to disable (squelch) output 11.<br>0 = disabled<br>1 = enabled |
| CTRL_OUT_10[2] | R/W | 0 | Select output 10 to be controlled by this GPIO.<br>GPIO is used to disable (squelch) output 10.<br>0 = disabled<br>1 = enabled |
| CTRL_OUT_9[1] | R/W | 0 | Select output 9 to be controlled by this GPIO.<br>GPIO is used to disable (squelch) output 9.<br>0 = disabled<br>1 = enabled |
| CTRL_OUT_8[0] | R/W | 0 | Select output 8 to be controlled by this GPIO.<br>GPIO is used to disable (squelch) output 8.<br>0 = disabled<br>1 = enabled |

### GPIO_0.GPIO_TOD_TRIG

Select which TOD register to be triggered by this GPIO. Applies when GPIO_FUNCTION is equal to 'TOD trigger'.

Table 306: GPIO_0.GPIO_TOD_TRIG Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_TOD_TRIG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 003h | RESERVED[7:4] | | | | TOD_TRIG_3[3] | TOD_TRIG_2[2] | TOD_TRIG_1[1] | TOD_TRIG_0[0] |

| GPIO_0.GPIO_TOD_TRIG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| TOD_TRIG_3[3] | R/W | 0 | Select TOD of DPLL 3 to be triggered by this GPIO.<br>The TOD read/write operation is triggered on the rising edge of this GPIO. The tod_write_selection or tod_read_trigger for TOD 3 has to be equal to 'Selected GPIO'.<br>CAUTION: if more than one GPIO is used to trigger the same TOD, the behaviour is undefined.<br>0 = disabled<br>1 = enabled |

| GPIO_0.GPIO_TOD_TRIG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| TOD_TRIG_2[2] | R/W | 0 | Select TOD of DPLL 2 to be triggered by this GPIO.<br>The TOD read/write operation is triggered on the rising edge of this GPIO. The tod_write_selection or tod_read_trigger for TOD 2 has to be equal to 'Selected GPIO'.<br>CAUTION: if more than one GPIO is used to trigger the same TOD, the behaviour is undefined.<br>0 = disabled<br>1 = enabled |
| TOD_TRIG_1[1] | R/W | 0 | Select TOD of DPLL 1 to be triggered by this GPIO.<br>The TOD read/write operation is triggered on the rising edge of this GPIO. The tod_write_selection or tod_read_trigger for TOD 1 has to be equal to 'Selected GPIO'.<br>CAUTION: if more than one GPIO is used to trigger the same TOD, the behaviour is undefined.<br>0 = disabled<br>1 = enabled |
| TOD_TRIG_0[0] | R/W | 0 | Select TOD of DPLL 0 to be triggered by this GPIO.<br>The TOD read/write operation is triggered on the rising edge of this GPIO. The tod_write_selection or tod_read_trigger for TOD 0 has to be equal to 'Selected GPIO'.<br>CAUTION: if more than one GPIO is used to trigger the same TOD, the behaviour is undefined.<br>0 = disabled<br>1 = enabled |

### GPIO_0.GPIO_DPLL_INDICATOR

Select the DPLL to be used to drive this GPIO. Applies when GPIO_FUNCTION is equal to 'lock indicator' or 'holdover indicator'. In case of 'lock indicator', if the DPLL is in synthesizer mode, then the GPIO indicates the live status of the System APLL.

Table 307: GPIO_0.GPIO_DPLL_INDICATOR Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_DPLL_INDICATOR Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | RESERVED[7:4] | | | | DPLL_INDEX[3:0] | | | |

| GPIO_0.GPIO_DPLL_INDICATOR Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL_INDEX[3:0] | R/W | 0 | DPLL index used by lock indicator or holdover indicator function.<br>The GPIO level is active when the DPLL is in locked state when GPIO_n.GPIO_FUNCTION = lock indicator.<br>The GPIO level is active when the DPLL is in holdover state when GPIO_n.GPIO_FUNCTION = holdover indicator.<br><br>0 = DPLL0<br>1 = DPLL1<br>2 = DPLL2<br>3 = DPLL3<br>4 = DPLL4<br>5 = DPLL5<br>6 = DPLL6<br>7 = DPLL7<br>8 = SYS_DPLL |

### GPIO_0.GPIO_LOS_INDICATOR

Configure the GPIO LOS indicator. Applies when GPIO_FUNCTION is equal to 'LOS indicator'.

Table 308: GPIO_0.GPIO_LOS_INDICATOR Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_LOS_INDICATOR Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 005h | RESERVED[7:5] | | | ACTIVE_LEVEL[4] | REFMON_INDEX[3:0] | | | |

| GPIO_0.GPIO_LOS_INDICATOR Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| ACTIVE_LEVEL[4] | R/W | 0 | Level of active GPIO LOS indicator.<br>0 = active low<br>1 = active high |
| REFMON_INDEX[3:0] | R/W | 0 | Reference monitor index.<br>Select the reference monitor which raises the LOS alarm. |

### GPIO_0.GPIO_REF_INPUT_DSQ_0

Select the set of inputs to be disqualified when the GPIO is at the configured level. Applies when GPIO_FUNCTION is equal to 'input clock disqualify'.

Table 309: GPIO_0.GPIO_REF_INPUT_DSQ_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_REF_INPUT_DSQ_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 006h | DSQ_INP_7[7] | DSQ_INP_6[6] | DSQ_INP_5[5] | DSQ_INP_4[4] | DSQ_INP_3[3] | DSQ_INP_2[2] | DSQ_INP_1[1] | DSQ_INP_0[0] |

| GPIO_0.GPIO_REF_INPUT_DSQ_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DSQ_INP_7[7] | R/W | 0 | Select input 7 to be disqualified by this GPIO.<br>GPIO is used to disqualify input 7.<br>0 = disabled<br>1 = enabled |
| DSQ_INP_6[6] | R/W | 0 | Select input 6 to be disqualified by this GPIO.<br>GPIO is used to disqualify input 6.<br>0 = disabled<br>1 = enabled |
| DSQ_INP_5[5] | R/W | 0 | Select input 5 to be disqualified by this GPIO.<br>GPIO is used to disqualify input 5.<br>0 = disabled<br>1 = enabled |
| DSQ_INP_4[4] | R/W | 0 | Select input 4 to be disqualified by this GPIO.<br>GPIO is used to disqualify input 4.<br>0 = disabled<br>1 = enabled |
| DSQ_INP_3[3] | R/W | 0 | Select input 3 to be disqualified by this GPIO.<br>GPIO is used to disqualify input 3.<br>0 = disabled<br>1 = enabled |
| DSQ_INP_2[2] | R/W | 0 | Select input 2 to be disqualified by this GPIO.<br>GPIO is used to disqualify input 2.<br>0 = disabled<br>1 = enabled |
| DSQ_INP_1[1] | R/W | 0 | Select input 1 to be disqualified by this GPIO.<br>GPIO is used to disqualify input 1.<br>0 = disabled<br>1 = enabled |
| DSQ_INP_0[0] | R/W | 0 | Select input 0 to be disqualified by this GPIO.<br>GPIO is used to disqualify input 0.<br>0 = disabled<br>1 = enabled |

### GPIO_0.GPIO_REF_INPUT_DSQ_1

Select the set of inputs to be disqualified when the GPIO is at the configured level. Applies when GPIO_FUNCTION is equal to 'input clock disqualify'.

Table 310: GPIO_0.GPIO_REF_INPUT_DSQ_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_REF_INPUT_DSQ_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 007h | DSQ_INP_15 [7] | DSQ_INP_14 [6] | DSQ_INP_13 [5] | DSQ_INP_12 [4] | DSQ_INP_11 [3] | DSQ_INP_10 [2] | DSQ_INP_9[ 1] | DSQ_INP_8[ 0] |

| GPIO_0.GPIO_REF_INPUT_DSQ_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DSQ_INP_15[7] | R/W | 0 | Select input 15 to be disqualified by this GPIO.<br>GPIO is used to disqualify input 15.<br>0 = disabled<br>1 = enabled |
| DSQ_INP_14[6] | R/W | 0 | Select input 14 to be disqualified by this GPIO.<br>GPIO is used to disqualify input 14.<br>0 = disabled<br>1 = enabled |
| DSQ_INP_13[5] | R/W | 0 | Select input 13 to be disqualified by this GPIO.<br>GPIO is used to disqualify input 13.<br>0 = disabled<br>1 = enabled |
| DSQ_INP_12[4] | R/W | 0 | Select input 12 to be disqualified by this GPIO.<br>GPIO is used to disqualify input 12.<br>0 = disabled<br>1 = enabled |
| DSQ_INP_11[3] | R/W | 0 | Select input 11 to be disqualified by this GPIO.<br>GPIO is used to disqualify input 11.<br>0 = disabled<br>1 = enabled |
| DSQ_INP_10[2] | R/W | 0 | Select input 10 to be disqualified by this GPIO.<br>GPIO is used to disqualify input 10.<br>0 = disabled<br>1 = enabled |
| DSQ_INP_9[1] | R/W | 0 | Select input 9 to be disqualified by this GPIO.<br>GPIO is used to disqualify input 9.<br>0 = disabled<br>1 = enabled |
| DSQ_INP_8[0] | R/W | 0 | Select input 8 to be disqualified by this GPIO.<br>GPIO is used to disqualify input 8.<br>0 = disabled<br>1 = enabled |

### GPIO_0.GPIO_REF_INPUT_DSQ_2

Select the set of DPLLs to have inputs disqualified when the GPIO is at the configured level. Applies when GPIO_FUNCTION is equal to 'input clock disqualify'.

Table 311: GPIO_0.GPIO_REF_INPUT_DSQ_2 Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_REF_INPUT_DSQ_2 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 008h | DSQ_DPLL_7[7] | DSQ_DPLL_6[6] | DSQ_DPLL_5[5] | DSQ_DPLL_4[4] | DSQ_DPLL_3[3] | DSQ_DPLL_2[2] | DSQ_DPLL_1[1] | DSQ_DPLL_0[0] |

| GPIO_0.GPIO_REF_INPUT_DSQ_2 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DSQ_DPLL_7[7] | R/W | 0 | Select DPLL 7.<br>GPIO is used to disqualify selected inputs for DPLL 7.<br>0 = disabled<br>1 = enabled |
| DSQ_DPLL_6[6] | R/W | 0 | Select DPLL 6.<br>GPIO is used to disqualify selected inputs for DPLL 6.<br>0 = disabled<br>1 = enabled |
| DSQ_DPLL_5[5] | R/W | 0 | Select DPLL 5.<br>GPIO is used to disqualify selected inputs for DPLL 5.<br>0 = disabled<br>1 = enabled |
| DSQ_DPLL_4[4] | R/W | 0 | Select DPLL 4.<br>GPIO is used to disqualify selected inputs for DPLL 4.<br>0 = disabled<br>1 = enabled |
| DSQ_DPLL_3[3] | R/W | 0 | Select DPLL 3.<br>GPIO is used to disqualify selected inputs for DPLL 3.<br>0 = disabled<br>1 = enabled |
| DSQ_DPLL_2[2] | R/W | 0 | Select DPLL 2.<br>GPIO is used to disqualify selected inputs for DPLL 2.<br>0 = disabled<br>1 = enabled |
| DSQ_DPLL_1[1] | R/W | 0 | Select DPLL 1.<br>GPIO is used to disqualify selected inputs for DPLL 1.<br>0 = disabled<br>1 = enabled |
| DSQ_DPLL_0[0] | R/W | 0 | Select DPLL 0.<br>GPIO is used to disqualify selected inputs for DPLL 0.<br>0 = disabled<br>1 = enabled |

### GPIO_0.GPIO_REF_INPUT_DSQ_3

Select the system DPLL to have its input disqualified when the GPIO is at the configured level. Applies when GPIO_FUNCTION is equal to 'input clock disqualify'.

Table 312: GPIO_0.GPIO_REF_INPUT_DSQ_3 Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_REF_INPUT_DSQ_3 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 009h | RESERVED[7:2] | | | | | | GPIO_DSQ_LEVEL[1] | DSQ_DPLL_SYS[0] |

| GPIO_0.GPIO_REF_INPUT_DSQ_3 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| GPIO_DSQ_LEVEL[1] | R/W | 0 | Indicates the GPIO level used to disqualify the selected inputs.<br>0 = low<br>1 = high |
| DSQ_DPLL_SYS[0] | R/W | 0 | Select system DPLL.<br>GPIO is used to disqualify selected inputs for system DPLL.<br>0 = disabled<br>1 = enabled |

### GPIO_0.GPIO_MAN_CLK_SEL_0

Switch between the configured input using this GPIO. Applies when GPIO_FUNCTION is equal to 'manual clock select'.

Table 313: GPIO_0.GPIO_MAN_CLK_SEL_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_MAN_CLK_SEL_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ah | ACTIVE_CLK_INDEX[7:4] | | | | INACTIVE_CLK_INDEX[3:0] | | | |

| GPIO_0.GPIO_MAN_CLK_SEL_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| ACTIVE_CLK_INDEX[7:4] | R/W | 0 | Input index.<br>Select input to be used when GPIO input is one (high). |
| INACTIVE_CLK_INDEX[3:0] | R/W | 0 | Input index.<br>Select input to be used when GPIO input is zero (low). |

### GPIO_0.GPIO_MAN_CLK_SEL_1

Applies when GPIO_FUNCTION is equal to 'manual clock select'.

Table 314: GPIO_0.GPIO_MAN_CLK_SEL_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_MAN_CLK_SEL_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Bh | DPLL7[7] | DPLL6[6] | DPLL5[5] | DPLL4[4] | DPLL3[3] | DPLL2[2] | DPLL1[1] | DPLL0[0] |

| GPIO_0.GPIO_MAN_CLK_SEL_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DPLL7[7] | R/W | 0 | Select DPLL 7.<br>GPIO is used to select the input for DPLL 7.<br>0 = disabled<br>1 = enabled |
| DPLL6[6] | R/W | 0 | Select DPLL 6.<br>GPIO is used to select the input for DPLL 6.<br>0 = disabled<br>1 = enabled |
| DPLL5[5] | R/W | 0 | Select DPLL 5.<br>GPIO is used to select the input for DPLL 5.<br>0 = disabled<br>1 = enabled |
| DPLL4[4] | R/W | 0 | Select DPLL 4.<br>GPIO is used to select the input for DPLL 4.<br>0 = disabled<br>1 = enabled |
| DPLL3[3] | R/W | 0 | Select DPLL 3.<br>GPIO is used to select the input for DPLL 3.<br>0 = disabled<br>1 = enabled |
| DPLL2[2] | R/W | 0 | Select DPLL 2.<br>GPIO is used to select the input for DPLL 2.<br>0 = disabled<br>1 = enabled |
| DPLL1[1] | R/W | 0 | Select DPLL 1.<br>GPIO is used to select the input for DPLL 1.<br>0 = disabled<br>1 = enabled |
| DPLL0[0] | R/W | 0 | Select DPLL 0.<br>GPIO is used to select the input for DPLL 0.<br>0 = disabled<br>1 = enabled |

### GPIO_0.GPIO_MAN_CLK_SEL_2

Applies when GPIO_FUNCTION is equal to 'manual clock select'.

Table 315: GPIO_0.GPIO_MAN_CLK_SEL_2 Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_MAN_CLK_SEL_2 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ch | RESERVED[7:1] | | | | | | | DPLL_SYS[0] |

| GPIO_0.GPIO_MAN_CLK_SEL_2 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL_SYS[0] | R/W | 0 | Select system DPLL.<br>GPIO is used to select the input for system DPLL.<br>0 = disabled<br>1 = enabled |

### GPIO_0.GPIO_SLAVE

Configure the GPIO slave active level.

Table 316: GPIO_0.GPIO_SLAVE Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_SLAVE Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Dh | RESERVED[7:1] | | | | | | | GPIO_SLAVE_LEVEL[0] |

| GPIO_0.GPIO_SLAVE Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| GPIO_SLAVE_LEVEL[0] | R/W | 0 | Indicates the GPIO level for slave mode.<br>0 = switch to slave mode when GPIO is low<br>1 = switch to slave mode when GPIO is high |

### GPIO_0.GPIO_ALERT_OUT_CFG

Configure the GPIO alert active level.

Table 317: GPIO_0.GPIO_ALERT_OUT_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_ALERT_OUT_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Eh | RESERVED[7:1] | | | | | | | GPIO_ALERT_OUT_LEVEL[0] |

| GPIO_0.GPIO_ALERT_OUT_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| GPIO_ALERT_OUT_LEVEL[0] | R/W | 0 | GPIO alert out active level.<br>0 = active low<br>1 = active high |

### GPIO_0.GPIO_TOD_NOTIFICATION_CFG

Enable the TOD Read notification for a GPIO.

Table 318: GPIO_0.GPIO_TOD_NOTIFICATION_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_TOD_NOTIFICATION_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Fh | RESERVED[7:4] | | | | GPIO_ASSERT_LEVEL[3] | TOD_READ_SECONDARY[2] | DPLL_TOD[1:0] | |

| GPIO_0.GPIO_TOD_NOTIFICATION_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| GPIO_ASSERT_LEVEL[3] | R/W | 0 | Indicates the level to drive the GPIO pin when a TOD read trigger event has occurred.<br>0 = active low<br>1 = active high |

| GPIO_0.GPIO_TOD_NOTIFICATION_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| TOD_READ_SECONDARY[2] | R/W | 0 | Select the primary or secondary TOD read registers.<br>The GPIO level becomes active after the TOD register is updated.<br>0 = ToD read primary<br>1 = ToD read secondary |
| DPLL_TOD[1:0] | R/W | 0 | DPLL TOD index.<br>Select the DPLL whose TOD register has been read.<br>0 = DPLL0<br>1 = DPLL1<br>2 = DPLL2<br>3 = DPLL3 |

### GPIO_0.GPIO_CTRL

Enable GPIO and configure GPIO mode and direction.

TRIGGER: Writing to this byte triggers a read and activation in hardware of all the bytes of the GPIO module.

Table 319: GPIO_0.GPIO_CTRL Bit Field Locations and Descriptions

| Offset Address (Hex) | GPIO_0.GPIO_CTRL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 010h | GPIO_FUNCTION[7:4] | | | | GPIO_PU_PD_MODE[3] | GPIO_CONTROL_DIR[2] | GPIO_CMOS_OD_MODE[1] | GPIO_FUNCTION_EN[0] |

| GPIO_0.GPIO_CTRL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| GPIO_FUNCTION[7:4] | R/W | 0 | Select GPIO function.<br>Selects which GPIO function to perform.<br>0x0 = lock indicator (out)<br>0x1 = holdover indicator (out)<br>0x2 = LOS indicator (out)<br>0x3 = alert out (out)<br>0x4 = inc DCO FFO (in)<br>0x5 = dec DCO FFO (in)<br>0x6 = input clock disqualify (in)<br>0x7 = manual clock select (in)<br>0x8 = reserved<br>0x9 = clock output control (in)<br>0xA = ToD trigger (in)<br>0xB = ToD read notification (out)<br>0xC = master/slave signal (in) |
| GPIO_PU_PD_MODE[3] | R/W | 0 | Select pull-up or pull-down.<br>Applies when GPIO direction is Input.<br>0 = pu<br>1 = pd |
| GPIO_CONTROL_DIR[2] | R/W | 0 | Select GPIO direction.<br>Applies when GPIO function mode is disabled.<br>0 = input<br>1 = output |
| GPIO_CMOS_OD_MODE[1] | R/W | 0 | Select CMOS or open drain.<br>0 = cmos<br>1 = open drain |
| GPIO_FUNCTION_EN[0] | R/W | 0 | Enable GPIO function mode.<br>0 = disabled<br>1 = enabled |

## Module: OUT_DIV_MUX

TRIGGER: Every register in this module is a trigger register. In the case of a multibyte register the highest address register byte is the trigger byte.

Table 320: OUT_DIV_MUX Register Index

| Offset (Hex) | Register Module Base Address: CA12h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | OUT_DIV_MUX.OUT_DIV8_MUX | Output divider 8 multiplexer. |
| 001h | OUT_DIV_MUX.OUT_DIV11_MUX | Output divider 11 multiplexer. |

### OUT_DIV_MUX.OUT_DIV8_MUX

Output divider 8 multiplexer configuration.

Table 321: OUT_DIV_MUX.OUT_DIV8_MUX Bit Field Locations and Descriptions

| Offset Address (Hex) | OUT_DIV_MUX.OUT_DIV8_MUX Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | RESERVED[7:1] | | | | | | | FOD5_TO_OUT_DIV8[0] |

| OUT_DIV_MUX.OUT_DIV8_MUX Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| FOD5_TO_OUT_DIV8[0] | R/W | 0 | Enable the connection between FOD 5 and output divider 8.<br>Selects FOD 5 as the driver for the clock and sync for output divider 8.<br>In normal mode, FOD 4 drives output divider 8, and FOD 5 drives output divider 9.<br>In coupled mode, FOD 5 drives both output divider 8 and 9.<br>0 = normal<br>1 = coupled |

### OUT_DIV_MUX.OUT_DIV11_MUX

Output divider 11 multiplexer configuration.

Table 322: OUT_DIV_MUX.OUT_DIV11_MUX Bit Field Locations and Descriptions

| Offset Address (Hex) | OUT_DIV_MUX.OUT_DIV11_MUX Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 001h | RESERVED[7:1] | | | | | | | FOD6_TO_OUT_DIV11[0] |

| OUT_DIV_MUX.OUT_DIV11_MUX Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| FOD6_TO_OUT_DIV11[0] | R/W | 0 | Enable the connection between FOD 6 and output divider 11.<br>Selects FOD 6 as the driver for the clock and sync for output divider 11.<br>In normal mode, FOD 6 drives output divider 10, and FOD 7 drives output divider 11.<br>In coupled mode, FOD 6 drives both output divider 10 and 11.<br>0 = normal<br>1 = coupled |

## Module: OUTPUT_0

TRIGGER: Every register in this module is a trigger register. In the case of a multibyte register the highest address register byte is the trigger byte.

Table 323: OUTPUT_0 Register Index

| Offset (Hex) | Register Module Base Address: CA14h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | OUTPUT_0.OUT_DIV | Output divider value. |
| 004h | OUTPUT_0.OUT_DUTY_CYCLE_HIGH | Output duty cycle. |
| 008h | OUTPUT_0.OUT_CTRL_0 | Output electrical characteristics. |
| 009h | OUTPUT_0.OUT_CTRL_1 | Output electrical characteristics. |
| 00Ch | OUTPUT_0.OUT_PHASE_ADJ | Output phase adjustment. |

a. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

### OUTPUT_0.OUT_DIV

The output clock frequency is the FOD frequency divided by the output divider value.

Table 324: OUTPUT_0.OUT_DIV Bit Field Locations and Descriptions

| Offset Address (Hex) | OUTPUT_0.OUT_DIV Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | OUT_DIV[7:0] | | | | | | | |
| 001h | OUT_DIV[15:8] | | | | | | | |
| 002h | OUT_DIV[23:16] | | | | | | | |
| 003h | OUT_DIV[31:24] | | | | | | | |

| OUTPUT_0.OUT_DIV Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| OUT_DIV[31:0] | R/W | 0 | Unsigned 32-bit output divider value. |

### OUTPUT_0.OUT_DUTY_CYCLE_HIGH

Sets the output duty cycle high value

Table 325: OUTPUT_0.OUT_DUTY_CYCLE_HIGH Bit Field Locations and Descriptions

| Offset Address (Hex) | OUTPUT_0.OUT_DUTY_CYCLE_HIGH Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | OUT_DUTY_CYCLE_HIGH[7:0] | | | | | | | |
| 005h | OUT_DUTY_CYCLE_HIGH[15:8] | | | | | | | |
| 006h | OUT_DUTY_CYCLE_HIGH[23:16] | | | | | | | |
| 007h | OUT_DUTY_CYCLE_HIGH[31:24] | | | | | | | |

| OUTPUT_0.OUT_DUTY_CYCLE_HIGH Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| OUT_DUTY_CYCLE_HIGH[31:0] | R/W | 0 | Unsigned 32-bit divider high value.<br>The divider high value determines the high pulse width. The duty cycle is: dc_high / (out_div - dc_high). If dc_high = 0, the duty cycle is 50 / 50. |

### OUTPUT_0.OUT_CTRL_0

Configure output pad electrical characteristics.

Meet JEDEC compliance with LVDS operation by setting OUT_CTRL_0.PAD_VSWING = 0 and OUT_CTRL_0.PAD_VOS = 2.

Meet JEDEC compliance with 2.5 LVPECL operation by setting OUT_CTRL_0.PAD_VSWING = 2 and OUT_CTRL_0.PAD_VOS = 0.

Meet JEDEC compliance with 3.3 LVPECL operation by setting OUT_CTRL_0.PAD_VSWING = 2 and OUT_CTRL_0.PAD_VOS = 4.

Table 326: OUTPUT_0.OUT_CTRL_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | OUTPUT_0.OUT_CTRL_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 008h | PAD_VOS[7:5] | | | PAD_VSWING[4:3] | | PAD_MODE[2:0] | | |

| OUTPUT_0.OUT_CTRL_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PAD_VOS[7:5] | R/W | 0 | Output common mode voltage.<br>0 = 0.9V<br>1 = 1.1V<br>2 = 1.3V<br>3 = 1.5V<br>4 = 1.7V<br>5 = 1.9V<br>6 = 2.1V<br>7 = 2.3V |
| PAD_VSWING[4:3] | R/W | 0 | Output single-ended voltage swing.<br>0 = 410mV<br>1 = 600mV<br>2 = 750mV<br>3 = 900mV |
| PAD_MODE[2:0] | R/W | 0 | Output mode.<br>0 = high-Z<br>1 = differential<br>2 = LVCMOS, inverted<br>3 = LVCMOS, in-phase<br>4 = reserved<br>5 = reserved<br>6 = LVCMOS, Q enabled, nQ High-Z<br>7 = reserved |

### OUTPUT_0.OUT_CTRL_1

Configure output pad electrical characteristics.

Table 327: OUTPUT_0.OUT_CTRL_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | OUTPUT_0.OUT_CTRL_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 009h | OUT_SYNC_DISABLE[7] | SQUELCH_VALUE[6] | SQUELCH_DISABLE[5] | PAD_VDDO[4:2] | | | PAD_CMOSDRV[1:0] | |

| OUTPUT_0.OUT_CTRL_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| OUT_SYNC_DISABLE[7] | R/W | 0 | Output phase synchronization disable.<br>0 = enable<br>1 = disable |
| SQUELCH_VALUE[6] | R/W | 0 | Squelch value.<br>0 = low<br>1 = high |

| OUTPUT_0.OUT_CTRL_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SQUELCH_DISABLE[5] | R/W | 0 | Enable or disable output squelch.<br>0 = squelch enabled<br>1 = squelch disabled |
| PAD_VDDO[4:2] | R/W | 0 | VDDO level.<br>0 = 1.8V<br>1 = 3.3V<br>2 = 2.5V<br>3 = 1.5V<br>4 = 1.2V |
| PAD_CMOSDRV[1:0] | R/W | 0 | LVCMOS output impedance enumeration (Ohm).<br>0 = 38 (3.3V), 44 (2.5V), 60 (1.8V), 85 (1.5V), 140 (1.2V)<br>1 = 25 (3.3V), 29 (2.5V), 40 (1.8V), 48 (1.5V), 100 (1.2V)<br>2 = 18 (3.3V), 20 (2.5V), 29 (1.8V), 40 (1.5V), 65 (1.2V)<br>3 = 15 (3.3V), 16 (2.5V), 23 (1.8V), 29 (1.5V), 50 (1.2V) |

### OUTPUT_0.OUT_PHASE_ADJ

Output phase adjustment in FOD cycles.

Table 328: OUTPUT_0.OUT_PHASE_ADJ Bit Field Locations and Descriptions

| Offset Address (Hex) | OUTPUT_0.OUT_PHASE_ADJ Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ch | OUT_PHASE_ADJ[7:0] | | | | | | | |
| 00Dh | OUT_PHASE_ADJ[15:8] | | | | | | | |
| 00Eh | OUT_PHASE_ADJ[23:16] | | | | | | | |
| 00Fh | OUT_PHASE_ADJ[31:24] | | | | | | | |

| OUTPUT_0.OUT_PHASE_ADJ Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| OUT_PHASE_ADJ[31:0] | R/W | 0 | Signed 32-bit value in FOD cycles to apply a phase shift to the output clock. |

## Module: SERIAL

Configure the serial communication ports.

Table 329: SERIAL Register Index

| Offset (Hex) | Register Module Base Address: CAE0h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | SERIAL.I2CM | I2C Master configuration. |
| 001h | RESERVED | This register must not be modified from the read value |
| 002h | SERIAL.SER0 | Slave serial interface 0 (main serial port) configuration. |
| 003h | SERIAL.SER0_SPI | SPI configuration for serial interface 0 (main serial port). |
| 004h | SERIAL.SER0_I2C | I2C configuration for serial interface 0 (main serial port). |
| 005h | SERIAL.SER1 | Slave serial interface 1 (auxiliary serial port) configuration. |
| 006h | SERIAL.SER1_SPI | SPI configuration for serial interface 1 (auxiliary serial port). |
| 007h | SERIAL.SER1_I2C | I2C configuration for serial interface 1 (auxiliary serial port). |
| 008h | SERIAL.SER_APPLY_CONFIG | Trigger serial configuration changes. |

### SERIAL.I2CM

I2C Master configuration.

Table 330: SERIAL.I2CM Bit Field Locations and Descriptions

| Offset Address (Hex) | SERIAL.I2CM Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | RESERVED[7:2] | | | | | | I2CM_PORT_SEL[1:0] | |

| SERIAL.I2CM Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| I2CM_PORT_SEL[1:0] | R/W | 0 | I2C Master port pin selection.<br>Configure the pins the I2C master block should connect to.<br>0 = I2C master<br>1 = serial interface 0<br>2 = serial interface 1 |

### SERIAL.SER0

Slave serial interface 0 (main serial port) configuration.

Table 331: SERIAL.SER0 Bit Field Locations and Descriptions

| Offset Address (Hex) | SERIAL.SER0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | RESERVED[7:3] | | | | | ADDRESS_SIZE[2] | MODE[1:0] | |

| SERIAL.SER0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| ADDRESS_SIZE[2] | R/W | 0 | Serial interface 0 (main serial port) address size.<br>0 = 1-byte<br>1 = 2-byte |
| MODE[1:0] | R/W | 0 | Serial interface 0 (main serial port) mode.<br>Set MODE = 0 to maintain current configuration (e.g. mode indicated by SER0_STATUS_MODE field will remain the same).<br>0 = no change<br>1 = I2C<br>2 = SPI<br>3 = disabled |

### SERIAL.SER0_SPI

SPI configuration for serial interface 0 (main serial port).

Table 332: SERIAL.SER0_SPI Bit Field Locations and Descriptions

| Offset Address (Hex) | SERIAL.SER0_SPI Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 003h | RESERVED[7:5] | | | SPI_SDO_DELAY[4] | SPI_CLOCK_SELECTION[3] | SPI_DUPLEX_MODE[2] | RESERVED[1:0] | |

| SERIAL.SER0_SPI Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SPI_SDO_DELAY[4] | R/W | 0 | SPI delay SDO driving edge.<br>0 = driving edge used for SDO<br>1 = SDO driving edge delayed half-cycle of SCLK |
| SPI_CLOCK_SELECTION[3] | R/W | 0 | SPI Clock Selection for SDI sampling.<br>0 = rising edge<br>1 = falling edge |

| SERIAL.SER0_SPI Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SPI_DUPLEX_MODE[2] | R/W | 0 | SPI 4-wire or 3-wire.<br>Select either 4-wire full duplex mode or 3-wire half duplex mode.<br>0 = full duplex<br>1 = half duplex |
| RESERVED | N/A | - | This field must not be modified from the read value |

### SERIAL.SER0_I2C

I2C configuration for serial interface 0 (main serial port).

Table 333: SERIAL.SER0_I2C Bit Field Locations and Descriptions

| Offset Address (Hex) | SERIAL.SER0_I2C Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | APPLY[7] | DEVICE_ADDRESS[6:0] | | | | | | |

| SERIAL.SER0_I2C Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| APPLY[7] | R/W | 0 | Apply the new I2C address when the confirmation code triggers configuration to serial interface 0 (main serial port).<br>0 = do not change<br>1 = apply new address |
| DEVICE_ADDRESS[6:0] | R/W | 0 | 7-bit I2C address. |

### SERIAL.SER1

Slave serial interface 1 (auxiliary serial port) configuration.

Table 334: SERIAL.SER1 Bit Field Locations and Descriptions

| Offset Address (Hex) | SERIAL.SER1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 005h | RESERVED[7:3] | | | | | ADDRESS_SIZE[2] | MODE[1:0] | |

| SERIAL.SER1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |

| SERIAL.SER1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| ADDRESS_SIZE[2] | R/W | 0 | Serial interface 1 (auxiliary serial port) address size.<br>0 = 1-byte<br>1 = 2-byte |
| MODE[1:0] | R/W | 0 | Serial interface 1 (auxiliary serial port) mode.<br>Set MODE = 0 to maintain current configuration (e.g. mode indicated by SER1_STATUS_MODE field will remain the same).<br>0 = no change<br>1 = I2C<br>2 = SPI<br>3 = disabled |

### SERIAL.SER1_SPI

SPI configuration for serial interface 1 (auxiliary serial port).

Table 335: SERIAL.SER1_SPI Bit Field Locations and Descriptions

| Offset Address (Hex) | SERIAL.SER1_SPI Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 006h | RESERVED[7:5] | | | SPI_SDO_DELAY[4] | SPI_CLOCK_SELECTION[3] | SPI_DUPLEX_MODE[2] | RESERVED[1:0] | |

| SERIAL.SER1_SPI Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SPI_SDO_DELAY[4] | R/W | 0 | SPI delay SDO driving edge.<br>0 = driving edge used for SDO<br>1 = SDO driving edge delayed half-cycle of SCLK |
| SPI_CLOCK_SELECTION[3] | R/W | 0 | SPI Clock Selection for SDI sampling.<br>0 = rising edge<br>1 = falling edge |
| SPI_DUPLEX_MODE[2] | R/W | 0 | SPI 4-wire or 3-wire.<br>Select either 4-wire full duplex mode or 3-wire half duplex mode.<br>0 = full duplex<br>1 = half duplex |
| RESERVED | N/A | - | This field must not be modified from the read value |

### SERIAL.SER1_I2C

I2C configuration for serial interface 1 (auxiliary serial port).

Table 336: SERIAL.SER1_I2C Bit Field Locations and Descriptions

| Offset Address (Hex) | SERIAL.SER1_I2C Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 007h | APPLY[7] | DEVICE_ADDRESS[6:0] | | | | | | |

| SERIAL.SER1_I2C Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| APPLY[7] | R/W | 0 | Apply the new I2C address when the confirmation code triggers configuration to serial interface 1 (auxiliary serial port).<br>0 = do not change<br>1 = apply new address |
| DEVICE_ADDRESS[6:0] | R/W | 0 | 7-bit I2C address. |

### SERIAL.SER_APPLY_CONFIG

Confirm serial interface update.

TRIGGER: Writing to this byte triggers a read and activation of all the bytes of the SERIAL module.

Table 337: SERIAL.SER_APPLY_CONFIG Bit Field Locations and Descriptions

| Offset Address (Hex) | SERIAL.SER_APPLY_CONFIG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 008h | SER0_CONFIRM_CODE[7:4] | | | | SER1_CONFIRM_CODE[3:0] | | | |

| SERIAL.SER_APPLY_CONFIG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SER0_CONFIRM_CODE[7:4] | R/W | 0 | Confirmation code for serial interface 0 (main serial port).<br>Confirmation code must be set to 0xA to apply the new configuration to serial interface 0 (main serial port).<br>After this register has been written, wait 500 us before re-accessing the serial interface. |
| SER1_CONFIRM_CODE[3:0] | R/W | 0 | Confirmation code for serial interface 1 (auxiliary serial port).<br>Confirmation code must be set to 0xA to apply the new configuration to serial interface 1 (auxiliary serial port).<br>After this register has been written, wait 500 us before re-accessing the serial interface. |

## Module: PWM_ENCODER_0

Configure the PWM encoder.

Table 338: PWM_ENCODER_0 Register Index

| Offset (Hex) | Register Module Base Address: CB00h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | PWM_ENCODER_0.PWM_ENCODER_ID | PWM encoder identifier. |
| 001h | PWM_ENCODER_0.PWM_ENCODER_CNFG | PWM encoder configuration. |
| 002h | PWM_ENCODER_0.PWM_ENCODER_SIGNATURE_0 | PWM encoder signature configuration. |
| 003h | PWM_ENCODER_0.PWM_ENCODER_SIGNATURE_1 | PWM encoder signature configuration. |
| 004h | PWM_ENCODER_0.PWM_ENCODER_CMD | PWM encoder command. |

a. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

### PWM_ENCODER_0.PWM_ENCODER_ID

Unique identifier defined by user.

Table 339: PWM_ENCODER_0.PWM_ENCODER_ID Bit Field Locations and Descriptions

| Offset Address (Hex) | PWM_ENCODER_0.PWM_ENCODER_ID Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | ENCODER_ID[7:0] | | | | | | | |

| PWM_ENCODER_0.PWM_ENCODER_ID Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| ENCODER_ID[7:0] | R/W | 0 | Unique PWM encoder ID in the PWM network. |

### PWM_ENCODER_0.PWM_ENCODER_CNFG

Configure the outputs to be used for transmission.

Table 340: PWM_ENCODER_0.PWM_ENCODER_CNFG Bit Field Locations and Descriptions

| Offset Address (Hex) | PWM_ENCODER_0.PWM_ENCODER_CNFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 001h | RESERVED[7:4] | | | | PPS_SEL[3] | SECONDARY_OUTPUT[2] | TOD_SEL[1:0] | |

| PWM_ENCODER_0.PWM_ENCODER_CNFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| PPS_SEL[3] | R/W | 0 | Select source to trigger transmission of<br>PWM PPS frame.<br>For dual-channel PWM encoders[0:3], a value of 0 means that TOD engine selected in tod_sel field is used as a trigger source, a value of 1 means that the output not used for PWM carrier is used as a trigger source.<br>For single-channel PWM encoders[4:7], a value of 1 indicates that the Q5 output divider is used as the PPS trigger source. Please note that in this case you also need to set secondary_output = 1.<br>0 = ToD PPS<br>1 = alternate PPS |
| SECONDARY_OUTPUT[2] | R/W | 0 | Select output to be used for PWM carrier.<br>For dual-channel PWM encoders[0:3], a value of 1 indicates that the secondary output is used for PWM carrier.<br>For single-channel PWM encoders[4:7], a value of 1 indicates that the Q5 output divider is used as the PPS source. Please note that in this case you also need to set pps_sel = 1.<br>0 = primary output<br>1 = alternate output |
| TOD_SEL[1:0] | R/W | 0 | DPLL TOD index.<br>DPLL index from which the TOD PPS is to be used for transmission (when pps_sel field = 0).<br>0 = ToD index 0<br>1 = ToD index 1<br>2 = ToD index 2<br>3 = ToD index 3 |

### PWM_ENCODER_0.PWM_ENCODER_SIGNATURE_0

Select signature symbols to be transmitted in PWM signature mode. Same signature must be applied at both encoder and decoder.

Table 341: PWM_ENCODER_0.PWM_ENCODER_SIGNATURE_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | PWM_ENCODER_0.PWM_ENCODER_SIGNATURE_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | FIFTH_SYMBOL[7:6] | | SIXTH_SYMBOL[5:4] | | SEVENTH_SYMBOL[3:2] | | EIGHTH_SYMBOL[1:0] | |

| PWM_ENCODER_0.PWM_ENCODER_SIGNATURE_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FIFTH_SYMBOL[7:6] | R/W | 0 | The fifth symbol of the signature.<br>zero (25 on/75 off duty cycle clock period),<br>one (75 on/25 off duty cycle clock period),<br>space (50 on/50 off duty cycle clock period)<br>0 = zero<br>1 = one<br>2 = space |
| SIXTH_SYMBOL[5:4] | R/W | 0 | The sixth symbol of the signature.<br>zero (25 on/75 off duty cycle clock period),<br>one (75 on/25 off duty cycle clock period),<br>space (50 on/50 off duty cycle clock period)<br>0 = zero<br>1 = one<br>2 = space |
| SEVENTH_SYMBOL[3:2] | R/W | 0 | The seventh symbol of the signature.<br>zero (25 on/75 off duty cycle clock period),<br>one (75 on/25 off duty cycle clock period),<br>space (50 on/50 off duty cycle clock period)<br>0 = zero<br>1 = one<br>2 = space |
| EIGHTH_SYMBOL[1:0] | R/W | 0 | The eighth symbol of the signature.<br>zero (25 on/75 off duty cycle clock period),<br>one (75 on/25 off duty cycle clock period),<br>space (50 on/50 off duty cycle clock period)<br>0 = zero<br>1 = one<br>2 = space |

### PWM_ENCODER_0.PWM_ENCODER_SIGNATURE_1

Select signature symbols to be transmitted in PWM signature mode. Same signature must be applied at both encoder and decoder.

Table 342: PWM_ENCODER_0.PWM_ENCODER_SIGNATURE_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | PWM_ENCODER_0.PWM_ENCODER_SIGNATURE_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 003h | RESERVED[7] | FIRST_SYMBOL[6] | SECOND_SYMBOL[5:4] | | THIRD_SYMBOL[3:2] | | FOURTH_SYMBOL[1:0] | |

| PWM_ENCODER_0.PWM_ENCODER_SIGNATURE_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| FIRST_SYMBOL[6] | R/W | 0 | The first symbol of the signature.<br>zero (25 on/75 off duty cycle clock period),<br>one (75 on/25 off duty cycle clock period)<br>0 = zero<br>1 = one |
| SECOND_SYMBOL[5:4] | R/W | 0 | The second symbol of the signature.<br>zero (25 on/75 off duty cycle clock period),<br>one (75 on/25 off duty cycle clock period),<br>space (50 on/50 off duty cycle clock period)<br>0 = zero<br>1 = one<br>2 = space |
| THIRD_SYMBOL[3:2] | R/W | 0 | The third symbol of the signature.<br>zero (25 on/75 off duty cycle clock period),<br>one (75 on/25 off duty cycle clock period),<br>space (50 on/50 off duty cycle clock period)<br>0 = zero<br>1 = one<br>2 = space |
| FOURTH_SYMBOL[1:0] | R/W | 0 | The fourth symbol of the signature.<br>zero (25 on/75 off duty cycle clock period),<br>one (75 on/25 off duty cycle clock period),<br>space (50 on/50 off duty cycle clock period)<br>0 = zero<br>1 = one<br>2 = space |

### PWM_ENCODER_0.PWM_ENCODER_CMD

Enable PWM encoder, signature mode and TOD transmission.

TRIGGER: Writing to this byte triggers a read and activation of all the bytes of the PMW_ENCODER module.

Table 343: PWM_ENCODER_0.PWM_ENCODER_CMD Bit Field Locations and Descriptions

| Offset Address (Hex) | PWM_ENCODER_0.PWM_ENCODER_CMD Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | RESERVED[7:3] | | | | | TOD_TX[2] | SIGNATURE_MODE[1] | ENABLE[0] |

| PWM_ENCODER_0.PWM_ENCODER_CMD Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| TOD_TX[2] | R/W | 0 | Enable TOD transmission.<br>The TOD transmission can be enabled only if signature mode is disabled.<br>0 = disabled<br>1 = enabled |
| SIGNATURE_MODE[1] | R/W | 0 | Enable signature mode.<br>0 = disabled<br>1 = enabled |
| ENABLE[0] | R/W | 0 | Enable PWM encoder.<br>0 = disabled<br>1 = enabled |

## Module: PWM_DECODER_0

Configure PWM decoder.

Table 344: PWM_DECODER_0 Register Index

| Offset (Hex) | Register Module Base Address: CB40h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | PWM_DECODER_0.PWM_DECODER_CNFG | PWM_PPS configuration. |
| 002h | PWM_DECODER_0.PWM_DECODER_ID | PWM decoder identifier. |
| 003h | PWM_DECODER_0.PWM_DECODER_SIGNATURE_0 | PWM decoder signature configuration. |
| 004h | PWM_DECODER_0.PWM_DECODER_SIGNATURE_1 | PWM decoder signature configuration. |
| 005h | PWM_DECODER_0.PWM_DECODER_CMD | PWM decoder command. |

a. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

### PWM_DECODER_0.PWM_DECODER_CNFG

Set the rate of the PWM PPS frames and enable the internal PWM PPS signal.

Table 345: PWM_DECODER_0.PWM_DECODER_CNFG Bit Field Locations and Descriptions

| Offset Address (Hex) | PWM_DECODER_0.PWM_DECODER_CNFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | PPS_RATE[7:0] | | | | | | | |
| 001h | GENERATE_PPS[15] | PPS_RATE[14:8] | | | | | | |

| PWM_DECODER_0.PWM_DECODER_CNFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| GENERATE_PPS[15] | R/W | 0 | Generate PPS pulse.<br>0 = do not generate internal PPS<br>1 = generate internal PPS |
| PPS_RATE[14:0] | R/W | 0 | PWM PPS rate in units of 0.5 Hz. |

### PWM_DECODER_0.PWM_DECODER_ID

Unique identifier defined by user.

Table 346: PWM_DECODER_0.PWM_DECODER_ID Bit Field Locations and Descriptions

| Offset Address (Hex) | PWM_DECODER_0.PWM_DECODER_ID Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | DECODER_ID[7:0] | | | | | | | |

| PWM_DECODER_0.PWM_DECODER_ID Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DECODER_ID[7:0] | R/W | 0 | Unique PWM decoder ID in the PWM network.<br>0xFF should not be used because it is reserved for broadcast. |

### PWM_DECODER_0.PWM_DECODER_SIGNATURE_0

Select signature symbols to be received in PWM signature mode. Same signature must be applied at both encoder and decoder.

Table 347: PWM_DECODER_0.PWM_DECODER_SIGNATURE_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | PWM_DECODER_0.PWM_DECODER_SIGNATURE_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 003h | FIFTH_SYMBOL[7:6] | | SIXTH_SYMBOL[5:4] | | SEVENTH_SYMBOL[3:2] | | EIGHTH_SYMBOL[1:0] | |

| PWM_DECODER_0.PWM_DECODER_SIGNATURE_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FIFTH_SYMBOL[7:6] | R/W | 0 | The fifth symbol of the signature.<br>zero (25 on/75 off duty cycle clock period),<br>one (75 on/25 off duty cycle clock period),<br>space (50 on/50 off duty cycle clock period)<br>0 = zero<br>1 = one<br>2 = space |
| SIXTH_SYMBOL[5:4] | R/W | 0 | The sixth symbol of the signature.<br>zero (25 on/75 off duty cycle clock period),<br>one (75 on/25 off duty cycle clock period),<br>space (50 on/50 off duty cycle clock period)<br>0 = zero<br>1 = one<br>2 = space |
| SEVENTH_SYMBOL[3:2] | R/W | 0 | The seventh symbol of the signature.<br>zero (25 on/75 off duty cycle clock period),<br>one (75 on/25 off duty cycle clock period),<br>space (50 on/50 off duty cycle clock period)<br>0 = zero<br>1 = one<br>2 = space |
| EIGHTH_SYMBOL[1:0] | R/W | 0 | The eighth symbol of the signature.<br>zero (25 on/75 off duty cycle clock period),<br>one (75 on/25 off duty cycle clock period),<br>space (50 on/50 off duty cycle clock period)<br>0 = zero<br>1 = one<br>2 = space |

### PWM_DECODER_0.PWM_DECODER_SIGNATURE_1

Select signature symbols to be received in PWM signature mode. Same signature must be applied at both encoder and decoder.

Table 348: PWM_DECODER_0.PWM_DECODER_SIGNATURE_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | PWM_DECODER_0.PWM_DECODER_SIGNATURE_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | RESERVED[7] | FIRST_SYMBOL[6] | SECOND_SYMBOL[5:4] | | THIRD_SYMBOL[3:2] | | FOURTH_SYMBOL[1:0] | |

| PWM_DECODER_0.PWM_DECODER_SIGNATURE_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| FIRST_SYMBOL[6] | R/W | 0 | The first symbol of the signature.<br>zero (25 on/75 off duty cycle clock period),<br>one (75 on/25 off duty cycle clock period)<br>0 = zero<br>1 = one |
| SECOND_SYMBOL[5:4] | R/W | 0 | The second symbol of the signature.<br>zero (25 on/75 off duty cycle clock period),<br>one (75 on/25 off duty cycle clock period),<br>space (50 on/50 off duty cycle clock period)<br>0 = zero<br>1 = one<br>2 = space |
| THIRD_SYMBOL[3:2] | R/W | 0 | The third symbol of the signature.<br>zero (25 on/75 off duty cycle clock period),<br>one (75 on/25 off duty cycle clock period),<br>space (50 on/50 off duty cycle clock period)<br>0 = zero<br>1 = one<br>2 = space |
| FOURTH_SYMBOL[1:0] | R/W | 0 | The fourth symbol of the signature.<br>zero (25 on/75 off duty cycle clock period),<br>one (75 on/25 off duty cycle clock period),<br>space (50 on/50 off duty cycle clock period)<br>0 = zero<br>1 = one<br>2 = space |

### PWM_DECODER_0.PWM_DECODER_CMD

Enable PWM decoder and signature mode.

TRIGGER: Writing to this byte triggers a read and activation of all the bytes of the PMW_DECODER module.

Table 349: PWM_DECODER_0.PWM_DECODER_CMD Bit Field Locations and Descriptions

| Offset Address (Hex) | PWM_DECODER_0.PWM_DECODER_CMD Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 005h | RESERVED[7:3] | | | | | TOD_FRAME_ACCESS_EN[2] | SIGNATURE_MODE[1] | ENABLE[0] |

| PWM_DECODER_0.PWM_DECODER_CMD Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| TOD_FRAME_ACCESS_EN[2] | R/W | 0 | TOD frame external access enable<br>When this bit of all PWM decoders (decoder 0 to decoder 15) are set to 0, the received TOD frame will be discarded immediately. Otherwise, the TOD frame will be held in the FIFO for 1 second to allow external access.<br>0 = TOD frame is discarded immediately<br>1 = TOD frame is helded in FIFO for 1 second |
| SIGNATURE_MODE[1] | R/W | 0 | Enable signature mode.<br>0 = disabled<br>1 = enabled |
| ENABLE[0] | R/W | 0 | Enable PWM decoder.<br>0 = disabled<br>1 = enabled |

## Module: PWM_USER_DATA

Configures PWM user data.

Table 350: PWM_USER_DATA Register Index

| Offset (Hex) | Register Module Base Address: CBC8h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | PWM_USER_DATA.PWM_SRC_ENCODER_ID | Source PWM encoder. |
| 001h | PWM_USER_DATA.PWM_DST_DECODER_ID | Destination PWM decoder. |
| 002h | PWM_USER_DATA.PWM_USER_DATA_SIZE | The PWM user data length in bytes. |
| 003h | PWM_USER_DATA.PWM_USER_DATA_CMD_STS | PWM user data command and status register. |

### PWM_USER_DATA.PWM_SRC_ENCODER_ID

The ID of the source PWM encoder.

Table 351: PWM_USER_DATA.PWM_SRC_ENCODER_ID Bit Field Locations and Descriptions

| Offset Address (Hex) | PWM_USER_DATA.PWM_SRC_ENCODER_ID Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | ENCODER_ID[7:0] | | | | | | | |

| PWM_USER_DATA.PWM_SRC_ENCODER_ID Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| ENCODER_ID[7:0] | R/W | 0 | PWM encoder identification. |

### PWM_USER_DATA.PWM_DST_DECODER_ID

The ID of the destination PWM decoder.

Table 352: PWM_USER_DATA.PWM_DST_DECODER_ID Bit Field Locations and Descriptions

| Offset Address (Hex) | PWM_USER_DATA.PWM_DST_DECODER_ID Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 001h | DECODER_ID[7:0] | | | | | | | |

| PWM_USER_DATA.PWM_DST_DECODER_ID Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DECODER_ID[7:0] | R/W | 0 | PWM decoder identification.<br>Use 0xFF for broadcast transmission. |

### PWM_USER_DATA.PWM_USER_DATA_SIZE

-

Table 353: PWM_USER_DATA.PWM_USER_DATA_SIZE Bit Field Locations and Descriptions

| Offset Address (Hex) | PWM_USER_DATA.PWM_USER_DATA_SIZE Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | BYTES[7:0] | | | | | | | |

| PWM_USER_DATA.PWM_USER_DATA_SIZE Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| BYTES[7:0] | R/W | 0 | The PWM user data length in bytes, from 1 to 128.<br>Indicates the number of bytes received or to be transmitted through OTP_EEPROM_PWM_BUFF. |

### PWM_USER_DATA.PWM_USER_DATA_CMD_STS

PWM user data command and status register.

TRIGGER: Writing to this byte triggers a read and activation of all the bytes of the PMW_USER_DATA module.

Table 354: PWM_USER_DATA.PWM_USER_DATA_CMD_STS Bit Field Locations and Descriptions

| Offset Address (Hex) | PWM_USER_DATA.PWM_USER_DATA_CMD_STS Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 003h | COMMAND_STATUS[7:0] | | | | | | | |

| PWM_USER_DATA.PWM_USER_DATA_CMD_STS Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| COMMAND_STATUS[7:0] | R/W | 0 | The user must set this field to 'Idle' whenever it is ready to receive new data. Before transmitting, the user has to set the 'Tx request' command and then wait for the 'Tx ack'. After this, the user can copy the data into OTP_EEPROM_PWM_BUF buffer and initiate a 'Start transmission' command. 0, 1, and 2 are set by the user. All the other status codes are set by the device.<br>0x00 = idle<br>0x01 = tx request<br>0x02 = start transmission<br>0x03 = tx ack<br>0x04 = tx in progress<br>0x05 = tx success<br>0x06 = tx invalid encoder ID<br>0x07 = tx wrong data size<br>0x08 = tx encoder error<br>0x09 = tx cancelled<br>0x0A = rx in progress<br>0x0B = rx success<br>0x0C = rx wrong data size<br>0x0D = rx lost frames<br>0x0E = rx timeout<br>0x0F = rx decoder error<br>0x10 = rx cancelled |

## Module: TOD_0

Configure the TOD registers.

Table 355: TOD_0 Register Index

| Offset (Hex) | Register Module Base Address: CBCCh[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | TOD_0.TOD_CFG | TOD configuration register. |

a. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

### TOD_0.TOD_CFG

Enable TOD counter, output channel sync and even-PPS mode.

TRIGGER: Writing to this byte triggers a read and activation of all the bytes of the TOD module.

Table 356: TOD_0.TOD_CFG Bit Field Locations and Descriptions

| Offset Address (Hex) | TOD_0.TOD_CFG Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | RESERVED[7:3] | | | | | TOD_EVEN_PPS_MODE[2] | TOD_OUT_SYNC_ENABLE[1] | TOD_ENABLE[0] |

| TOD_0.TOD_CFG Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| TOD_EVEN_PPS_MODE[2] | R/W | 0 | Enable even-PPS mode.<br>If enabled, then the pulse is generated every 2 seconds.<br>0 = disabled<br>1 = enabled |
| TOD_OUT_SYNC_ENABLE[1] | R/W | 0 | Enable the TOD output channel synchronization.<br>Set this flag to 1 to disable the TOD output channel synchronization.<br>0 = enabled<br>1 = disabled |
| TOD_ENABLE[0] | R/W | 0 | Enable TOD.<br>0 = disabled<br>1 = enabled |

## Module: TOD_WRITE_0

Configure the write registers.

Table 357: TOD_WRITE_0 Register Index

| Offset (Hex) | Register Module Base Address: CC00h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | TOD_WRITE_0.TOD_WRITE | TOD write registers. |
| 00Bh | RESERVED | This register must not be modified from the read value |
| 00Ch | TOD_WRITE_0.TOD_WRITE_COUNTER | Indicates when TOD write is completed. |
| 00Dh | TOD_WRITE_0.TOD_WRITE_SELECT_CFG_0 | TOD write trigger configuration. |
| 00Eh | RESERVED | This register must not be modified from the read value |
| 00Fh | TOD_WRITE_0.TOD_WRITE_CMD | TOD write trigger selection. |

a. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

### TOD_WRITE_0.TOD_WRITE

The maximum frequency of the clock driving the TOD accumulator is 1 GHz for DPLL 0 and 1, and 770 MHz for DPLL 2 and 3 .

Table 358: TOD_WRITE_0.TOD_WRITE Bit Field Locations and Descriptions

| Offset Address (Hex) | TOD_WRITE_0.TOD_WRITE Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | SUBNS[7:0] | | | | | | | |
| 001h | NS[15:8] | | | | | | | |
| 002h | NS[23:16] | | | | | | | |
| 003h | NS[31:24] | | | | | | | |
| 004h | NS[39:32] | | | | | | | |
| 005h | SECONDS[47:40] | | | | | | | |
| 006h | SECONDS[55:48] | | | | | | | |
| 007h | SECONDS[63:56] | | | | | | | |
| 008h | SECONDS[71:64] | | | | | | | |
| 009h | SECONDS[79:72] | | | | | | | |
| 00Ah | SECONDS[87:80] | | | | | | | |

| TOD_WRITE_0.TOD_WRITE Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SECONDS[87:40] | R/W | 0 | Seconds part of TOD.<br>Unsigned 48-bit value in seconds. |
| NS[39:8] | R/W | 0 | Nanoseconds part of TOD.<br>Unsigned 32-bit value in nanoseconds.<br>The maximum value is 0x3b9ac9ff = 999,999,999 ns. |
| SUBNS[7:0] | R/W | 0 | Sub-nanoseconds part of TOD.<br>Unsigned 8-bit value in units of 1/256 nanoseconds. |

### TOD_WRITE_0.TOD_WRITE_COUNTER

This counter increments to indicate completion.

Table 359: TOD_WRITE_0.TOD_WRITE_COUNTER Bit Field Locations and Descriptions

| Offset Address (Hex) | TOD_WRITE_0.TOD_WRITE_COUNTER Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ch | WRITE_COUNTER[7:0] | | | | | | | |

| TOD_WRITE_0.TOD_WRITE_COUNTER Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| WRITE_COUNTER[7:0] | R/O | 0 | TOD write counter.<br>This counter increments after the TOD is written to. |

### TOD_WRITE_0.TOD_WRITE_SELECT_CFG_0

Select the PWM decoder or the input index used as a trigger for TOD write.

Table 360: TOD_WRITE_0.TOD_WRITE_SELECT_CFG_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | TOD_WRITE_0.TOD_WRITE_SELECT_CFG_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Dh | PWM_DECODER_INDEX[7:4] | | | | REF_INDEX[3:0] | | | |

| TOD_WRITE_0.TOD_WRITE_SELECT_CFG_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PWM_DECODER_INDEX[7:4] | R/W | 0 | PWM decoder index used as trigger.<br>Applicable when tod_write_selection = 3 |
| REF_INDEX[3:0] | R/W | 0 | Input reference index used as trigger.<br>Applicable when tod_write_selection = 2 |

### TOD_WRITE_0.TOD_WRITE_CMD

Select the TOD mode and trigger source.

TRIGGER: Writing to this byte triggers a read and activation of all the bytes of the TOD_WRITE module.

Table 361: TOD_WRITE_0.TOD_WRITE_CMD Bit Field Locations and Descriptions

| Offset Address (Hex) | TOD_WRITE_0.TOD_WRITE_CMD Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Fh | RESERVED[7:6] | | TOD_WRITE_TYPE[5:4] | | TOD_WRITE_SELECTION[3:0] | | | |

| TOD_WRITE_0.TOD_WRITE_CMD Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |

| TOD_WRITE_0.TOD_WRITE_CMD Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| TOD_WRITE_TYPE[5:4] | R/W | 0 | TOD write type.<br>0 = absolute TOD<br>1 = delta TOD plus<br>2 = delta TOD minus. |
| TOD_WRITE_SELECTION [3:0] | R/W | 0 | TOD write trigger selection.<br>Applicable when tod_write_type = 0 (absolute ToD). For options 2, 3, 4 and 6, the trigger is always on the rising edge of the selected signal. This field will be cleared when the command is finished.<br>0 = disabled, no trigger<br>1 = immediate<br>2 = selected reference clock input<br>3 = selected PWM decoder's 1 PPS output<br>4 = rising edge of the ToD PPS signal<br>5 = feedback from FOD<br>6 = selected GPIO |

## Module: TOD_READ_PRIMARY_0

Configure the TOD read primary registers

Table 362: TOD_READ_PRIMARY_0 Register Index

| Offset (Hex) | Register Module Base Address: CC40h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | TOD_READ_PRIMARY_0.TOD_READ_PRIMARY | TOD read primary registers. |
| 00Bh | TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_COUNTER | Indicates when TOD read is completed. |
| 00Ch | TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_SEL_CFG_0 | TOD read trigger configuration. |
| 00Dh | TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_SEL_CFG_1 | TOD read trigger configuration. |
| 00Eh | TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_CMD | TOD read trigger selection. |

a. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

### TOD_READ_PRIMARY_0.TOD_READ_PRIMARY

The maximum frequency of the clock driving the TOD accumulator is 1 GHz for DPLL 0 and 1, and 770 MHz for DPLL 2 and 3 .

Table 363: TOD_READ_PRIMARY_0.TOD_READ_PRIMARY Bit Field Locations and Descriptions

| Offset Address (Hex) | TOD_READ_PRIMARY_0.TOD_READ_PRIMARY Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | SUBNS[7:0] | | | | | | | |
| 001h | NS[15:8] | | | | | | | |
| 002h | NS[23:16] | | | | | | | |
| 003h | NS[31:24] | | | | | | | |
| 004h | NS[39:32] | | | | | | | |
| 005h | SECONDS[47:40] | | | | | | | |
| 006h | SECONDS[55:48] | | | | | | | |
| 007h | SECONDS[63:56] | | | | | | | |
| 008h | SECONDS[71:64] | | | | | | | |
| 009h | SECONDS[79:72] | | | | | | | |
| 00Ah | SECONDS[87:80] | | | | | | | |

| TOD_READ_PRIMARY_0.TOD_READ_PRIMARY Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SECONDS[87:40] | R/O | 0 | Seconds part of TOD.<br>Unsigned 48-bit value in seconds. |
| NS[39:8] | R/O | 0 | Nanoseconds part of TOD.<br>Unsigned 32-bit value in nanoseconds.<br>The maximum value is 0x3b9ac9ff = 999,999,999 ns. |
| SUBNS[7:0] | R/O | 0 | Sub-nanoseconds part of TOD.<br>Unsigned 8-bit value in units of 1/256 nanoseconds. |

### TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_COUNTER

This counter increments to indicate completion.

Table 364: TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_COUNTER Bit Field Locations and Descriptions

| Offset Address (Hex) | TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_COUNTER Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Bh | READ_COUNTER[7:0] | | | | | | | |

| TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_COUNTER Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| READ_COUNTER[7:0] | R/O | 0 | TOD read counter.<br>This counter increments after the TOD is read from. |

### TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_SEL_CFG_0

Select the PWM decoder or the input index used as a trigger for TOD read.

Table 365: TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_SEL_CFG_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_SEL_CFG_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ch | PWM_DECODER_INDEX[7:4] | | | | REF_INDEX[3:0] | | | |

| TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_SEL_CFG_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PWM_DECODER_INDEX[7:4] | R/W | 0 | PWM decoder index used as trigger. |
| REF_INDEX[3:0] | R/W | 0 | Input reference index used as trigger. |

### TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_SEL_CFG_1

Select the DPLL for WR_FREQ event to be used as a trigger for TOD read.

Table 366: TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_SEL_CFG_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_SEL_CFG_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Dh | RESERVED[7:3] | | | | | DPLL_INDEX[2:0] | | |

| TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_SEL_CFG_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL_INDEX[2:0] | R/W | 0 | DPLL index used as trigger |

### TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_CMD

Read TOD read primary trigger selection.

TRIGGER: Writing to this byte triggers a read and activation of all the bytes of the TOD_READ_PRIMARY module.

Table 367: TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_CMD Bit Field Locations and Descriptions

| Offset Address (Hex) | TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_CMD Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Eh | RESERVED[7:5] | | | TOD_READ_TRIGGER_MODE[4] | TOD_READ_TRIGGER[3:0] | | | |

| TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_CMD Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| TOD_READ_TRIGGER_MODE[4] | R/W | 0 | Select single shot TOD read or continuous TOD read.<br>0 = single shot<br>1 = continuous |
| TOD_READ_TRIGGER[3:0] | R/W | 0 | Read TOD trigger.<br>For options 2, 3, 4 and 7, the trigger is always on the rising edge of the selected signal. This field will be cleared when the command is finished.<br>0 = disabled, no trigger<br>1 = immediate<br>2 = internal TOD PPS signal<br>3 = selected reference clock input<br>4 = selected PWM decoder's 1 PPS output<br>5 = reserved<br>6 = a write to DPLL_WR_FREQ<br>7 = selected GPIO |

## Module: TOD_READ_SECONDARY_0

Configure the TOD read secondary registers

Table 368: TOD_READ_SECONDARY_0 Register Index

| Offset (Hex) | Register Module Base Address: CC90h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | TOD_READ_SECONDARY_0.TOD_READ_SECONDARY | TOD read secondary registers. |

Table 368: TOD_READ_SECONDARY_0 Register Index

| Offset (Hex) | Register Module Base Address: CC90h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 00Bh | TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_COUNTER | Indicates when TOD read is completed. |
| 00Ch | TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_SEL_CFG_0 | TOD read trigger configuration. |
| 00Dh | TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_SEL_CFG_1 | TOD read trigger configuration. |
| 00Eh | TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_CMD | TOD read trigger selection. |

a. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

### TOD_READ_SECONDARY_0.TOD_READ_SECONDARY

The maximum frequency of the clock driving the TOD accumulator is 1 GHz for DPLL 0 and 1, and 770 MHz for DPLL 2 and 3 .

Table 369: TOD_READ_SECONDARY_0.TOD_READ_SECONDARY Bit Field Locations and Descriptions

| Offset Address (Hex) | TOD_READ_SECONDARY_0.TOD_READ_SECONDARY Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | SUBNS[7:0] | | | | | | | |
| 001h | NS[15:8] | | | | | | | |
| 002h | NS[23:16] | | | | | | | |
| 003h | NS[31:24] | | | | | | | |
| 004h | NS[39:32] | | | | | | | |
| 005h | SECONDS[47:40] | | | | | | | |
| 006h | SECONDS[55:48] | | | | | | | |
| 007h | SECONDS[63:56] | | | | | | | |
| 008h | SECONDS[71:64] | | | | | | | |
| 009h | SECONDS[79:72] | | | | | | | |
| 00Ah | SECONDS[87:80] | | | | | | | |

| TOD_READ_SECONDARY_0.TOD_READ_SECONDARY Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SECONDS[87:40] | R/O | 0 | Seconds part of TOD.<br>Unsigned 48-bit value in seconds. |
| NS[39:8] | R/O | 0 | Nanoseconds part of TOD.<br>Unsigned 32-bit value in nanoseconds.<br>The maximum value is 0x3b9ac9ff = 999,999,999 ns. |
| SUBNS[7:0] | R/O | 0 | Sub-nanoseconds part of TOD.<br>Unsigned 8-bit value in units of 1/256 nanoseconds. |

### TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_COUNTER

This counter increments to indicate completion.

Table 370: TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_COUNTER Bit Field Locations and Descriptions

| Offset Address (Hex) | TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_COUNTER Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Bh | READ_COUNTER[7:0] | | | | | | | |

| TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_COUNTER Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| READ_COUNTER[7:0] | R/O | 0 | TOD read counter.<br>This counter increments after the TOD is read from. |

### TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_SEL_CFG_0

Select the PWM decoder or the input index used as a trigger for TOD read.

Table 371: TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_SEL_CFG_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_SEL_CFG_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ch | PWM_DECODER_INDEX[7:4] | | | | REF_INDEX[3:0] | | | |

| TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_SEL_CFG_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| PWM_DECODER_INDEX[7:4] | R/W | 0 | PWM decoder index used as trigger. |
| REF_INDEX[3:0] | R/W | 0 | Input reference index used as trigger. |

### TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_SEL_CFG_1

Select the DPLL for WR_FREQ event to be used as a trigger for TOD read.

Table 372: TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_SEL_CFG_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_SEL_CFG_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Dh | RESERVED[7:3] | | | | | DPLL_INDEX[2:0] | | |

| TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_SEL_CFG_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| DPLL_INDEX[2:0] | R/W | 0 | DPLL index used as trigger |

### TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_CMD

Read TOD read secondary trigger selection.

TRIGGER: Writing to this byte triggers a read and activation of all the bytes of the TOD_READ_SECONDARY module.

Table 373: TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_CMD Bit Field Locations and Descriptions

| Offset Address (Hex) | TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_CMD Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Eh | RESERVED[7:5] | | | TOD_READ_TRIGGER_MODE[4] | TOD_READ_TRIGGER[3:0] | | | |

| TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_CMD Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |

| TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_CMD Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| TOD_READ_TRIGGER_MODE[4] | R/W | 0 | Select single shot TOD read or continuous TOD read.<br>0 = single shot<br>1 = continuous |
| TOD_READ_TRIGGER[3:0] | R/W | 0 | Read TOD trigger.<br>For options 2, 3, 4 and 7, the trigger is always on the rising edge of the selected signal. This field will be cleared when the command is finished.<br>0 = disabled, no trigger<br>1 = immediate<br>2 = internal TOD PPS signal<br>3 = selected reference clock input<br>4 = selected PWM decoder's 1 PPS output<br>5 = reserved<br>6 = a write to DPLL_WR_FREQ<br>7 = selected GPIO |

## Module: OUTPUT_TDC_CFG

Configure the global parameters of the output TDC.

Table 374: OUTPUT_TDC_CFG Register Index

| Offset (Hex) | Register Module Base Address: CCD0h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | OUTPUT_TDC_CFG.OUTPUT_TDC_CFG_GBL_0 | Fastlock enable delay. |
| 002h | OUTPUT_TDC_CFG.OUTPUT_TDC_CFG_GBL_1 | Fastlock disable delay. |
| 004h | OUTPUT_TDC_CFG.OUTPUT_TDC_CFG_GBL_2 | Output TDC configuration. |

### OUTPUT_TDC_CFG.OUTPUT_TDC_CFG_GBL_0

Configure the fast lock enable delay.

Table 375: OUTPUT_TDC_CFG.OUTPUT_TDC_CFG_GBL_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | OUTPUT_TDC_CFG.OUTPUT_TDC_CFG_GBL_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | FAST_LOCK_ENABLE_DELAY[7:0] | | | | | | | |
| 001h | FAST_LOCK_ENABLE_DELAY[15:8] | | | | | | | |

| OUTPUT_TDC_CFG.OUTPUT_TDC_CFG_GBL_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FAST_LOCK_ENABLE_DELAY[15:0] | R/W | 0 | Duration to wait after enabling output TDC fast lock.<br>Unsigned 16-bit value in microseconds. 0 = default 500 microseconds.<br>When output TDC is enabled, it needs time for the reference clock to settle to the correct frequency. Fast lock is used to shorten the settling time to within microseconds compared to milliseconds. |

### OUTPUT_TDC_CFG.OUTPUT_TDC_CFG_GBL_1

Configure the fast lock disable delay.

Table 376: OUTPUT_TDC_CFG.OUTPUT_TDC_CFG_GBL_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | OUTPUT_TDC_CFG.OUTPUT_TDC_CFG_GBL_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | FAST_LOCK_DISABLE_DELAY[7:0] | | | | | | | |
| 003h | FAST_LOCK_DISABLE_DELAY[15:8] | | | | | | | |

| OUTPUT_TDC_CFG.OUTPUT_TDC_CFG_GBL_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FAST_LOCK_DISABLE_DELAY[15:0] | R/W | 0 | Duration to wait after disabling fast lock to allow the output TDC reference clock time to settle.<br>Unsigned 16-bit value in microseconds. 0 = default 500 microseconds.<br>Fast lock is disabled prior to measurement and needs time to settle afterwards. |

### OUTPUT_TDC_CFG.OUTPUT_TDC_CFG_GBL_2

Configure the output TDC .

TRIGGER: Writing to this byte triggers a read and activation in hardware of all the bytes of the OUTPUT_TDC_CFG module.

Table 377: OUTPUT_TDC_CFG.OUTPUT_TDC_CFG_GBL_2 Bit Field Locations and Descriptions

| Offset Address (Hex) | OUTPUT_TDC_CFG.OUTPUT_TDC_CFG_GBL_2 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | RESERVED[7:2] | | | | | | REF_SEL[1] | ENABLE[0] |

| OUTPUT_TDC_CFG.OUTPUT_TDC_CFG_GBL_2 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| REF_SEL[1] | R/W | 0 | Select reference clock for output TDC.<br>ref_sel change takes effect when 'enable' transitions from 0 -> 1.<br>If ref_sel is changed when 'enable' = 1, the change is ignored.<br>0 = XTAL<br>1 = XO_DPLL |
| ENABLE[0] | R/W | 0 | Enable or disable output TDC.<br>Output TDC is disabled by default to save power when not in use.<br>Ready state is indicated by OUTPUT_TDC_CFG_STATUS.state.<br>0 = disabled<br>1 = enabled |

## Module: OUTPUT_TDC_0

Configure the output TDC.

Table 378: OUTPUT_TDC_0 Register Index

| Offset (Hex) | Register Module Base Address: CD00h[a] | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | OUTPUT_TDC_0.OUTPUT_TDC_CTRL_0 | Output TDC control register. |
| 002h | OUTPUT_TDC_0.OUTPUT_TDC_CTRL_1 | Output TDC control register. |
| 004h | OUTPUT_TDC_0.OUTPUT_TDC_CTRL_2 | Output TDC control register. |
| 005h | OUTPUT_TDC_0.OUTPUT_TDC_CTRL_3 | Output TDC control register. |
| 006h | OUTPUT_TDC_0.OUTPUT_TDC_CTRL_4 | Output TDC control register. |

a. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

### OUTPUT_TDC_0.OUTPUT_TDC_CTRL_0

Configure output TDC.

Table 379: OUTPUT_TDC_0.OUTPUT_TDC_CTRL_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | OUTPUT_TDC_0.OUTPUT_TDC_CTRL_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | SAMPLES[7:0] | | | | | | | |
| 001h | SAMPLES[15:8] | | | | | | | |

| OUTPUT_TDC_0.OUTPUT_TDC_CTRL_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SAMPLES[15:0] | R/W | 0 | Unsigned 16-bit value indicating the number of samples to use for measurement.<br>0 = 4096 samples.<br>When using more than one sample, the final measurement is an average. |

### OUTPUT_TDC_0.OUTPUT_TDC_CTRL_1

Configure output TDC.

Table 380: OUTPUT_TDC_0.OUTPUT_TDC_CTRL_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | OUTPUT_TDC_0.OUTPUT_TDC_CTRL_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | TARGET_PHASE_OFFSET[7:0] | | | | | | | |
| 003h | TARGET_PHASE_OFFSET[15:8] | | | | | | | |

| OUTPUT_TDC_0.OUTPUT_TDC_CTRL_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| TARGET_PHASE_OFFSET[15:0] | R/W | 0 | Target phase offset for alignment operation.<br>Signed 16-bit target phase offset in picoseconds.<br>Used in alignment mode, ignored in measurement mode. |

### OUTPUT_TDC_0.OUTPUT_TDC_CTRL_2

Configure output TDC.

Table 381: OUTPUT_TDC_0.OUTPUT_TDC_CTRL_2 Bit Field Locations and Descriptions

| Offset Address (Hex) | OUTPUT_TDC_0.OUTPUT_TDC_CTRL_2 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | ALIGN_TARGET_MASK[7:0] | | | | | | | |

| OUTPUT_TDC_0.OUTPUT_TDC_CTRL_2 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| ALIGN_TARGET_MASK[7:0] | R/W | 0 | Used in alignment mode to indicate the target DPLL(s). The outputs of these DPLL(s) will be aligned to the outputs of the source DPLL.<br>DPLL alignment target mask index.<br>Alignment mode: Each set bit represents the DPLLs to be aligned with the 'source_index' DPLL.<br>Bit 0 corresponds to DPLL0, bit 1 DPLL1, etc.<br>0b00000001 = DPLL0<br>. . .<br>0b10000000 = DPLL7<br>. . .<br>0b00000011 = DPLL0 and DPLL1<br>. . . |

### OUTPUT_TDC_0.OUTPUT_TDC_CTRL_3

Configure output TDC.

Table 382: OUTPUT_TDC_0.OUTPUT_TDC_CTRL_3 Bit Field Locations and Descriptions

| Offset Address (Hex) | OUTPUT_TDC_0.OUTPUT_TDC_CTRL_3 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 005h | TARGET_INDEX[7:4] | | | | SOURCE_INDEX[3:0] | | | |

| OUTPUT_TDC_0.OUTPUT_TDC_CTRL_3 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| TARGET_INDEX[7:4] | R/W | 0 | Used in measurement mode to indicate the target clock.<br>Indicates the target to measure against 'source_index'. If the target is a DPLL index, then the Master Sync signal from that DPLL is used for measurement. The delay between the Master Sync and the output clock is 9 FOD cycles.<br>0x0 = DPLL0<br>0x1 = DPLL1<br>0x2 = DPLL2<br>0x3 = DPLL3<br>0x4 = DPLL4<br>0x5 = DPLL5<br>0x6 = DPLL6<br>0x7 = DPLL7<br>0x8 = GPIO6<br>0x9 = GPIO1<br>0xA = GPIO2<br>0xB = GPIO7 |
| SOURCE_INDEX[3:0] | R/W | 0 | Used in measurement and alignment mode to indicate the source clock.<br>In measurement mode, indicates the source to be used as the measurement reference. If the source is a DPLL index, then the Master Sync signal from that DPLL is used for measurement. The delay between the Master Sync and the output clock is 9 FOD cycles. In alignment mode, the source must be a DPLL index.<br>0x0 = DPLL0<br>0x1 = DPLL1<br>0x2 = DPLL2<br>0x3 = DPLL3<br>0x4 = DPLL4<br>0x5 = DPLL5<br>0x6 = DPLL6<br>0x7 = DPLL7<br>0x8 = GPIO6<br>0x9 = GPIO1<br>0xA = GPIO2<br>0xB = GPIO7 |

### OUTPUT_TDC_0.OUTPUT_TDC_CTRL_4

Configure output TDC.

TRIGGER: Writing to this byte triggers a read and activation in hardware of all the bytes of the OUTPUT_TDC module.

Table 383: OUTPUT_TDC_0.OUTPUT_TDC_CTRL_4 Bit Field Locations and Descriptions

| Offset Address (Hex) | OUTPUT_TDC_0.OUTPUT_TDC_CTRL_4 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 006h | DISABLE_MEASUREMENT_FILTER[7] | ALIGN_THRESHOLD_COUNT[6:4] | | | ALIGN_RESET[3] | TYPE[2] | MODE[1] | GO[0] |

| OUTPUT_TDC_0.OUTPUT_TDC_CTRL_4 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DISABLE_MEASUREMENT_FILTER[7] | R/W | 0 | Large measurements are considered outliers and filtered out.<br>If 'source_index' is a DPLL index, measurements larger than 1/2 the master divider frequency are filtered out. To disable this filtering, set 'disable_measurement_filter' = 1. If 'source_index' is a GPIO, the filtering is always disabled.<br>0 = filter enabled<br>1 = filter disabled |
| ALIGN_THRESHOLD_COUNT[6:4] | R/W | 0 | Threshold count to determine when alignment is done.<br>In single shot alignment mode, this determines the number of sequential measurement readings that match 'target_phase_offset' before declaring alignment is done.<br>Value of 0 means count of 1. |
| ALIGN_RESET[3] | R/W | 0 | Reset output TDC accumulated adjustments to zero prior to starting output TDC operation. (i.e. clear accumulated coarse phase delay and fine phase advance adjustments)<br>Measurement mode: Set to '1' to reset the output TDC alignment of the target specified by the 'target_index' field.<br>Alignment mode: Set to '1' to reset the output TDC alignment of the target(s) specified by the 'alignment_target_mask' field.<br>Takes effect when 'go' field is set to '1' at the start the output TDC operation.<br>0 = keep accumulated<br>1 = clear accumulated |
| TYPE[2] | R/W | 0 | Type of output TDC operation, single shot or continuous.<br>Single shot: Collect the number of samples (average if necessary) and clear 'go' when completed.<br>Continuous: Same as single shot mode, except the operation will be repeated continuously. To stop operation, clear 'go'.<br>0 = single shot<br>1 = continuous |

| OUTPUT_TDC_0.OUTPUT_TDC_CTRL_4 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| MODE[1] | R/W | 0 | Select mode of output TDC operation.<br>Measurement mode: Take a measurement at approx. 100 us intervals. When 'samples' measurements is reached, the average measurement is stored it in OUTPUT_TDCn_MEASUREMENT.<br>Alignment mode: Aligns the targets in 'align_target_mask' to 'source_index' to match 'target_phase_offset' picoseconds.<br>0 = measurement<br>1 = alignment |
| GO[0] | R/W | 0 | Start or stop output TDC operation.<br>Write 1 to start output TDC operation and clear OUTPUT_TDCn_STATUS.valid. OUTPUT_TDCn_STATUS.valid will be set when the measurement is valid or when the alignment operation reaches the 'target_phase_offset' picoseconds. OUTPUT_TDCn_STATUS.status can be used to check output TDC operational status.<br>For 'type' = single shot, when the operation is complete, 'go' will be cleared to 0 and OUTPUT_TDC0_STATUS.status will be set to 'Idle' on success and an error status on failure.<br>For 'type' = continuous, on success, 'go' will stay set and the operation continues until user clears 'go' to cancel the alignment operations. On failure, the operation stops and 'go' will be cleared.<br>0 = stop output TDC operation<br>1 = start output TDC operation |

## Module: INPUT_TDC

-

Table 384: INPUT_TDC Register Index

| Offset (Hex) | Register Module Base Address: CD20h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | INPUT_TDC.INPUT_TDC_SDM_FRAC | Input TDC feedback divider fractional value. |
| 002h | INPUT_TDC.INPUT_TDC_SDM_MOD | Input TDC feedback divider modulus value. |
| 004h | INPUT_TDC.INPUT_TDC_FBD_CTRL | Input TDC feedback divider control. |
| 005h | INPUT_TDC.INPUT_TDC_CTRL | Input TDC control |

### INPUT_TDC.INPUT_TDC_SDM_FRAC

Input TDC feedback divider fractional value.

Table 385: INPUT_TDC.INPUT_TDC_SDM_FRAC Bit Field Locations and Descriptions

| Offset Address (Hex) | INPUT_TDC.INPUT_TDC_SDM_FRAC Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | SDM_FRAC[7:0] | | | | | | | |
| 001h | SDM_FRAC[15:8] | | | | | | | |

| INPUT_TDC.INPUT_TDC_SDM_FRAC Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SDM_FRAC[15:0] | R/W | 0 | Input TDC feedback divider fractional value. |

### INPUT_TDC.INPUT_TDC_SDM_MOD

Input TDC feedback divider modulus value.

Table 386: INPUT_TDC.INPUT_TDC_SDM_MOD Bit Field Locations and Descriptions

| Offset Address (Hex) | INPUT_TDC.INPUT_TDC_SDM_MOD Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | SDM_MOD[7:0] | | | | | | | |
| 003h | SDM_MOD[15:8] | | | | | | | |

| INPUT_TDC.INPUT_TDC_SDM_MOD Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SDM_MOD[15:0] | R/W | 0 | Input TDC feedback divider modulus value. |

### INPUT_TDC.INPUT_TDC_FBD_CTRL

Input TDC feedback divider control.

Table 387: INPUT_TDC.INPUT_TDC_FBD_CTRL Bit Field Locations and Descriptions

| Offset Address (Hex) | INPUT_TDC.INPUT_TDC_FBD_CTRL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | FBD_INTEGER_MODE_EN[7] | FBD_INTEGER[6:0] | | | | | | |

| INPUT_TDC.INPUT_TDC_FBD_CTRL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| FBD_INTEGER_MODE_EN[7] | R/W | 0 | Input TDC feedback divider integer mode enable.<br>When set to '0', the input TDC feedback divider will be programmed internally and the input TDC frequency will be configured as 625 MHz.<br>When set to '1', all parameters apply (sdm_frac, sdm_mod, fbd_integer, and sdm_order).<br>0 = disabled<br>1 = enabled |
| FBD_INTEGER[6:0] | R/W | 0 | Input TDC feedback divider integer value.<br>ITDC_UI = 1 / (32 * input TDC frequency). |

### INPUT_TDC.INPUT_TDC_CTRL

Input TDC control

TRIGGER: Writing to this byte triggers a read and activation in hardware of all the bytes of the INPUT_TDC module.

Table 388: INPUT_TDC.INPUT_TDC_CTRL Bit Field Locations and Descriptions

| Offset Address (Hex) | INPUT_TDC.INPUT_TDC_CTRL Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 005h | RESERVED[7:3] | | | | | SDM_ORDER[2:1] | | REF_SEL[0] |

| INPUT_TDC.INPUT_TDC_CTRL Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| SDM_ORDER[2:1] | R/W | 0 | Input TDC SDM order.<br>If sdm_frac = 0, then sdm_order is ignored and treated as zero.<br>0 = integer<br>1 = 1st order<br>2 = 2nd order<br>3 = 3rd order |
| REF_SEL[0] | R/W | 0 | Control mux to forward either a XTAL or XO_DPLL reference towards Input TDC. By default, a XTAL reference is forwarded towards it.<br>0 = XTAL<br>1 = XO_DPLL |

## Module: SCRATCH

These multipurpose registers are not used by FW and are intended to for users to maintain their own data.

Table 389: SCRATCH Register Index

| Offset (Hex) | Register Module Base Address: CF50h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | SCRATCH.SCRATCH0 | Multipurpose register |
| 004h | SCRATCH.SCRATCH1 | Multipurpose register |
| 008h | SCRATCH.SCRATCH2 | Multipurpose register |
| 00Ch | SCRATCH.SCRATCH3 | Multipurpose register |

### SCRATCH.SCRATCH0

User read or write data. The HW reset value will be restored on soft reset.

Table 390: SCRATCH.SCRATCH0 Bit Field Locations and Descriptions

| Offset Address (Hex) | SCRATCH.SCRATCH0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | SCRATCH0[7:0] | | | | | | | |
| 001h | SCRATCH0[15:8] | | | | | | | |
| 002h | SCRATCH0[23:16] | | | | | | | |
| 003h | SCRATCH0[31:24] | | | | | | | |

| SCRATCH.SCRATCH0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SCRATCH0[31:0] | R/W | 0 | User data. |

### SCRATCH.SCRATCH1

User read or write data. The HW reset value will be restored on soft reset.

Table 391: SCRATCH.SCRATCH1 Bit Field Locations and Descriptions

| Offset Address (Hex) | SCRATCH.SCRATCH1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | SCRATCH1[7:0] | | | | | | | |
| 005h | SCRATCH1[15:8] | | | | | | | |
| 006h | SCRATCH1[23:16] | | | | | | | |
| 007h | SCRATCH1[31:24] | | | | | | | |

| SCRATCH.SCRATCH1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SCRATCH1[31:0] | R/W | 0 | User data. |

### SCRATCH.SCRATCH2

User read or write data. The HW reset value will be restored on soft reset.

Table 392: SCRATCH.SCRATCH2 Bit Field Locations and Descriptions

| Offset Address (Hex) | SCRATCH.SCRATCH2 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 008h | SCRATCH2[7:0] | | | | | | | |
| 009h | SCRATCH2[15:8] | | | | | | | |
| 00Ah | SCRATCH2[23:16] | | | | | | | |
| 00Bh | SCRATCH2[31:24] | | | | | | | |

| SCRATCH.SCRATCH2 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SCRATCH2[31:0] | R/W | 0 | User data. |

### SCRATCH.SCRATCH3

User read or write data. The HW reset value will be restored on soft reset.

Table 393: SCRATCH.SCRATCH3 Bit Field Locations and Descriptions

| Offset Address (Hex) | SCRATCH.SCRATCH3 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ch | SCRATCH3[7:0] | | | | | | | |
| 00Dh | SCRATCH3[15:8] | | | | | | | |
| 00Eh | SCRATCH3[23:16] | | | | | | | |
| 00Fh | SCRATCH3[31:24] | | | | | | | |

| SCRATCH.SCRATCH3 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| SCRATCH3[31:0] | R/W | 0 | User data. |

## Module: EEPROM

Access EEPROM.

Table 394: EEPROM Register Index

| Offset (Hex) | Register Module Base Address: CF68h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | EEPROM.EEPROM_I2C_ADDR | EEPROM I2C address. |
| 001h | EEPROM.EEPROM_SIZE | EEPROM data transfer size. |
| 002h | EEPROM.EEPROM_OFFSET | EEPROM offset. |
| 004h | EEPROM.EEPROM_CMD | EEPROM command. |

### EEPROM.EEPROM_I2C_ADDR

EEPROM I2C address.

Table 395: EEPROM.EEPROM_I2C_ADDR Bit Field Locations and Descriptions

| Offset Address (Hex) | EEPROM.EEPROM_I2C_ADDR Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | RESERVED[7] | I2C_ADDR[6:0] | | | | | | |

| EEPROM.EEPROM_I2C_ADDR Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| RESERVED | N/A | - | This field must not be modified from the read value |
| I2C_ADDR[6:0] | R/W | 0 | I2C address of the EEPROM. |

### EEPROM.EEPROM_SIZE

Configure the number of bytes to read or write.

Table 396: EEPROM.EEPROM_SIZE Bit Field Locations and Descriptions

| Offset Address (Hex) | EEPROM.EEPROM_SIZE Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 001h | BYTES[7:0] | | | | | | | |

| EEPROM.EEPROM_SIZE Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| BYTES[7:0] | R/W | 0 | Number of bytes to read or write.<br>These bytes are transferred through OTP_EEPROM_BUFF. Valid range is 0 to 128. |

### EEPROM.EEPROM_OFFSET

Address offset inside the EEPROM.

Table 397: EEPROM.EEPROM_OFFSET Bit Field Locations and Descriptions

| Offset Address (Hex) | EEPROM.EEPROM_OFFSET Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | EEPROM_OFFSET[7:0] | | | | | | | |
| 003h | EEPROM_OFFSET[15:8] | | | | | | | |

| EEPROM.EEPROM_OFFSET Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| EEPROM_OFFSET[15:0] | R/W | 0 | Unsigned 16-bit value in bytes indicating the offset inside the EEPROM. |

### EEPROM.EEPROM_CMD

Initiate EEPROM read or write.

Table 398: EEPROM.EEPROM_CMD Bit Field Locations and Descriptions

| Offset Address (Hex) | EEPROM.EEPROM_CMD Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | EEPROM_CMD[7:0] | | | | | | | |
| 005h | EEPROM_CMD[15:8] | | | | | | | |

| EEPROM.EEPROM_CMD Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| EEPROM_CMD[15:0] | R/W | 0 | Command.<br>0xEE01 = Read from EEPROM<br>0xEE02 = Write to EEPROM<br>0xEE03 = Write (no verify) |

## Module: OTP

Configure OTP. Please contact IDT for details.

Table 399: OTP Register Index

| Offset (Hex) | Register Module Base Address: CF70h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | OTP.OTP_CMD | OTP command. |
| 004h | OTP.OTP_CM_CTR | Device counter. |
| 006h | OTP.OTP_HOST_CTR | Update counter. |

### OTP.OTP_CMD

Initiate OTP transaction. Please contact IDT for details.

Table 400: OTP.OTP_CMD Bit Field Locations and Descriptions

| Offset Address (Hex) | OTP.OTP_CMD Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | OTP_CMD[7:0] | | | | | | | |
| 001h | OTP_CMD[15:8] | | | | | | | |
| 002h | OTP_CMD[23:16] | | | | | | | |
| 003h | OTP_CMD[31:24] | | | | | | | |

| OTP.OTP_CMD Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| OTP_CMD[31:0] | R/W | 0 | - |

### OTP.OTP_CM_CTR

Word counter updated by the device. Please contact IDT for details.

Table 401: OTP.OTP_CM_CTR Bit Field Locations and Descriptions

| Offset Address (Hex) | OTP.OTP_CM_CTR Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | OTP_CM_CTR[7:0] | | | | | | | |
| 005h | OTP_CM_CTR[15:8] | | | | | | | |

| OTP.OTP_CM_CTR Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| OTP_CM_CTR[15:0] | R/O | 0 | Total number of 32-bit words transferred through the OTP buffer during the current command<br>This 16-bit counter is updated by the internal processor, and represents the total number of 32-bit words transferred through the OTP buffer during the current command. Please contact IDT for details. |

### OTP.OTP_HOST_CTR

Word counter updated by the user. Please contact IDT for details.

Table 402: OTP.OTP_HOST_CTR Bit Field Locations and Descriptions

| Offset Address (Hex) | OTP.OTP_HOST_CTR Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 006h | OTP_HOST_CTR[7:0] | | | | | | | |
| 007h | OTP_HOST_CTR[15:8] | | | | | | | |

| OTP.OTP_HOST_CTR Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| OTP_HOST_CTR[15:0] | R/W | 0 | Total number of 32-bit words transferred through the OTP buffer during the current command<br>This 16-bit counter is updated by the external host processor, and represents the total number of 32-bit words transferred through the OTP buffer during the current command. Please contact IDT for details. |

## Module: BYTE

Configure the OTP registers. Please contact IDT for details.

Table 403: BYTE Register Index

| Offset (Hex) | Register Module Base Address: CF80h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 000h | BYTE.OTP_EEPROM_PWM_BUFF_0 | OTP/EEPROM/PWM buffer. |
| 001h | BYTE.OTP_EEPROM_PWM_BUFF_1 | |
| 002h | BYTE.OTP_EEPROM_PWM_BUFF_2 | |
| 003h | BYTE.OTP_EEPROM_PWM_BUFF_3 | |
| 004h | BYTE.OTP_EEPROM_PWM_BUFF_4 | |
| 005h | BYTE.OTP_EEPROM_PWM_BUFF_5 | |
| 006h | BYTE.OTP_EEPROM_PWM_BUFF_6 | |
| 007h | BYTE.OTP_EEPROM_PWM_BUFF_7 | |
| 008h | BYTE.OTP_EEPROM_PWM_BUFF_8 | |
| 009h | BYTE.OTP_EEPROM_PWM_BUFF_9 | |
| 00Ah | BYTE.OTP_EEPROM_PWM_BUFF_10 | |
| 00Bh | BYTE.OTP_EEPROM_PWM_BUFF_11 | |
| 00Ch | BYTE.OTP_EEPROM_PWM_BUFF_12 | |
| 00Dh | BYTE.OTP_EEPROM_PWM_BUFF_13 | |
| 00Eh | BYTE.OTP_EEPROM_PWM_BUFF_14 | |

Table 403: BYTE Register Index

| Offset (Hex) | Register Module Base Address: CF80h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 00Fh | BYTE.OTP_EEPROM_PWM_BUFF_15 | |
| 010h | BYTE.OTP_EEPROM_PWM_BUFF_16 | |
| 011h | BYTE.OTP_EEPROM_PWM_BUFF_17 | |
| 012h | BYTE.OTP_EEPROM_PWM_BUFF_18 | |
| 013h | BYTE.OTP_EEPROM_PWM_BUFF_19 | |
| 014h | BYTE.OTP_EEPROM_PWM_BUFF_20 | |
| 015h | BYTE.OTP_EEPROM_PWM_BUFF_21 | |
| 016h | BYTE.OTP_EEPROM_PWM_BUFF_22 | |
| 017h | BYTE.OTP_EEPROM_PWM_BUFF_23 | |
| 018h | BYTE.OTP_EEPROM_PWM_BUFF_24 | |
| 019h | BYTE.OTP_EEPROM_PWM_BUFF_25 | |
| 01Ah | BYTE.OTP_EEPROM_PWM_BUFF_26 | |
| 01Bh | BYTE.OTP_EEPROM_PWM_BUFF_27 | |
| 01Ch | BYTE.OTP_EEPROM_PWM_BUFF_28 | |
| 01Dh | BYTE.OTP_EEPROM_PWM_BUFF_29 | |
| 01Eh | BYTE.OTP_EEPROM_PWM_BUFF_30 | |
| 01Fh | BYTE.OTP_EEPROM_PWM_BUFF_31 | |
| 020h | BYTE.OTP_EEPROM_PWM_BUFF_32 | |
| 021h | BYTE.OTP_EEPROM_PWM_BUFF_33 | |
| 022h | BYTE.OTP_EEPROM_PWM_BUFF_34 | |
| 023h | BYTE.OTP_EEPROM_PWM_BUFF_35 | |
| 024h | BYTE.OTP_EEPROM_PWM_BUFF_36 | |
| 025h | BYTE.OTP_EEPROM_PWM_BUFF_37 | |
| 026h | BYTE.OTP_EEPROM_PWM_BUFF_38 | |
| 027h | BYTE.OTP_EEPROM_PWM_BUFF_39 | |
| 028h | BYTE.OTP_EEPROM_PWM_BUFF_40 | |
| 029h | BYTE.OTP_EEPROM_PWM_BUFF_41 | |
| 02Ah | BYTE.OTP_EEPROM_PWM_BUFF_42 | |
| 02Bh | BYTE.OTP_EEPROM_PWM_BUFF_43 | |
| 02Ch | BYTE.OTP_EEPROM_PWM_BUFF_44 | |
| 02Dh | BYTE.OTP_EEPROM_PWM_BUFF_45 | |
| 02Eh | BYTE.OTP_EEPROM_PWM_BUFF_46 | |

Table 403: BYTE Register Index

| Offset (Hex) | Register Module Base Address: CF80h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 02Fh | BYTE.OTP_EEPROM_PWM_BUFF_47 | |
| 030h | BYTE.OTP_EEPROM_PWM_BUFF_48 | |
| 031h | BYTE.OTP_EEPROM_PWM_BUFF_49 | |
| 032h | BYTE.OTP_EEPROM_PWM_BUFF_50 | |
| 033h | BYTE.OTP_EEPROM_PWM_BUFF_51 | |
| 034h | BYTE.OTP_EEPROM_PWM_BUFF_52 | |
| 035h | BYTE.OTP_EEPROM_PWM_BUFF_53 | |
| 036h | BYTE.OTP_EEPROM_PWM_BUFF_54 | |
| 037h | BYTE.OTP_EEPROM_PWM_BUFF_55 | |
| 038h | BYTE.OTP_EEPROM_PWM_BUFF_56 | |
| 039h | BYTE.OTP_EEPROM_PWM_BUFF_57 | |
| 03Ah | BYTE.OTP_EEPROM_PWM_BUFF_58 | |
| 03Bh | BYTE.OTP_EEPROM_PWM_BUFF_59 | |
| 03Ch | BYTE.OTP_EEPROM_PWM_BUFF_60 | |
| 03Dh | BYTE.OTP_EEPROM_PWM_BUFF_61 | |
| 03Eh | BYTE.OTP_EEPROM_PWM_BUFF_62 | |
| 03Fh | BYTE.OTP_EEPROM_PWM_BUFF_63 | |
| 040h | BYTE.OTP_EEPROM_PWM_BUFF_64 | |
| 041h | BYTE.OTP_EEPROM_PWM_BUFF_65 | |
| 042h | BYTE.OTP_EEPROM_PWM_BUFF_66 | |
| 043h | BYTE.OTP_EEPROM_PWM_BUFF_67 | |
| 044h | BYTE.OTP_EEPROM_PWM_BUFF_68 | |
| 045h | BYTE.OTP_EEPROM_PWM_BUFF_69 | |
| 046h | BYTE.OTP_EEPROM_PWM_BUFF_70 | |
| 047h | BYTE.OTP_EEPROM_PWM_BUFF_71 | |
| 048h | BYTE.OTP_EEPROM_PWM_BUFF_72 | |
| 049h | BYTE.OTP_EEPROM_PWM_BUFF_73 | |
| 04Ah | BYTE.OTP_EEPROM_PWM_BUFF_74 | |
| 04Bh | BYTE.OTP_EEPROM_PWM_BUFF_75 | |
| 04Ch | BYTE.OTP_EEPROM_PWM_BUFF_76 | |
| 04Dh | BYTE.OTP_EEPROM_PWM_BUFF_77 | |
| 04Eh | BYTE.OTP_EEPROM_PWM_BUFF_78 | |

Table 403: BYTE Register Index

| Offset (Hex) | Register Module Base Address: CF80h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 04Fh | BYTE.OTP_EEPROM_PWM_BUFF_79 | |
| 050h | BYTE.OTP_EEPROM_PWM_BUFF_80 | |
| 051h | BYTE.OTP_EEPROM_PWM_BUFF_81 | |
| 052h | BYTE.OTP_EEPROM_PWM_BUFF_82 | |
| 053h | BYTE.OTP_EEPROM_PWM_BUFF_83 | |
| 054h | BYTE.OTP_EEPROM_PWM_BUFF_84 | |
| 055h | BYTE.OTP_EEPROM_PWM_BUFF_85 | |
| 056h | BYTE.OTP_EEPROM_PWM_BUFF_86 | |
| 057h | BYTE.OTP_EEPROM_PWM_BUFF_87 | |
| 058h | BYTE.OTP_EEPROM_PWM_BUFF_88 | |
| 059h | BYTE.OTP_EEPROM_PWM_BUFF_89 | |
| 05Ah | BYTE.OTP_EEPROM_PWM_BUFF_90 | |
| 05Bh | BYTE.OTP_EEPROM_PWM_BUFF_91 | |
| 05Ch | BYTE.OTP_EEPROM_PWM_BUFF_92 | |
| 05Dh | BYTE.OTP_EEPROM_PWM_BUFF_93 | |
| 05Eh | BYTE.OTP_EEPROM_PWM_BUFF_94 | |
| 05Fh | BYTE.OTP_EEPROM_PWM_BUFF_95 | |
| 060h | BYTE.OTP_EEPROM_PWM_BUFF_96 | |
| 061h | BYTE.OTP_EEPROM_PWM_BUFF_97 | |
| 062h | BYTE.OTP_EEPROM_PWM_BUFF_98 | |
| 063h | BYTE.OTP_EEPROM_PWM_BUFF_99 | |
| 064h | BYTE.OTP_EEPROM_PWM_BUFF_100 | |
| 065h | BYTE.OTP_EEPROM_PWM_BUFF_101 | |
| 066h | BYTE.OTP_EEPROM_PWM_BUFF_102 | |
| 067h | BYTE.OTP_EEPROM_PWM_BUFF_103 | |
| 068h | BYTE.OTP_EEPROM_PWM_BUFF_104 | |
| 069h | BYTE.OTP_EEPROM_PWM_BUFF_105 | |
| 06Ah | BYTE.OTP_EEPROM_PWM_BUFF_106 | |
| 06Bh | BYTE.OTP_EEPROM_PWM_BUFF_107 | |
| 06Ch | BYTE.OTP_EEPROM_PWM_BUFF_108 | |
| 06Dh | BYTE.OTP_EEPROM_PWM_BUFF_109 | |
| 06Eh | BYTE.OTP_EEPROM_PWM_BUFF_110 | |

Table 403: BYTE Register Index

| Offset (Hex) | Register Module Base Address: CF80h | |
|---|---|---|
| | Individual Register Name | Register Description |
| 06Fh | BYTE.OTP_EEPROM_PWM_BUFF_111 | |
| 070h | BYTE.OTP_EEPROM_PWM_BUFF_112 | |
| 071h | BYTE.OTP_EEPROM_PWM_BUFF_113 | |
| 072h | BYTE.OTP_EEPROM_PWM_BUFF_114 | |
| 073h | BYTE.OTP_EEPROM_PWM_BUFF_115 | |
| 074h | BYTE.OTP_EEPROM_PWM_BUFF_116 | |
| 075h | BYTE.OTP_EEPROM_PWM_BUFF_117 | |
| 076h | BYTE.OTP_EEPROM_PWM_BUFF_118 | |
| 077h | BYTE.OTP_EEPROM_PWM_BUFF_119 | |
| 078h | BYTE.OTP_EEPROM_PWM_BUFF_120 | |
| 079h | BYTE.OTP_EEPROM_PWM_BUFF_121 | |
| 07Ah | BYTE.OTP_EEPROM_PWM_BUFF_122 | |
| 07Bh | BYTE.OTP_EEPROM_PWM_BUFF_123 | |
| 07Ch | BYTE.OTP_EEPROM_PWM_BUFF_124 | |
| 07Dh | BYTE.OTP_EEPROM_PWM_BUFF_125 | |
| 07Eh | BYTE.OTP_EEPROM_PWM_BUFF_126 | |
| 07Fh | BYTE.OTP_EEPROM_PWM_BUFF_127 | |

### BYTE.OTP_EEPROM_PWM_BUFF_0

Holds data to be used to be transferred into the OTP or EEPROM. Please contact IDT for details.

Table 404: BYTE.OTP_EEPROM_PWM_BUFF_0 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_0 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 000h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_0 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_1

-

Table 405: BYTE.OTP_EEPROM_PWM_BUFF_1 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_1 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 001h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_1 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_2

-

Table 406: BYTE.OTP_EEPROM_PWM_BUFF_2 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_2 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 002h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_2 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_3

-

Table 407: BYTE.OTP_EEPROM_PWM_BUFF_3 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_3 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 003h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_3 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_4

-

Table 408: BYTE.OTP_EEPROM_PWM_BUFF_4 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_4 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_4 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_5

-

Table 409: BYTE.OTP_EEPROM_PWM_BUFF_5 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_5 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 005h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_5 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_6

-

Table 410: BYTE.OTP_EEPROM_PWM_BUFF_6 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_6 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 006h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_6 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_7

-

Table 411: BYTE.OTP_EEPROM_PWM_BUFF_7 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_7 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 007h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_7 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_8

-

Table 412: BYTE.OTP_EEPROM_PWM_BUFF_8 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_8 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 008h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_8 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_9

-

Table 413: BYTE.OTP_EEPROM_PWM_BUFF_9 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_9 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 009h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_9 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_10

-

Table 414: BYTE.OTP_EEPROM_PWM_BUFF_10 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_10 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ah | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_10 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_11

-

Table 415: BYTE.OTP_EEPROM_PWM_BUFF_11 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_11 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Bh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_11 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_12

-

Table 416: BYTE.OTP_EEPROM_PWM_BUFF_12 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_12 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Ch | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_12 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_13

-

Table 417: BYTE.OTP_EEPROM_PWM_BUFF_13 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_13 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Dh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_13 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_14

-

Table 418: BYTE.OTP_EEPROM_PWM_BUFF_14 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_14 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Eh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_14 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_15

-

Table 419: BYTE.OTP_EEPROM_PWM_BUFF_15 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_15 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00Fh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_15 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_16

-

Table 420: BYTE.OTP_EEPROM_PWM_BUFF_16 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_16 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 010h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_16 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_17

-

Table 421: BYTE.OTP_EEPROM_PWM_BUFF_17 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_17 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 011h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_17 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_18

-

Table 422: BYTE.OTP_EEPROM_PWM_BUFF_18 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_18 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 012h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_18 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_19

-

Table 423: BYTE.OTP_EEPROM_PWM_BUFF_19 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_19 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 013h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_19 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_20

-

Table 424: BYTE.OTP_EEPROM_PWM_BUFF_20 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_20 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 014h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_20 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_21

-

Table 425: BYTE.OTP_EEPROM_PWM_BUFF_21 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_21 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 015h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_21 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_22

-

Table 426: BYTE.OTP_EEPROM_PWM_BUFF_22 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_22 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 016h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_22 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_23

-

Table 427: BYTE.OTP_EEPROM_PWM_BUFF_23 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_23 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 017h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_23 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_24

-

Table 428: BYTE.OTP_EEPROM_PWM_BUFF_24 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_24 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 018h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_24 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_25

-

Table 429: BYTE.OTP_EEPROM_PWM_BUFF_25 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_25 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 019h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_25 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_26

-

Table 430: BYTE.OTP_EEPROM_PWM_BUFF_26 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_26 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Ah | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_26 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_27

-

Table 431: BYTE.OTP_EEPROM_PWM_BUFF_27 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_27 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Bh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_27 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_28

-

Table 432: BYTE.OTP_EEPROM_PWM_BUFF_28 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_28 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Ch | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_28 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_29

-

Table 433: BYTE.OTP_EEPROM_PWM_BUFF_29 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_29 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Dh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_29 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_30

-

Table 434: BYTE.OTP_EEPROM_PWM_BUFF_30 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_30 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Eh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_30 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_31

-

Table 435: BYTE.OTP_EEPROM_PWM_BUFF_31 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_31 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01Fh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_31 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_32

-

Table 436: BYTE.OTP_EEPROM_PWM_BUFF_32 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_32 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 020h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_32 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_33

-

Table 437: BYTE.OTP_EEPROM_PWM_BUFF_33 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_33 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 021h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_33 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_34

-

Table 438: BYTE.OTP_EEPROM_PWM_BUFF_34 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_34 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 022h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_34 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_35

-

Table 439: BYTE.OTP_EEPROM_PWM_BUFF_35 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_35 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 023h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_35 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_36

-

Table 440: BYTE.OTP_EEPROM_PWM_BUFF_36 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_36 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 024h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_36 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_37

-

Table 441: BYTE.OTP_EEPROM_PWM_BUFF_37 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_37 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 025h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_37 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_38

-

Table 442: BYTE.OTP_EEPROM_PWM_BUFF_38 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_38 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 026h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_38 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_39

-

Table 443: BYTE.OTP_EEPROM_PWM_BUFF_39 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_39 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 027h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_39 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_40

-

Table 444: BYTE.OTP_EEPROM_PWM_BUFF_40 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_40 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 028h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_40 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_41

-

Table 445: BYTE.OTP_EEPROM_PWM_BUFF_41 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_41 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 029h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_41 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_42

-

Table 446: BYTE.OTP_EEPROM_PWM_BUFF_42 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_42 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 02Ah | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_42 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_43

-

Table 447: BYTE.OTP_EEPROM_PWM_BUFF_43 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_43 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 02Bh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_43 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_44

-

Table 448: BYTE.OTP_EEPROM_PWM_BUFF_44 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_44 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 02Ch | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_44 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_45

-

Table 449: BYTE.OTP_EEPROM_PWM_BUFF_45 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_45 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 02Dh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_45 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_46

-

Table 450: BYTE.OTP_EEPROM_PWM_BUFF_46 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_46 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 02Eh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_46 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_47

-

Table 451: BYTE.OTP_EEPROM_PWM_BUFF_47 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_47 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 02Fh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_47 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_48

-

Table 452: BYTE.OTP_EEPROM_PWM_BUFF_48 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_48 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 030h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_48 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_49

-

Table 453: BYTE.OTP_EEPROM_PWM_BUFF_49 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_49 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 031h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_49 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_50

-

Table 454: BYTE.OTP_EEPROM_PWM_BUFF_50 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_50 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 032h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_50 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_51

-

Table 455: BYTE.OTP_EEPROM_PWM_BUFF_51 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_51 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 033h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_51 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_52

-

Table 456: BYTE.OTP_EEPROM_PWM_BUFF_52 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_52 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 034h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_52 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_53

-

Table 457: BYTE.OTP_EEPROM_PWM_BUFF_53 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_53 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 035h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_53 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_54

-

Table 458: BYTE.OTP_EEPROM_PWM_BUFF_54 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_54 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 036h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_54 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_55

-

Table 459: BYTE.OTP_EEPROM_PWM_BUFF_55 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_55 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 037h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_55 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_56

-

Table 460: BYTE.OTP_EEPROM_PWM_BUFF_56 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_56 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 038h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_56 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_57

-

Table 461: BYTE.OTP_EEPROM_PWM_BUFF_57 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_57 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 039h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_57 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_58

-

Table 462: BYTE.OTP_EEPROM_PWM_BUFF_58 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_58 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 03Ah | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_58 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_59

-

Table 463: BYTE.OTP_EEPROM_PWM_BUFF_59 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_59 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 03Bh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_59 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_60

-

Table 464: BYTE.OTP_EEPROM_PWM_BUFF_60 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_60 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 03Ch | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_60 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_61

-

Table 465: BYTE.OTP_EEPROM_PWM_BUFF_61 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_61 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 03Dh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_61 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_62

-

Table 466: BYTE.OTP_EEPROM_PWM_BUFF_62 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_62 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 03Eh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_62 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_63

-

Table 467: BYTE.OTP_EEPROM_PWM_BUFF_63 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_63 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 03Fh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_63 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_64

-

Table 468: BYTE.OTP_EEPROM_PWM_BUFF_64 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_64 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 040h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_64 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_65

-

Table 469: BYTE.OTP_EEPROM_PWM_BUFF_65 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_65 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 041h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_65 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_66

-

Table 470: BYTE.OTP_EEPROM_PWM_BUFF_66 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_66 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 042h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_66 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_67

-

Table 471: BYTE.OTP_EEPROM_PWM_BUFF_67 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_67 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 043h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_67 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_68

-

Table 472: BYTE.OTP_EEPROM_PWM_BUFF_68 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_68 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 044h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_68 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_69

-

Table 473: BYTE.OTP_EEPROM_PWM_BUFF_69 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_69 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 045h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_69 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_70

-

Table 474: BYTE.OTP_EEPROM_PWM_BUFF_70 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_70 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 046h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_70 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_71

-

Table 475: BYTE.OTP_EEPROM_PWM_BUFF_71 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_71 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 047h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_71 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_72

-

Table 476: BYTE.OTP_EEPROM_PWM_BUFF_72 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_72 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 048h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_72 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_73

-

Table 477: BYTE.OTP_EEPROM_PWM_BUFF_73 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_73 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 049h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_73 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_74

-

Table 478: BYTE.OTP_EEPROM_PWM_BUFF_74 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_74 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 04Ah | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_74 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_75

-

Table 479: BYTE.OTP_EEPROM_PWM_BUFF_75 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_75 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 04Bh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_75 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_76

-

Table 480: BYTE.OTP_EEPROM_PWM_BUFF_76 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_76 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 04Ch | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_76 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_77

-

Table 481: BYTE.OTP_EEPROM_PWM_BUFF_77 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_77 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 04Dh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_77 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_78

-

Table 482: BYTE.OTP_EEPROM_PWM_BUFF_78 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_78 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 04Eh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_78 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_79

-

Table 483: BYTE.OTP_EEPROM_PWM_BUFF_79 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_79 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 04Fh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_79 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_80

-

Table 484: BYTE.OTP_EEPROM_PWM_BUFF_80 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_80 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 050h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_80 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_81

-

Table 485: BYTE.OTP_EEPROM_PWM_BUFF_81 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_81 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 051h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_81 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_82

-

Table 486: BYTE.OTP_EEPROM_PWM_BUFF_82 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_82 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 052h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_82 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_83

-

Table 487: BYTE.OTP_EEPROM_PWM_BUFF_83 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_83 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 053h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_83 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_84

-

Table 488: BYTE.OTP_EEPROM_PWM_BUFF_84 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_84 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 054h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_84 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_85

-

Table 489: BYTE.OTP_EEPROM_PWM_BUFF_85 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_85 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 055h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_85 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_86

-

Table 490: BYTE.OTP_EEPROM_PWM_BUFF_86 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_86 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 056h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_86 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_87

-

Table 491: BYTE.OTP_EEPROM_PWM_BUFF_87 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_87 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 057h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_87 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_88

-

Table 492: BYTE.OTP_EEPROM_PWM_BUFF_88 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_88 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 058h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_88 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_89

-

Table 493: BYTE.OTP_EEPROM_PWM_BUFF_89 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_89 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 059h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_89 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_90

-

Table 494: BYTE.OTP_EEPROM_PWM_BUFF_90 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_90 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 05Ah | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_90 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_91

-

Table 495: BYTE.OTP_EEPROM_PWM_BUFF_91 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_91 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 05Bh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_91 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_92

-

Table 496: BYTE.OTP_EEPROM_PWM_BUFF_92 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_92 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 05Ch | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_92 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_93

-

Table 497: BYTE.OTP_EEPROM_PWM_BUFF_93 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_93 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 05Dh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_93 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_94

-

Table 498: BYTE.OTP_EEPROM_PWM_BUFF_94 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_94 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 05Eh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_94 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_95

-

Table 499: BYTE.OTP_EEPROM_PWM_BUFF_95 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_95 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 05Fh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_95 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_96

-

Table 500: BYTE.OTP_EEPROM_PWM_BUFF_96 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_96 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 060h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_96 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_97

-

Table 501: BYTE.OTP_EEPROM_PWM_BUFF_97 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_97 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 061h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_97 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_98

-

Table 502: BYTE.OTP_EEPROM_PWM_BUFF_98 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_98 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 062h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_98 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_99

-

Table 503: BYTE.OTP_EEPROM_PWM_BUFF_99 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_99 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 063h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_99 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_100

-

Table 504: BYTE.OTP_EEPROM_PWM_BUFF_100 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_100 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 064h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_100 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_101

-

Table 505: BYTE.OTP_EEPROM_PWM_BUFF_101 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_101 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 065h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_101 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_102

-

Table 506: BYTE.OTP_EEPROM_PWM_BUFF_102 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_102 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 066h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_102 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_103

-

Table 507: BYTE.OTP_EEPROM_PWM_BUFF_103 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_103 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 067h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_103 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_104

-

Table 508: BYTE.OTP_EEPROM_PWM_BUFF_104 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_104 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 068h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_104 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_105

-

Table 509: BYTE.OTP_EEPROM_PWM_BUFF_105 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_105 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 069h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_105 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_106

-

Table 510: BYTE.OTP_EEPROM_PWM_BUFF_106 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_106 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 06Ah | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_106 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_107

-

Table 511: BYTE.OTP_EEPROM_PWM_BUFF_107 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_107 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 06Bh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_107 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_108

-

Table 512: BYTE.OTP_EEPROM_PWM_BUFF_108 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_108 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 06Ch | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_108 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_109

-

Table 513: BYTE.OTP_EEPROM_PWM_BUFF_109 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_109 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 06Dh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_109 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_110

-

Table 514: BYTE.OTP_EEPROM_PWM_BUFF_110 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_110 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 06Eh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_110 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_111

-

Table 515: BYTE.OTP_EEPROM_PWM_BUFF_111 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_111 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 06Fh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_111 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_112

-

Table 516: BYTE.OTP_EEPROM_PWM_BUFF_112 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_112 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 070h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_112 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_113

-

Table 517: BYTE.OTP_EEPROM_PWM_BUFF_113 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_113 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 071h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_113 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_114

-

Table 518: BYTE.OTP_EEPROM_PWM_BUFF_114 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_114 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 072h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_114 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_115

-

Table 519: BYTE.OTP_EEPROM_PWM_BUFF_115 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_115 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 073h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_115 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_116

-

Table 520: BYTE.OTP_EEPROM_PWM_BUFF_116 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_116 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 074h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_116 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_117

-

Table 521: BYTE.OTP_EEPROM_PWM_BUFF_117 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_117 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 075h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_117 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_118

-

Table 522: BYTE.OTP_EEPROM_PWM_BUFF_118 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_118 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 076h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_118 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_119

-

Table 523: BYTE.OTP_EEPROM_PWM_BUFF_119 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_119 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 077h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_119 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_120

-

Table 524: BYTE.OTP_EEPROM_PWM_BUFF_120 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_120 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 078h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_120 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_121

-

Table 525: BYTE.OTP_EEPROM_PWM_BUFF_121 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_121 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 079h | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_121 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_122

-

Table 526: BYTE.OTP_EEPROM_PWM_BUFF_122 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_122 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 07Ah | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_122 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_123

-

Table 527: BYTE.OTP_EEPROM_PWM_BUFF_123 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_123 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 07Bh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_123 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_124

-

Table 528: BYTE.OTP_EEPROM_PWM_BUFF_124 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_124 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 07Ch | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_124 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_125

-

Table 529: BYTE.OTP_EEPROM_PWM_BUFF_125 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_125 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 07Dh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_125 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_126

-

Table 530: BYTE.OTP_EEPROM_PWM_BUFF_126 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_126 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 07Eh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_126 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

### BYTE.OTP_EEPROM_PWM_BUFF_127

-

Table 531: BYTE.OTP_EEPROM_PWM_BUFF_127 Bit Field Locations and Descriptions

| Offset Address (Hex) | BYTE.OTP_EEPROM_PWM_BUFF_127 Bit Field Locations | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 07Fh | DATA[7:0] | | | | | | | |

| BYTE.OTP_EEPROM_PWM_BUFF_127 Bit Field Descriptions | | | |
|---|---|---|---|
| Bit Field Name | Field Type | Default Value | Description |
| DATA[7:0] | R/W | 0 | Data to be transferred into OTP, EEPROM or PWM. |

# Revision History

| Revision Date | Description of Change |
|---|---|
| September 30, 2020 | Fix description of tod_out_sync_enable<br>Fix inconsistent use of INPUTn and CLKm<br>Fix typo in description of SCSR_DPLL_PHASE_MEASUREMENT_CFG<br>Improve the description of GPIO_DPLL_INDICATOR<br>Improve the description of DPLL_MASTER_DIV<br>Fix the options of SCSR_OTP_STATUS<br>Improve the description of phase_lock_max_error<br>Improve the description of "fb_select_ref" in regards to qual/disqual of the input to the DPLL<br>Expanded options of FORCE_LOCK_INPUT[7:3] and MANUAL_REFERENCE[4:0] to include fb_clk<br>Fix description of register SCSR_IN_DIV<br>Improve the description of DPLLx_FILTER_STATUS<br>Improve the description of fbd_integer_mode_en<br>Improve the description of sdm_order |
| May 4, 2020 | Updated trigger register description to include 200 microsecond wait time after writing a trigger register.<br>Added missing DPLL_TRANS_CTRL.<br>Change GPIO_MAN_CLK_SEL_0 description from "input clock disqualify" to "manual clock select".<br>Change MAJ_REL, MIN_REL and HOTFIX_REL reset values to match the firmware version.<br>Fix DPLL_SYS_STATUS that RESERVED is bits [7:6].<br>Fix various typos. |
| January 20, 2020 | Updated to match v4.8(.7) register map / descriptions and Timing Commander Personality v8.1<br>Use new Renesas document template |
| November 04, 2019 | Updated default value for I2C in page 4 |
| June 13, 2019 | Updated to match v4.8 register map / descriptions and Timing Commander Personality v7.5<br>Note that there were no customer-visible register changes between v4.7.x and v4.8.x register maps |
| February 28, 2019 | Updated to match v4.7.4 register map / descriptions and Timing Commander Personality v7.4 |
| September 12, 2018 | Further improvements and clarifications to descriptions<br>Updated to match v4.7 register map and Timing Commander Personality v6.x |
| August 27, 2018 | Improved and clarified many register descriptions |
| July 3, 2018 | Updated to match v4.6 register map (pipeline 13472) and Timing Commander Personality v5.x<br>Added hardware revision ID register to the documentation. |
| June 11, 2018 | Updated Additional Documents table to match current datasheets |
| February 23, 2018 | Updated to match v4.5 register map (Pipeline 10035) and Timing Commander Personality v4.x |
| February 21, 2018 | Updated introductory text to highlight trigger register functionality.<br>Removed older history associated with Rev A silicon that is not being used any more.<br>Updated the version numbering to match other documentation. |
| November 2, 2017 | First release of this document for the Revision B silicon. Updated to match v4.0.0 / v4.0.1 (Pipeline 7017) and Timing Commander Personality v3.x |

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)


### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com


### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2026 Renesas Electronics Corporation. All rights reserved.