How to Use this Document

This document, working in conjunction with the 8A3xxxx Family Programming Guide, is targeted for programming the 8A35010 device. The 8A3xxxx Family Programming Guide contains information on how to access internal registers and what those registers do specifically for all devices in the 8A3xxxx family. Not all devices in the family support all the same features or quantities of logic blocks, however the register blocks all behave and are addressed at the same locations in all device. Some devices will not make use of all register blocks since the associated feature or block of circuitry may not be available in that particular device. This Programming Guide Addendum will indicate which register modules are support in the 8A35010 device.

In addition, there are several other pieces of documentation that describe specific functions or details that would overly burden this document. Table 1 shows related documents.

Table 1: Related Documentation for 8A35010

Document Title	Document Description
8A35010 Datasheet	Contains a functional overview of the device and hardware-design related details including pinouts, AC & DC specifications and applications information related to power filtering and terminations.
8A3xxx Family Programming Guide	Contains detailed register descriptions and address maps for all members of the family of devices. All devices use some subset of this register map.
8A35010 Programming Guide Addendum	Indicates which registers in the 8A3xxxx Family Programming Guide are supported by the 8A35010 device.
8A3xxxx Family EEPROM Configuration Guide	Describes how an External I^2C EEPROM has its contents structured to load device configurations for all devices in the 8A3xxxx family
8A3xxxx Family OTP Memory Programming Guide	Describes memory structure for internal one-time programmable memory and details the programming sequence to be followed for all devices in the 8A3xxxx family
8A35010 Evaluation Board Reference Manual	Describes the Evaluation Board for the 8A35010
8A35010 Timing Commander Personality User Manual	Detailed description of how to use IDT's Timing Commander configuration tool with the 8A35010

The table below indicates which register modules are present or not in the 8A35010 device. Rows that are greyed-out indicate register modules that are not supported in the 8A35010. Rows with a pink background indicate modules that are partially supported. Hyper-links will point to additional tables indicating which part(s) of the module are supported and which part(s) are not. Modules with white backgrounds are fully supported.

Please refer to the 8A3xxxx Family Programming Guide for further details on individual registers within the modules and the bit fields within those registers. Register addressing is the same for all family members.

Table 2: 8A35010 Register Set Module Index

Module Base Address (Hex)	Link	Module Description
C000h	Module: RESET_CTRL	General reset management
C014h	Module: GENERAL_STATUS	Chip hardware status registers
C080h	Module: STATUS	Live status of alarms and events
C0D0h	Module: GPIO_USER_CONTROL	GPIO user control

Table 2: 8A35010 Register Set Module Index

Module Base Address (Hex)	Link	Module Description
C100h	Module: STICKY_STATUS_CLEAR	Sticky status clear
C108h	Module: GPIO_TOD_NOTIFICATION_CLEAR	Clear GPIO output time of day read notification
C10Ch	Module: PWM_RANGING_STATUS_0	PWM status registers
C114h	PWM_RANGING_STATUS_1	Chip status registers. Same as PWM_RANGING_STATUS_0.
C11Ch	Module: ALERT_CFG	Notification configuration
C128h	Module: SYS_DPLL_XO	System DPLL XO configuration
C130h	Module: SYS_APLL	System APLL configuration
C13Ch	Module: SYS_APLL_CP	System APLL configuration
C144h	Module: INPUT_0	Input configuration
C154h	INPUT_1	Input configuration. Same as INPUT_0.
C164h	INPUT_2	Input configuration. Same as INPUT_0.
C180h	INPUT_3	Input configuration. Same as INPUT_0.
C190h	INPUT_4	Input configuration. Same as INPUT_0.
C1A0h	INPUT_5	Input configuration. Same as INPUT_0.
C1B0h	INPUT_6	Input configuration. Same as INPUT_0.
C1C0h	INPUT_7	Input configuration. Same as INPUT_0.
C1D0h	INPUT_8	Input configuration. Same as INPUT_0.
C1E0h	INPUT_9	Input configuration. Same as INPUT_0.
C200h	INPUT_10	Input configuration. Same as INPUT_0.
C210h	INPUT_11	Input configuration. Same as INPUT_0.
C220h	INPUT_12	Input configuration. Same as INPUT_0.
C230h	INPUT_13	Input configuration. Same as INPUT_0.

Table 2: 8A35010 Register Set Module Index

Module Base Address (Hex)	Link	Module Description
C240h	INPUT_14	Input configuration. Same as INPUT_0.
C250h	INPUT_15	Input configuration. Same as INPUT_0.
C260h	Module: REF_MON_0	Reference monitors
C268h	REF_MON_1	Reference monitors. Same as REF_MON_0.
C270h	REF_MON_2	Reference monitors. Same as REF_MON_0.
C280h	REF_MON_3	Reference monitors. Same as REF_MON_0.
C288h	REF_MON_4	Reference monitors. Same as REF_MON_0.
C290h	REF_MON_5	Reference monitors. Same as REF_MON_0.
C298h	REF_MON_6	Reference monitors. Same as REF_MON_0.
C2A0h	REF_MON_7	Reference monitors. Same as REF_MON_0.
C2A8h	REF_MON_8	Reference monitors. Same as REF_MON_0.
C2B0h	REF_MON_9	Reference monitors. Same as REF_MON_0.
C2B8h	REF_MON_10	Reference monitors. Same as REF_MON_0.
C2C0h	REF_MON_11	Reference monitors. Same as REF_MON_0.
C2C8h	REF_MON_12	Reference monitors. Same as REF_MON_0.
C2D0h	REF_MON_13	Reference monitors. Same as REF_MON_0.
C2D8h	REF_MON_14	Reference monitors. Same as REF_MON_0.
C2E0h	REF_MON_15	Reference monitors. Same as REF_MON_0.
C300h	Module: DPLL_0	DPLL0 registers
C33Ch	DPLL_1	DPLL1 registers. Same as DPLL_0.

Table 2: 8A35010 Register Set Module Index

Module Base Address (Hex)	Link	Module Description
C380h	DPLL_2	DPLL2 registers. Same as DPLL_0.
C3BCh	DPLL_3	DPLL3 registers. Same as DPLL_0.
C400h	DPLL_4	DPLL4 registers. Same as DPLL_0.
C43Ch	DPLL_5	DPLL5 registers. Same as DPLL_0.
C480h	DPLL_6	DPLL6 registers. Same as DPLL_0.
C4BCh	DPLL_7	DPLL7 registers. Same as DPLL_0.
C500h	Module: SYS_DPLL	SYS_DPLL registers
C580h	Module: DPLL_CTRL_0	DPLL0 control registers
C5B8h	DPLL_CTRL_1	DPLL1 control registers. Same as DPLL_CTRL_0.
C600h	DPLL_CTRL_2	DPLL2 control registers. Same as DPLL_CTRL_0.
C638h	DPLL_CTRL_3	DPLL3 control registers. Same as DPLL_CTRL_0.
C680h	DPLL_CTRL_4	DPLL4control registers. Same as DPLL_CTRL_0.
C6B8h	DPLL_CTRL_5	DPLL5 control registers. Same as DPLL_CTRL_0.
C700h	DPLL_CTRL_6	DPLL6 control registers. Same as DPLL_CTRL_0.
C738h	DPLL_CTRL_7	DPLL7 control registers. Same as DPLL_CTRL_0.
C780h	Module: SYS_DPLL_CTRL	DPLL0 control registers
C800h	Module: DPLL_PHASE_0	DPLL0 write phase
C804h	DPLL_PHASE_1	DPLL1 write phase. Same as DPLL_PHASE_0.
C808h	DPLL_PHASE_2	DPLL2 write phase. Same as DPLL_PHASE_0.
C80Ch	DPLL_PHASE_3	DPLL3 write phase. Same as DPLL_PHASE_0.
C810h	DPLL_PHASE_4	DPLL4 write phase. Same as DPLL_PHASE_0.

Table 2: 8A35010 Register Set Module Index

Module Base Address (Hex)	Link	Module Description
C814h	DPLL_PHASE_5	DPLL5 write phase. Same as DPLL_PHASE_0.
C818h	DPLL_PHASE_6	DPLL6 write phase. Same as DPLL_PHASE_0.
C81Ch	DPLL_PHASE_7	DPLL7 write phase. Same as DPLL_PHASE_0.
C820h	Module: DPLL_FREQ_0	DPLL0 write frequency
C830h	DPLL_FREQ_1	DPLL1 write frequency. Same as DPLL_FREQ_0.
C840h	DPLL_FREQ_2	DPLL2 write frequency. Same as DPLL_FREQ_0.
C850h	DPLL_FREQ_3	DPLL3 write frequency. Same as DPLL_FREQ_0.
C860h	DPLL_FREQ_4	DPLL4 write frequency. Same as DPLL_FREQ_0.
C880h	DPLL_FREQ_5	DPLL5 write frequency. Same as DPLL_FREQ_0.
C890h	DPLL_FREQ_6	DPLL6 write frequency. Same as DPLL_FREQ_0.
C8A0h	DPLL_FREQ_7	DPLL7 write frequency. Same as DPLL_FREQ_0.
C8B0h	Module: GPIO_CFG	GPIO global config
C900h	Module: GPIO_0	GPIO registers
C912h	GPIO_1	GPIO registers. Same as GPIO_0.
C924h	GPIO_2	GPIO registers. Same as GPIO_0.
C936h	GPIO_3	GPIO registers. Same as GPIO_0.
C948h	GPIO_4	GPIO registers. Same as GPIO_0.
C95Ah	GPIO_5	GPIO registers. Same as GPIO_0.
C980h	GPIO_6	GPIO registers. Same as GPIO_0.
C992h	GPIO_7	GPIO registers. Same as GPIO_0.
C9A4h	GPIO_8	GPIO registers. Same as GPIO_0.

Table 2: 8A35010 Register Set Module Index

Module Base Address (Hex)	Link	Module Description
C9B6h	GPIO_9	GPIO registers. Same as GPIO_0.
C9C8h	GPIO_10	GPIO registers. Same as GPIO_0.
C9DAh	GPIO_11	GPIO registers. Same as GPIO_0.
CA00h	GPIO_12	GPIO registers. Same as GPIO_0.
CA12h	GPIO_13	GPIO registers. Same as GPIO_0.
CA24h	GPIO_14	GPIO registers. Same as GPIO_0.
CA36h	GPIO_15	GPIO registers. Same as GPIO_0.
CA50h	Module: OUTPUT_0	Output registers
CA60h	OUTPUT_1	Output registers. Same as OUTPUT_0.
CA80h	OUTPUT_2	Output registers. Same as OUTPUT_0.
CA90h	OUTPUT_3	Output registers. Same as OUTPUT_0.
CAA0h	OUTPUT_4	Output registers. Same as OUTPUT_0.
CAB0h	OUTPUT_5	Output registers. Same as OUTPUT_0.
CAC0h	OUTPUT_6	Output registers. Same as OUTPUT_0.
CAD0h	OUTPUT_7	Output registers. Same as OUTPUT_0.
CB00h	OUTPUT_8	Output registers. Same as OUTPUT_0.
CB10h	OUTPUT_9	Output registers. Same as OUTPUT_0.
CB20h	OUTPUT_10	Output registers. Same as OUTPUT_0.
CB30h	OUTPUT_11	Output registers. Same as OUTPUT_0.
CB40h	Module: SERIAL	Serial Interfaces registers
CB4Ch	Module: PWM_ENCODER_0	PWM encoder registers

Table 2: 8A35010 Register Set Module Index

Module Base Address (Hex)	Link	Module Description
CB54h	PWM_ENCODER_1	PWM encoder registers. Same as PWM_ENCODER_0.
CB5Ch	PWM_ENCODER_2	PWM encoder registers. Same as PWM_ENCODER_0.
CB64h	PWM_ENCODER_3	PWM encoder registers. Same as PWM_ENCODER_0.
CB6Ch	PWM_ENCODER_4	PWM encoder registers. Same as PWM_ENCODER_0.
CB80h	PWM_ENCODER_5	PWM encoder registers. Same as PWM_ENCODER_0.
CB88h	PWM_ENCODER_6	PWM encoder registers. Same as PWM_ENCODER_0.
CB90h	PWM_ENCODER_7	PWM encoder registers. Same as PWM_ENCODER_0.
CB98h	Module: PWM_DECODER_0	PWM decoder registers
CBA0h	PWM_DECODER_1	PWM decoder registers. Same as PWM_DECODER_0.
CBA8h	PWM_DECODER_2	PWM decoder registers. Same as PWM_DECODER_0.
CBB0h	PWM_DECODER_3	PWM decoder registers. Same as PWM_DECODER_0.
CBB8h	PWM_DECODER_4	PWM decoder registers. Same as PWM_DECODER_0.
CBC0h	PWM_DECODER_5	PWM decoder registers. Same as PWM_DECODER_0.
CBC8h	PWM_DECODER_6	PWM decoder registers. Same as PWM_DECODER_0.
CBD0h	PWM_DECODER_7	PWM decoder registers. Same as PWM_DECODER_0.
CBD8h	PWM_DECODER_8	PWM decoder registers. Same as PWM_DECODER_0.
CBE0h	PWM_DECODER_9	PWM decoder registers. Same as PWM_DECODER_0.
CBE8h	PWM_DECODER_10	PWM decoder registers. Same as PWM_DECODER_0.
CC00h	PWM_DECODER_11	PWM decoder registers. Same as PWM_DECODER_0.
CC08h	PWM_DECODER_12	PWM decoder registers. Same as PWM_DECODER_0.

Table 2: 8A35010 Register Set Module Index

Module Base Address (Hex)	Link	Module Description
CC10h	PWM_DECODER_13	PWM decoder registers. Same as PWM_DECODER_0.
CC18h	PWM_DECODER_14	PWM decoder registers. Same as PWM_DECODER_0.
CC20h	PWM_DECODER_15	PWM decoder registers. Same as PWM_DECODER_0.
CC28h	Module: PWM_USER_DATA	PWM user data registers
CC40h	Module: TOD_0	ToD registers
CC44h	TOD_1	ToD registers. Same as TOD_0.
CC48h	TOD_2	ToD registers. Same as TOD_0.
CC4Ch	TOD_3	ToD registers. Same as TOD_0.
CC50h	Module: TOD_WRITE_0	Write ToD registers
CC60h	TOD_WRITE_1	Write ToD registers. Same as TOD_WRITE_0.
CC80h	TOD_WRITE_2	Write ToD registers. Same as TOD_WRITE_0.
CC90h	TOD_WRITE_3	Write ToD registers. Same as TOD_WRITE_0.
CCA0h	Module: TOD_READ_PRIMARY_0	Read ToD registers
CCB0h	TOD_READ_PRIMARY_1	Read ToD registers. Same as TOD_READ_PRIMARY_0.
CCC0h	TOD_READ_PRIMARY_2	Read ToD registers. Same as TOD_READ_PRIMARY_0.
CCD0h	TOD_READ_PRIMARY_3	Read ToD registers. Same as TOD_READ_PRIMARY_0.
CD00h	Module: TOD_READ_SECONDARY_0	Read ToD registers
CD10h	TOD_READ_SECONDARY_1	Read ToD registers. Same as TOD_READ_SECONDARY_0.
CD20h	TOD_READ_SECONDARY_2	Read ToD registers. Same as TOD_READ_SECONDARY_0.
CD30h	TOD_READ_SECONDARY_3	Read ToD registers. Same as TOD_READ_SECONDARY_0.

Table 2: 8A35010 Register Set Module Index

Module Base Address (Hex)	Link	Module Description
CF68h	Module: EEPROM	EEPROM registers
CF70h	Module: OTP	OTP registers
CF80h	Module: BYTE	OTP registers
D000h	RESERVED	This module must not be modified from the read value

Module: STATUS

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Table 3: STATUS Register Index

Offset (Hex)	Register Module Base Address: C080h	
	Individual Register Name	Register Description
000h	STATUS.I2CM_STATUS	I2C master configuration state
001h	RESERVED	This register must not be modified from the read value
002h	STATUS.SER0_STATUS	Slave serial interface configuration state
003h	STATUS.SER0_SPI_STATUS	SPI configuration state
004h	STATUS.SER0_I2C_STATUS	I2C slave configuration state
005h	STATUS.SER1_STATUS	Slave serial interface configuration state
006h	STATUS.SER1_SPI_STATUS	SPI configuration state
007h	STATUS.SER1_I2C_STATUS	I2C slave configuration state
008h	STATUS.IN0_MON_STATUS	Input reference monitor status
009h	STATUS.IN1_MON_STATUS	Input reference monitor status
00Ah	STATUS.IN2_MON_STATUS	Input reference monitor status
00Bh	STATUS.IN3_MON_STATUS	Input reference monitor status
00Ch	STATUS.IN4_MON_STATUS	Input reference monitor status
00Dh	STATUS.IN5_MON_STATUS	Input reference monitor status
00Eh	STATUS.IN6_MON_STATUS	Input reference monitor status
00Fh	STATUS.IN7_MON_STATUS	Input reference monitor status
010h	STATUS.IN8_MON_STATUS	Input reference monitor status
011h	STATUS.IN9_MON_STATUS	Input reference monitor status
012h	STATUS.IN10_MON_STATUS	Input reference monitor status
013h	STATUS.IN11_MON_STATUS	Input reference monitor status
014h	STATUS.IN12_MON_STATUS	Input reference monitor status
015h	STATUS.IN13_MON_STATUS	Input reference monitor status
016h	STATUS.IN14_MON_STATUS	Input reference monitor status

Table 3: STATUS Register Index

Offset (Hex)	Register Module Base Address: C080h	
	Individual Register Name	Register Description
017h	STATUS.IN15_MON_STATUS	Input reference monitor status
018h	STATUS.DPLL0_STATUS	DPLL status
019h	STATUS.DPLL1_STATUS	DPLL status
01Ah	STATUS.DPLL2_STATUS	DPLL status
01Bh	STATUS.DPLL3_STATUS	DPLL status
01Ch	STATUS.DPLL4_STATUS	DPLL status
01Dh	STATUS.DPLL5_STATUS	DPLL status
01Eh	STATUS.DPLL6_STATUS	DPLL status
01Fh	STATUS.DPLL7_STATUS	DPLL status
020h	STATUS.DPLL_SYS_STATUS	System DPLL status
021h	STATUS.SYS_APLL_STATUS	System APLL status
022h	STATUS.DPLL0_REF_STAT	DPLL input reference status
023h	STATUS.DPLL1_REF_STAT	DPLL input reference status
024h	STATUS.DPLL2_REF_STAT	DPLL input reference status
025h	STATUS.DPLL3_REF_STAT	DPLL input reference status
026h	STATUS.DPLL4_REF_STAT	DPLL input reference status
027h	STATUS.DPLL5_REF_STAT	DPLL input reference status
028h	STATUS.DPLL6_REF_STAT	DPLL input reference status
029h	STATUS.DPLL7_REF_STAT	DPLL input reference status
02Ah	STATUS.DPLL_SYS_REF_STAT	System DPLL input reference status
02Bh	STATUS.USER_GPIO0_TO_7_STATUS	User controlled GPIO level
02Ch	STATUS.USER_GPIO8_TO_15_STATUS	User controlled GPIO level
02Eh	STATUS.IN0_MON_FREQ_STATUS	Input reference monitor frequency status
030h	STATUS.IN1_MON_FREQ_STATUS	Input reference monitor frequency status
032h	STATUS.IN2_MON_FREQ_STATUS	Input reference monitor frequency status
034h	STATUS.IN3_MON_FREQ_STATUS	Input reference monitor frequency status
036h	STATUS.IN4_MON_FREQ_STATUS	Input reference monitor frequency status
038h	STATUS.IN5_MON_FREQ_STATUS	Input reference monitor frequency status
03Ah	STATUS.IN6_MON_FREQ_STATUS	Input reference monitor frequency status
03Ch	STATUS.IN7_MON_FREQ_STATUS	Input reference monitor frequency status
03Eh	STATUS.IN8_MON_FREQ_STATUS	Input reference monitor frequency status
040h	STATUS.IN9_MON_FREQ_STATUS	Input reference monitor frequency status

Table 3: STATUS Register Index

Offset (Hex)	Register Module Base Address: C080h	
	Individual Register Name	Register Description
042h	STATUS.IN10_MON_FREQ_STATUS	Input reference monitor frequency status
044h	STATUS.IN11_MON_FREQ_STATUS	Input reference monitor frequency status
046h	STATUS.IN12_MON_FREQ_STATUS	Input reference monitor frequency status
048h	STATUS.IN13_MON_FREQ_STATUS	Input reference monitor frequency status
04Ah	STATUS.IN14_MON_FREQ_STATUS	Input reference monitor frequency status
04Ch	STATUS.IN15_MON_FREQ_STATUS	Input reference monitor frequency status

Module: STICKY_STATUS_CLEAR

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Table 4: STICKY_STATUS_CLEAR Register Index

Offset (Hex)	Register Module Base Address: C100h	
	Individual Register Name	Register Description
000h	STICKY_STATUS_CLEAR.IN0_TO_7_MON_STICKY_STATUS_CLEAR	Clear sticky reference monitor status
001h	STICKY_STATUS_CLEAR.IN8_TO_15_MON_STICKY_STATUS_CLEAR	Clear sticky reference monitor status
002h	STICKY_STATUS_CLEAR.DPLL_STICKY_STATUS_CLEAR	Clear sticky DPLL status
003h	STICKY_STATUS_CLEAR.DPLL_SYS_STICKY_STATUS_CLEAR	Clear sticky System DPLL status
004h	STICKY_STATUS_CLEAR.SYS_APLL_STICKY_STATUS_CLEAR	Clear sticky system APLL status
005h	STICKY_STATUS_CLEAR.ALL_STICKY_STATUS_CLEAR	Clear all sticky status bits

Module: ALERT_CFG

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Table 5: ALERT_CFG Register Index

Offset (Hex)	Register Module Base Address: C11Ch	
	Individual Register Name	Register Description
000h	ALERT_CFG.IN1_0_MON_ALERT_MASK	GPIO alert mask for monitors 0, 1
001h	ALERT_CFG.IN3_2_MON_ALERT_MASK	GPIO alert mask for monitors 2, 3
002h	ALERT_CFG.IN5_4_MON_ALERT_MASK	GPIO alert mask for monitors 4, 5
003h	ALERT_CFG.IN7_6_MON_ALERT_MASK	GPIO alert mask for monitors 6, 7

Table 5: ALERT_CFG Register Index

Offset (Hex)	Register Module Base Address: C11Ch	
	Individual Register Name	Register Description
004h	ALERT_CFG.IN9_8_MON_ALERT_MASK	GPIO alert mask for monitors 8, 9
005h	ALERT_CFG.IN11_10_MON_ALERT_MASK	GPIO alert mask for monitors 10, 11
006h	ALERT_CFG.IN13_12_MON_ALERT_MASK	GPIO alert mask for monitors 12, 13
007h	ALERT_CFG.IN15_14_MON_ALERT_MASK	GPIO alert mask for monitors 14, 15
008h	ALERT_CFG.DPLL3_2_1_0_ALERT_MASK	GPIO alert mask for DPLLs 0, 1, 2, 3
009h	ALERT_CFG.DPLL7_6_5_4_ALERT_MASK	GPIO alert mask for DPLLs 4, 5, 6, 7
00Ah	ALERT_CFG.SYS_ALERT_MASK	GPIO alert mask for System DPLL and APLL

Module: REF_MON_0

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Table 6: REF_MON_0 Register Index

Offset (Hex)	Register Module Base Address: C260h[1]	
	Individual Register Name	Register Description
000h	REF_MON_0.IN_MON_FREQ_CFG	Reference monitor frequency configuration.
002h	REF_MON_0.IN_MON_DSQF_INTV	Reference frequency disqualification interval.
003h	REF_MON_0.IN_MON_ACT_CFG	Activity limit and disqualifications timers.
004h	REF_MON_0.IN_MON_LOS_CFG	Loss of signal configuration
005h	REF_MON_0.IN_MON_CFG	Reference monitor configuration.

1. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

Module: DPLL_0

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Table 7: DPLL_0 Register Index

Offset (Hex)	Register Module Base Address: C300h[1]	
	Individual Register Name	Register Description
000h	DPLL_0.DPLL_SM_SIZE	Configure frequency step size for GPIO increment/decrement mode
002h	DPLL_0.DPLL_CTRL_0	Reference switching configuration.
003h	DPLL_0.DPLL_CTRL_1	Forced lock reference selection.
004h	DPLL_0.DPLL_CTRL_2	External feedback and frame/sync pulse configuration
005h	DPLL_0.DPLL_HO_ADVCD_CFG_0	Advanced holdover configuration.
006h	DPLL_0.DPLL_HO_ADVCD_CFG_1	Advanced holdover configuration.

Table 7: DPLL_0 Register Index

Offset (Hex)	Register Module Base Address: C300h[1]	
	Individual Register Name	Register Description
007h	DPLL_0.DPLL_HO_CFG	Holdover configuration.
008h	DPLL_0.DPLL_LOCK_0	Phase lock threshold.
009h	DPLL_0.DPLL_LOCK_1	Phase lock monitor duration.
00Ah	DPLL_0.DPLL_LOCK_2	Frequency lock threshold.
00Bh	DPLL_0.DPLL_LOCK_3	Frequency lock monitor duration.
00Ch	DPLL_0.DPLL_REF_PRIORITY_0	Select input for highest (0) priority.
00Dh	DPLL_0.DPLL_REF_PRIORITY_1	Select input for priority 1.
00Eh	DPLL_0.DPLL_REF_PRIORITY_2	Select input for priority 2.
00Fh	DPLL_0.DPLL_REF_PRIORITY_3	Select input for priority 3.
010h	DPLL_0.DPLL_REF_PRIORITY_4	Select input for priority 4.
011h	DPLL_0.DPLL_REF_PRIORITY_5	Select input for priority 5.
012h	DPLL_0.DPLL_REF_PRIORITY_6	Select input for priority 6.
013h	DPLL_0.DPLL_REF_PRIORITY_7	Select input for priority 7.
014h	DPLL_0.DPLL_REF_PRIORITY_8	Select input for priority 8.
015h	DPLL_0.DPLL_REF_PRIORITY_9	Select input for priority 9.
016h	DPLL_0.DPLL_REF_PRIORITY_10	Select input for priority 10.
017h	DPLL_0.DPLL_REF_PRIORITY_11	Select input for priority 11.
018h	DPLL_0.DPLL_REF_PRIORITY_12	Select input for priority 12.
019h	DPLL_0.DPLL_REF_PRIORITY_13	Select input for priority 13.
01Ah	DPLL_0.DPLL_REF_PRIORITY_14	Select input for priority 14.
01Bh	DPLL_0.DPLL_REF_PRIORITY_15	Select input for priority 15.
01Ch	DPLL_0.DPLL_REF_PRIORITY_16	Select input for priority 16.
01Dh	DPLL_0.DPLL_REF_PRIORITY_17	Select input for priority 17.
01Eh	RESERVED	This register must not be modified from the read value
01Fh	RESERVED	This register must not be modified from the read value
020h	RESERVED	This register must not be modified from the read value
021h	RESERVED	This register must not be modified from the read value
022h	RESERVED	This register must not be modified from the read value
023h	RESERVED	This register must not be modified from the read value
024h	RESERVED	This register must not be modified from the read value
025h	RESERVED	This register must not be modified from the read value
026h	DPLL_0.DPLL_FASTLOCK_CFG_0	Fast lock configuration for lock acquisition and recovery states.

Table 7: DPLL_0 Register Index

Offset (Hex)	Register Module Base Address: C300h[1]	
	Individual Register Name	Register Description
027h	DPLL_0.DPLL_FASTLOCK_CFG_1	Fast lock configuration.
028h	DPLL_0.DPLL_FASTLOCK_PSL	Fast lock phase slope limit.
02Ah	DPLL_0.DPLL_FASTLOCK_FSL	Fast lock frequency slope limit.
02Ch	DPLL_0.DPLL_FASTLOCK_BW	Fast lock loop filter bandwidth .
02Eh	DPLL_0.DPLL_MAX_FREQ_OFFSET	DPLL maximum frequency offset limit
030h	DPLL_0.DPLL_WRITE_PHASE_TIMER	Write phase timer.
032h	DPLL_0.DPLL_PRED_CFG	Pre-defined configuration selection.
033h	DPLL_0.DPLL_COMBO_SLAVE_CFG0	Combo mode slave primary source configuration.
034h	DPLL_0.DPLL_COMBO_SLAVE_CFG1	Combo mode slave secondary source configuration.
035h	DPLL_0.DPLL_COMBO_MASTER_CFG	Combo mode master configuration
036h	DPLL_0.DPLL_SLAVE_REF_CFG	Slave mode configuration.
037h	DPLL_0.DPLL_REF_MODE	Reference switching control configuration.
038h	DPLL_0.DPLL_MODE	DPLL operating modes.

1. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

Module: DPLL_CTRL_0

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Table 8: DPLL_CTRL_0 Register Index

Offset (Hex)	Register Module Base Address: C580h[1]	
	Individual Register Name	Register Description
000h	DPLL_CTRL_0.DPLL_HS_TIE_RESET	Reset hitless switching time interval error.
001h	DPLL_CTRL_0.DPLL_MANU_REF_CFG	Select reference to be used for manual reference selection mode.
002h	DPLL_CTRL_0.DPLL_DAMPING	DPLL loop damping factor
003h	DPLL_CTRL_0.DPLL_DECIMATOR_BW_MULT	DPLL decimator bandwidth multiplier
004h	DPLL_CTRL_0.DPLL_BW	DPLL bandwidth.
006h	DPLL_CTRL_0.DPLL_PSL	DPLL phase slope limit.
008h	DPLL_CTRL_0.DPLL_PRED0_DAMPING	Pre-defined configuration 0 damping factor.
009h	DPLL_CTRL_0.DPLL_PRED0_DECIMATOR_BW_MULT	Pre-defined configuration 0 decimator bandwidth multiplier.
00Ah	DPLL_CTRL_0.DPLL_PRED0_BW	Pre-defined configuration 0 bandwidth.
00Ch	DPLL_CTRL_0.DPLL_PRED0_PSL	Pre-defined configuration 0 phase slope limit.
00Eh	DPLL_CTRL_0.DPLL_PRED1_DAMPING	Pre-defined configuration 1 damping factor.

Table 8: DPLL_CTRL_0 Register Index

Offset (Hex)	Register Module Base Address: C580h[1]	
	Individual Register Name	Register Description
00Fh	DPLL_CTRL_0.DPLL_PRED1_DECIMATOR_BW_MULT	Pre-defined configuration 1 decimator bandwidth multiplier.
010h	DPLL_CTRL_0.DPLL_PRED1_BW	Pre-defined configuration 1 bandwidth.
012h	DPLL_CTRL_0.DPLL_PRED1_PSL	Pre-defined configuration 1 phase slope limit.
014h	DPLL_CTRL_0.DPLL_PHASE_OFFSET_CFG	DPLL tracks reference with specified offset.
01Ch	DPLL_CTRL_0.DPLL_FOD_FREQ	Fractional Output Divider (FOD) frequency in Hz.
024h	DPLL_CTRL_0.DPLL_MASTER_DIV	Master divider value.
028h	DPLL_CTRL_0.DPLL_COMBO_SW_VALUE_CNFG	Write DCO FFO value to be added to combo bus.
02Eh	RESERVED	This register must not be modified from the read value
02Fh	RESERVED	This register must not be modified from the read value
030h	DPLL_CTRL_0.DPLL_MANUAL_HOLDOVER_VALUE	Hardware DCO value to be used for manual holdover.
036h	RESERVED	This register must not be modified from the read value
037h	RESERVED	This register must not be modified from the read value

1. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

Module: GPIO_0

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Table 9: GPIO_0 Register Index

Offset (Hex)	Register Module Base Address: C900h[1]	
	Individual Register Name	Register Description
000h	GPIO_0.GPIO_SM	Increment/decrement DCO FFO configuration.
001h	GPIO_0.GPIO_OUT_CTRL_0	GPIO controlled output squelch, outputs 0-7.
002h	GPIO_0.GPIO_OUT_CTRL_1	GPIO controlled output squelch, outputs 8-11.
003h	GPIO_0.GPIO_TOD_TRIG	GPIO controlled ToD trigger input.
004h	GPIO_0.GPIO_DPLL_INDICATOR	GPIO output of DPLL lock and holdover states.
005h	GPIO_0.GPIO_LOS_INDICATOR	GPIO output of DPLL loss of signal (LoS).
006h	GPIO_0.GPIO_REF_INPUT_DSQ_0	GPIO controlled input disqualification for inputs 0-7.
007h	GPIO_0.GPIO_REF_INPUT_DSQ_1	GPIO controlled input disqualification for inputs 8-15.
008h	GPIO_0.GPIO_REF_INPUT_DSQ_2	GPIO controlled input disqualification for DPLLs.
009h	GPIO_0.GPIO_REF_INPUT_DSQ_3	GPIO controlled input disqualification for System DPLL and disqualification level.

Table 9: GPIO_0 Register Index

Offset (Hex)	Register Module Base Address: C900h[1]	
	Individual Register Name	Register Description
00Ah	GPIO_0.GPIO_MAN_CLK_SEL_0	GPIO controlled manual clock selection.
00Bh	GPIO_0.GPIO_MAN_CLK_SEL_1	DPLLs to be controlled by manual clock selection.
00Ch	GPIO_0.GPIO_MAN_CLK_SEL_2	DPLLs to be controlled by manual clock selection.
00Dh	GPIO_0.GPIO_SLAVE	GPIO controlled device slave mode.
00Eh	GPIO_0.GPIO_ALERT_OUT_CFG	GPIO output for indicating alerts.
00Fh	GPIO_0.GPIO_TOD_NOTIFICATION_CFG	GPIO output configuration for DPLL ToD.
010h	GPIO_0.GPIO_CTRL	Select GPIO function.

1. This register module is instantiated multiple times. This is the base address of the first instantiation of this module. For later instantiations, use the appropriate module base address.

Module: SERIAL

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Table 10: SERIAL Register Index

Offset (Hex)	Register Module Base Address: CB40h	
	Individual Register Name	Register Description
000h	SERIAL.I2CM	I2C Master configuration.
001h	RESERVED	This register must not be modified from the read value
002h	SERIAL.SER0	Slave serial interface 0 configuration.
003h	SERIAL.SER0_SPI	SPI configuration, serial interface 0.
004h	SERIAL.SER0_I2C	I2C configuration, serial interface 0.
005h	SERIAL.SER1	Slave serial interface 1 configuration.
006h	SERIAL.SER1_SPI	SPI configuration, serial interface 1.
007h	SERIAL.SER1_I2C	I2C configuration, serial interface 1.
008h	SERIAL.SER_APPLY_CONFIG	Trigger serial configuration changes.

Revision History

Revision Date	Description of Change
July 18, 2017	First release of the *8A35010 Programming Guide Addendum* Created to match FW Build 4595 and Timing Commander Personality v0.58

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