200 kHz Phase Shift Full Bridge for 3.3kW Electric Vehicle On-board Charger

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Introduction

Phase Shift Full Bridge (PSFB) is a classic topology for applications requiring a wide range of voltage transfer ratio, such as battery chargers. An advantage of this circuit over an LLC topology is that it does not require either variable switching frequency or a variable DC-link voltage to regulate the battery voltage. However, there is one imperfection in PSFBs: while soft switching is achievable at high load, the devices inevitably enter hard switching at low load.

For PSFBs, compared to traditional Si devices, Renesas GaN FETs offer:

- High switching frequency and high power density
- Large phase shift angle and high efficiency
- Extensive soft switching region
- Low loss during hard switching

These benefits are a result of.

- Low Output Charge (Q_{oss})
- Low Switching Losses

With GaN, PSFBs become more competitive than ever. To further improve efficiency, an active snubber is adopted as a replacement for the conventional RCD snubber as shown in the schematic.

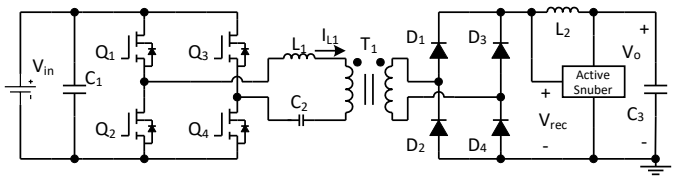


Figure 1. Simplified schematic of the 200 kHz PSFB

Converter Design

A prototype of the PSFB was designed using the 72mΩ GaN FET (TPH3212PS), shown in Fig. 2. The key specifications of the prototype is summarized below in Table 1.

Figure 2. TPH3212PS 200kHz 3.3kW PSFB prototype

Table I Key parameters of the PSFB

DC-link Voltage (V)	380 ~ 410
Battery Voltage (V)	250 ~ 450
Maximum Power (W)	3300
Maximum Current (A)	11
Switching frequency (kHz)	200
Transformer turns ratio	1:1.18
Leakage inductance (μH)	1.0
Resonant inductor (μH)	1.7
Output inductor (μH)	65
DC blocking capacitor (μF)	5

As can be found in Table I, resonant inductance is about 2.7 μH, which is the combination of two inductances; leakage and resonant inductance. This resonant inductance allows di/dt as high as 150 A/μs with 410 V DC-link, which significantly increases the maximum phase shift angle, consequently reducing power loss caused by the freewheeling time. This trick can easily push the angle over 0.9π (the higher the angle the less free-wheeling time required), which allows the turns-ratio of transformer to be reduced and further improving the efficiency. Using this technique a 450 V battery can be charged with a 410 V DC-link and 0.93π phase shift. The high di/dt allows 26 A of current to be reached in 175ns at a power level of 3600 W in Fig. 3. Ch2 demonstrates I_{L1} changing 25A, from -11A to 14A around the trigger point, and Ch4 gives V_{rec} as labeled in Fig. 1.

$$di/dt = 410V/2.7\ \mu H = 150\ A/\mu s$$

$$Phs_{450V\_max} = \pi \times 450\ V/(410\ V \times 1.18) = 0.93\pi$$

$$dt_{450V\_max} = 0.5 \times 5\ \mu s \times (\pi - 0.93\pi)/\pi = 0.175\ \mu s$$

$$di_{450V\_max} = 150\ A/\mu s \times 0.175\ \mu s = 26\ A$$

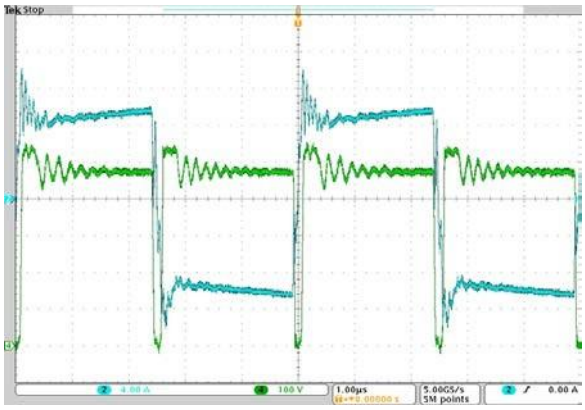


Figure 3. I_{L1} and V_{rec} at 410V DC-link, 450V Battery, 3.6kW

As noted in Fig. 3, voltage spike on V_{rec} is clamped around 540V by the active snubber. The active snubber is developed with off-line switchers, such as the STMicroelectronic's VIPER06HS or ON Semiconductor's NCP1060AD100. A simplified schematic of the active snubber circuit is given in Fig. 4.

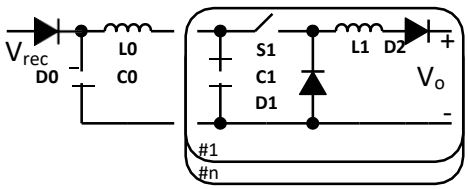


Figure 4. Simplified schematic of the active snubber

As shown in Fig. 1 and 4, the active snubber has three terminals connected to V_{rec} and V_o. It is composed of two parts, an input filter and switcher cells. The components are summarized in Table 2.

Table 2 Key components of the active snubber

C0 (μF)	0.5
L0 (μH)	10
C1 (μF)	0.2
L1 (μH)	2700
D0	SCS206
S1	VIPER06HS, or NCP1060AD100
D1, D2	ES1J

The switcher, S1, is configured to work with constant peak current. This configuration only requires tuning of the compensation resistor shown within its respective datasheet. In this design, the snubber is composed by three switcher cells and able to pump 100s mA depending on the requirement from the parasitic capacitance of transformer (T1), and rectifiers (D1~D4) in Fig. 1. The junction capacitance of D0 in Fig. 4 also contributes to the parasitic capacitance. In this design, D1~D4 are 650 V SiC Schottky SCS210 diodes, and D0 in Fig. 4 is SCS206 diode. By tuning the compensation resistor in the switcher circuits, the overshoot caused by the parasitic components can be clamped at desired V_{rec} as demonstrated in Fig. 3.

The dead time must be shorter than 175ns to give 0.93π phase shift. Soft switching and device characteristics are discussed in detail later on in this design guide. Table 3

shows the GaN FET and Si MOSFET discussed in the soft switching analysis.

Table 3 Comparison of output charge and energy

	$R_{on(tpy)}$ (mΩ)	$C_{o(tr)\_400V}$ (pF)	$C_{o(er)\_400V}$ (pF)
TPH3212PS	72	225	142
IPP60R090CFD7	75	751	73

Q1 and Q2 in Fig. 1 compose the lagging phase leg, which starts its transition before power transfer. Q3 and Q4 compose the leading phase leg, which starts its transition after power transfer. Since I_{L1} is always higher at the end of power transfer, it is always easier for the leading leg to obtain soft switching. In other words, the lagging leg loses soft switching at higher power than the leading leg does.

In the following discussion, the switching transition after Q1 turned-off is studied for both soft and hard switching. An ideal soft switching waveform along with a simplified circuit diagram are sketched in Fig. 5. Q1 is turned off at t1, and Q2 is turned on at t2. A zero voltage soft switching transition is accomplished during the dead time t_{db}. During this process, C_{oss} of Q1 is charged from 0V to V_{dc}, and C_{oss} of Q2 is discharged from V_{dc} to 0V. In other words, Q_{oss_0ToVdc} and E_{oss_0ToVdc} are injected to Q1, and Q_{oss_VdcTo0} and E_{oss_VdcTo0} are removed from Q2. Meanwhile, $Q_{oss\_VdcTo0} \times V_{dc}$ are energized to the DC-link since the discharging current of Q2 flows through the DC-link. The process is powered by the inductor current, I_{L1}. The equations (1) and (2) give the relationship between I_{L1} and the charge and energy during the transition. I_{L1_1} is the current at t1, and I_{L1_2} is the current at t2. In (2), average current during the transition is approximated by arithmetic mean, which is smaller than the actual value.

$$E_{oss\_0ToVdc} + \left(Q_{oss\_VdcTo0} \times V_{dc} - E_{oss\_VdcTo0}\right) = 0.5 \times L_1 \times \left(I^2_{L1\_1} - I^2_{L1\_2}\right) \quad (1)$$

$$Q_{oss\_0ToVdc} + Q_{oss\_VdcTo0} = 0.5 \times t_{db} \times \left(I_{L1\_1} + I_{L1\_2}\right) \quad (2)$$

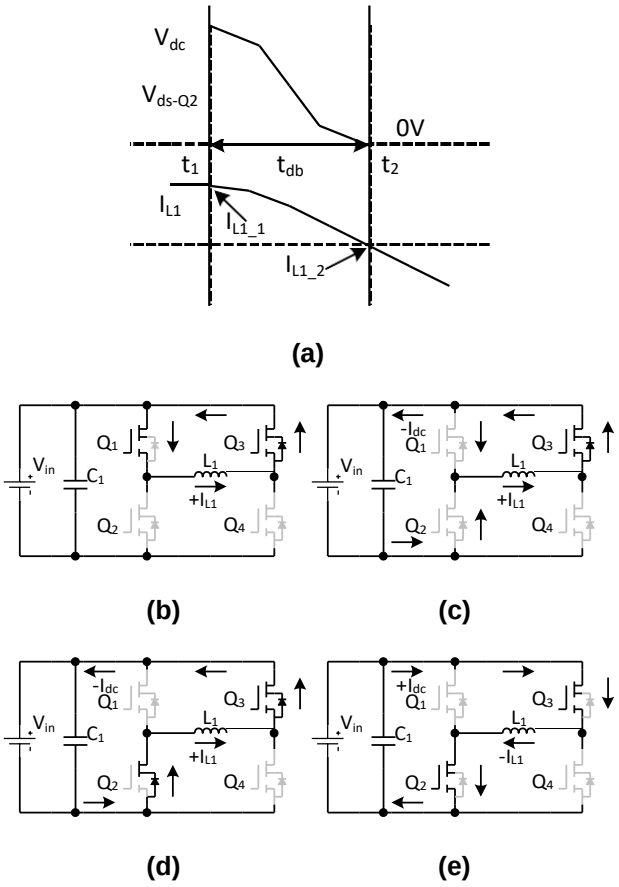


Figure 5. Ideal soft switching waveform and simplified circuit diagram showing current flow (a) waveform, and current flow (b) before t1, (c) after t1, (d) before t2, (e) after t2

If there is no restriction on t_{db}, the minimum I_{L1_1} to maintain soft switching is obtained when I_{L1_2} is 0A. If t_{db} is targeted to a value, such as 87.5ns in this case, the minimum I_{L1_1} can also be derived from the equations. The corresponding values are calculated at 400V DC-link and summarized in Table 4. They define the boundary between soft switching and hard switching. When I_{L1_1} is lower than the boundary values in Table 4, Q1 and Q2 start hard switching. Assuming Q2 is turned on with V_x remaining on its drain, Fig. 6 and Fig. 7 give waveform and simplified circuit diagram for two typical cases of hard switching.

Table 4 Boundary of soft switching

	t_{db} (ns)	I_{L1_1} (A)	I_{L1_2} (A)
TPH3212PS	70	5.2	0
IPP60R090CFD7	128	9.4	0
TPH3212PS	87.5	5.3	-1.2
IPP60R090CFD7	87.5	10.1	3.63

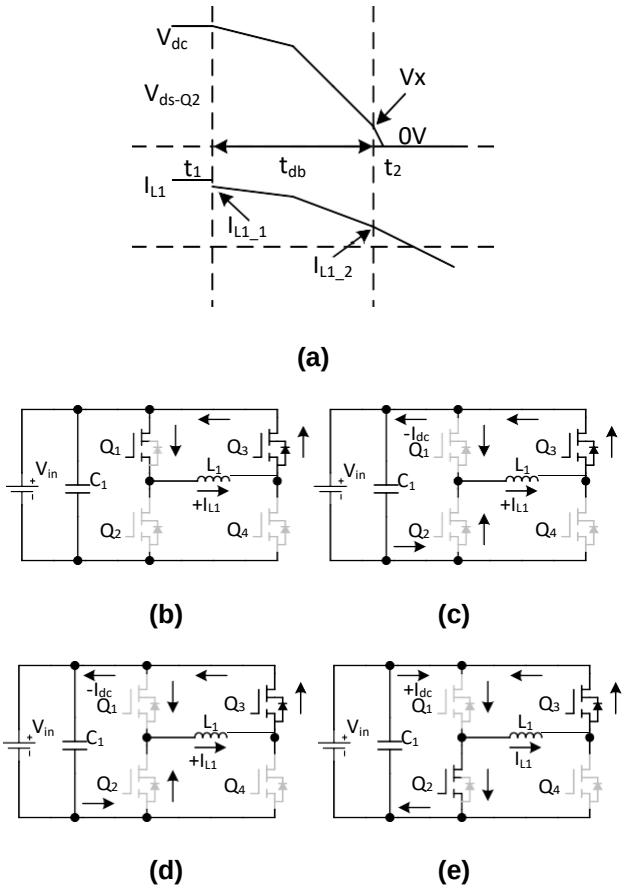


Fig. 6 Ideal soft switching waveform and simplified circuit diagram showing current flow (a) waveform, and current flow (b) before t1, (c) after t1, (d) before t2, (e) after t2

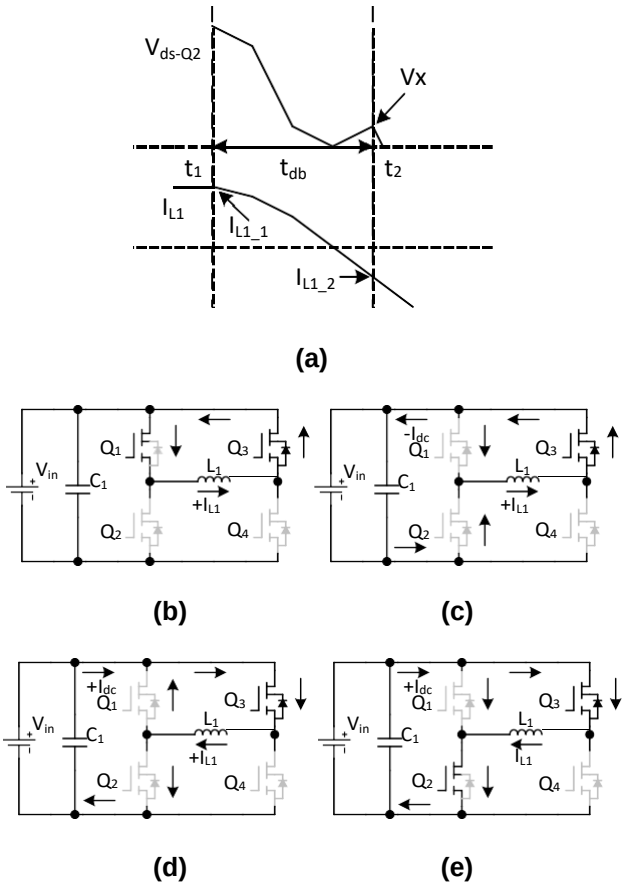


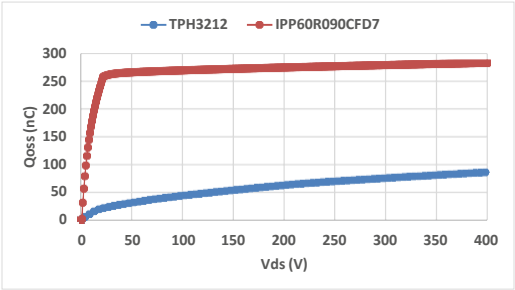
Fig. 7 Ideal soft switching waveform and simplified circuit diagram showing current flow (a) waveform, and current flow (b) before t1, (c) after t1, (d) before t2, (e) after t2

For both cases, before turn-on of Q2, $Q_{oss\_0To(Vdc-Vx),}$ has been charged to Q1, and $Q_{oss\_VdcToVx,}$ has been discharged from Q2. Correspondingly, $E_{oss\_0To(Vdc-Vx)}$ has been stored in Q1, $E_{oss\_VdcToVx}$ has been removed from Q2, and $Q_{oss\_VdcToVx}$ x V_{dc} has been stored in DC-link. In other words, there is $Q_{oss\_(Vdc-Vx)ToVdc}$ going to be charged into Q1 during turn-on of Q2. The charging of $Q_{oss\_(Vdc-Vx)ToVdc}$ in Q1 causes turn-off loss in Q1, $E_{oss\_(Vdc-Vx)ToVdc}$, and one part of turn-on loss in Q2, V_{dc} x $Q_{oss\_(Vdc-Vx)ToVdc}$ - $E_{oss\_(Vdc-Vx)ToVdc}$. The discharging of $Q_{oss\_VxToVdc}$ in Q2 causes another part of turn-on loss in Q2, $E_{oss\_VxToVdc}$. On the other hand, turn-on of Q2 also suffers from losses caused by I_{L1_2}, which is not included in this discussion. For both cases in Fig 6 and Fig. 7, (1) and (2) can be rewritten as (3) and (4) by simply replacing the Q_{oss} and E_{oss} and assigning 87.5ns to dead time, t_{db}. Since Q_{oss} and E_{oss} are

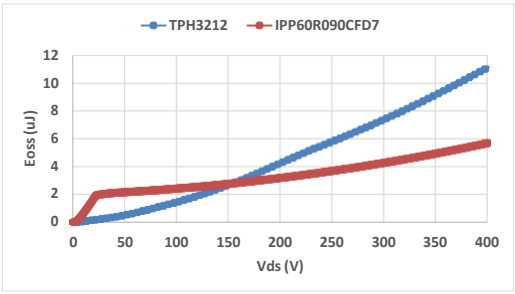
voltage dependent, the following analysis is calculated with the C – V curve instead of $C_{o(tr)}$ or $C_{o(er)}$ defined at fixed voltage. With experimental C - V curve, Q_{oss} vs. V_{ds} and E_{oss} .vs V_{ds} curves of devices are calculated and shown in Fig. 8. With the curves, V_x – I_{L1_1} and I_{L1_2} – I_{L1_1} curves are calculated with (3) and (4) in Fig. 9.

$$E_{oss\_0To(Vdc-Vx)} + \left(Q_{oss\_VdcToVx} \times V_{dc} - E_{oss\_VdcToVx}\right) = 0.5 \times L_1 \times \left(I^2_{L1\_1} - I^2_{L1\_2}\right) \quad (3)$$

$$Q_{oss\_0To(Vdc-Vx)} + Q_{ss\_VdcToVx} = 0.5 \times t_{db} \times \left(I_{L1\_1} + I_{L1\_2}\right) \quad (4)$$

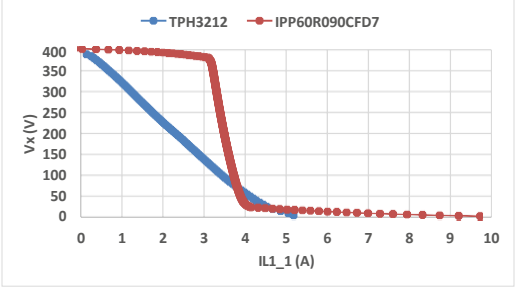


(a)

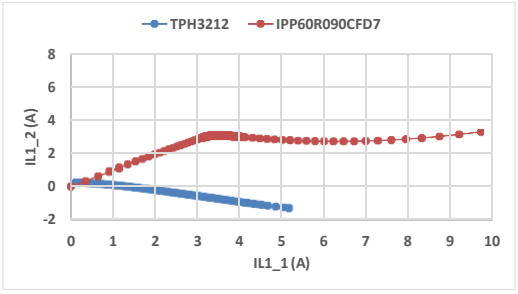


(b)

Fig. 8 (a) Q_{oss} .vs Vds curve, and (b) E_{oss} .vs Vds curve from 0V to 400V



(a)

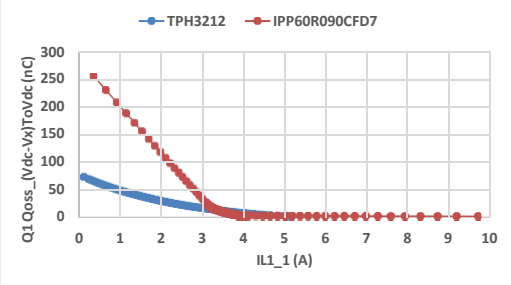


(b)

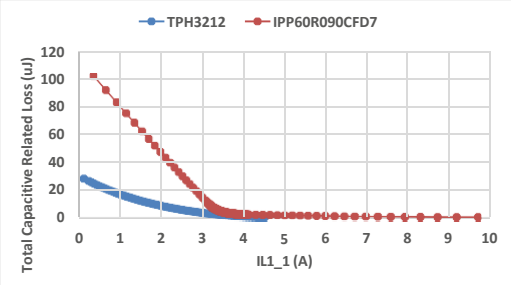
Fig. 9 (a) V_x – I_{L1_1} curve, and (b) I_{L1_2} – I_{L1_1} curve from 0A to 10A

From the V_x – I_{L1_1}, it is worth noting that V_x of both GaN and Si stay below 50V at I_{L1_1} higher than 4A. Once I_{L1_1} becomes less than 4A, V_x of GaN increases gradually whereas that of Si jumps dramatically and becomes steady around 400V. This difference can be explained by the Q_{oss} - V_{ds} curve. The charge of GaN is more uniformly distributed across the whole voltage range while most of the Si charge is located in the low voltage region. From the I_{L1_2} – I_{L1_1}, as can be expected, for GaN, a t_{db} longer than the transition time required by the minimum I_{L1_1} will make V_x slightly pass the valley of Q2 V_{ds} and end up with a negative I_{L1_2}. If fine-tuning of t_{db} can be practically implemented in nanoseconds, V_x would be able to stay right at the valley of Q2 V_{ds}. As for Si, Q2 will be turned on around 3A I_{L1_2} from 10A to 3A I_{L1_1}.

The remaining charge in Q1 and the loss of a phase leg are presented in Fig 10. As discussed above, this loss is stored in Q1, $E_{oss\_(Vdc-Vx)ToVdc}$, and dissipated in Q2, V_{dc} x $Q_{oss\_(Vdc-Vx)ToVdc}$ - $E_{oss\_(Vdc-Vx)ToVdc}$. On the other hand, the remaining energy in Q2, E_{oss_VxTo0}, is dissipated during the transition. The total dissipated energy related to parasitic capacitance is V_{dc} x $Q_{oss\_(Vdc-Vx)ToVdc}$ - $E_{oss\_(Vdc-Vx)ToVdc}$ + E_{oss_VxTo0}. From Fig. 10 (b), it is obvious that GaN significantly reduces the remaining charge and the loss caused by it, especially in light load condition with I_{L1_1} lower than 3A. At 1A I_{L1_1}, the loss caused by remaining charge of GaN is only 25% of that of Si. In other words, GaN cuts 75% of demand on heat dissipation and improves power density by cutting a significant portion of heat sink.



(a)



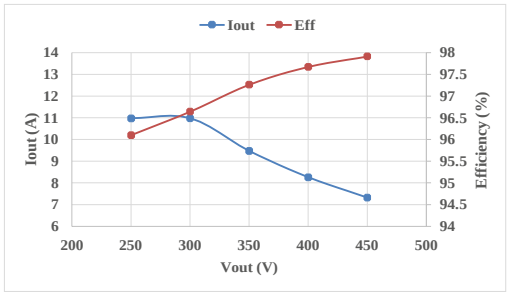
(b)

Fig. 10 (a) remaining charge in Q1, $Q_{oss\_(Vdc-Vx)ToVdc}$, and (b) the loss of a phase leg, V_{dc} x $Q_{oss\_(Vdc-Vx)ToVdc}$ - $E_{oss\_(Vdc-Vx)ToVdc}$ + E_{oss_VxTo0}

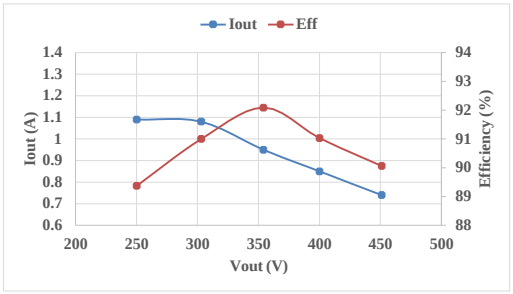
Converter Evaluation

With the active snubber, the PSFB is tested across a battery voltage range from 250V to 450V and performance in difference load conditions are evaluated in this section.

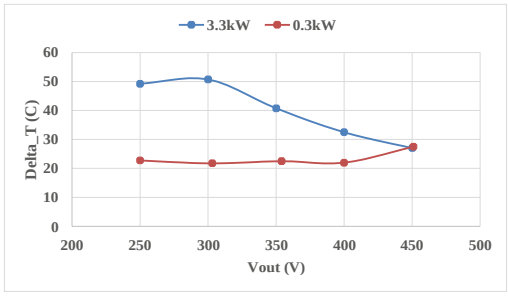
As shown in Fig. 11 (a), efficiency of the PSFB rises with battery voltage or phase shift angle increasing, and it is above 96% over the whole battery voltage range from 250V to 450V. Notably, the arithmetic mean of efficiency is above 97% from 250V to 450V. In Fig. 11 (b), it is found that converter efficiency is still around 90% at only 10% load. Benefiting from extremely low switching loss, the GaN devices generate a minimal amount of heat and cause very low temperature rise during hard switching at 10% load, as shown in Fig. 11 (c).



(a)



(b)



(c)

Figure 11. Efficiency at (a) 3.3kW or 100% load and (b) 0.3kW or 10% load, and (c) device temperature rise at different load conditions.