100 kHz Dual Active Bridge for 3.3kW Bi-directional Battery Charger

Introduction

Dual Active Bridge (DAB) is a classic topology for bi-directional power conversion requiring a wide range of voltage transfer ratio, such as battery chargers. An advantage of this circuit over a CLLC topology is that it does not require either variable switching frequency or a variable DC-link voltage to regulate the battery voltage. However, there is one imperfection in DABs: soft switching is not available in some conditions. Specifically, devices are operated in hard switching when a DAB works at either low power or a strong voltage transfer ratio.

For DABs, Renesas GaN FETs offer the following benefits versus traditional Si devices:

- High switching frequency and high power density
- Low loss during hard switching

These benefits are the result of Renesas GaN attributes including:

- Low Output Charge (Q_{oss})
- Low Reverse Recovery Charge (Q_{rr})
- Low Switching Losses

With GaN, DABs become more competitive than ever. To balance common mode impedance, four identical inductors instead of one inductor are used in the design. Voltage blocking capacitors are added for voltage mode control.

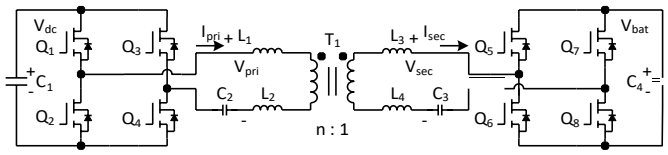


Figure 1. Simplified schematic of the 100 kHz DAB

Converter Design

A prototype of the DAB was designed using the 50mΩ GaN FET (TPH3205WSBQA), shown in Fig. 2. The key specifications of the prototype are summarized below in Table 1.

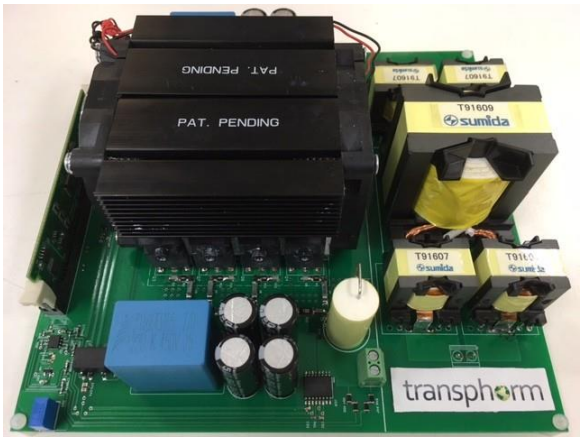


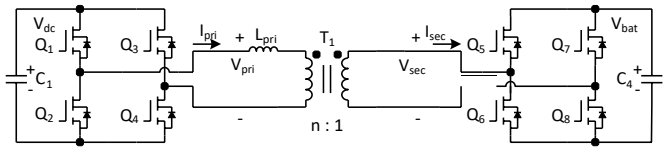
Figure 2. TPH3205WSBQA 100 kHz 3.3kW DAB prototype

Table I Parameters of the DAB

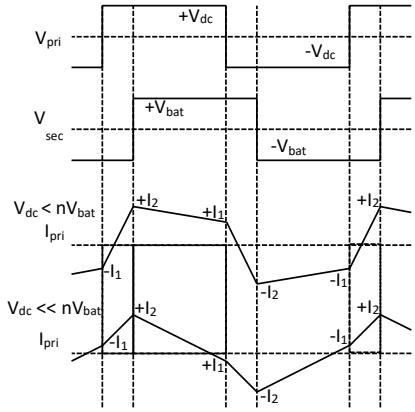
DC-link Voltage (V)	380 ~ 410
Battery Voltage (V)	250 ~ 450
Maximum Power (W)	3300
Maximum Current (A)	11
Q1 – Q8	TPH3205WSBQA
Switching frequency (kHz)	100
Transformer turns ratio	1.125:1
Inductors, L1 – L4 (μH)	6.5
DC blocking capacitor (μF)	5
Max. Phase Shift Angle	0.2π

For a DAB, the power flow is controlled by a phase shift angle between primary and secondary full bridges. In equation 1, n is the turns ratio of transformer, V_{dc} is the dc link voltage, V_{bat} is the battery voltage, f_{sw} is the switching frequency, L_{pri} is the equivalent inductance of L1 to L4 on primary-side, and D is (phase shift angle / π). Usually, D is from -0.5 to +0.5, and power flow is controlled by tuning D. A simplified schematic with typical waveforms are shown in Fig. 3,

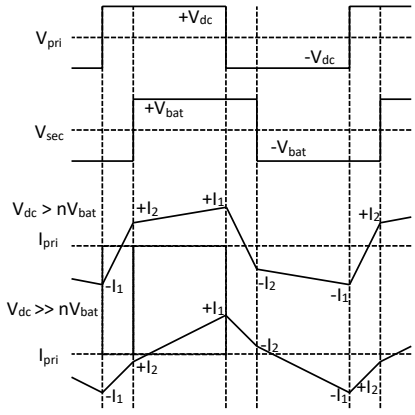
$$P = \frac{nV_{dc}V_{bat}}{*_{+_S}L_{p01}} D(1-D) \quad (1)$$



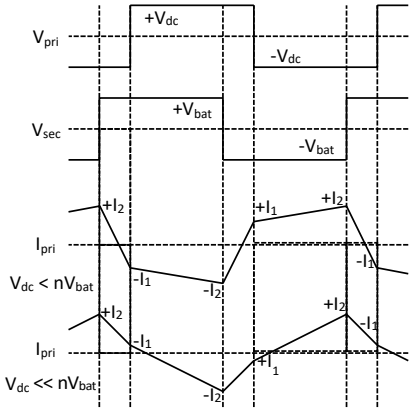
(a)



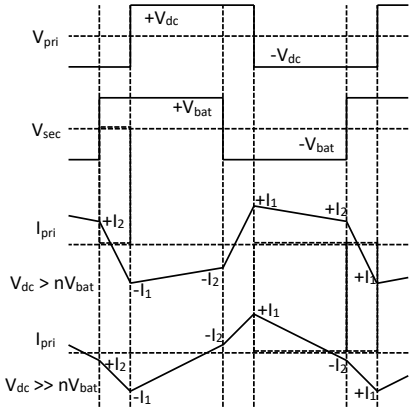
(b)



(c)



(d)



(e)

Figure 3. (a) Simplified schematic, and waveforms for power flow (b) from primary to secondary, $V_{dc} < nV_{bat}$, (c) from primary to secondary, $V_{dc} > nV_{bat}$, (d) from secondary to primary, $V_{dc} < nV_{bat}$, (e) from secondary to primary, $V_{dc} > nV_{bat}$

In the typical waveforms, currents at alternation of voltage polarity are defined as +/- I_1 for V_{pri} and +/- I_2 for V_{sec}, and I_1 and I_2 can be either positive or negative value. A positive value of I_1 or I_2 indicates soft switching or zero voltage switching (ZVS) during the corresponding alternation, whereas a negative value of I_1 or I_2 indicates hard switching. I_1 and I_2 can be calculated by (2) and (3) for both power flowing from primary to secondary and power flowing from secondary to primary.

$$I_8 = \frac{8}{9+_S\text{-}L_{p01}} : V_{dc} + nV_{bat}(2D-1)\mathrm{D} \quad (2)$$

$$I_* = \frac{8}{9+_S\text{-}L_{p01}} (V_{dc}(2D-1) + nV_{bat}) \quad (3)$$

RMS value of I_{pri} can be obtained from (4), and RMS of I_{sec} can be calculated from (5). The primary average current I_{pri_avg} can be obtained from (6) for power flowing from primary to secondary. Correspondingly, the output current I_{sec_avg} can be calculated via (7) for power flowing from primary to secondary. It is found that, with defined currents and voltage in Fig. 3, (2) – (7) are identical for both directions of power flow. As for (6) - (7), the sign of I_{pri_avg} and I_{sec_avg} is positive during power flowing from primary to secondary, and negative during power flowing from secondary to primary.

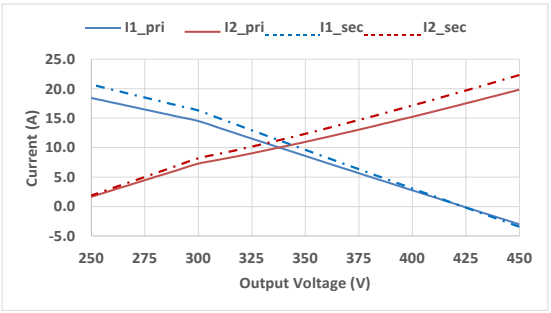
$$I_{pri\_rms} = \mathrm{K}\frac{8}{\mathrm{L}}\overline{(I^*_{\ 8} + I^*_{\ *} + (1-2D)I_8 I_*)} \quad (4)$$

$$I_{sec\_rms} = n\mathrm{K}\frac{8}{\mathrm{L}}\overline{(I^*_{\ 8} + I^*_{\ *} + (1-2D)I_{\ 8}\ I_{\ *})} \quad (5)$$

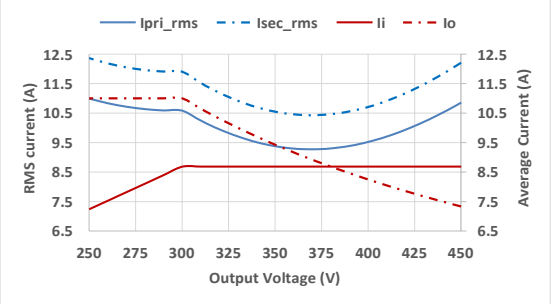
$$I_{\mathrm{NOi\_QRS}} = \frac{8}{*}(I_{\ 8}(1-2D) + I_{\ *}) \quad (6)$$

$$I_{\mathrm{TUV}\_avY} = \frac{8}{*} n{:}I_{\ 8} + I_{\ *}(1-2D)\mathrm{D} \quad (7)$$

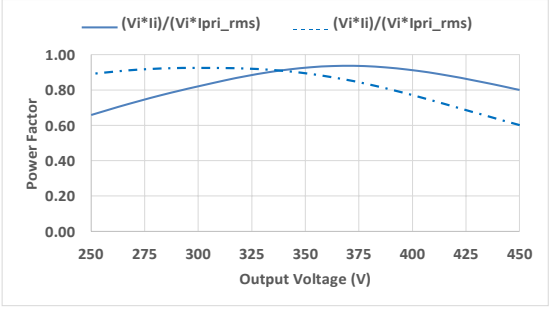
With the parameters in Table I, the currents of the DAB can be obtained via (1) – (7). Fig. 4 summarizes the relationship between the currents and battery voltage at 100% load, 3.3kW. Battery current is clamped at 11A when battery voltage is less than 300V. In Fig. 4 (a), it is found that, I_2 is positive across the whole range, and I_1 is positive except for V_{bat} higher than 425V. In other words, at 100% power, both full bridges are operated in ZVS from 250V to 425V. When V_{bat} is higher than 425V, secondary full bridge maintains ZVS while primary full bridge becomes hard switching with low transition current. The difference between current waveforms at 400V and 450V can be represented by Fig. 3 (b) $V_{dc} < nV_{bat}$ and $V_{dc} << nV_{bat}$ correspondingly. RMS and average currents are plotted in Fig. 4 (b). The difference in RMS currents between primary and secondary is only the turns ratio, n, whereas the difference in average current between primary and secondary is determined by the voltages. With the RMS and average currents, the power factors of both full bridges are plotted in Fig. 4 (c). With battery voltage diverging from the nominal voltage, 338V, the power factors of both sides decrease.



(a)



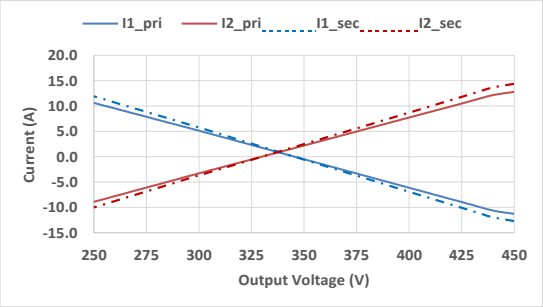
(b)



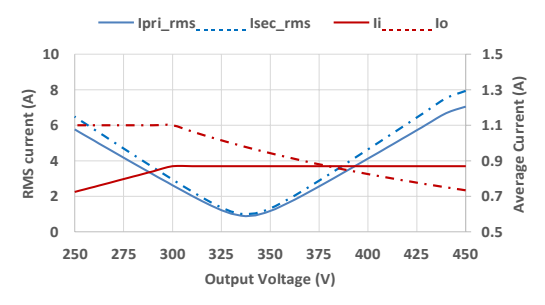
(c)

Figure 4. (a) Currents at voltage alternation, (b) RMS and average current, and (c) power factor of the DAB at 100% power, 3.3kW, with 380V input voltage and from 250V to 450V output voltage

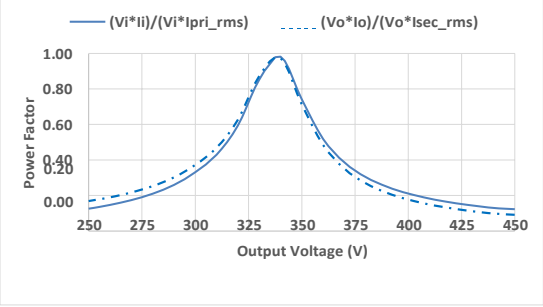
The corresponding plots at 10% power are shown in Fig. 5. In Fig. 5 (a), I_1 is negative when V_{bat} is greater than nominal, 338V, and I_2 is negative when V_{bat} is less than nominal voltage. In other words, primary-side full bridge is always hard switching at $V_{dc} < nV_{bat}$, and secondary-side full bridge is always hard switching at $V_{dc} > nV_{bat}$. In Fig. 5 (b), the RMS currents are higher than the average currents since DC link and battery voltages need to be maintained. Consequently, the power factors of both full bridges decrease rapidly with battery voltage diverging from the nominal voltage, 338V.



(a)



(b)



(c)

Figure 5. (a) Currents at voltage alternation, (b) RMS and average current, and (c) power factor of the DAB at 10% power, 0.33kW, flowing from primary to secondary with 380V input voltage and from 250V to 450V output voltage

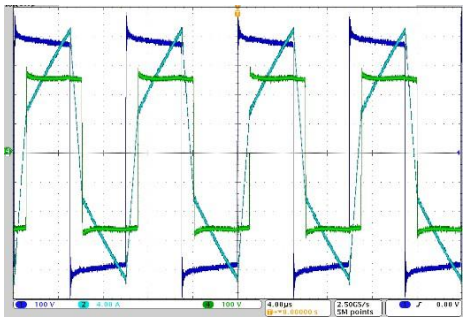
From Fig. 4 and 5, it is found that operation at either voltage diverging from nominal voltage or light load can cause hard switching of one side full bridge. In other words, devices at both full bridges must be able to handle hard switching at 100 kHz. During hard switching at either negative I_1 or I_2, reverse recovery of body diodes happens in the turn off device, which causes losses for both turn-off and turn-on devices in a phase leg. The loss caused by reverse recovery charge and output charge is (Q_{rr} x Vdc) for a phase leg as Q_{oss} is included in Q_{rr} measurement for Renesas's Cascode GaN FET and most Si MOSFETs. On the other hand, for other devices whose datasheet do not include Q_{oss} in Q_{rr}, the switching loss related to charge is Q_{oss} x V_{dc}. To demonstrate the advantage of GaN in DAB, especially at hard switching, Table II gives a comparison between GaN and Si in terms of Q_{oss} and Q_{rr}. GaN reduces more than 70% Q_{oss} and Q_{rr} of Si. As a result, GaN significantly reduces the switching loss of a phase leg. Compared to Si, GaN is able to maintain high efficient conversion when the DAB is operated in hard switching conditions. On the other hand, when similar switching losses are maintained, GaN-based DABs are able to switch at frequencies up to five times the frequency of DABs built with Si. The increment of switching frequency promises power density improvements.

Table II Comparison of GaN and Si

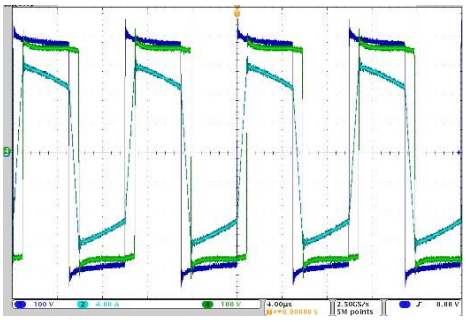
	TPH3205WS WSBQA	IPW60R070 CFD7
V_{ds} (V)	650	600
R_{on} (mΩ) typ	49	57
Q_{oss} (nC) typ	108	396
Q_{rr} (nC) typ	136	570
switching loss of a phase leg (uJ) (without VI loss)	54	228

Converter Evaluation

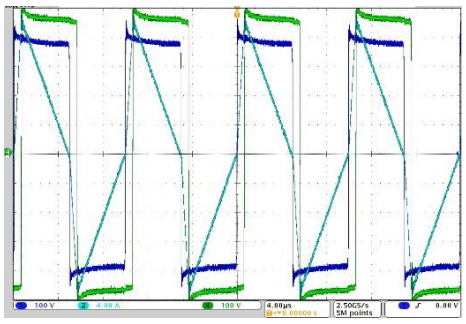
The prototype is evaluated in this section. Fig. 6 gives charging mode, power flowing from primary to secondary, voltage and current waveforms at 3300W, 380Vdc, and various battery voltages from 250V_{bat} to 450V_{bat}. Fig. 7 gives corresponding waveforms in discharging mode. Fig. 8 gives discharging mode waveform at 450V_{bat}, 330W and 3300W. Dark blue is V_{pri}, light blue is I_{pri}, and green is V_{sec}.



(a)

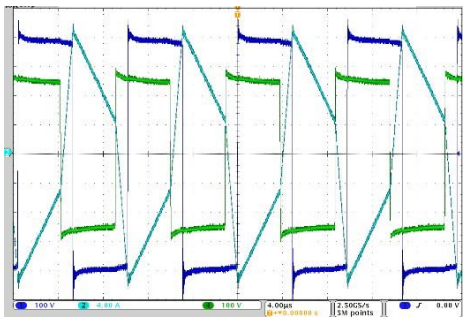


(b)

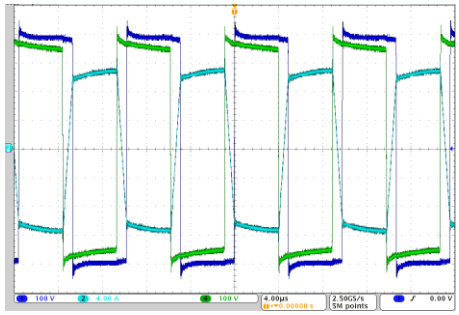


(c)

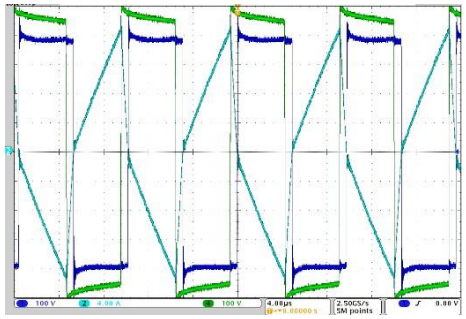
Figure 6. Charging at 3300W, 380V_{dc} and (a) 250V_{bat} (b) 350V_{bat} (c) 450V_{bat}



(a)

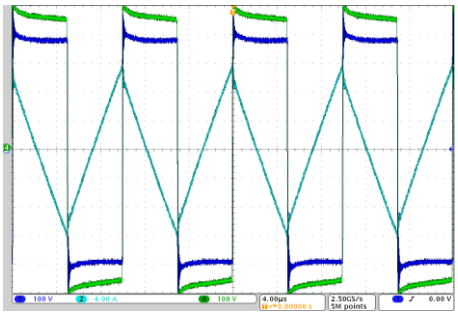


(b)

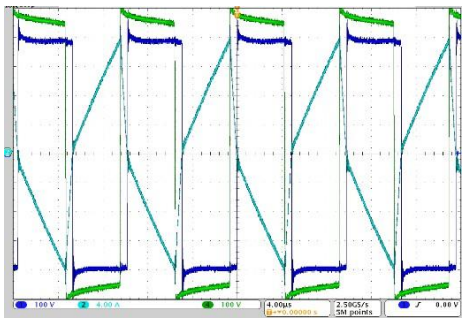


(c)

Figure 7. Discharging at 3300W, 380V_{dc} and (a) 250V_{bat} (b) 350V_{bat} (c) 450V_{bat}



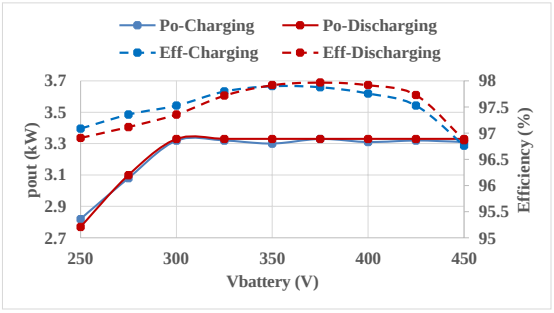
(a)



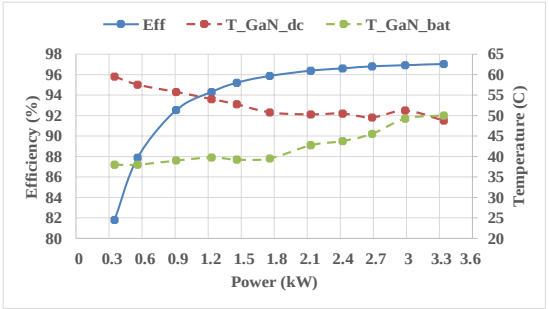
(b)

Figure 8. Discharging at 380V_{dc}, 450V_{bat} (a) 330W and (b) 3300W

Efficiency curves for operation presented in Fig. 6 and Fig. 7 are presented in Fig. 9 (a). Efficiency and temperature curves for operation presented in Fig. 8 are presented in Fig. 9 (b).



(a)



(b)

Figure 9. (a) Efficiency at 3300W, 380V_{dc}, from 250V_{bat} to 450V_{bat}, and (b) efficiency and temperature at 380V_{dc}, 450V_{bat}, from 330W to 3300W

At 3300W, efficiency of the prototype is above 97% from 250V_{bat} to 450V_{bat}, and above 97.5% from 300V_{bat} to 425V_{bat}. Especially, from 350V_{bat} to 400V_{bat}, the efficiency is close to 98%. As can be noted in Fig. 6 (c), 7 (c), and 9 (a) that, at 3300W and 450V_{bat}, the DAB is operated at hard switching. When power decreases, the DAB is operated at more negative current as shown in Fig. 8. From the efficiency and temperature in Fig. 9 (b), as predicted by Fig. 4 (a) and 5 (a), the primary-side full bridge is in hard switching and the secondary-side full bridge is in soft switching. As a result, when power decreases, device temperature of the primary-side bridge increases while device temperature of the secondary-side bridge decrease. The peak temperature rise is less than 40°C when the devices are switched at 100 kHz 12A. In other words, power density can be further improved by shrinking the heatsink's size.