IP Leaflet

USB3.1 Gen1 Peripheral Controller IP Core

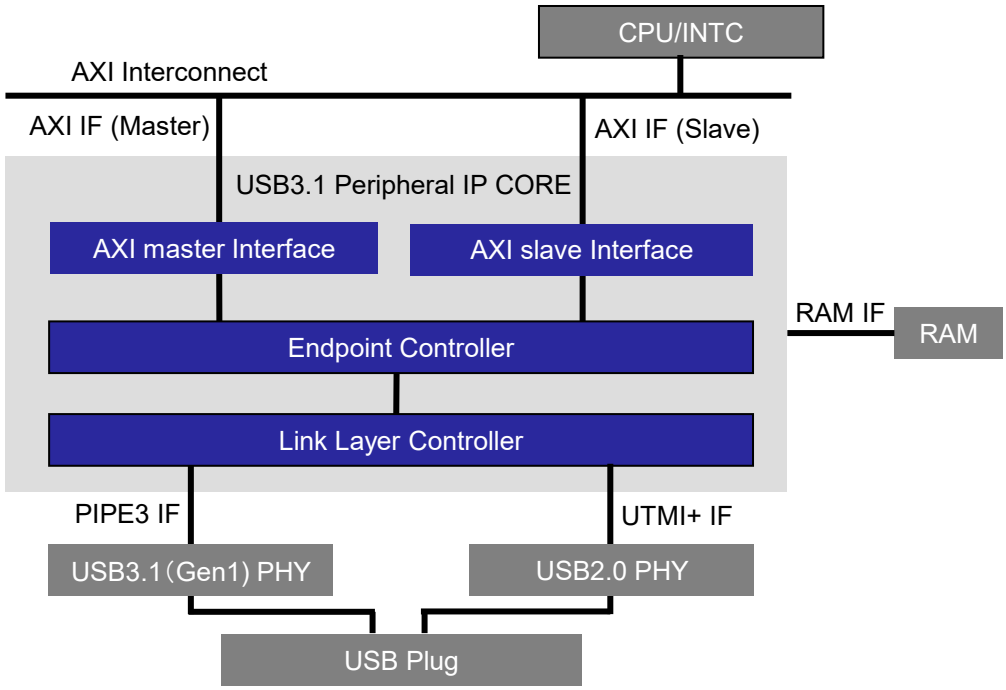
Overview

The Renesas USB3.1 Gen1 Peripheral Controller IP is compliant with the Universal Serial Bus (USB) 3.1 Specification and enables connectivity to USB3.1 system with proven design experiences.
This core contains Endpoint Controller and has AXI bus bridge. This IP supports Super Speed (5 Gbps), High Speed (480 Mbps) and Full Speed (12Mbps).

Key Features

General

- Compliant with Universal Serial Bus 3.1 Specification Revision 1.0
- Compliant with Universal Serial Bus Specification Revision 2.0
- Compliant with PIPE3(PHY Interface for the PCI Express and USB3.0 Super Speed Architectures) Version 3.0
- Compliant with USB2.0 Transceiver Macrocell Interface Plus (UTMI+) Specification Revision 1.0
- Compliant with AMBA® AXI Protocol v1.0 Specification



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USB 3.1 Function

- 5Gbps USB3.1 Super Speed transfer
- Compliant with PIPE3 (PHY Interface for the PCI Express and USB3.0 Super Speed) architecture (32bit@125MHz)
- Maximum of 30 PIPE (PIPE0 not included) can be used (configurable)
- Configurations provided below can be set for each PIPE
    - Endpoint Number: between0 and 15
    - Transfer Type: control (only PIPE0)/bulk/interrupt (*isochronous is not supported)
    - Max Burst Size: fixed to 1 for PIPE0 (control), between 1 and 16 (bulk) and between 1 and 3(interrupt)
- Max Sequence Number: fixed to 31
- Stream ID control supported (UASP can be supported)
- Suspend/Resume function
- Power Management by sending/receiving of link commands is supported
- Remote Wakeup request can be transmitted

AXI Master I/F

- Address Bus width :32 bit
- Data Bus width :64 bit
- Maximum Burst Length :16 burst
- Burst Size :1/2/4/8 byte

AXI Slave I/F

- Address Bus width :32 bit (valid address bus width: 10bit)
- Data Bus width :64 bit
- Maximum Burst length :16 burst
- Burst Size :1/2/4 byte

Product Details

IP Core

The core part of this IP provides EPC(EndPoint Controller) functionality. The IP as a whole has the interfaces as the following.

AXI interface

This IP has AXI Master interface and Slave interface. The master interface is for transaction data handling, and the slave interface is for register interface. The master interface supports 32-bit address, 64-bit data bus width, 16bursts. The slave interface supports 32-bit address, 64-bit data bus width, 16bursts.

PIPE interface supports 32-bit 125MHz PIPE3 interface for Super Speed PHY interface.

UTMI+ interface supports UTMI+ interface for High / Full speed interface.

Related Products

uPD720230,uPD720231A : USB3.0 SATA Bridge