

## 32-bit RISC CPU IP

# SH2-DSP CPU

### Overview

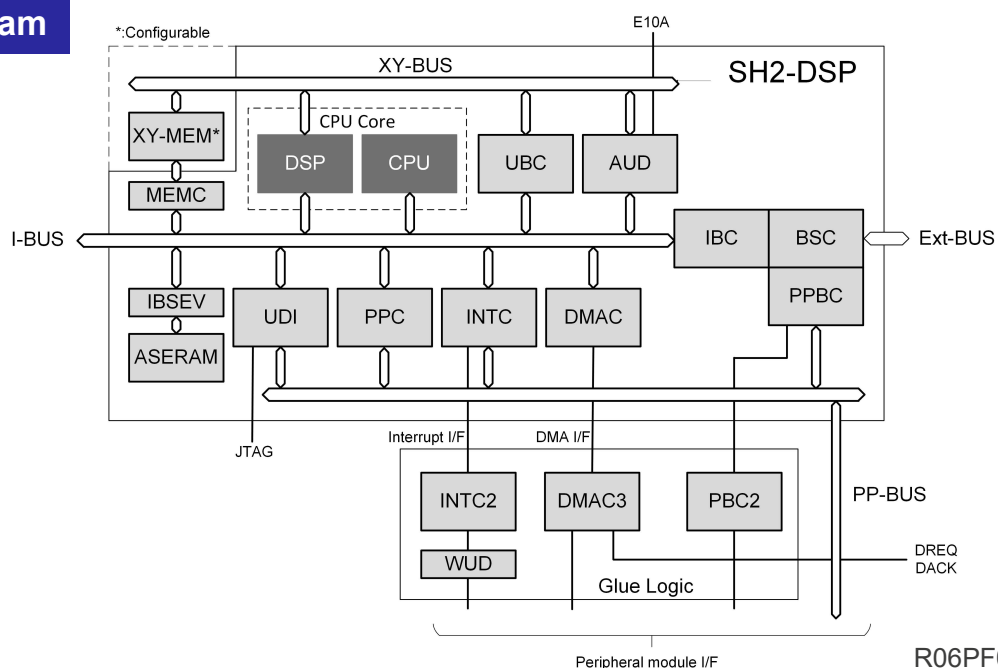
The SH2-DSP CPU interprets and executes the SH-DSP instruction that extended the SH-2 instruction. For multiply instructions and DSP arithmetic instructions, calculations are performed with a digital signal processor (DSP) module.



### Key Features

- Instruction length: 16/32 bits
- Global register: 32 bits x 16,  
Control register: 32 bits x 6,  
System register: 32 bits x 4
- GR for DSP: 40 bits x 2, 32 bits x 6, CR for DSP CR: 32 bits x 1
- Multiply-add calculation specification
  - Internal bus: 32 bits-BUS x 1, 16 bits-BUS x 2
  - Multiply-accumulate instruction:  
Integer: Single precision: 2-3 cycles,  
double precision: 4-6 cycles, Fixed Point: Single precision: 1 cycle
- DSP core: 40 bits ALU, barrel shifter, priority encoder
- Peripheral circuit
  - AUD, UBC, UDI, PPC, INTC, DMAC, IBC, BSC, PPBC

### Block diagram



PMO-25-016  
R06PF0079EJ0101