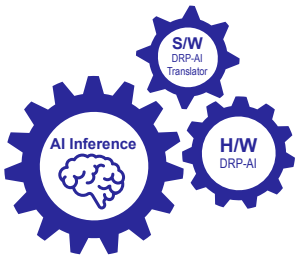
Highly Power-Efficient Embedded AI MPUs for Vision AI

RENESAS RZ/V SERIES

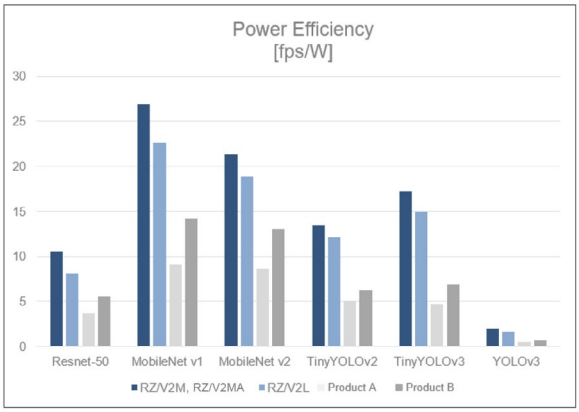
The Renesas RZ/V series of microprocessors (MPUs) for vision AI incorporate Renesas' exclusive DRP-AI AI accelerator delivering excellent AI inference performance and low power consumption.

The RZ/V series consists of three products. The RZ/V2L with 3D graphics engine and highly versatile peripheral functions is suitable for a wide range of applications. The RZ/V2M features a high-performance image signal processor (ISP) with 4K/30fps support. To enable existing systems to easily implement AI function, the RZ/V2MA is embedded with high-speed interfaces such as PCIe and USB3.1. Also, the embedded OpenCV accelerator can increase the speed of existing image processing algorithm in addition to AI.



Features

- The DRP-AI, AI inference hardware, utilizes dynamically reconfigurable technology exclusive to Renesas to deliver design flexibility, fast AI processing, and very high power efficiency.
- Combination of hardware (DRP-AI) and software (DRP-AI translator) results in high power efficiency.
- DRP-AI translator provides the capability to expand to more complex AI models without requiring hardware change.
- Deliver excellent inference performance and power efficiency, irrespective of complexity and size of the AI model (right figure).



Applications

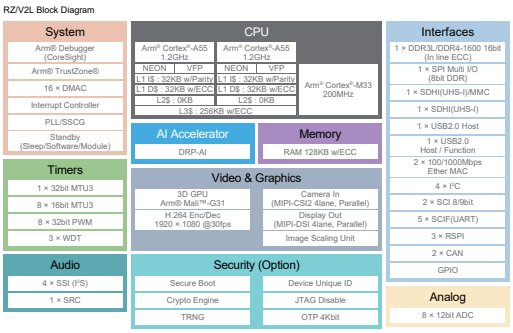
- Security cameras
- POS systems
- Intercom systems
- Smart cameras
- Robot vacuum cleaners
- Smart appliances
- AI gateway
- Entrance/Exit management system
- Infrastructure monitoring
- Retail
- Logistic

Advantages

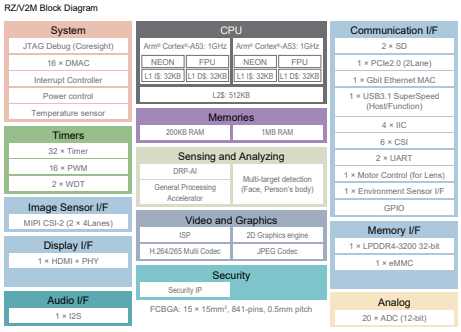
- No heat sink or cooling fan is needed, enabling reduced product size & BOM costs.
- RZ/V2L enables building of a vision AI system using an inexpensive camera module without an external ISP.
- RZ/V2M provides "Tuned ISP" for growing list of sensors to use highest quality images without needing labor intensive ISP parameter tuning.
- High-speed interfaces (PCIe, Gb Ether, USB3.1) enable adding on AI functions in existing system.
- RZ/V2MA provides OpenCV Accelerator (DRP) to accelerate image processing other than AI.

Block Diagram

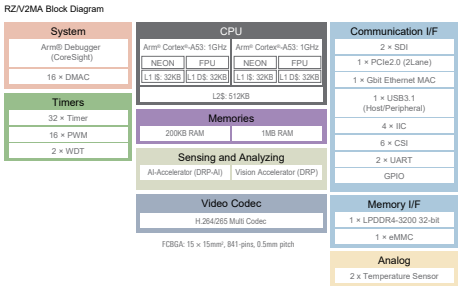
RZ/V2L Block Diagram



RZ/V2M Block Diagram



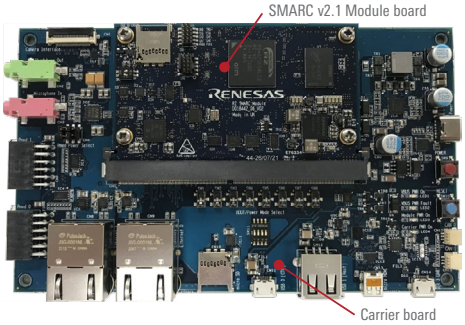
RZ/V2MA Block Diagram



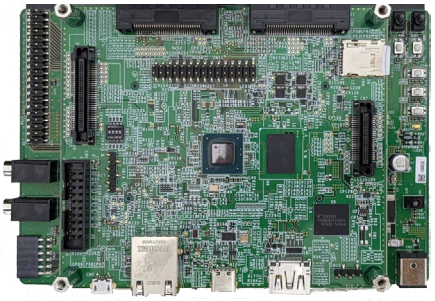
Note: Refer to the hardware manual of the MPU for usage conditions of each function.

Evaluation Board Kit (EVK)

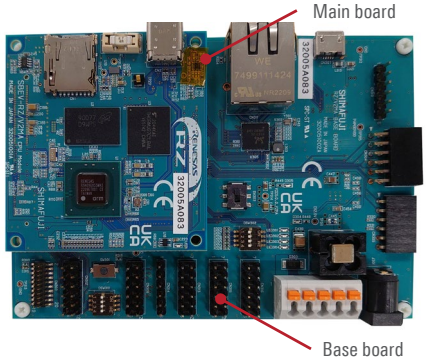
RZ/V2L Evaluation Board Kit (EVK)



RZ/V2M Evaluation Board Kit (EVK)



RZ/V2MA Reference Board (Evaluation Kit)



Note the RZ/V2MA reference solution is provided by Renesas partners.

Ordering Information

Product Group	RZ/V2L		RZ/V2M	RZ/V2MA
Part Number	R9A07G054L24GBG	R9A07G054L23GBG	R9A09G011GBG	R9A09G055MA3GBG
AI accelerator	DRP-AI	DRP-AI	DRP-AI	DRP-AI + Vision Accelerator (DRP + OpenCV library)
ISP function	Simple ISP by DRP Library	Simple ISP by DRP Library	Tuned ISP by H/W	-
Main CPU	Cortex-A55 x2	Cortex-A55 x2	Cortex-A53 x2	Cortex-A53 x2
Sub CPU	Cortex-M33 x1	Cortex-M33 x1	-	-
Graphics	3D (Arm Mali-G31)	3D (Arm Mali-G31)	2D	Video Codec: H.264/265 Multi-codec
Video Codec	H.264	H.264	H.265/H.264 Multi codec	H.264/265 Multi-codec
Display Interface	1x MIPI DSI or 1x Digital Parallel output	1x MIPI DSI or 1x Digital Parallel output	1x MIPI DSI	-
Camera Interface	1x MIPICSI-2 or 1x Digital Parallel input	1x MIPICSI-2 or 1x Digital Parallel input	2x MIPI CSI-2	-
Gigabit Ethernet	2ch	2ch	1ch	1ch
Package	LFBGA	LFBGA	FCBGA	FCBGA
Pin Count	551pin	456pin	841pin	841pin
Package Information	21mm x 21mm, 0.8mm pitch	15mm x 15mm, 0.5mm pitch	15mm x 15mm, 0.5mm pitch	15mm x 15mm, 0.5mm pitch

■ Learn more about the RZ/V series: renesas.com/rzv

■ Learn more about the RZ/V2L Evaluation Kit: https://www.renesas.com/rzv2l-evaluation-kit

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Document No. R01PF0220EJ0200
Date of release: March 2023