Platform for Embedded System in Package

PfESiP EP – 1

An all in one solution putting together high-end MCU, large amount of peripherals and flexibility with low unit price; this is the new concept of Renesas Electronics. The PfESiP-EP1 is a system in package, grouping both a V850E2 MCU and a Gate Array to add additional functionalities to the platform.

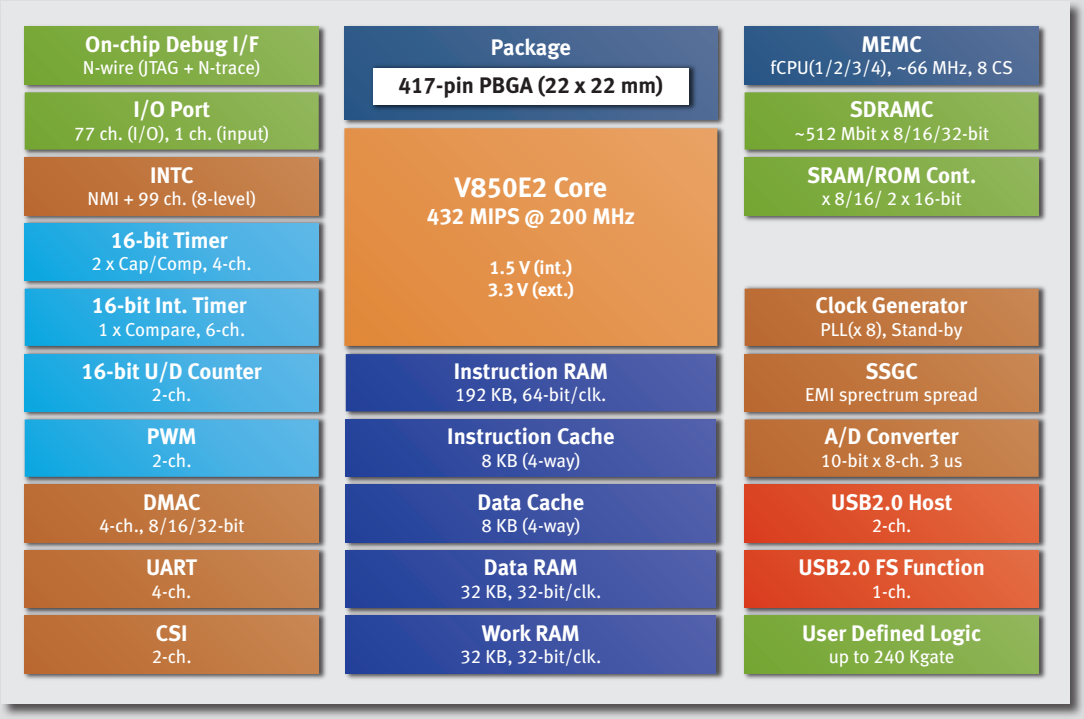
The PfESiP-EP1 is the first born of a new generation of System in Package. It conjugates the high performances of a V850E2S, whose family is the leader in 32-bits CPU, running at 430 MIPS and a gate array to aggregate peripherals to the MCU thus allowing to spare space and costs and to gain efficiency.

An MCU based on the latest technologies to achieve high performances and allowing a high degree of customization in the most efficient way: PfESiP is the product which supplies Renesas Electronics' 32-bit world leader CPU with an unmatched flexibility.

Features

- V850E2 CPU core, max. 430 MIPS in operation
- CPU in 150 nm technology (CB-12)
- 1.5 V core voltage
- Low power consumption MCU: 1 W
- USB2.0 FS (host x2, device x1)
- On board memory controller, UARTs, ADC
- 16/32-bits selectable external bus
- Large instruction RAM 192 KB
- Up to 240 K usable gates
- 0.35 um embedded UDL (EA9HD)
- Large choice of packages (from 417 to 572 PBGA)
- I/O voltage options: 1.8 V, 2.5 V, 3.3 V
- Low EMI noise

Block Diagram – 32-bit External Bus Type



PfESiP – EP1	V850E2	User Defined Logic (Default)
Technology	150 nm	0.35 µm
Size		up to 240 K gates***
Performance	400 MIPS	up to 100 MHz system frequency
External bus	16/32-bit	
Core VDD	1.5 ± 0.1 V	3.3 V
Power consumption	1 W*	0.048 µW/MHz/gate**
I/O level	1.8 V, 2.5 V, 3.3 V	
Package	417 PBGA, 464 PBGA, 550 PBGA, 572 PBGA	

* MCU in normal conditions ** 0.1 operation rate *** Utilization rate 60%

Features

Technology (architecture). The EP1 offers a V850E2S-based MCU providing high real-time performance at a very low power consumption. The 150 nm technology used for the MCU allows high integration rate, performance and low power consumption. Associated to the V850E2 architecture build around a main pipeline, it allows the system to work at 200 MHz for more than 400 MIPS.

High integration. In addition to the V850E2S, the PfESiP – EP1 embeds various functions: Memory controller, DMAC, UART, USB host and function, ADC. For more flexibility and integration, EP1 also includes a gate array. This part going up to 240 K gates can be used to integrate additional features such as Ethernet MAC, I²C, or more simply some glue logic needed.

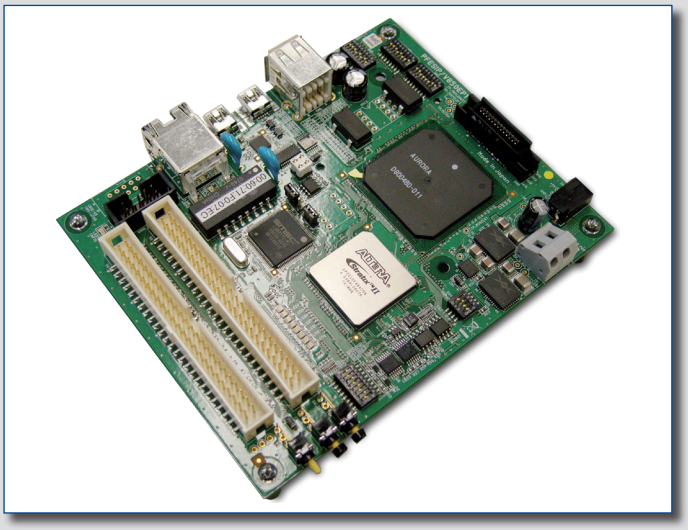
Thus the EP1 is completely adaptable to every application's needs. Result of this strategy for the final product is higher integration rate, smaller boards and lower unit cost in comparison to standards products.

Low power consumption and low noise. Renesas Electronics' 150 nm technology allows mixing optimum transistors in order to reach targeted performance while lowering the maximum power consumption. Thanks to this technology and an optimized design, power consumption of the embedded V850E2S has been cut down to 1 W. To provide low noise performance the 0.35 µm Renesas Electronics' technology (EA9HD) has been chosen for the User Defined Logic.

Easy development. Versatile development boards embedding FPGA and peripherals (USB connector, Ethernet, RAM, ROM) allow a very simple and fast development phase. Once the FPGA is developed, Renesas Electronics will take care of the transfer into the PfESiP's UDL.

A large collection of pre-developed IPs is available in Renesas Electronics' libraries, allowing thus easy integration in the UDL and its fast development.

In addition complete support is provided by Renesas Electronics in a local fashion for both hardware and software development.



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