LOW-POWER MULTI-PORT PRODUCTS

ELIMINATE INTER-PROCESSOR COMMUNICATION BOTTLENECKS IN HIGH-END HANDSETS WITH LOW-POWER MULTI-PORTS

Devices in the IDT® family of low-power multi-ports are the first in the industry designed specifically to address the needs of high-end multimedia handset applications. These high-speed, power-efficient solutions for inter-processor communication are ideal for interfacing up to three DSPs, MPUs, NPUs, ASICs and/or FPGAs.

The flexible, cost-effective multi-ports deliver access times as fast as 55 ns and data rates of 800 Mbps per port to clear out internal data flow bottlenecks. They provide maximum functionality while taking up minimum board space, with packages as small as 6mm x 6mm.

The IDT multi-ports have a 1.8V core voltage; and are available in configurations up to 32K x 16, and synchronous and asynchronous operation. They reduce operating and standby currents by up to 95 percent compared to traditional dual-ports. Operating current is only 15 mA (typ.) and standby current is just 2 µA (typ.) to help extend talk and standby times.

The architecture of IDT low-power multi-ports enables modular, reusable handset designs that can quickly be optimized to address different market requirements. The devices use a standard SRAM interface and support multiple voltage configurations, so existing application or baseband subsystems can be mixed and matched with minimal design effort, saving development time. These features help maximize the returns on system engineering investments, while also significantly shortening new-product design cycles.

The IDT Mobile Multimedia Interconnect™ M^2I is fully optimized for multimedia applications in high-end mobile handsets and personal digital assistant devices. It uses a synchronous architecture that yields cycle times approximately 3x faster than asynchronous dual-port RAMs, and together with an internal counter, enables a data burst mode that eliminates the 50% inefficiency caused by the address-data-address-data scheme used in asynchronous address-data multiplex (ADM) interconnects. The net result is a 6x bandwidth improvement over asynchronous ADM devices. The interconnect has also been power-optimized, drawing 40% less operating current than the asynchronous dual-port RAM approach. The combination of fewer and faster clock cycles with the significantly lower operating current results in a 90% lower battery drain, independent of the type or size of the data being transferred.

Moreover, the M^{2}I ADM interface consumes approximately 50% fewer pins than non-multiplexed solutions. It also liberates GPIO pins on the processors by deploying 8 dynamically programmable GPIO extender pins. These pins allow the interconnect to assume monitor and control responsibilities that would otherwise be undertaken by the processors, enabling the processor to be used for even more value added functions. In total, the mobile multimedia interconnect liberates more than 20 pins on the processors that can then be used to implement differentiating functionality.

Finally, the ADM interface on the new M^{2}I maintains the modular nature of the dual-processor architectures, making it a popular interface standard supported by handset processor manufacturers. The new device also supports the traditional non-multiplexed interface, enabling it to interface with both current and legacy processors. This affords designers the freedom to mix and match both processors and processor manufacturers to meet a broad range of requirements.

Features	Dual Ports	Tri-Ports	Benefits
1.8V core voltage	✓	✓	Significantly reduces power consumption
ADM (address/data multiplexed interface)	✓		Allows interface to TI and other vendor processors, while reducing pin count and trace routing
Tri-port architecture—Bi-directional access to the memory from all three ports		✓	Enables high-speed communication between an application processor and dual broadband processors
Organizations			Accommodates capacity requirements of high-end handsets
• 4K x 16/18	✓		
• 8K x 16/18	✓	✓	
• 16K x 16	✓		
• 32K x 16	✓		
Low operating and standby currents			Increases both talk and standby time in handset applications
• 15 mA (typ.) operating current	✓		
• 2 µA (typ.) standby current	✓		
• 30 mA (typ.) operating current		✓	
• 4 µA (typ.) standby current		✓	
Access times as fast as 55 ns (Data rates up to 800 Mbps per port)	✓	✓	Supports unmatched bandwidth for high-speed inter-processor communication; helps eliminate communication bottlenecks
Standard SRAM interface	✓	✓	Provides ease of use and enables flexible and reusable designs
Programmable special function pins	✓		Enable flexibility by freeing-up GPIO pins on the processors. This programmability allows better design optimization
Interrupt functionality	✓	✓	Facilitates inter-processor communication; allows ping-pong memory accesses
Simultaneous access to the memory from each port	✓	✓	Doubles the bandwidth that multiplexed SRAM solutions provide
Multiple voltage configurations	✓	✓	Reduces the need for external logic; enables simpler, highly modular and reusable designs
Common pinouts and footprints	✓	✓	Enhances design flexibility
Input Read and Output Drive registers	✓		Allows up to 5 external binary devices to be controlled/monitored through the dual-port memory interface; processor I/O ports can be used for other tasks
Small packages			Saves board-space in tightly packaged handsets
• 6mm x 6mm x 1mm, 0.5mm-pitch fpBGA	✓		
• 7mm x 7mm x 1mm, 0.5mm-pitch fpBGA		✓	

Part Number	Organization (Density x Bus Width)	Technical Specs (Voltage)	Package Type	Description
70P247/248	4K x 16	1.8V core, 1.8V and 3.3/3.0/2.5V I/O	100-ball fpBGA[1] (CVBGA[2])	Asynchronous Dual-Port RAM
70P257/258	8K x 16	1.8V core, 1.8V and 3.3/3.0/2.5V I/O	100-ball fpBGA[1] (CVBGA[2])	Asynchronous Dual-Port RAM
70P9268	16K x 16	1.8V core and I/O	100-ball fpBGA[1] (CVBGA[2])	Mobile Multimedia Interconnect (M2I) (Synchronous)
70P27	32K x 16	1.8V core and I/O	144-ball fpBGA[1] (CABGA[3]), TQFP[4]	Asynchronous Dual-Port RAM
70P5258M/525M	8K x 16	1.8V core, 1.8V and 3.3/ I/O	144-ball fpBGA[1] (CABGA[3]), TQFP[4]	TriPort Multi-Port RAM (Asynchronous)

[1] fpBGA: Fine Pitch Ball Grid Array
[2] CVBGA: Chip Array Very Thin Ball Grid Array
[3] CABGA: Chip Array Ball Grid Array
[4] TQFP: Thin Quad Flat Package

Applications

Multimedia Smartphone

To address the ever-increasing processing requirements of high-end, multimedia handsets, many manufacturers adopt dual-processor architectures. This approach provides the necessary computing performance, yet it also mandates a high-speed communication link between the two processors. Without IDT multiport devices the UART, USB and I^2C interfaces built into the application and baseband processors can't transfer data fast enough to keep pace with today's 3G and 3.5G wireless standards and the applications that high-end phones run.

IDT low-power multi-port products address this problem directly. They deliver the requisite high data rates—unmatched throughput performance—combined with very low power consumption and space-saving packaging. Beyond that, they offer advanced functions that help reduce the complexity and increase the modularity of wireless handset designs. See Figure 1.

Visit www.IDT.com/go/multiport for more information.

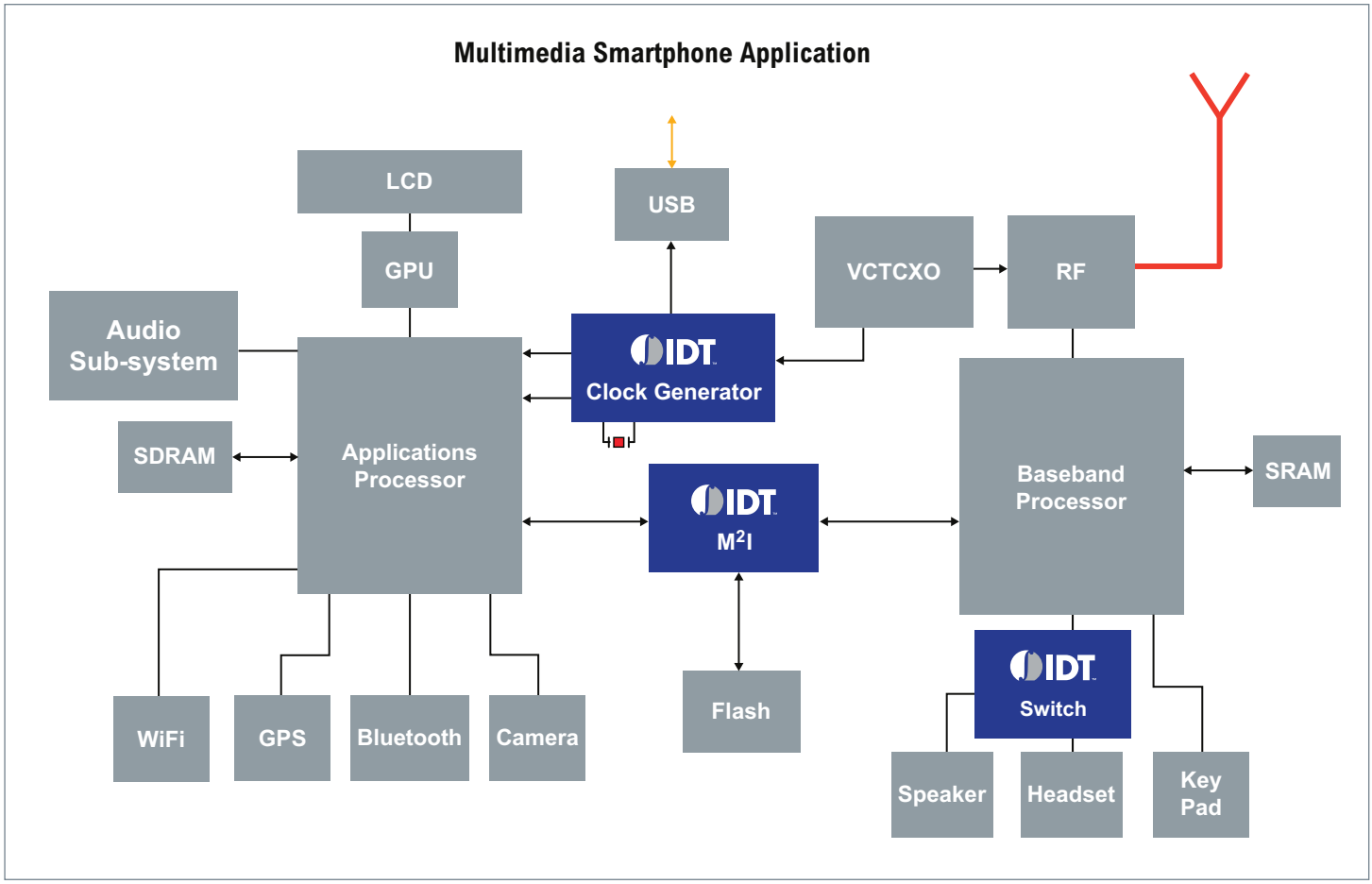

Figure 1. The IDT low-power Mobile Multimedia Interconnect M²I devices are ideal for multimedia smartphones, offering 16K x 16 configuration and achieving per-port data rates as high as 800 Mbps.

Innovate with IDT and accelerate your interprocessor communications.

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