RENESAS
BIG IDEAS FOR EVERY SPACE

RENESAS RZ

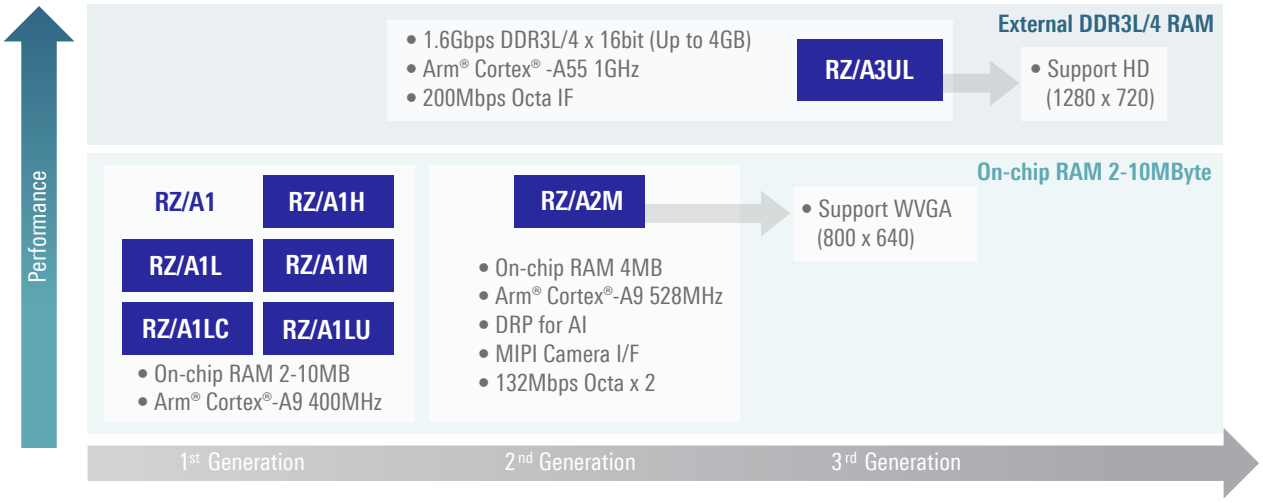
RTOS-Based MPU

Introduction to Renesas RZ/A Series

The RZ/A series is an RTOS-based microprocessor (MPU) combining excellent real-time performance and fast boot time based on Renesas' proprietary technology and Arm® ecosystem, and is as user-friendly as Renesas MCUs.

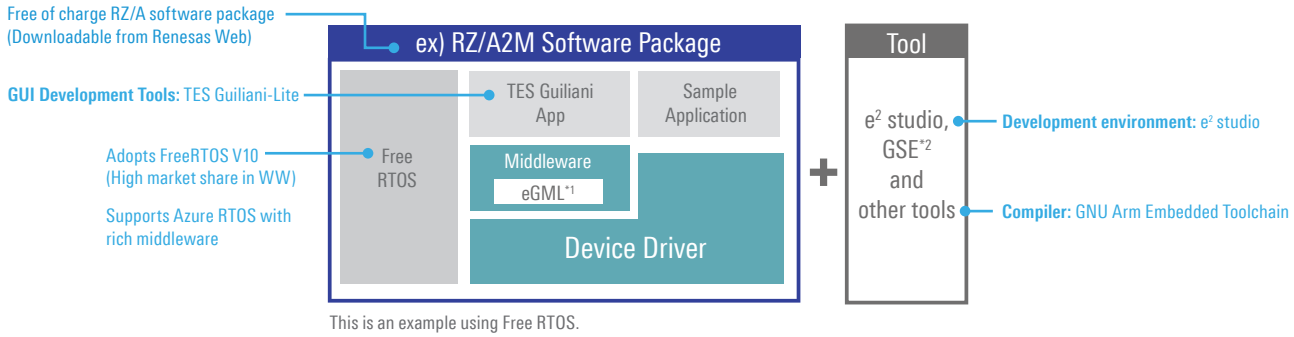
The high-speed performance of RZ/A MPU can quickly process graphics and high-load applications in the third generation RZ/A3UL group MPU. RZ/A2M is embedded with Dynamically Reconfigurable Processor (DRP) technology enabling real-time video image pre-processing at the endpoint, for embedded AI applications. RZ/A1 group offers up to 10 MB of on-chip SRAM, which can buffer up-to WXGA resolution graphics without the need for external SDRAM.

RZ/A Series Product Positioning



Benefits of RZ/A Series - Develop like MCUs

RZ/A series MPUs retain the ease-of-use of Renesas MCUs due to rich integrated development environments, and deliver higher performance than MCUs.



This is an example using Free RTOS.
*1 embedded Graphics Multiplatform Library
*2 Guiliani Streaming Editor

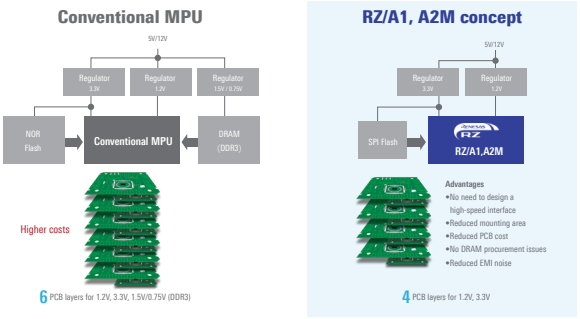
RENESAS RZ/A SERIES

Benefits of RZ/A3UL

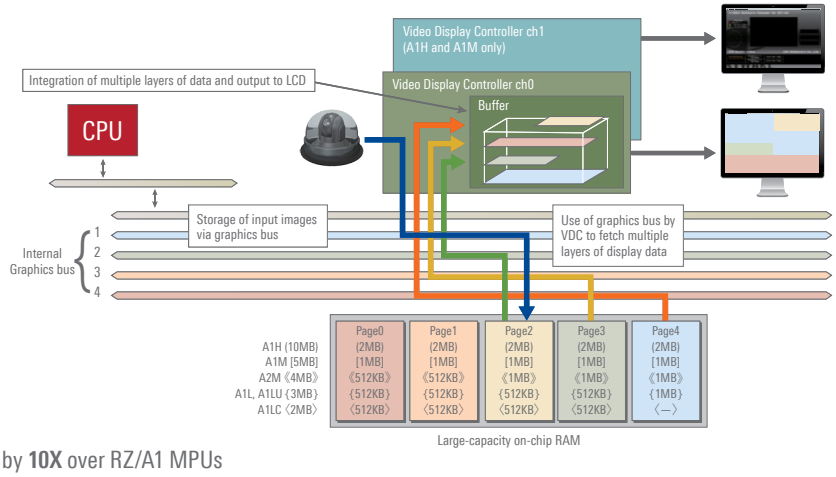
- 64bit CPU@1GHz RTOS MPU
- Choice of two memory I/Fs for different applications
  - Octal-SPI Flash/Octal-SPI RAM: For simple and low cost PCB design
  - DDR3L/DDR4: For high resolution HMI and camera use cases
- Pin-compatible RZ/A3UL (RTOS) and RZ/G2UL (Linux) for easy migration
  - The 361-pin package is pin-compatible between RZ/A3UL and RZ/G2UL

Benefits of RZ/A1 Group, and RZ/A2M MPUs

- Eliminate the need to design a high-speed interface
- Reduced mounting area
- Reduced PCB cost
- No DRAM procurement issues
- Reduced EMI noise



- Include on-chip graphics display and camera input capabilities



- RZ/A2M MPUs with DRP improve image processing performance by **10X** over RZ/A1 MPUs
  - Dynamically Reconfigurable Processor (DRP) technology accelerates image processing
  - Enables hybrid e-AI solutions with DRP for image processing + CPU for inference

Product Information

	RZ/A1H, RZ/A1M	RZ/A1LU	RZ/A1L	RZ/A1LC	RZ/A2M	RZ/A3UL
CPU/Frequency	Cortex-A9/400MHz				Cortex-A9/528MHz	Cortex-A55/1.0GHz
On-Chip RAM	5MB / 10MB	3MB		2MB	4MB	128KB (w/ ECC)
Supported Flash ROM	NOR, Serial (DDR*1), NAND	NOR, Serial (DDR)	NOR, Serial (SDR)		NOR, Serial (DDR), NAND, HyperFlash, OctaFlash	Serial (DDR), OctaFlash
RAM Interface	SDRAM				SDRAM, HyperRAM, OctaRAM	DDR3L/DDR4, OctaRAM
Graphics Engine	2D (OpenVG)	Unavailable			2D, Sprite Engine	Unavailable
LCD Controller	VDC5 (2ch)	VDC5 (1ch)			VDC6 (1ch)	LCDC (1ch)
Camera Interface	Digital (Parallel)Analog	Digital (Parallel)			Digital (Parallel/Serial: MIPI)	Digital (Serial: MIPI)
JPEG Codec Unit	Available		Unavailable		Available	Unavailable
Connectivity	2 x USB2.0(FS/HS) 2 x SDHI 1 x 10/100base Ethernet				2 x USB2.0 (FS/HS/OTG) 2 x SDHI (UHS-I) 2 x 10/100base Ethernet*2	1 x USB2.0 Host 1 x USB2.0 (Host/Function) 2x SDHI (UHS-I) 2 x 10/100/1000 Ethernet*2
Package	256QFP, 324BGA, 256BGA*3	176QFP, 208QFP, 233BGA, 176BGA*3	176QFP, 208QFP, 176BGA*3	176BGA*3	324BGA*3, 272BGA*3, 256BGA*3, 176BGA*3	361PBGA*3

*1 Frequency limitations apply
*2 2ch can be used simultaneously
*3 For industrial/consumer use

For more information, visit www.renesas.com/rza

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