8-bit CPU IP

H8/300 CPU

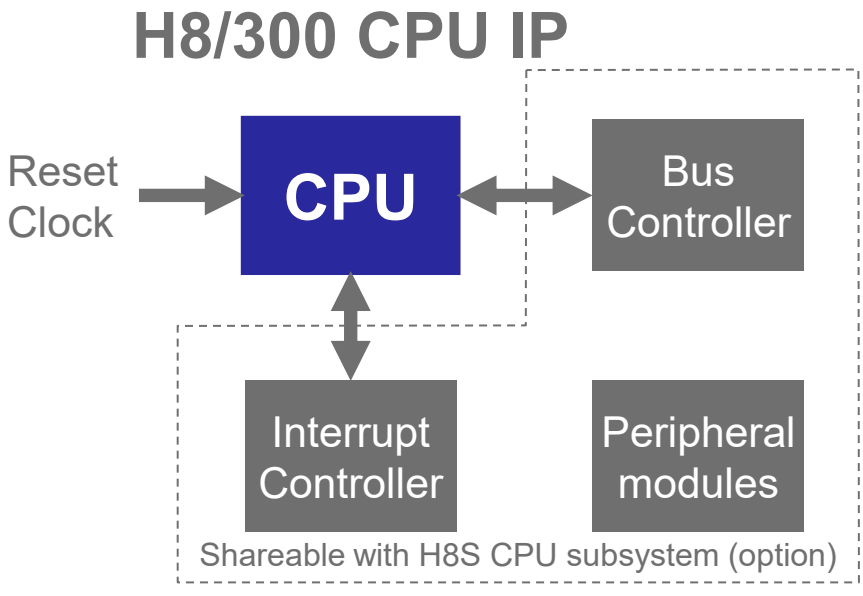
Overview

H8/300 is a high speed 8-bit CPU with an internal 16-bit architecture.
H8/300 CPU IP is compatible with H8S CPU subsystem IP (H8S C200) on system, bus and interrupt interface. So, it can be used in place of H8S CPU with other peripheral modules of optional information packages. It can optimize CPU subsystem gate size for small systems.
Its instruction set is compatible H8/300 and H8/300L series microcontroller products.

Key Features

- Small gate size
- Common interface with H8S CPU subsystem IP
  - system (reset and clock) interface
  - bus interface
  - interrupt interface
- Sharable peripheral modules (option) with H8S CPU subsystem
  - 16-bit free-running timer (FRT)
  - 8-bit timer
  - 14-bit PWM timer
  - 8-bit PWM timer
  - Watchdog timer (WDT)
  - Serial communication interface
- RTL design using Verilog
- Applicable to various processes and FPGAs

Block Diagram



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