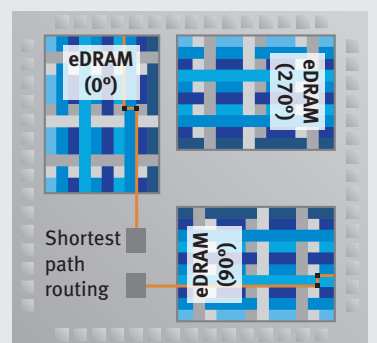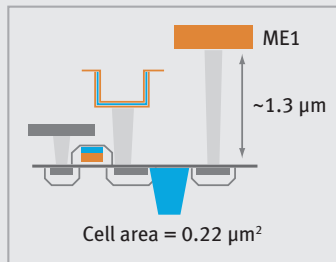# 90 nm SoC Technology

CB-90 ASIC Design Platform

The CB-90 ASIC design platform is based on Renesas Electronics' UX6 process technology. It is designed for a wide range of low-power, high-performance applications, such as broadband communications equipment, high-end computing and storage systems and mobile computing devices.

Renesas Electronics' eDRAM MIM2 process gives the CB-90 a competitive advantage by significantly reducing cell size and improving performance. The technology also facilitates system design by allowing orientation-free cells and signal routes that permit active wires to run over eDRAM macros for optimized integration and performance.

eDRAM Solution

COB
MIM2 capacitor
Dielectric: ZrO_2
Cell size: 0.22 µm²
Cs = 16 fF
Salicided high-Ion cell Tr.
Stacked contact
CMOS compatible

ME1
~1.3 µm
Cell area = 0.22 µm²

eDRAM (0°)
eDRAM (270°)
eDRAM (90°)
Shortest path routing

Product Outline

	CB-90
Node length (Lnode)	90 nm (60 nm gate length)
Metal Layer	Up to 9
Gate count (raw)	100 Mgates
Gate density (raw)	426 kgates/mm²
Core VDD	1.0 ± 0.1 V
Power consumption	0.51 nW/MHz/gate*
System frequency	500 MHz
I/O level	1.8, 2.5, 3.3 V
IO PAD number	960 (for wire bonding package, VDD/GND include)
Package and PAD type	35 µm staggered cup, 55 µm straight cup for QFP, PBGA and FPBGA, 140 to 160 µm staggered bump for FCBGA

* Operation rate: 0.1

CB-90 ASIC Design Platform

Features

- 90 nm technology
- Up to 9 metal layers
- Very high speed
- Gate count up to 100 million gates
- 1.0 V core voltage

- Power consumption down to 0.51 nW/MHz/gate
- I/O voltage options: 1.8 V, 2.5 V, 3.3 V
- Flexible I/O structure supports USB, HDMI, S-ATA, PCI
- Package types : PBGA, FPBGA, FCBGA, QFP

Architecture

For optimal designs, the CB-90 offers two different masters, low (L) and normal (M) consumption. The technology also provides a choice between three different transistor types to enable optimal allocation of performance/low power/high integration areas on the same chip.

High integration

Renesas Electronics' UX6 process used for the CB-90 family achieves high integration with support for up to 100 million usable gates. Up to nine levels of all-copper wiring (minimum wiring pitch 0.28 µm) in the CB-90 libraries permit increased density and higher reliability. The use of low-resistance copper means wiring layers can be thinner. Reduced wire capacitance contributes to higher speed and lower power consumption.

High clock speeds are possible because of 1-V, high-speed CMOS transistors that realize ultra-low power using a gate length of 60 nm, aluminium wiring, PAD-AL and low-k (k = 2.9) intermetal dielectrics.

Low power consumption

The optimal transistor mix, in line with target circuit performance, lowers power consumption by approximately 40% compared with previous chip generations. The use of low-power techniques, including a multi-power-supply design flow and automatic voltage control technology, further reduces power consumption.

The combination of low-standby leakage, high-density cell libraries and unique low-power design techniques allows Renesas Electronics to realize sophisticated power management in its system LSI devices.

I/Ps

CPU cores like the standard ARM processor plus peripherals can be obtained from our product IP portfolio. Application-specific cores for networking (Ethernet), consumer (HDMI), and PC (USB, PCI express, S-ATA) help to build genuine SoC designs. Analog cores like PLLs, ADCs and DACs complete this wide range of macros.

Interfacing

The CB90 I/O structure provides broad interfacing support thanks to I/O voltages of 1.8, 2.5 and 3.3 V. Ready-to-use USB, S-ATA, HDMI, PCI express standards give access to the latest high-speed interface versions. Different package options, such as PBGA, FPBGA and FCBGA, satisfy a wide range of application needs.

RAMs

CB-90 provides very high density RAMs to meet the needs of complex ASICs with SDRAMs and embedded DRAMs based on MIM2 technology with zirconium oxide (ZrO2). Renesas Electronics' eRAM technology frees the user from the usual constraints of the bottleneck between the chip and separate memory. The result is high overall system speed.

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