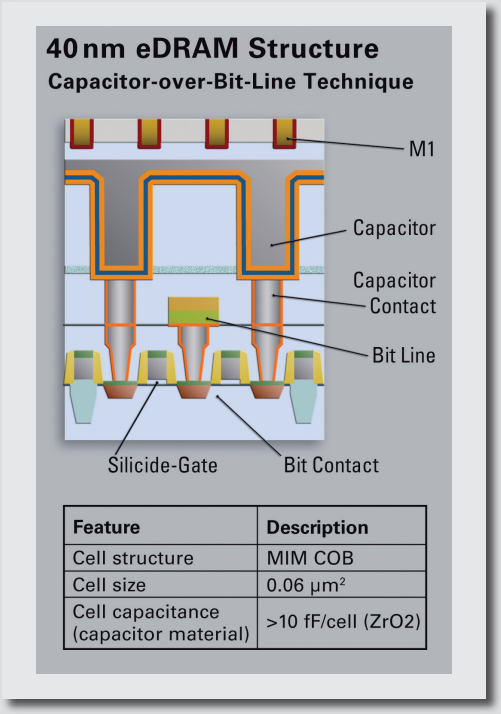
40 nm SoC Technology

CB-40L ASIC Design Platform

Renesas new CB-40L brings system-on-chip development one step beyond and proposes unmatched performances, integration and power consumption.

Using an improved high-K over silicon dioxide transistor technology, derivated from the 55 nm technology, Renesas is able to divide by two the dynamic and static power consumption of the chip compared to the former technology. Furthermore, CB40-L allows unequaled gate and memories density while CPU cores and high speed interfaces are efficiently bundled in the chip.



Feature	Description
Cell structure	MIM COB
Cell size	0.06 µm²
Cell capacitance (capacitor material)	>10 fF/cell (ZrO2)

Features

- 40 nm technology
- Up to 7 metal layers
- Very high gate count up to 400 millions gates
- 1.0 V and 1.1 V core voltage optimized architecture
- Extreme low power consumption down to 0.18 nw/MHz/gate
- Extreme low leakage current using high-K transistors
- I/O voltage options : 1.8 V, 2.5 V, 3.3 V
- Flexible I/O structure supports USB, HDMI, S-ATA, PCIe, LVDS, PCI
- Various package types: PBGA, FPBGA, FCBGA, ...

Product Outline

	CB-40L	
Node length (Lnode)	40 nm (40 nm gate length)	
Metal Layer	Up to 7	
Gate count (raw)	400 Mgates	
Gate density (raw)	2000 Kgates/mm²	
Core VDD	1.0 ± 0.1 V	1.1 ± 0.1 V
Power consumption*	0.18 nW/MHz/gate	0.21 nW/MHz/gate
System frequency	500 MHz	400 MHz
Gate insulator	Hf-doped silicate	
I/O level	1.8 V, 2.5 V, 3.3 V	
IO PAD number	1200 (for wire bonding package, VDD/GND include)	
Package and PAD type	30 µm staggered PAD, PBGA 40 µm straight wire PBGA, 100 µm staggered bump for FCBGA	

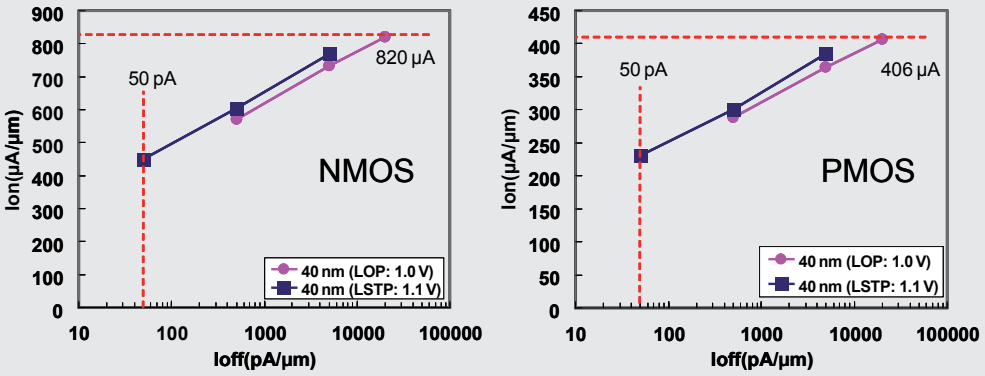
*Activity factor is 0.1

Features

Architecture. The CB-40L technology offers the choice of various different transistor types for enabling an optimum configuration of performance/low power/high-integration targeted area partitioning on the same chip. Furthermore the advanced High-K over silicon dioxide transistor technology inaugurated with the 55 nm reduces considerably the leakage current. This results into a considerable reduction of dynamic and static power consumption compared to the previous technologies.

Power consumption. Using 40 nm enhanced technologies such as High-K over silicon dioxide transistor, to reduce the leakage current, together with advanced design method solutions permits to reduce considerably the power consumption without compromising with the performances. For instance power separation to allow the hibernation of some part of the chip when not used, clock gating to reduce the dynamic power, flip-flop retention to reduce the leakage and mixed cells to achieve the best performance with minimum consumption.

40 nm Tr Characters (LSTP/LOP)



Product
CB-40L (1.1 V LSTP)
CB-40M (1.0 V LOP)

Additional Features

I/Ps. CPU cores such as the new ARM Cortex family (A9, A8, A5, R4) or ARM11 plus peripherals can be collected from our product IP-folio. Application-specific cores for networking (Ethernet), consumer (HDMI), and PC (USB, PCI express, S-ATA) help to build genuine SoC designs. Analog cores like PLLs, ADCs and DACs complete this wide range of macros.

Interfacing. The CB-40 I/O structure permits the broad variety of interfacing support. I/O voltage of 1.8 V, 2.5 V and 3.3 V are supported, allowing a broad variety of interfacing support. USB, S-ATA, HDMI, PCI express standards are ready to use, granting the availability of the latest version of high-speed interfaces. All kind of applications can be met using the range of available packages: PBGA, FPBGA and FCBGA.

RAMs. CB-40 provides very high density RAMs in order to satisfy every need of complex ASICs with SDRAM and embedded DRAMs. Renesas' eDRAM MIM2 process gives the CB-40 a competitive advantage by significantly reducing cell size and improving performance. The technology also facilitates system design by allowing orientation-free cells and signal routes that permit active wires to run over eDRAM macros for optimized integration and performance. With the Renesas' approach of eDRAM technology the user is freed from the bottleneck which exists between the chip and separate memory. High level overall system speed with very limited power consumption can thus easily be achieved.

Application focus. CB-40's features allow fitting perfectly for applications that require the combination of low consumption, high integration rate and high performances with a high amount of high-density RAM: Medical, PLCs, Comunication, PoS, ...

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