Technical Customer Documentation GTM-IP

Errata Sheet

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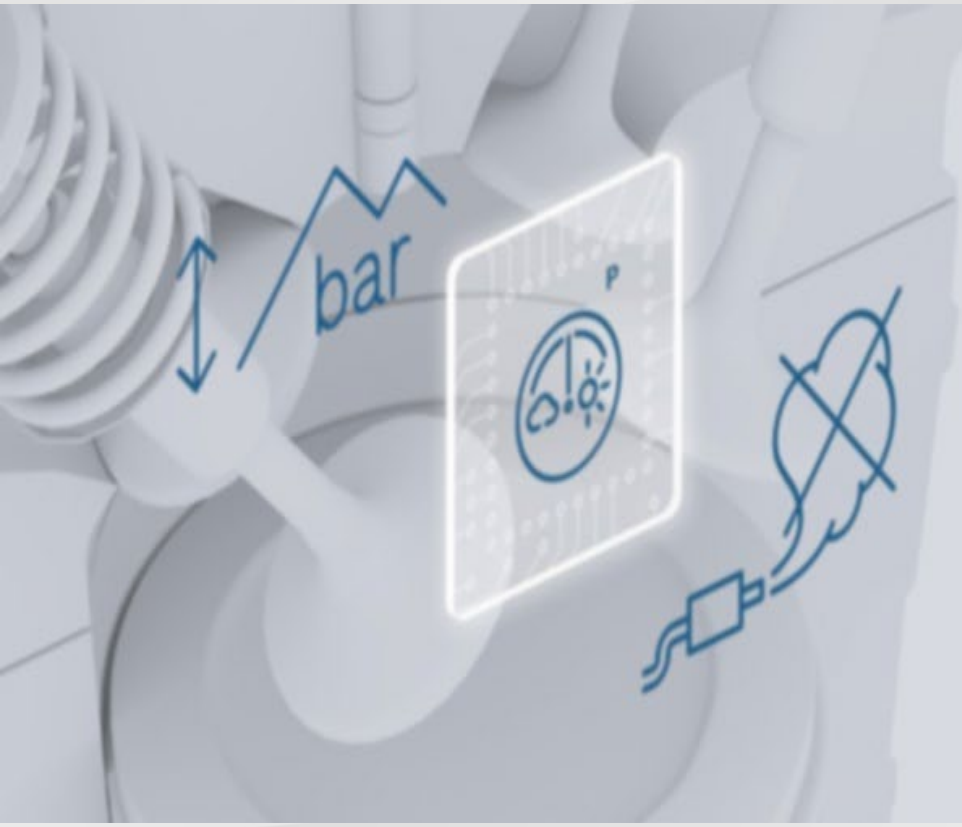

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Revision History

Rev.	Date	Remark
1.00	12.04.2018	• Initial version - Only one Errata sheet for all GTM Generation. • New errata in this revision: GTM-IP-322, GTM-IP-323, GTM-IP-324, GTM-IP-325, GTM-IP-326
1.01	24.05.2018	• New errata in this revision: GTM-IP-329, GTM-IP-331, GTM-IP-332, GTM-IP-333 • Updated erratum in this revision: GTM-IP-322: Updated workaround section
1.02	19.10.2018	• New erratum in this revision: GTM-IP-334 • Updated errata in this revision: GTM-IP-241, GTM-IP-242, GTM-IP-243, GTM-IP-244, GTM-IP-245, GTM-IP-246, GTM-IP-247, GTM-IP-250, GTM-IP-251, GTM-IP-252, GTM-IP-254, GTM-IP-255, GTM-IP-256, GTM-IP-261, GTM-IP-262, GTM-IP-263, GTM-IP-265, GTM-IP-266, GTM-IP-267, GTM-IP-269, GTM-IP-270, GTM-IP-274, GTM-IP-275, GTM-IP-276, GTM-IP-277, GTM-IP-278, GTM-IP-279, GTM-IP-280, GTM-IP-281, GTM-IP-282, GTM-IP-283, GTM-IP-284, GTM-IP-285, GTM-IP-287, GTM-IP-289, GTM-IP-290, GTM-IP-291, GTM-IP-292, GTM-IP-293, GTM-IP-294, GTM-IP-304, GTM-IP-306, GTM-IP-308, GTM-IP-312, GTM-IP-329: updated “refer to” releases GTM-IP-260: Updated workaround section
1.03	28.03.2019	• New errata in this revision: GTM-IP-335, GTM-IP-336, GTM-IP-339
1.03b	03.04.2019	• Corrected “impacted release” release information for: GTM-IP-336, GTM-IP-339
1.04	11.07.2019	• Updated erratum with additional “lost signal” cause: GTM-IP-162 • New errata in this revision: GTM-IP-340, GTM-IP-341, GTM-IP-342
1.05	17.12.2019	• Updated erratum with additional “refer to” cause: GTM-IP-342 • New errata in this revision: GTM-IP-344, GTM-IP-345, GTM-IP-346
1.06	17.03.2020	• Remove internal Release (V3.1.5-BE) from “refer to”: GTM-IP-344, GTM-IP-345, GTM-IP-346 • New errata in this revision: GTM-IP-347, GTM-IP-348
1.06b	30.04.2020	• Corrected DPLL_CTRL_1.PCMF1/2 to DPLL_CTRL_1.PCM1/2 in workaround 3c): GTM-IP-348
1.07	25.05.2020	• Spelling corrections and removing multiple blanks: Be aware that this led to new line breaks across the document • Removed v3.1.5-BC from column “refer to” permanently • New errata in this revision: GTM-IP-349, GTM-IP-350, GTM-IP-351, GTM-IP-352, GTM-IP-353, GTM-IP-354

1.08	10.12.2020	• New errata in this revision: GTM-IP-357, GTM-IP-358, GTM-IP-359, GTM-IP-360, GTM-IP-361
1.08b	14.01.2021	• Corrected Remark for 1.08: Including releases in “refer to”: v1.5.0-A0 for GTM-IP-(62, 72, 73, 74, 75, 76, 77, 78, 80, 85, 90, 91, 96, 97, 104, 105, 106, 107, 110, 111, 112, 113, 114, 118, 119, 120, 121, 122, 123, 125, 126, 127, 128, 129, 130, 131, 133, 135, 136, 137, 138, 139, 140, 143, 146, 150, 152, 153, 154, 158, 161, 163, 164, 166, 167, 168, 169, 170, 172, 173, 174, 175, 178, 181, 202, 204, 205, 209, 210, 215, 218, 219, 220, 221, 222, 223, 251, 271, 272, 278, 283, 292, 300, 301, 302, 306, 317, 320, 336, 339, 340, 342, 346, 348, 353) v1.5.1-A1 for GTM-IP-(351, 353) v1.5.2-A2 for GTM-IP-(351, 353) v2.0.2-A1 for GTM-IP-(162, 166, 167, 168, 169, 170, 172, 173, 174, 177, 208, 209, 210, 212, 215, 218, 219, 220, 221, 222, 223, 247, 271, 272, 292, 300, 301, 306, 317, 323, 348, 351) v2.1.2-A2 for GTM-IP-353 v3.0.3-A1 for GTM-IP-(348, 353) v3.0.3-A2 for GTM-IP-(348, 353) v3.0.4-A1 for GTM-IP-(348, 353) v3.1.4-A0 for GTM-IP-(238, 241, 351, 353) v3.1.5-A0 for GTM-IP-(238, 241, 308, 348, 349, 350, 351, 353) v3.1.5-A1 for GTM-IP-(238, 241, 308, 348, 351, 353) v3.1.5-A2 for GTM-IP-(308, 348, 351, 353) v3.1.5-A3 for GTM-IP-(308, 348, 351, 353) v3.1.5-A4 for GTM-IP-(308, 348, 351, 353) v3.1.5-A5 for GTM-IP-(308, 348, 351, 353) v3.1.5-A6 for GTM-IP-(308, 348, 351, 353) v3.1.5-A8 for GTM-IP-(308, 348, 351, 353) v3.1.5-AA for GTM-IP-(308, 348, 351, 353) v3.1.5-AB for GTM-IP-(308, 348, 351, 353) v3.1.5-AC for GTM-IP-(308, 348, 351, 353) v3.0.5-A1 for GTM-IP-323 v3.0.5-A2 for GTM-IP-351 Removing releases from “refer to”: v3.1.4-A0 for GTM-IP-(344, 345, 352) v3.1.5-A0 for GTM-IP-352
2.00	05.05.2021	• New errata in this revision: GTM-IP-362, GTM-IP-364, GTM-IP-365, GTM-IP-367, GTM-IP-368, GTM-IP-369, GTM-IP-370, GTM-IP-371, GTM-IP-372, GTM-IP-373, GTM-IP-374, GTM-IP-375, GTM-IP-376, GTM-IP-377, GTM-IP-378, GTM-IP-379, GTM-IP-380 • Updated errata in this revision: GTM-IP-136 (case CM0=1 is now covered by new GTM-IP-380)
2.01	06.08.2021	• New errata in this revision: GTM-IP-381, GTM-IP-382, GTM-IP-385, GTM-IP-386, GTM-IP-387, GTM-IP-388, GTM-IP-389, GTM-IP-390, GTM-IP-391, GTM-IP-392, GTM-IP-393, GTM-IP-394 • Updated errata in this revision: GTM-IP-136 (no overstrike text) GTM-IP-358 (remove new Gen4 register)

		GTM-IP-362 (typo) GTM-IP-370 (typo) GTM-IP-376 (remove older releases than v3.0.2-A1) • Using common Font for History and Errata
2.02	20.10.2021	• New errata in this revision: GTM-IP-355, GTM-IP-395, GTM-IP-396, GTM-IP-397, GTM-IP-398, GTM-IP-399, GTM-IP-400, GTM-IP-401, GTM-IP-402, GTM-IP-405 • Updated errata in this revision (typo): GTM-IP-78, GTM-IP-106, GTM-IP-122, GTM-IP-126, GTM-IP-131, GTM-IP-158, GTM-IP-162, GTM-IP-171, GTM-IP-276, GTM-IP-316, GTM-IP-359, GTM-IP-371 • Updated errata in this revision: GTM-IP-364 (grammar correction) GTM-IP-365 (including register name) GTM-IP-368 (defining effects more precisely) GTM-IP-369 (defining workaround more precisely) GTM-IP-372 (grammar correction) GTM-IP-375 (defining effects more precisely) GTM-IP-376 (grammar correction) GTM-IP-392 (including Note) GTM-IP-393 (including Note) GTM-IP-394 (defining description and workaround more precisely) • Including releases in “refer to”: v1.4.0 for GTM-IP-(53, 54, 100) v1.4.4-11 for GTM-IP-(52, 62, 63, 64, 65, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 80, 85, 90, 91, 96, 97, 104, 105, 106, 107, 110, 111, 112, 113, 114, 118, 119, 120, 121, 122, 123, 125, 126, 127, 128, 129, 130, 131, 133, 135, 136, 137, 138, 139, 140, 143, 146, 150, 151, 152, 153, 154, 158, 161, 162, 163, 164, 166, 167, 168, 169, 170, 172, 173, 174, 175, 177, 178, 181, 202, 204, 205, 209, 210, 212, 215, 218, 219, 220, 221, 222, 223, 247, 250, 251, 300, 301, 302, 306, 317, 320, 323, 336, 340, 342, 346, 348, 349, 350, 353, 361) v1.5.0-A0 for GTM-IP-(162, 167, 177) v3.1.5-A0 for GTM-IP-(231, 232, 233, 234, 247, 250, 323) v3.1.5-A1 for GTM-IP-234 v3.1.5-A2 for GTM-IP-(235, 236) v3.1.5-BB and v3.1.5-BD for GTM-IP-322 v4.1.0-0A1 for GTM-IP-(362, 364, 365, 367, 368, 369, 370, 371, 372, 373, 375, 376, 377, 378, 379, 381, 382, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394) v4.1.0-0B0 for GTM-IP-(376, 387) v4.1.0-0B1 for GTM-IP-(376, 382) v4.1.0-0C0 for GTM-IP-385 • Removing releases in “refer to”: v3.1.5-A4 for GTM-IP-(235, 236) v3.1.5-AF for GTM-IP-(262, 263) v3.1.5-B0 for GTM-IP-(262, 263) v3.1.5-B1 for GTM-IP-(262, 263) v3.1.5-B2 for GTM-IP-(262, 263) v3.1.5-B3 for GTM-IP-(262, 263) v3.1.5-B4 for GTM-IP-(262, 263) v3.1.5-B5 for GTM-IP-(262, 263) v3.1.5-B6 for GTM-IP-(262, 263)

		v3.1.5-B7 for GTM-IP-(262, 263) v3.1.5-B8 for GTM-IP-(262, 263) v3.1.5-B9 for GTM-IP-(262, 263) v3.1.5-BA for GTM-IP-(262, 263) v3.1.5-BB for GTM-IP-(262, 263) v3.1.5-BD for GTM-IP-(262, 263)
2.03	17.12.2021	• New errata in this revision: GTM-IP-403, GTM-IP-404, GTM-IP-406, GTM-IP-407, GTM-IP-408, GTM-IP-409, GTM-IP-410, GTM-IP-411, GTM-IP-413, GTM-IP-414, GTM-IP-415, GTM-IP-416 • Updated errata in this revision (typo): GTM-IP-122, GTM-IP-168, GTM-IP-359, GTM-IP-381 • Updated errata in this revision: GTM-IP-281 (workaround) GTM-IP-405 (workaround)
2.04	01.03.2022	• New errata in this revision: GTM-IP-418, GTM-IP-419, GTM-IP-421, GTM-IP-422, GTM-IP-423, GTM-IP-424, GTM-IP-425, GTM-IP-427, GTM-IP-428, GTM-IP-429, GTM-IP-430, GTM-IP-431, GTM-IP-432, GTM-IP-433, GTM-IP-434, GTM-IP-435, GTM-IP-436, GTM-IP-437, GTM-IP-438 • Updated errata in this revision (typo): GTM-IP-166, GTM-IP-259, GTM-IP-262, GTM-IP-405, GTM-IP-413, GTM-IP-416 • Updated errata in this revision (font): GTM-IP-408 • Updated errata in this revision: GTM-IP-262 (workaround) GTM-IP-405 (workaround) GTM-IP-411 (workaround)
2.05	29.04.2022	• New errata in this revision: GTM-IP-417, GTM-IP-426, GTM-IP-439, GTM-IP-440, GTM-IP-441, GTM-IP-445, GTM-IP-446, GTM-IP-448, GTM-IP-449, GTM-IP-450, GTM-IP-451, GTM-IP-452, GTM-IP-453, GTM-IP-454 • Updated errata in this revision: GTM-IP-262 (title, effects, workaround, refer to) GTM-IP-263 (refer to) GTM-IP-405 (effects, description, workaround) GTM-IP-419 (description) GTM-IP-425 (effects) GTM-IP-432 (effects, description) GTM-IP-433 (effects, description) GTM-IP-436 (effects) GTM-IP-437 (effects) GTM-IP-438 (effects, description) • Including v4.1.0-0A2 release in “refer to” for: GTM-IP-(362, 364, 365, 367, 368, 369, 370, 371, 372, 373, 375, 376, 377, 378, 379, 381, 382, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 398, 399, 400, 401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 415, 416, 418, 419, 421, 422, 423, 424, 425, 427, 428, 429, 430, 431, 432, 433, 434, 435, 436, 437)

2.06	30.06.2022	• New errata in this revision: GTM-IP-459, GTM-IP-460, GTM-IP-462, GTM-IP-465, GTM-IP-466, GTM-IP-467, GTM-IP-468, GTM-IP-469 • Updated errata in this revision: GTM-IP-445 (effects, description) GTM-IP-446 (effects, description)
2.07	30.09.2022	• New errata in this revision: GTM-IP-456, GTM-IP-458, GTM-IP-463, GTM-IP-464, GTM-IP-470, GTM-IP-471, GTM-IP-473, GTM-IP-474, GTM-IP-475, GTM-IP-476, GTM-IP-477, GTM-IP-478 • Updated errata in this revision: GTM-IP-262 (title, effects, description, workaround) GTM-IP-329 (description) GTM-IP-347 (workaround) GTM-IP-423 (excluding v3.1.5-B4 in “refer to”) GTM-IP-430 (effects, description, workaround) GTM-IP-462 (description) • Updated specification version in references
2.08	15.12.2022	• New errata in this revision: GTM-IP-479, GTM-IP-480, GTM-IP-481, GTM-IP-482, GTM-IP-486, GTM-IP-487, GTM-IP-488, GTM-IP-490, GTM-IP-492 • Updated errata in this revision: GTM-IP-352 (title, effects, description) GTM-IP-421 (effects, description) • Including v4.1.0-120 release in “refer to” for: GTM-IP-(469, 470, 471) • Including v4.1.0-130 release in “refer to” for: GTM-IP-(469, 470, 471, 473, 476)
2.08a	23.01.2023	• Updated headline and description (“asynchronous”): GTM-IP-488
2.09	31.03.2023	• New errata in this revision: GTM-IP-461, GTM-IP-494, GTM-IP-495, GTM-IP-497, GTM-IP-499, GTM-IP-500, GTM-IP-501, GTM-IP-502, GTM-IP-504 • Updated errata in this revision: GTM-IP-445 (title, effects, description) GTM-IP-490 (title, description) GTM-IP-492 (effects) GTM-IP-431 (effects, description) GTM-IP-(262, 408, 479) (description) GTM-IP-(471, 473) (description, workaround) GTM-IP-479 (description, refer to) GTM-IP-(353, 402, 413, 414, 421, 470, 481, 482, 486, 487) (workaround)
2.10	23.06.2023	• New errata in this revision: GTM-IP-442, GTM-IP-483, GTM-IP-506, GTM-IP-507, GTM-IP-508 • Updated errata in this revision: GTM-IP-(430, 481) (effects) GTM-IP-473 (effects, description) GTM-IP-456 (effects, workaround) GTM-IP-(482, 499) (description)

		GTM-IP-495 (description, workaround) GTM-IP-(451, 462, 480, 497, 500, 501, 502, 504) (workaround)
2.11	29.09.2023	• New errata in this revision: GTM-IP-510, GTM-IP-511, GTM-IP-513, GTM-IP-514, GTM-IP-515, GTM-IP-516, GTM-IP-517, GTM-IP-518 • Updated errata in this revision: GTM-IP-470 (title, description, workaround, refer to) GTM-IP-393 (effects, description) GTM-IP-(407, 478, 494) (description) GTM-IP-490 (description, workaround) GTM-IP-(471, 479, 480, 481, 482, 486, 495, 497, 499, 500, 501, 502, 504) (description, refer to) GTM-IP-(410, 411, 458, 462, 477) (workaround) GTM-IP-473 (refer to)
2.12	15.12.2023	• New errata in this revision: GTM-IP-519, GTM-IP-520, GTM-IP-521 • Updated errata in this revision: GTM-IP-358 (effects) GTM-IP-518 (description) GTM-IP-517 (description, workaround) GTM-IP-(423, 470, 471, 479, 480, 481, 482, 486, 495, 497, 499, 500, 501, 502, 504) (description, refer to) GTM-IP-(515) (refer to)
2.13	27.03.2024	• References updated • New errata in this revision: GTM-IP-512, GTM-IP-522, GTM-IP-523, GTM-IP-525 GTM-IP-526, GTM-IP-527, GTM-IP-529, GTM-IP-530 • Updated errata in this revision: GTM-IP-437 (effects, workaround) GTM-IP-517 (workaround)
2.14	26.04.2024	• New errata in this revision: GTM-IP-528 • Updated errata in this revision: GTM-IP-530 (effects, description, refer to) GTM-IP-(523, 529) (description) GTM-IP-517 (description, workaround)
2.15	28.06.2024	• New errata in this revision: GTM-IP-532, GTM-IP-533 • Updated errata in this revision: GTM-IP-458 (Title, Effects, Description,Workaround) GTM-IP-318 (Title, Description, Workaround) GTM-IP-523 (Workaround)
2.16	27.09.2024	• Updated errata in this revision: GTM-IP-(318, 517) (Description) GTM-IP-522 (Description,Workaround)
2.17	28.02.2025	• New errata in this revision: GTM-IP-537, GTM-IP-538, GTM-IP-540

		• Updated errata in this revision: GTM-IP-(374, 523) (Description) GTM-IP-522 (Description,Workaround)
2.18	30.06.2025	• New errata in this revision: GTM-IP-524, GTM-IP-535, GTM-IP-536, GTM-IP-539 GTM-IP-541 • Updated errata in this revision: GTM-IP-538 (Effects) GTM-IP-351 (Description) GTM-IP-(340, 526) (Workaround)
2.19	30.09.2025	• New errata in this revision: GTM-IP-542, GTM-IP-543

References

This document refers to the following documents.

Authors(s)	Title
AE/EIN2	GTM-IP Specification 1.3, 1.4.0, 1.4.2, 1.5.0, 1.5.1, 1.5.2, 1.5.3, 1.5.4, 1.5.5
AE/EIN2	GTM-IP Specification 2.0.2
AE/PJ-SCI	GTM-IP Specification 2.1.0
AE/EIN2	GTM-IP Specification 3.0.3 / 3.0.4
AE/PJ-SCI	GTM-IP Specification 3.1.2 / 3.1.3 / 3.1.4 / 3.1.5
AE/EID5	GTM-IP Specification 3.5.0
AE/EIY4	GTM-IP Specification 4.1.0
AE/EIY4	GTM-IP_Specification_v4.1 v1.10
AE/EIY4	GTM-IP_Specification_v4.1 v1.20
AE/EIY4	GTM-IP_Specification_v4.1 v1.30
ME-IC/PAY4	GTM-IP_Specification_v4.1 v1.40
ME-IC/PAY4	GTM-IP_Specification_v4.1 v1.50

AE/EIN2	Different device dependent GTM-IP xxx Module Integration Guides
AE/PJ-SCI	Different device dependent GTM-IP xxx Module Integration Guides
AE/EID5	Different device dependent GTM-IP xxx Module Integration Guides

Note: AE/EIN2 is reorganized to ME-IC/PAY4.
Note: AE/PJ-SCI is reorganized to ME-IC/PAY4.
Note: AE/EID5 is reorganized to ME-IC/PAY4.
Note: AE/EIY4 is reorganized to ME-IC/PAY4.

Disclaimer

This errata sheet covers all generations and all deliveries of the GTM-IP, independent from a dedicated GTM-IP customer. All GTM-IP releases listed under the “refer to” column of the erratum definition within this document refer to the GTM-IP release ID as defined in the GTM-IP revision register at the point in time the corresponding release was generated and delivered to GTM-IP customers.

The correct update of the GTM-IP revision register is especially in case of a late ECO fix process in the responsibility of the GTM-IP customer and/or semiconductor vendor. The final judgement whether an erratum is valid for a given piece of silicon therefore is within the sole responsibility of customer and/or semiconductor vendor and may vary from the listing of impacted GTM-IP releases as delivered by Bosch and listed within this document.

Definitions

Severity (low/medium/high):

Describes the severity of a problem in regards of the likelihood of the problem to be visible/detected/recognized by an application and the worst case impact the problem could cause to an application if no circumvention is put in place.

Critical/Non-Critical:

A problem is marked as critical if the problem is likely to impact an application in a way that is severe and visible to the customer and no workaround is available to circumvent the issue.

Errata

Errata-ID	Errata	refer to

Errata-ID	Errata	refer to
GTM-IP-1	Title : GTM Top Level: Pipelined Protocol limited support of wr_response_masking Scope : pipelined mode : write response masking is activated. Severity : Low Classification : Non-critical Effects : If multiple transactions are issued in one pipelined transfer and the transaction buffer has one free entry and another transaction is issued the command is not executed as expected. The handling of the transaction buffer control gets out of sequence. Description : If in pipeline mode the write response masking is activated following limitation exists: Workaround : a) Do not use the Bridge mode write response masking at all b) Ensure that with aei_buffer_cnt = 1 no additional transaction is issued. Deactivate aei_sel and setup a new pipelined transfer sequence.	v1.3

Errata-ID	Errata	refer to
GTM-IP-2	Title : GTM Top Level: Standard/Back2Back Protocol limited support of wr_response_masking Scope : standard mode : write response masking is activated. Severity : Low Classification : Non-critical Effects : If while starting a new transaction the condition aei_free_buffer_cnt = 0 is true, the transaction buffer control gets out of sequence. Description : If in standard mode the write response masking is activated following limitation exists: Workaround : Only start new transactions when write response masking is enabled when aei_free_buffer_cnt != 0.	v1.3

Errata-ID	Errata	refer to
GTM-IP-3	Title : GTM Top Level: DPLL RAM Interface memory timing Scope : The CE is held high as long as the bus interface is selected. This results in multiple READs of the same address. Severity : Low Classification : Non-critical Effects : The function of the bus interface and the DPLL is fully as specified, but in case of an ECC error on this address multiple errors might be detected and signaled. Here only the Licensee can judge if this will be a problem in the overall system. Description : The DPLL memory timing while executing an AEI READ is not as defined in the timing diagrams. Workaround : None	v1.3

GTM-IP-4	Title : GTM Top Level: Debug not fully verified Scope : GTM-IP v1.3 : Req001, Req002, Req003, Req104, Req106, Req107 not functional GTM-IP v1.4 : Req104, Req106, Req107 not functional. Severity : Low Classification : Non-critical Effects : limitation Description : Req001 : Debugger shall be able to read all GTM registers, which are visible from the peripheral bus. Read-access of the debugger must be possible without destroying or changing the contents of these registers. Req002 : Synchronous start and stop of the whole GTM with one or more cores and other peripheral units configurable by debugger. Req003 : Debugger shall be able to read all GTM addresses read-/writeable from the peripheral bus when GTM is running or halted. Req104 : Signals of MCS0-x (Interface to program/data RAM of each MCS) ADDRx(12) DINx(32) DOUTx(32) Channelx(4) (8x MCS channel + 1x CPU) PC_Acc(1) (High: Program-Counter = instruction fetch; Low: data-address = data read/write) RD_WR(1) (RD = data read -> trace DOUT, WR = data write -> trace DIN) have to be routed out of GTM for debugging purposes Valid(1) (High: RAM accessed by MCS; Low: RAM accessed by AEI) Req106 : Signals of DPLL TASI(1) (Low: No active slope of TRIGGER is detected; High: Active slope of TRIGGER is detected) SASI(1) (Low: No active slope of STATE is detected; High: Active slope of STATE is detected) RAM1a/1bc/2_DPLL_Acc(1) (Low: DPLL access; High: CPU access) RAM1a/1bc/2_W1R0(1) (Low: Read; High: Write) RAM1a/1bc/2_CE (1) RAM1a/1bc/2_ADDR(Depends on RAM) RAM1a/1bc/2_DIN(24) RAM1a/1bc/2_DOUT(24) have to be routed out of GTM for debugging purposes	v1.3

Errata-ID	Errata	refer to
	Req107 : Signals of TBU_BASE0: TBU_TS0(27) and TBU_UP0(2) Signals of TBU_BASE1: TBU_TS1(24) and TBU_UP1(1) Signals of TBU_BASE2: TBU_TS2(24) and TBU_UP2(1) Workaround : None	

Errata-ID	Errata	refer to
GTM-IP-5	Title : GTM Top Level: Debug GTM_HALT during RAM init Scope : GTM HALT function. Severity : Low Classification : Non-critical Effects : Description : The GTM_HALT signal should not be set to high during RAM initialization of MCS RAMs. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-6	Title : GTM Top Level: Interrupt clear gtm_aei_irq_clr not functional Scope : GTM top level interrupt. Severity : Low Classification : Non-critical Effects : Description : The clearing of the interrupt with the primary input signal gtm_aei_irq_clr is not functional. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-7	Title : MAP: bit SSL not functional Scope : MAP Severity : Low Classification : Non-critical Effects : Description : STATE Signal select; routing from TIM0_CH2 to TIM0_CH5 not functional. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-8	Title : MAP: bits TSPPx_DLD not functional Scope : MAP Severity : Low Classification : Non-critical Effects : Description : Inverse direction bit generation for PMSM not functional. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-9	Title : MAP: bits TSPPx_IyV not functional Scope : MAP Severity : Low Classification : Non-critical Effects : Description : Disable functionality for PMSM not functional. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-10	Title : TBU: channel 2 FBC mode not fully verified Scope : TBU Severity : Low Classification : Non-critical Effects : Description : TBU channel 0,1 functional. Channel 2 not fully verified but instantiates same RTL code as channel 1. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-11	Title : MON: status bits ACT_CMUx and ACT_CMUFXy exchanged Scope : MON Severity : Low Classification : Non-critical Effects : Description : Bits ACT_CMUFXy and ACT_CMUx exchanged in implementation according to spec. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-12	Title : CMP: not verified Scope : CMP Severity : Low Classification : Non-critical Effects : Description : Not functional. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-13	Title : BRC: Maximum throughput mode (MTM) not functional Scope : BRC Severity : Low Classification : Non-critical Effects : Description : Maximum throughput mode (MTM) not functional. Register BRC_SRC_[x]_ADDR Bit BRC_MODE. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-14	Title : ATOM: SOMS mode not functional Scope : ATOM SOMS mode. Severity : Low Classification : Non-critical Effects : Description : Signal Output Mode Shift not functional. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-15	Title : ATOM: CMP_CTRL <= compare strategy not functional Scope : ATOM Severity : Low Classification : Non-critical Effects : Description : CMP_CTRL <= compare strategy not functional. Register ATOM[i]_CH[x]_CTRL Bit CMP_CTRL. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-16	Title : ATOM: Bit WR_REQ not functional Scope : ATOM Severity : Low Classification : Non-critical Effects : Description : CPU Write request bit for ARU_EN and locking of shadow registers in case of match not functional. Register ATOM[i]_CH[x]_CTRL Bit WR_REQ not functional. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-17	Title : ATOM: Bit WRF not functional Scope : ATOM Severity : Low Classification : Non-critical Effects : Description : Bit Write request fail flag not functional. Register ATOM[i]_CH[x]_STAT Bit WRF not functional. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-18	Title : DPLL: Emergency mode not functional Scope : DPLL Severity : Low Classification : Non-critical Effects : Description : Emergency mode of DPLL not functional. Register DPLL_CTRL_0 Bit RMO=1. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-19	Title : DPLL: Synchronous motor control not functional Scope : DPLL Severity : Low Classification : Non-critical Effects : Description : Synchronous motor control of DPLL not functional. Register DPLL_CTRL_1 Bit SMC=1. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-20	Title : DPLL: Continuous mode for sub_inc generation Scope : DPLL Severity : Low Classification : Non-critical Effects : Description : Continuous mode for sub_inc generation of DPLL not functional. Register DPLL_CTRL_1 Bit DMO=1. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-21	Title : DPLL: Trigger Time stamp extension Scope : DPLL Severity : Low Classification : Non-critical Effects : Description : Trigger Time stamp extension DPLL_APT_sync not functional. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-22	Title : DPLL: State Time stamp extension Scope : DPLL Severity : Low Classification : Non-critical Effects : Description : State Time stamp extension DPLL_APS_sync not functional. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-23	Title : DPLL: TBU resolution Scope : DPLL Severity : Low Classification : Non-critical Effects : Description : Low resolution of TBU not functional in combination with DPLL calculations. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-24	Title : DPLL: Switch between forward/backward directions Scope : DPLL Severity : Low Classification : Non-critical Effects : Description : Switch between forward/backward directions (bit DIR) of DPLL not functional. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-25	Title : DPLL: Action calculation Scope : DPLL Severity : Low Classification : Non-critical Effects : Description : Action calculation of DPLL not functional. Workaround : Calculation has to be done by software.	v1.3

Errata-ID	Errata	refer to
GTM-IP-26	Title : DPLL: DPLL_IRQ_NOTIFY Bit DCGI Scope : DPLL Severity : Low Classification : Non-critical Effects : Engine direction change interrupt not available. Description : This bit is not connected to any interrupt line. Workaround : Polling with software on BWD1/2 necessary.	v1.3

Errata-ID	Errata	refer to
GTM-IP-27	Title : DPLL: DPLL_IRQ_NOTIFY Bits PDI and PEI Scope : DPLL Severity : Low Classification : Non-critical Effects : Two separate interrupts. Description : These bits are not combined to a common interrupt line, but to the separate interrupt lines 0 or 1 respectively. Workaround : Interrupt bundling can be done by software.	v1.3

Errata-ID	Errata	refer to
GTM-IP-28	Title : TIM: TIM0_CH[x]_CTRL Bit 7 (TBU0x_SEL) Scope : TIM Severity : Low Classification : Non-critical Effects : TBU resolution cannot be selected for channels 1 to 7. Description : Bit 7 of TIM0_CH[x]_CTRL register is only available in TIM0 channel 0 and not in TIM0 channel 1 to 7. Workaround : TBU resolution must be established by software on behalf of edge detected interrupt of TIM. Software can then read TBU0 and determine full TBU.	v1.3

Errata-ID	Errata	refer to
GTM-IP-29	Title : MCS: MCS[i]_CTRL bit 16 (RAM_RST) Scope : In the case of an MCFG borrow configuration. Severity : Low Classification : Non-critical Effects : The RAM1 (small RAM) of the MCS instance that is borrowing a RAM is not reset in the case of a SW-RAM reset. Description : RAM1 not reset in case of SW-RAM reset. Workaround : SW: all SW-RAM resets should be applied before modifying MCFG_CTRL register.	v1.3

Errata-ID	Errata	refer to
GTM-IP-30	Title : GTM-HALT for FIFO-RAM, MCS-RAM and DPLL-RAM Scope : GTM HALT function. Severity : Low Classification : Non-critical Effects : Description : Not functional. Workaround :	v1.3

Errata-ID	Errata	refer to
GTM-IP-31	Title : GTM Top Level: AEI Split; Clear MSK_WR_RSP bit in GTM_BRIDGE_MODE register Scope : Failure can occur in synchronous or asynchronous Bridge mode. Severity : Low Classification : Non-critical Effects : AEI split protocol gets stuck. Bus interface hangs. No new transfers possible. Description : If the bridge operates in the mode when MSK_WR_RSP is set. While clearing this bit it can happen that following expected aei_response_ready acknowledges are not sent. Workaround : No workaround available. Don't use MSK_WR_RSP = 1 at all.	v1.3

Errata-ID	Errata	refer to
GTM-IP-32	Title : GTM Top Level: AEI Split; Set MSK_WR_RSP bit in GTM_BRIDGE_MODE register Scope : Failure can occur in synchronous or asynchronous Bridge mode. Severity : Low Classification : Non-critical Effects : Behavior is not AEI split protocol conform. An attached bus master can get out of sequence. Bus interface could hang. No new transfers possible. Description : If the MSK_WR_RSP is set by a write transaction and immediately another write transaction follows there can be an unexpected aei_response_ready signal sent. While clearing this bit it can happen that following expected aei_response_ready acknowledges are not sent. Workaround : Wait with sending of a new transaction after reconfiguring the bridge until the aei_free_buffer_cnt is equal to buffer_size.	v1.3

Errata-ID	Errata	refer to
GTM-IP-33	Title : DPLL: Action calculation Scope : action calculation stops when last action was calculated independent of performing the calculation of all actions so far; the next round starts with a new event or new data. Severity : Low Classification : Non-critical Effects : It may happen that actions are not calculated with the first event possible, but they are going to be calculated within the next events. Description : When not starting with the first action within one increment after the last action no update calculation of the first actions is performed until a new valid input event appears or new data arrived. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-34	Title : GTM Top Level: AEI Bridge; Wrong status on h#3c Scope : AEI bridge Severity : Low Classification : Non-critical Effects : Description : While writing or reading on the undefined address h#3c, aei_status is not showing error code unsupported address. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-35	Title : FIFO_EMPTY/LWM Interrupt generation Scope : FIFO Interrupt behavior. Severity : Low Classification : Non-critical Effects : Interrupt not raised in case of interrupt enable in combination with FIFO internal state. Description : The FIFO_EMPTY/LWM interrupt is not visible at the GTM-IP outside when the interrupt is enabled with the corresponding FIFOx_CHx_EN bit and the FIFO has the status empty and/or the lower watermark is not reached yet. Workaround : The interrupt can be raised by software using the corresponding FIFOx_CHy_NOTIFY bit.	v1.3

Errata-ID	Errata	refer to
GTM-IP-36	Title : GTM Top Level: Bus interface can hang when bridge is configured to MSK_WR_RS = 1 Scope : AEI bridge Severity : Medium Classification : Non-critical Effects : Behavior is not AEI protocol conform. An attached bus master can get out of sequence. Bus interface could hang. No new transfers possible. Description : Depending on clock ratio of aei_clk/sys_clk, configured buffer_depth, idle cycles between transaction requests (aei_sel), point of response requests (aei_response_req) and type of transaction already stored in transaction buffer it can happen that aei_response_ready/aei_ready signals are not sent. Workaround : No workaround available. Don't use MSK_WR_RSP = 1 at all.	v1.3

Errata-ID	Errata	refer to
GTM-IP-39	Title : CMU: CMU Fractional Dividers GCLK, ECLK Scope : CMU Fractional dividers. Severity : Low Classification : Non-critical Effects : Not the full 24 bits can be used to define the input clock division. Description : The fractional divider register values for numerator and denominator use a 24 bit signed value to determine the output clock division value. Workaround : Use only 23 bits to define the division factor.	v1.3

Errata-ID	Errata	refer to
GTM-IP-40	Title : DPLL: CTO, CTON, CSO, CSON bits of register DPLL_STATUS Scope : DPLL Status register. Severity : Low Classification : Non-critical Effects : The bits CTO,CSO, CTON, CSON of the status register are not working correctly. The calculations concerning equations 16.10a,b or 16.5a,b are correct as well as the actions to set the internal values to zero in case of an underflow and to clip data to the maximum positive value in case of an overflow are executed correctly. Description : The status bits CTO, CTON, CSO, CSON were implemented with incorrect behavior compared to the specification. The bits CTON, CSON are signaling that the calculation of equations 16.10a, 16.5a were leading to negative results so that the internal values were set to zero. The status bits CTO, CSO are signaling a real overflow of equations 16.10a,b and 16.5a,b as long as the bits CSON, CTON are not set. When the bits CTO, CSO are set together with the flags CTON/CSON they are all set because of a negative overflow of equations 10.10a or 16.5a . Workaround : Don't use bits CSON, CTON. Bits CSO, CTO are signaling overflow of equations 16.10a,b/16.5a,b in total. The error flag raised together with the bits CTON, CSON can be ignored.	v1.3

Errata-ID	Errata	refer to
GTM-IP-41	Title : AEI Status Signal for TIM[i]_CH[x]_CNTS Scope : AEI Status Signal. Severity : Low Classification : Non-critical Effects : Description : Writing to register CNTS in mode TBCM (in channel 1 to 7) the expected AEI status signal value "10" did not occur. Workaround : Don't write to CNTS register in TBCM mode in channel 1 to 7.	v1.3

Errata-ID	Errata	refer to
GTM-IP-42	Title : TIM: Signal level bit via ARU in mode TIPM Scope : TIM ARU connection. Severity : Low Classification : Non-critical Effects : Description : Assume that TIM is configured in mode TIPM and ISL=1, continuous measurement: The ARU control bit ACB(0) does not represent the signal level state at the time of the last GPR update. In measurement mode one-shot the error is not visible. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-43	Title : TBU: Wrong Timing behavior of TBU debug signals Scope : TBU Debug signals. Severity : Low Classification : Non-critical Effects : The signals GTM_DBG_TBU_UPx (x:0..2) are indicating the update one clock tick too early. Description : The Signals GTM_DBG_TBU_UPx (x:0..2) are triggered one clock cycle before the actual update occurs. Workaround : Add delay register to output GTM_DBG_TBU_UPx (x:0..2).	v1.3

Errata-ID	Errata	refer to
GTM-IP-44	Title : MCS: ECC Error Handling Scope : MCS ECC Error handling. Severity : Low Classification : Non-critical Effects : As a result of this ERRATUM bit 2 in MCS Register STA will never be set as a result of an ECC error of MCS RAM. Description : The ECC Signals of the MCS RAM modules are not handled by the MCS module. Workaround : None	v1.3 v1.4.0 v1.4.2

Errata-ID	Errata	refer to
GTM-IP-45	Title : DPLL: Wrong behavior of DPLL debug signals Scope : DPLL Debug interface. Severity : Low Classification : Non-critical Effects : No distinction between DPLL internal versus AEI accesses can be made during debugging. Description : The DPLL debug output signals gtm_dbg_dpll_ram1a_acc, gtm_dbg_dpll_ram1b_acc and gtm_dbg_dpll_ram2_acc are not operating correctly. Instead of indicating DPLL internal versus AEI ram accesses, all accesses to the RAMs are leading to a pulse on this signals. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-46	Title : TOM: 0% duty cycle with tom_cm1=0 immediately after 100% duty cycle with tom_cm1>tom_cm0 not applied Scope : TOM PWM generation. Severity : Low Classification : Non-critical Effects : In the described case a requested duty cycle of 0% is not applied. Description : If first 100 % duty cycle with tom_cm1>tom_cm0 is applied for more than one period and afterwards 0% duty cycle is requested by setting tom_cm1=0, the 0% duty cycle is not applied. The output stays at 100% duty cycle although tom_cm1=0. The erratum is not valid for 100% duty cycle with tom_cm1=tom_cm0. Workaround : For 100% duty cycle register tom_cm1 has to be set equal to tom_cm0 (tom_cm1=tom_cm0).	v1.3

Errata-ID	Errata	refer to
GTM-IP-47	Title : ATOM: 0% duty cycle with atom_cm1=0 immediately after 100% duty cycle with atom_cm1>atom_cm0 not applied Scope : ATOM PWM generation in SOMP mode. Severity : Low Classification : Non-critical Effects : In the described case a requested duty cycle of 0% is not applied. Description : If first 100 % duty cycle with tom_cm1>tom_cm0 is applied for more than one period and afterwards 0% duty cycle is requested by setting tom_cm1=0, the 0% duty cycle is not applied. The output stays at 100% duty cycle although tom_cm1=0. The erratum is not valid for 100% duty cycle with tom_cm1=tom_cm0. Workaround : For 100% duty cycle register atom_cm1 has to be set equal to atom_cm0 (atom_cm1=atom_cm0).	v1.3

Errata-ID	Errata	refer to
GTM-IP-48	Title : DPLL: incorrect AEI status on write access to shadow register Scope : DPLL Severity : Low Classification : Non-critical Effects : IF the AEI status is evaluated by the CPU, the accessing CPU my assume that the write access was successful. Description : On a write access to the register DPLL_CTRL_0_SHADOW_STATE, DPLL_CTRL_0_SHADOW_TRIGGER, DPLL_CTRL_1_SHADOW_STATE, DPLL_CTRL_1_SHADOW_TRIGGER the incorrect AEI status "00" is returned instead of "10". Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-49	Title : DPLL: RAM 1A unsupported address Scope : DPLL Severity : Low Classification : Non-critical Effects : On access to the address range 0x28380 to 0x283fc all operations are performed on the RAM 1A bus. This may lead to an undesired access to RAM area. Description : On a read/write to address 0x28380 to 0x283FC the RAM 1A is accessed. According to address map of this device this address areas must not address RAM 1A and return the AEI status 'unsupported address' instead. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-50	Title : TOM/ATOM: forced update does not lead to an asynchronous update of output Scope : TOM / ATOM SOMP mode. Severity : Medium Classification : Non-critical Effects : In the described case the output is not set asynchronously to correct value. Description : In case of PWM generation running in continuous mode and a forced update of CM1 register with the value of SR1 register at point in time of CN0 > SR1 does not lead to an asynchronous setting of output according to new values of register CM0, CM1 and the current value of register CN0. Workaround : If only CM1 has to be changed write directly to CM1 instead of forcing update of CM1 with SR1.	v1.3

Errata-ID	Errata	refer to
GTM-IP-51	Title : DPLL: DPLL_STATUS bit#4 (CRO) Scope : DPLL Severity : Low Classification : Non-critical Effects : When a CRO overflow in the arithmetic occurs this cannot be recognized. The calculation itself is terminated by setting the result value with "0xFFFFFF", which allows to proceed with the further calculations. Description : The CRO bit of the DPLL status register is not set when an overflow occurs. Workaround : None	v1.3

Errata-ID	Errata	refer to
GTM-IP-52	Title : DPLL: Data loss of PMTR data transferred via ARU interface Scope : DPLL Severity : Medium Classification : Non-critical Effects : An action could not be calculated because data are not available for DPLL. Description : Depending on the state of the ARU transfers compared to the internal DPLL status (CAIP) it is possible that the ARU data transfer of action data (PMTR) is confirmed at the ARU interface but the data got lost. Workaround : None	v1.3 v1.4.0 v1.4.2 v1.4.4-11

Errata-ID	Errata	refer to
GTM-IP-53	Title : DPLL: Sub-increment correction wrong at direction change when direction change occurs around a gap Scope : DPLL Severity : High Classification : Critical Effects : The sub_inc generation is wrong. Description : The sub_inc correction is wrong because the values nmb_t_tar/old are used in a wrong manner which is needed for correction of sub_inc . The PSTC value correction is also wrong. Workaround : For sub_inc correction use pulse correction mode, for PSTC write correct value by CPU.	v1.3 v1.4.0

Errata-ID	Errata	refer to
GTM-IP-54	Title : DPLL: Wrong storage of time stamp in RAM data field, when a gap occurs. Scope : DPLL Severity : High Classification : Critical Effects : The TSF data fields in memory are inconsistent. The prediction of the next increment and the calculation of actions can be wrong. Description : The values TSF are stored to wrong memory locations when the gap should be extended. Workaround : None	v1.3 v1.4.0

Errata-ID	Errata	refer to
GTM-IP-57	Title : DPLL: Wrong clipping behavior for CDT_TX/SX_nom values following equations 16.5.a and 16.10b of Specification. Scope : DPLL Severity : Medium Classification : Non-critical Effects : The clipping behavior for detection of clipping of the CDT_TX/SX_nom values so far restricts the size of the variables to 23 bit which leads to an inaccuracy of add_in calculations for longer event cycles. Description : The clipping behavior for detection of clipping of the CDT_TX/SX_nom values so far restricts the size of the variables to 23 bit which leads to an inaccuracy of add_in calculations for longer event cycles. Workaround : None	v1.3 v1.4.0 v1.4.2

Errata-ID	Errata	refer to
GTM-IP-58	Title : DPLL: Incorrect calculation of PVT window in case of low_res = 1 and ts0_hrt = 1. Scope : DPLL Severity : Medium Classification : Non-critical Effects : PVT wrong if low_res=1 and ts0_hrt=1. Description : The calculation of the PVT window is incorrect when low_res= 1 and ts0_hrt = 1. Workaround : None	v1.3 v1.4.0 v1.4.2

Errata-ID	Errata	refer to
GTM-IP-59	Title : DPLL: Wrong sub_inc correction for direction change. Scope : DPLL Severity : Medium Classification : Non-critical Effects : The sub_inc generation is wrong when a direction change occurs. Description : Following circumstances of wrong pulse correction were found. a) pulse correction in direction change is incorrect when it was not possible to apply all the sub_incs for more than one event window before the direction change happens. E.g. very short time window for new event in direction change due to a special test case where the event frame before the direction change is in the same duration as the event frames of normal speed forward/backward operation. b) incorrect pulse correction when pd_store values have to be corrected in direction change c)The pulse correction is wrong when between the calculation of the pulse correction and the storage of the correction value in the inc_cnt register further fast sub_inc pulses are generated. Workaround : In case of a) and c) this is a physically unrealistic situation for a combustion engine, because in direction change the convolution is much slower than in normal forward operation where this effects should not be active In case of b) sub_inc correction can be done by the CPU in pulse correction mode via mpval.	v1.3 v1.4.0 v1.4.2

Errata-ID	Errata	refer to
GTM-IP-60	Title : DPLL: No sub_incs for sub_in2 generator in direct load mode Scope : DPLL Severity : Medium Classification : Non-critical Effects : No sub_incs for sub_in2 generator in direct load mode. Description : In direct load mode no sub_incs can be generated on output signal sub_inc2_2. Workaround : None	v1.3 v1.4.0 v1.4.2

Errata-ID	Errata	refer to
GTM-IP-61	Title : DPLL: Unintended sub_incs for trigger out of range or state out of range Scope : DPLL Severity : Medium Classification : Non-critical Effects : Unwanted sub_incs depending on mode (RMO,SMC) if signals TOR or SOR equal to one. Description : If the internal signals tor=1 or sor=1 sub_inc pulses will be generated on the sub_inc_c outputs. This was identified for test case vp87. Workaround : None	v1.3 v1.4.0 v1.4.2

Errata-ID	Errata	refer to
GTM-IP-62	Title : GTM_Top level: Bus interface blocked by 2 consecutive write commands to the BRIDGE_MODE register Scope : All AEI protocols variants. Severity : Low Classification : Non-critical Effects : GTM AEI bus interface is blocked, depending on the AEI protocol variant aei_ready or aei_response_ready will not occur. Description : Two consecutive write commands to the BRIDGE_MODE register, can result in a missing aei_response_ready or aei_ready. Due to this the bus interface will be blocked forever, only a hardware aei_reset can resolve this situation. This behavior can occur if the second write command is issued while the signal aei_free_buffer_cnt !=buffer_depth_c. Workaround : Workaround 1: Do not make use of 2 consecutive write commands to the BRIDGE_MODE register, any combinations of the 2 write commands can be collapsed to 1 write command. Workaround 2: Ensure that the second write command is issued while aei_free_buffer_cnt =buffer_depth_c. This condition cannot be controlled/observed by the hardware which means, it must be guaranteed by software e.g. a loop which ensures that dependent of the aei_clk/sys_clk ratio a certain amount of clocks will pass before the second write is issued. This will guarantee that the first write command is fully executed and the AEI transaction buffer is empty before the second write is accepted.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1

Errata-ID	Errata	refer to
GTM-IP-63	Title : SPE: SIE bits are not functional Scope : SPE Severity : Low Classification : Non-critical Effects : Every three input signals of the corresponding TIM module are evaluated by the SPE module independent of SIE bit. Therefore a toggling signal of the input where SIEx is cleared may disturb correct input pattern detection. Description : IF bit SIEx is set to 0, only the update of register AIP is blocked. Internal actions (e.g. NIPD IRQ generation, Pattern Pointer update, ...) are not affected by the SIEx bits. Workaround : For every SPE input where SIEx is set to 0, the corresponding TIM input port has to be set to a defined constant level. This level has to be taken into account if defining the pattern SPE[i]_PAT.	v1.3 v1.4.0 v1.4.2 v1.4.4-11

Errata-ID	Errata	refer to
GTM-IP-64	Title : TOM/ATOM force update for disabling a channel Scope : TOM/ATOM SOMP mode. Severity : Low Classification : Non-critical Effects : In the described case it may happen that at CHx_CN0=CHx_CM0-1 channel x or others are disabled and/or the output of channel x or others are disabled too early (less than one CMU_FXCLK / CMU_CLKx tick). As a result the value of CN0 of disabled channel may be one less than expected. Description : If the trigger output of one channel x (TRIG[x]) is used to update ENDIS_STAT with value of ENDIS_CTRL and/or OUTEN_STAT with value of OUTEN_CTRL it may happen that depending on CMU_CLK_NUM and CMU_CLK_DEN the update takes places during time window CHx_CN0=CHx_CM0-1 instead of the CHx_CN0=CHx_CM0 (i.e. after the time window CHx_CN0=CHx_CM0-1). Workaround : None	v1.3 v1.4.0 v1.4.2 v1.4.4-11

Errata-ID	Errata	refer to
GTM-IP-65	Title : TOM: CLK_SRC value '101', '110' and '111' leads to dead lock of channel Scope : TOM Severity : Low Classification : Non-critical Effects : In the described case the CLK_SRC value can no longer updated by a forced update. It stays on the value '111' until the channel it is reset by SW (bit RST_CHx in register TOM[i]_TGC[0/1]_CTRL) or by HW-reset. Description : After updating the CLK_ SRC register with the value '101','110','111' either by normal update at the end of a period (CN0 >= CM0) or by a forced update the compare units CCU0 and CCU1 are stopped. Then, a forced update of the CLK_SRC register is no longer possible because of deselection of FXCLK. As a result the clock of the compare units cannot be enabled again by forced update. Workaround : Don't write to bit field CLK_SRC_SR of register TOM[i]_CH[x]_CTRL the value '111'.	v1.3 v1.4.0 v1.4.2 v1.4.4-11

Errata-ID	Errata	refer to
GTM-IP-66	Title : GTM: auto clear of bit RST in register GTM_RST not functional Scope : GTM Severity : Low Classification : Non-critical Effects : In the described case the first write access after a soft reset is not performed. Description : After setting the bit RST in register GTM_RST this bit is not reset automatically. Because of this, the soft reset stays active until the next AEI access. If the following access is a write access, the write cannot be performed correctly because of active reset although the write access clears the bit RST and deactivates the soft reset. If the following access is a read access, the read is performed correctly, the bit RST is cleared and deactivates the soft reset. Workaround : Read back the register GTM_RST immediately after each setting of bit RST in register GTM_RST.	v1.3

Errata-ID	Errata	refer to
GTM-IP-67	Title : DPLL: wrong reset values for action output data Scope : DPLL Severity : Low Classification : Non-critical Effects : The only effect is that the difference between the wrong and the specified reset value can be seen, when the registers are read out via AEI Interface. In case of action calculation the register is only read out via ARU submodule where an action calculation has happened before. In such a case the reset value is no longer valid and visible. Description : The DPLL registers DPLL_TSA0..23/31 and DPLL_PSAC0..23/31 are in reset state loaded with "0x000000" instead of specified "0x7FFFFF". Workaround : None	v1.3 v1.4.0 v1.4.2 v1.4.4-11

Errata-ID	Errata	refer to
GTM-IP-68	Title : TOM: after (channel) reset the channel starts with SYS_CLK instead of FX_CLK0 Scope : TOM Severity : Low Classification : Non-critical Effects : In the described case, if the Global Clock Divider is programmed to a value < 1, the CCUx units would generate PWM signals of wrong period. Description : After a (channel) reset of a TOM channel the CLK_SRC register is reset to 000 but the selected clock is the SYS_CLK (clock input of Global Clock Divider) instead of the specified FX_CLK0. Workaround : After reset of a TOM channel force the update of CLK_SRC register before enabling generation of PWM signal.	v1.3 v1.4.0 v1.4.2 v1.4.4-11

Errata-ID	Errata	refer to
GTM-IP-69	Title : ATOM: in SOMP mode bit ACBO signaling inconsistent Scope : ATOM SOMP mode. Severity : Low Classification : Non-critical Effects : In the described mode the signaling of CCU0 trigger events in register ATOM[i]_CH[x]_STAT is incorrect. Description : If ATOM channel is running in SOMP mode, on a CCU1 trigger the bit ACBO[4] in register ATOM[i]_CH[x]_STAT is set, but not bit ACBO[3] on a CCU0 trigger. Workaround : Don't evaluate SCBO bit field in ATOM SOMP mode. Use ATOM_IRQ_NOTIFY register instead to check for CCU0 or CCU1 trigger.	v1.3 v1.4.0 v1.4.2 v1.4.4-11

Errata-ID	Errata	refer to
GTM-IP-70	Title : MCS: MCS write access to common trigger register Scope : MCS Severity : High Classification : Non-critical Effects : The write access of the corresponding MCS channel will be lost completely, which may cause potential problems in applications, where the common trigger register is written by both, an MCS-channel and the CPU. Description : If an MCS-channel and CPU via AEI are setting (clearing) a bit of the trigger register at the same time with an STRG (CTRG) write access, the AEI access will be prioritized as mentioned in the specification. Workaround : Duplicate each MCS write Access to the trigger register in the MCS code and assure that the delay between write accesses from CPU to the trigger register is more than 9 clock cycles.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1

Errata-ID	Errata	refer to
GTM-IP-71	Title : TOM/ATOM : PWM generation with register CM0=CM1=1 not correct Scope : TOM/ATOM Severity : Low Classification : Non-critical Effects : The signal level of the TOM/ATOM output signal is not correct. A pulse will be generated instead of a constant output signal with inverse signal level. Description : If the configuration registers CM0 and CM1 are set to 1, the output signal should set to inverse signal level (0 % duty cycle) but a pulse of one period is generated. Following hint has to be part of specification: If CM0=0 or CM0=1, no PWM is generated at all. The output is the inverse value of signals level bit. Workaround : Avoid configuration of CM0=1.	v1.3 v1.4.0 v1.4.2 v1.4.4-11

Errata-ID	Errata	refer to
GTM-IP-72	Title : DPLL: reading DPLL_RAM_INI triggers RAM initialization Scope : DPLL Severity : Low Classification : Non-critical Effects : In the described case the DPLL RAM initialization may be triggered unintentional. Description : Reading the register DPLL_RAM_INI may set bit 4 of register and thus start DPLL RAM initialization. If this happens depends on the preceding read/write access data. Workaround : Before reading register DPLL_RAM_INI perform a reset of AEI bridge and read register GTM_BRIDGE_MODE. Make sure that no other read/write access occurs between reading back GTM_BRIDGE_MODE and reading DPLL_RAM_INI.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-73	Title : DPLL: AEI status '10' on write access to read only register Scope : DPLL Severity : Low Classification : Non-critical Effects : In the described case the wrong AEI status is returned. Description : A write access to the read only register DPLL_AOSV_2, DPLL_CTRL_0_SHADOW_TRIGGER, DPLL_CTRL_0_SHADOW_STATE, DPLL_CTRL_1_SHADOW_TRIGGER, DPLL_CTRL_1_SHADOW_STATE returns the AEI status '10' instead of '00'. Workaround : None	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-74	Title : GTM_Top level: After a GTM bus bridge reset the following transfer can be performed twice Scope : All AEI protocols variants. Severity : Low Classification : Non-critical Effects : In the described case an unexpected state can occur. E.g. transfer after GTM bridge reset is a FIFO access, this will result in an unexpected FIFO state (Write: data was issued twice to FIFO; Read: one data will be lost). This failure can be activated dependent on the protocol, GTM_BRIDGE_MODE in use, buffer depth of the bridge, clock frequencies. Description : A write to bit BRG_RST of register GTM_BRIDGE_MODE will perform a reset of the GTM bus bridge. The next following transfer (read / write) can be executed twice. Workaround : Every time after issuing a bridge reset by writing the BRG_RST Bit =1. The next following transfer must be to a register which is not sensitive to twice read or write. It is recommended to use a READ to register GTM_BRIDGE_MODE.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-75	Title : GTM_Top level: GTM bus bridge - restriction on mixing of AEI protocol variants Scope : Mixing AEI protocols variants. Severity : Low Classification : Non-critical Effects : Leaving Split mode by aei_split=0 while aei_free_buffer_cnt != buffer_depth_c can influence the correct operation of consecutive transactions in AEI pipelined or standard protocol. Description : Activation/deactivation of AEI split protocol is only allowed if the aei_free_buffer_cnt = buffer_depth_c otherwise the correct operation of the bus bridge cannot be ensured. Workaround : If protocol mixing is implemented: Enter Split mode: Ensure that aei_split=1 is assigned only if aei_free_buffer_cnt = buffer_depth_c; Leave Split mode: Ensure that aei_split=0 is assigned only if aei_free_buffer_cnt = buffer_depth_c.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1

Errata-ID	Errata	refer to
GTM-IP-76	Title : GTM_Top level: GTM bus bridge - Delayed execution of AEI write command with AEI standard back2back protocol in synchronous mode Scope : AEI protocol standard back2back. Severity : Low Classification : Non-critical Effects : Due to this faulty behavior up to buffer_depth write transactions are not executed, this may result in unexpected GTM behavior. Description : If bridge is configured to MSK_WR_RS = 1 and BRG_MODE= 0 and AEI standard back2back protocol is in use and the last accepted write transfer results in an aei_free_buffer_cnt= 0 and no further transfer is requested (aei_sel=0) then the bridge does not execute the stored commands in the transaction buffer. The bridge will continue executing the stored commands when aei_sel=1 is applied (next new transfer is requested). Workaround : End each back2back transfer with a "dummy read" this will ensure that all stored commands are executed.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-77	Title : GTM_Top level: GTM bus bridge - restriction on using AEI pipelined protocol in synchronous mode Scope : AEI protocol pipelined. Severity : Medium Classification : Non-critical Effects : This faulty behavior may result in unexpected GTM behavior. Description : If bridge is configured to MSK_WR_RS = 1 and BRG_MODE= 0 and AEI pipelined protocol is in use and the last accepted transfer results in an aei_free_buffer_cnt= 0 while aei_pipe = 1 then the bridge generates unexpected write and read commands to the GTM_IP. Workaround : a) Insert new transfers in AEI pipelined protocol only if aei_free_buffer_cnt > 1. If more transfers have to be scheduled when aei_free_buffer_cnt = 1 then stop AEI pipeline protocol by deasserting aei_pipe and start a new AEI pipelined transaction. b) use bridge in mode MSK_WR_RS = 0.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-78	Title : TIM: TIM input signal incorrect while TIM_RST is active Scope : TIM Severity : Low Classification : Non-critical Effects : TIM debug out pin will not show same signal characteristic as primary input signal if TIM_RST is assigned. Description : While TIM_RST is active the input to the TIM_CH, TDU unit and the TIM debug out port is assigned "0" independent of the primary TIM input signal value. Workaround : None	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-80	Title : TIM: TIM input signal incorrect while TIM channel is disabled Scope : TIM Severity : Low Classification : Non-critical Effects : Description : While TIM_EN=0 in register TIM[i]_CH[x]_CTRL, the bit 0 of ECNT is 0 and not reflecting the actual signal level at the filter output. This means that the signal value embedded in register TIM[i]_CH[x]_GPRn, TIM[i]_CH[x]_CNTS and TIM[i]_CH[x]_ECNT will be not showing the filtered output signal value. Workaround : None. As soon as the TIM channel is enabled the signal value bit 0 of ECNT is correct.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-81	Title : TIM: TGPS mode reset behavior of ECNT not functional Scope : TIM Severity : Low Classification : Non-critical Effects : Description : The setting ECNT_RESET=1 in register TIM[i]_CH[x]_CTRL has no function. Workaround : None	v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-82	Title : TIM: TGPS mode delayed start of operation Scope : TIM Severity : Low Classification : Non-critical Effects : Description : If the setting ISL=0,DSL=1 and TIM_MODE = 101 in register TIM[i]_CH[x]_CTRL is configured, the counting of clock events in TIM[i]_ch[x]_CNT is started with the first rising input signal edge and not immediately with enabling the channel when the input signal is 1. Workaround : Setup the TIM channel in a way that it is ensured that a rising edge is present immediately after the channel is enabled. This can be achieved by the following configuration sequence: --Activate TGPS with DSL=1 WRITE TIM_CH_CTRL #DSL | #TGPS -- set CNTS to 0 to prevent TIM_CNT from counting WRITE TIM_CH_CNTS h#0 -- set TIM input via IN_SRC reg to 1 WRITE TIM_IN_SRC h#A -- enable the channel WRITE TIM_CH_CTRL #DSL | #TGPS | #EN -- set TIM input via IN_SRC reg to 0 WRITE TIM_IN_SRC h#1 -- set CNTS to sampling frequency WRITE TIM_CH_CNTS h#xxx -- clear notify bit WRITE TIM_CH_NOTIFY h#1 -- switch back to TIM_CH input WRITE TIM_IN_SRC h#5	v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-83	Title : TIM: TGPS mode input signal delayed by one system clock Scope : TIM Severity : Low Classification : Non-critical Effects : This will result in a deviation of 1 if TBU values running on system clock are used for capturing in the TIM[i]_CH[x]_GPRn registers. Description : The TIM channel input signal is delayed by one additional system clock before it is used for gating the TIM[i]_CH[x]_CNT counter. Workaround : None	v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-84	Title : TIM: TGPS one shot mode counter value incorrect Scope : TIM Severity : Low Classification : Non-critical Effects : Description : After the TIM channel is stopped in TGPS one shot mode the register TIM[i]_CH[x]_CNT has the value 1. The correct expected value should be 0. Workaround : None	v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-85	Title : TIM: TPWM one shot mode counter value incorrect Scope : TIM Severity : Low Classification : Non-critical Effects : Description : After the TIM channel is stopped in TPWM one shot mode the register TIM[i]_CH[x]_CNT has the value 1. The correct expected value should be 0. Workaround : None	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-86	Title : TIM: TPWM mode with external capture ARU signal level incorrect Scope : TIM Severity : Low Classification : Non-critical Effects : Description : If the setting EXT_CAP_EN=1, ARU_EN=1 and TIM_MODE = 000 in register TIM[i]_CH[x]_CTRL is configured, the signal value in the ARU data word is incorrect. Workaround : None	v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-87	Title : TIM: TBCM mode with external capture edge counter not functional Scope : TIM Severity : Low Classification : Non-critical Effects : Description : If the setting EXT_CAP_EN=1 and TIM_MODE = 100 in register TIM[i]_CH[x]_CTRL is configured, the edge counter ECNT is not functional. Only bit 0 is toggling on an input vector change all other bits keep 0. The embedded ECNT value in register TIM[i]_CH[x]_GPRn, TIM[i]_CH[x]_CNTS shows the same behavior. Workaround : None	v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-88	Title : TIM: TBCM mode with external capture not functional Scope : TIM Severity : Low Classification : Non-critical Effects : Description : If the setting EXT_CAP_EN=1 and TIM_MODE = 100 in register TIM[i]_CH[x]_CTRL is configured, an external capture event does not capture data in the registers TIM[i]_CH[x]_GPRn and is not issuing a NEWVAL interrupt. If ARU_EN=1 is set, no ARU transfer is initiated on an external capture event. Workaround : None	v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-89	Title : TIM: TGPS mode with external capture not functional Scope : TIM Severity : Low Classification : Non-critical Effects : Description : If the setting EXT_CAP_EN=1 and TIM_MODE = 101 in register TIM[i]_CH[x]_CTRL is configured, the specified functionality is not functional. Workaround : None. Don't use this configuration.	v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-90	Title : TIM: While timeout event occurs ARU signal level is not updated Scope : TIM Severity : Low Classification : Non-critical Effects : Description : If the setting ARU_EN=1 in register TIM[i]_CH[x]_CTRL is configured and a new ARU transfer is initiated due to a TDU timeout event the ARU signal value bit is not updated to the actual signal value. Workaround : Don't use the signal level value transferred with the TDU timeout ARU transfer. Take instead the signal value of the last ARU transfer in TIEM mode.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-91	Title : TIM: GPRz_OFL bit set when ARU is enabled and GPR capture event and ARU is serviced at the same time Scope : TIM Severity : Low Classification : Non-critical Effects : Description : If the setting ARU_EN=1 in register TIM[i]_CH[x]_CTRL is configured and an ARU transfer is serviced in the same system clock cycle as a new capture event takes place the GPRz_OFL bit is set. No update of the ARU signal level bit to the actual input value is done. Workaround : None. Don't use ARU routing if input signal change time is smaller than ARU round trip time.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-92	Title : TIM: TIMx_CH[0]_CTRL Bit 7 (TBU0x_SEL) Scope : TIM Severity : Low Classification : Non-critical Effects : TBU resolution can be selected for channel 0 in instances x>=1. Description : Bit 7 of TIMx_CH[0]_CTRL register is available in instance x>=1. Higher TBU resolution can be selected. Workaround : Don't write Bit 7 with value 1.	v1.3

Errata-ID	Errata	refer to
GTM-IP-94	Title : DPLL: Unintended missing trigger/state interrupts Scope : DPLL in normal and emergency mode, SMC-mode. Severity : High Classification : Critical Effects : Leads to unexpected missing trigger/state which leads to loss of lock condition. Description : The missing trigger/state interrupt occurs unintended even when the relevant input signal is correct. Workaround : Not known, would probably depend on intended operation mode.	v1.3

Errata-ID	Errata	refer to
GTM-IP-96	Title : GTM_Top level: GTM bus bridge - Delayed execution of AEI write command with AEI standard protocol in synchronous mode Scope : AEI protocol standard. Severity : Low Classification : Non-critical Effects : Due to this faulty behavior up to buffer_depth write transactions are not executed, this may result in unexpected GTM behavior. Description : If bridge is configured to MSK_WR_RS = 1 and BRG_MODE= 0 and AEI standard protocol is in use and the last accepted write transfer results in an aei_free_buffer_cnt= 0 and no further transfer is requested (aei_sel=0) then the bridge does not execute the stored commands in the transaction buffer. The bridge will continue executing the stored commands when aei_sel=1 is applied (next new transfer is requested). Workaround : End each standard transfer with a "dummy read" this will ensure that all stored commands are executed.	v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-97	Title : MCFG: Borrow mode Scope : MCS RAM configuration. Severity : Low Classification : Critical Effects : In the described case the MCS reads wrong data out of RAM. Description : If MCFG configures an MCS instance in borrow mode and the corresponding MCS reads data on its RAM port 1, wrong data is read. Workaround : None	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1

Errata-ID	Errata	refer to
GTM-IP-99	Title : DPLL: Software reset Scope : DPLL Severity : Low Classification : Non-critical Effects : In the above mentioned test case the DPLL is disabled in backwards direction. After starting the DPLL again (den = 1) the DPLL should start in forward mode but due to the missing reset of the direction state register the DPLL goes back to backward mode again. Description : When DPLL is disabled the reset of the state registers is not executed. Workaround : Perform software reset when DPLL is disabled.	v1.5.0-A1 v1.5.1-A1 v1.5.2-A1

Errata-ID	Errata	refer to
GTM-IP-100	Title : TOM: CN0 starts counting although FXCLK is disabled Scope : TOM Severity : Low Classification : Non-critical Effects : In the described case the counter CN0 of a TOM channel may start counting although global FXCLK is disabled. Description : If under following conditions -update of work register is disabled (UPEN_CTRLx=0 of register TOM[i]_CH[x]_GLB_CTRL), -CMU FXCLK is disabled, -CM0,CM1 > 0 the TOM channel is enabled, the counter CN0 starts counting with SYS_CLK period. Workaround : Enable TOM channels after enabling FXCLK.	v1.3 v1.4.0

Errata-ID	Errata	refer to
GTM-IP-101	Title : TIM: External capture in TPWM and TPIM not correctly disabled Scope : TIM Severity : Low Classification : Non-critical Effects : Tim channel will capture data to GPR register and issue an interrupt if an external capture event occurs. Description : If Bit EXT_CAP_EN = 1 and TIM_EN = 0 and TIM_MODE = TPWM or TPIM tim channel will capture on an external capture event. This should not be the case because with TIM_EN = 0 the function should be disabled. Workaround : Write Bit EXT_CAP_EN together with TIM_EN bit. Ensure EXT_CAP_EN is only set if TIM_EN= 1.	v1.5.0-A1 v1.5.1-A1 v1.5.2-A1

Errata-ID	Errata	refer to
GTM-IP-104	Title : DPLL: Wrong direction decision when 24bit TBU wrap around occurs between active slope and following inactive slope Scope : DPLL Severity : High Classification : Non-critical Effects : Direction change is wrongly announced and performed. Description : If a wraparound of the 24 bit TBU time base value assigned to DPLL occurs and this event happens after an active slope and before the following inactive slope, a wrong decision about the direction is done. TC_gtmFUNCSW_dpll_acc_fw_bw. Workaround : None	v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1

Errata-ID	Errata	refer to
GTM-IP-105	Title : DPLL: When action runs into past a wrong timestamp is delivered Scope : DPLL Severity : Low Classification : Non-critical Effects : Wrong output data for action in past. Description : When action runs into past the wrong time stamp will be the output for TSAC value. This happens if action runs into past during a direction change condition. The correct output data in this case would be the time value of the last active event on the DPLL input. When the action runs into past condition the output value will be not the latest timestamp but some older value. This is no difference compared to the correct output data because in any case when the timestamp of the DPLL output is in past an action will be executed immediately because of the fact that a value is in past. This is independent on the wrong time value. Workaround : None	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1

Errata-ID	Errata	refer to
GTM-IP-106	Title : DPLL: Wrong evaluation of action in past condition Scope : DPLL Severity : High Classification : Critical Effects : Wrong and too early action output data. The action is closed although there should be further action calculations to precise the time when the action should be taken. Description : Wrong evaluation of action in past, when the TBU has a 24bit wraparound. This means that due to this wrong behavior an action calculation is finished as "past" although the action calculation should still be active. This behavior occurs when the timestamps TSF_T8p+m) and TSF_T(p) of equations 16.11a2, 16.11a4, 16.13a2 and 16.13a4) or the time stamps TSF_T(p+m-n) and TSF_T(p-n) of equations 16.11a1, 16.11a3, 16.13a1, 16.13a3 are different above the 24 bit wraparound of the TBU_CH0 timestamp. Workaround : Possibly the timestamp fields in memories RAM1c, RAM2 could be observed and the action calculation could be disabled by setting the action enable bits to '0' when the conditions are such the timestamps are used for calculations were there is an 24bit overrun between both relevant values.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1

Errata-ID	Errata	refer to
GTM-IP-107	Title : DPLL: Wrong PVT check evaluation Scope : DPLL Severity : High Classification : Non-critical Effects : Direction decision/change too early or wrong when an unexpected missing trigger occurs before. Description : Wrong PVT check evaluation because the PVT evaluation is not skipped for two events (one increment) when unexpected missing trigger occurs before. Workaround : None	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1

Errata-ID	Errata	refer to
GTM-IP-108	Title : GTM_Top level: GTM bus bridge - not functional in synchronous mode Scope : AEI protocol in synchronous mode. Severity : High Classification : Non-critical Effects : AEI interface behaves correctly with the defined AEI protocols. But no transaction is executed inside the GTM_IP. This means no register will be written on a write transaction and no register will be read on a read transaction. The AEI interface signals will be aei_rdata=0x00000000;aei_status=0x0 on any read/write transaction. Description : The GTM bus bridge is not functional in synchronous mode if the GTM_IP configuration parameter aei_input_register_c =1 is set. Workaround : A) Only the configuration setting aei_input_register_c=0 is allowed if the GTM_IP can be configured/used in synchronous mode. B) Use asynchronous operation of GTM bus bridge from reset with async_bridge_from_reset_c=1 and aei_input_register_c=1 if it is ensured that no write to GTM_BRIDGE_MODE register will switch to synchronous mode.	v1.5.3-A1

Errata-ID	Errata	refer to
GTM-IP-110	Title : MCS: NARD(I) instruction not working properly Scope : MCS Severity : Medium Classification : Non-critical Effects : NARD(I) terminating too early. If NARD(I) terminates with SAT=0, the information that the data source has no data is not reliable. Description : It is possible that the NARD(I) instruction is terminating with SAT = 0 (unsuccessful ARU transfer), although the desired data source is ready to send data. In this case, the data source does not receive the request to send and thus no data is lost. This scenario happens in two cycles within an ARU round trip cycle. Workaround : Duplicate NARD(I) instruction as NARD R0, R1, addr JBS STA, SAT, go_on NARD R0, R1, addr go_on: ... and ensure, that the sequence above is executed as an "atomic" sequence, that is not interrupted by Software (e.g. enabling/disabling of MCS-channel).	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-111	Title : DPLL: RDT_T/S, RCDT_T/S overrun in case of big DT_T_actual and DT_S_actual values, CDT_T and CDT_S values Scope : DPLL Severity : High Classification : Critical Effects : RDT_t/s and EDT_t/s, medt_t/s values negative in sign and/or wrong in value. Therefore wrong subincrement prediction and wrong action results may happen in such cases. Description : When the calculated value of dt_t/s_actual is bigger than 0x7FFFFF, the calculation of the rdt_t/s value leads because of a sign overrun of the serial divider (due to a too small bit width) to the calculation of a negative value for rdt_t/s which leads to too big edt_t, medt_t values. This results in faulty action calculation and wrong sub-increment prediction. In the special situation actions were ended as action in past instead of further calculating new action output data. The situation forced by setting the TBU_CH0_BASE could happen in a real application when car is starting out of stop in start/stop mode. Another reason why the described situation may occur even when dt_actual is smaller than 0x7FFFFF is: When dt_actual is also quite large and/or MEDT_T/S is large and/or QDT_T/S is bigger than 1 and/or SYN_T is bigger than 1 the value CDT_TX in equation e.g. 16.5a/16.5b may become bigger than 0x7FFFFF where the value RCDT_TX/SX of e.g. equation 16.17b may overrun for the same reason. Workaround : None	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-112	Title : ATOM: On SOMC mode CPU controlled, change of compare strategy is ignored Scope : ATOM SOMC mode. Severity : Low Classification : Non-critical Effects : On a change of compare strategy, if with the new compare strategy on one channel (CCU0 or CCU1) should be enabled but was not enabled before, the new compare is not started on the newly selected compare unit CCUx. The compare unit that was enabled but should no longer be enabled, is disabled correctly. As a result, already running CCUx units may be disabled but newly chosen ones will not be enabled. Description : In ATOM SOMC mode and ARU_EN=0 (i.e. ARU is disabled), if an update of the compare strategy takes place before compare match, the change is not handled correctly. An already running compare may be canceled, but a new one on the other compare unit may not be started. E.g. on change of compare strategy from ACB[4:2]=010 to ACB[4:2]=011, the compare on CCU0 is canceled, but the compare on CCU1 is not started. Workaround : After changing compare strategy also update both compare register CM0 and CM1. To cancel a pending compare use compare strategy ACB[4:2]=111 (i.e. change ARU address, which has no effect if ARU_EN=0).To set up a new compare write after setting ACB[4:2]=111 the new desired ACB[4:2] value and update also compare register CM0 and CM1.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-113	Title : DPLL: Wrong calculation of TSAC for actions due to the misbehavior of an internal address pointer Scope : DPLL action calculation. Severity : High Classification : Critical Effects : In result of the erroneous action calculation TSAC gets an unpredictable value. The effect is caused by the value of internal registers and pointers which are not accessible via AEI interface. Therefore, there is no defined way to predict the misbehavior. Description : A DPLL internal address pointer to RAM 2 or RAM1c can have an unintended overflow and thus point to an unpredictable address inside RAM. As a result the calculated TSAC may be wrong. When the error occurs depends for different configurations on different situations and is not predictable by SW due to observation of DPLL status information. The sub increment generation is not effected. The probability to get the wrong pointer depends on the TNU/SNU value and can be estimated with 1/(2*TNU+2) or 1/(2*SNU+2) respectively. It is independent on the chosen NUTE/NUSE value. The new calculation at the next input event for the same action request does not lead to a correct address pointer. The observed variation of TSAC depends on the current and last TBU_CH0_BASE value. Workaround : Use PSAC instead of TSAC; No workaround for the TSAC calculation possible - only an error detection seems to be possible when the action is calculated redundantly with the angle difference of >= 360/(TNU+SYN_NT+1) or >= 360/(SNU+SYN_NS+1). In that case at least one of the two calculations is correct. The difference must be evaluated by software. It is also possible to predict the TSAC value by software using the PSAC value and compare it with the provided one.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-114	Title : DPLL: unintended pulse correction by MPVAL1 with first event after enabling the DPLL if PCM1 is not set Scope : DPLL pulse correction. Severity : Low Classification : Non-critical Effects : Unintended pulse correction leads to wrong TBU counter value. Description : When the MPVAL1 value is written different to zero and when the first event after enabling the DPLL is detected the pulse correction is done in any case even when the control bit PCM1 is not set. Workaround : As a workaround prevent setting the MPVAL1 value before and at the moment the DPLL is enabled until the first event is detected.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-115	Title : TIM: TGPS mode early start of operation Scope : TIM Severity : Low Classification : Non-critical Effects : Description : If the setting ISL=0,DSL=0 and TIM_MODE = 101 in register TIM[i]_CH[x]_CTRL is configured, the counting of clock events in TIM[i]_ch[x]_CNT is started as soon as the channel is enabled independent of the present input signal level. Workaround : Setup the TIM channel in a way that it is ensured that counting only starts if input signal=0. This can be achieved by the following configuration sequence: --Activate TGPS with DSL=0 WRITE TIM_CH_CTRL #TGPS -- set CNTS to 0 to prevent TIM_CNT from counting WRITE TIM_CH_CNTS h#0 -- set TIM input via IN_SRC reg to 0 WRITE TIM_IN_SRC h#9 -- enable the channel WRITE TIM_CH_CTRL #TGPS | #EN -- set TIM input via IN_SRC reg to 1 WRITE TIM_IN_SRC h#2 -- set CNTS to sampling frequency WRITE TIM_CH_CNTS h#xxx -- clear notify bit WRITE TIM_CH_NOTIFY h#1 -- switch back to TIM_CH input WRITE TIM_IN_SRC h#5	v1.5.0-A1

Errata-ID	Errata	refer to
GTM-IP-116	Title : TIM: wrong signal level in TIM ARU data, when input pulse with length of 1 system clock triggers the data capture Scope : TIM Severity : Low Classification : Non-critical Effects : Description : Independent of the selected TIM mode, a wrong ARU signal level is transferred if ARU_EN=1 and an input pulse with the length of 1 system clock triggers a TIM capture. Workaround : Ensure that pulse has length greater than 1 GTM system clock. This can be achieved by using the TIM_FLT.	v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-118	Title : DPLL: requested action not calculated Scope : DPLL Severity : High Classification : Critical Effects : A requested action is not calculated because the DPLL internal processing unit is not triggered although the input data for the action calculation was transferred via the ARU interface correctly (different to Erratum GTM-IP-52). If further requests for action calculation are placed within the same event cycle they are either not served on the ARU interface nor calculated. Description : A requested action is not calculated because the DPLL internal processing unit is not triggered although the input data for the action calculation was transferred via the ARU interface correctly (different to erratum GTM-IP-52). The faulty behavior can happen in a phase of 4 system clocks when an internal observation timeframe for new action data ends, if during that interval new action data is transferred. The action data is transferred correctly to the RAM1a memory but the action calculation is not started. The behavior was detected in an environment where multiple action calculations were requested within the same input event cycle (valid active slope on trigger/state input). If further requests for action calculation are placed within the same event cycle they are not calculated either. Because the ARU transmission cycle is 78 system clocks long for device 103, the occurrence probability can be estimated by 4/78 = 0,051. Workaround : None	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-119	Title : TIM: timeout or gpr overflow bit in TIM ARU data not set correctly Scope : TIM Severity : Low Classification : Non-critical Effects : The status information in the ARU ACB bits for indicating timeout or GPR overflow is not usable. Description : Independent of the selected TIM mode if ARU_EN=1 and the timeout unit is enabled , the ARU ACB1 (GPR overflow) bit or the ARU ACB2 (timeout) bit is not set correctly in case a TDU timeout event occurs 1 GTM system clock before a GPR update event. Workaround : Configure the TIM filter and the TIM timeout unit to operate on the same cmu_clk which must have a clock frequency lower or equal to GTM system_clk / 2. When using this configuration it is guaranteed that a timeout event will never occur 1 system clock before a GPR update event.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-120	Title : TOM/ATOM SOMP mode: center aligned PWM with 0% duty cycle not applied as expected Scope : TOM/ATOM SOMP mode. Severity : Low Classification : Non-critical Effects : If the 0% duty cycle is requested as described, first one period of 100% duty cycle is applied before the correct 0% duty cycle is applied. The erroneous period of 100% cannot be tolerated in most applications. If CM1=1 and CM1<CM0<=MAX a small pulse of only one clock period (depending on selected CMU_CLKx/FXCLKx) is generated. Description : If an (A)TOM channel is configured to reset CN0 on trigger by a preceding channel the period of this channel is defined by the value this trigger while the edges inside this period are defined by CM0 and CM1. For this configuration (usually used to create center aligned PWM) one would expect to get 0% duty cycle by setting CM0>=MAX and CM1=0 where MAX is the expected value of CN0 when trigger of preceding channel resets CN0. For this configuration, 0% duty cycle is not applied correctly. For the same (A)TOM configuration with CM1=1 and CM1<CM0<=MAX a pulse 0%< low/high pulse <100% is expected. For this configuration the pulse is not generated as expected. In general, a configuration of CM1=0 or CM1=1 causes unexpected behavior. Workaround : Avoid for configuration of CN0 reset by other channel (center aligned PWM) setting of CM1=1,0. Set up 0% duty cycle by setting CM1=2 and CM0>MAX.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-121	Title : DPLL: no calculation of subincrements due to lost trigger edge for dpll internal data processing unit when PMT request via ARU just before active trigger/state edge Scope : DPLL Severity : High Classification : Critical Effects : sub_inc generation goes wrong, loss of synchronization most probably. PMT calculation bases on last observed edge and maybe thus less accurate. A further effect is that the unit to check for missing trigger interrupt (which recognizes the new trigger edge) is not getting an update for the new timestamp to check for. As a result the missing calculation is not indicated by the missing trigger interrupt. Description : When a new input event (Trigger or State) occurs and in a short time frame before an action request (PMT) is placed at the DPLL via an ARU transfer it may happen that the input event is not recognized by the DPLL internal data processing unit. Thus the sub_inc generation is not calculated as well as the synchronization and sub increments will get lost due to the lost input event. Workaround : None	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-122	Title : SPE: on detection of bouncing, corresponding input pattern is not treated to be valid Scope : SPE Severity : High Classification : Non-critical Effects : With the detection of bouncing (setting of BIS) and erroneously ignoring the new input pattern (not updating AIP and PIP, not signaling NIPD) the SPE module stops updating of SPE_PAT_PTR and thus of updating SPE_OUT_CTRL. For restart of SPE module (i.e. automatic update of SPA_PAT_PTR) the register AIP and PIP have to be reinitialized by software. For motor control applications, a stuck of pattern pointer SPE_PAT_PTR may lead to critical stuck of commutation. Description : In case the SPE module detects a sequence of input patterns that leads to a signaling of bouncing (flag BIS), this last input pattern is not treated to be valid and thus the register AIP and PIP are not updated , no new input pattern flag is raised (NIPD) and the pattern pointer SPE_PAT_PTR is stuck at its value. Because of the missing update of the AIP and PIP register, each succeeding input pattern is, although a valid succeeding input pattern, treated to be invalid. As a result, with the input patterns following the bouncing pattern, a pattern error is signaled (flag PERR is set). Workaround : After detection of bouncing (indicated by flag/interrupt BIS in register SPE_IRQ_NOTIFY), for reenable of automatic update of SP_PAT_PTR on valid new input pattern sequence, the software has to react immediately (triggered by interrupt) and reinitialize the bit fields AIP and PIP.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-123	Title : DPLL: Wrong aei_status when DPLL RAM1b is accessed in initialization phase Scope : DPLL Severity : Low Classification : Non-critical Effects : Between end of the initialization of RAM1a and the end of initialization of RAM1b, the aei_status is "00" instead of "10" when RAM1b is accessed. Description : When the DPLL RAM1b is accessed via GTM_bridge during initialization phase, between end of the initialization of RAM1a and the end of initialization of RAM1b, the aei_status is "00" instead of "10". The initialization status of the DPLL RAM is noted correctly in register DPLL_RAM_INI. Workaround : Poll init_1b bit of register DPLL_RAM_INI before accessing RAM1b the first time after power up.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-124	Title : FIFO: Wrong aei_status returned if writing unimplemented IRQ mode to FIFO[i]_CH[x]_IRQ_MODE register Scope : FIFO Severity : Low Classification : Non-critical Effects : Wrong status is reported on GTM via bridge signal aei_status and GTM_IRQ_NOTIFY register. Description : If to register FIFO[i]_CH[x]_ IRQ_MODE is written a mode value that is not enabled by the hardware configuration (silicon vendor can define available set of IRQ modes), an aei_status of b#11 is reported/returned instead of b#10. Workaround : Write to register FIFO[i]_CH[x]_IRQ_MODE only available mode values.	v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-125	Title : DPLL: DPLL RAM read access while GTM is in HALT state is leading to misbehavior of DPLL Scope : DPLL while GTM in HALT state. Severity : High Classification : Non-critical Effects : If a DPLL read access is interrupted by a HALT state and while HALT state the DPLL RAM is accessed, the interrupted read access of DPLL is redone with a corrupted result. Depending on the interrupted read address, the sub increment generation and/or the position minus time calculation may get wrong. Description : If the DPLL is performing a read access to its RAMs (two system clock cycles per read) while the GTM is just entering the HALT state (gtm_halt input is set to '1') and the read access is interrupted by the HALT state immediately after address phase, the interrupted read access is not redone correctly if leaving the HALT state. Workaround : Don't access DPLL RAMs while GTM is in HALT state (input port gtm_halt='1'). This may make DPLL debugging much more complicated.	v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-126	Title : ATOM: on debug access (aei_debug_access=1) reading of SR0/SR1 invalidates SR0/SR1 data for ARU interface Scope : GTM in debug mode (aei_debug_access=1) and ATOM channel in SOMC mode with ARU enabled. Severity : Low Classification : Non-critical Effects : In the described case the related ATOM channel is stuck in an internal state waiting for ARU data to be read although it signals via ARU that no valid data is available. The problem can be solved by either reading SR0/SR1 register via CPU interface (software) or by a (software) reset of the channel. Description : If under the condition - ATOM channel is configured to SOMC mode, - ARU enabled, - the channel has a compare match results stored in its SR0/SR1 register and waits that this result is read via ARU, a debug read access to register SR0 or SR1 register is performed (with aei_debug_access=1), the ATOM channel cancels its write request to ARU (i.e. signal of ARU interface indicating valid data) but remains in an internal state waiting for the SR0/SR1 data to be read. As a result the ATOM channel is stuck until the register SR0 or SR1 is read via CPU or the channel is reset (software reset). Workaround : Don't read in debug mode (aei_debug_access='1') register SR0 or SR1 of ATOM channel if channel is configured to SOMC mode and ARU is enabled.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1

Errata-ID	Errata	refer to
GTM-IP-127	Title : IRQ mode single pulse: interrupt may be lost in case of entering HALT state (setting gtm_halt='1') Scope : IRQ mode 'single pulse' and GTM HALT state (gtm_halt='1'). Severity : High Classification : Non-critical Effects : In the described case the interrupt is indicated in corresponding notify register but on GTM outside this interrupt is never raised (i.e. no interrupt service routine may be called). Description : In case of an interrupt source raises an interrupt in the same clock period where gtm_halt is set to '1' (i.e. the HALT state is entered) and the SYS_CLK is stopped, the interrupt notify flag in the corresponding register is set but after leaving the HALT state the interrupt pulse is not generated on interrupt line of GTM. The interrupt is lost for interrupt service routine. In general, independent of interrupt mode, currently it may be the case that the interrupt NOTIFY is set in the same cycle as gtm_halt is set but the interrupt is signaled on an out port of GTM after leaving HALT state. The behavior one could expect for all interrupt modes is that the notify flag is set only if the interrupt line indicates it on the out port of GTM. The interrupt clear request on GTM input port is executed in any case, independent of gtm_halt state. Note, the setting of an interrupt has higher priority than clearing an interrupt if the requests are raised at the same point in time. Workaround : Avoid using of single pulse mode for interrupts if debugging GTM (setting GTM to HALT state).	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1

Errata-ID	Errata	refer to
GTM-IP-128	Title : GTM_Top level: AEI pipeline bus transactions before and after a write to BRIDGE_MODE register might be serviced incorrectly Scope : AEI pipelined protocol. Severity : Low Classification : Non-critical Effects : a) Read access to the GTM responds with unexpected data. b) Write access to the GTM is not performed. Description : The bus transaction before and after a write transaction to the BRIDGE_MODE register with BRG_RST=1 (Bridge soft reset), can be serviced incorrectly. Workaround : Workaround : Ensure that the write command to the BRIDGE_MODE register is issued while the transaction buffer is empty (aei_free_buffer_cnt =buffer_depth_c). This condition cannot be controlled/observed by the hardware which means, it must be guaranteed by software e.g. a loop which ensures that dependent on the aei_clk/sys_clk ratio a certain amount of clocks will pass before the next command is issued. This will guarantee that the Bridge soft reset is executed while no other transaction is in service by the transaction buffer. The same has to be ensured for the command which follows directly after the BRIDGE_MODE access.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1

Errata-ID	Errata	refer to
GTM-IP-129	Title : GTM_Top level: AEI split bus transactions before and after a write to BRIDGE_MODE register might be serviced incorrectly Scope : AEI split protocol. Severity : Low Classification : Non-critical Effects : a) Read access to the GTM responds with unexpected data. b) Write access to the GTM is not performed. c) GTM Bus interface does not issue aei_response_ready which could lead to bus timeout of the serving bus master. Description : The bus transaction before and after a write transaction to the BRIDGE_MODE register with BRG_RST=1 (Bridge soft reset), can be serviced incorrectly. Workaround : Workaround : Ensure that the write command to the BRIDGE_MODE register is issued while the transaction buffer is empty (aei_free_buffer_cnt =buffer_depth_c). This condition cannot be controlled/observed by the hardware which means, it must be guaranteed by software e.g. a loop which ensures that dependent on the aei_clk/sys_clk ratio a certain amount of clocks will pass before the next command is issued. This will guarantee that the Bridge soft reset is executed while no other transaction is in service by the transaction buffer. The same has to be ensured for the command which follows directly after the BRIDGE_MODE access.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1

Errata-ID	Errata	refer to
GTM-IP-130	Title : GTM_Top level: AEI standard/back2back bus transactions before and after a write to BRIDGE_MODE register might be serviced incorrectly Scope : AEI standard/back2back protocol. Severity : Low Classification : Non-critical Effects : a) Read access to the GTM responds with unexpected data. b) Write access to the GTM is not performed. Description : The bus transaction before and after a write transaction to the BRIDGE_MODE register with BRG_RST=1 (Bridge soft reset), can be serviced incorrectly. Workaround : Workaround : Ensure that the write command to the BRIDGE_MODE register is issued while the transaction buffer is empty (aei_free_buffer_cnt =buffer_depth_c). This condition cannot be controlled/observed by the hardware which means, it must be guaranteed by software e.g. a loop which ensures that dependent on the aei_clk/sys_clk ratio a certain amount of clocks will pass before the next command is issued. This will guarantee that the Bridge soft reset is executed while no other transaction is in service by the transaction buffer. The same has to be ensured for the command which follows directly after the BRIDGE_MODE access.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2

Errata-ID	Errata	refer to
GTM-IP-131	Title : GTM-IP hardware configuration insert_dft_testreg_c = 0 causes problems on access to GTM top level register Scope : GTM-IP hardware configuration insert_dft_testreg_c = 0. Severity : High Classification : Critical Effects : If the hardware configuration insert_dft_testreg_c = 0 is chosen, a write access to any of GTM top level register could affect any or multiple writable register of the GTM top level register. As a result the effect is not predicable. E.g. it may be not possible to disable RF_PROT and to reset GTM. The unpredictable modification of register GTM_BRIDGE_MODE of GTM_TIM[i]_AUX_IN_SRC in case of write access may lead to undesired behavior of GTM. Description : In case of a hardware configuration insert_dft_testreg_c = 0, depending on synthesis tool, a read or write access to one of the GTM top level register (GTM_REV, GTM_RST,.., GTM_TIM[i]_AUX_IN_SRC) may lead to parallel access to all top level register. As result, reading one of the top level register returns a combinational signals of all register, writing to one of the top level register leads to writing to all of writable top level register. If synthesis tool sets uninitialized signals to '0', the implementation should be correct (i.e. this faulty behavior is not present). Workaround : Avoid writing to GTM top level register to keep their reset values.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1

Errata-ID	Errata	refer to
GTM-IP-132	Title : GTM_TOP level: AEI write to BRIDGE_MODE register can result in blocking of AEI configuration interface Scope : all AEI protocols. Severity : Low Classification : Non-critical Effects : GTM Bus interface does not issue aei_ready/aei_response_ready which could lead to bus timeout of the serving bus master. Description : If the GTM bus bridge operates in MSK_WR_RESP=1 mode, a requested change of the GTM_IP bridge mode (Bit BRG_MODE) can result in blocking of the bus interface. Workaround : Workaround : Ensure that the write command to the BRIDGE_MODE register bit BRG_MODE which switches the mode of the bridge (ASYNC/SYNC) is assigned only when in addition the Bit BRG_RST is set to '1'.	v1.5.4-A2 v1.5.4-A3 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-133	Title : DPLL: RAM 1 b+c initialization outside used address range Scope : DPLL RAM initialization. Severity : Low Classification : Non-critical Effects : If at RAM 1 b+c port a memory protection unit checks for illegal RAM address accesses, the DPLL RAM initialization would cause an illegal access error. Description : The DPLL needs for RAM 1 b+c 384 words with 24 bit width. As a result, during initialization of RAM, only 384 words needs to be accessed. The address range would be at RAM 1 b+c port from 0 to 17Fh (word addresses) while with the provided 9 address lines at RAM 1 b+c port a range of 512 words could be accessed in theory. Erroneously, the DPLL tries to access 181 word, i.e. at RAM 1 b+c port the addresses 0 to 180h are accessed. Note, it can be hardware configured by silicon vendor if after reset a DPLL RAM initialization is started. Workaround : It has to be ensured by hardware or software that before initialization of DPLL RAM a potential check of illegal RAM address accesses is disabled.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3

Errata-ID	Errata	refer to
GTM-IP-134	Title : (A)TOM: trigger chain between instances works only under special conditions Scope : TOM / ATOM SMOP/SOMC mode. Severity : Medium Classification : Non-critical Effects : If there is a register in trigger chain between (A)TOM instance i and instance i+1, a channel x of (A)TOM instance i+1 cannot react on a trigger out of (A)TOM instance i. The trigger will only be recognized if the triggered channel is running with SYS_CLK (the clock before fractional divider of CMU). Description : The trigger signal between (A)TOM instances (e.g. signal TOM_TRIG_[i]) can be registered and with this delayed by one SYS_CLK period to break long combinational path. The silicon vendor can define it by hardware configuration if there is a register to break the combinational path. It can be configured to be after each instance, after each second, after each third, ... (see microcontroller specification of silicon vendor). If there is a register in the this trigger path between (A)TOM instance i and the succeeding (A)TOM instance i+1, this trigger is only recognized by a channel of instance i+1 if the channel of instance i+1 that should react on the trigger is running with SYS_CLK period (i.e. the selected CMU_FXCLKx / CMU_CLKx period is identical to SYS_CLK period). If a lower frequency is chosen to clock the channel of instance i+1, the trigger is not recognizable by a channel of instance i+1. Workaround : If there is a register in trigger path between (A)TOM instance i and (A)TOM instance i+1, the channel of instance i+1 that should be triggered has to use a clock of period identical to SYS_CLK period. A second workaround could be to set up on instance i+1 a redundant channel to trigger other channel of instance i+1 like it was set up on instance i to trigger other channel. Then, start both instances synchronously by using the TBU time base comparator of AGC/TGCx unit (i.e. the ATOM[i]_AGC_ATC_TB / TOM[i]_TGC[y]_ACT_TB register).	v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2

Errata-ID	Errata	refer to
GTM-IP-135	Title : TIM: Bad ACB word in the case of timeout detection Scope : TIM timeout detection in combination with ARU transfers. Severity : Medium Classification : Non-critical Effects : The ARU connected data sink of the TIM channel will detect a valid measurement cycle after a timeout event although only a timeout event occurred. Description : If the timeout detection unit (TDU) of a TIM channel is enabled and the ARU routing for this channel is enabled the ACB bits of the ARU data may signalize a timeout detection with subsequent valid measurement cycle (ACB2=1 and ACB1=1) although no measurement cycle has finished at all (e.g. no signal change at the input port). This always happens if two or more successive timeout events occur without any ARU read access from the TIM's data sink (e.g. MCS channel or FIFO channel). Workaround : In order to reliably detect that a measurement cycle finished after a timeout, the application should additionally route the edge counter via ARU. Whenever the ARU destination detects a transfer with ACB2=1 and ACB1=1 and the edge counter did not change since the last ARU transfer, the received ARU word should be treated as normal timeout event (ACB2=1 and ACB1=0). Otherwise, it could be interpreted as true timeout with subsequent valid measurement cycle. This workaround can be applied directly in the MCS if the MCS is used as data destination. If FIFO is used as data destination, the workaround has to be implemented by SW.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3

GTM-IP-136	Title : (A)TOM: wrong output signal in case of PWM with CM0=0 on triggered channel (RST_CCU0=1) Scope : TOM, ATOM SOMP mode. Severity : Low Classification : Non-critical Effects : For the configuration RST_CCU0=1 and (CM0=0, CM0<CM1) no edge is generated at all. (CM0=1 covered by GTM-IP-380.) Description : In the specification up to version v1.5.4 following statement can be found in chapter 11.3 TOM Channel: "The configuration of CM1=0 represents 0% duty cycle at the output, the configuration of CM1 >= CM0 represents 100% duty cycle. If both registers are configured to 0 (CM0=CM1=0), the output is 0% duty cycle." For ATOM SOMP mode the similar statement could be assumed to be valid. If the counter CN0 of a channel x is reset by its own comparator (bit RST_CCU0 of register TOM[i]_CH[x]_CTRL/ATOM[i]_CH[x]_CTRL is not set), i.e. if CN0>= CM0, the statement is valid. If counter CN0 is reset by the trigger of a preceding channel (bit RST_CCU0 of register TOM[i]_CH[x]_CTRL/ATOM[i]_CH[x]_CTRL is set) the statement is not valid. Under the assumption that the channel y that resets CN0 of channel x (if RST_CCU0=1 on channel x) counts from CN0=0 to CN0=MAX one can expect the following behavior on channel x: 1) The counter CN0 of channel x counts from 0 to MAX like the counter of triggering channel y. The resulting period on channel x is MAX+1. 2) If SL=1, CM0 defines the rising edge, CM1 the falling edge. If SL=0, it is vice versa. 3) If CM0<=MAX+1, CM1<=MAX+1 and CM0!=CM1, CM0 and CM1 are defining together two independent edges inside the period of CN0 counting from 0 to MAX. 4) If CM0=0 and CM1=MAX+1 the output is 100% dc 5) If CM0=CM1<=MAX+1 the output is 100% SL 6) If CM1=0 and CM0>MAX+1 the output is 0% SL The erroneous behavior that can be observed is: - CM0=0, no edge is generated at all, counter CN0 is not running - CM0=1 covered by GTM-IP-380.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3

Errata-ID	Errata	refer to
	Workaround : Instead of configuration CM0=0 and CM1>0 use the configuration CM1=0 and CM0>CM1 and invert value of SL bit. Note: The behavior in case of CM0=0 was excluded from specification As a result following behavior is described in specification v1.5.5.x: If the counter register CN0 of channel x is reset by the trigger signal coming from another channel or the assigned TIM module (configured by RST_CCU0=1), following statements are valid: - CM0 defines the edge to SL value, CM1 defines the edge to !SL value. - if CM0=CM1, the output is 100% SL (CM0 has higher priority). - if CM0=0, the output stays at its last value (CN0 stops counting).	

Errata-ID	Errata	refer to

GTM-IP-137	Title :
	MCS: AEI related MCS Disabling
	
	Scope :
	MCS
	
	Severity :
	Low
	
	Classification :
	Non-critical
	
	Effects :
	The MCS channel is still running although CPU requested a disabling of the channel.
	
	Description :
	Whenever an MCS channel is being disabled by CPU via AEI, it is possible that the disabling request is ignored by the MCS channel.
	
	Workaround :
	Repeat clearing the EN bit of the register MCS[i]_CH[x]_CTRL in a loop until it is cleared. For example:
	
	do
	MCS[i]_CH[x]_CTRL = 0x0;
	MCS[i]_RST = 1 << (x + 8); // set CAT
	MCS[i]_RST = 1 << (x + 16); // set CWT
	while (MCS[i]_CH[x]_CTRL & 0x1)
	
	It should be noted that this could take the whole duration of an ARU round trip time (if an ARU transfer is currently running) or the duration of a WURM suspension time (if currently a WURM is suspended).
		v1.3
		v1.4.0
		v1.4.2
		v1.4.4-11
		v1.5.0-A0
		v1.5.0-A1
		v1.5.1-A1
		v1.5.2-A1
		v1.5.2-A2
		v1.5.3-A1
		v1.5.3-A2
		v1.5.4-A1
		v1.5.4-A2
		v1.5.4-A3

Errata-ID	Errata	refer to
GTM-IP-138	Title : DPLL: Wrong PSTC/PSSC value after initialization and restart. Scope : DPLL Severity : Low Classification : Non-critical Effects : First calculations of actions are wrong. Description : After initialization when ftd=0 (first trigger detected) the PSTC value should be set equal to PSTM. This is not done so far. The PSTC value is not initialized with PSTM value on 1st TRIGGER edge. When FTD is set to 1, PSTC is not updated with PSTM value. After each stop and restart, PSTC continues counting without any synchronization with current position. Workaround : Write PSTC/PSSC via CPU.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3

Errata-ID	Errata	refer to
GTM-IP-139	Title : ATOM SOMC mode: forced update does not activate comparison Scope : ATOM SOMC mode. Severity : Low Classification : Non-critical Effects : In the described case, the ARU read request is canceled but no new comparison with new CMx register values is activated. The system may stick in waiting for late update event to happen. The ACBO bits are erroneously not cleared. Description : Under following configuration: -ATOM SOMC mode, -ARU_EN=1, -no comparison active (bit DV in register ATOM[i]_CH[x]_STAT = 0) If in this case a late update is tried by first setting WR_REQ (see register ATOM[i]_CH[x]_CTRL), then updating SRx register and maybe ACB control bits in register ATOM[i]_CH[x]_CTRL and finally updating the CMx register via a forced update, the register CMx are updated correctly but no new comparison is activated. The ACBO bits are erroneously not cleared. The ARU read request is canceled because of WR_REQ=1. Workaround : After the forced update write additionally by CPU the new desired value of CM0 or CM1 to corresponding work register CM0 or CM1 to activate comparison and to reset ACBO bits.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-140	Title : ATOM SOMC mode: a write access to ATOM_CH_CTRL sets WRF if CCU0 compare match already occurred but CCU1 compare match open Scope : ATOM SOMC mode. Severity : Low Classification : Non-critical Effects : In the described case the WRF flag may be set erroneously. Description : Under following configuration: -ATOM SOMC mode, -ARU_EN=1 For compare strategy 'serve last', if after CCU0 compare match and before CCCU1 compare match the shadow registers ATOM_CH_SR0/1 are written out a write access to register ATOM_CH_CTRL is done, WRF bit is set independent of written bit WR_REQ. Workaround : If ATOM[i]_CH[x]_CTRL is written without the intention to set WR_REQ while there may be a comparison active on this channel x, reset afterwards erroneously set WRF flag by writing a '1' to WRF bit of register ATOM[i]_CH[x]_STAT.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-141	Title : TIM: Incorrect data captured to GPR registers and routed via ARU when EGPRi_SEL,GPRi_SEL= 100 in TIM channel mode TIEM, TPWM, TIPM, TPIM, TGPS Scope : TIM Severity : Low Classification : Non-critical Effects : a) Inconsistency of ARU signal level bit and bit[0] of ARU word which shows the captured ECNT. b) Reading of TIM[i]_CH[x]_GPRi shows inconsistency when comparing bits [31:24] to [7:0]. At the point in time of capture event the bits [31:24] contain the correct value and are subject to be changed with new incoming edge. Description : In case of a TIM channel capture event issued by a rising edge at TIM[i]_CH[x]_FOUT the capturing of the TIM[i]_CH[x]_ECNT register to the TIM[i]_CH[x]_GPRi register is incorrect. The captured value will be ECNT+2; bit 0 (signal level) will be 0. The correct operation would be to capture ECNT+1; bit 1 (signal level) would be 1. Workaround : a) When using captured ECNT data via ARU routing the correct edge count data can be reconstructed by: IF ARU_SIGNAL_LEVEL ==1 AND ARU_DATA[0] == 0 THEN ARU_DATA = ARU_DATA -1; b) When reading TIM[i]_CH[x]_GPRi by configuration interface the data can be corrected as long as there is no GPR overflow and no new edge by: IF TIM[i]_CH[x]_GPRi[24] == 1 AND TIM[i]_CH[x]_GPRi[0] == 0 THEN TIM[i]_CH[x]_GPRi[23:0] = TIM[i]_CH[x]_GPRi[23:0] -1.	v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-142	Title : TIM: Incorrect data captured to GPR registers and routed via ARU when EGPRi_SEL,GPRi_SEL= 100 in TIM channel mode TBCM Scope : TIM Severity : Low Classification : Non-critical Effects : a) In 2 following ARU transfers the ARU word which shows the captured ECNT do not increment by 1. b) Reading of TIM[i]_CH[x]_GPRi shows inconsistency between [31:24] and [7:0]. Description : In case of a TIM channel capture event issued by a input pattern match to condition TIM[i]_CH[x]_CNTS the capturing of the TIM[i]_CH[x]_ECNT register to the TIM[i]_CH[x]_GPRi register can be incorrect. Starting at t=0 with counter value ECNT(t=0), the captured values of two consecutive edges can be ECNT(t=0)+2 followed by ECNT(t=0)+2 instead of ECNT(t=0)+1 followed by ECNT(t=0)+2. Workaround : a) Ignore captured ECNT data via ARU and build with MCS independent counter which increments on each ARU transfer. b) When reading TIM[i]_CH[x]_GPRi by configuration interface use only TIM[i]_CH[x]_GPRi[31:24] as EDGE counter; don't use TIM[i]_CH[x]_GPRi[23:0].	v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-143	Title : GTM_TOP level: AEI pipelined write to GTM_BRIDGE_MODE register directly after setting aei_reset='0' can result in blocking of AEI configuration interface Scope : AEI pipelined protocol. Severity : Low Classification : Non-critical Effects : GTM Bus interface does not issue aei_ready which could lead to bus timeout of the serving bus master. Description : If the GTM bus bridge is reset with aei_reset= '0' and the next AEI transfer is a write command to GTM_BRIDGE_MODE register the AEI configuration interface can be blocked. Workaround : Ensure that after setting aei_reset to inactive state the next command must be a read to any other register except GTM_BRIDGE_MODE. Issue desired write to GTM_BRIDGE_MODE register afterwards.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-144	Title : TIM: TIM interrupts as trigger source from TIM to TOM/ATOM not functional Scope : TIM Severity : Medium Classification : Non-critical Effects : The selection of an interrupt of TIM channel x+1 by EXT_CAP_SRCx(2:0) = 000, 010,100,101,110,111 to trigger corresponding TOM/ATOM channel leads to erroneous trigger behavior. As a result the TOM/ATOM does not react on the intended interrupt. Description : According to specification one could select with the configuration bits EXT_CAP_SRCx(2:0) of register TIM[i]_CH[x]_ECTRL one of six TIM channel x+1 interrupts as a source for signal TIM_EXT_CAPTURE(x). The signal is used internally in TIM channel x and forwarded to a corresponding ATOM/TOM channel . For the signal path TIM_EXT_CAPTURE(x) which is forwarded to ATOM/TOM the selection is incorrect for the values of EXT_CAP_SRCx(2:0) = 000, 010,100,101,110,111. Only the selection of TIM_IN(x-1), TIM_IN(x) or AUX_IN(x) is possible with the values EXT_CAP_SRCx(2:0) = 001 or 011. For the signal path TIM_EXT_CAPTURE(x) which is used inside TIM channel x, the selection works as specified. Workaround : None. Do not use the configuration EXT_CAP_SRCx(2:0) = 000, 010,100,101,110,111.	v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-145	Title : MCS: Unexpected Memory Overflow. Scope : MCS Severity : Medium Classification : Non-critical Effects : The MCS program will be halted after executing an instruction in the described memory region while a scheduling mode with instruction prefetching is used. Description : If the last 3 memory locations of the upper MCS RAM contain any machine code, the MCS causes a memory overflow during the execution of such an instruction in the case that the selected scheduling mode supports instruction prefetching (e.g. Accelerated Mode, Single Prioritization Mode, or Multiple Prioritization Mode). Workaround : Do not put executable MCS machine in the last 3 memory locations of the upper MCS RAM or use the Round Robin Scheduler.	v2.1.1-A1

Errata-ID	Errata	refer to
GTM-IP-146	Title : ATOM SOMC mode: compare match does not clear WR_REQ Scope : ATOM SOMC mode. Severity : Low Classification : Non-critical Effects : In the described case the bit WR_REQ is not reset. As a result no new ARU read request is set up after final compare match. Description : If an ATOM channel is operating in SOMC mode, ARU is enabled and, initiated by setting WR_REQ=1, a late update of CM0/CM1 register and/or compare strategy (i.e. ACB[4..0]) was successfully done, then, after final compare match the WR_REQ bit should be reset. This is erroneously not done. Workaround : Reset WR_REQ by software after late update (after forced update).	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1

Errata-ID	Errata	refer to
GTM-IP-147	Title : MCS: Unexpected WURM latency. Scope : MCS Severity : Medium Classification : Non-critical Effects : Unexpected program execution time. Description : According to the specification, the WURM latency (time between WURM match event and begin of execution of succeeding instruction) should be 2 + NPS (7) clock cycles. However the actual WURM latency is 1+2*NPS (11) clock cycles. Workaround : None	v2.1.1-A1

Errata-ID	Errata	refer to
GTM-IP-150	Title : TIM: Valid edge after Timeout Scope : TIM timeout detection in combination with ARU transfers. Severity : Medium Classification : Non-critical Effects : If a valid edge occurs after a timeout event, the valid edge is not signalized reliably via the ACB bits over the ARU. Description : Assume that a TIM timeout event triggers an ARU write request with timeout information ACB2=1 and ACB1=0. If this request is acknowledged by the ARU while a new valid edge occurs, the valid edge is neither signalized by setting the bits ACB2=1 and ACB1=1 within the acknowledged transfer nor by setting up a new subsequent ARU write request for the new valid edge with ACB2=0 and ACB1=0. Workaround : The workaround for this issue requires an additional plausibility check within the MCS or CPU via FIFO: 1) Always store the received data ARUDATA(47:0)n and ACB0n in temporary variables. 2) If an ARU transfer with ACB2n+1=1 and ACB1n+1=0 is received also check the following: If ACB0n+1 != ACB0n OR ARUDATA(47:0)n+1 != ARUDATA(47:0)n then a timeout with subsequent valid edge has occurred, which means ACB1 must be corrected to 1.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1

Errata-ID	Errata	refer to
GTM-IP-151	Title : DPLL: Wrong storage of TSF_T, TSF_S in RAM2 or RAM1c Scope : DPLL storage of timestamp data of TRIGGER and STATE processing unit. Severity : Medium Classification : Non-critical Effects : The TSF_T/S data when used out of the RAM may be corrupted and all calculations following from that. This can happen if the TSF_T/S data of a gap is stored in the range of the wraparound of the apt_2b, aps_1c2 pointers. The TSF_T/S data are used for calculation of the prediction and for action calculation. Description : The TSF_T/S data when written to the RAM may be corrupted and all calculations following from that as well if the TSF_T/S data of a gap are stored in the range of the wraparound of the apt_2b, aps_1c2 pointers. Workaround : Modify the pointer apt_2b after resynchronization such that the wraparound of the TSF_T/S data fields does not contain timestamp data of a gap. As well the profile should be defined that under start conditions (apt_2b = 0) the wraparound of the timestamp data fields TSF_T, TSF_S is not within the range of the wraparound of the pointer apt_2b, aps_1c2.	v1.3 v1.4.0 v1.4.2 v1.4.4-11

Errata-ID	Errata	refer to
GTM-IP-152	Title : DPLL: THVAL value not immediately available at inactive trigger slope Scope : DPLL storage of value THVAL into memory. Severity : Low Classification : Non-critical Effects : The value THVAL is not available in the memory at the specified point in time. Description : According to the specification chapter 16.8.6.7 it is specified that "for each invalid trigger slope....store this value to THVAL". The value THVAL is calculated correctly but this value is stored into the THVAL memory location with every new active edge of the trigger signal. Workaround : If the THVAL value is needed immediately with the inactive trigger edge it is necessary to calculate the THVAL value by an TIM_CHO/1 to obtain the active and inactive slopes in input event mode. With this timestamps the CPU is able to calculate the time span within the CPU.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-153	Title : TIM: Incorrect data captured to CNTS register when TIM channel operates in mode TPWM or TPIM and CNTS_SEL = 1 and selected CMU_CLK != sys_clk Scope : TIM Severity : Low Classification : Non-critical Effects : Unexpected values in CNTS_REG. Description : In case of CNTS_SEL = 1 and TIM_MODE = TPWM or TPIM in the CNTS_REG register the value of TBU_TS0 shall be captured. This does not happen when the selected CMU_CLK != sys_clk. Workaround : Setup the TIM channel to operate on a CMU_CLK (Divider =1) which is identical to sys_clk. Please notice that the measurement with TIM_CNT has resolution of sys_clk.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1

Errata-ID	Errata	refer to
GTM-IP-154	Title : TOM : Incorrect duty cycle in PCM mode (bit reversed mode) Scope : TOM Severity : Low Classification : Non-critical Effects : Unexpected duty cycle in PCM mode. Description : The generated duty cycle on the TOM output in PCM mode is always one smaller than the configured value in the CM1 register. So if the value 1 is configured, a duty cycle of 0 % will be generated. Configuring the max value (0xFFFF) in the CM1 register results in a duty cycle of max-1. Expected is 100 % duty cycle in this case. A zero in CM1 register results in 100 % duty cycle. Workaround : Configure always the value for the expected duty cycle in the CM1 register with expected duty cycle + 1. To get 0 % duty cycle, value 1 has to be configured . To get 100 % duty cycle, 0 has to be configured to CM1 register while CM0 is always configured with max. value of 0xFFFF. Configuring CM0=0x1000 and CM1 = 0xFFFF will also get a duty cycle of 100 %.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-155	Title : CMP : Incorrect AEI status by writing 1 to bits 11:23 to register CMP_EN, CMP_IRQ_NOTIFY, CMP_IRQ_EN, CMP_IRQ_FORCINT, CMP_EIRQ_EN Scope : CMP: GTM device configurations without TOM instances. Severity : Low Classification : Non-critical Effects : No functional influence to specified GTM. After writing a 1 to bits 11 to 23 of register CMP_EN, CMP_IRQ_EN, CMP_EIRQ_EN, a 1 is read back from these register bits. Writing a 1 to one of the bits 11 to 23 of register CMP_EN, CMP_IRQ_NOTIFY, CMP_IRQ_EN, CMP_IRQ_FORCINT, CMP_EIRQ_EN leads to AEI status 0. Description : In the register CMP_EN, CMP_IRQ_NOTIFY, CMP_IRQ_EN, CMP_IRQ_FORCINT, CMP_EIRQ_EN the bits 11 to 23 are read and writable by AEI bus. The AEI status in case of writing a '1' to bits 11 to 23 should be 2 but is erroneously 0. Setting the bits 11 to 23 in the register CMP_EN, CMP_IRQ_NOTIFY, CMP_IRQ_EN, CMP_IRQ_FORCINT, CMP_EIRQ_EN to '1' should also be not possible. Workaround : Do not write 1 to bits 11 to 23 of register CMP_EN, CMP_IRQ_NOTIFY, CMP_IRQ_EN, CMP_IRQ_FORCINT, CMP_EIRQ_EN.	v2.1.1-A1

Errata-ID	Errata	refer to
GTM-IP-156	Title : CMP : Pointless ABWC10 feature Scope : CMP Severity : Low Classification : Non-critical Effects : If ABWC comparator 10 is enabled every signal level 1 of ATOM2_OUT4 generates a compare error (i.e. sets error indication for ABWC10). Description : According to specification v2.1.1.0 in ABWC comparator 10 a bitwise compare of DTMA Bit Number One=20 (i.e. ATOM2_OUT4) against DTMA Bit Number Two=21 (open because ATOM2_OUT5 does not exist) is done. As a result a compare against '0' is done which leads to a compare error if ATOM2_OUT4 is 1. This comparison doesn't make sense because the second inputs is open. The specification has to be adapted, too. Workaround : Do not enable ABWC comparator 10 (bit ABWC10_EN in register CMP_EN).	v2.1.1-A1

Errata-ID	Errata	refer to
GTM-IP-157	Title : CMU : Incorrect aei status by writing 1 to bit 24 of register CMU_CLK_6/7_CTRL Scope : CMU: GTM device configurations without DPLL. Severity : Low Classification : Non-critical Effects : No functional influence to specified GTM. After writing a 1 to bit 24 of register CMU_CLK_6_CTRL or CMU_CLK_7_CTRL, a 1 is read back from this register bit. Writing a 1 to bit 24 of register CMU_CLK_6_CTRL or CMU_CLK_7_CTRL leads to AEI status 0. Description : If according to GTM device configuration no DPLL is available, bit 24 of register CMU_CLK_6_CTRL and CMU_CLK_7_CTRL is reserved. Erroneously, writing a '1' to bit 24 is possible and leads to AEI status 0. Workaround : Do not write 1 to bit 24 of register CMU_CLK_6/7_CTRL.	v2.0.2-A1 v2.1.1-A1

Errata-ID	Errata	refer to
GTM-IP-158	Title : DPLL: Reset of pcm1/pcm2 bits in relation to an interrupt. Scope : DPLL Severity : Low Classification : Non-critical Effects : When the PCM1/2 bits are written in the critical timeframe the bits are cleared before they are used. Description : The PCM1/2 bits are reset after the correction values MPVAL1/2 are used to calculate the number of sub_incs for the next increment and to calculate the add_in values. See specification chapter 16.8.6.7 (States 5, 25). The problem is that the PCM1 bit is transferred with an active edge into the dedicated shadow registers, but cleared sometime later. If the PCM1/2 bits are written by the CPU in between the point of time of the transfer to the shadow register and the point of time were the PCM1/2 bits are cleared, the bits are cleared and never used. This is not what one should expect from a properly defined user interface and to prevent additional expenditure to calculate the correct point of time for writing the PCM1/2 bits. From application point of view the desired behavior is that the PCM1/2 bits are cleared when transferred to their shadow registers (not in state 5, 25). The proposed workaround would fit to this described modification. Workaround : The point of time when the PCM1/2 bits are written by the CPU must be around 750 system clocks after the TASI interrupt. This time could be derived by a GTM resource like an ATOM channel.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-159	Title : ATOM SOMB mode: writing to CM0/CM1 marks them as valid independent of compare strategy Scope : ATOM SOMB mode. Severity : Low Classification : Non-critical Effects : In the described case the ATOM channel sticks in a state where no update of CM0/CM1 register with content of SR0/SR1 register (received via ARU) will take place. Description : In case of ATOM SOMB mode enabled and ARU transfer enabled (ARU_EN=1) a writing to CM0/CM1 marks these values to be valid and activates the compare with the compare strategy given by current value received via ARU (i.e. given by bit field ACBI which was updated with value from ACB_SR because ARU_EN=1). If there was no ARU data received after channel enable, the initial ACBI value '000' is used. This value means 'do nothing'. The erroneous behavior is that although the compare strategy is 'do nothing' the written CM0/CM1 values are treated to be valid and block further update of CM0/CM1 register. The channel sticks in this state. The same erroneous behavior can be expected with compare strategy '001' and '111'. Workaround : If ATOM SOMB mode enabled and ARU_EN=1, don't write directly to CM0/CM1 register.	v2.1.1-A1

Errata-ID	Errata	refer to
GTM-IP-160	Title : ATOM SOMB mode: cancel of compare via forced update and compare strategy '111' blocks further update via ARU Scope : ATOM SOMB mode. Severity : Low Classification : Non-critical Effects : In the described case the ATOM channel sticks in a state where no update of CM0/CM1 register with content of SR0/SR1 register (received via ARU) will take place. Description : If an ATOM channel has received valid data via ARU and a compare is running, a forced update with WR_REQ=1 and ACB[4..2]='111' only cancels running compare but marks updated CM0/CM1 register content to be valid. This blocks further update of CM0/CM1 register via ARU. Workaround : After first forced update with ACB[4..2]='111' do a second one with SR0/SR1 values in the past and ACB[4..0]='01000' if at least TBU_TS0 is enabled and ACB[4..0]='01100' if only TBU_TS1 is enabled. This second forced update leads to an immediate compare match (because SR0/SR1 in the past) with no change at the output (because ACB[1..0]='00').	v2.1.1-A1

Errata-ID	Errata	refer to
GTM-IP-161	Title : DPLL MTI/TORI-IRQ's are not activated when low_res='1' and ts0_hrt='1'; MSI/SORI-IRQ's are not activated when low_res='1' and ts0_hrs='1' Scope : DPLL in mode low_res='1' and tso_hrt='1' ts0_hrs='1'. Severity : Medium Classification : Critical Effects : When this effect is activated by the configuration and when the upper tbu_ts0 bits are not equal to "000" the interrupts MTI/TORI or MSI/SORI are not activated. A consequence of this is that the lock1/2 bits and the MTI/MSI flags in the DPLL_STATUS register are not operating correctly. Description : The DPLL Interrupts MTI/TORI are not raised when the DPLL is configured with low_res='1' and ts0_hrt='1' when the upper three bits of the tbu_ts0 are not equal to "000". The DPLL Interrupts MSI/SORI are not raised when the DPLL is configured with low_res='1' and ts0_hrs='1' when the upper three bits of the tbu_ts0 are not equal to "000". Workaround : Don't use the configuration low_res='1' and ts0_hrt='1'. The signals are working correctly for the configurations low_res='0' and low_res='1' and ts0_hrt/s='0'.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-162	Title : DPLL: Input signal (active edge) which is ignored by PVT-check occurring at a gap in the profile or a lost input signal causes that the MTI_IRQ is not activated. Scope : DPLL Severity : Medium Classification : Non-critical Effects : For the gap where the described situation occurs the MTI interrupt is not activated. In this moment the lock1/2 signals are unaffected. The possible problem is that in case of monitoring the DPLL synchronization e.g. with the use of the MTI_IRQ in a gap such monitoring may report a synchronization problem which is not real. A lost input signal cannot be detected because no interrupt will be generated. Description : The DPLL interrupt MTI_IRQ is not raised when: a) during a gap in the profile an active input signal edge is ignored by the PVT check. b) the input signal is getting lost after an active input signal edge is ignored by the PVT check. Workaround : The violated PVT check is reported by the activation of the PWI interrupt. This interrupt can be used to check if a gap condition in the profile or a lost input signal has occurred. This information can be used to correct the wrong information out of the DPLL.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-163	Title : TIM: timeout signaled when TDU unit is re-enabled Scope : TIM Severity : Low Classification : Non-critical Effects : Unexpected timeout event when TIM TDU is enabled. Description : In the following situation an undesired timeout event is signaled: After stopping the TDU the TO_CNT bit field will have an arbitrary value TO_CNT0 <= TOV0 bit field. Assume TOV will be reconfigured to value TOV1 with TOV1 <= TO_CNT0. If the TDU will be enabled again by writing to TOCTRL a value !=0 and at the same time the TCS selected CMU_CLK has an active edge an unintended timeout is signaled. This results due to the fact that for one clock cycle TO_CNT0 >= TOV1 . Workaround : If TDU unit has to be re-enabled with a TOV value TOV1 which is less than the previous one in use TOV0 (2 alternatives are available): A) Wait with disabling TDU until condition TOV1 > TO_CNT is fulfilled. Configure TOV with TOV1 reenable TDU Unit. B) Disable TDU; if TOV1 <= TO_CNT write TOV with 0xFF; enable TDU unit; reconfigure TOV to desired value TOV1.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-164	Title : TIM: capturing of data into TIM[i]_CH[x]_CNTS with setting CNTS_SEL=1 not functional in TPWM and TPIM mode Scope : TIM Severity : Medium Classification : Non-critical Effects : Captured data in TIM[i]_CH[x]_CNTS is not as expected. Description : If CNTS_SEL=1 is selected and a new input edge is signaled by the TIM Filter unit while the selected CMU_CLK has no rising edge the register TIM[i]_CH[x]_CNTS will capture data TIM[i]_CH[x]_CNT instead of TBU_TS0. Workaround : A) Select with CLK_SEL a CMU_CLK which is identical to SYS_CLK (clock divider applied in CMU channel and for global fractional divider). B) Use TIEM mode to capture TBU_TS0 for rising and falling input edges. C) PWM mode: Use CNTS_SEL=0 with CMU_CLK source selected as in use for TBU_TS0 counting. Capture with EGPR0_SEL=0,GPR0_SEL=0 in GPR0_REG TBU_TS0 and with EGPR1_SEL=0,GPR1_SEL= 3 in GPR1_REG CNT. Calculate the desired timestamp with GPR0_REG - GPR1_REG + CNTS_REG.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-166	Title : DPLL: The Content of registers DPLL_apt_sync.APT_2b_ext and DPLL_aps_sync.APS_1c2_ext is added independently of the state of DPLL_apt_sync.APT_2b_status or DPLL_aps_sync.APS_1c2_status to the pointers apt_2b/aps_1c2. Scope : DPLL Severity : Low Classification : Non-critical Effects : Wrong status of pointers apt_2b or aps_1c2 after synchronization has been executed. Description : If during synchronization the registers DPLL_apt_sync.APT_2b_ext and DPLL_aps_sync.APS_1c2_ext are loaded with non-zero values they are added to the pointers apt_2b/aps_1c2 independently from the status of the control bits DPLL_apt_sync.APT_2b_status or DPLL_aps_sync.APS_1c2_status. Correctly this should happen only when the control signals DPLL_apt_sync.APT_2b_status or DPLL_aps_sync.APS_1c2_status are set to "1". Workaround : If the pointers apt_2b/aps_1c2 should remain unchanged after synchronization the registers DPLL_apt_sync.APT_2b_ext and DPLL_aps_sync.APS_1c2_ext must be set to zero before synchronization is performed.	v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-167	Title : ATOM SOMP mode: for RST_CCU0=1 and ARU_EN=1, if CN0 reaches CM0 an update of the register SRx is requested Scope : ATOM SOMP mode. Severity : Medium Classification : Non-critical Effects : For the described configuration, the ATOM channel requests and updates the SR0/SR1 register not only after the update of CM0/CM1. Depending on time between CM0 of this channel and the value of CN0 in case of reset by the trigger, the SR0/SR1 register may be updated two times between two triggers to reset CN0. In case of ARU_EN=1, means the update of SR0/SR1 is requested via ARU, if CM0 is greater than the end value of CN0 before it is reset by trigger, no further update via ARU is requested because CN0 never reaches CM0. Description : For the configuration ATOM SOMP mode, ARU_EN=1, RST_CCU0=1 an update of SR0/SR1 register via ARU is requested erroneously any time CN0 reaches CM0. Because of RST_CCU0=1, if CN0 reaches CM0, CN0 is not reset but counting until it is reset be the trigger of a preceding channel. Therefore, it may not be the end of a period if CN0 reaches CM0. The expected point in time for a new ARU read request to update the shadow register SR0/SR1 would be the trigger to reset CN0 which triggers also the update of CM0/CM1 with the value of SR0/SR1. Workaround : 1) If new data via ARU is provided by FIFO, avoid for ATOM SOMP mode the combination of configuration ARU_EN=1 and RST_CCU0=1. 2) If new data is provided by MCS, ensure by MCS that only one time per period new data for SR0/SR1 register can be read. This can be reached by starting the 'master period' which triggers the reset of CN0 on a time base value and provide to the MCS the start value and the period. Then, the MCS can calculate a time for providing new ARU data.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1

GTM-IP-168	Title : DPLL: CPU read / write accesses to RAM2 in competition to DPLL accesses to RAM2 may lead to wrong SYN_T data read by DPLL Scope : DPLL Severity : High Classification : Critical Effects : DPLL TRIGGER processing unit reads out from RAM2 wrong syn_t, syn_t_old data. As a result sub increment calculations of the DPLL are wrong. This leads to loss of synchronization. Further observations are corrupted data in the TSF_T data field of RAM2 as a consequence of the desynchronization. Description : If at a dedicated point in time during sub increment calculation the DPLL TRIGGER processing unit reads a profile value out of RAM2 and in competition a second read/write operation is scheduled on the RAM2 via CPU/DMA interface, there is a dedicated state and signal constellation that leads to the effect that the RAM2 output data belonging to the CPU/DMA access is used as read data for the internal TRIGGER processing unit. This can lead to a wrong internal syn_t, syn_t_old value leading to a desynchronization of the DPLL. The desynchronization can be detected if the missing trigger interrupt (MTI-irq) is activated together with a suitable parameter TOV. Workaround : The application SW has to avoid any access (CPU or DMA) to DPLL RAM2 in the time window starting with the active TRIGGER edge and ending with the TASI interrupt. Workaround 1: Synchronization of CPU/DMA accesses to phases where DPLL is not accessing RAM2. This can be reached by synchronizing DPLL RAM2 accesses to TRIGGER signal using the TASI interrupt and checking continuously if the RAM2 access is finished before next active TRIGGER edge. As an alternative for TASI interrupt one can start with the TIM0_CH0 active edge interrupt an ATOM pulse (SOMP mode, one shot mode) of the length 200 SYS_CLK periods. With the CCU1 interrupt of the ATOM channel the critical phase of DPLL internal RAM2 accesses is finished and now the CPU/DMA can access DPLL RAM2. Workaround 2: Asynchronous CPU/DMA accesses to phases where DPLL is not accessing RAM2. This can be achieved by using MCS to calculate and set flags that indicate the uncritical phase of DPLL RAM2 accesses.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-169	Title : DPLL: no TORI/SORI interrupt in case low_res = 1 AND ts0_hrt/s = 0 Scope : DPLL Severity : Low Classification : Non-critical Effects : The TORI/SORI interrupt is not coming in that configuration. Description : If the described configuration is chosen there is no TORI/SORI interrupt raised at all. Workaround : For the configuration low_res=1 and ts0_hrt/s = 0 use TOM or ATOM to generate an interrupt on time out of TRIGGER/STATE: With every TRIGGER/STATE edge adapt (A)TOM period to current speed and reset CN0. If CN0 is not reset by next TRIGGER/STATE event, (A)TOM raises an edge interrupt at the end of the period.	v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-170	Title : DPLL: Action calculation: requested action not always calculated immediately Scope : DPLL Severity : Low Classification : Non-critical Effects : Requested actions are not calculated regularly with every tooth (as long as they are not in the past). Description : If the action calculation by DPLL was interrupted due to a new input event it may happen that with the next TRIGGER/STATE input event, after sub increment calculation is finished, the action calculation starts again at the same internal action number which has been interrupted before. If in between new action data arrives where the action number is above the currently calculated action this new action data is only calculated after the next input event. The reason for that behavior is that if action calculation was interrupted the action calculation starts with the internal action address which was stored at the end of the event cycle before. New PMT data for action with higher action number are not recognized. The action calculation stops if the action number zero is reached. Generally: The calculation of sub increments and PMT cannot be done in parallel due to resource sharing. This leads to the behavior that PMT calculation is interrupted if a new input event (TRIGGER/STATE) occurs. When DPLL is doing the action calculations the DPLL has exclusive access rights to RAM1a which contains the PMT request values. Then the DPLL cannot accept new PMT requests via ARU. Workaround : Request actions which are not "past" so far with every new tooth. The synchronization of the MCS task to TIM input event can be done by routing the TIM edge capture event value via ARU to MCS. Then, if new PMT data is arriving after the action number has reached the value zero, the action is calculated immediately starting with the highest action number again. As a workaround one can request the action calculation tooth by tooth until action runs into past. An additionally PMT request can be placed earlier after new input event (TRIGGER/STATE) while DPLL is doing sub increment calculations because then RAM1a can be handled exclusively for updating PMT requests via ARU. Generally it is recommended to send PMT requests at least 3 teeth before action has to be executed. This ensures that even under presence of the erratum the MCS, ATOM are getting calculated action results at least from a calculation of the action in an input event cycle before.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-171	Title : TIM: signal level bit in TIM ARU data not set correctly Scope : TIM Severity : Low Classification : Non-critical Effects : The signal level information in the ARU ACB0 bit is not as expected. Description : Relevant mode TIEM with ISL=1 and ARU_EN=1. In case of input signal changes with distance smaller than ARU routing time the signal level Bit ACB0 might be incorrect if overflow bit ACB1 is set. The erroneous behavior occurs, if an edge starts an ARU transfer and one system clock before the ARU request is serviced the input signal changes. In this case with ACB1=1 the overflow condition is signaled correctly, but the signal level bit ACB0 will not be updated (it will remain the previous signal level). Workaround : With MCS or with CPU the faulty ACB condition can be identified if it can be ensured that never 3 input edges occur in the range of the ARU Routing time. Next is shown a pseudo code which can be used as a workaround: Last_ACB0 = -1 Foreach ARU_DATA If ARU_DATA(ACB1) ==1 If Last_ACB0 != -1 If Last_ACB0 != ARU_DATA(ACB0) Message(Hit on ERRATA: Detected faulty state of signal level) ARU_DATA(ACB0) = Last_ACB0 else Message(No signal level present yet, cannot apply workaround) Last_ACB0 = ARU_DATA(ACB0)	v2.1.1-A1 v2.1.2-A1

Errata-ID	Errata	refer to
GTM-IP-172	Title : TIM: overflow bit in TIM ARU data not set; signal level bit in ARU data has opposite value Scope : TIM Severity : Low Classification : Non-critical Effects : The overflow information in the ARU ACB1 bit is not set, ARU ACB0 signal level incorrect. Description : Relevant mode TIEM with ISL=1 and ARU_EN=1. In case of 2 input signal changes with distance smaller than ARU routing time the overflow Bit ACB1 might not be set. The erroneous behavior occurs, if an edge (first_level) starts an ARU transfer and one system clock before the ARU request is serviced the input signal changes (! first_level). In this case the overflow bit ACB1 is not set (keeps ACB1=0), and the signal level bit ACB0 will be incorrect ACB0= first_level. Note that the irq_notify(3) bit (gpr_overflow) is set correctly. Workaround : Workaround A: Ensure with TIM filter that input signal changes smaller than ARU Routing Time will be removed. Configure FLT_FE/FLT_RE with filter delay which is greater than ARU Routing time. Workaround B: Select ECNT or CNT to be transferred in ARU_DATA. Next is shown a pseudo code which can be used as a workaround: Last_CNT = -1 Foreach ARU_DATA If ARU_DATA(ACB1) ==0 If Last_CNT != -1 If Last_CNT+1 != ARU_DATA(CNT) Message(Hit on ERRATA: Detected overflow condition) ARU_DATA(ACB1) = 1 ARU_DATA(ACB0) = not ARU_DATA(ACB0) else Message(No signal level present yet, cannot apply workaround) Last_CNT = ARU_DATA(CNT)	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-173	Title : DPLL: new PMT data not received Scope : DPLL Severity : Low Classification : Non-critical Effects : PMT result calculated on "older" PMT input data because a pending data transfer with newer input data to the DPLL cannot be executed. Description : The root cause of the problem in a dedicated constellation of time is an action calculation with the result "past" although a pending data transfer to the DPLL via ARU with new input data on the same PMT channel cannot be executed. So the data transfer of the new action data starts after the action calculation so that first the action is finished e.g. with the result past before the new input data can be used. When the DPLL receives PMT requests after a new input slope, only that requests can be considered, which are transferred during a simple ARU routing cycle. The DPLL blocks new PMT requests when there is a time of about 200 ns since the last PMT request is passed. New PMT requests are only accepted after the calculation of the pending action calculations are performed. This calculation starts in step 13 (33) of the state machine, about 10 us after the input event and ends depending on the number x of actions to be calculated x*3.7 us later. After this time a single new PMT request is accepted, but there is no possibility to stop an action calculation with an update of data. The "old" value is always calculated. Workaround : When the calculated action is transmitted to the MCS check, if there is an ARU transfer with new data of this action was blocked by the ARU, because the DPLL was not ready to receive new data within these increment. Also in the case the ARU transfer was just performed, the corresponding action contains only the "old" PMT requirements. Ignore this action value and wait for the new value which appears about 3,7 us after the PMT requirement update was transmitted. New action values relating to new PMT requests are considered in the states 18 to 20 (38 to 40) of the state machine. Typically one PMTR update is transmitted and then corresponding action is calculated until a new PMTR is accepted (when not transmitted in a block with directly succeeding ARU transmissions).	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-174	Title : DPLL: PMT result not sent to ARU Scope : DPLL Severity : Medium Classification : Non-critical Effects : The results of a PMT calculation are not transferred to their target. This can only happen if the result of the PMT is "PAST". Description : The root cause for the problem is that before reaching a dedicated state of the DPLL there is a gap in time in which the DPLL.act_n(i) bit of an action is reset before the act_n_shd_reg signal (shadow register) is set to "1" which starts the transfer of the output data via ARU. If in this gap a new input event is arriving the act_n(i) and the internal state controller changes to the processing of this new input event the signal act_n_shd(i) is not set and so there is no request for transmitting the output data to the ARU placed. This leads to the situation in which an action calculation is finished without transferring the data via the ARU. PMT calculations were the result is not "PAST" are not affected by this issue. The time frame in which an incoming input signal is causing the misbehavior is about 25 system clock cycles. Workaround : In general a workaround has to take into account that a message ending in "past" is going to have the issue when during action calculation at a dedicated point of time a new input event occurs. For the MCS program it is therefore necessary that the MCS program is reading the PMT data from DPLL via non-blocking ARU reads to prevent that the MCS program is blocked. Additionally, the MCS program should make inside the loop that is doing the non-blocking ARU reads a plausibility check if the requested action is 'out of time' or 'out of angle'. The MCS can read at any time from TBU the time base tbu_ts0 and the angle from tbu_ts1/tbu_ts2. This information should be used to determine if there is a requested action pending or out of date. If the MCS program did not get back a result in the expected time window, it could either request the old value again or, if the requested event is in the past, request a new value. Additionally the TIM0 interrupt could be routed to the MCS to check if an active edge occurred. In this case all actions which delivered a result so far must not be checked again independently if their result was "PAST" or not. If the PMT is used such that the PMT result is transferred directly from the DPLL to the ATOM, there should be a default assignment to the ATOM which is not in PAST to make sure that, even if the DPLL fails to send the PMT result to the ATOM, the ATOM is not missing an event completely.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-175	Title : DPLL: Incorrect reset behavior of internal registers if hardware reset of GTM module is implemented as "active high" by setup of parameter reset_active_c ='1' Scope : DPLL Severity : Low Classification : Non-critical Effects : Four registers within the DPLL submodule are going to stay in permanent reset if the constant reset_active_c='1' is chosen for the GTM-IP. Description : The GTM-IP provides the opportunity to implement the hardware reset either active high or active low. The behavior of the IP implementation can be adjusted by the semiconductor manufacturer via a constant ("reset_active_c") in the gtm_scale_pack.vhd. Because four internal VHDL processes of the DPLL submodules are using a hardwired active low reset, this registers will not operate correctly because this registers will be kept in reset permanently if the active high reset (reset_active_c<='1') is deactivated for normal operation. Workaround : So far no IP implementation with reset_active_c='1' is known so there is no action needed for the so far existing devices at all. New IP implementations by semiconductor manufacturer must not use the setup reset_active_c= '1' at all together with the existing versions of the GTM-IP. For newer versions the bug is going to be fixed.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1

Errata-ID	Errata	refer to
GTM-IP-176	Title : TOM/ATOM SOMP mode: initial delay of one shot pulse triggered by preceding channel Scope : TOM/ATOM SOMP mode. Severity : Low Classification : Non-critical Effects : The first pulse after channel enable is not generated. Description : In case of following configuration of TOM/AOM SOMP mode: the triggered channel is configured to - RST_CCU0=0, - OSM=1, - OSM_TRIG=1, - CN0=MAX-1, and the preceding channel which triggers the single pulse generation is configured to - TRIGOUT=1 - CM0=MAX -> the triggering channel counts from 0 to MAX-1 until it triggers the first pulse on trigger from preceding channel is not generated. Workaround : Preset CN0 of triggered channel to CN0 < MAX-1.	v2.1.1-A1 v2.1.2-A1 v2.1.2-A2

Errata-ID	Errata	refer to
GTM-IP-177	Title : DPLL: setting of lock1= '1' status flag delayed by one event if profile has no gaps (syn_nt/ns = 0) Scope : DPLL Severity : Low Classification : Non-critical Effects : lock1 flag is set delayed by one event. Description : In case that there is no gap in the profile there the status flag lock1 is delayed by one event cycle compared. Workaround :	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
GTM-IP-178	Title : MCS: Evaluation of CAT bit after blocking ARU instruction Scope : MCS Severity : Medium Classification : Non-critical Effects : If the mechanism for canceling blocking ARU transfers by CPU is used the MCS may signalize an aborted ARU transfer by a set CAT bit although the transfer has finished successfully. Description : The specification for the instructions ARD, AWR, ARDI, and AWRI claims that the CAT bit can be evaluated by the MCS program in order to check if the last ARU transfer was successful (CAT=0) or canceled by Software (CAT=1). However, since the CAT bit can be set directly by Software to cancel an ARU transfer at any time the bit does not reflect the status information reliably. Bad case: If the CPU software is setting CAT between the time of ARU data arrival and evaluation of CAT bit. The solution of the problem is to change the current specification and the implementation in the following way: - The function of existing flag Successful ARU Transfer (SAT) is extended to reflect also the status of blocking ARU transfers. - For ARU blocking commands the following sentence "At the beginning of the instruction execution the CAT bit in the register STA is always cleared. After the execution of the instruction the CAT bit is updated in order to show if the instruction finished successfully (CAT = 0) or it was canceled by the CPU (CAT = 1). " is replaced by "At the beginning of the instruction execution the CAT bit in the register STA is always cleared. After the execution of the instruction the SAT flag in the register STA is updated in order to show if the transfer was successful (SAT = 1) or if the transfer failed (SAT = 0) due to a cancel by CPU". Workaround : If the mechanism for canceling blocking ARU transfers by CPU is used and data consistency by ARU transfers is important, a possible workaround may check the consistency by inspection of the transferred data (e.g. checking for linear increment of ECNT for data transfers from TIM to MCS).	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1

Errata-ID	Errata	refer to
GTM-IP-181	Title : TIM: Incorrect signal level bit ECNT[0] in mode TIEM, TPWM, TIPM, TPIM, TGPS Scope : TIM Severity : Low Classification : Non-critical Effects : Inconsistency of input signal level with ECNT bit[0]. Description : In case of reenabling a previously disabled TIM channel the bit ECNT[0] might not reflect the actual signal level of the corresponding input TIM[i]_CH[x]_FOUT until the next input edge occurs. This situation can only occur if between disabling and reenabling the ECNT register is not read. Workaround : a) After disabling the TIM channel, ensure that the ECNT register is read at least once and afterwards the TIM channel can be re-enabled. b) Before reenabling a TIM channel, issue a TIM channel reset a reconfigure the TIM channel control registers.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2

Errata-ID	Errata	refer to
GTM-IP-182	Title : TIM: incorrect signal level provided from previous channel Scope : TIM Severity : Medium Classification : Non-critical Effects : Unexpected signal level. Description : If USE_PREV_CH_IN=1 or USE_PREV_TDU_IN=1 is in use and the previous channel is operating in TBCM mode (TIM_MODE="100") the signal level is not consistent with the value of ECNT[0] of the previous channel. Workaround : No workaround available. It has to be noted that all events are signaled but the rise/fall conditions are incorrect, potentially with TO_CTRL="11" all events can be counted.	v3.0.2-A1 v3.0.3-A1

Errata-ID	Errata	refer to
GTM-IP-183	Title : TIM: signal event data cannot be forwarded from previous channel to next channel Scope : TIM Severity : Low Classification : Non-critical Effects : Filtered input data cannot be fed to more than 2 channels. Description : If USE_PREV_CH_IN=1 is in use and channel is operating in mode (TIM_MODE !=TBCM) the signal event data (level, rise_edge, fall_edge) cannot be forwarded from the previous channel to the next channel. Workaround : Setup next channel with same filter settings and use same primary input data with CICTRL= 1.	v3.0.2-A1 v3.0.3-A1

Errata-ID	Errata	refer to
GTM-IP-184	Title : TIM TDU: starting TDU on CMU clock selected by CLK_SEL not functional Scope : TIM Severity : Medium Classification : Non-critical Effects : TDU cannot be started correctly. Description : TDU_START="001|101" is operating on CMU Clock selected by TCS instead of CMU clock selected by CLK_SEL. Workaround : Set in addition TCS=CLK_SEL to select the CMU clock. It has to be noted that the TDU counters and the start condition will operate on the same CMU clock.	v3.0.2-A1 v3.0.3-A1

Errata-ID	Errata	refer to
GTM-IP-185	Title : TIM TDU: stopping the TDU will not reset the TDU counters Scope : TIM Severity : Medium Classification : Non-critical Effects : TDU counter values are not reset after stopping the TDU. Description : If TDU is configured to TDU_START!="000" and TDU_STOP=000 and TDU_RESYNC=0000 and the TDU is stopped by writing TOCTRL=00 the TDU counters TO_CNTn are not reset and hold their last values. Workaround : No workaround available. Potentially stopping the TDU with TDU_STOP=001|010|011|100 can be used.	v3.0.2-A1 v3.0.3-A1

Errata-ID	Errata	refer to
GTM-IP-186	Title : TIM: external capture sources tdu_sample_evt, tdu_word_evt, tdu_frame_evt cannot be selected Scope : TIM Severity : Low Classification : Non-critical Effects : Register bits cannot be written. Description : Writing EXT_CAP_SRC in register TIM[i]_CH[x]_ECTRL with values 1100|1101|1110 is not possible, an illegal module access AEI_STATUS="10" will be issued. Workaround : Set EXT_CAP_SRC="0101" in channel x and use the TDU unit of the next channel (x+1) to generate the tdu_sample_evt, tdu_word_evt or tdu_frame_evt. By setting TODET_IRQ_SRC in register TIM[i]_CH[x+1]_ECTRL a selection of the sources is possible.	v3.0.2-A1 v3.0.3-A1

Errata-ID	Errata	refer to
GTM-IP-187	Title : TIM TDU: TDU counter TO_CNT2 is reset Scope : TIM Severity : Medium Classification : Non-critical Effects : TO_CNT2 not counting as expected. Description : If TDU is configured to TDU_RESYNC=0000 and SLICING!=11 the counter TO_CNT2 is reset with condition tdu_sample_evt. This behavior is not according to the specification. Workaround : No workaround available. Potentially resynchronize the TDU with TDU_RESYNC!=0000 can be used.	v3.0.2-A1 v3.0.3-A1

Errata-ID	Errata	refer to
GTM-IP-188	Title : TIM TDU: TDU cannot be started as expected Scope : TIM Severity : Medium Classification : Non-critical Effects : TO_CNTn counters are not starting as expected. Description : If TDU is configured to TO_CTRL=00 the counters will not start with the condition defined by TDU_START. Workaround : No workaround available. Potentially using TO_CTRL!=00 can be applied.	v3.0.2-A1 v3.0.3-A1

Errata-ID	Errata	refer to
GTM-IP-190	Title : ARU: DYN update not be as expected Scope : ARU Severity : Low Classification : Non-critical Effects : Dyn-ID from old SR_HIGH and new SR_LOW will merging into ARU routing. Description : If Update-Bit in SR register is set, SR_LOW is written and dyn_id_counter reaches 0 an update will be done with new SR_LOW and old SR_HIGH data. Workaround : Before writing SR_LOW and SR_HIGH write additional SR_HIGH with Update-Bit=0.	v3.0.2-A1 v3.0.3-A1

Errata-ID	Errata	refer to
GTM-IP-191	Title : TIM TDU: TDU counters are reset unexpected Scope : TIM Severity : Medium Classification : Non-critical Effects : TO_CNTn counters are reset unexpected. Description : If TDU is configured to TO_CTRL=00 and TDU_RESYNC=0000|0001|1001 the counters will be reset to 0 on each rising/falling input edge. This behavior is not according to the specification, the counters should continue incrementing. Workaround : No workaround available. Potentially a non-faulty TDU_RESYNC condition can be used.	v3.0.3-A2

Errata-ID	Errata	refer to
GTM-IP-192	Title : TIM TDU: TDU starts unexpected Scope : TIM Severity : Low Classification : Non-critical Effects : TO_CNTn counters start/restart unexpected. Description : If TDU is configured to TO_CTRL=00 and TDU_START=011|111 the counters will start/restart on each rising/falling input edge. This behavior is not according to the specification, the TDU should not start. Workaround : Use TO_START=100 and select an EXT_CAP_SRC which ensures that the ext_capture event will never occur.	v3.0.3-A2

Errata-ID	Errata	refer to
GTM-IP-194	Title : TIM TDU: TDU register TO_CNT2 is reset unexpected Scope : TIM Severity : Low Classification : Non-critical Effects : TO_CNT2 register is reset unexpected. Description : If TDU is configured to SLICING=11 the register TO_CNT2 is reset unexpected. According to specification TO_CNT2 register is not in usage at all when SLICING=11 is configured, no change of initial value is allowed. Workaround : Before TDU functionality is started in mode SLICING!=11 every time initialize the TO_CNT2 if needed.	v3.0.3-A2

Errata-ID	Errata	refer to
GTM-IP-195	Title : TIM TDU: TDU register TO_CNT is loaded with TOV_CNT2 unexpected Scope : TIM Severity : Medium Classification : Non-critical Effects : TO_CNT register is loaded unexpected. Description : If TDU is configured to SLICING=11 and TDU_RESYNC !=0000 and TDU_START !=000 the register TO_CNT is loaded unexpected with TOV2 at each start condition. According to specification TO_CNT2 register loading is only valid at each start condition if TDU_START=000 and TDU_RESYNC=0000 is in use. Workaround : No workaround available. Limited functionality is available if TO_CNT != TOV2 is not needed at occurrence of start condition.	v3.0.3-A2

Errata-ID	Errata	refer to
GTM-IP-196	Title : TIM TDU: TDU tdu_timeout_evt, tdu_word_evt, tdu_frame_evt occur unexpected Scope : TIM Severity : Medium Classification : Non-critical Effects : TDU events occur to early. Description : If TDU is configured to TCS_USE_SAMPLE_EVT=1 the tdu_word_evt and tdu_frame_evt and tdu_timeout_evt occur unsynchronized to tdu_sample_evt/ tdu_word_evt. Workaround : No workaround available.	v3.0.3-A2

Errata-ID	Errata	refer to
GTM-IP-197	Title : TIM TDU: TDU register TO_CNT1 is reset unexpected Scope : TIM Severity : Low Classification : Non-critical Effects : TO_CNT1 register is reset unexpected. Description : If TDU is configured to SLICING=11 and TDU_RESYNC=0x1x the register TO_CNT1 is reset unexpected on tdu_word_evt. According to specification TO_CNT1 register should continue counting. Workaround : No workaround available.	v3.0.3-A2

Errata-ID	Errata	refer to
GTM-IP-198	Title : TIM TDU: TDU register TO_CNT2 is reset unexpected Scope : TIM Severity : Medium Classification : Non-critical Effects : TO_CNT2 register is reset unexpected. Description : If TDU is configured to SLICING=00 and TDU_RESYNC=1xxx the register TO_CNT2 is reset unexpected. Workaround : No workaround available.	v3.0.3-A2

Errata-ID	Errata	refer to
GTM-IP-199	Title : ARU: DYN_UPDATE_EN in ARU_[x]_DYN_ROUTE_HIGH unnecessary Scope : ARU Severity : Low Classification : Non-critical Effects : If DYN_ROUTE_SWAP in ARU_[x]_DYN_CTRL register is set and DYN_UPDATE_EN are different in ARU_[x]_DYN_ROUTE_HIGH and ARU_[x]_DYN_ROUTE_SR_HIGH after swapping it is not clearly with value of DYN_ROUTE_EN is in which register. Description : If DYN_ROUTE_SWAP in ARU_[x]_DYN_CTRL register is set DYN_UPDATE_EN is unused. After swapping it is not clearly with value of DYN_ROUTE_EN is in which register. Workaround : Before writing DYN_ROUTE_SWAP resetting DYN_UPDATE_EN in both register.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2

Errata-ID	Errata	refer to
GTM-IP-200	Title : ARU: DYN_UPDATE_EN in ARU_[x]_DYN_ROUTE_SR_HIGH not reset if dyn update is active Scope : ARU Severity : Low Classification : Non-critical Effects : If DYN_UPDATE_EN is not reset dyn update will done more than once. For updating more than once use swap function. Description : Dyn update is defined as a one-time job. Workaround : if reading ARU_[x]_DYN_ROUTE_HIGH has same value as ARU_[x]_DYN_ROUTE_SR_HIGH with DYN_UPDATE_EN=1 writing DYN_UPDATE_EN=0 in ARU_[x]_DYN_ROUTE_SR_HIGH.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2

Errata-ID	Errata	refer to
GTM-IP-201	Title : DTM: cross channel dead time does not prevent two cross linked outputs to be high Scope : DTM Severity : High Classification : Non-critical Effects : In case of inputs signals DTM_IN[2x] and DTM_IN[2x+1] have rising edges at different point in times and both are high for a common time window, the DTM does not prevent that both high signal are forwarded to the outputs DTM_OUT[2x] and DTM_OUT[2x+1]. As a result, for expected application of full/half bridge controlling, the high side and low side switches controlled by these two outputs are enabled at the same point in time. This damages typically the switches. Description : In case of full/half bridge controlling where the low side switch signal is not the inverse signal of the high side switch signal, one can use the DTM cross channel dead time mode to introduce dead time. Then two neighbored TOM/ATOM channel generate two PWM signals at the DTM inputs DTM_IN[2x] and DTM_IN[2x+1] and the DTM should introduce the dead time wherever necessary and avoid enabling of both output signals at the same point in time. The final output signals are available at DTM_OUT[2x] and DTM_OUT[2x+1]. If both DTM inputs have their edges at the same point in time (typically, one has arising edge while the other one has a falling edge) the correct dead time is applied. If it happens that both DTM input signals are high over a common time period, the DTM erroneously does not prevent from setting both outputs DTM_OUT[2x] and DTM_OUT[2x+1]. In typical applications this causes a damage of the switches. Workaround : In case of DTM cross channel mode enabled, avoid by TOM/ATOM signal generation that both cross linked DTM inputs DTM_IN[2x] and DTM_IN[2x+1] are high (i.e. '1') at the same point in time.	v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2

Errata-ID	Errata	refer to
GTM-IP-202	Title : (A)TOM: no CCU1 interrupt in case of CM1=0 or 1 and RST_CCU0=1 Scope : TOM / ATOM SOMP mode. Severity : Low Classification : Non-critical Effects : For the described configuration no CCU1 interrupt is generated. Description : In case of channel x has configuration of RST_CCU0=1 (i.e. CN0 is reset by trigger input) and CN0 counts from 0 to MAX: if CM1=0, CM0>0 -> no CCU1 interrupt is generated, if CM1=1, CM0=MAX+1 -> only one time a CCU1 interrupt is generated. Workaround : Use for triggering channel y (i.e. the channel that triggers on channel x the reset of counter CN0) the configuration of CM0=MAX, CM1=1. In case of duty cycle configuration of CM1=0 and CM0>0 on channel x use instead of CCU1 interrupt on channel x the CCU0 interrupt of triggering channel y. In case of duty cycle configuration of CM1=1 and CM0=MAX+1 on channel x use instead of CCU1 interrupt on channel x the CCU1 interrupt of triggering channel y.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-203	Title : ARU: Read access to the final address may be skipped when at same point in time a dynamic access occurs Scope : ARU Severity : Low Classification : Non-critical Effects : Requested data transfer on last ARU read address is not served. Description : When dynamic mode is used the normal read access on last address (e.g. aru_round_trip_cycles is 50 -> the last ARU read address is 49) is skipped if at the same point in time a dynamic address is requested to be served. Workaround : 1) do not used last ARU read address if aru_dyn is enabled, 2) do not used aru_dyn, 3) use dyn_wait=0 or 15 only, 4)change ARU_CADDR_END to reset_value + 1.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-204	Title : TIM: incorrect signal level on TIM_MODE change if TIM channel is disabled Scope : TIM Severity : Low Classification : Non-critical Effects : Unexpected signal level. Description : If TIM_EN=0 and TIM_MODE=0b100 (TBCM) and corresponding channel input signal is high any write of TIM_MODE!=0b100 while TIM_EN=0 will not update the signal level bit ECNT[0]. Expected operation is that ECNT[0] will be set to the actual channel input value on TIM_MODE change. Workaround : Avoid change of TIM mode from TIM_MODE=0b100 to TIM_MODE!=0b100 while TIM_EN=0. If TIM channel is enabled (TIM_EN=1) the ECNT(0) value is updated to correct signal value immediately.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-205	Title : TIM: unexpected CNTS register update in TPWM OSM mode Scope : TIM Severity : Low Classification : Non-critical Effects : Unexpected CNTS register content. Description : If OSM=1 and TIM_MODE=0b000 (TPWM) an active edge defined by DSL will stop the measurement. In case of an inactive edge following after 1 GTM system clock cycle the active edge the CNTS register will be reset unexpected. Workaround : a) Use CMU clock in TIM channel with frequency lesser than system clock or b) enable filter and configure filter parameter in a way that two consecutive edges will never occur with distance of GTM system clock.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-206	Title : TIM: incorrect signal level on USE_PREV_CH_IN change if TIM channel is disabled Scope : TIM Severity : Low Classification : Non-critical Effects : Unexpected signal level. Description : If input signal level from actual channel and previous channel has opposite value, a change of USE_PREV_CH_IN in Register TIM_CH_ECTRL while TIM_EN=0 will not update the signal level bit ECNT[0]. Expected operation is that ECNT[0] will be set to the actual channel input value chosen by USE_PREV_CH_IN. With enabling the channel by TIM_EN=1 the signal level bit ECNT[0] is updated correctly. Workaround : a) Determine signal level in case of USE_PREV_CH_IN=1 by reading of ECNT[0] of the previous channel. or b) Enabling of the channel by TIM_EN=1 will update the signal level in ECNT[0].	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-207	Title : TIM: TIM channel TBCM mode signals opposite edge polarity to following channel Scope : TIM Severity : Low Classification : Non-critical Effects : Wrong edge information. Description : If TIM_MODE=0b100 (TBCM) the edge information to the following channel is incorrect. If ECNT[0] changes to 1 a falling edge and if ECNT[0] changes to 0 a rising edge is signaled to the following channel. Workaround : No workaround available.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-208	Title : DPLL: Start of subincrement generation and action calculation delayed by one input event if PCM1/2 bits are set and DPLL_STATUS.FTD = '0' Scope : DPLL Severity : Medium Classification : Non-critical Effects : Delayed start of subincrement generation and action calculation (PMT) by one input event. Description : The DPLL is delaying the start of subincrement generation and the action calculation by one input event cycle if the DPLL starts after activation (DPLL_CTRL1.DEN= 0 ->1) when the flag DPLL_STATUS.FTD = 0. In these situations and when additionally PCM1/2 was activated just before or remains (DPLL_CTRL1.PCM1/2 = 1) the subincrement generation is starting delayed by one input event cycle. This results in a wrong state of the TBU_TS1 angle clock. The start of action calculation (PMT) could be delayed by one input event cycle as well. Workaround : The issue can happen only when the DPLL starts after activation (DPLL_CTRL1.DEN= 0 ->1) when the Flag DPLL_STATUS.FTD = '0'. In these situations and when additionally PCM1/2 was activated just before (DPLL_CTRL1.PCM1/2 = '1') the DPLL_CTRL1.PCM1/2 bits must be set to '0' before the DPLL is activated again.	v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-209	Title : TOM/ATOM: no update of CM0/CM1/CLK_SRC via trigger signal from preceding instance if selected CMU_CLKx is not SYS_CLK Scope : TOM/ATOM Severity : Low Classification : Non-critical Effects : In the described configuration no update of CM0, CM1 and CLK_SRC is done although the update is enabled by register TOM[i]_TGC[y]_GLB_CTRL / ATOM[i]_AGC_GLB_CTRL. Description : The trigger signal between (A)TOM instances (e.g. signal TOM_TRIG_[i]) can be registered and with this delayed by one SYS_CLK period to break long combinational path. The silicon vendor can define it by hardware configuration if there is a register to break the combinational path. It can be configured to be after each instance, after each second, after each third, ... (see microcontroller specification of silicon vendor). If there is a register in the this trigger path between (A)TOM instance i and the succeeding (A)TOM instance i+1, this trigger from instance i does not trigger the update of register CM0, CM1 and CLK_SRC with content of SR0, SR1 and CLK_SRC_SR if the triggered channel of instance i+1 is not running with a selected CMU_CLKx = SYS_CLK. Workaround : If there is a register in trigger path between (A)TOM instance i and (A)TOM instance i+1, the channel of instance i+1 that should be triggered has to use a clock of period identical to SYS_CLK period. A second workaround could be to set up on instance i+1 a redundant channel to trigger other channel of instance i+1 like it was set up on instance i to trigger other channel. Then, start both instances synchronously by using the TBU time base comparator of AGC/TGCx unit (i.e. the ATOM[i]_AGC_ATC_TB / TOM[i]_TGC[y]_ACT_TB register).	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-210	Title : ATOM: data loss in SOMS one-shot mode if ARU is enabled and the period of 2*CMU_CLKx is greater than ARU roundtrip time. Scope : ATOM Severity : Low Classification : Non-critical Effects : Delivered data from ARU is not marked as valid (bit DV not set) and will be ignored. Description : ATOM in SOMS one-shot mode starts to requests new data from ARU with ARU_EN = 1. If new data is delivered by ARU and stored into SR0/1 register, the data will be transferred to CM0/1 register and the ATOM starts to shift with next selected CMU_CLKx. In parallel ATOM requests immediately new data from ARU. If ARU will deliver next data before the first bit of the first data is shifted out which means before the next CMU_CLKx takes place, the data will be stored into SR0/1 register but it will not be marked as valid (bit DV not set) and therefore it will be ignored. Workaround : It has to be ensured, that the time between delivering of two new data via ARU is greater than the CMU_CLKx period. This can be reached by delivering the data by MCS instead of by FIFO. The issue can only occur if the ARU roundtrip time is less than 2 CMU_CLKx periods.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-211	Title : ARU: DYN_UPDATE_EN in ARU_[x]_DYN_ROUTE_HIGH removed Scope : ARU Severity : Low Classification : Non-critical Effects : It is unfavorable to manage 2 signals with the same signal name but different functions. Additionally the signal DYN_ROUTE_EN in ARU_[x]_DYN_ROUTE_HIGH is not necessary. Description : DYN_UPDATE_EN is already defined in ARU_[x]_DYN_ROUTE_SR_HIGH. A second source with same name but different functions is unfavorable. Workaround : Bit 28 of ARU_[x]_DYN_ROUTE_HIGH must be '0' by a write to the register. Do not check bit 28 for any functions.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2

Errata-ID	Errata	refer to
GTM-IP-212	Title : F2A: stream data register will not be deleted after disabling stream. Scope : F2A Severity : Low Classification : Non-critical Effects : Delivering unexpected data by F2A after stream enable. Description : Disabling a data stream inside the F2A will not delete existing valid data inside F2A. So after reenabling the disabled stream, F2A will deliver the old data - independent of the configured data transfer direction. Workaround : Before enabling a data stream, the F2A has to be emptied. After disabling the stream, the ARU read address has to be set to reset value 0x1FE (always empty address). Then the F2A stream has to be configured into the direction ARU to FIFO and the stream must be enabled, so that old data will be transported into FIFO, which requires a short delay. At last the FIFO channel must be flushed and finally disabled.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-213	Title : DTM: shut-off priority causes spikes at DTM output Scope : DTM Severity : High Classification : Non-critical Effects : An unintended pulse is generated at DTM output DTM_OUT[x]_N while DTM should keep the output in configured shut-off state. Description : If DTM shut-off feature is configured with UPD_MODE = 0b010 and DTM_SEL = 0b00 .. 0b11 an edge at input DTM[i-1]_IN0_REDGE, DTM[i-1]_IN0_FEDGE, IN0_REDGE or IN0_FEDGE while shut-off is active (i.e. signal shut_off is high) cause a small pulse at DTM output DTM_OUT[x]_N. Which edge type on input DTM[i-1]_IN0_REDGE, DTM[i-1]_IN0_FEDGE, IN0_REDGE or IN0_FEDGE triggers a pulse at the output depends on DTM_SEL. If DTM shut-off feature is configured with UPD_MODE = 0b001 an edge at TIM_CH_IN0, TIM_CH_IN1 or DTM_AUX_IN or DTM[i-1]_PSU_IN while shut-off is active (i.e. signal shut_off is high) cause a small pulse at DTM output DTM_OUT[x]_N. The root cause of the problem is the specified behavior for DTM: "Note: The reset of SHUT_OFF_SYNC has higher priority than the set of this signal." To solve the problem with specification v3.1.2 the following was specified and implemented: "Note: The reset of SHUT_OFF_SYNC has lower priority than the set of this signal.". Workaround : Do not use UPD_MODE = 0b010 or 0b001 for reset of shut-off.	v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-214	Title : MCS V3: Unexpected bus master access. Scope : MCS V3 Severity : Low Classification : Non-critical Effects : MCS is initiating an unexpected bus master access. So, data of the MCS may be written unexpectedly to a GTM submodule of cluster 0. A possibly incomplete and unexpected read access to an MCS register might be executed. Description : If an MCS channel of the MCS v3 instance of cluster 0 (enabled by bit MCS0_USE_V3 of register GTM_RST) is disabled by an MCS instruction (e.g. MOVL STA, 0x0) and the next or the next but one instruction would access the bus master interface (e.g. BRDI R0, R1 or BWRI R0, R1) the MCS channel is stopped reliably but the specified bus transfer instruction could be spuriously initiated. If the Round Robin Scheduling mode is applied, the MCS program is executed correctly. Workaround : The two succeeding memory locations after a disabling MCS instruction must not contain a bus master transfer instruction if Round Robin Scheduling is not used.	v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-215	Title : FIFO: read pointer will be incremented in ring buffer mode on empty FIFO channel with read access from AFD_CHx_BUF_ACC Scope : FIFO Severity : Low Classification : Non-critical Effects : FIFO channel delivers undefined data to ARU. Description : If an empty FIFO channel x is configured into ring buffer mode an then a read access to AFD_CH[x]_BUF_ACC is executed, the read pointer of this FIFO channel x will be incremented. Workaround : There are 2 possibilities to avoid this erratum : 1. Do not execute a read access to AFD_CH[x]_BUF_ACC after setting the corresponding FIFO channel into ring buffer mode while the FIFO channel is empty. In general there are no real application to read a FIFO channel from CPU side (AFD_CH[x]_BUF_ACC)while the FIFO channel is in ring buffer mode. 2. Do not set a FIFO channel into ring buffer mode while the FIFO channel is empty. First fill the FIFO channel and afterwards configure them into ring buffer mode.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-217	Title : ATOM SOMB mode: if ARU_EN=1, a force update does not update ACBI flags but uses value from ATOM_CH_CTRL register Scope : ATOM SOMB mode. Severity : Low Classification : Non-critical Effects : In the described case the wrong compare strategy may be used. Description : In case of ATOM SOMB mode and ARU_EN=1, if the channel has received new values via ARU and the new values were stored in register SR0, SR1 and ACB_SR register, a force update does not update the ACBI register with the content of register ACB_SR. Instead, the value of register ATOM_CH_CTRL is updated to ACBI register. Workaround : Do not used a forced update if data for ATOM is provided via ARU (ARU_EN=1).	v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-218	Title : DPLL: PWI-IRQ permanently activated Scope : DPLL after reactivation. Severity : Low Classification : Non-critical Effects : PWI-Irq permanently activated. Description : When the DPLL is activated (DPLL_CTRL_1.den= '1') and after that a) the register DPLL_CTRL_0 is written and b) the STATE input signals (emergency mode) is activated, it happens that after the activation of the PWI-IRQ (active input signal event is rejected by negative PVT check) the PWI-IRQ is again and again activated. Workaround : The issue can happen only when the DPLL starts after activation (DPLL_CTRL1.DEN= 0 ->1) when the control register DPLL_CTRL_0 is written after that. If this is prevented the issue will not occur.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-219	Title : DPLL: Wrong internal pointer calculation in case of backwards direction can lead to wrong PMT calculation results (PMT in PAST) Scope : PMT computation of GTM/DPLL in backwards direction. Severity : Low Classification : Non-critical Effects : Wrong PMT computation results by DPLL when DPLL is operating in backwards direction. Description : A DPLL internal pointer register is calculated wrong in backwards direction. In this case the PMT calculations leading to wrong results e.g. PMT in "past". This can only happen in backwards direction. Workaround : combustion engine: a)don't use PMT calculation in backwards direction. or b) If PMT calculations needed even in backwards direction the PMT results must be sent from DPLL to MCS to verify that PMT result is not erroneously in PAST before sent to ATOM.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-220	Title : DPLL: PVT check is deactivated in case of direction change; Behaviour implemented but not documented in specification so far Scope : DPLL-PVT parameter. Severity : Low Classification : Non-critical Effects : Described and implemented behavior not documented in specification. Description : The behavior that the parameter PVT is set to zero after an direction change has occurred is implemented but so far not described in the specification in an adequate manner. Workaround :	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-221	Title : DPLL: Possible inconsistency of internal pointers and parameter NUTE/NUSE when NUTE/NUSE modified in dedicated time window Scope : DPLL increment prediction and PMT calculation. Severity : Low Classification : Non-critical Effects : This inconsistency may lead to the use of wrong data which can corrupt the results of the increment prediction and the frequency calculation as well as the calculation of PMT. Description : The parameters NUTE/NUSE are DPLL internally used to modified pointers as well as to decide which data to be used for doing the prediction of the next increment or the selection of the algorithm of PMT calculation to be used. After a new input signal reaches the DPLL either on TRIGGR or STATE processing unit the internal pointers are updated shortly after the TASI/SASI-irq's. If the NUTE/NUSE parameter is changed after that point of time the pointers are not updated until the next input event such that the described inconsistency may occur. This inconsistency may lead to the use of wrong data which can corrupt the results of the increment prediction and the frequency calculation as well as the calculation of PMT. Workaround : Modification of NUSE/NUTE, VTN/VSN parameters must be done in uncritical time windows: a) after new input signal(TIM0_CH0_irq) before TASI/SASI-irq. b) after PMT calculation has finished for a dedicated increment: e.g. number of active PMT (n) that small THVAL > 10us +n*3us; In this case the parameter NUTE/VTN may be modified after the TISI irq.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-222	Title : DPLL: TAXI-irq not deactivated for THMA=0 Scope : DPLL-TAXI-irq. Severity : Low Classification : Non-critical Effects : TAXI-irq is activated even if parameter THMA set to zero. Description : TAXI-irq not deactivated for THMA=0; The internal interrupt signal is not set correctly such that the notify bit of the DPLL_IRQ_NOTIFY.TAXI bit can only be reset if the taxi-irq is internally deactivated with a next input event which does not cause an activation of this interrupt. Workaround : Use DPLL_IRQ_EN to deactivate TAXI-irq if not needed.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-223	Title : DPLL: discontinuities in the sub increments when DPLL_NUTC/S.FST/FSS=1; set to full scale Scope : DPLL sub increments. Severity : Medium Classification : Non-critical Effects : Not well distributed sub increments in between two teeth. Description : When the physical deviations are used (DPLL_CTRL_1.AMT/AMS=1) or higher accelerations are happening and at the same time NUTE/FST, NUSE/FSS are set to full scale it happens that the sub increment generation is showing irregular behavior. This means that the pulse generator frequency is not calculated correctly which ends up in either to fast or too slow generated micro ticks. Workaround : Don't use DPLL in "fullscale" mode, when NUTE/NUSE is set to maximum and FST/FSS is set to one, when stronger accelerations exist or physical deviation with significant deviation is used. It is possible as well that for the phase of acceleration or the place in the profile, when a physical deviation is relevant for equation DPLL-2c, DPLL_2c1 or DPLL-7c, DPLL-7c1 that just the control bit DPLL_FST/FSS is set to '0'. In this case the error calculation EDT_T, MEDT_T must be observed and checked if not getting to high. If so, this values can be modified via CPU.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-224	Title : DPLL: TASI/SASI-irq's set twice in one input event cycle together with DPLL_CTRL_11.INCF1/2='1'. Scope : DPLL TASI/SASI irq. Severity : Low Classification : Non-critical Effects : The interrupt TASI is set twice in one input event cycle when DPLL_CTRL_11.INCF1=1. The interrupt SASI is set twice in one input event cycle when DPLL_CTRL_11.INCF2=1. Description : If the control bit DPLL_CTRL_11.INCF1/2 is set the TASI/SASI-irq is set twice in one input event cycle. Workaround : Either don't use the configuration DPLL_CTRL_11.INCF1/2= '1' or prevent that TASI/SASI-irq is set twice by dynamically enabling/disabling the TASI/SASI-irq's. The dynamic modification of the TASI/SASI irq's can be done together with the use of the DPLL_STA Register: After an input event is accepted (DPLL_STA.STA_T=0x8) the TASI irq is set in state DPLL_STA_STA_T=0xF. After that happened the TASI irq can be disabled with DPLL_IRQ_EN until this state DPLL_STA.STA_T=0xF occurred again. This states can be monitored in the MCS0. The SASI-irq can be treated similar to that as well by the use of DPLL_CTRL_11.STA_S.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1

Errata-ID	Errata	refer to
GTM-IP-225	Title : DPLL: Wrong action in past decision in case of DPLL_CTRL_11.ACBU=1 for angle condition and DPLL operating in backwards direction Scope : DPLL Severity : Low Classification : Non-critical Effects : The decision about action in past based on the angle criterion will be incorrect under the described conditions. Description : If the control bit DPLL_CTRL_11.ACBU = 1 and the DPLL is operating in backwards direction the decision about action in past based on the angle criterion will be incorrect. Workaround : Don't use DPLL_CTRL_11.ACBU=1 for DPLL operating in backward direction.	v3.1.4-A0

Errata-ID	Errata	refer to
GTM-IP-226	Title : ATOM SOMC mode: cancel compare may lead to wrong output behavior afterwards Scope : ATOM SOMC mode. Severity : Low Classification : Non-critical Effects : In the described case, after cancel of the compare strategy, the following compare events will just toggle the output on each compare match, independent of ACB(41:0) and SL. Description : In case of a compare event with ACB(4:2)=0b100 or 0b101 is canceled after first event match (CCU0) and before second event (CCU1) by writing to bit field ACB(4:0) of register ATOM[i]_CH[x]_CTRL the value 0b111XX, for further compare events the output will be toggled with each compare event independent of bit field ACB(41:0) and SL. Workaround : Do not cancel compare events of strategy 0b100 or 0b101 by writing 0b111XX to bit field ACB(4:0) of register ATOM[i]_CH[x]_CTRL.	v3.1.4-A0

Errata-ID	Errata	refer to
GTM-IP-227	Title : GTM_MX[y]: TIM_AUX_IN multiplexing incorrect Scope : GTM Top Level Severity : Low Classification : Non-critical Effects : In the described configuration the wrong TOM output is selected. Description : The configuration CCM[y]_TIM_AUX_IN_SRC.SRC_CH[x]=0 and CCM[y]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[x]=1 in block GTM_MX[y] selects the TOM output TOM[y]_OUT[x+1] instead of specified output TOM[y]_OUT[x+1]_N. Workaround : Use the DTM swap feature to swap TOM[y]_OUT[x+1] and TOM[y]_OUT[x+1]_N.	v3.1.4-A0

Errata-ID	Errata	refer to
GTM-IP-228	Title : MCS: instruction BWRI not functional Scope : MCS Severity : High Classification : Critical Effects : Write access to unintended address of MCS cluster address space. Description : If the MCS is executing the instruction BWRI A B, it is possible that the data is written to another location as mentioned in the address register B. Workaround : None	v3.1.4-A0

Errata-ID	Errata	refer to
GTM-IP-229	Title : DPLL: No PMT (action) calculation under specific conditions if ARU operates in dynamic configuration mode. Scope : DPLL PMT calculation. Severity : Medium Classification : Non-critical Effects : PMT calculation does not start even if new PMT request has been transferred to DPLL RAM1a memory. Description : If the ARU operates in dynamic configuration mode it can happen that the PMT calculation is not starting although the PMT data input has been transferred to DPLL. Workaround : Don't use ARU in dynamic configuration mode.	v3.1.4-A0

Errata-ID	Errata	refer to
GTM-IP-231	Title : DPLL: Doubled number of micro ticks for the first input event if DPLL operates in mode DPLL_CTRL_11.INCF1/2='1' after the DPLL is restarted and the DPLL was enabled before (DPLL_CTRL_1.DEN = '0' -> '1') Scope : DPLL micro tick generation. Severity : High Classification : Critical Effects : Doubled number of micro ticks for the first input event after DPLL is restarted (6° shift on angle clock). Description : If the DPLL is restarted with DPLL_CTRL_1.DEN is changed from '0' to '1' and the Flag DPLL_STATUS.FTD = '0' in normal mode (DPLL_CTRL_0.RMO='0') or if flag DPLL_STATUS.FSD ='0' if DPLL operates in emergency_mode (DPLL_CTRL_0.RMO='1') the number of micro ticks of the sub_inc1/_c output is doubled for the first relevant input event (TRIGGER/STATE). If the DPLL is operating in synchronous motor control (DPLL_CTRL_1.SMC = '1') and the DPLL is restarted and DPLL_STATUS.FSD = '1' , the number of micro ticks of the sub_inc2/_c output is doubled for the first STATE input event. Workaround : Disable DPLL_CTRL_11.INCF1/2 for first input event after DPLL is restarted.	v3.1.4-A0 v3.1.5-A0

Errata-ID	Errata	refer to
GTM-IP-232	Title : DPLL: Missing micro ticks in mode DPLL_CTRL_11.INCF1 = '1' when PVT condition is detected after DPLL was started/restarted. Scope : DPLL micro tick generation. Severity : High Classification : Critical Effects : Missing micro ticks on angle clock when PVT condition is detected under described operation conditions. Description : If the DPLL is restarted with DPLL_CTRL_1.DEN is changed from '0' to '1' and the mode DPLL_CTRL_11.INCF1 is activated and the second event after the restart arrives under a PVT violation the DPLL does not place any micro ticks for this second input event. The reason is that the PVT check is not suppressed for the first two input events after the restart. The missing micro ticks are generating a -6° shift on the angle clock. Workaround : Disable DPLL_CTRL_11.INCF1 for first two input events after restart.	v3.1.4-A0 v3.1.5-A0

Errata-ID	Errata	refer to
GTM-IP-233	Title : DTM: False reset level of output signal DTM_OUT[x]_N Scope : DTM, TOM, ATOM Severity : Low Classification : Non-critical Effects : The signal level of the output signals DTM_OUT[x]_N changes with the first clock edge after reset going inactive. Description : If the DTM channel is instantiated with complete functionality, the reset level of output signal DTM_OUT[x]_N is set to inverted value of constant (a)tom_out_reset_level_c from gtm_config_pack.vhd. The reset level should be the not inverted value of (a)tom_out_reset_level_c which is the same level as the corresponding (A)TOM output signal. If for the DTM channel only an output register is instantiated for the (A)TOM output signals (A)TOM[i]_OUT[x]_N, the reset value is set to the value of the constant (a)tom_out_reset_level_c from gtm_config_pack.vhd. In this case, the reset value should be zero. In both cases the signal level of the corresponding output signal is set to the correct value after the first clock edge take place. Workaround : None	v3.1.4-A0 v3.1.5-A0

Errata-ID	Errata	refer to
GTM-IP-234	Title : GTM_Toplevel: False AEI address of first AEI access directly after deactivating of GTM_HALT if GTM_RST was written in active phase of GTM_HALT Scope : GTM Toplevel Severity : Low Classification : Non-critical Effects : The first AEI access directly after GTM_HALT goes inactive is always executed to GTM_REV register if the GTM_RST register is written to '1' while GTM_HALT was active and the AEM2 input pipeline register are implemented. Description : The first AEI access after GTM_HALT goes inactive is executed always to GTM_REV register (aei_addr = 0) under the following circumstance : 1. A AEI write access with value '1' to GTM_RST register is executed while GTM_HALT was active. This results into an software reset after GTM_HALT goes inactive. 2. The mentioned AEI access is executed directly after GTM_HALT goes inactive. The AEI access is executed at same time as the software reset 3. The AEM2 input pipeline register are implemented for this device. Workaround : Execute one dummy AEI read access to GTM_REV register after GTM_HALT goes inactive or wait two clock cycles after GTM_HALT goes inactive before execution of the first AEI access.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1

Errata-ID	Errata	refer to
GTM-IP-235	Title : ARU: False system clock on AEI registers and IRQ submodule Scope : ARU Severity : Medium Classification : Non-critical Effects : 1. AEI write accesses to ARU registers are not executed reliably. 2. Hardware clear of ARU interrupts from GTM outside don't work reliably. Description : In case of CFG_CLOCK_RATE=1 (see register GTM_HW_CONFIG) cluster 0 can be configured to run with clock frequency of AEI_SYS_CLK while the ARU always runs with frequency AEI_SYS_CLK/2. For this configuration following erroneous behavior can be observed: 1. If in this case either the CPU or the MCS0 does a write access to one of the ARU register, this write access may not be successful. Reading one of the ARU register is always correct. 2. A hardware interrupt clear for any ARU interrupt by interrupt controller or by a DMA unit (outside GTM) may not be successful. Workaround : Configure Cluster 0 with system clock divided by 2 if 1. an ARU configuration register has to be written or 2. a hardware interrupt clear of ARU interrupt is used.	v3.1.5-A2

GTM-IP-236	Title :
	MCS: BRD(I) or BWR(I) access to register GTM_CLS_CLK_CFG by MCS0 may be erroneous
	
	Scope :
	MCS0
	
	Severity :
	Low
	
	Classification :
	Non-critical
	
	Effects :
	1. Read access of task n:
	- The value read out of register GTM_CLS_CLK_CFG is incorrect.
	- Subsequently scheduled BRD/BRDI or BWR/BWRI commands of task n or other tasks (in the following clock cycles) to any address may lead to corruption of the BRD/BRDI read data.
	2. Write access of task n:
	- Subsequently scheduled BRD/BRDI or BWR/BWRI commands of task n or other tasks (in the following clock cycles) to any address may lead to corruption of the BRD/BRDI read data.
	
	Description :
	In case of CFG_CLOCK_RATE=1 (see register GTM_HW_CONFIG) cluster 0 can be configured to run with clock frequency of AEI_SYS_CLK. For this configuration of cluster 0 running at AEI_SYS_CLK (e.g. 200MHz) a bus read or a bus write of MCS0 task n to register GTM_CLS_CLK_CFG may lead to erroneous behavior.
	1. Read access of task n:
	A task n of MCS0 reads via BRD/BRDI command the register GTM_CLS_CLK_CFG.
	The erroneously behavior is that the read value may be wrong and subsequently scheduled tasks doing also a BRD/BRDI may also be corrupted.
	2. Write access of task n:
	A task n of MCS0 writes via BWR/BWRI command a value to the register GTM_CLS_CLK_CFG.
	The erroneously behavior is that subsequently scheduled tasks doing also a BRD/BRDI may be corrupted.
	
	Workaround :
	Workaround 1:
	Configure Cluster 0 with system clock divided by 2.
	Workaround 2:
	If cluster 0 clock is system clock:
	1. Read access task n:
	To get cluster clock configuration value of MCS0 read register CCM[i]_CFG instead of register GTM_CLS_CLK_CFG.
	2. Write access of task n:
	Task n disables all other tasks before GTM_CLS_CLK_CFG is written and does a NOP after each access to register GTM_CLS_CLK_CFG.
	Code example for task n=2, other enabled tasks are task 0,1:
	MOVL R0, 0
	MOVL R1, 1
		v3.1.5-A2

Errata-ID	Errata	refer to
	BWR R0, MCS0_CH0_CTRL; -- disable task 0 BWR R0, MCS0_CH1_CTRL; -- disable task 1 BRD R2, GTM_CLS_CLK_CFG; -- read in R2 NOP BWR R3, GTM_CLS_CLK_CFG; -- write R3 NOP BWR R1, MCS0_CH0_CTRL; -- enable task 0 BWR R1, MCS0_CH1_CTRL; -- enable task 1	

Errata-ID	Errata	refer to
GTM-IP-237	Title : ARU: CADDR counter reset by SW may not be executed Scope : ARU Severity : Low Classification : Non-critical Effects : ARU counter CADDR isn't reset by SW reset request. Description : In case of CFG_CLOCK_RATE=1 (see register GTM_HW_CONFIG) cluster 0 can be configured to run with clock frequency of AEI_SYS_CLK while the ARU always runs with frequency AEI_SYS_CLK/2. For this configuration of cluster 0 running at AEI_SYS_CLK (e.g. 200MHz) ARU CADDR counter reset by SW - which is initiated by writing to CMU_CLK_EN register inside CMU after it was enabled by bit ARU_ADDR_RSTGLB of register CMU_GLB_CTRL) - may not be executed. The HW reset or ARU counter CADDR is not affected. Workaround : Configure Cluster 0 with system clock divided by 2.	v3.1.5-A3 v3.1.5-A4 v3.1.5-A5

Errata-ID	Errata	refer to
GTM-IP-238	Title : ARU: skipping DYN_READ_ID0 in update-, swap- and ring-mode after dynamic routing cycle with DYN_CLK_WAIT = 15 Scope : ARU Severity : Low Classification : Non-critical Effects : DYN_READ_ID0 is skipped. Dynamic routing ID's starts with DYN_READ_ID1. Description : In a dynamic routing cycle 6 configured ID's are executed with a defined delay of DYN_CLK_WAIT-clock cycles. As the DYN_READ_ID's the actual number of DYN_CLK_WAIT can be reloaded in update-, swap- and ring-mode. If the reloaded value is 15, which means no ID's has to be executed for the actual dynamic routing cycle (6 ID's) - then the first ID (DYN_READ_ID0) of the succeeding dynamic routing cycle is skipped and only the ID's 1 to 5 will be executed. Workaround : Do not use value 15 for DYN_CLK_WAIT in update-, swap- and ring-mode.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5

Errata-ID	Errata	refer to
GTM-IP-239	Title : TIM: data loss on interface to ARU Scope : TIM Severity : Low Classification : Critical Effects : In case of the described configuration the TIM channel does not realizes that the ARU data was not read correctly and the reading sub-module sticks in the ARU read operation to this TIM channel. Description : In case of CFG_CLOCK_RATE=1 (see register GTM_HW_CONFIG) some cluster can be configured to run with clock frequency of AEI_SYS_CLK while the ARU always runs with frequency AEI_SYS_CLK/2. For this configuration of a cluster running at AEI_SYS_CLK (e.g. 200MHz) also the TIM module in this cluster is running at AEI_SYS_CLK. In this case and if a TIM channel is configured to send data to ARU (ARU_EN bit in TIM[i]_CH[x]_CTRL register), the acknowledge of the reading ARU module gets lost. As a result the TIM channel is assuming that the data was read while the reading sub-module (e.g. FIFO, BRC, MCS) sticks in the ARU read operation. Workaround : Workaround 1: If the data from TIM channel should be routed over the ARU to the MCS module, then the MCS can read the data directly over the AEI bus master interface instead of routing it through the ARU. Hint : For this workaround the TIM channel and the MCS channel have to be in the same cluster. Workaround 2: If the data from TIM channel should be routed over the ARU to the FIFO or BRC module, then the MCS can read the data directly over the AEI bus master interface and forward the data via its ARU interface to FIFO or BRC. Hint: If to each TIM channel only one MCS task is assigned to forward the data to ARU, the additional delay caused by this forwarding is the sum of AEI bus master interface read instruction (BRD(I)) and the ARU write instruction (AWR). For this workaround the TIM channel and the MCS channel have to be in the same cluster.	v3.1.5-A3

Errata-ID	Errata	refer to
GTM-IP-241	Title : MCS: MRDIO instruction Scope : MCS Severity : Medium Classification : Non-critical Effects : The target register A of the instruction is updated correctly, however the current value of the MHB register is not updated. Description : The instruction MRDIO A, B does not update the MHB register. Workaround : Specify the program code by calculating the address offset in the program sequence and using the instruction MRDI instead of MRDIO.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A8 v3.1.5-AA v3.1.5-AC v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-242	Title : MCFG: Borrow Mode Scope : MCFG Severity : Low Classification : Non-critical Effects : Invalid data is read/written from/to the MCS RAM. Description : The borrow mode for i-th MCS is not functional if the selected clock rate (configuration register GTM_CLS_CLK_CFG) of the i-th cluster differs from the clock rate of cluster 0. Workaround : Cluster i and cluster 0 must run with the same clock rate.	v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-AA v3.1.5-AC v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-243	Title : DPLL: DPLL_CTRL_11.STATE_EXT Scope : DPLL Severity : Low Classification : Non-critical Effects : The control bit DPLL_CTRL_11.STATE_EXT can be set even if DPLL_CTRL_1.DEN = '1'. Description : The specification describes that the control bit DPLL_CTRL_11.STATE_EXT can be set only if the bit DPLL_CTRL_11.WSTATE_EXT and DPLL_CTRL_1.DEN = '0'. The implementation is that the STATE_EXT bit could be set even if DPLL_CTRL_1.DEN = '1'. Workaround : Never set the DPLL_CTRL_11.STATE_EXT = '1' if DPLL_CTRL_1.DEN = '1'.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-AA v3.1.5-AC v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-244	Title : GTM_Toplevel: ARU SYS_CLK not disabled by GTM_HALT Scope : GTM_Toplevel Severity : Low Classification : Non-critical Effects : CADDR counter is not stopped while GTM_HALT is active. Round robin behavior is ongoing while GTM_HALT is active. Description : On active GTM_HALT, the SYS_CLK for ARU is not disabled. Workaround : None	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-AA v3.1.5-AC v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-245	Title : GTM_Toplevel: In CFG_CLOCK_RATE=1 environment unpredictable clock enabling for clusters with CLS[c]_CLK_DIV=0b10 while GTM_HALT is deactivated Scope : GTM_Toplevel Severity : Low Classification : Non-critical Effects : 1. Cluster configured to CLS[c]_CLK_DIV=0b10: counters/comparators in these clusters will not continue operation correctly due to one missing clock. 2. In GTM_HALT single step mode cluster configured to CLS[c]_CLK_DIV=0b10 will never continue operation due to missing clock. Description : In CFG_CLOCK_RATE=1 environment and GTM_HALT changed to inactive and cluster configured to CLS[c]_CLK_DIV=0b10 these cluster clocks could be omitted. In GTM_HALT single step mode these clusters will never receive a clock. Workaround : None. HINT: When all clusters are configured to CLS[c]_CLK_DIV=0b10 the behavior is correct.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-AA v3.1.5-AC v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-246	Title : GTM_Toplevel: Unexpected setting of output signal GTM_RESTORE while GTM_HALT is active Scope : GTM_Toplevel Severity : Low Classification : Non-critical Effects : Unexpected raising of GTM output signal GTM_RESTORE. Unknown effect to GTM-external logic. Description : After changing cluster clock setting by writing value 0b01 to corresponding bit field of GTM_CLS_CLK_CFG register while GTM_HALT is active, GTM output signal GTM_RESTORE is set unexpectedly. Workaround : Reconfigure cluster clock setting by writing value 0b01 to corresponding bit field of GTM_CLS_CLK_CFG register while GTM_HALT is inactive. Afterwards changed GTM_HALT to active.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-AA v3.1.5-AC v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-247	Title : DPLL: Input event not served after DPLL_CTRL_1.DEN is activated Scope : DPLL Severity : Medium Classification : Critical Effects : Input events on TRIGGER/STATE input not served. Description : After the DPLL is enabled by setting DPLL_CTRL_1.DEN = 0 --> 1 there is a time frame in which a new input signal either TRIGGER or STATE is not recognized and not stored. After power on reset or DPLL software reset this timeframe is about 140 clock cycles. When the DPLL is enabled after the module was disabled the timeframe is 20 clock cycles for a STATE signal and about 45 clock cycles for a TRIGGER input signal. In case of the TRIGGER input signal the time window can be longer if there are accesses to memory RAM1b in parallel. Each RAM1b access will lengthen the time window by 10 clock cycles. Workaround : a) Input event will be neglected, DPLL calculations will start with one event delayed. b) Enable again of DPLL during operation: Within the time frame after the DPLL is enabled the TIM inputs must be observed if an input event has arrived. To adopt the angle clock the missing pulses must be repeated by the PCM1/2 mechanism. c) Enable again of DPLL during operation: Within the time frame after the DPLL is enabled the TIM inputs must be observed if an input event has arrived. Repeat the missing event/pulses by insertion of a TIM input event by writing to configuration register TIM0_IN_SRC.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-AA v3.1.5-AC v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-249	Title : MCS: NARD(I) instruction not functional Scope : MCS Severity : Medium Classification : Critical Effects : If an ARU data source has no data available, the non-blocking ARU instructions NARD and NARDI suspend until new data is available. If new data is available at the data source the non-blocking instructions read the data successfully. Description : If the GTM is integrated with a configurable clock rate (Bit field CFG_CLOCK_RATE of register CCM[i].HW_CONF is set) the instruction NARD and NARDI are not functional. Workaround : If the ARU data sources that should to be read with NARD(I) are within the same cluster as the MCS, consider a possible workaround by accessing the source modules via AEI bus master interface. If the data consistency of the ARU data sources to be read is either not important or it can be reconstructed from the read ARU data the NARD(I) instruction can be achieved by using a blocking ARD(I) and setting up another MCS channel that is cancelling the blocking ARD(I) by cyclic setting of the corresponding CAT bits via bus master interface (writing to MCS_CAT register). The delay between entering the blocking ARU instruction ARD(i) and the write access to the MCS_CAT register must be greater than 1 ARU round trip time. A successful workaround for the SAT bit might be possible by initializing the target registers of the ARD(I) instruction with invalid data in order to detect read ARU data after the instruction has terminated.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7

Errata-ID	Errata	refer to
GTM-IP-250	Title : DPLL: DPLL_STATUS.BWD1/2 not reset after DPLL_CTRL_1.DEN = 1->0->1, when DPLL_CTRL_0 has been written some time before. Scope : DPLL Severity : Medium Classification : Critical Effects : Incorrect status of DPLL_STATUS.BWD1/2 and wrong angle clock because of opposite direction dependent calculation. Description : If the DPLL is disabled and enabled again it happens that the DPLL_STATUS.BWD1/2 flags are not reset. There are 2 conditions in which the DPLL is disabled for a too short timeframe. a) If no active input signal is processed in the DPLL by enable again within a timeframe smaller than ~1,2us (@100MHz GTM clk frequency or 120 system clock cycles) after the register DPLL_CTRL_0 has been written. b) If an active input signal is processed in the DPLL by enable again within a timeframe smaller than 8,6us (@100MHz, GTM clk frequency or 860 system clock cycles) after the register DPLL_CTRL_0 has been written. Workaround : When the DPLL is disabled there should be at least a) a time of 1,2us or 120 system clock cycles until the DPLL is enabled again (DPLL_CTRL_1.DEN = 1), when no active input signal is processed/expected in this situation. b) a time of 8,6us or 860 system clock cycles until the DPLL is enabled again (DPLL_CTRL_1.DEN = 1), when an active input signal is processed or expected in this situation.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-AA v3.1.5-AC v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-251	Title : GTM Top Level: AEI Split; Write to GTM_BRIDGE_MODE register can result in blockage of AEI configuration interface Scope : AEI SPLIT mode. Severity : Medium Classification : Non-critical Effects : Behaviour is not AEI split protocol conform. Bus interface will be blocked. No new transfers possible. Description : If in AEI Split mode a write to the GTM_BRIDGE_MODE register is active and the signal conditions AEI_RESPONSE_REQ=0 and AEI_TRANSACTION_CNT!=0 occur, the bus interface will be blocked forever. Workaround : If this erratum is relevant for a device, can only be judged by the integrator of the GTM_IP in the SOC. The bus interface is fully operational if the condition AEI_RESPONSE_REQ=0 and AEI_TRANSACTION_CNT!=0 will never occur. Typically the state AEI_RESPONSE_REQ=1 is set as soon as AEI_READY=1 was signaled.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-AA v3.1.5-AC v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-252	Title : GTM_BRIDGE_MODE write protection by bit field BRIDGE_MODE_WRDIS not fully functional Scope : GTM_BRIDGE_MODE protection. Severity : Low Classification : Non-critical Effects : GTM_BRIDGE_MODE write protection not functional. Description : If BRIDGE_MODE_WRDIS=1 is set, a write to register GTM_BRIDGE_MODE signals an AEI_STATUS=b10. But the bit fields BRG_RST, MSK_WR_RESP and BRG_MODE can still be changed. Protection is not working correctly! Workaround : No workaround available Don't use BRIDGE_MODE_WRDIS=1.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-AA v3.1.5-AC v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-253	Title : DPLL: PMT data transfer to DPLL via ARU not operating correctly. PMT data could get lost. Scope : DPLL ARU interface. Severity : Medium Classification : Critical Effects : PMT data (PSA, DLA) not transferred to DPLL-RAM1a while ACB bits are transferred correctly to registers DPLL_ACB. Description : In a dedicated internal state of the DPLL-ARU interface there is a coincidence of two independent events. a) A new ARU data transfer starts (PMT data). b) The DPLL is internally switching to calculation of PMT. Because the ARU interface for is switched off during PMT calculation for exclusive internal use of RAM1a this leads to the situation that the incoming PMT data (PSA, DLA) are not transferred into the DPLL-RAM1a. The ACB data of the PMT request is transferred correctly to the DPLL_ACB registers. Workaround : Control of DPLL_ACT_STA .ACT_N(i) via MCS0 (or CPU) to verify if PMT data has reached the DPLL. If data missed DPLL_ACT_STA .ACT_N(i)=0 the PMT transfer should be repeated.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8

Errata-ID	Errata	refer to
GTM-IP-254	Title : TIM TDU: TDU_STOP=b101 not functional Scope : TIM Severity : Low Classification : Non-critical Effects : TO_CNT1, TO_CNT cannot be stopped counting. Description : Stop counting of register TO_CNT on an tdu_word_event or stop counting of TO_CNT1 on a tdu_frame_event is not possible. Workaround : No workaround available.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-255	Title : RTL Simulation uses incorrect file in simulation which can lead to incorrect simulation results Scope : RTL Simulation. Severity : Low Classification : Non-critical Effects : Simulation not functional. Description : This erratum only covers the RTL simulation at licensee. For synthesis the correct files are in use if delivered file list (design/gtm_pck/syn/include/gtm_pck.filelist) is used. If in simulation for the entity gtm_ip no configuration is in use, it can happen that due to compilation order a wrong architecture (named fpga File: clk_latch_fpga.vhd) is chosen for the entity clk_latch. Workaround : A) Ensure that delivered configuration gtm_ip_cfg.vhd is in use for simulation. B) remove file clk_latch_fpga.vhd from release database.	v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-AA v3.1.5-AC v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-256	Title : Wrong AEI Status Signal for protected write to TIM[i]_CH[x]_GPR0 Scope : AEI Status Signal. Severity : Low Classification : Non-critical Effects : Incorrect AEI status signaling if protected write occurs. Description : Writing to register GPR0 in any mode different to TSSM the expected AEI status signal value "10" does not occur. Protection of the register is functional, GPR0 will not change content. Workaround : No workaround available.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AC v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-257	Title : Capturing TBU_TS0 values while TBU_CH0_CTRL .LOW_RES=1 not functional for TIM[i] for i=1..n Scope : TIM Severity : Low Classification : Critical Effects : Capturing wrong TBU_TS0 values in TIM[i]_CH[x]_CNTS or TIM[i]_CH[x]_GPR0 or TIM[i]_CH[x]_GPR1, (i=1..n). Description : While using TBU_CH0_CTRL.LOW_RES=1, in all TIM[i] i=1..n instances the lower bits of TBU_TS0[23:0] are captured instead of the higher bits TBU_TS0[26:3]. Affected capture source selection (i=1..n): - TIM[i]_CH[x]_CTRL.CNTS_SEL=1; - TIM[i]_CH[x]_CTRL.EGPR0_SEL=0, TIM[i]_CH[x]_CTRL.GPR0_SEL=0; - TIM[i]_CH[x]_CTRL.EGPR1_SEL=0, TIM[i]_CH[x]_CTRL.GPR1_SEL=0. Workaround : A) Setup another TBU channel e.g. TBU_TS1 or TBU_TS2 which is clocked by another CMU_clock source with a frequency of clock_frequency(TBU_TS0) / 8. Select this TBU_TSx source for capturing to TIM[i]_CH[x]_GPR0 or TIM[i]_CH[x]_GPR1. B) If captured values are processed by MCS or CPU correct them by divide by 8.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB

Errata-ID	Errata	refer to
GTM-IP-258	Title : GTM_Toplevel: GTM_RESTORE signal transition 1->0 may occur 1 clock cycle to early Scope : GTM_Toplevel Severity : Medium Classification : Non-critical Effects : GTM_RESTORE may be released 1 clock cycle to early. This could lead to the effect that external data trace unit will trace information twice. Description : If signal GTM_HALT_REQ is raised while GTM_CLSi_ENCLK=0 and cluster i is operating on single clock rate, the corresponding GTM_RESTORE signal will change to 0 one clock cycle to early. Workaround : If it can be ensured that GTM_HALT_REQ is raised when GTM_CLSi_ENCLK=1 and cluster i is operating on single clock rate. The faulty behavior can be prevented.	v3.1.5-A9 v3.1.5-AB

Errata-ID	Errata	refer to
GTM-IP-259	Title : GTM_Toplevel: GTM_ACTIVE signal incorrect Scope : GTM_Toplevel Severity : Low Classification : Non-critical Effects : GTM_HALT state of GTM_IP cannot be entered. Due to missing GTM_HALT_ACTIVE signal, handshake protocol with GTM_HALT_REQ signal is violated. There can be the situation that GTM_IP cannot leave the GTM_HALT state anymore. Description : If signal GTM_HALT_REQ is raised while all clusters are switched off, the GTM_ACTIVE signal is not switching to 1. Workaround : Prevent switching off all clocks in all clusters when GTM_HALT_REQ will be used. At least 1 cluster clock must be kept enabled.	v3.1.5-AD

Errata-ID	Errata	refer to
GTM-IP-260	Title : TOM/ATOM: async. update in SOMP mode with CM1=0 and selected CMU clock unequal sys_clk not functional Scope : TOM/ATOM Severity : Low Classification : Non-critical Effects : The output signal level is not set to inactive level. It will remain at actual level. Description : An asynchronous update of the duty cycle by writing value 0 to CM1 register while a CMU clock unequal sys_clk is selected is not working. It is expected that the output signal level is set immediately to inactive level but it will remain at actual level. Workaround : Writing value 1 instead of 0 to CM1 register will set the output to inactive level in the actual generated PWM period. If the duty cycle duration should be zero also for the following period, the user has to take care, that the CM1 register is loaded with a 0 at the beginning of the next PWM period. Otherwise, if the content of register CM1 remains at 1, a peak of one clock cycle with the selected CMU clock will be observed, with the next PWM period.	v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-261	Title : ATOM SOMB: writing new value to CM1 register is not recognized as valid data Scope : ATOM Severity : Low Classification : Non-critical Effects : If a new value is written to CM1 register and afterwards a new value to SR1 register is written, the CM1 register will be reloaded with the content of SR1 register immediately. The compare cycle starts with the reloaded value. The first value which was written to CM1 register get lost. Description : Writing a new compare value to CM1 register is not recognized as valid data. Workaround : Start a new compare cycle by writing new compare values to SRx register and update the CMx register with the force update mechanism.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-B1 v3.1.5-B8

GTM-IP-262	Title : SPEC-DPLL: PSSC/PSTC behaviour description incorrect Scope : DPLL Severity : Low Classification : Non-critical Effects : The PSSC value is not updated at the following trigger slope but at the following STATE slope with the value PSSC=PSSM +/- correction value with correction value = inc_cnt1 - nmb_s. This might lead to an unexpected behaviour of the GTM IP. The PSTC value is not updated at the following STATE slope but at the following TRIGGER slope with the value PSTC=PSTM +/- correction value with correction value = inc_cnt1 - nmb_t. This might lead to an unexpected behaviour of the GTM IP. Description : When changing from normal to emergency mode (DPLL_CTRL_0.RMO = 0->1) the RAM1b.PSSC value is not calculated as specified. When changing from emergency to normal mode (DPLL_CTRL_0.RMO = 1->0) the RAM1b.PSTC value is not calculated as specified. In the specification it is written: For changing from normal mode to emergency mode at the following TRIGGER slope (according to the RMO value in the shadow register)[1)] the PSSC value is calculated by PSSC = PSSM + correction value (forward direction) or PSSC = PSSM - correction value (backward direction) with the correction value = inc_cnt1 - nmb_t. For changing from emergency mode to normal mode at the following STATE slope (according to the RMO value in the shadow register)[2)] the PSTC value is calculated by PSTC = PSTM + correction value (forward direction) or PSTC = PSTM - correction value (backward direction) with the correction value = inc_cnt1 - nmb_s. In case no further TRIGGER or STATE events the CPU has to perform the above corrections. Instead the following behaviour should be specified: For changing from normal mode to emergency mode at the following STATE slope (according to the RMO value in the shadow register)[2)] the PSSC value is calculated by PSSC = PSSM + correction value (forward direction) or PSSC = PSSM - correction value (backward direction) with the correction value = inc_cnt1 - nmb_s. For changing from emergency mode to normal mode at the following TRIGGER slope (according to the RMO value in the shadow register)[1)] the PSTC value is calculated by PSTC = PSTM + correction value (forward direction) or PSTC = PSTM - correction value (backward direction) with the correction value = inc_cnt1 - nmb_t. In case no further TRIGGER or STATE events the CPU has to perform the above corrections.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD

Errata-ID	Errata	refer to
	[1] stored in an independent shadow register for an active TRIGGER event and for DEN = 1. [2] stored in an independent shadow register for an active STATE event and for DEN = 1. Workaround : 1) If possible leave PSSC or PSTC as is. If a different value for PSSC/PSTC is necessary the value could be written by CPU interface as already written in the specification. Starting with version 3.1.5 the modification could be done by MCS0 as well. 2) Alternatively, the application can disable the DPLL via DPLL_CTRL_1.DEN=0 and then re-start the DPLL in emergency or normal mode with the following sequence: Setting up the DPLL modes as desired, for example (not mandatory values) GTM_DPLL_CTRL_1.B.PIT = 1; -- only as an example GTM_DPLL_CTRL_1.B.DMO = 0; -- only as an example GTM_DPLL_CTRL_1.B.COA = 0; -- only as an example GTM_DPLL_CTRL_1.B.SYSF = 1; -- only as an example GTM_DPLL_CTRL_1.B.TSL = 1; -- only as an example GTM_DPLL_CTRL_1.B.SSL = 3; -- only as an example GTM_DPLL_CTRL_0.B.SEN/TEN = 1; -- only as an example Then switch into emergency/normal mode and enable the DPLL again. GTM_DPLL_CTRL_0.B.RMO = 1 or 0; -- only as an example GTM_DPLL_CTRL_0.B.SEN/TEN = 1; -- only as an example GTM_DPLL_CTRL_1.B.DEN = 1; -- only as an example In this case the behaviour for PSSC/PSTC is different: For DPLL_CTRL_0.RMO = 0->1: PSSC=PSSM. For DPLL_CTRL_0.RMO = 1->0: PSTC=PSTM. If in this case nevertheless a different value for PSSC/PSTC is necessary the value could be written by CPU interface as already written in the specification. Starting with version 3.1.5 the modification could be done by MCS0 as well.	

Errata-ID	Errata	refer to
GTM-IP-263	Title : DPLL: DPLL_STATUS.lock1 flag (0 ->1) delayed after direction change when DPLL operating in DPLL_CTRL_0.rmo = 1. Scope : DPLL Severity : Low Classification : Non-critical Effects : When the DPLL is operating in emergency mode (DPLL_CTRL_0.rmo = 1) and a direction change happens the lock1 flag is reset to "0" as described in spec. The problem is, that the lock1 bit is set to "1" again after 4 detected gaps (missing state irq, ms -flag) and not as requested after 2 subsequent gaps. Description : The DPLL_STATUS.lock1 flag does not behave like requested in the specification: When the DPLL is operating in emergency mode (DPLL_CTRL_0.rmo = 1) and a direction change happens the lock1 flag is reset to "0" as described in spec. The problem is, that the lock1 bit is set to "1" again after 4 detected gaps (missing state irq, ms -flag) and not as requested after 2 subsequent gaps. Workaround : If you need to use this information one could observe the missing state interrupt to check for the correct point in time when the lock1 flag should be set again. If the use of the lock1 flag is not time critical it could be used as is with the latency describe above.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD

Errata-ID	Errata	refer to
GTM-IP-264	Title : MCS: Bad reactivation of MCS program after GTM halt phase Scope : MCS Severity : Medium Classification : Non-critical Effects : The reactivated program can execute either an unexpected program branch or it can read unexpected data from RAM. Description : If the bit field CFG_CLK_RATE of register CCM[i]_CH_CONF is set and an MCS runs on a cluster i while bit field CLSi_CLK_DIV of register GTM_CLS_CLK_CFG is set to 1, the reactivation of an MCS channel after GTM halt phase can lead to an unexpected program behavior. Workaround : Do not use GTM halt feature or run MCS program on a cluster configured with value 2 for bit field CLSi_CLK_DIV of register GTM_CLS_CLK_CFG.	v3.1.5-A9 v3.1.5-AB

Errata-ID	Errata	refer to
GTM-IP-265	Title : SPE: Same internal enable clock signal on SPE in GTM clusters (1..n) like internal enable clock signal of SPE in GTM cluster 0 Scope : SPE Severity : Medium Classification : Non-critical Effects : Due to the described wrong clock enable signal in the SPE modules of cluster 1..n the SPE(1..n) irq and eirq output signals can get lost. Description : Due to the described wrong clock enable signal in the SPE modules of cluster 1..n the SPE(1..n) irq and eirq output signals can get lost. This is because the irq/eirq signals are gated with the described clock enable signal. The SPE(1..n) irq/eirq signals can get lost when the cluster n has a different clock setup compared to cluster 0 and cluster 0 is running on a non-divided clock. This problem does not occur in the so called level interrupt mode (SPE[i]_IRQ_MODE=0x0). Workaround : One of the following countermeasures can be used to solve the problem: a) If possible use interrupt level mode. b) Use for cluster 0 a non-divided clock (GTM_CLS_CLK_CFG(1:0)= 01). c) Use the same clock divider values for cluster 0 and the cluster in which the SPE modules shall be used.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-266	Title : SPE/DPLL: Loss of DPLL-STATE input signal Scope : SPE/DPLL Severity : Medium Classification : Non-critical Effects : The DPLL does not get a STATE input signal. Description : If the GTM clusters 0 and 1 are running on different clocks an internal handshake signal is getting lost which has the effect that the DPLL does not get a STATE input signal. Workaround : Use the same clock divider values for cluster 0 and the cluster 1 (GTM_CLS_CLK_CFG(1:0)= GTM_CLS_CLK_CFG(3:2)).	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-267	Title : DPLL: Pulses are not generated at highest speed when DPLL_CTRL_11.INCF1/2 ='1' after change of direction Scope : DPLL Severity : Low Classification : Non-critical Effects : Under the described conditions a part of the micro ticks is not generated at maximum speed. If the system operates slow enough under the direction change condition all the micro ticks can be generated until the next input signal occurs. If the next input signal after the direction change comes faster and not all the micro ticks for the direction change has placed the DPLL is able to give out the pulses at highest speed with the next input signal if in automatic end mode (DPLL_CTRL_1.DMO='0') the pulse correction strategy is set to DPLL_CTRL_1.COA='0'. If DPLL_CTRL_1.COA='1' the missed micro ticks are repeated together with the pulses for the next increment. The number of subincrements in total is not corrupted at all. Description : When the DPLL is operated in DPLL_CTRL_11.INCF1/2='1' pulse generation mode the micro ticks during direction change should be generated with highest speed. This is not the case for all the scheduled micro ticks. Workaround : If the pulse alignment under direction change condition is not a problem no workaround is needed. If it is necessary to have the pulses in time, as described in the specification, the pulse generation can be accelerated by forcing the speed of the pulse generator. If the signals DPLL_CTRL_1.PCM1/2, DPLL_CTRL_11.PCMF1/2 = '1', DPLL_CTRL_11.PCMF1_INCCNT_B = '1' are used the number of pulses given by DPLL_MPVAL1/2 (RAM1b) are generated at highest speed. In this case the overall number of pulses to be generated is not modified.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-269	Title : MCS: Missing ECC Error handling on data fetch of MRDIO instruction Scope : MCS Severity : High Classification : Non-critical Effects : The corresponding MCS channel does not signalize the ECC error in its ERR flag and the channel does not halt immediately after reading the data. Description : If an ECC error input signal (mcs[i]_ram0_ecc_err and mcs[i]_ram1_ecc_err) of the i-th MCS instance signalizes an ECC error during the data fetch phase of an MRDIO instruction, the ECC error is not recognized by the MCS. Workaround : Specify the program code by calculating the address offset in the program sequence and using the instruction MRDI instead of MRDIO.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-270	Title : (A)TOM: output signal is postponed one period for the values CM0=1 and CM1>CM0 if CN0 is reset by the trigger of a preceding channel (RST_CCU0=1) Scope : TOM, ATOM SOMP mode. Severity : Low Classification : Non-critical Effects : The expected output edge will be postponed by one period. Description : If counter CN0 is reset by the trigger of a preceding channel (bit RST_CCU0 of register TOM[i]_CH[x]_CTRL/ATOM[i]_CH[x]_CTRL is set), then the value of CM0 defines the signal edge to SL (signal level), whereas CM1 defines the edge to !SL (inverted signal level). If - in this case - the value 1 is configured for the output edge to SL (CM0=1) and CM1 is configured to greater than CM0 (CM1>CM0) the expected output edge will be postponed by one period. Workaround : Instead of configuring CM0=1 it is also possible to configure CM1=1 and to invert SL to get the expected edge at counter value 1 (CN0=1).	v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B1 v3.1.5-B8

GTM-IP-271	Title : DPLL: No DCGI-irq after direction change and DPLL_CTRL_0 has been written Scope : DPLL Severity : Low Classification : Non-critical Effects : DCGI-irq does not occur. Description : If the DPLL is running in normal mode and a direction change is detected after the register dpll_ctrl_0 has been written the DCGI-Interrupt does not occur for following direction changes until both a TRIGGER and a STATE input signal has been arrived at the DPLL inputs. Workaround : 1) Don't write to DPLL_CTRL_0 until both an active TRIGGER, STATE input signal has occurred in case of an direction change within this time frame. How to prevent this, under need of changes of: a)Need to deactivate Trigger/state input signal (replacing changes on DPLL_CTRL_0.SEN, DPLL_CTRL_0.TEN): Switch according TIM input channels receiving the TRIGGER/STATE input signal by: Modification of TIM[i]_CH[x]_IN:SRC.MODE[i]="10", VAL[i] b) Need to change from normal mode to emergency mode by change of DPLL_CTRL_0.RMO If this is necessary the write operation to DPLL_CTRL_0 cannot be prevented. c) Changes of DPLL_CTRL_0.TNU, SNU. MLT: Such changes should not be necessary, if not the write operation to DPLL_CTRL_0 cannot be prevented. d) Changes of Adaption modes TRIGGER, STATE (replacing changes of DPLL_CTRL_0.AMT, AMS) Activate/Deactivate AMT, AMS after power up, activate mode by writing adapt data to RAM1c PD(ADT_S) and or RAM2 PD (ADT_T) e) Changes of Input Delay TRIGGER,STATE (replacing changes of DPLL_CTRL_0.IDT, IDS) Activate/Deactivate TIM[i]_CH[x]_CTRL.FLT_EN to enable or disable filter input data within the dedicated TIM input channel. f) Changes of DPLL_CTRL_0.IFP: If such changes are necessary the write operation to DPLL_CTRL_0 cannot be prevented.	v1.3 v1.4.0 v1.4.2 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
	if 1) is not doable: 2) After writing to DPLL_CTRL_0: Check for direction change by evaluating the register DPLL_STATUS.BWD1 when an inactive edge occurred on TRIGGER (TISI-irq) until both an active TRIGGER, STATE input signal has occurred. The pulse corrections and pointer modifications of the direction change are operated correctly !	

GTM-IP-272	Title : DPLL: No update of DPLL_RAM1b.PSTC after direction change and DPLL_CTRL_0 has been written Scope : DPLL Severity : High Classification : Non-critical Effects : Incorrect PSTC value, incorrect PMT/action results. At the tooth with the incorrect PSTC only it can be observed that the subincrements are generated at highest speed. Description : If the DPLL is running in normal mode and a direction change is detected after the register dpll_ctrl_0 has been written the DPLL_RAM1b.PSTC value is not updated for the following active input signal and keeps the difference for the following input signals. Workaround : 1) Don't write to DPLL_CTRL_0 until both an active TRIGGER, STATE input signal has occurred in case of an direction change within this time frame. How to prevent this, under need of changes of: a)Need to deactivate Trigger/state input signal (replacing changes on DPLL_CTRL_0.SEN, DPLL_CTRL_0.TEN): Switch according TIM input channels receiving the TRIGGER/STATE input signal by: Modification of TIM[i]_CH[x]_IN:SRC.MODE[i]="10", VAL[i] b) Need to change from normal mode to emergency mode by change of DPLL_CTRL_0.RMO If this is necessary the write operation to DPLL_CTRL_0 cannot be prevented. c) Changes of DPLL_CTRL_0.TNU, SNU. MLT: Such changes should not be necessary, if not the write operation to DPLL_CTRL_0 cannot be prevented. d) Changes of Adaption modes TRIGGER, STATE (replacing changes of DPLL_CTRL_0.AMT, AMS) Activate/Deactivate AMT, AMS after power up, activate mode by writing adapt data to RAM1c PD(ADT_S) and or RAM2 PD (ADT_T) e) Changes of Input Delay TRIGGER,STATE (replacing changes of DPLL_CTRL_0.IDT, IDS) Activate/Deactivate TIM[i]_CH[x]_CTRL.FLT_EN to enable or disable filter input data within the dedicated TIM input channel. f) Changes of DPLL_CTRL_0.IFP:	v1.3 v1.4.0 v1.4.2 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
	If such changes are necessary the write operation to DPLL_CTRL_0 cannot be prevented. if 1) is not doable: 2) In this case (direction change after DPLL_CTRL_0 has been written before both a TRIGGER and STATE input event has occurred) the PSTC value has to be corrected via CPU access from outside the DPLL. To achieve this the calculation PSTC_new=PSTC_old +/- nmb_t_tar (+ forward(dir1=0); - backward(dir1=0)) has to be performed and stored to RAM1b.PSTC earlier as 1000 system clock cycles after the active input event, or 850 system clock cycles after the TASI-irq has occurred. The PSTC value is internally of the DPLL used for PMT calculations. If no PMT calculation is ongoing in the tooth after direction change and the PSTC value is not needed in GTM external processes the described timing constraint for the PSTC correction can be relaxed until before the next PMT calculations are requested or the PSTC value is needed otherwise.	

Errata-ID	Errata	refer to
GTM-IP-273	Title : TBU: If GTM is operating in mode CFG_CLOCK_RATE=1 and cluster 0 configured to CLS[0]_CLK_DIV=0b01 all clusters i with CLS[i]_CLK_DIV=0b10 will operate on TBU_TS[j] values not consistent with source of TBU_CH[j]_BASE in Cluster 0. Scope : TBU Severity : High Classification : Critical Effects : 1. TBU_TS[j] in cluster[1..n] are not counting continuously (only odd or only even values present). 2. TBU_TS[j] in cluster[1..n] are not changing at all. 3. TBU_TS[1,2] using subinc clocks from DPLL can arbitrarily stop and continue again counting. Description : If TBU (cluster 0) is operating in CFG_CLOCK_RATE=1 environment with undivided system clock (CLS[0]_CLK_DIV=0b01) the signals TBU_TS[i] are not synchronized properly for clusters j[1..n] which operate on CLS[j]_CLK_DIV=0b10. Workaround : None. HINT: When cluster 0 operates with CLS[0]_CLK_DIV=0b10, TBU_TS[j] in clusters[1..n] operate correctly.	v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF

Errata-ID	Errata	refer to
GTM-IP-274	Title : MCS: MRDIO instruction cannot store read data in entire register set XOREG Scope : MCS Severity : High Classification : Non-critical Effects : If the instruction tries to store read data to register A (with A is element of RS0, RS1, ..., RS7, GMI0, GMI1, DSTA, DSTAX) the data is stored in another register. The invalid address of the actual target register can be obtained by forcing the most significant address bit (bit 4) of register A to zero. Description : MRDIO instruction cannot store read data in the register RS0, RS1, ..., RS7, GMI0, GMI1, DSTA, or DSTAX. Workaround : Specify the program code by calculating the address offset in the program sequence and using the instruction MRDI instead of MRDIO and move the read data of register A (A is element of OREG) to the desired register of the set XOREG using the instruction MOV.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-275	Title : MCS: DIVS instruction could read wrong data if MCS is not in round robin mode Scope : MCS Severity : High Classification : Non-critical Effects : The DIVS instruction is calculating wrong results if the delay between the DIVS and the preceding BRD(i) instruction is one or two clock cycles. Description : If a DIVS instruction tries to access data that results from a previous bus read access (instruction BRD or BRDI) and the delay between the corresponding BRD(I) instruction and the DIVS instruction is one or two clock cycles, the DIVS reads wrong data. However, the DIVS instruction should initiate a pipeline flush due to a data dependency hazard. Workaround : Solution 1: Configure the MCS with scheduling mode round robin. In this case the delay between the BRD(I) and the DIVS instruction is always greater than 2. Solution 2: Add two NOP statements between BRD(I) and DIVS. E.g.: modify sequence "BRDI R0, R1; DIVS R0, R2, 16" as "BRDI R0, R1; NOP; NOP; DIVS R0, R2, 16".	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-276	Title : MCS Bus Master Interface: A write initiated by a BWR/ BWRI instruction to the read only address range ADC_CH[0]_DATA to ADC_CH[31]_STA will block the bus master interface forever Scope : MCS Severity : High Classification : Non-critical Effects : MCS channel program execution stops. PC is not incrementing. Description : If a BWR / BWRI instruction writes to the address range ADC_CH[0]_DATA to ADC_CH[31]_STA the bus master interface will be blocked. No further bus master accesses (read or write) of every MCS channel will be executed anymore. These accesses are stored in the bus master transaction buffer. As soon as the transaction buffer is full all instructions BRD / BRDI / BWR / BWRI will suspend and wait forever. Please notice that read data in case of BRD / BRDI will be not deterministic anymore. Note: Transaction buffer length cluster 0 = 8; Transaction buffer length cluster 1-n = 2. Workaround : No workaround available. MCS code has to be developed in a way that no write will be used to the addresses ADC_CH[0]_DATA to ADC_CH[31]_STA. If the BWRI instruction is in use the correctness of the address has to be proven to prevent unintended writes to the address range ADC_CH[0]_DATA to ADC_CH[31]_STA.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-277	Title : AFD: Erroneous behavior of back-to-back accesses on AEI to FIFO interface Scope : AFD Severity : High Classification : Critical Effects : False data are read from FIFO. Description : Parallel accesses from CPU and MCS master interface to the AEI interface of the AFD submodule can result in back to back accesses on AFD AEI interface. Two erroneous scenario could occur on this back to back accesses : 1. A write access followed back to back by a read access on AFD[i]_CH[z]_BUF_ACC register results in an erroneous write access to a undefined address of the FIFO memory. 2. A write access to AFD[i]_CH[z]_BUF_ACC register followed back to back by a direct FIFO memory write access. Here the second write access to the FIFO memory will not happen and results in a data loss. Workaround : For the first scenario are no work around available. For the second scenario a work around could be to proof the correct written data by reading the data back. If the data was not written, write again.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-278	Title : FIFO: Restoring of F2A (ARU to FIFO interface) read access to FIFO after GTM_HALT condition not functional Scope : FIFO Severity : Low Classification : Non-critical Effects : False data are read from FIFO. Description : GTM_HALT is activated while the submodule F2A is executing a read access to a FIFO channel buffer. Then the F2A read access has to be stopped and restored after GTM_HALT is deactivated. The restoring of the F2A read access will hand back false data to F2A. Workaround : No workaround available.	v1.4.0 v1.4.2 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-279	Title : TIM Serial shift mode TSSM: Using GPR1 register as shadow register for CNTS register is not functional Scope : TIM TSSM mode. Severity : Low Classification : Non-critical Effects : Reloading amount of bits per word (CNTS) not possible by using the shadow register GPR1. Description : In TSSM mode writing the GPR1 register defines the amount of bits which shall be captured in the next word. On the capture event (CNTS[15:8]=CNTS[7:0]) the GPR1 register content should be transferred to CNTS. This functionality is not usable: a) The GPR1 register cannot be written under all circumstances. b) The update of CNTS with GPR1 is not possible under all circumstances. Workaround : Solution 1: Define CNTS once by using same amount of bits per word for all captures. Don't use the shadow register update mechanism for CNTS. Solution 2: Define in CNTS the total amount of bits in the frame which have to be shifted. Define with the external capture mechanism (signal tssm_ext_capture) the capture events for capturing individual amount of bits per word. This can be realized by setting up the counters in the TDU by writing register TOV. After each capture by reconfiguring the register TOV the amount of bits for the next word can be defined/adjusted.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-280	Title : FIFO : Ring buffer mode not functional if corresponding FIFO buffer is completely filled Scope : FIFO ring buffer mode. Severity : Low Classification : Non-critical Effects : The samples in the FIFO buffer are transmitted to ARU in ring buffer mode only once. Thereafter the transmission stops. Description : Transmitting a set of samples frequently to ARU, the FIFO ring buffer mode can be used. At first the samples are written into the corresponding FIFO buffer. Thereafter the FIFO ring buffer mode is activated and the frequently transmission of the samples to ARU starts. If the number of samples matches exactly the FIFO buffer size, the samples are transmitted only once to ARU. Afterwards no further values will be transmitted to ARU. Workaround : A simple work around is just to configure the size of the FIFO buffer at least one element bigger than the needed number of samples which should be transmitted to ARU in ring buffer mode.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-281	Title : TIM Serial shift mode TSSM EXT_CAP_EN=0: Capturing of data not synchronized with selected shift clock Scope : TIM TSSM mode. Severity : Low Classification : Non-critical Effects : Capturing data to registers TIM[i]_CH[x]_GPRn will occur to early. Description : If the capture condition CNTS[15:8]=CNTS[7:0] is true the capture event shall happen synchronized to the selected shift_clock. Due to this erratum, the synchronization to the shift clock is missing and the capture event will be triggered immediately. This results in incorrect data in the GPRn registers: a) captured time base values TBU_TS* show values inconsistent compared with word_time= shift_clock * (CNTS[7:0] + 1) b) capturing CNT register to GPR1 occurs to early, last sampled bit of word can be incorrect. Workaround : Use the external capture mechanism (signal tssm_ext_capture) with EXT_CAP_EN=1. Define with the counters in the TDU the shift clock and the external capture event. Ensure with the counter start conditions that the shift clock and the external capture event are not active in the same system clock.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-282	Title : TIM Serial shift mode TSSM EXT_CAP_EN=1: On occurrence of the capture condition CNTS[15:8]>=CNTS[7:0] no capture trigger (NEWVAL _IRQ) occurs and no data capture to the registers GPR0/1 will take place. Scope : TIM TSSM mode. Severity : Low Classification : Non-critical Effects : NEWVAL IRQ not occurring, capture to registers TIM[i]_CH[x]_GPRn does not occur. Description : If the setting EXT_CAP_EN=1 and TIM_MODE = 110 (TSSM) in register TIM[i]_CH[x]_CTRL is configured, 2 capture conditions are active: a) An event on the external capture mechanism (signal tssm_ext_capture) will start a capture. b) If the condition CNTS[15:8]=CNTS[7:0] is true a capture will be started. Due to this erratum the capture condition b) will never start a capture. Workaround : Use case: Capture 40 bits in 2 words with 16 bit and last word with 8 bit. With CNTS[7:0]=15 after 16 bits per word a capture shall be initiated. The end of the frame is generated in the TDU by counting the total amount of bits. Configuring TOV=49 will issue the external capture event for the last word. Workaround: Use only the external capture mechanism (signal tssm_ext_capture). This can be realized by setting up the counter in the TDU by writing register TOV=15. After the second capture reconfiguring the register TOV=7 will shorten the last word to 8 bits.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-283	Title : FIFO : Too short IRQ output length in IRQ level mode when hysteresis for direction read is enabled Scope : FIFO hysteresis read direction. Severity : Low Classification : Non-critical Effects : The IRQ output level is just set for one clock period and not held as expected. Description : If FIFO[i]_IRQ_MODE(z).IRQ_MODE is configured to level mode and FIFO[i]_IRQ_MODE(z).DMA_HYSTERESIS is enabled in DMA direction read mode (FIFO[i]_IRQ_MODE(z).DMA_HYST_DIR = 0), the IRQ output level is just set for one clock period and not held as expected in level mode. Workaround : If possible, do not use IRQ level mode when hysteresis is enabled in read direction. There are no known workaround if a IRQ level is needed e.g. to trigger a DMA controller.	v1.3 v1.4.0 v1.4.2 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-284	Title : TOM/ATOM : CCU0 interrupt at the wrong time in case of RST_CCU0=1 Scope : TOM/ATOM interrupt generation. Severity : Medium Classification : Non-critical Effects : CCU0 interrupt occurring at the wrong time. Description : If a TOM/ATOM channel is triggered from trigger chain TRIG_[x-1] or from TIM_EXT_CAPTURE(x) by setting of configuration bit RST_CCU0 = 1 (and ATOM has to be in SOMP mode), the CCU0 interrupt will be set at the end of the PWM period and not at the compare match of CN0 >= CM0. Workaround : Depending on application and available resources, several workarounds are imaginable : 1. Workaround (switching CM0 and CM1): If only the interrupt at the second signal change of the TOM/ATOM channel is needed, it is possible to switch the two compare values CM0 and CM1. Thereby the CCU1 interrupt happens at the second signal change and can be used instead of the CCU0 interrupt. As a side effect, the signal level will then be inverted, but this can be corrected by setting the corresponding configuration bit SL. 2. Workaround (usage of CM1 from triggering channel): If only one channel is triggered by a preceding channel, the first signal edge of the triggering channel can be used to generate the missing interrupt by setting CM1 of the triggering channel to the same value as CM0 of the channel which is triggered. 3. Workaround (DTM usage): If it is possible to use the TOM/ATOM output signal outside the GTM as the trigger event instead of the interrupt signal and if a DTM submodule is connected to the corresponding TOM/ATOM channel, the DTM functionality can be used to modify the output signal in the way, that a single pulse is formed at each signal edge.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-285	Title : TIM: Captured value in TIM[i]_CH[x]_GPR1 incorrect Scope : TIM Severity : Low Classification : Non-critical Effects : Captured value shows deviation by 1 to expected value. Description : If SWAP_CAPTURE=1 and GPR1_SEL=b11 and EGPR1_SEL=0 and TIM_MODE=0b000 or 0b001 is in use in TIM[i] channel [x] the captured value in TIM[i]_CH[x]_GPR1 is incorrect. Captured value deviates by 1. Workaround : Workaround: Compensate deviation in CPU or in MCS program by adding 1 to value read from TIM[i]_CH[x]_GPR1.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-287	Title : GTM_TOP level: AEI configuration interface using pipelined protocol in synchronous mode with write buffer enabled is not fully functional Scope : AEI pipelined protocol. Severity : Low Classification : Non-critical Effects : a) After writing GTM_BRIDGE_MODE= h#2 it can happen that the GTM Bus interface does not issue aei_ready which could lead to bus timeout of the serving bus master. b) Read accesses occurring after a write buffer full state could return incorrect data. Description : If the GTM bus bridge operates in BYPASS_SYNC=0, MSK_WR_RESP=1, BRG_MODE=0 mode and the AEI Pipelined protocol is in use correct functionality is not guaranteed. AEI split protocol is fully functional. Workaround : Workaround : Configure GTM_BRIDGE_MODE register to phase aligned mode(h#7) instead of sync mode. this setting will increase access latency by 1-2 aei_clk cycles.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-289	Title : GTM_TOP level: AEI configuration interface using standard protocol in synchronous mode with write buffer enabled may behave incorrect. A write transaction can be executed twice. Scope : AEI standard protocol. Severity : Medium Classification : Non-critical Effects : A write transaction is executed twice. Description : If the GTM bus bridge operates in BYPASS_SYNC=0, MSK_WR_RESP=1, BRG_MODE=0 mode and the AEI Standard protocol is in use the following situation may result in an incorrect behavior: If the write buffer is full (signaled with aei_free_buffer_cnt=0) and no new request is available (aei_sel=0) the actual write transaction scheduled out of the write buffer may be executed twice. AEI split protocol is fully functional. Workaround : In most situations a write which is executed twice will not influence the overall functionality. It has to be judged by the application if this may lead to an incorrect operation of the application. A twice write to registers like AFD*_CH*_BUF_ACC, *_IRQ_FORCINT, *_IRQ_NOTIFY, *TOM*_CH*_CN0,*TOM*_GLB_CTRL,*_RST will have a high probability that the application might operate incorrect. Workaround: Configure GTM_BRIDGE_MODE register to phase aligned mode(h#7) instead of sync mode.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-290	Title : GTM_TOP level: AEI configuration interface using pipelined protocol writing to GTM_BRIDGE_MODE not fully functional Scope : AEI pipelined protocol. Severity : Low Classification : Non-critical Effects : a) After writing the register GTM_BRIDGE_MODE with one of the defined sequences, it can happen that the GTM Bus interface does not issue aei_ready which could lead to bus timeout of the serving bus master. Description : If the AEI Pipelined protocol is in use, 2 consecutive writes to the register GTM_BRIDGE_MODE may fail: Faulty write sequences are: i) GTM_BRIDGE_MODE=h#3;GTM_BRIDGE_MODE=h#2 ii) GTM_BRIDGE_MODE=h#13;GTM_BRIDGE_MODE=h#2 AEI split and standard protocol is functional. Workaround : Workaround : a) Write with only one access: GTM_BRIDGE_MODE =h#2. b) Ensure that for the second write the bit BRG_RST is always written: i) GTM_BRIDGE_MODE=h#3; GTM_BRIDGE_MODE=h#10002, ii) GTM_BRIDGE_MODE=h#13; GTM_BRIDGE_MODE=h#10002.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-291	Title : MCS: bad value of register CTRG / MCS[i]_CTRG Scope : MCS Severity : Low Classification : Non-critical Effects : The read access to the register does not reflect the state of the bit fields TRGx with x = 16 to 23. Description : If the bit field EN_TIM_FOUT of register MCS[i]_CTRL_STAT is set, a read access to the bit fields 16 to 23 of register CTRG / MCS[i]_CTRG returns always 0. Workaround : Read the state of the bit fields TRGx with x = 16 to 23 with register STRG / MCS[i]_STRG.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-292	Title : DPLL: pulse correction at direction change incompletely for DPLL_CTRL_1.SMC='1'. Scope : DPLL Severity : Low Classification : Non-critical Effects : Under the assumption of DPLL_CTRL_1.SMC=1 the pulse correction at direction change is done incompletely such that some pulses may be not placed immediately after the direction change. Description : Under the assumption of DPLL_CTRL_1.SMC=1 the pulse correction at direction change is done incompletely such that some pulses may be not placed immediately after the direction change. Because the status of the register DPLL_INC_CNT1/2 for automatic end mode (DPLL_CTRL_1.DMO = 0) is correct the pulses can be placed for the next active input signal event. Workaround : 1) No action, wait for repeating missed pulses in automatic end mode at the next active input event. 2) V3.1.5: Observe DPLL_INC_CNT1/2 and do pulse correction (DPLL_CTRL_1.PCM1/2 under use of DPLL_CTRL_11.PCMF1/2 and pcmf1/2_inccnt_b) when DPLL activities due to pulse correction has finished.	v1.3 v1.4.0 v1.4.2 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-293	Title : MCS: Accessing MCS RAM while disabling last MCS channel fails. Scope : MCS RAM Severity : Low Classification : Non-critical Effects : In the case of a write access the data is not written to the RAM and in the case of the read access the read data is wrong. Description : If the CPU either wants to read or write data from an MCS RAM while the last MCS channel of the associated MCS is getting disabled by the MCS channel itself the memory access is failing. Last channel means that after disabling this channel no other channel of this MCS is enabled anymore. Workaround : Ensure that at least one MCS channel is running continuously on the MCS instance.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B8

Errata-ID	Errata	refer to
GTM-IP-294	Title : MCS Bus Master Interface: An access to the address range ADC_CH[0]_DATA to ADC_CH[31]_STA while a CPU access to an address in the same cluster is pending will block the MCS bus master interface forever Scope : MCS ADC interface. Severity : High Classification : Critical Effects : MCS channel program execution stops. PC is not incrementing. Description : If the CPU is executing a read or write access which is not serviced in the same cycle and the MCS issues via the bus master interface an access to the ADC-IF address range the bus master interface will block forever. ALL MCS channels which make use of the bus master interface will be affected. A CPU access which cannot be serviced in the same cycle can occur due to: 1. CPU access to RAM address range, 2. CPU access to registers AFD[i]_CH[j]_BUF_ACC, 3. CPU access to a register while actually the bus is in use by the bus master interface. Workaround : No workaround available.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5

Errata-ID	Errata	refer to
GTM-IP-295	Title : MCS[1:n] Bus Master Interface: If the buffer of the bus master interface is full and new accesses are scheduled by other MCS channels the MCS bus master interface will block forever Scope : MCS bus master interface. Severity : High Classification : Critical Effects : MCS channel program execution stops. PC is not incrementing. Description : If the buffer of the bus master interface is full, new scheduled accesses by the MCS are not serviced correctly, this leads to a blockage of the bus master interface. All MCS channels which make use of the bus master interface will be affected. How can the buffer reach the full state: If back2back accesses of multiple MCS channels occur where at least one cannot be executed in a single cycle. For example an access to register AFD[i]_CH[j]_BUF_ACC. Another scenario could be that a CPU access to an address which is not serviced in the same cycle (e.g. RAM address) can postpone the execution of scheduled bus master accesses and this leads to the buffer full state. Workaround : Workarounds 1.) Use MCS in cluster 0, faulty state can never occur due to buffer_depth=8 2.) All other clusters have implemented buffer_depth=2. Ensure that only 1 or 2 MCS channels are operating on the bus master interface, then the faulty state can never occur.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5

Errata-ID	Errata	refer to
GTM-IP-296	Title : DEBUG : Debug signals GTM_DBG_ARU_DATAi_val are not a one fast clock high level pulse Scope : DEBUG signal interface. Severity : Low Classification : Non-critical Effects : Sampling one debug data GTM_DBG_ARU_DATAi_H/L twice or more by the debugger logic. Description : 1.) Depending on the clock configuration of cluster 0 (GTM_CLS_CLK_CFG(1:0)) the length of the ARU debug signal GTM_DBG_ARU_DATAi_val can be one or two cycle related to the fast input clock. If the clock divider of cluster 0 (GTM_CLS_CLK_CFG(1:0)) is configured to two, the signal GTM_DBG_ARU_DATAi_val is a one cycle high level pulse related to the fast input clock. If the clock divider of cluster 0 (GTM_CLS_CLK_CFG(1:0)) is configured to one, the signal GTM_DBG_ARU_DATAi_val is a two cycle high level pulse related to the fast input clock. 2.) If ARU dynamic routing feature is in use it could happen, that a ARU CADDR is hold stable over two or more ARU clock cycles. If a valid debug information is presented on the debug bus at this point in time, the debug signal GTM_DBG_ARU_DATAi_val could be active for two clock cycles of the slow clock, while internal one data transfer is executed only. Workaround : 1.) Do not strobe the debug signal GTM_DBG_ARU_DATAi_val generated from slow cluster clock with the fast clock but with the by two divided fast clock. 2.) Independently of the length from GTM_DBG_ARU_DATAi_val, the high level of this signal always signalize exactly one valid debug pattern on the debug bus. Back-to-back transfers of debug data on the debug bus is not possible. Before the next debug pattern is presented on the debug bus, GTM_DBG_ARU_DATAi_val will drop to low level. The debag data should therefore only be captured on the raising edge of GTM_DBG_ARU_DATAi_val and not every cycle GTM_DBG_ARU_DATAi_val is active.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.5.0-A0

Errata-ID	Errata	refer to
GTM-IP-298	Title : TOM/ATOM: wrong output behavior in SOMP oneshot mode when oneshot pulse is triggered by TIM_EXT_CAPTURE(x) Scope : TOM/ATOM SOMP oneshot mode. Severity : Low Classification : Non-critical Effects : The TOM/ATOM output is set immediately to SL and not as expected with a delay of the first initial oneshot period. Description : If TOM/ATOM is configured in SOMP oneshot mode (OSM = 1) and the oneshot trigger is configured to TIM_EXT_CAPTURE(x) (OSM_TRIG = 1, EXT_TRIG = 1) the output behavior is not as expected depending on the selected CMU clock. 1. If the selected CMU clock is configured to sys_clk (ATOM : CMU_CLK_[z]_CTRL = 0, TOM : CMU_FXCLK0 used) no initial oneshot period (CN0 is set to zero and then counts until CN0 >= CM0) is executed and the output is set to SL immediately and not as expected after the first initial period. 2. If the selected CMU clock is configured to CMU_CLK_[z]_CTRL > 0 (ATOM)/CMU_FXCLK[1..n] (TOM) then an initial period is executed but the output is set immediately to SL and not as expected when the second oneshot period starts. Workaround : For GTM generation v3 following workaround is possible : Use up/down counter mode (UDMODE > 0) instead of up counter mode (UDMODE = 0). It has to be taken into account that in up/down counter mode the oneshot cycles ends if the counter CN0 counts down and value zero is reached. A second trigger of TIM_EXT_CAPTURE(x) in the up counting phase will be ignored but a second trigger while the counter CN0 counts down will trigger the next oneshot cycle, which will be executed directly afterwards without the initial period. For GTM generation v2 no workaround available because up/down counter mode is not available. If it is possible configure the selected CMU clock to sys_clk period. Then the generated oneshot pulse length is correct but without executing of the initial period.	v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.5.0-A0

Errata-ID	Errata	refer to
GTM-IP-299	Title : TOM/ATOM: wrong output behavior in SOMP oneshot mode when oneshot pulse is triggered by trig_[x-1] Scope : TOM/ATOM SOMP oneshot mode. Severity : Low Classification : Non-critical Effects : The TOM/ATOM output is set immediately to SL and not as expected with a delay of the first initial oneshot period. Description : If TOM/ATOM is configured in SOMP oneshot mode (OSM = 1) and the oneshot trigger is configured to trigger signal from trigger chain trig_[x-1] (OSM_TRIG = 1, EXT_TRIG = 0) the output signal is set immediately to SL and not as expected after a delay of the first initial oneshot period (CN0 counts from 0 until it reaches the value of CM0). The first initial oneshot period isn't executed. Workaround : For GTM generation v3 and later following workaround is possible : Use up/down counter mode (UDMODE > 0) instead of up counter mode (UDMODE = 0). It has to be taken into account that in up/down counter mode the oneshot cycles ends if the counter CN0 counts down and value zero is reached. A second trigger of from trigger chain by trig_[x-1] in the up counting phase will be ignored but a second trigger while the counter CN0 counts down will trigger the next oneshot cycle, which will be executed directly afterwards without the initial period. For GTM generation v2 no workaround available because up/down counter mode is not available. If it is possible work without the initial period for GTM generation v2 because the generated pulse length is correct.	v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.5.0-A0

Errata-ID	Errata	refer to
GTM-IP-300	Title : DPLL: Change to forward operation when DPLL_THMI is set to zero does not work correctly. Scope : DPLL Severity : Medium Classification : Non-critical Effects : DPLL direction does not change to forward (BWD1=0) if DPLL_THMI is set to 0. The current status of the direction is hold that means in case of BWD1=0 the direction will stay in forward (BWD1=0), in case of BWD1=1 the direction stays at backward (BWD1=1). Description : If direction control is set up via the TRIGGER input signal (DPLL_CTRL_1.IDDS=0, DPLL_CTRL_1.SMC=0) and DPLL_THMI is set to zero the direction does not change to forward (BWD1=0) when the current direction is backward (BWD1=1). Instead, when DPLL_THMI=0, the direction set latest is hold. Workaround : DPLL_CTRL_1.IDDS=0: If the DPLL is operating in forward direction (BWD1=0) the direction can be kept by setting DPLL_THMI=0. If the DPLL is operating in backward direction the direction can be switched to forward by setting the DPLL_THMI value to the biggest possible value DPLL_THMI=0x00FFFF. This should set the direction back to forward. Use different mechanism of direction control DPLL_CTRL_1.IDDS=1: In this case the direction can be controlled by setting the TIM0_IN6 input signal of the GTM when MAP_CTRL.TSEL=0. In both cases the direction evaluation is done with the inactive edge of the TRIGGER input signal. The TRIGGER input signal must be active even in emergency mode to handle the direction changes correctly. If the TRIGGER input signal is not in a usable condition the necessary input signal sequence can be generated by a direct modification of the input signal of TIM0_CH0 with the use of TIM[0]_IN_SRC.MAKE_0/VAL_0 and TIM[0]_CH[0]_ECTRL.USE_LUT(GTM v3.1.5 additionally).	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.5.0-A0

GTM-IP-301	Title : DPLL: Reset of DPLL_STATUS.BWD1=1 by disabling the DPLL does not cause the direction to change from backward to forward in any case. Scope : DPLL Severity : Medium Classification : Non-critical Effects : DPLL internal direction remains in current direction while DPLL_STATUS.BWD1 bit is reflecting it's reset value during a toggle sequence (1->0->1) of the DPLL enable bit DPLL_CTRL_1.DEN. After the end of the toggle sequence the BWD1 bit returns to the state of the current internal direction when the next active STATE input signal arrives. Description : The issue occurs when the DPLL is operating in normal mode (DPLL_CTRL_0.RMO=0, DPLL_CTRL_1.SMC=0) and the direction of the trigger signal is evaluated in the mode DPLL_CTRL_1.IDDS=0 (input direction is detected comparing the THMI value with the duration between active and inactive slope of TRIGGER). If in this configuration a direction change happens on the trigger signal which is not plausible, because the direction change happens due to e.g. a disturbed signal, the direction change performed by the DPLL should be removed. The direction in which the DPLL is operating can be read out by the status register DPLL_STATUS.BWD1. To disable the DPLL by setting DPLL_CTRL_1.DEN = 1->0->1 is resetting the BWD1 bit but this does not remove the direction change in every case and the BWD1 bit could be set to the unwanted direction again. The issue occurs when the DPLL has not received an active input signal on the STATE input such that DPLL_STATUS.fsd=0 before the DPLL is disabled (den=1->0->1) and switched to emergency mode (DPLL_CTRL_1.RMO=1). The issue does not occur if the DPLL is in the status of DPLL_STATUS.fsd=1 or if the DPLL is not switched to emergency mode (DPLL_CTRL_1.RMO=0) after the DPLL has been disabled/enabled. Workaround : If the issue occurs under the described conditions the wrong direction could be corrected by: 1) adding an additional input signal (active edge followed by inactive edge while not exceeding the THMI limit) to the trigger input which switches the DPLL back to forward direction. 2) Switching to the direction control mode DPLL_CTRL_1.IDDS=1 and to control the direction by setting the GTM input signal TIM0_IN6 to e.g. zero (forward direction). For combustion engine operation and MAP_CTRL.TSEL=0 the TDIR/SDIR signals can be used to control the direction with the TIM0_IN6 input signal. This TIM0_IN6 signal must be set directly on the GTM input pin by the mechanisms provided by the	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.5.0-A0

Errata-ID	Errata	refer to
	semiconductor supplier who integrated the GTM. This mechanism is bound to the resource of the TIM0_IN6 input channel.	

Errata-ID	Errata	refer to
GTM-IP-302	Title : DPLL: Pulse generation ongoing for DPLL_CTRL_1.DMO=1 (continuous mode) if DPLL_CTRL_1.sge1/2=0. Scope : DPLL Severity : Medium Classification : Non-critical Effects : pulse generator cannot be switched off by setting DPLL_CTRL_1.SGE1=0. Description : In continuous mode (DPLL_CTRL_1.DMO=1) the pulse generation cannot be switched off by setting DPLL_CTRL_1.SGE1/2=0. The pulse generation is ongoing independently from the chosen mode (DPLL_CTRL_0.RMO, DPLL_CTRL_1.SMC). Workaround : Set number of pulses to DPLL_CNT_NUM1/2 =0 to suppress pulse generation for DPLL_CTRL_1.DMO=1.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1

Errata-ID	Errata	refer to
GTM-IP-304	Title : MCS: Scheduling modes Single Prioritization and Multiple Prioritization are not functional Scope : MCS Severity : Medium Classification : Non-critical Effects : The program execution of a prioritized MCS channel can skip an instruction that is directly following a suspending instruction. Description : If an MCS instance is configured with the Single or Multiple Prioritization Scheduling mode and the last non-suspended and prioritized MCS channel (CLP) is entering its suspended state (which means that the MCS starts scheduling the remaining non-prioritized channels with accelerated scheduling scheme) and if the suspended state of CLP is resumed five clock cycles after it was entering the suspended state the MCS channel CLP is not executing the instruction that is following the suspending instruction. Workaround : Add an additional NOP instruction after all suspending instructions (WURM, WURMX, WURCX, WUCE, ARD, ARDI, NARD, NARDI, AWR, AWRI, BRD, BRDI, BWR, and BWRI) in a prioritized MCS program.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-305	Title : TIM Signal Generation with serial shift mode TSSM: If TSSM_OUT is used in channel x and channel x+1 uses edges of FOUT_PREV, these edges show an unexpected delay which lead to a delayed operation of channel measurement or TDU functionality of channel x+1 Scope : TIM TSSM mode. Severity : Low Classification : Non-critical Effects : Channel measurements or TDU functionality in channel x+1 triggered with unexpected delay. Description : If channel x operates in TSSM mode and signal generation is active with (CNTS[21:20]!=b00) and channel x+1 uses the signal edges from FOUT_PREV(x+1) a) for channel measurements with TIM[i]_CH[x+1]_ECTRL.USE_PREV_CH_IN=1 or b) inside the timeout detection unit with TIM[i]_CH[x+1]_ECTRL.USE_PREV_TDU_IN=1 The actions in TDU or channel measurement triggered by edges on FOUT_PREV(x+1) will occur with unexpected delay (delay correlates to shift clock in channel x). Workaround : Using the LUT in the filter unit in channel x+1 ensures that the signal edge information of FOUT_PREV(x+1) is reconstructed properly on F_OUT[x+1]. Use the following settings: TIM[i]_CH[x+1]_ECTRL.USE_LUT=b10; TIM[i]_CH[x+1]_TDUC.TO_CNT2=0xF0; TIM[i]_CH[x+1]_ECTRL.USE_PREV_CH_IN=0; TIM[i]_CH[x+1]_ECTRL.USE_PREV_TDU_IN=0.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.5.0-A0

Errata-ID	Errata	refer to
GTM-IP-306	Title : DPLL: DPLL_NUTC.syn_t_old, DPLL_NUSC.syn_s_old not updated according specification. Scope : DPLL Severity : Low Classification : Non-critical Effects : The registers bits DPLL_NUTC.syn_t_old are not updated with the previous value of DPLL_NUTC_syn_t but by the bits of the input data word. The registers bits DPLL_NUSC.syn_s_old are not updated with the previous value of DPLL_NUSC_syn_s but by the bits of the input data word. Description : The DPLL specification defines for DPLL_NUTC.WSYN=1 that an update of register DPLL_NUTC allows writing of the bits DPLL_NUTC.syn_t while DPLL_NUTC.syn_t_old inherits the previous value of DPLL_NUTC_syn_t. Differing from the specified behavior the actual hardware does not update the value of DPLL_NUTC.syn_t_old with the previous value of DPLL_NUTC.syn_t but instead updates DPLL_NUTC.syn_t_old according to the corresponding bits of the write operation executed by the CPU. The DPLL specification defines for DPLL_NUTC.WSYN=1 that an update of register DPLL_NUSC allows writing of the bits DPLL_NUSC.syn_s while DPLL_NUSC.syn_s_old inherits the previous value of DPLL_NUSC_syn_s. Differing from the specified behavior the actual hardware does not update the value of DPLL_NUSC.syn_s_old with the previous value of DPLL_NUSC.syn_s but instead updates DPLL_NUSC.syn_s_old according to the corresponding bits of the write operation executed by the CPU. Workaround : If the update of syn_t/s_old shall be done like described in the specification the register DPLL_NU(T/S)C.syn_t/s must be read first, then the DPLL_NU(T/S)C.syn_(t/s) can be used to modify the bits which are written to DPLL_NU(T/S)C.syn_(t/s)_old. As the current behavior of DPLL_NUT/SC.syn_s/t_old is in use by and can be advantageous for certain applications, there is no intend to change the current hardware behavior at this point in time. Instead a specification update to align the specification with the current hardware behavior is planned for future GTM generations.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-307	Title : IRQ: AEI_IM_ADDR is not set in GTM_IRQ_NOTIFY by AEI_WRITE or AEI_READ with status 0b10 if cluster 0 is disabled Scope : IRQ Severity : Low Classification : Non-critical Effects : an illegal address access is not supported by any irq signals. Description : bit 2 - AEI_IM_ADDR - in register GTM_IRQ_NOTIFY is not set if cluster 0 is disabled and - an AEI_WRITE or AEI_READ to a cluster 0 register is done - an AEI_WRITE to any enabled cluster register with responded status b#10 is done. Workaround : a) do not disabled cluster 0. b) cluster 0 is disabled; after each WRITE access check GTM_AEI_STA_XPT; if the read value is >0, it signs an access error. c) cluster 0 is disabled; do not read from cluster 0 register or any other disabled cluster register.	v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-308	Title : TIM, ARU : Limitation that back-to-back TIM data transfers at full ARU clock rate cannot be transferred correctly with ARU dynamic routing feature Scope : ARU Routing, DEBUG signal interface. Severity : Low Classification : Non-critical Effects : a) If the ARU CADDR is kept stable and data is transferred back-to-back for 2 or more consecutive aru clock cycles while operating in ARU dynamic routing mode, then every second data provided by the TIM module gets lost. b) Debugging of an ARU data transfer not completely correct. Every second GTM_DBG_ARU_DATAi_val signal missing. Description : If TIM input signals with signal changes faster or equal than ARU clock rate are processed with the TIM and the results are routed via ARU in dynamic routing mode, it is likely that there is a data loss and only each second data can be transferred. Workaround : Do not use the dynamic routing feature of ARU in the manner that the same ARU caddr is served for multiple cycles with back-to-back data transfers. Ensure that every ARU clock cycle the CADDR address will change.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-309	Title : TIM Signal Generation with serial shift mode TSSM in channel x: Generated TSSM_OUT signal used in lookup table of inputsrc module of channel x has unpredictable delay Scope : TIM TSSM mode. Severity : Low Classification : Non-critical Effects : Lookup table in TIM channel inputsrc module shows unexpected results. Description : If channel x operates in TSSM mode and signal generation is active with (CNTS[21:20]!=b00) and channel x uses the signal TSSM_OUT(x) in the lookup table with USE_LUT(x)=0b11. Results of lookup table function will behave unexpected due to delayed input of TSSM_OUT(x) (delay correlates to shift clock in channel x). Workaround : Use lookup table of inputsrc module channel x+1. The TSSM_OUT signal of channel x which is routed via FOUT_NEXT(x) to channel x+1 can be used with USE_LUT(x+1)=0b10.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.5.0-A0

Errata-ID	Errata	refer to
GTM-IP-312	Title : GTM Bus Bridge: Aborting an AEI access (AEI standard protocol) to the GTM while the buffer of the AEI bridge is full results in an unexpected behavior. Scope : AEI standard protocol. Severity : Low Classification : Non-critical Effects : a) Read access returns unexpected data. b) Blockage of configuration interface. Description : If the AEI bridge is configured to MSK_WR_RSP = 1 to operate with the transaction buffer, continuous accesses can fill up the transaction buffer. If the buffer is filled (aei_free_buffer_cnt=0) and a new access is performed it will be pending until aei_free_buffer_cnt /= 0. The AEI standard protocol allows to abort an access by aei_sel=0. If this is done while aei_free_buffer_cnt=0 the condition for the unexpected behavior is valid. Workaround : Ensure that an access will never be aborted when AEI buffer is full (aei_free_buffer_cnt=0).	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-316	Title : SW Reset not functional if cluster 0 is disabled Scope : SW Reset Severity : Low Classification : Non-critical Effects : Config variable global_reset_en_c = 1: if cluster 0 is disabled and a write to register GTM_RST is working SW gets no request. No soft reset is activated. Config variable global_reset_en_c = 0: if cluster 0 is disabled and a write with 0x1 to register GTM_RST is working SW gets no request. No soft reset is activated because soft reset is disabled by Config variable global_reset_en_c = 0. Description : SW could not write to GTM_RST if cluster 0 is disabled. The write access to GTM_RST by disabled cluster 0 gets no request. Workaround : Config variable global_reset_en_c = 1: a.) cluster 0 must be enabled for usage SW reset. b) Hardware reset for GTM must be activated. Config variable global_reset_en_c = 0: a write to GTM_RST.RST with '0' works well. Do not write '1' to GTM_RST.RST.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

GTM-IP-317	Title : DPLL: When DPLL_CTRL_0.RMO=0 and DPLL_CTRL_1.SMC=0: DPLL_STATUS.LOCK1 is set incorrectly when direction change, unexpected missing trigger or trigger out of range occurs. When DPLL_CTRL_0.RMO=1 and DPLL_CTRL_1.SMC=0:DPLL_STATUS.LOCK1 is set incorrectly when direction change, unexpected missing state or state out of range occurs. When DPLL_CTRL_0.RMO=1 and DPLL_CTRL_1.SMC=1:DPLL_STATUS.LOCK2 is set incorrectly when direction change, unexpected missing state or state out of range occurs. Scope : DPLL Severity : Low Classification : Non-critical Effects : For DPLL_CTRL_0.RMO=0 AND DPLL_CTRL_1.SMC=0: DPLL_STATUS.LOCK1 status flags operating incorrectly. If the DPLL_STATUS.LOCK1 flag is set incorrectly the DPLL_STATUS.itn flags could be set if additionally an unexpected missing trigger event would occur. For DPLL_CTRL_0.RMO=1 AND DPLL_CTRL_1.SMC=0: DPLL_STATUS.LOCK1 status flags operating incorrectly. If the DPLL_STATUS.LOCK1 flag is set incorrectly the DPLL_STATUS.isn flags could be set if additionally an unexpected missing state event would occur. For DPLL_CTRL_0.RMO=1 AND DPLL_CTRL_1.SMC=1: DPLL_STATUS.LOCK2 status flags operating incorrectly. If the DPLL_STATUS.LOCK2 flag is set incorrectly the DPLL_STATUS.isn flags could be set if additionally an unexpected missing state event would occur. Description : DPLL_CTRL_0.RMO=0 and DPLL_CTRL_1.SMC=0: When DPLL_STATUS.LOCK1=0 and a direction change, an input signal with unexpected missing trigger occurs or if an trigger out of range event occurs the DPLL_STATUS.LOCK1 flag is set after two subsequent missing trigger interrupts has happened. The correct behavior is that DPLL_STATUS.LOCK1 is set after two subsequent missing trigger interrupt in either the same direction or without an unexpected missing trigger (missing trigger interrupt and DPLL_STATUS.ITN=1) interrupt or an trigger out of range interrupt occurs in between. DPLL_CTRL_0.RMO=1 and DPLL_CTRL_1.SMC=0: When DPLL_STATUS.LOCK1=0 and a direction change, an input signal with unexpected missing state occurs or if an state out of range event occurs the DPLL_STATUS.LOCK1 flag is set after two subsequent missing state interrupts has happened. The correct behavior is that DPLL_STATUS.LOCK1 is set after two subsequent missing state interrupt in either the same direction or without an unexpected missing	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1

Errata-ID	Errata	refer to
	state (missing state interrupt and DPLL_STATUS.ISN=1) interrupt or an state out of range interrupt occurs in between. DPLL_CTRL_0.RMO=1 and DPLL_CTRL_1.SMC=1: When DPLL_STATUS.LOCK2=0 and a direction change, an input signal with unexpected missing state occurs or if an state out of range event occurs the DPLL_STATUS.LOCK2 flag is set after two subsequent missing state interrupts has happened. The correct behavior is that DPLL_STATUS.LOCK2 is set after two subsequent missing state interrupt in either the same direction or without an unexpected missing state (missing state interrupt and DPLL_STATUS.ISN=1) interrupt or an state out of range interrupt occurs in between. Workaround : For DPLL_CTRL_0.RMO=0 AND DPLL_CTRL_1.SMC=0: When DPLL_STATUS.LOCK1= 0 the status of unexpected missing trigger, direction change and trigger out of range must be monitored to make the decision if DPLL_STATUS.LOCK1 is set correctly or not. For this reason either the interrupts DPLL_IRQ_NOTIFY.MTI, CDTI, TORI or the signals DPLL_STATUS.BWD1, ITN, TOR should be evaluated. For DPLL_CTRL_0.RMO=1 AND DPLL_CTRL_1.SMC=0: When DPLL_STATUS.LOCK1= 0 the status of unexpected missing state, direction change and state out of range must be monitored to make the decision if DPLL_STATUS.LOCK1 is set correctly or not. For this reason either the interrupts DPLL_IRQ_NOTIFY.MSI, CDSI, SORI or the signals DPLL_STATUS.BWD1/, ISN, SOR should be evaluated. For DPLL_CTRL_0.RMO=1 AND DPLL_CTRL_1.SMC=1: When DPLL_STATUS.LOCK2=0 the status of unexpected missing state, direction change and state out of range must be monitored to make the decision if DPLL_STATUS.LOCK2 is set correctly or not. For this reason either the interrupts DPLL_IRQ_NOTIFY.MSI, CDSI, SORI or the signals DPLL_STATUS.BWD2, ISN, SOR should be evaluated.	

Errata-ID	Errata	refer to
GTM-IP-318	Title : MCS: NARD(I) instruction reports unexpected status STA.SAT Scope : MCS Severity : High Classification : Non-critical Effects : The available data from the ARU source is not sent via ARU. Description : If the bit field CFG_CLOCK_RATE of register CCM[i]_HW_CONF is set and an MCS runs on a cluster i while bit field CLS[i]_CLK_DIV of register GTM_CLS_CLK_CFG is set to 1, the execution of a NARD or NARDI instruction might signalize an unsuccessful data transfer (bit field SAT of internal MCS register STA is cleared) although the data source has data available for sending. The unexpected behavior depends on the current state of the internal ARU counter. Workaround : The workaround for standard ARU routing (ARU_CTRL.ARU_[k]_DYN_EN=0, with k=0 or k=1) is as follows: NARD instruction: Replace existing instruction NARD A, B, C by the sequence NARD A, B, 0x1FF NARD A, B, C NARDI instruction: Replace existing instruction NARDI A, B by the sequence NARD A, B, 0x1FF NARDI A, B	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-319	Title : (A)TOM: Unexpected (A)TOM_CCU1TCx_IRQ in up/down counter mode Scope : TOM/ATOM Severity : Low Classification : Non-critical Effects : Interrupt signal (A)TOM_CCU1TCx_IRQ is set unexpectedly. Description : If the up-down counter mode is activated (bit field UDMODE of register (A)TOM[i]_CH[x]_CTRL is set to a value greater than zero) and the interrupt (A)TOM_CCU1TCx_IRQ is enabled (bit field CCU1TC_IRQ_EN of register (A)TOM[i]_CH[x]_IRQ_EN is set), the interrupt signal (A)TOM_CCU1TCx_IRQ will be set unexpectedly direct after the interrupt (A)TOM_CCU0TCx_IRQ were set and indicates that the counter (A)TOM[i]_CH[x]_CN0 reaches (A)TOM[i]_CH[x]_CM0. Workaround : If the interrupt (A)TOM_CCU1TCx_IRQ is needed, it can be disabled by the first occurrence of itself and enabled again with the interrupt (A)TOM_CCU0TCx_IRQ. With the following occurrence of the interrupt (A)TOM_CCU1TCx_IRQ it will be disabled again and so on.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-320	Title : ATOM: Unexpected restart of a SOMS oneshot cycle while ATOM[i]_CH[x]_CM0 is zero Scope : ATOM Severity : Low Classification : Non-critical Effects : Restarting of a oneshot cycle starts immediately while ATOM[i]_CH[x]_CM0 is zero and a write access to ATOM[i]_CH[x]_SR0 is executed with a value unequal to zero. Description : If ATOM is set to SOMS oneshot mode (bit field MODE of ATOM[i]_CH[x]_CTRL is set to 0b11 and bit field OSM in register ATOM[i]_CH[x]_CTRL is set) a oneshot cycle is started immediately by writing a value unequal to zero to ATOM[i]_CH[x]_SR0 register while the value of ATOM[i]_CH[x]_CM0 register is zero. Workaround : Avoid value 0 in ATOM[i]_CH[x]_CM0 register if SOMS oneshot mode is enabled (bit field OSM in register ATOM[i]_CH[x]_CTRL).	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-321	Title : BRIDGE_MODE_WRDIS not functional if cluster 0 is disabled Scope : SW Reset Severity : Low Classification : Non-critical Effects : Config variable global_reset_en_c = 1: if cluster 0 is disabled and a write to register GTM_RST is working SW gets no response and bridge mode write is not disabled. Config variable global_reset_en_c = 0: if cluster 0 is disabled and a write to register GTM_RST with '1' to bit BRIDGE_MODE_WRDIS is working SW gets no response and bridge mode write is not disabled. Description : SW could not write to GTM_RST if cluster 0 is disabled. The write access to GTM_RST by disabled cluster 0 gets no response. Workaround : Config variable global_reset_en_c = 1: a.) cluster 0 must be enabled for usage bridge mode write disable Config variable global_reset_en_c = 0: a write to GTM_RST.BRIDGE_MODE_WRDIS works well by avoiding a write '1' to GTM_RST.RST.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-322	Title : DPLL: PSTC, PSSC not updated correctly after fast pulse correction completed (DPLL_CTRL1.PCM1/2 = 0). Scope : DPLL Severity : Low Classification : Non-critical Effects : After the pulse correction is performed the fields NMB_T/S_TAR are set to wrong values such that after a new input event the parameters PSTC/PSSC are not updated correctly. Incorrect PSTC/PSSC values are ending up in wrong NA[i] parameters. These wrong NA[i] values are leading to incorrect PMT calculations. The pulse generation itself (register DPLL_INC_CNT1/2 and the status of the angle clocks TBU_TS1/2) is correct and not affected by this issue. Description : When additional pulses are requested using DPLL_CTRL_11.PCMF1/2=1 AND PCMF1/2_INCCNT_B=0 the PSTC/PSSC parameters as well as NMB_T/S_TAR are not updated correctly, because either the amount of additional pulses (MPVAL1/2) are not incremented or NMB_T/S_TAR is set to a wrong value. Workaround : The process requesting the pulse correction has to be extended by the following sequence to avoid the described issue: 1) Read value of NMB_T/S_TAR before pulse correction is started. (To read the correct NMB_T/S_TAR or NMB_T/S_TAR_OLD value the signal DPLL_OSW.swon_t/s must be read. If swon_t=0 NMB_T/S_TAR_OLD must be read. If swon_t=1 NMB_T/S_TAR must be read) 2) Start pulse correction by setting DPLL_CTRL_1. PCM1/2 and wait until pulse correction is executed. (Monitor DPLL_CTRL_1.PCM1/2). 3) Read value of NMB_T/S_TAR/_OLD again and check if correct (The swon_t/s value should not have changed since NMB_T/S_TAR/_OLD was read so the same address (see 1.) has to be used). If incorrect overwrite with corrected value. Alternatively overwrite with correct value without checking. After the next following active input signal the PSTC/PSSC values are correct. Ideally the pulse correction/workaround should be applied for the TRIGGER input channel in between the inactive edge of the input signal and the next following active edge of the next input signal (TISI-Irq.). In this case it is guaranteed that the swon_t signal is not going to change. For better understanding of the workaround an application document is available (GTM_workaround_gtm_ip_322_PSTC.pdf).	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-323	Title : DPLL: Registers DPLL_NUTC.SYN_T and DPLL_NUSC.SYN_S are updated by the profile (ADT_T.NT/ADT_S.NS) before the DPLL is synchronized (DPLL_STATUS.SYT/S=0). Scope : DPLL Severity : Low Classification : Non-critical Effects : When the DPLL is enabled and before the DPLL is synchronized (by writing to the relevant pointers (DPLL_APT_2c/DPLL_APS_1C3) the DPLL_NUTC.SYN_T/DPLL_NUSC.SYN_S registers are unexpectedly updated by the profile. Because the SYN_T_OLD and SYN_S_OLD registers are updated by SYN_T, SYN_S they are affected as well. The DPLL internal processes of calculation of the number of micro ticks for the next increment is not affected by that bug. Description : The registers DPLL_NUTC.SYN_T and DPLL_NUSC.SYN_S as well as the corresponding *_OLD registers are updated unexpectedly by the profile (ADT_T.NT/ADT_S.NS) before the DPLL is synchronized (DPLL_STATUS.SYT/S=0). This is not a problem for the calculation of the number of pulses (nmb_t/s,..), due to the fact that the correct value of SYN_T/S for the internal use is determined by the signal DPLL_STATUS.SYT/S. The micro tick generation of the DPLL is not affected by this bug. This problem is only relevant if the SYN_T/S values are read from other consumers than the DPLL. Workaround : When DPLL_NUTC.SYN_T/_OLD, DPLL_NUSC_SYN_S/_OLD values are needed outside the DPLL it must be checked that the DPLL is already synchronized (DPLL_STATUS.SYT/SYS). When the relevant DPLL channel (TRIGGER/STATE) is not synchronized yet the SYN_T/S values should be taken into account as "1".	v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-324	Title : GTM Toplevel: GTM_HALT_ACTIVE signal incorrect Scope : GTM Toplevel Severity : Low Classification : Non-critical Effects : A write access to GTM_RST while GTM_HALT_REQ is active will execute the GTM reset immediately while the expected behavior would be that the reset will be executed after the GTM_HALT_REQ goes inactive. Therefore the output signal GTM_HALT_ACTIVE is reset while GTM_HALT_REQ is still active. Description : Output signal GTM_HALT_ACTIVE goes unexpectedly to zero while GTM_HALT_REQ is set to one and cluster 0 is disabled and a write access to GTM_RST is performed. This is a debug scenario only and not related to functional usage of the GTM. Workaround : Enable cluster 0 before setting of GTM_HALT_REQ.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

GTM-IP-325	Title : TIM: Bits ACB[2:1] lost on interface to ARU (always zero) Scope : TIM, ARU transfers Severity : High Classification : Critical Effects : ARU bits ACB[2:1] sent by TIM are always zero Description : In case of CFG_CLOCK_RATE=1 (see register CCM[i]_HW_CONF) some cluster can be configured to run with clock frequency of AEI_SYS_CLK (fast clusters) while the ARU always runs with frequency AEI_SYS_CLK/2 (half speed). For this configuration of a cluster running at AEI_SYS_CLK (fast cluster) also the TIM module in this cluster is running at AEI_SYS_CLK (fast speed). In this case and if a TIM channel is configured to send data to ARU (ARU_EN bit in TIM[i]_CH[x]_CTRL register), the bits ACB[2:1] will not be transferred with any ARU transfer request, they are always 0. Due to this any master receiving ARU data is not able to use the ACB bit information received from a fast running TIM. ACB[1]: additional ARU request event received while actual request not finished ACB[2]:Timeout event occurred Workaround : Workaround 1: For applications that are in a single cluster, use AEI communication (MCS-TIM) instead of ARU communication. Workaround 2: Use half clock rate for the cluster that contains the TIM module read out via ARU. Workaround 3: If the data from TIM channel should be routed over the ARU to the MCS module, then the MCS can read the information (TIM[i]_CH[x]_IRQ_NOTIFY[4:3]) directly over the AEI bus master interface instead of routing it through the ARU. Hint : For this workaround the TIM channel and the MCS channel have to be in the same cluster. Workaround 4: If the data from TIM channel should be routed over the ARU to the FIFO or BRC module, then the MCS can read the information	v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
	(TIM[i]_CH[x]_IRQ_NOTIFY[4:3]) directly over the AEI bus master interface and forward the data via its ARU interface to FIFO or BRC. Hint: For this workaround the TIM channel and the MCS channel have to be in the same cluster. Workaround 5: Depending on the application it might be possible by comparing the actual ARU data with the previous received ARU data to "reconstruct" the ACB bits [2:1].	

Errata-ID	Errata	refer to
GTM-IP-326	Title : TIM: ARU bit ACB[0] (signal level) incorrect in case a second ARU request occurs while the actual request is just acknowledged Scope : TIM, ARU transfers Severity : Low Classification : Non-critical Effects : ARU bit ACB[0] not consistent with data transferred in ARU data words Description : An issued ARU request will be served at least after the ARU round trip time. If one aei_sys_clk clock before the ARU request is acknowledged a new capture event occurs (overflow condition due to e.g. input change) the bit ACB[0] will not show the new value. The overflow bit ACB[1] and the ARU data words selected by (E)GPRy_SEL) will show the correct behavior only the ACB[0] will show the previous state. Workaround : Workaround 1: Ensure that events which trigger a ARU request occur with a greater timely distance than the ARU round trip time. Workaround 2: Use the signal level information embedded in the ARU data words (selectable by ECNT/TIM_INP_VAL). This data will show the correct signal level.	v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

GTM-IP-329	Title : Interference of MCS to AEI/ADC and CPU to AEI traffic within the same cluster could result in incorrect MCS program execution Scope : Usage of MCS AEI master port (AEI and ADC communication from MCS); MCS channel code execution; Dynamic usage of GTM_MCS_AEM_DIS Severity : High Classification : Critical Effects : Incorrect MCS channel code execution (skipping execution of instructions or repetitive execution of instructions) or processing of incorrect read data from AEI or ADC interface by MCS channel code. Description : Operations of the MCS via it's AEI master port on the AEI bus can be categorized into 3 different types of operations based on the response time required by an addressed resource to complete the operation on the bus. As operations from MCS to ADC are also handled via the MCS AEI master port, ADC operations are also relevant regarding the bus traffic scenarios. The vast majority of register accesses via AEI as well as ADC reads complete with zero wait states (N=0) on the AEI bus and fall into the first category. The second category is defined by register operations to a small set of special registers that require 1 wait cycle (N=1) on the AEI interface to complete while the third category covers AEI accesses to memories (e.g. DPLL memory, MCS memory or FIFO memory) as well as 2 special registers in MCS that require multiple wait cycles (N>1) on the AEI interface to complete. Certain interferences between accesses from MCS to the AEI/ADC interface and AEI accesses from CPU within the same cluster can result in bus traffic situations that impact the correct program execution of MCS channels. These rare but critical traffic conditions must be avoided to ensure the correct execution of MCS code. Further the dynamic usage of GTM_MCS_AEM_DIS to temporarily disable a MCS AEI master port (AEI and ADC communication path) must be avoided. This switch can only be used for the permanent disablement of the MCS AEI master port. MCS AEI master port usage scenarios proven to avoid the problematic traffic conditions under all circumstances include the usage scenarios described in the workaround section of this erratum. Usage of MCS to AEI or ADC communication not covered by tested scenarios must be avoided. Communication from MCS to any GTM resource via ARU is not impacted and has no influence on the problems and scenarios described within this erratum. GTM resources with 1 AEI wait cycle (N=1): GTM_RST GTM_CLS_CLK_CFG BRC_RST TIM[i]_RST TOM[i]_TGC0_GLB_CTRL TOM[i]_TGC1_GLB_CTRL	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
	DPLL_CTRL_1 ATOM[i]_AGC_GLB_CTRL GTM resources with more than 1 AEI wait cycle (N>1): AFD[i]_[0-7]_BUFF_ACC FIF0[i]_MEMORY RAM address space* DPLL_RAM1A RAM address space (DPLL_RR1) DPLL_RAM1B RAM address space (DPLL_RR1) DPLL_RAM1C RAM address space (DPLL_RR1) DPLL_RAM2 RAM address space (DPLL_RR2) MCS[i]_MEM RAM address space* MCS[i]_CTRG MCS[i]_STRG * Not accessible from MCS Workaround : To ensure that a correct execution of MCS channel code is not influenced by certain traffic scenarios on the MCS AEI/ADC bus master interface, only proven usage scenarios are allowed for MCS to AEI/ADC communication. The most common usage scenarios tested to be safe include: · Option 1: Limit the usage of the MCS AEI master port (ADC and AEI communication) to one MCS channel per MCS at a time. ARU communication is available for all MCS channels and there are no limitations for the CPU access path in this usage model. In case multiple MCS channels want to use the AEI master port for AEI or ADC communication, establish a mechanism that ensures that only one channel uses the AEI master at a time (e.g. exchange a token between channels or use trigger registers to hand over the AEI master port ownership between MCS channels). · Option 2: Limit the usage of the MCS AEI master port to ADC communication only. The usage of the MCS AEI master port for AEI communication must be avoided for all channels. ARU communication is available for all MCS channels and there are no limitations for the CPU access path in this usage model. · Option 3: Limit the usage of the MCS AEI master port to ADC as well as AEI communication with zero wait cycles (N=0) only. AEI communication from MCS to resources with N>0 must be avoided. Further the access from CPU to this cluster has to be limited to accesses with zero or one wait cycle (N=0 and N=1) only. Memories or registers with N>1 within the given clusters cannot be accessed by the CPU in this usage model. If the CPU has to access these resources in this cluster, the number of MCS threads using the MCS AEI master port to access AEI or ADC temporarily has to be limited to one thread while all other MCS threads accessing AEI or ADC have to be suspended while the CPU accesses N>1 resources.	

Errata-ID	Errata	refer to
GTM-IP-331	Title : GTM_TIM[i]_AUX_IN_SRC and GTM_EXT_CAP_EN_[i] register: wrong status 2 by AEI write access if cluster 0 is disabled Scope : Register access via legacy address Severity : Low Classification : Non-critical Effects : If status 2 is responded an interrupt bit in GTM_IRQ_NOTIFY is set and the write address will be caught in register GTM_AEI_STA_XPT. Any further AEI access with responded status >0 will not be caught in GTM_AEI_STA_XPT until GTM_AEI_STA_XPT is reset by AEI read to GTM_AEI_STA_XPT. Description : AEI write access to the register GTM_TIM[i]_AUX_IN_SRC and GTM_EXT_CAP_EN_[i] via the legacy address space responds with status 2 even though the write operation is correctly executed and the register contains the correct new value. Workaround : Do not use the legacy addresses of the listed registers while cluster 0 is disabled.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-332	Title : Access to registers GTM_TIM[i]_AUX_IN_SRC and GTM_EXT_CAP_EN_[i] via legacy address space: read data always 0 for AEI read access while cluster 0 is disabled Scope : Register access via legacy address Severity : Low Classification : Non-critical Effects : If cluster 0 is disabled, register data unequal to 0 would not be read from any register which is not part of a cluster (see list of impacted register sections)via its legacy address. Description : AEI read access to registers via legacy address space which are not in any cluster will respond always with read value 0 if cluster 0 is disabled. Impacted registers are: GTM_TIM[i]_AUX_IN_SRC GTM_EXT_CAP_EN_[i] Workaround : Do not access the impacted registers via their legacy address while cluster 0 is disabled.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-333	Title : MCS bus master interface: a not word aligned address access to DPLL ram region can cause incorrect execution of MCS channel code Scope : MCS bus interface; MCS program execution. Severity : Low Classification : Non-critical Effects : MCS channel program execution incorrect. Instructions might be executed multiple times or might be skipped. MCS BRD* instruction reads wrong data. Description : MCS accesses to the DPLL ram regions with not correctly aligned address while concurrently CPU accesses to the same cluster occur could result in incorrect execution of MCS channel code. Workaround : Ensure that address used in BWR* /BRD* instructions is correctly aligned.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-334	Title : DPLL RAM content of single address can be corrupted after leaving debug mode. Scope : GTM Debug Severity : Low Classification : Non-critical Effects : Data in RAM might be corrupted Description : Assume a MCS RAM write access to DPLL RAM address x in RAM1a, RAM1bc or RAM2 is executed at the point in time when the GTM is switched to debug mode (gtm_halt_req=1). Any following write access to DPLL address space while in debug mode will corrupt the data in memory location x when the restore operation which is executed while leaving debug mode (gtm_halt_req=0) is processed. Read operations to DPLL address space while in debug mode will not corrupt the DPLL memory content. Workaround : If only READ accesses to DPLL address space are performed while in debug mode the described effect will never occur. When write accesses to DPLL address space are performed while in debug mode the following workaround has to be considered: a) determine with the debugger whether a BWR instruction to DPLL RAM was executed just before the HALT occurred. b) The active address and the data of this instruction has to be written again with a debug access directly before leaving debug mode.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-335	Title : TOM output signal to SPE not functional if up/down counter mode is configured Scope : TOM - SPE interface Severity : Low Classification : Non-critical Effects : TOM output signal TOM[i]_CH[x]_SOUR to SPE not functional. Description : TOM output signal TOM[i]_CH[x]_SOUR to SPE not functional if up/down counter mode is configured by setting of TOM[i]_CH[x]_CTRL.UDMODE > 0. Workaround : No workaround available. Don't use up/down counter mode together with SPE interface.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

GTM-IP-336	Title : GTM Bus Bridge: Incorrect AEI access execution in case the previous AEI access was aborted with the access timeout abort function Scope : CPU interface accesses Severity : Low Classification : Non-critical Effects : Read access returns random data. Write access does not change the content of the target address. Description : In case the GTM internal AEI access timeout abort function is in use (GTM_CTRL.TO_VAL != 0 and GTM_CTRL.TO_MODE=1), a following AEI access can be corrupted: a) A write access might not be executed (register/ memory not written to the specified value) b) A read access can return random data (read value does not reflect the content of the addressed register / memory). Hint: As a timeout based abort of a GTM register access is assumed to be an error scenario, the internal state of the GTM might be exposed. To ensure the proper behavior after such an severe incident, the GTM IP should be re-initialized as part of a recovery action on system level. Workaround : Do not use the AEI access abort mode, use the observe mode instead (Set GTM_CTRL.TO_MODE=0). Enable additionally the timeout observe IRQ by setting GTM_IRQ_EN.AEI_TO_XPT_IRQ=1 to invoke higher level recovery mechanisms for GTM re-initialization. (e.g. abort the pending access to the GTM and reinitialize the GTM_IP from hardware reset).	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-339	Title : DPLL: Control bits DPLL_CTRL_11.PCMF1 and DPLL_CTRL_11.PCMF2 are not reset to 0 after a pulse correction is completed. Scope : DPLL Severity : Low Classification : Non-critical Effects : After a pulse correction is executed by writing to DPLL_CTRL_1.PCM1=1 and this signal is reset to 0 again, the signal DPLL_CTRL_11.PCMF1 is not reset back to 0. After a pulse correction is executed by writing to DPLL_CTRL_1.PCM2=1 and this signal is reset to 0 again, the signal DPLL_CTRL_11.PCMF2 is not reset back to 0. Description : In DPLL specification it is written in DPLL.12.40."When taken the MPVAL1 value to RPCUx and INC_CNT1 the PCM1 bit is reset immediately and after that also the PCMF1 bit. " The implemented behavior of the DPLL is that the PCMF1 bit is not reset after the PCM1 bit is reset to 0. In mode DPLL_CTRL_1.SMC=1, the same is true for the signal DPLL_CTRL_11.PCMF2. Workaround : Before a following pulse correction is executed this signal must be set to 0 again if needed. When a sequence of pulse corrections with the same configuration of DPLL_CTRL_11.PCMF1 or DPLL_CTRL_11.PCMF2 is executed no modification of DPLL_CTRL_11.PCMF1 or DPLL_CTRL_11.PCMF2 is necessary. When reset of DPLL_CTRL_11.PCMF1 or DPLL_CTRL_11.PCMF2 is needed this can be done by writing to register DPLL_CTRL_11.PCMF1/2.	v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

GTM-IP-340	Title : TOM/ATOM: Generation of TRIG_CCU0/TRIG_CCU1 trigger signals skipped in initial phase of A/TOM SOMP one-shot mode. Scope : TOM/ATOM Severity : Low Classification : Non-critical Effects : Missing TRIG_CCU0 and TRIG_CCU1 trigger signals in init phase of subsequent pulses in A/TOM one-shot mode, when one shot-mode is started with writing to CN0 values greater equal CM0-1 or CM1-1. Description : Configuration in use: A/TOM[i]_CH[x]_CTRL.OSM=1 A/TOM[i]_CH[x]_CTRL.OSM_TRIG=0 A/TOM[i]_CH[x]_CTRL.UDMODE=00 ATOM[i]_CH[x]_CTRL.MODE=10 Expected behavior: The generation of one-shot pulses in A/TOM can be initiated by a write to CN0. In this case the pulse generation comprises of an initial phase where the signal level at A/TOM output is inactive followed by a pulse. The duration of the initial phase can be controlled by the written value of CN0, where the duration is defined by CM0-CN0. After the counter CN0 reaches the value of CM0-1, the pulse starts with its active edge, CN0 is reset, and starts counting again. When CN0 reaches CM1-1, the inactive edge of the pulse occurs. Due to the fact, that the capture compare units CCU0 and CCU1 compare also in the initial phase of the pulse generation, the trigger conditions for these comparators apply also in this initial phase. Thus, the TRIG_CCU0 and TRIG_CCU1 signals also occur in the initial phase of the one-shot pulse. When these trigger signals are enabled in the A/TOM[i]_CH[x]_IRQ_EN, an interrupt signal is generated by A/TOM on the CCU0TC and CCU1TC trigger conditions and the corresponding A/TOM[i]_CH[x]_IRQ_NOTIFY bits are set. Observed behavior: For certain start values of CN0 and dependent on the history of pulse generation, the trigger signals TRIG_CCU0 and TRIG_CCU1 are skipped. As a consequence, this can led to missing interrupts CCU0TC and CCU1TC on behalf of their missing trigger signals TRIG_CCU0 and TRIG_CCU1. For the first pulse generation after enabling the channel, all trigger signals TRIG_CCU0 and TRIG_CCU1 appear as expected and described in the section expected behavior. If the channel stays enabled and a new value CN0 is written to trigger a subsequent one-shot pulse, the TRIG_CCU0/TRIG_CCU1 triggers in the initial phases of subsequent one-shot pulses are skipped under the following conditions:	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
	- For TRIG_CCU0 trigger: if the one-shot pulse is started by writing a value to CN0 greater or equal to CM0-1. - For TRIG_CCU1 trigger: if the one-shot pulse is started by writing a value to CN0 greater or equal to CM1-1. Workaround : 1. Workaround: Disabling, resetting (channel reset), initializing and re-enabling of the channel before starting the next one-shot pulse by writing of CN0 will ensure the correct behavior of CCU0TC and CCU1TC interrupt source. 2. Workaround: Starting a new one-shot pulse by writing twice the counter CN0 whereas the first value, which is written to CN0 should be zero followed by the value which defines the length of the initial phase. Be aware that in this case, the total length of the initial phase until the pulse is started, is influenced by the time between the two write accesses to CN0.	

GTM-IP-341	Title : TOM/ATOM: False generation of TRIG_CCU1 trigger signal in SOMP one-shot mode with OSM_TRIG=1 when CM1 is set to value 1. Scope : TOM/ATOM Severity : Low Classification : Non-critical Effects : Missing TRIG_CCU1 trigger signal in initial phase of the one-shot cycle and unexpected TRIG_CCU1 trigger signal at the end of the operation phase of the one-shot cycle. Description : Configuration in use: A/TOM[i]_CH[x]_CTRL.OSM=1 A/TOM[i]_CH[x]_CTRL.OSM_TRIG=1 A/TOM[i]_CH[x]_CTRL.UDMODE=00 ATOM[i]_CH[x]_CTRL.MODE=10 Expected behavior: The generation of one-shot pulses in A/TOM can be initiated by the trigger event TRIG_[x-1] from trigger chain or by TIM_EXT_CAPTURE(x) trigger event from TIM, whereas the counter CN0 is reset to zero and starts counting. In this case the pulse generation comprises of an initial phase where the signal level at A/TOM output is inactive followed by a pulse. The duration of the initial phase is always as long until the counter CN0 reaches CM0-1. After the counter CN0 reaches the value of CM0-1, the pulse starts with its active edge, CN0 is reset, and starts counting again. When CN0 reaches CM1-1, the inactive edge of the pulse occurs. Due to the fact, that the capture compare units CCU0 and CCU1 compare also in the initial phase of the pulse generation, the trigger conditions for these comparators apply also in this initial phase. Thus, the TRIG_CCU0 and TRIG_CCU1 signals also occur in the initial phase of the one-shot pulse. When these trigger signals are enabled in the A/TOM[i]_CH[x]_IRQ_EN, an interrupt signal is generated by A/TOM on the CCU0TC and CCU1TC trigger conditions and the corresponding A/TOM[i]_CH[x]_IRQ_NOTIFY bits are set. Observed behavior: If the compare register CM1 is set to 1 and a new one-shot pulse is triggered, two effects can be observed. - The first observed behavior is that the capture compare unit doesn't generate the TRIG_CCU1 trigger signal in the initial phase of the one-shot cycle. - The second observed behavior is that at the end of the operation phase of the one-shot cycle, where CN0 reaches CM0-1 a second time, the capture	v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
	compare unit generates a TRIG_CCU1 trigger signal which is not expected at this point in time. Workaround : Instead of using value 1 for CM1 it could be possible to generate the same pulse length by using a higher CMU_FXCLK/CMU_CLK frequency. Then, to get the same pulse length, the value of CM1 has to be multiplied by the difference of the two CMU_FXCLK/CMU_CLK frequencies. Be aware that this workaround is only possible, if you are not already using the CMU_FXCLK(0) because there is no higher CMU_FXCLK frequency to select. Example for TOM: Instead of using CMU_FXCLK(1), which has the divider value 2**4, use CMU_FXCLK(0), which has the divider value 2**0. In this case, CM1 has to be configured with value 2**4 minus 2**0 which is equal to 2**4=16. Hint: To get the same length of period, which defines the length of the initial phase, the value for the period in CM0 has to be multiplied by the same value. A second limitation is that the maximum length of the period, which is configured in CM0, is limited. Using a higher CMU_FXCLK/CMU_CLK frequency reduces the maximum possible period.	

Errata-ID	Errata	refer to
GTM-IP-342	Title : DPLL: Unwanted direction change when switching to emergency mode during active phase of TRIGGER input signal. Scope : DPLL Severity : Medium Classification : Non-critical Effects : By changing into the emergency mode the active direction is wrong. Description : When the DPLL is configured to DPLL_CTRL_1.IDDS=0 and the DPLL is switched to DPLL_CTRL_0.RMO=1 during the active phase of the TRIGGER input signal (timeframe between active and inactive input signal slope) and the TRIGGER input signal is causing a direction change, the direction status (DPLL_STATUS.BWD1) switches back to the former direction when the switch to emergency mode (RMO=1) is executed. Workaround : Don't change DPLL_CTRL_0.RMO when TRIGGER input signal is between active and inactive slope of input signal. A necessary switch to DPLL_CTRL_0.RMO=1/0 should be done only when the direction (DPLL_STATUS.BWD1) remains in a correct state. Hint: If the direction change is caused by a disturbed or incorrect input signal the direction change can be recovered by using the ATOM-TIM loopback to generate an additional input signal to the DPLL. This input signal sets back the direction indication within the DPLL to the correct value.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2

Errata-ID	Errata	refer to
GTM-IP-344	Title : DPLL: Incorrect AEI_STATUS on internal MCS2DPLL interface on valid and implemented address accesses Scope : DPLL, MCS0 Severity : Low Classification : Non-critical Effects : When the master interface of the MCS is accessing any address of the MCS2DPLL interface the DPLL always responds by setting the internal signal mcs_aeim_status = "0b11". When this happens the register CCM0_AEIM_STA is storing the mcs_aeim_status of "0b11" and additionally storing the address of the access. Whenever the MCS2DPLL interface is operating correctly it is not possible to check for invalid accesses under the described conditions. If the Register MCS[0]_CTRL_STAT.HLT_AEIM_ERR=0b1 the MCS0 channel which executed the bus master access is halted. Description : The status signal on the MCS2DPLL interface is always responding with "0b11" independent if an available or an unavailable address with correct byte alignment of that interface is accessed. Workaround : The register bit field MCS0_CTRL_STAT.HLT_AEIM_ERR must be set to "0b0" to prevent the MCS0 channels from halt. For the mcs_aeim_status there is no workaround possible. The master AEI interface of the MCS is operating correctly under the above configuration, but it is not possible to check for invalid address accesses via the CCM0_AEIM_STA register when the MCS is accessing any address of the MCS2DPLL interface.	v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-345	Title : SPE: Incorrect behavior of direction change control via SPE_CMD.SPE_CTRL_CMD bits Scope : SPE, TOM Severity : High Classification : Non-critical Effects : Modifying the direction bit ("00" <-> "01") in SPE_CTRL_CMD does not provide the correct output pattern to the BLDC motor. Due to a wrong pat_ptr position incorrect output patterns will be sent to the motor, which are not correlated to the sensor position In addition the SPE logic can generate unpredictable IRQs (perr_irq, dchg_irq, bis_irq) Description : A direction change ("00" <-> "01") via SPE_CTRL_CMD disturbs the increment/decrement of the pat_ptr resulting in incorrect output patterns not corresponding to the input pattern position. Changing the direction bit in SPE_CTRL_CMD can also generate invalid IRQs Workaround : Do not use SPE_CTRL_CMD. Instead reprogram the SPE_OUT_PAT register to change the direction.	v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

GTM-IP-346	Title : ATOM SOMS mode: Shift cycle is not executed correctly in case the reload condition is deactivated with ATOM[i]_AGC_GLB_CTRL.UPEN=0 Scope : ATOM Severity : Medium Classification : Non-critical Effects : After the counter CN0 reaches CM0 the output stays stable for two shift clock cycles before the next shift will be executed. Description : ATOM is configured to SOMS continuous mode by setting the following configuration bit fields: ATOM[i]_CH[x]_CTRL.MODE=11 ATOM[i]_CH[x]_CTRL.OSM=0 ATOM[i]_CH[x]_CTRL.ARU_EN=0 ATOM[i]_AGC_GLB_CTRL.UPEN[x]=0b00 Expected behavior: After the counter CN0 reaches CM0, no reload cycle is executed due to the configuration of UPEN=0b00. Instead of a reload cycle a shift cycle has to be executed to ensure an continuous shifting. Observed behavior: Neither a reload cycle nor a shift cycle is executed when the counter CN0 reaches CM0. The shifting stops and the shift register CM1 as well as the output ATOM[i]_CH[x]_OUT stays unexpectedly stable for two shift clock cycles whereas the counter CN0 continuously counting further on. Workaround : Increase the number of bits that have to be shifted out inside CM0 register to the maximum value of 23 to ensure an continuous shifting of all bits of the shift register CM1.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-347	Title : TOM/ATOM: Reset of (A)TOM[i]_CH[x]_CN0 with TIM_EXT_CAPTURE are not correctly synchronized to selected CMU_CLK/CMU_FXCLK Scope : ATOM, TOM Severity : High Classification : Non-critical Effects : The output signal (A)TOM[i]_CH[x]_OUT is not set correctly for the compare values 0 and 1 of the operation register bit fields (A)TOM[i]_CH[x]_CM1.CM1 and (A)TOM[i]_CH[x]_CM0.CM0. Description : To reset the counter (A)TOM[i]_CH[x]_CN0 (SOMP mode in ATOM), the input signal TIM_EXT_CAPTURE can be used by configuration of (A)TOM[i]_CH[x]_CTRL.EXT_TRIG=1 and (A)TOM[i]_CH[x]_CTRL.RST_CCU0=1. The reset of the counter (A)TOM[i]_CH[x]_CN0 should happen synchronously to the internal selected CMU clock CMU_CLK/CMU_FXCLK. Therefore a synchronization stage is implemented to synchronize the input signal TIM_EXT_CAPTURE to the internal selected CMU clock CMU_CLK/CMU_FXCLK. It can be observed, that the reset of the counter is done immediately with the occurrence of the input signal TIM_EXT_CAPTURE and not as expected synchronously to the selected CMU clock enable CMU_CLK/CMU_FXCLK. As a consequence of this, the output signal for the compare values 0 and 1 of (A)TOM[i]_CH[x]_CM1.CM1 and (A)TOM[i]_CH[x]_CM0.CM0 will not be set correctly. Workaround : 1. Workaround: Do not use clock dividing for the affected (A)TOM channels, so the undivided cluster clock is used. For this configure the control registers in the CMU and CCM to generate non-dividing CMU_FXCLK and/or CMU_CLK signals. Select within the (A)TOM the non-dividing CMU_FXCLK0 (for TOM) and/or CMU_CLK0..7 (for ATOM) via the settings for CLK_SRC in the (A)TOM[i]_CH[x]_CTRL register(s). 2. Workaround: Avoid the compare values 0 and 1 for the operation register bit fields (A)TOM[i]_CH[x]_CM1.CM1 and (A)TOM[i]_CH[x]_CM0.CM0.	v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-348	Title : DPLL: Correction of missing pulses delayed after start of pulse generation Scope : DPLL Severity : Low Classification : Non-critical Effects : When the pulse generation has been started by setting DPLL_CTRL_1.SGE1/2 and not all scheduled pulses could be generated there is no fast pulse correction after the second active input signal. Beyond that the DPLL internal pulse counter DPLL_INC_CNT1/2 is incremented correctly so that no pulse is getting lost. After the third input event the pulse correction is working as specified. Description : The described errata occurs in the DPLL configuration DPLL_CTRL_1.DMO=0 (Automatic end mode) and DPLL_CTRL_1.COA=0 (Fast pulse correction). When after the start of pulse generation (DPLL_CTRL_1.SGE1/2=0-->1) not all pulses scheduled could be generated, repeating the pulses at fast speed is not executed at the second TRIGGER/STATE input event. Workaround : 1) DPLL must be in direct load mode (DPLL_CTRL_1.DLM1/2 =1). Set DPLL_ADD_IN_LD1/2.ADD_IN_LD1/2=0 for the first two increments after the DPLL pulse generation has been started by DPLL_CTRL_1.SGE1/2=1 (all GTM Versions) 2) Do nothing: If there is no need to do the pulse correction for the second input signal after start of pulse generation. With the third input signal the pulse correction is starting to work. 3) Use pulse correction mechanism triggered by DPLL_CTRL_1.PCM1/2: a) Set DPLL_MPVAL1/2.MPVAL1/2 to the desired number of pulses which has to be sent out fast. b) Set DPLL_CTRL_11.PCMF1/2=1 AND DPLL_CTRL_11.PCMF1/2_INCCNT_B=1. c)Trigger the fast pulses by setting DPLL_CTRL_1.PCM1/2=1. This workaround is doable for all GTM Versions v3.1.5 and newer.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1

GTM-IP-349	Title : TOM-SPE: OSM-Pulse width triggered by SPE_NIPD for selected CMU_FXCLK not correct Scope : TOM, SPE Severity : Medium Classification : Non-critical Effects : The OSM-Pulse width triggered by SPE_NIPD are not correct. Description : The SPE_NIPD signal is used to reset TOM_CH_CN0 and to generate a one-shot pulse. When the CMU_FXCLK of the corresponding TOM_CH is set to a value unequal to 0, there are two effects observed: 1) the first pulse triggered by SPE_NIPD is generated with the CMU_FXCLK(0), while any subsequent pulses are generated with the configured CMU_FXCLK 2) the pulses generated with the correct CMU_FXCLK, show no determinism. Some pulses end with CCU_TRIG1, some with CCU_TRIG0. Workaround : Use SYS_CLK by selecting CMU_FXCLK(0) instead of a value unequal to zero for CMU_FXCLK. To reach the same pulse width on the output signal, the value for the period (TOM[i]_CH[x]_CM0.CM0) and duty cycle (TOM[i]_CH[x]_CM1.CM1) has to be scaled due to the relationship between SYS_CLK and the needed CMU_FXCLK.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

GTM-IP-350	Title : TOM-SPE: Update of SPE[i]_OUT_CTRL triggered by SPE_NIPD not working for a delay value 1 in TOM[i]_CH[x]_CM1 Scope : TOM, SPE Severity : Medium Classification : Non-critical Effects : The update of SPE_OUT_CTRL register is not executed. Description : When configured in one-shot mode some TOM channels can initiate a delayed change of register SPE_OUT_CTRL. The delay can be configured in TOM[i]_CH[x]_CM1 register of the corresponding TOM channel. Expected behavior: The SPE_OUT_CTRL register changed its content after a delay of CMU_FXCLK cycles which are configured in the TOM channel. For CM1=0, no update is expected, for CM1=1, the update is expected with the next CMU_FXCLK, for CM1=2, a delay of two CMU_FXCLK clock cycles is expected. Observed behavior: For CM1=1, there is no change of SPE_OUT_CTRL at all, independent of CMU_FXCLK. Workaround : Use SYS_CLK by selecting CMU_FXCLK(0) instead of a value unequal to zero for CMU_FXCLK. To get the trigger signal from TOM for the delayed update at the same time, the value for the period (TOM[i]_CH[x]_CM0.CM0) and duty cycle (TOM[i]_CH[x]_CM1.CM1) has to be scaled due to the relationship between SYS_CLK and the needed CMU_FXCLK.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-351	Title : MAP: Disable of input lines by MAP_CTRL register not implemented for input signals TSPP0 TIM0_CHx(48) (x=0..2) and TSPP1 TIM0_CHx(48) (x=3..5). Scope : MAP Severity : High Classification : Critical Effects : The specified disable function of the input signals TIM0_CH0(48), TIM0_CH1(48), TIM0_CH2(48) of TSPP0 submodule and the input signals TIM0_CH3(48), TIM0_CH4(48), TIM0_CH5(48) of TSPP1 submodule are not implemented, hence the input signals cannot be disabled. Description : The Control bits TSPP0_I0V, TSPP0_I1V, TSPP0_I2V, TSPP1_I0V, TSPP1_I1V, TSPP1_I2V of register MAP_CTRL are not operating as specified. The enable/disable functions of the input signals TIM0_CH0(48), TIM0_CH1(48), TIM0_CH2(48) of TSPP0 submodule and the input signals TIM0_CH3(48), TIM0_CH4(48), TIM0_CH5(48) of TSPP1 submodule are not implemented, hence the input signals cannot be disabled. Workaround : The combined TRIGGER or STATE output signals to the DPLL module can be disabled by using the control signals DPLL_CTRL_0.TEN(TRIGGER, TSPP0) and DPLL_CTRL_0.SEN (STATE, TSPP1). No workaround exists for switching off the level input signals of the TSPP0 and TSPP1 submodules individually.	v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

GTM-IP-352	Title : ATOM: Wrong reload of data from ARU in SOMS and SOMP mode if TIM_EXT_CAPTURE(x) or TRIGIN(x) is selected as clock source Scope : ATOM Severity : Medium Classification : Non-critical Effects : For the described modes the reloading and update of new values for the shadow registers from ARU is corrupted. In the SOMS one-shot mode the channel stops. Description : ATOM configuration: - SOMP or SOMS mode (ATOM[i]_CH[x]_CTRL.MODE=0b10/0b11) - ARU input stream enabled (ATOM[i]_CH[x]_CTRL.ARU_EN=1) - TRIGIN(x) or TIM_EXT_CAPTURE(x) as selected clock source (ATOM[i]_CH[x]_CTRL.CLK_SRC=0b1101/0b1110) Expected behavior in SOMS mode: ATOM Channel in SOMS mode shifts all data provided by ARU. Observed behavior in SOMS mode: An ARU read request is initiated and not cancelled after the first data was received from the ARU. The received data overwrites the previously received data in the ATOM[i]_CH[x]_SRy.SRy register (y=0,1). In SOMS continuous mode with ATOM[i]_CH[x]_CTRL.OSM=0, an update of the ATOM[i]_CH[x]_CMy.CMy register (y=0,1) from last received data in ATOM[i]_CH[x]_SRy.SRy register (y=0,1) is executed at the end of the period. In SOMS one-shot mode with ATOM[i]_CH[x]_CTRL.OSM=1, the ATOM channel stops after data is shifted out which was stored in shift register ATOM[i]_CH[x]_CM1.CM1 by the CPU. Data which was transferred via ARU stays in shadow register ATOM[i]_CH[x]_SR1.SR1 and will not be reloaded into the shift register; instead the channel stops. Expected behavior in SOMP continuous mode: Synchronized to the beginning of a new period ATOM Channel requests new data from ARU. The received values from ARU are stored into the shadow registers. If the actual period is ended the stored values are copied from the shadow registers into the operation registers for the new period. At the same time, a new read request to the ARU is started. Observed behavior in SOMP continuous mode: ATOM Channel requests new data from ARU without synchronization to the beginning of a new period. The received values are stored into the shadow registers and then copied directly into the operation registers. The next ARU read request is started immediately without synchronization to the actual period.	v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
	SOMP one-shot mode together with the reloading of values via the ARU is not supported and is therefore not affected by this ERRATUM. Workaround : If TIM_EXT_CAPTURE(x) is to be used as clock source, this can be configured within the CCM as clock source for one of the CMU clock sources. This clock source must then be selected in the ATOM itself. If TRIGIN(x) is to be used as clock source, the output signal of the ATOM channel, which delivers the trigger signal TRIGIN(x), can be routed to TIM input as AUX_IN signal. Now the TIM_EXT_CAPTURE(x) signal from this TIM module can be used with the same workaround as described before for TIM_EXT_CAPTURE(x) clock source. An additional clock delay of 3 cluster clocks would need to be considered for the generation of the TRIGIN(x) source.	

GTM-IP-353	Title : SPEC-ATOM: Specification of the smallest possible PWM Period in SOMP mode wrong, when ARU_EN=1 Scope : SPEC-ATOM Severity : High Classification : Non-critical Effects : When the ATOM channel operates in SOMP mode and receives updates of PWM period and/or duty cycle via ARU, new PWM period and/or duty cycle values get lost, when the PWM Period is smaller than the ARU round trip time plus one or two ARU clock cycles for the given microcontroller device the PWM Period runs on. Description : Configuration in use: ATOM[i]_CH[x]_CTRL.MODE=0b10 (SOMP), ATOM[i]_CH[x]_CTRL.ARU_EN=1, ATOM[i]_AGC_GLB_CTRL.UPEN_CTRLx=1 Functionality: When ATOM[i]_CH[x]_CTRL.ARU_EN=1 and ATOM[i]_AGC_GLB_CTRL.UPEN_CTRLx=1 the PWM period and duty cycle (PWM characteristic) can be reloaded via ARU in SOMP mode. The ATOM generates a PWM on the operation registers ATOM[i]_CH[x]_CM0.CM0 and ATOM[i]_CH[x]_CM1.CM1 while the new values received via ARU are stored in the shadow registers ATOM[i]_CH[x]_SR0.SR0 and ATOM[i]_CH[x]_SR1.SR1. Reloading of the ATOM[i]_CH[x]_CM0.CM0 and ATOM[i]_CH[x]_CM1.CM1 registers with the values from ATOM[i]_CH[x]_SR0.SR0 and ATOM[i]_CH[x]_SR1.SR1 takes place, when the old PWM period expires (ATOM[i]_CH[x]_CN0.CN0 reaches ATOM[i]_CH[x]_CM0.CM0 in up counter mode or ATOM[i]_CH[x]_CN0.CN0 reaches 0 in up/down counter mode). Therefore, it is important, that the new PWM characteristic is available in the shadow registers ATOM[i]_CH[x]_SR0.SR0 and ATOM[i]_CH[x]_SR1.SR1 before ATOM[i]_CH[x]_CN0.CN0 reaches ATOM[i]_CH[x]_CM0.CM0 (up counter mode) or 0 (up/down counter mode). Problem description: The GTM-IP specification defines as minimal possible PWM period, where the PWM characteristic can be reloaded in a predictable manner so that new data is always available in time at the ATOM channel, to be the ARU round trip time of the specific microcontroller device. This is not correct, because the data needs two additional ARU clock cycles to flow through the ARU from a source to the ATOM channel plus one clock cycle for loading the value from the shadow registers ATOM[i]_CH[x]_SR0.SR0 and ATOM[i]_CH[x]_SR1.SR1 to the registers ATOM[i]_CH[x]_CM0.CM0 and ATOM[i]_CH[x]_CM1.CM1. When the PWM period is smaller than the ARU round trip time plus three ARU clock cycles, the PWM output is not correct.	v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
	Workaround : Hint: The PWM period has to be larger than ARU round trip time + 3 ARU clock cycles. This can be reached by either choosing a smaller device, or by using ARU dynamic routing, or by reducing the value of ARU_CADDR_END to a value, which fits the PWM period. So, PWM period greater than ARU_CADDR_END + 1 + 3 ARU clock cycles.	

Errata-ID	Errata	refer to

GTM-IP-354	Title :
	MCS: Unresolved hazard resulting from RAW (Read After Write) dependency
	
	Scope :
	MCS
	
	Severity :
	Medium
	
	Classification :
	Non-critical
	
	Effects :
	The executed order of the program sequence is not as specified in the program code.
	
	Description :
	If an MCS instruction sequence has any RAW (read after write) data dependency, which involves one of the following SFRs mentioned below the read access is executed before the write access if the latency of these instructions is one or two clock cycles. The involved SFRs are: GMI0, GMI1, DSTA, DSTAX or AXIMI.
	
	Example: Assume that following sequence
	MOV GMI0, R0 // write GMI0
	MOV R1, GMI0 // read GMI0
	is executed in two subsequent clock cycles (w/o any additional wait cycles), read access of GMI0 is executed before the write access to GMI0.
	
	Workaround :
	Ensure that the delay between such RAW dependencies is always greater than 2 clock cycles. For example:
	
	1) Chose round robin scheduling mode in which that the situation will never occur.
	2) Reformulate the sequence in a way that there are at least two instructions between the critical RAW dependency. For example:
	MOV GMI0, R0
	NOP
	NOP
	MOV R1, GMI0
		v3.0.2-A1
		v3.0.3-A1
		v3.0.3-A2
		v3.0.4-A1
		v3.1.4-A0
		v3.1.5-A0
		v3.1.5-A1
		v3.1.5-A2
		v3.1.5-A3
		v3.1.5-A4
		v3.1.5-A5
		v3.1.5-A6
		v3.1.5-A7
		v3.1.5-A8
		v3.1.5-A9
		v3.1.5-AA
		v3.1.5-AB
		v3.1.5-AC
		v3.1.5-AD
		v3.1.5-AE
		v3.1.5-AF
		v3.1.5-B0
		v3.1.5-B1
		v3.1.5-B2
		v3.1.5-B3
		v3.1.5-B4
		v3.1.5-B5
		v3.1.5-B6
		v3.1.5-B7
		v3.1.5-B8
		v3.1.5-B9
		v3.1.5-BA
		v3.1.5-BB
		v3.1.5-BD
		v3.5.0-A0
		v3.5.0-A1
		v3.5.0-A2

Errata-ID	Errata	refer to

GTM-IP-355	Title :
	SPEC-(A)TOM: Missing description of (A)TOM output behavior for all possible SL and FREEZE Bit combinations
	
	Scope :
	TOM ATOM
	
	Severity :
	Low
	
	Classification :
	Non-critical
	
	Effects :
	The user is not aware of the different behavior of the affected outputs (A)TOM[i]_CH[x]_OUT in combination with SL and FREEZE bit combinations
	
	Description :
	The (A)TOM control register description lacks a description of the behavior of the output (A)TOM[i]_CH[x]_OUT for the different SL and FREEZE combinations together with internal ENDIS signal.
	
	The following description is missing for SL:
	Note:
	If (A)TOM[i]_CH[x]_CTRL.FREEZE=0 and the channel is disabled (ENDIS=0), the internal register SOUR inside (A)TOM sub unit SOU is set to the inverse value of (A)TOM[i]_CH[x]_CTRL.SL.
	By enabling the channel (ENDIS=1), the register SOUR is not changed. Thus, if the output is enabled afterwards (OUTEN=1), the output (A)TOM[i]_CH[x]_OUT is the inverse value of (A)TOM[i]_CH[x]_CTRL.SL.
	Note:
	If (A)TOM[i]_CH[x]_CTRL.FREEZE=1 and the channel is disabled (ENDIS=0), the output register of SOU unit is not changed and output (A)TOM[i]_CH[x]_OUT is not changed.
	
	Workaround :
	None
		v3.0.2-A1
		v3.0.3-A1
		v3.0.3-A2
		v3.0.4-A1
		v3.1.4-A0
		v3.1.5-A0
		v3.1.5-A1
		v3.1.5-A2
		v3.1.5-A3
		v3.1.5-A4
		v3.1.5-A5
		v3.1.5-A6
		v3.1.5-A7
		v3.1.5-A8
		v3.1.5-A9
		v3.1.5-AA
		v3.1.5-AB
		v3.1.5-AC
		v3.1.5-AD
		v3.1.5-AE
		v3.1.5-AF
		v3.1.5-B0
		v3.1.5-B1
		v3.1.5-B2
		v3.1.5-B3
		v3.1.5-B4
		v3.1.5-B5
		v3.1.5-B6
		v3.1.5-B7
		v3.1.5-B8
		v3.1.5-B9
		v3.1.5-BA
		v3.1.5-BB
		v3.1.5-BD
		v3.5.0-A0
		v3.5.0-A1
		v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-357	Title : MCS: instructions XCHB, SETB, and CLRB do not suppress register write Scope : MCS Severity : Low Classification : Non-critical Effects : If B[4:0] is greater than or equal to 24, unexpected write accesses to the referred SFR of A can occur. Description : According to the specification, the instructions XCHB CLRB, and SETB perform a specific bit operation on the B[4:0]-th bit of register A, but only if B[4:0] is less than 24. If B[4:0] is greater than or equal to 24, the content of A shall not be modified. However, the current RTL implementation of these instructions always read register A and it is always followed by a write back to register A, independently of the value B[4:0]. But the read content of A is only modified if B[4:0] is less than 24. Thus, the functional behavior of this implementation is correct in the case that A is a register which only has non-volatile register bits. However, if A is a register that has volatile bits, the result might also be modified if B[4:0] is greater than or equal to 24, since the write access to this register might modify its content. Workaround : MCS program must ensure that B[4:0] is always in the range of 0 to 23, at least if volatile SFRs are used as argument A in the instructions XCHB, SETB, or CLRB.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-358	Title : TOM/ATOM: Synchronous update of working register for RST_CCU0=1 and UDMODE=0b01 not correct Scope : TOM, ATOM Severity : Low Classification : Critical Effects : The synchronous update of the working register (A)TOM[i]_CH[x]_CM0 and (A)TOM[i]_CH[x]_CM1 is done unintendedly with the selected trigger signal TRIGIN[x] or TIM_EXT_CAPTURE. As a result, depending on the actual output level an edge to (A)TOM[i]_CH[x]_CTRL.SL could occur. Description : TOM/ATOM is configured in SOMP mode with ATOM[i]_CH[x]_CTRL.MODE="10" (only for ATOM) and up-down counter mode is enabled by setting of (A)TOM[i]_CH[x]_CTRL.UDMODE=0b01. With the additional configuration of (A)TOM[i]_CH[x]_CTRL.RST_CCU0=1, the counter direction from up to down is changed with the trigger signal from a preceding channel TRIGIN[x] or with the TIM_EXT_CAPTURE signal from TIM module. Expected behaviour: The synchronous update of the working registers (A)TOM[i]_CH[x]_CM0 and (A)TOM[i]_CH[x]_CM1 in this configuration shall be done only when the channel counter (A)TOM[i]_CH[x]_CN0 reaches zero. Observed behaviour: Additionally to the update of the working registers (A)TOM[i]_CH[x]_CM0 and (A)TOM[i]_CH[x]_CM1 when the channel counter (A)TOM[i]_CH[x]_CN0 reaches zero, the update is executed with the selected trigger signal TRIGIN[x] or TIM_EXT_CAPTURE(x). This is not expected in this configuration with (A)TOM[i]_CH[x]_CTRL.UDMODE=0b01. Workaround : For settings where the PWM phases are longer than the register access times on target system: Ensure to deliver new data to the associated shadow registers (A)TOM[i]_CH[x]_SR0 and (A)TOM[i]_CH[x]_SR1 only when the channel counter ATOM[i]_CH[x]_CN0 is in down counting phase. The down counting phase is reported by the according interrupt. The described workaround is only possible for ATOM as long as the ARU interface is disabled and the new shadow register values are delivered by configuration interface and not by ARU interface.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-359	Title : TOM: Both edges on TOM_OUT_T at unexpected times for RST_CCU0=1 and UDMODE>0 Scope : TOM Severity : Low Classification : Non-critical Effects : The second output signal TOM_OUT_T is set one CMU clock cycle too early in up-counting phase and one CMU clock cycle to late in down-counting phase. Description : TOM channel is configured in up-down counter mode by setting of TOM[i]_CH[x]_CTRL.UDMODE>0 and the channel is triggered by an preceding channel or by TIM_EXT_CAPTURE with configuration of TOM[i]_CH[x]_CTRL.RST_CCU0=1. Expected behaviour: In up-counting phase, the output signal TOM_OUT is set to SL when CN0 >= CM1 and the second output signal TOM_OUT_T has to be set to SL when CN0 >= CM0. In down-counting phase the output signals has to be set to !SL when CN0 < CM1/CM0. Observed behaviour: The second output signal TOM_OUT_T is set to SL in up counting phase when CN0 >= CM0 - 1, which is one CMU clock cycle to early. When the counter is counting down, the output signal TOM_OUT_T is set to !SL when CN0 < CM0 - 1, which is one CMU clock cycle too late. Workaround : The compare value TOM[i]_CH[x]_CM0 for the second output signal TOM_OUT_T has to be configured with a value, which is greater by one (CM0+1).	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-360	Title : SPEC-(A)TOM: PCM mode (BITREV=1) is only available for UDMODE=0 Scope : TOM, ATOM Severity : Low Classification : Non-critical Effects : The user is not aware that the combination of PCM mode together with up-down counting mode is not supported and may not be used. Description : If TOM/ATOM channel is configured in PCM mode with (A)TOM[i]_CH[x]_CTRL.BITREV=1, the channel may be configured in up-counting mode only with (A)TOM[i]_CH[x]_CTRL.UDMODE=0. Up-down counting mode ((A)TOM[i]_CH[x]_CTRL.UDMODE>0) is not supported for PCM mode. This limitation was added to the specification of GTM generation 4. Workaround : Do not use the combination of PCM mode together with up-down counting mode.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

GTM-IP-361	Title : IRQ: Missing pulse in single-pulse interrupt mode on simultaneous interrupt and clear event Scope : IRQ Severity : Medium Classification : Non-critical Effects : Missing pulse on interrupt signal IRQ_line. All modules, which deliver an interrupt signal and have more than one internal interrupt source which are ORed are affected. The only exceptions are the modules ARU and DPLL. Description : In single-pulse interrupt mode ([MODULE]_IRQ_MODE = 0b11) only the first interrupt event of the interrupt bits of the interrupt notify register inside this module generates a pulse on the output signal IRQ_line, if the associated interrupt is enabled ([MODULE]_IRQ_EN=1). All further interrupt events have no effect on the output signal IRQ_line until all enabled interrupts are cleared, except when an interrupt and a clear event (HW_clear or a SW_clear) occur at the same time. Expected behaviour: On simultaneous occurrence of an interrupt and clear event, a pulse on the output signal IRQ_line is generated. Observed behaviour: If the associated notify register bit of the interrupt event is not set and another bit of the same notify register is set and this interrupt is enabled, no pulse on the output signal IRQ_line is generated. All modules ([MODULE]) are affected by this ERRATUM, which are able to generate interrupts and which has multiple interrupt sources which are ORed to the output. Not affected are the modules DPLL and ARU. Workaround : On a SW clear prevent HW clear events and read the interrupt notify register to check on new interrupts without a received interrupt pulse on IRQ_line. In this case repeat the SW clear step to enable interrupt generation again. When disabling the HW clear is not an option refrain from using the single-pulse interrupt mode.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to

GTM-IP-362	Title :
	MCS: Using wrong WURM mask during execution of instruction WURMX or WURCX
	
	Scope :
	MCS
	
	Severity :
	High
	
	Classification :
	Non-critical
	
	Effects :
	WURMX or WURCX instruction is sensitive to the wrong volatile bit to be observed (e.g. interrupt or trigger bit) for one cluster clock cycle.
	
	Description :
	If a WURM mask defined in R6 for usage with the instruction WURMX or WURCX is updated exactly one clock cycle before the associated instruction is executed, the WURMX or WURCX instruction is using the old (not yet updated) value of R6 as WURM mask for exactly one cluster clock cycle.
	
	Example: Assume that the sequence
	MOVL R6, 0x2
	...
	MOVL R6, 0x1
	WURMX R0, STRG
	is executed with Accelerated Scheduling Mode and the scheduler does not apply any delay between both instructions, the WURMX instruction is using the old value 0x2 as WURM mask for the very first cluster clock cycle. In subsequent cluster clock cycles the correct value 0x2 is used as WURM mask.
	
	Workaround :
	Ensure that delay between update of the WURM mask R6 and its associated WURM instruction is greater than one cluster clock cycle. For example:
	1. Insert NOP instruction or another useful instruction between update of R6 and the associated WURMX or WURCX instruction.
	2. use Round Robin Scheduling Mode
		v3.0.2-A1
		v3.0.3-A1
		v3.0.3-A2
		v3.0.4-A1
		v3.1.4-A0
		v3.1.5-A0
		v3.1.5-A1
		v3.1.5-A2
		v3.1.5-A3
		v3.1.5-A4
		v3.1.5-A5
		v3.1.5-A6
		v3.1.5-A7
		v3.1.5-A8
		v3.1.5-A9
		v3.1.5-AA
		v3.1.5-AB
		v3.1.5-AC
		v3.1.5-AD
		v3.1.5-AE
		v3.1.5-AF
		v3.1.5-B0
		v3.1.5-B1
		v3.1.5-B2
		v3.1.5-B3
		v3.1.5-B4
		v3.1.5-B5
		v3.1.5-B6
		v3.1.5-B7
		v3.1.5-B8
		v3.1.5-B9
		v3.1.5-BA
		v3.1.5-BB
		v3.1.5-BD
		v3.5.0-A0
		v3.5.0-A1
		v3.5.0-A2
		v4.1.0-0A0
		v4.1.0-0A1
		v4.1.0-0A2

GTM-IP-364	Title : ATOM: ARU read request does not start at expected timepoint in UDMODE=1 and UDMODE=3 Scope : ATOM Severity : High Classification : Non-critical Effects : The effect depends on the UDMODE configuration: UDMODE=1: The remaining time, from starting a ARU read request until new data from ARU should be received is only half of the defined PWM period instead of the full PWM period. UDMODE=3: No new ARU read request is started when the counter CN0 changes the count direction from down to up and therefore no new data can be delivered in this case. Description : ATOM is configured in SOMP continuous up-down counter mode with UDMODE=1,3 and ARU interface is enabled by setting of ARU_EN=1. Expected behaviour: A new ARU read request has to be started always after the operation registers are updated from their shadow registers. This depends on the UDMODE configuration: UDMODE=1: new ARU read request after CN0 changes the count direction from down to up. UDMODE=2: new ARU read request after CN0 changes the count direction from up to down. UDMODE=3: new ARU read request in both cases Observed behaviour: A new ARU read request is always started when the counter CN0 changes the count direction from up to down, independently from UDMODE configuration. UDMODE=1: new ARU read request after CN0 changes the count direction from up to down. UDMODE=2: works as expected. UDMODE=3: new ARU read request after CN0 changes the count direction from up to down. Workaround :	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2

Errata-ID	Errata	refer to
	Workaround for UDMODE=1: The PWM period length in up-down counter mode has to be double the length as the ARU round trip cycle (plus 3 ARU clock cycles). Workaround for UDMODE=3: Use AEI interface for reloading new shadow register values instead of ARU.	

Errata-ID	Errata	refer to
GTM-IP-365	Title : ATOM: Changing ATOM[i]_CH[x]_CTRL_SOMP.SL via the ARU in SOMP continuous up-counting mode with UDMODE=0 not functional Scope : ATOM Severity : Medium Classification : Non-critical Effects : ATOM output signal ATOM_OUT is stuck at SL value as long as no new data is received via the ARU. Description : ATOM is configured in SOMP continuous up-counting mode by setting of UDMODE=0 and the ARU is enabled by setting of ARU_EN=1. Expected behaviour: It is possible to change ATOM[i]_CH[x]_CTRL_SOMP.SL synchronously to the PWM period via the ARU. If no new value is received via the ARU, the last received value via the ARU has to be taken into account. Observed behaviour: The new received value for ATOM[i]_CH[x]_CTRL_SOMP.SL via the ARU is taken into account for the following PWM period after the new value was received via the ARU as expected. However, if this value received via the ARU differs from the value configured in the ATOM[i]_CH[x]_CTRL_SR.SL_SR register and no new value for ATOM[i]_CH[x]_CTRL_SOMP.SL is received via the ARU within the next period, no further edge to the output signal ATOM_OUT is forced for the following periods as long as no new data is received via the ARU. Workaround : Limitation: The new ATOM[i]_CH[x]_CTRL_SOMP.SL value, which is send via the ARU should not differ from the value, which is configured inside ATOM[i]_CH[x]_CTRL_SR.SL_SR register. One possible workaround is to ensure that for each ATOM period a new value is delivered via the ARU.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2

Errata-ID	Errata	refer to
GTM-IP-367	Title : MCS: Instructions WURMX and WURCX implement invalid extended register set for argument A Scope : MCS Severity : Low Classification : Non-critical Effects : If the SW tool chain is expanding a '1' for the don't care bit at position 14, the WURMX and WURCX instruction will use a wrong register A. Description : Current implementation uses register set XOREG for the argument A of instructions WURMX and WURCX. However, the specification only allows the usage of the register set OREG, which is a subset of XOREG. In detail: the current implementation is evaluating a don't care bit of its instruction code (bit position 14) for determination of the register address A. Workaround : The SW tool chain must ensure that the unused don't care bits of these instructions are always expanded as '0'.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2

Errata-ID	Errata	refer to
GTM-IP-368	Title : MCS: Registers MCS[i]_HBP[h]_IRQ_MODE do not respect parameter IRQ_MODE_RST_VAL Scope : MCS Severity : Low Classification : Non-critical Effects : The reset value of the registers MCS[i]_HBP[h]_IRQ_MODE is 0x00000000. The reset value cannot be changed. Description : The parameter IRQ_MODE_RST_VAL defines the reset value of the IRQ mode registers. All IRQ mode registers of the GTM should respect this parameter. However, the registers MCS[i]_HBP[h]_IRQ_MODE do not respect this parameter. Workaround : The software must set the registers MCS[i]_HBP[h]_IRQ_MODE to the value of the parameter IRQ_MODE_RST_VAL during device initialization.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2

Errata-ID	Errata	refer to
GTM-IP-369	Title : MCS: Hardware Break Point IRQs are not cleared by write access to register MCS[i]_HBP[h]_IRQ_MODE Scope : MCS Severity : Low Classification : Non-critical Effects : The bitfields of registers MCS[i]_HBP[h]_IRQ_NOTIFY are not cleared by a write access to registers MCS[i]_HBP[h]_IRQ_MODE. Description : A write access to a register MCS[i]_HBP[h]_IRQ_MODE shall clear the associated IRQ notify bits of registers MCS[i]_HBP[h]_IRQ_NOTIFY. However, this functionality is not implemented. Workaround : The software must explicitly clear the registers MCS[i]_HBP[h]_IRQ_NOTIFY after a write access to MCS[i]_HBP[h]_IRQ_MODE.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2

GTM-IP-370	Title : TOM/ATOM: Unexpected reset of CN0 in up-down counter mode and CM0=2 Scope : TOM, ATOM Severity : Medium Classification : Non-critical Effects : Unexpected reset of the counter CN0. Description : TOM/ATOM is configured in SOMP mode with ATOM[i]_CH[x]_CTRL.MODE=0b10 (only for ATOM) and up-down counter mode is enabled by setting of (A)TOM[i]_CH[x]_CTRL.UDMODE != 0b00. Expected behaviour: In this case, the counter CN0 changes its count direction from up to down either until CN0 reaches CM0-1 for RST_CCU0=0 or with the selected trigger signal TRIGIN (EXT_TRIG=0) or EXT_TRIGIN (EXT_TRIG=1) for RST_CCU0=1. Observed behaviour: There are three different configuration scenarios, where the counter CN0 is unexpectedly reset. 1. In case of RST_CCU0=0: The period value inside CM0 is configured to 2 and then reconfigured to a value greater than 2. After the counter CN0 starts incrementing and reaches value 1, CN0 is once reset to 0 unexpectedly, before it starts incrementing again. 2. In case of RST_CCU0=1 and EXT_TRIG=0: The TRIGIN signal from a preceding channel is used to reset the count direction of CN0. After the period value CM0 of the preceding channel is reconfigured from value 2 to a greater value, CN0 of this channel, which is triggered by the preceding channel, is once reset to 0 similar to the first scenario, which happens in the preceding channel. 3. In case of RST_CCU0=1 and EXT_TRIG=1: The EXT_TRIGIN signal from TIM module is used to reset the count direction of CN0. If the EXT_TRIGIN signal occurs while the counter CN0 is incrementing and reaches the value 1, CN0 is once reset unexpectedly. However, there is already no deterministic dependency between the EXT_TRIGIN signal and the reset of CN0. Workaround : No workaround available. The following limitations have to be considered:	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2

Errata-ID	Errata	refer to
	For scenario 1 and 2: Do not use value 2 for the period, which is configured inside CM0. For scenario 3: Do not use EXT_TRIGIN as trigger signal to change the count direction in up-down counter mode.	

Errata-ID	Errata	refer to
GTM-IP-371	Title : MCS: Instruction MWRIL applies unexpected address offset calculation Scope : MCS Severity : Low Classification : Non-critical Effects : If the don't care bits 2 to 15 of the instruction code are set unequal to zero, a wrong address is calculated for the memory access. Description : The MCS instruction MWRIL applies an address offset calculation by evaluation of bits 2 to 15 of the corresponding instruction code, although these bits are defined as don't care bits. Workaround : Ensure that the don't care bits 2 to 15 of the instruction word are set to zero.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2

Errata-ID	Errata	refer to
GTM-IP-372	Title : MCS: Bad address overflow detection in Harvard architecture logic Scope : MCS Severity : Low Classification : Non-critical Effects : The timing for the execution of a RAM access is one instruction cycle longer than expected. Description : If a memory access by an instruction MWRI A, B, C or MRDI A, B, C is executed with a negative value for offset C, the Harvard logic detects an incorrect address overflow leading to the fact that the RAM accesses will be executed sequentially instead of parallel. The memory access is executed functionally correct but as a sequential access, which requires two instruction cycles instead of one instruction cycle. Workaround : Do not use a negative address offset as argument C.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2

Errata-ID	Errata	refer to
GTM-IP-373	Title : MCS: Invalid ECC Error Behavior during RAM write access Scope : MCS Severity : Low Classification : Non-critical Effects : Unexpected halt and ECC error signalization of an MCS channel. Description : If an MCS performs a parallel write access using the MCS Harvard architecture and the corresponding ECC error input signal (MCSi_RAMx_ECC_ERR) is set to high during the write access, the MCS signalizes this ECC error, which means that it stops the MCS channel, sets the error flag STA.ERR = 1 and updates the bitfield MCS[i]_CTRL_STAT.ERR_SRC_ID. However, the ECC error input signals should only be evaluated during read accesses (instruction fetch or data read) and it should be ignored during write accesses. Workaround : Ensure that the ECC input signal is zero during an MCS write access.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2

Errata-ID	Errata	refer to
GTM-IP-374	Title : SPEC-ATOM: Statement on timing of duty cycle output level change not correct for SOMP up/down-counter mode Scope : ATOM Severity : Low Classification : Non-critical Effects : When the ATOM channel is configured in SOMP up/down-counter mode, a change of bit ATOM[i]_CH[x]_CTRL.SL will be visible immediately after the value is written by software and not, as described in the specification, with the next compare match event of one of the CCUx compare units. Description : The duty cycle output level is determined by ATOM[i]_CH[x]_CTRL.SL bit. The specification describes in section “ATOM Signal output mode PWM (SOMP)”, that “the duty cycle output level can be changed during runtime by writing the new duty cycle level into SL bit of the channels configuration register”. Further, it is mentioned: “the new signal level becomes active for the next trigger CCU_TRIGx (since bit SL is written)”. However, the timing specification in the second part of the statement is only valid for the SOMP in up-counter mode. When the ATOM is configured in SOMP up/down-counter mode, the new signal level becomes immediately active, when the ATOM[i]_CH[x]_CTRL.SL bit is written. Workaround : No workaround for SOMP up/down-counter mode. Use SOMP up-counter mode, if update of SL-Bit needed during runtime.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-375	Title : ATOM: Data from ARU are read only once in SOMC mode even though ARU blocking mode is disabled while FREEZE=1 and ENDIS=0. Scope : ATOM Severity : Medium Classification : Non-critical Effects : In SOMC mode and activated FREEZE mode, reading new compare values stops after the first received data instead of continuing data reads. Description : ATOM is configured in SOMC mode and ARU input stream is enabled and ARU blocking mode is disabled. Configuration register setting: ATOM[i]_CH[x]_CTRL.MODE==0b01 (SOMC mode) ATOM[i]_CH[x]_CTRL.ARU_EN==0b1 (ARU input stream enabled) ATOM[i]_CH[x]_CTRL.ABM==0b0 (ARU blocking mode disabled) Expected behaviour: If the channel gets disabled while ATOM[i]_CH[x]_CTRL.FREEZE is set, a pending ARU read request will still be held active, even if the current request is served from ARU with valid data. This is the expected non-blocking behavior. Observed behaviour: If the channel gets disabled while ATOM[i]_CH[x]_CTRL.FREEZE is set and afterwards the ARU read request is served by an ARU read valid, the ARU read request is reset and no more data is requested from ARU interface. This corresponds to a blocking behavior. Workaround : Instead of using the ARU interface for reloading new compare values while the channel is in FREEZE mode, the configuration interface can be used to deliver the new compare values. If DPLL is used as data source for the ATOM compare values, a MCS channel has to be used to first read the data from DPLL by ARU interface and afterwards to write the data via MCS master interface to ATOM. The used MCS module has to be in the same cluster as the ATOM module.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2

Errata-ID	Errata	refer to
GTM-IP-376	Title : TOM/ATOM: Interrupt trigger signals CCU0TC_IRQ and CCU1TC_IRQ are delayed by one CMU_CLK period related to the output signals. Scope : ATOM, TOM Severity : Medium Classification : Critical Effects : Interrupt signals CCU0TC_IRQ and CCU1TC_IRQ are raised with a delay of one CMU_CLK period. Depending on the CMU_CLK period related to system frequency outside of GTM the this can be an issue or none at all. Description : Interrupt trigger signals CCU0TC_IRQ and CCU1TC_IRQ are delayed by one CMU_CLK period if the following configurations are used: 1. Both CCU0TC_IRQ and CCU1TC_IRQ are affected (ATOM: in SOMP mode) when the channel is configured in up-down counter mode ((A)TOM[i]_CH[x]_CTRL.UDMODE>0). 2. CCU1TC_IRQ only is affected (ATOM: in SOMP mode) when the channel is configured in up-counter mode ((A)TOM[i]_CH[x]_CTRL.UDMODE==0) and (A)TOM[i]_CH[x]_CTRL.SR0_TRIG is enabled. Workaround : No workaround available.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1

Errata-ID	Errata	refer to
GTM-IP-377	Title : AXIS responds with an error status if a write burst access is in progress with write strobes being all zero Scope : AXIS Severity : Low Classification : Critical Effects : Unexpected AXIS error response only. Probably an interrupt (GTM_AEI_IRQ) is set. Description : If during a data transfer of a write burst access all write strobe bits are set to 0x0 to prevent the actual writing to the specified address, then the GTM answers with an error status AXI SLVERR (0b10). But this special case to set all write strobes to zero during a data transfer of a burst access is allowed by AXI protocol. The GTM may not set any error status. Workaround : none	v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2

Errata-ID	Errata	refer to
GTM-IP-378	Title : AXIS response could be DECERR which is not expected for an AXIS slave component Scope : AXIS Severity : Low Classification : Non-critical Effects : Unexpected AXIS error response (DECERR) Description : For certain error cases the GTM responds with a DECERR (0b11). The AXI protocol defines DECERR as no slave available at the transaction address. Hence an AXI slave component must not respond with a DECERR error. Workaround : none	v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2

Errata-ID	Errata	refer to
GTM-IP-379	Title : GTM_AEI: "Abort once" function GTM_CTRL.TO_MODE="01" behaving as "Abort all" GTM_CTRL.TO_MODE="11" Scope : GTM_AEI Severity : Low Classification : Non-critical Effects : First timed-out access is aborted correctly. Subsequent timed-out accesses are aborted as well which is not compliant to the specification. Description : If GTM_CTRL.TO_MODE="01" (Abort once) is selected, the behavior is erroneously identical to the configuration of GTM_CTRL.TO_MODE="11" (Abort). Workaround : Use GTM_CTRL.TO_MODE="11" (Abort). In this case all the timed-out accesses are aborted; the first unresponsive address can be determined by reading out the GTM_AEI_ADDR_XPT register.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2

Errata-ID	Errata	refer to
GTM-IP-380	Title : (A)TOM: potentially wrong output signal in case of RST_CCU0=1 and CM0=1 on triggered channel in SOMP mode Scope : TOM, ATOM Severity : Low Classification : Non-critical Effects : For the configuration RST_CCU0=1 and CM0=1, CM0<CM1 no edge is generated for the first period, after CM0 is updated from SR0 with '1' and CM0>1 in the period before. Description : When the reset of (A)TOM_CHx_CN0 of a TOM or ATOM channel is triggered by a preceding channel or assigned TIM module (RST_CCU0=1) and the ATOM channel is configured in SOMP mode, the CM0 value defines the edge to SL and CM1 defines the edge to !SL. Expected behavior: When SR0 is configured to '1', and CM0 is updated with SR0=1 on trigger signal coming from previous channel, an edge to SL is expected, when CN0=CM0=1. Observed behavior: When CM0 is updated synchronously from SR0 for the next period, and CM0>1 at the actual period, no edge to SL is generated when CM0=CN0=1 for the first period after CM0=1 becomes active (was updated to CM0=1 from SR0). Workaround : In addition to configuring SR0=1 and letting the (A)TOM channel update CM0 with '1' at the start of the next period, a hot reconfiguration of CM0=1 can be done. However, the hot reconfiguration needs to be done after the edge to SL was performed in the actual period. Otherwise the CM0 value would be overwritten by '1' and the edge to SL would be generated immediately after hot reconfiguration and not at the intended old CM0 value. The workaround is applicable where the system can update the CM0 value in time; otherwise the setting of CM0=1 should not be used.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2

Errata-ID	Errata	refer to
GTM-IP-381	Title : (A)TOM: Changing the output signal level synchronously to the period by writing to (A)TOM[i]_CH[x]_CTRL_SR.SL_SR for 0% duty cycle with (A)TOM[i]_CH[x]_CM0.CM0=MAX+1 and (A)TOM[i]_CH[x]_CM1.CM1=0 and (A)TOM[i]_CH[x]_CTRL.RST_CCU0=1 not functional Scope : TOM, ATOM Severity : Medium Classification : Non-critical Effects : The output signal (A)TOM_OUT is not set to the inverse signal level, which is configured by writing to (A)TOM[i]_CH[x]_CTRL_SR.SL_SR. Description : (A)TOM channel is configured to be triggered by a preceding channel with (A)TOM[i]_CH[x]_CTRL.RST_CCU0=1. Additionally the channel is configured to 0 % duty cycle by setting of (A)TOM[i]_CH[x]_CM0.CM0=MAX+1 and (A)TOM[i]_CH[x]_CM1.CM1=0. In this case, the output signal (A)TOM_OUT is set to inverse signal level SL. Expected behaviour: By writing a value to (A)TOM[i]_CH[x]_CTRL_SR.SL_SR, the value of the output signal can be changed synchronously with the period. Observed behavior: Changing the signal level by writing a value to (A)TOM[i]_CH[x]_CTRL_SR.SL_SR is intermittent not taken into account in the next period on the output signal (A)TOM_OUT. Workaround : Changing the constant signal level of the output signal (A)TOM_OUT synchronously to the period can be achieved by configuring 100 % duty cycle with (A)TOM[i]_CH[x]_CM0.CM0=0 and (A)TOM[i]_CH[x]_CM1.CM1=MAX. In this case, the inverted signal level has to be written to (A)TOM[i]_CH[x]_CTRL_SR.SL_SR to reach the same constant output level on (A)TOM_OUT. A second workaround is to not change the value of (A)TOM[i]_CH[x]_CTRL_SR.SL_SR but to switch between 0 % duty cycle ((A)TOM[i]_CH[x]_CM0.CM0>MAX, (A)TOM[i]_CH[x]_CM1.CM1=0) and 100 % duty cycle ((A)TOM[i]_CH[x]_CM0.CM0=0, (A)TOM[i]_CH[x]_CM1.CM1=MAX) to get the required signal level on the output signal (A)TOM_OUT.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1

Errata-ID	Errata	refer to
GTM-IP-382	Title : TIO: Interrupts are not cleared by a write access to interrupt mode register Scope : TIO Severity : Low Classification : Non-critical Effects : The bitfields of registers TIO[i]_G[g]_CH[c]_IRQ_NOTIFY are not cleared by a write access to registers TIO[i]_G[g]_CH[c]_IRQ_MODE. Description : Hence a write access to a register TIO[i]_G[g]_CH[c]_IRQ_MODE shall clear the associated IRQ notify bits of registers TIO[i]_G[g]_CH[c]_IRQ_NOTIFY. However, this functionality is not implemented. Workaround : The software must reset the registers TIO[i]_G[g]_CH[c]_IRQ_NOTIFY manually after a write access to TIO[i]_G[g]_CH[c]_IRQ_MODE.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0

Errata-ID	Errata	refer to
GTM-IP-385	Title : AXIS: Bridge software reset initiated by writing BRIDGE_MODE.BRG_RST=1 will corrupt AXIS slave protocol Scope : AXIS, GTM_AEI Severity : Low Classification : Non-critical Effects : AXIS-Transaction is not terminated, protocol corrupted Description : Only Devices with AXIS interfaces are affected. The invocation of the AEI Bridge software reset (writing BRIDGE_MODE.BRG_RST=1), resets also the AXIS transaction ID. Due to this the GTM_AXIS module is unable to serve the response of this transfer. This AXIS transaction will not be terminated at all! Software reset is not allowed to reset the AXIS transaction IDs in the GTM_AEI write buffer. Workaround : Use asynchronous reset AXIS_ARESETN instead of writing BRIDGE_MODE.BRG_RST=1 (synchronous reset).	v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0

Errata-ID	Errata	refer to
GTM-IP-386	Title : ARU: Delivering data via ARU_ACCESS does not take into account the status of the ARU cluster isolation from the requesting module Scope : ARU Severity : Medium Classification : Non-critical Effects : ARU_ACCESS data will be delivered even though the ARU cluster isolation of the requesting module is active. Description : Via the ARU registers ARU_ACCESS, ARU_DATA_H and ARU_DATA_L it is possible to write (ARU_ACCESS.WREQ) or to read (ARU_ACCESS.RREQ) data to/from each module, which is connected to the ARU. If the ARU cluster isolation of the cluster from the requesting module is active by setting of GTM_ARU_COM_DIS(k)=1, the read or write request from ARU_ACCESS must not be served. This works correctly for the ARU_ACCESS read access but not for the write access. The write access will always deliver valid data and does not take into account the status of the cluster isolation from the requesting module. Workaround : Do not deliver data via the ARU registers ARU_ACCESS, ARU_DATA_H and ARU_DATA_L as long as the cluster of the addressed module (ARU_ACCESS.ADDR) is isolated (GTM_ARU_COM_DIS(k)=1).	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1

Errata-ID	Errata	refer to
GTM-IP-387	Title : DPLL: Wrong calculation of pulse generator frequency for DPLL_CTRL_0.AMT/S=1 and DPLL_CTRL_11.ADT/S=1 when number of pulses (DPLL_CTRL_0.MLT or DPLL_MLS1/2.MLS1/2) is too small. Scope : DPLL Severity : Medium Classification : Non-critical Effects : The frequency of the generated sub increment pulses of the DPLL is too small. This leads to an unbalanced generation of micro ticks. Description : When the number of pulses per increment DPLL_CTRL_0.MLT is smaller than 127, or DPLL_MLS1/2.MLS1/2 is smaller than 128 and the correction of physical deviations is used (DPLL_CTRL_0.AMT/AMS=1 and DPLL_CTRL_11.ADT/ADS=1), the calculation of internal values such as DPLL_DT_T/S_ACT.DT_T/S_ACT, DPLL_RDT_T/S_ACT.RDT_T/S_ACT, and DPLL_ADD_IN_CAL1/2.ADD_IN_CAL_1/2 is wrong. The resulting frequency of the generated sub increment pulses of the DPLL is too small. Workaround : 1) Don`t use pulse numbers DPLL_CTRL_0.MLT < 127 and/or DPLL_MLS1/2.MLS1/2 < 128, when using correction of physical deviation (DPLL_CTRL_11.ADT/ADS=1 when DPLL_CTRL_0.AMT/AMS=1). 2) When 1) cannot be applied use configuration DPLL_CTRL_11.ADT/ADS=0 when DPLL_CTRL_0.AMT/AMS=1 is used.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1

Errata-ID	Errata	refer to
GTM-IP-388	Title : GTM_AEI: write transaction in Split Mode to BRIDGE_MODE register (writing BRIDGE_MODE=h#10003) will probably never terminate Scope : GTM_AEI Severity : Low Classification : Non-critical Effects : AEI configuration interface will be blocked. Description : AEI Bridge is in async_bridge mode (BRIDGE_MODE.BRG_MODE='1'). Issuing an AEI Bridge software reset while switching to Mask write response mode through a split mode access (writing BRIDGE_MODE=h#10003) can under certain circumstances prevent the aei_response_ready-Signal from being set. The split transaction is therefore not properly terminated and the protocol is corrupted. Note: For Generation 3 and before the errata is not relevant because a programming sequence for register is mandatory ("Generic programing sequence for altering GTM_BRIDGE_MODE reg" from May 2017). Workaround : Issue the Reset in a separate transaction: Write BRIDGE_MODE=h#10001 then BRIDGE_MODE=h#3	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1

Errata-ID	Errata	refer to
GTM-IP-389	Title : DTM: HRES output calculation for short input pulses and enabled dead time incorrect Scope : DTM Severity : Medium Classification : Non-critical Effects : Value of output signal DTM_OUT0_HRES_[x]/DTM_OUT1_HRES_[x] not as expected. Description : DTM channel is configured for dead time calculation. High resolution PWM support is enabled. Configuration: CDTM[i]_DTM[d]_CH_CTRL2.DT[0/1]_[x]=1 CDTM[i]_DTM[d]_CH[x]_DTV.HRES=1 Expected behaviour: The HRES output value must be calculated correctly after three cluster clock cycles, even if the subsequent input edge on DTM_IN or DTM_IN_T or DTM_IN_PREV occurs after less than three cluster clocks. Observed behaviour: The calculated value of the HRES output signal for the current input signal edge is incorrect if the subsequent input signal edge on DTM_IN or DTM_IN_T or DTM_IN_PREV occurs after less than 3 cluster clock cycles. Workaround : Avoid pulses from connected module TOM, ATOM or TIO which are shorter than 3 cluster clock cycles together with enabled dead time calculation. No workaround available for shorter input pulses on DTM_IN or DTM_IN_T or DTM_IN_PREV.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1

Errata-ID	Errata	refer to
GTM-IP-390	Title : MCS-RTL: Invalid instruction trace output Scope : MCS Severity : Low Classification : Non-critical Effects : The concerned instruction is missing in the generated instruction trace. Description : The MCS instruction trace output does not signalize a WURM, WURMX or WURCX instruction, if the corresponding match event for that instruction occurs one cluster clock cycle after the MCS channel enters its suspended state. Workaround : none.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0

Errata-ID	Errata	refer to
GTM-IP-391	Title : MCS-RTL: Unexpected repeated break point action Scope : MCS Severity : Low Classification : Non-critical Effects : The MCS cannot resume from the corresponding suspended instruction by a simple write access to register MCS[i]_HBP[k]_STATUS. Description : After the MCS is getting resumed from an instruction break point that is configured at a memory location containing a suspending instruction (e.g. WURM), the MCS is executing the instruction at the break point correctly but without incrementing the Program Counter. Afterwards the instruction at the activated break point is executed again. Workaround : Disable the actual break point at MCS channel x by clearing the appropriate MCS[i]_HBP[k]_CTRL.EN_CH[x] first, and then resume the MCS channel x by a write access to MCS[i]_HBP[k]_STATUS.HALT_CH[x].	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0

Errata-ID	Errata	refer to
GTM-IP-392	Title : MCS-RTL: Potential unexpected write access before instruction break point Scope : MCS Severity : Medium Classification : Non-critical Effects : The MCS stops at the specified instruction break point as expected but the subsequent write access is executed, which is not expected. Description : If an MCS program sequence has an instruction break point activated there are two scenarios at which unexpected write accesses are executed: 1) A subsequent instruction is executing a parallel memory write exactly 2 cluster clock cycles after the instruction at the break point. 2) A subsequent instruction is executing an AEI bus master write access exactly 1 cluster clock cycle after the instruction at the break point. Note: This errata does not apply when the Round Robin scheduling mode is active. Workaround : Add one NOP (scenario 2) respectively two (scenario 1) NOP instructions between the instruction at the break point and the subsequent write access instructions.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0

Errata-ID	Errata	refer to
GTM-IP-393	Title : MCS-RTL: Potential invalid bit field STA.Z for parallel memory read access Scope : MCS Severity : Medium Classification : Non-critical Effects : Potentially unexpected value for flag STA.Z. Description : If a memory read instruction that is executing a parallel read access is followed by an instruction that is reading the STA register for the evaluation of the bit field STA.Z and the delay between both instructions is exactly one clock cycle, the bitfield STA.Z might reflect a wrong value. Note: This errata does not apply when the Round Robin scheduling mode is active. Workaround : 1) Re-schedule instruction sequence to avoid critical data dependency 2) Add one NOP instruction between the parallel memory read access instruction and the instruction that is reading the register STA.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0

Errata-ID	Errata	refer to
GTM-IP-394	Title : MCS-RTL: Potential wrong data for register MHB during parallel memory read access Scope : MCS Severity : Medium Classification : Non-critical Effects : Subsequent instruction is using invalid MHB data. Description : A memory read instruction is executing a parallel read access and the 8 LSBs of the read data are stored in the register MHB. The MCS reflects wrong data for the register MHB if one of the following scenarios about data dependencies to the subsequent instruction occurs: A) The subsequent instruction is reading the register MHB in any argument and the delay between both instructions is exactly two cluster clock cycles. B) The subsequent instruction is a parallel memory write instruction that is writing register MHB to the memory and the delay between both instructions is exactly three cluster clock cycles. C) The subsequent instruction is a parallel memory read or write instruction that is reading register MHB in any argument and the delay between both instructions is exactly three cluster clock cycles. Note: This errata does not apply when the Round Robin scheduling mode is active. Workaround : 1) Re-Schedule instruction sequence to avoid critical data dependency 2) Add two (for scenario A) or three (for scenario B and C) NOP instructions between the parallel memory read access instruction at the subsequent instruction that is reading the register MHB.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0

Errata-ID	Errata	refer to
GTM-IP-395	Title : GTM_AEI: Two consecutive Soft-Resets through Split-Mode make Bridge unresponsive Scope : GTM_AEI Severity : Medium Classification : Non-critical Effects : Communication with core is not possible anymore Description : Only devices with BRIDGE_BUFF_DPT = 1 (BRIDGE_MODE.BUFF_DPT='1') are affected. If two consecutively occurring Split-mode accesses write BRIDGE_MODE.BRG_RESET = '1', the bridge might become unresponsive. Workaround : Insert at least one other CPU access in between soft resets.	v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1

Errata-ID	Errata	refer to
GTM-IP-396	Title : GTM_AEI: After a software reset the AEI bridge might not execute an accepted transaction. Scope : GTM_AEI Severity : High Classification : Non-critical Effects : Write transaction is signaled to be successful without changing the value of the addressed register. Description : When the AEI Bridge operates in sync_bridge mode (BRIDGE_MODE.BRG_MODE = '0') or bypasses synchronizer flip-flops (BRIDGE_MODE.BYPASS_SYNC = '1') while a soft-reset is issued (writing BRIDGE_MODE.BRG_RST = '1'), an upcoming transaction might be accepted by the bridge but never actually executed. Note: For Generation 3 and before the errata is not relevant because a programming sequence for register is mandatory ("Generic programing sequence for altering GTM_BRIDGE_MODE reg" from May 2017). Workaround : 1) Switch to async_mode (BRIDGE_MODE.BRG_MODE = '1') and turn off bypassing synchronizer flip-flops (BRIDGE_MODE.BYPASS_SYNC = '0') before issuing a soft reset. OR 2) Issue always a read access directly after issuing a software reset.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1

Errata-ID	Errata	refer to
GTM-IP-397	Title : TOM-RTL: TOM_OUT is set with one clock cycle delay for SR0_TRIG=1 and consecutive values for SR0 and CM1 Scope : TOM Severity : Medium Classification : Critical Effects : The edge on the output signal TOM_OUT will be generated with one cycle delay of the selected clock by TOM[i]_CH[x]_CTRL.CLK_SRC related to the expected time when TOM[i]_CH[x]_CN0.CN0 matches with TOM[i]_CH[x]_CM1.CM1-1. Description : TOM channel is configured in continuous counting-up mode with TOM[i]_CH[x]_CTRL.RST_CCU0=0 and TOM[i]_CH[x]_CTRL.SR0_TRIG is enabled. If the registers TOM[i]_CH[x]_SR0.SR0 and TOM[i]_CH[x]_CM1.CM1 are configured with consecutive values (CM1=SR0+1), then the edge on the output signal TOM_OUT will be generated with one cycle delay of the selected clock by TOM[i]_CH[x]_CTRL.CLK_SRC related to the expected time when TOM[i]_CH[x]_CN0.CN0 matches with TOM[i]_CH[x]_CM1.CM1-1. Workaround : No workaround available except avoiding consecutive values for TOM[i]_CH[x]_SR0.SR0 and TOM[i]_CH[x]_CM1.CM1.	v4.1.0-0C0 v4.1.0-0C1

Errata-ID	Errata	refer to
GTM-IP-398	Title : DPLL: Incorrect DPLL_THVAL calculation leading to a false direction decision in case of tbu_ts0 wraps around Scope : DPLL Severity : High Classification : Non-critical Effects : Wrong value of DPLL_THVAL and false direction decision. Description : When a) the inactive edge of TRIGGER input signal is used for detection of the direction (DPLL_CTRL_1.IDDS=1) and b) the input delay information is used to correct time stamps (DPLL_CTRL_0.IDT=1) and c) in between the active input signal edge and the inactive input signal edge on TRIGGER tbu_ts0 wraps around, the calculation of DPLL_THVAL.THVAL is incorrect incurring a false direction decision. Workaround : Don't use DPLL_CTRL_0.IDT=1 when evaluating direction with DPLL_CTRL_1.IDDS=1.	v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1

Errata-ID	Errata	refer to
GTM-IP-399	Title : MCS-RTL: Potentially invalid MCS data trace output for parallel memory access. Scope : MCS Severity : Medium Classification : Non-critical Effects : MCS produces invalid data trace. Description : If an MCS instruction executes a parallel memory access and more than one MCS channel is active, the data trace interface potentially reports invalid data concerning the following information about the memory access instruction: - channel number - memory address - transferred data - data direction (read or write). Workaround : None.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1

Errata-ID	Errata	refer to
GTM-IP-400	Title : MCS-RTL: Division instruction may produce unexpected memory overflow and wrong results Scope : MCS Severity : Medium Classification : Non-critical Effects : An MCS channel stops with a memory overflow error and the calculated results of the division instruction are wrong. Description : Assume that a division instruction (DIVU or DIVS) is located in the MCS memory within the address range [MP1-4*6, ..., MP1-4]. If this instruction is executed with an Accelerated Scheduling Mode or a prioritized Scheduling Mode the associated MCS channel potentially stops its execution and signalizes a memory overflow. In this case the calculated results of the instruction are wrong. Workaround : Re-order program sequence in a way that any division instruction is located outside the critical address range [MP1-4*6, ..., MP1-4] of the MCS memory.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1

Errata-ID	Errata	refer to
GTM-IP-401	Title : MCS-RTL: Potential wrong data in memory during parallel memory write access while storing the register STA to memory Scope : MCS Severity : Medium Classification : Non-critical Effects : MCS writes wrong data of register STA to memory. Description : Assume that an MCS instruction executes a parallel memory access in order to write the register STA to the memory. If its preceding instruction is updating at least one of the following status flags: STA.CY, STA.Z, STA.N, STA.V, or STA.CWT and the delay between both instructions is exactly one cluster clock cycle potentially wrong data of the associated status flags are written to the memory. The content of the register STA itself remains correct. Note: This errata does not apply when the Round Robin scheduling mode is active. Workaround : 1) Re-schedule instruction sequence to avoid critical data dependency OR 2) Add one NOP instruction between the concerned memory write instruction and its predecessor instruction.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1

Errata-ID	Errata	refer to
GTM-IP-402	Title : GTM_AEI: Soft reset might not be triggered when issued through Pipeline-Mode Scope : GTM_AEI Severity : Medium Classification : Non-critical Effects : AEI Bridge will not be set into initial state. Description : A pipeline write access setting BRIDGE_MODE.BRG_RST to '1' might not trigger a soft-reset if the preceding transaction has already been in pipeline mode. Note: For Generation 3 and before the errata is not relevant because a programming sequence for register is mandatory ("Generic programing sequence for altering GTM_BRIDGE_MODE reg" from May 2017). Workaround : Integration dependent: 1) Issue the soft reset with a write command in any mode other than pipeline mode. OR 2) Issue a read transaction in standard mode before writing BRIDGE_MODE.BRG_RST in pipeline mode.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1

Errata-ID	Errata	refer to
GTM-IP-403	Title : MCS-RTL: Unexpected stack pointer decrement Scope : MCS Severity : Low Classification : Non-critical Effects : Unexpected content of stack pointer register R7. Description : If an RET or an POP instruction is executing a parallel data read access and an ECC error is signaled during the read access, the associated MCS channel signals the error correctly and it correctly stops the channel execution. However, the corresponding stack pointer register R7 is decremented, which is not expected during error handling. Workaround : None. Higher level error routines might have to consider the described deviation.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0

Errata-ID	Errata	refer to
GTM-IP-404	Title : MCS-RTL: Division instruction reports unrelated ECC error Scope : MCS Severity : Medium Classification : Non-critical Effects : Unexpected signaling of an ECC error. Description : If a sequential division instruction is executed at memory location x and a read access to a subsequent memory location x+y with 1 <= y <= 6 has an ECC error, the former instruction reports incorrectly an ECC error. Workaround : None.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0

Errata-ID	Errata	refer to
GTM-IP-405	Title : MCS Bus Master Interface: Any access to the reserved address space of the ADCIF, while the cluster is operating on GTM half clock, will afterwards block the ADCIF Scope : MCS, ADCIF Severity : Medium Classification : Non-critical Effects : Accesses to the ADCIF will not be performed. MCS reading from any ADCIF address of an unimplemented ADC channel will always receive data 0x80000000 (no new valid data available). MCS aei access status monitoring register CCM[i]_AEIM_STA indicates status 0x3 in the of address space of the ADCIF. Description : In case the cluster operates on GTM half clock, as soon as an MCS channel issues a read or write access to the reserved ADCIF address space (not implemented ADC channels), no subsequent ADCIF access (independently from which MCS channel) will be executed on the ADCIF. The reserved address space ranges from 0x5500 up to 0x55FF. In case of ADCIF read accesses, the received data will be 0x80000000 (no new valid data available). The MCS bus master interface will not be blocked, only the ADCIF will be blocked. Accesses to the addresses outside of the ADCIF address space will be executed as expected. Workaround : MCS code is expected to be developed in a way that no access to the reserved ADCIF address space (not implemented ADC channels) will occur.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1

Errata-ID	Errata	refer to
GTM-IP-406	Title : (A)TOM: FREEZE mode has no effect on (A)TOM_OUT_T in up-down counter mode with RST_CCU0=1 Scope : TOM, ATOM Severity : Medium Classification : Critical Effects : Output signal (A)TOM_OUT_T is set to inverse signal level (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL) and does not keep the value. Description : The channel is set into FREEZE mode while it is configured in up-down counter mode and triggered by a preceding channel or by TIM_EXT_CAPTURE. Configuration for TOM: TOM[i]_CH[x]_CTRL.UDMODE>0 TOM[i]_CH[x]_CTRL.RST_CCU0=1 TOM[i]_CH[x]_CTRL.FREEZE=1 (FREEZE mode) TOM[i]_TGC[g]_ENDIS_STAT.ENDIS_STAT=0 Configuration for ATOM: ATOM[i]_CH[x]_CTRL.MODE=0b10 (SOMP mode) ATOM[i]_CH[x]_CTRL.UDMODE>0 ATOM[i]_CH[x]_CTRL.RST_CCU0=1 ATOM[i]_CH[x]_CTRL.FREEZE=1 (FREEZE mode) ATOM[i]_AGC_ENDIS_STAT.ENDIS_STAT=0 Expected behaviour: In FREEZE mode when the channel is disable, it is expected that the output signal (A)TOM_OUT as well as (A)TOM_OUT_T has to keep its last value. Observed behaviour: In FREEZE mode when the channel is disable, the output signal (A)TOM_OUT_T is set to inverted signal level (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL) and does not keep its last value. Workaround : No workaround available.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0

Errata-ID	Errata	refer to
GTM-IP-407	Title : MCS-RTL: Unified error behavior Scope : MCS Severity : Low Classification : Non-critical Effects : MCS errors are signaled correctly, the associated MCS channel is stopped reliably but other registers associated with the erroneous instruction might change. Description : In order to provide a unified error behavior for the various types of MCS errors the GTM4.1 specification has been refined. In addition to the already existing error behavior (namely stopping the associated MCS channel [x], setting bit field STA.ERR and MCS[i]_ERR.ERR[x], and updating bit field MCS[i]_CTRL_STAT.ERR_SRC_ID) no other MCS registers or memory cells are updated. The listed GTM4.1 releases might not behave according to that new unified error behavior. This means for the case that an MCS instruction causes an error, additionally to the unified error behavior the state of the registers associated with the instruction causing the error may nevertheless change (e.g. the program counter could be incremented). Workaround : None.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1

GTM-IP-408	Title : (A)TOM-RTL: Missing edge on output signal (A)TOM_OUT when CN0 is reset with force update event Scope : TOM, ATOM Severity : Medium Classification : Critical Effects : Missing edge and false output signal level on (A)TOM_OUT Description : The channel is configured in continuous up-counter mode. Then a new period is started with a force update event and reset of CN0 is activated. Configuration for TOM: TOM[i]_CH[x]_CTRL.UDMODE=0 TOM[i]_TGC[g]_FUPD_CTRL.FUPD_CTRL[c]=0b10 TOM[i]_TGC[g]_FUPD_CTRL.RSTCN0_CH[c]=0b10 Configuration for ATOM: ATOM[i]_CH[x]_CTRL.MODE=0b10 (SOMP mode) ATOM[i]_CH[x]_CTRL.UDMODE=0 ATOM[i]_AGC_FUPD_CTRL.FUPD_CTRL[k]=0b10 ATOM[i]_AGC_FUPD_CTRL.RSTCN0_CH[k]=0b10 Expected behaviour: After the counter (A)TOM[i]_CH[x]_CN0.CN0 has been reset and therefore a new period has to be started and the output signal (A)TOM_OUT has to be set immediately to SL value (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL) and after the counter reaches (A)TOM[i]_CH[x]_CM1.CM1. an edge on (A)TOM_OUT to inverted SL value (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL) is expected. Observed behaviour: An edge on the output signal (A)TOM_OUT to SL value (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL) at the beginning of the new period does not happen. Instead, the output signal (A)TOM_OUT holds its last value. A second observation is in case of the SL value (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL) changes synchronously together with the force update event, an edge on (A)TOM_OUT to the inverted SL value (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL) when (A)TOM[i]_CH[x]_CN0.CN0 reaches (A)TOM[i]_CH[x]_CM1.CM1 does not happen. Workaround : No workaround available.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
		v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0

Errata-ID	Errata	refer to
GTM-IP-409	Title : DPLL: Flags of registers DPLL_STA_FLAG are not set Scope : DPLL, MCS Severity : Medium Classification : Non-critical Effects : The event represented by the flags will be missed and not set in the registers. This affects the DPLL_STA_FLAG register as well as the MCS register DSTAX with the bit fields: STA_FLAG_T, STA_FLAG_S, INC_CNT1_FLAG, INC_CNT2_FLAG. Description : The flags of register DPLL_STA_FLAG (STA_FLAG_T, STA_FLAG_S, INC_CNT1_FLAG, INC_CNT2_FLAG) are not set when one of these flags is cleared by a write operation of MCS register DSTAX (STA_FLAG_T, STA_FLAG_S, INC_CNT1_FLAG, INC_CNT2_FLAG) within the same cluster0 clock cycle. Workaround : If DPLL_CTRL_0.RMO = 0, only use DPLL_STA_FLAG.STA_FLAG_T or DPLL_STA_FLAG.INC_CNT1_FLAG. If DPLL_CTRL_0.RMO = 1 and DPLL_CTRL_SMC = 0, only use DPLL_STA_FLAG.STA_FLAG_S or DPLL_STA_FLAG.INC_CNT1_FLAG. If DPLL_CTRL_0.RMO = 1 and DPLL_CTRL_SMC = 1, only use one of DPLL_STA_FLAG.STA_FLAG_S, DPLL_STA_FLAG.INC_CNT2_FLAG, DPLL_STA_FLAG.STA_FLAG_T, or DPLL_STA_FLAG.INC_CNT1_FLAG.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0

GTM-IP-410	Title : GTM_AEI: The AEI bridge might not execute an accepted write transaction Scope : GTM_AEI Severity : High Classification : Non-critical Effects : Write transaction is signaled to be accepted but will never be executed. Description : If the AEI Bridge operates in pipeline mode while a soft-reset is issued (writing BRIDGE_MODE.BRG_RST = '1'), upcoming write transactions primed in the buffer although accepted may never be actually executed. The maximum number of non-executed transactions depends on the buffer depth (BRIDGE_BUFF_DPT). Workaround : Issue a read access to any address after the soft reset.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
		v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0

Errata-ID	Errata	refer to
GTM-IP-411	Title : A change of the BRIDGE_MODE register might be delayed indefinitely Scope : GTM_AEI Severity : Low Classification : Non-critical Effects : Frequently polling the BRIDGE_MODE register ends in a deadlock. Description : After making a write access to the BRIDGE_MODE register, the bit fields BRG_MODE and BYPASS_SYNC will not be updated until the transaction buffer is empty. In split mode the bridge allows new transactions to be added to the buffer, even when an update of these bits is pending. Polling the register in split mode might prevent the buffer from getting empty and hence prevents the actual update of the described bit fields. Workaround : Option 1, possible in all devices: after every failed attempt to read back the new values, increase the wait time before issuing the next read transaction. Option 2, only possible in devices without AXIS; integration dependent: Use standard mode (which is entered by setting AEI_PIPE and AEI_SPLIT at zero while asserting AEI_SEL) to write and read back the affected bits.	v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1

Errata-ID	Errata	refer to
GTM-IP-413	Title : SPEC-ATOM: Wrong register bit field descriptions for ATOM[i]_CH[x]_CTRL Scope : ATOM Severity : Low Classification : Non-critical Effects : The user does not immediately find the register bits for the functionality behind bits 21, 22, and 23 in the overview figure of the ATOM Channel control register. The user might get confused about the doubled specification of register bits 21, 22, and 23 one time with functionality behind and the other time marked as "not used" in SOMP mode. Description : The specification (revision 2.1.2.1) of the ATOM Channel control register for SOMP mode (ATOM[i]_CH[x]_CTRL) is wrong in two points: First, in the register overview figure the register bit fields for bits 21, 22, and 23 are marked as "not used". However, these register bits are implemented as described in the bit field description. Second, in the register bit fields description subsection, a duplicate entry exists where the register bits 23:21 are marked as "not used". Workaround : Hint: Use the bit field descriptions for bits 23:21 as described in chapter 7.6.9.	v2.1.2-A2

Errata-ID	Errata	refer to
GTM-IP-414	Title : SPEC-ATOM: Control bits of the TRIG_[x] multiplexer are switched Scope : ATOM Severity : Low Classification : Non-critical Effects : A wrong trigger signal is used for subsequent channels. A misconfiguration can break a trigger chain over multiple channels. Description : There is an error in the figure 12.2.1 (revision 2.0.2) or 7.2.1 (revisions 2.1.x.x) for the ATOM Channel architecture. The control bits of the TRIG_[x] multiplexer are switched. The correct behaviour is: When the multiplexer is configured with a '0', one of the signals TIM_EXT_CAPTURE(x) or TRIG[x-1] is used for TRIG[x]. When the multiplexer is configured with '1', the TRIG_CCU0 signal is used. Only the figure is wrong. The register bit description in the ATOM Channels control register is correct. Workaround : Hint: Use the register bit description in the ATOM Channels control register instead of the figure.	v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2

Errata-ID	Errata	refer to
GTM-IP-415	Title : TIO: Internal compare events are not cleared Scope : TIO Severity : Medium Classification : Non-critical Effects : Unexpected behavior of a dual compare instruction e.g. unexpected instruction end. Description : If a dual compare command is disabled by writing TIO[i]_ENDIS.CH[x:x]=0 and enabled again by writing TIO[i]_ENDIS.CH[x:x]=1, compare events which have been detected during the first activation are not cleared. The TIO will react on these invalid compare events. Workaround : It is possible to do a software reset at both affected channels and to setup a new compare instruction as before.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1

Errata-ID	Errata	refer to
GTM-IP-416	Title : TIO: Buffer empty signalization (PL_EVT) is not correct Scope : TIO Severity : Medium Classification : Non-critical Effects : PL_EVT does not reliably reflect the emptiness of the buffers. Description : If a buffer is reloaded by its predecessors buffer which has been written with TIO[i]_G[g]_CH[c]_SCMD.SCMD=0x0 or TIO[i]_G[g]_CH[c]_OCMD.OCMD=0x0, then the buffer filled flag is not set to 0 (0 = buffer empty). Examples of affected reloading: Reloading a buffer e.g. at instruction end with its predecessors buffer TIO[i]_G[g]_CH[c]_SCMD.SCMD = TIO[i]_G[g]_CH[c-1]_OCMD.OCMD with TIO[i]_G[g]_CH[c-1]_OCMD.OCMD = 0x0 or TIO[i]_G[g]_CH[c]_OCMD.OCMD = TIO[i]_G[g]_CH[c]_SCMD.SCMD with TIO[i]_G[g]_CH[c]_SCMD.SCMD = 0x0. Workaround : Do not use instruction sequences with command value 0x0 for TIO[i]_G[g]_CH[c]_SCMD.SCMD or TIO[i]_G[g]_CH[c]_OCMD.OCMD	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1

Errata-ID	Errata	refer to
GTM-IP-417	Title : GTM_AEI: AXIS interface might violate AXI protocol when Mask Write Response is set Scope : GTM_AEI Severity : Low Classification : Non-critical Effects : AXI protocol is violated. Description : Only AXIS devices affected: If BRIDGE_MODE.MSK_WR_RSP = 1, when write and read accesses are done in parallel, depending on internal race conditions the AXIS will potentially violate the AXI protocol. In these cases the output ports for BVALID or RLAST will not be set correctly. Workaround : No workaround in hardware possible. Application shall avoid setting Mask Write Response active.	v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-418	Title : GTM-TOP: Wrong AEI status on accesses to ICM registers while cluster 0 clock is switched off Scope : GTM-TOP, ICM Severity : Low Classification : Non-critical Effects : Wrong AEI status indicates a valid AEI access. Description : Bus accesses to ICM register while cluster 0 clock is switched off by setting of GTM_CLS_CLK_CFG.CLS0_CLK_DIV=0b00 should return AEI status value of 0b10 but it returns always AEI status value of 0b00. Workaround : 1) Do not access ICM while cluster 0 clock is disabled. OR 2) Avoid switching off Cluster 0.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0

GTM-IP-419	Title : TIM: Potentially wrong capture values Scope : TIM Severity : High Classification : Non-critical Effects : TIM[i]_CH[x]_CNT register is not reset and wrong values could be captured into TIM[i]_CH[x]_GPR0 and TIM[i]_CH[x]_GPR1 registers. Description : Configuration: The TIM channel is configured in TIEM, TIPM, TGPS or TSSM mode by setting of TIM[i]_CH[x]_CTRL.TIM_MODE=0b010, 0b011, 0b101, 0b110. The TIM channel is disabled (TIM[i]_CH[x]_CTRL.TIM_EN=0) and later enabled again (TIM[i]_CH[x]_CTRL.TIM_EN=1). Expected behaviour for TIEM/TIPM/TGPS mode: The registers TIM[i]_CH[x]_CNT, TIM[i]_CH[x]_ECNT.ECNT[15:1], TIM[i]_CH[x]_GPR0 and TIM[i]_CH[x]_GPR1 are set to their reset values. In case of an input signal edge or an input capture event or an active selected CMU clock (TGPS mode) at the same time as the channel is enabled, this event has to be taken into account and the TIM[i]_CH[x]_CNT register must be updated/incremented based on its reset value. Due to this a capture event can happen depending on the configured TIM mode and the register values. Expected behaviour for TSSM mode: The registers TIM[i]_CH[x]_CNT, TIM[i]_CH[x]_ECNT.ECNT[15:1], TIM[i]_CH[x]_GPR0 and TIM[i]_CH[x]_GPR1 are set to their initial values. The initial value for TIM[i]_CH[x]_CNT register depends on TIM[i]_CH[x]_CTRL.ISL and TIM[i]_CH[x]_CNTS.CNTS(22). If TIM[i]_CH[x]_CNTS.CNTS(22) is set to 0 and TIM[i]_CH[x]_CTRL.ISL is set to 0 the initial value of TIM[i]_CH[x]_CNT is 0x000000. An input signal event simultaneously to the channel enable is not taken into account. Observed behaviour for TIEM/TIPM/TGPS mode: If no input signal event or input capture event or active selected CMU clock (TGPS mode) occurs, the registers TIM[i]_CH[x]_CNT, TIM[i]_CH[x]_ECNT.ECNT[15:1], TIM[i]_CH[x]_GPR0 and TIM[i]_CH[x]_GPR1 are set to their reset values as expected. If an input signal event or an input capture event or an active selected CMU clock (TGPS mode) occurs at same time as the channel gets enabled, the TIM[i]_CH[x]_CNT register continues to count (or update) based on the previous (old) value. As a result, a capture could be performed too early and/or with the wrong values. The TIM[i]_CH[x]_ECNT.ECNT[15:1] register is set to its reset value as expected.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
	Observed behaviour for TSSM mode: The registers TIM[i]_CH[x]_CNT is not set to its initial value of 0x000000 on channel enabling when TIM[i]_CH[x]_CNTS.CNTS(22) is set to 0 and TIM[i]_CH[x]_CTRL.ISL is set to 0. Note: The TIM channel modes TPWM, TPIM and TBCM (TIM[i]_CH[x]_CTRL.TIM_MODE=0b000, 0b001, 0b100) are not affected. Workaround : Workaround 1: Reset the TIM channel by setting of TIM[i]_RST.RST_CH[x]=1 before enabling the TIM channel. Workaround 2: The following sequence has to be executed on the disabled channel but before the actual enabling of the channel, to ensure that the TIM[i]_CH[x]_CNT register is set to its reset value when the channel is enabled: 1. Configure TIM[i]_CH[x]_CNTS=0 2. Enable the TIM channel with the following configuration inside the TIM[i]_CH[x]_CTRL register: - TIM_EN=1 - TIM_MODE=0b101 (TGPS) - ISL=1 - OSM=1 - ARU_EN=0 - select a fast CMU_CLK_RES, e.g. CLK_SEL=0b000 3. Wait until an edge on the selected CMU_CLK_RES occurs. This can be observed on the NEWVAL IRQ notify register. This event sets the TIM[i]_CH[x]_CNT register to its reset value. 4. Disable TIM channel (TIM[i]_CH[x]_CTRL.TIM_EN=0) 5. Configure the former TIM channel configuration in TIM[i]_CH[x]_CTRL register and enable the TIM channel again.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0

GTM-IP-421	Title : GTM_AEI: Changing BRIDGE_MODE.MSK_WR_RSP in Pipeline mode can lead to violation of Pipeline protocol Scope : GTM_AEI Severity : Low Classification : Non-critical Effects : Transaction not terminated according to protocol, user might be stuck waiting for AEI_READY to be set. Description : In Pipeline mode, a reconfiguration of the BRIDGE_MODE.MSK_WR_RSP directly after another write transaction can lead to a hang of following write transactions by not setting the AEI_READY. Please also check on errata GTM-IP-487 and GTM-IP-488. Workaround : 1) Make sure the transaction preceding the write of BRIDGE_MODE.MSK_WR_RSP is a read transaction. OR 2) Integration dependent: Issue the write to BRIDGE_MODE.MSK_WR_RSP in standard mode instead of pipeline mode.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
		v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0

GTM-IP-422	Title : DPLL: Wrong DPLL_RDT_S_ACT/DPLL_RDT_T_ACT value in case of overflow correction Scope : DPLL Severity : Medium Classification : Non-critical Effects : Wrong value in either DPLL_RDT_T_ACT (emergency mode) or DPLL_RDT_S_ACT (normal mode) after detection of overflow condition. With the next active input signal slope a potentially wrong value of DPLL_RDT_T_ACT is stored to DPLL_RDT_T of RAM2 and DPLL_RDT_S_ACT is stored to DPLL_RDT_S of RAM1bc. This might lead to different settling behaviour of the sub increments and wrong results for PMT calculations if these values are actually used. Description : The wrong overflow correction occurs for DPLL_RDT_S_ACT when the DPLL is in normal mode (DPLL_CTRL_0.RMO=0, DPLL_CTRL_1.SMC=0) or for DPLL_RDT_T_ACT when the DPLL is in emergency mode (DPLL_CTRL_0.RMO=1, DPLL_CTRL_1.SMC=0). Instead of 0xFFFFFF the value 0x000000 is written in both cases. A problem in calculation of pulse frequency (settling behaviour) or for PMT values may occur, when the mode DPLL_CTRL_0.RMO is switched to the other mode (normal mode <-> emergency mode). If the overflow value was not yet overwritten (due to engine revolution happening before mode's switch) the wrong value might come into use for the described calculations. Workaround : Modification of DPLL_RDT_T_ACT (emergency mode) or DPLL_RDT_S_ACT (normal mode) after detection of overflow condition is not possible but does not cause any negative effects on pulse generation or PMT calculation at all. The values stored to DPLL_RDT_T of RAM2 or DPLL_RDT_S of RAM1bc need to be corrected by following workaround sequence: 1) Check if relevant overflow on either DPLL_RDT_T_ACT or DPLL_RDT_S_ACT occurred. This can be done by observation of DPLL_STATUS.CRO when interrupt DPLL_IRQ_NOTIFY.EI occurred. 2) Check which of the interrupts DPLL_IRQ_NOTIFY.TASI/SASI has occurred next and based on that DPLL_RDT_T or DPLL_RDT_S has to be corrected. 3) For DPLL_CTRL_0.RMO=0 and DPLL_CTRL_1.SMC=0, DPLL_RDT_S[DPLL_APS.APS -1] has to be written to 0xFFFFFF.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0

Errata-ID	Errata	refer to
	For DPLL_CTRL_0.RMO=1 and DPLL_CTRL_1.SMC=0, DPLL_RDT_T[DPLL_APT.APT -1] has to be written to 0xFFFFFF.	v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0

Errata-ID	Errata	refer to
GTM-IP-423	Title : MCS: Unexpected Memory overflow when using RET instruction Scope : MCS Severity : Low Classification : Non-critical Effects : MCS channel stops unexpectedly and signals an unexpected memory overflow. Description : If a RET instruction is executed at memory location MP1-4 (last valid memory location) and the associated operation for getting the target address from the stack is executed with a serial memory access (either MCS[i]_CTRL_STAT.EN_HVD = 0 or the stack area is located in the second RAM module RAM1), the corresponding MCS channel stops and signals a memory overflow instead of executing the instruction. Workaround : Reschedule MCS program in a way that memory location MP1-4 has no RET instruction.	v4.1.0-0D0

Errata-ID	Errata	refer to
GTM-IP-424	Title : MCS: Missing Memory overflow detection on literal addresses Scope : MCS Severity : Medium Classification : Non-critical Effects : MCS channel executes an unexpected RAM access instead of signaling a memory overflow. Description : For a memory access at memory location x using a direct memory access (instructions MRD, MWR, or MWRL) or an indirect memory access with literal offset (instruction MRDI or MWRI), an address overflow is not detected for the range 2^(RAW + USR) <= x < 2^14. Workaround : Software needs to avoid accesses to invalid addresses. Otherwise no workaround in hardware possible.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1

Errata-ID	Errata	refer to
GTM-IP-425	Title : MCS: Instructions BRDI and BWRI evaluate unused address bits Scope : MCS Severity : Low Classification : Non-critical Effects : The word alignment for the address of indirect bus master instructions are checked unexpectedly leading to a false error indication. BRD and BRDI accesses of any MCS channel in the affected MCS instance that are following the non-wordaligned access might receive no data or wrong data. The received data for a BRD or BRDI instruction might also be stored in another register of the same MCS channel. Further, the MCS program execution of any channel might be stopped. Description : Bus master instructions with indirect addressing (BRDI and BWRI) use the bits 2 to 15 of register B for defining its target address. However, if the bit slice B[1:0] is unequal to 0 the current implementation of the GTM-IP behaves as follows: bit field CCM[i]_AEIM_STA.AEIM_XPT_STA is updated with value 1 and CCM[i]_AEIM_STA.AEIM_XPT_ADDR is updated with the address of the selected register B. Further, if bit field MCS[i]_CTRL_STAT.HLT_AEIM_ERR is set then the associated MCS channel stops and indicates an unexpected bus master error. Workaround : The use of the lower address bits are forbidden for indirect addressing. Hence this error needs to be avoided by the application.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1

Errata-ID	Errata	refer to
GTM-IP-426	Title : MCS: Unexpected Break Point initiation Scope : MCS Severity : Low Classification : Non-critical Effects : An MCS can execute an unexpected break point event for recently enabled bit field MCS[i]_HBP[h]_CTRL.EN_CH[x]. Description : The current implementation of an MCS hardware break point h is as follows: Potential break point match events that are defined by the bit fields MCS[i]_HBP[h]_CTRL.TYPE, MCS[i]_HBP[h]_CTRL.DATA, MCS[i]_HBP[h]_CTRL.AND, and MCS[i]_HBP[h]_CTRL.NOT and the input port DBG_MCS[i]_BP_EN are stored in an internal pipeline register for all enabled MCS channels but without considering the current values of the bitfields MCS[i]_HBP[h]_CTRL.EN_CH[x]. However, such a potential break point match event of an MCS channel x is actually fired if it is reaching the end of the pipeline register and the corresponding bit field MCS[i]_HBP[h]_CTRL.EN_CH[x] is currently set to 1. This means, the functional behavior of the h-th hardware break point is only correct, if this hardware break point is not re-configured in a way that other running MCS channels y are changing their break point enable behavior from MCS[i]_HBP[h]_CTRL.EN_CH[y]=0 to MCS[i]_HBP[h]_CTRL.EN_CH[y]=1. Workaround : No workaround in hardware possible. Debugger applications must try to avoid such critical reconfigurations.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0

Errata-ID	Errata	refer to
GTM-IP-427	Title : MCS: Missing resume from Hardware Break Point Scope : MCS Severity : Low Classification : Non-critical Effects : Pending hardware break points cannot be resumed by setting input port DBG_MCS[i]_BP_EN to 0 Description : The hardware break point functionality is defined that the i-th MCS instance shall resume from any pending hardware break point if GTM-IP input port DBG_MCS[i]_BP_EN is set to 0. However, this feature is not functional. Workaround : Resuming from a pending break point can be done by a write access to clear the bit fields MCS[i]_HBP[h]_STATUS.HALT_CH[x].	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0

Errata-ID	Errata	refer to
GTM-IP-428	Title : DPLL: Pulse correction is executed twice Scope : DPLL Severity : Low Classification : Non-critical Effects : One additional pulse correction with DPLL_MPVAL1/2 pulses with impact on the angle base CCM[0]_TBU_TS1 or CCM[0]_TBU_TS2. Description : If DPLL_CTRL_1.PCM1/2 is set during DPLL_CTRL_1.DEN=0 or DPLL_CTRL_1.DEN changes from 1 to 0, these values are immediately transferred to the respective shadow registers DPLL_CTRL_1_TRIGGER_SHADOW and DPLL_CTRL_1_STATE_SHADOW. Since the DPLL_CTRL_1.DEN=0 the DPLL_CTRL_1.PCM1/2 registers are not cleared when transferred to the shadow registers. When DPLL_CTRL_1.DEN=1 and the next relevant input signal on either STATE or TRIGGER arrives the pulse corrections are executed due to the state of the named shadow registers. As the DPLL_CTRL_1.PCM1/2 were not cleared this is leading to an additional pulse correction for the next following input signal (TRIGGER / STATE). Workaround : Avoid setting DPLL_CTRL_1.PCM1/2 when DPLL_CTRL_1.DEN=0.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0

GTM-IP-429	Title : TIM: Missing glitch detection interrupt event Scope : TIM Severity : Low Classification : Non-critical Effects : The TIM[i]_CH[x]_IRQ_NOTIFY.GLITCHDET bit is not set. Thus, no interrupt is triggered. Furthermore, the external capture source EXT_CAPTURE(x) is not triggered, if its source is set to TIM_GLITCHDET_IRQ. Description : Configuration: TIM filter is configured in immediate edge propagation mode by setting TIM[i]_CH[x]_CTRL.FLT_MODE_RE = 0 or TIM[i]_CH[x]_CTRL.FLT_MODE_FE = 0. The filter is enabled by setting TIM[i]_CH[x]_CTRL.FLT_EN = 1. Expected behaviour: As long as the filter threshold is not reached and the input signal level unexpectedly changes, it is an input glitch occurs, the internal glitch detection interrupt event signal (TIM_GLITCHDET_IRQ) should have a HIGH pulse of one cluster clock cycle. Observed behaviour: When the input signal glitch occurs at the same time the filter counter reaches its threshold, the internal glitch detection interrupt event signal (TIM_GLITCHDET_IRQ) does not occur. Workaround : The filter counter threshold can be set to the next higher value. Thus, a former not detected glitch would be detected. In that case, the output signal would be changed (one clock cycle longer), when the input signal is a single cycle pulse.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
		v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0

GTM-IP-430	Title : TIM: Unexpected increment of filter counter Scope : TIM Severity : Medium Classification : Critical Effects : If an input edge occurs during the acceptance time, the following output signal change will happen one or more selected CMU clock cycles earlier than expected. This depends on the initial configuration and the reconfiguration of the filter mode and the filter counter threshold. If the filter mode for both edges is configured to immediate edge propagation and both filter counter thresholds are set to zero, the counter falsely can count up to a higher value than one without resetting. If one or both filter modes and/or thresholds are reconfigured during the application, the higher count of the filter counter can lead to a difference of more than one CMU clock cycle between the expected and actual output signal change at the next occurring input edge. If only one filter counter threshold is set to zero, the difference of the expected and actual output signal change is one CMU clock cycle. Description : Configuration: TIM filter is configured in immediate edge propagation mode by setting TIM[i]_CH[x]_CTRL.FLT_MODE_RE = 0 and/or TIM[i]_CH[x]_CTRL.FLT_MODE_FE = 0. The filter is enabled by setting TIM[i]_CH[x]_CTRL.FLT_EN = 1. The filter counter threshold is set to zero by setting TIM[i]_CH[x]_FLT_RE.FTL_RE = 0 and/or TIM[i]_CH[x]_FLT_FE.FTL_FE = 0. Expected behaviour: When the input signal level changes, the filter counter should not increment. Observed behaviour: When the input signal level changes, the filter counter increments by one and is not reset. Workaround : If acceptable, use a threshold greater than zero. Otherwise there is no workaround available. However, there is a possibility of minimizing the absolute error, deriving from this bug. If possible, a faster CMU clock can be selected. This leads to a shorter absolute time difference between the expected and actual output signal change. Additionally when applying this, the filter counter thresholds need to be assimilated proportionally in order to make the filter work as before.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
		v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0

GTM-IP-431	Title : TIM: Glitch detection interrupt event of filter is not a single cycle pulse Scope : TIM Severity : Medium Classification : Critical Effects : Effect 1: The longer lasting HIGH signal of the glitch detection interrupt event signal (GLITCHDET_IRQ) may lead to an unexpected behaviour within the GTM only if GLITCHDET_IRQ is used for the external capture signal EXT_CAPTURE(x). Effect 2: If the related interrupt notify register (The TIM[i]_CH[x]_IRQ_NOTIFY) is cleared while the GLITCHDET_IRQ signal is still HIGH, the interrupt will unexpectedly retrigger. Description : Configuration: The TIM filter must be enabled by setting TIM[i]_CH[x]_CTRL.FLT_EN = 1. Expected behaviour: As long as the filter threshold is not reached and the input signal level changes unexpectedly, the glitch detection interrupt event signal (GLITCHDET_IRQ) should have a single cycle HIGH pulse. Observed behaviour: When the input signal level changes unexpectedly for longer than one clock cycle, the glitch detection interrupt event signal (GLITCHDET_IRQ) is HIGH for as many cluster clock cycles as the unexpected signal change is present. Workaround : No workaround in hardware. For the unexpected retrigger of the interrupt directly after an interrupt clear step, the interrupt routine has to consider that the interrupt might be invalid.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
		v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0

Errata-ID	Errata	refer to
GTM-IP-432	Title : TIO: Compare mode: Output value not correct if two events occur at the same time Scope : TIO Severity : Medium Classification : Critical Effects : Value of O_OUT[c:c] (driving TIO_G[g]_OUT[c:c]) might have a wrong value. Description : Action on O_OUT[c:c] (driving TIO_G[g]_OUT[c:c]) can be missing if in compare mode the current channel is configured as cyclic buffer and the trigger events of PL_TRIG_OUT[c:c] and O_TRIG_OUT[c:c] occur in the same cluster clock cycle. The action defined by O_TRIG_OUT[c:c] should be applied here. Workaround : No workaround in hardware possible. The application should avoid this scenario by disabling one of the two triggers.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1

Errata-ID	Errata	refer to
GTM-IP-433	Title : TIO: Incorrect behaviour on O_OUT in case of consecutive compare events Scope : TIO Severity : Medium Classification : Non-critical Effects : Value of O_OUT[c:c] (driving TIO_G[g]_OUT[c:c]) might have a wrong value. Description : Output O_OUT[c:c] (driving TIO_G[g]_OUT[c:c]) can be incorrect if the two compare events of a dual compare instruction occur back2back, it is if the second compare event coming in the next cluster clock after the first compare event. The error can only occur if the first compare event actually changes the O_OUT[c:c] value. Workaround : Workaround1: Ensure that the resolution of master and slave channel is identical (PL_UPDATE[c:c] =PL_UPDATE[c-1:c-1]). Workaround2: Ensure that the 2 resolutions PL_UPDATE[c:c] and PL_UPDATE[c-1:c-1] can never occur back2back.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1

Errata-ID	Errata	refer to
GTM-IP-434	Title : TIO: Number of register bit fields don't scale with design parameter Scope : TIO Severity : Low Classification : Non-critical Effects : If NTIO_CH8 is less than 3 the two TIO control registers (TIO[i]_RSEL_CTRL1, TIO[i]_RSEL_CTRL2) have unused bits implemented. This needs to be considered when reading the content of these registers. Description : Register content TIO[i]_RSEL_CTRL1.SEL_CLKEN6_[g], TIO[i]_RSEL_CTRL1.SEL_CLKEN7_[g], TIO[i]_RSEL_CTRL2.SEL_TB1_[g] and TIO[i]_RSEL_CTRL2.SEL_TB2_[g] correspond to a TIO design parameter NTIO_CH8=3, but not the real value if it is less than 3. Workaround : Adapt expected read values of the corresponding registers as it should be for design parameter NTIO_CH8=3.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0

Errata-ID	Errata	refer to
GTM-IP-435	Title : DPLL: Doubled pulse correction Scope : DPLL Severity : Low Classification : Non-critical Effects : Pulse correction is executed two times with DPLL_MPVAL1/DPLL_MPVAL2 instead of one time DPLL_MPVAL1/DPLL_MPVAL2. Description : In automatic end mode (DPLL_CTRL_1.DMO=0) using DPLL_CTRL_1.PCM1/2=1 and DPLL_CTRL_11.INCF1/2=1, when DPLL_CTRL_1.DEN=0->1 changes and the first input signal on either TRIGGER/STATE arrives the pulse correction is executed two times with DPLL_MPVAL1/DPLL_MPVAL2. Workaround : Workaround 1: Postpone the pulse correction under the described conditions to the second increment. Workaround 2: For even values of pulse corrections half of the original DPLL_MPVAL1/DPLL_MPVAL2 can be used. With that the effective number of corrected pulses will match the original DPLL_MPVAL1/DPLL_MPVAL2.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0

Errata-ID	Errata	refer to
GTM-IP-436	Title : TIO: In dual compare mode the initialization of internal compare event enables is not correct Scope : TIO Severity : Medium Classification : Non-critical Effects : Compare events are not detected as configured and expected. This can result in an unexpected instruction end and in an unexpected behaviour of O_OUT[c:c] (driving TIO_G[g]_OUT[c:c]). Description : In the dual compare mode the initialization of internal compare event enable flags at state transition DISABLED to ENABLED is not performed, because the inner logic depends on TIO[i]_G[g]_CH[c]_OCMD_COMP.CMD_ACTIVE_CC=b01 which is not intended. Workaround : No workaround in hardware possible. The application should avoid state transitions from DISABLED to ACTIVATED via ENABLED, but instead implement state transfers from DISABLED directly to ACTIVATED.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0

Errata-ID	Errata	refer to
GTM-IP-437	Title : TIO: In dual compare mode the update of internal compare event enables is incorrect Scope : TIO Severity : Medium Classification : Critical Effects : Compare events which occur during TIO[i]_G[g]_CH[c]_OCMD_COMP.CMD_ACTIVE_CC=b00 are detected and stored. After enabling the same instruction again this the stored compare events can result in an unexpected instruction end and in an unexpected behaviour of O_OUT[c:c] (driving TIO_G[g]_OUT[c:c]). Description : In dual compare mode the update of internal compare event enables is done even if instruction is not activated (TIO[i]_G[g]_CH[c]_OCMD_COMP.CMD_ACTIVE_CC=b00). Workaround : The application should avoid this corner case of deactivating an instruction and activating it again (via writing TIO[i]_G[g]_CH[c]_OCMD_COMP.CMD_ACTIVE_CC). The flow to deactivate and safely re-start a dual compare command is: 1. Deactivating the dual compare command by writing TIO[i]_G[g]_CH[c]_OCMD_COMP.CMD_ACTIVE_CC=0x0 2. Disabling both channels by writing TIO[i]_CENDIS.CH[x]=0b1 and TIO[i]_CENDIS.CH[x-1]=0b1 with x=g*8+c. 3. Activate (new) dual compare command by writing TIO[i]_G[g]_CH[c]_OCMD_COMP.CMD_ACTIVE_CC/=0x0 4. Enable both dual compare channels synchronously by writing TIO[i]_SENDIS.CH[x]=0b1 and TIO[i]_SENDIS.CH[x-1]=0b1 with x=g*8+c.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0

Errata-ID	Errata	refer to
GTM-IP-438	Title : TIO: Incorrect behaviour on O_OUT in case of consecutive compare events (2nd event should invert O_OUT) Scope : TIO Severity : Medium Classification : Non-critical Effects : Value of O_OUT[c:c] (driving TIO_G[g]_OUT[c:c]) might have a wrong value. Description : In dual compare mode "serve both master first" the output O_OUT[c:c] (driving TIO_G[g]_OUT[c:c]) can be incorrect if two compare events of a dual compare instruction occur back2back, it is if the second compare event coming in the next cluster clock after the first compare event. The error can only occur if the first compare event actually changes the O_OUT[c:c] value and the second compare event should invert the O_OUT[c:c] value. Workaround : Workaround1: Ensure that the resolution of master and slave channel is identical (PL_UPDATE[c:c] =PL_UPDATE[c-1:c-1]). Workaround2: Ensure that the 2 resolutions PL_UPDATE[c:c] and PL_UPDATE[c-1:c-1] can never occur back2back.	v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0

Errata-ID	Errata	refer to
GTM-IP-439	Title : TIO: Wrong output value on O_OUT in capture mode Scope : TIO Severity : Medium Classification : Non-critical Effects : Value of O_OUT[c:c] (driving TIO_G[g]_OUT[c:c]) might have a wrong value. Description : In capture mode the output O_OUT[c:c] (driving TIO_G[g]_OUT[c:c]) of channel [x] might have a wrong value if a write access to TIO_O.CH[x] is done one cluster clock cycle before the instruction terminates. Workaround : Workaround: Do not write TIO[i]_O.CH[x] if the capture instruction in channel [x] is activated.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0

Errata-ID	Errata	refer to
GTM-IP-440	Title : MCS: Unexpected data break point behavior Scope : MCS Severity : Low Classification : Non-critical Effects : Data break points might unexpectedly be initiated or not initiated at all. Description : The hardware break point functionality has the following unexpected behavior if a break point is configured with MCS[i]_HBP[h]_CTRL.TYPE = DADR or MCS[i]_HBP[h]_CTRL.TYPE = DPAT and a serial data access occurs: 1) In the case of the execution of a prefetched instruction that is following any serial data access, the prefetched instruction might be misinterpreted as data resulting in an unexpected break point. 2) Serial data accesses resulting from stack operations of the instructions CALL, CALLI, or RET do not initiate any break point. Workaround : No workaround in hardware possible.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0

Errata-ID	Errata	refer to
GTM-IP-441	Title : DPLL: Missing pulse correction in case of DPLL_CTRL_1.SMC=1 Scope : DPLL Severity : Medium Classification : Non-critical Effects : Missing pulse correction via sub increment generator 1 for CCM[0]_TBU_TS1 under the described configuration. Description : If DPLL_CTRL_1.SMC=1 and DPLL_CTRL_0.RMO=1 and DPLL_CTRL_11.PCMF1=0 no pulse correction on CCM[0]_TBU_TS1 is executed. Workaround : 1) Use DPLL_CTRL_0.RMO=0 when DPLL_CTRL_1.SMC=1. In this case fast pulse corrections via DPLL_CTRL_11.PCMF1 are possible. 2) Use DPLL_CTRL_11.PCMF1=1 for pulse corrections. In this case no negative values for DPLL_MPVAL1 can be used.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0

Errata-ID	Errata	refer to
GTM-IP-442	Title : GTM Top Level: GTM_HALT mode not functional when cluster 0 clock is disabled Scope : GTM Top Level Severity : Low Classification : Non-critical Effects : Functional operation of GTM is not completely stopped although gtm_halt_req is set and GTM_HALT mode is started. This will lead to an undefined state of the GTM and the GTM cannot be reliably resumed out of this state. Description : In case gtm_halt_req=1 enters the GTM_HALT mode all functional operation of the GTM shall stop. In case if the cluster 0 is switched off by GTM_CLS_CLK_CFG.CLS_CLK_DIV0=0b00 this will not happen for all other clusters 1, ... NCCM-1 correctly. Operation of GTM functionality will partly continue, which is unexpected. Workaround : No workaround available. Make sure to turn on the cluster 0 clock before setting gtm_halt_req=1 to switch to GTM_HALT mode.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-445	Title : GTM Top Level: test_clk is not propagated to cluster clock dividers Scope : GTM Top Level Severity : Low Classification : Non-critical Effects : For devices containing clusters which can run on slow (divided) clk only: These cluster cannot be tested with the test_clk input for transient failures. Description : For GTM-IP integrator only; Production test capability: The external test_clk is not propagated to the clusters clock divider stage due to the top-level generic int_clk_en_g not being propagated to the clusters. As a consequence external clk input is used for the cluster clock in test mode(scan_mode=1) instead of the test_clk input. This issue is only relevant for devices containing clusters which can run on slow (divided) clk only. Workaround : Workarounds: 1) Test the "slow clusters" separately with a slow clk input clock. 2) Synthesize the device with fast (undivided) clock constraints even for the "slow clusters".	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0

Errata-ID	Errata	refer to
GTM-IP-446	Title : (A)TOM: (A)TOM_OUT not set correctly when channel is triggered by preceding channel Scope : TOM, ATOM Severity : Medium Classification : Non-critical Effects : Missing toggle on the output signal (A)TOM_OUT to the inverse value of (A)TOM[i]_CH[x]_CTRL.SL. Description : Configuration: The channel is configured to be triggered by a preceding channel by setting of (A)TOM[i]_CH[x]_CTRL.RST_CCU0=1. ATOM is configured to SOMP mode. For devices which have one or more of the GTM top-level parameters (A)TOM_TRIG_CHAIN/(A)TOM_TRIG_INTCHAIN set pipeline register stages are in place in the trigger chain between the triggering channel and the triggered channel. The selected CCM clock resolutions are configured to be unequal to the cluster clocks. The value of (A)TOM[i]_CH[x]_CTRL.SL for the new period was configured to the opposite value compared to the current period. After the counter (A)TOM[i]_CH[x]_CN0.CN0 reaches the value of (A)TOM[i]_CH[x]_CM1.CM1, the output signal (A)TOM_OUT is set to the inverse value of (A)TOM[i]_CH[x]_CTRL.SL, but before the counter (A)TOM[i]_CH[x]_CN0.CN0 reaches the value of (A)TOM[i]_CH[x]_CM0.CM0, the trigger signal from preceding channel occurs and (A)TOM[i]_CH[x]_CN0.CN0 is reset. A new period is started. Expected behavior: An edge to the inverse value of (A)TOM[i]_CH[x]_CTRL.SL on (A)TOM_OUT occurs when the counter (A)TOM[i]_CH[x]_CN0.CN0 reaches the value of (A)TOM[i]_CH[x]_CM1.CM1 in the new period. Observed behavior: No edge occurs on (A)TOM_OUT when the counter (A)TOM[i]_CH[x]_CN0 reaches the value of (A)TOM[i]_CH[x]_CM1.CM1 in the new period. Workaround : Restrict the usage of the trigger chain to the channels which are not separated by a pipeline register. See also the description of the pipeline configuration bits ((A)TOM_TRIG_CHAIN/(A)TOM_TRIG_INTCHAIN) in the CCM[i]_HW_CONF register.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0

Errata-ID	Errata	refer to
GTM-IP-448	Title : MCS: Unexpected state of register MCS[i]_HBP[k]_STATUS Scope : MCS Severity : Low Classification : Non-critical Effects : The status register MCS[i]_HBP[k]_STATUS might signalize a break point from a previous configuration. Description : Assume that the k-th MCS break point is configured with MCS[i]_HBP[k]_CTRL.SCOPE = 2 and this break point is enabled for an MCS channel x by setting MCS[i]_HBP[k]_CTRL.EN_CH[x] = 1. If the MCS channel x reaches that break point, the register MCS[i]_HBP[k]_STATUS signalizes the break point correctly by setting MCS[i]_HBP[k]_STATUS.HALT_CH[x] = 1. Further, if we assume that the k-th break point is reconfigured again with MCS[i]_HBP[k]_CTRL.SCOPE = 2 and it is enabled for another channel y (with x unequal to y) by setting MCS[i]_HBP[k]_CTRL.EN_CH[y] = 1 the following unexpected behavior might happen: The register MCS[i]_HBP[k]_STATUS still signalizes MCS[i]_HBP[k]_STATUS.HALT_CH[x] = 1 from the first break point although the second break point has already been reached. The second break point is nevertheless signalized correctly by setting bit field MCS[i]_HBP[k]_STATUS.HALT_CH[y] = 1. Workaround : No workaround in hardware possible.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0

Errata-ID	Errata	refer to
GTM-IP-449	Title : TIO: Erroneous assertion of PL_EVT when channel is configured as a cyclic buffer Scope : TIO Severity : Low Classification : Non-critical Effects : PL_EVT[c:c] is asserted to indicate an empty buffer which is not intended. Description : Configuration: The channel is configured as a cyclic buffer with S resource configured as a count instruction or a buffer and the O resource configured as a buffer. The PL_EVT[c:c] is unexpectedly asserted on every exchange that loads the instruction with 0x0 into the O resource. Workaround : For the described configuration, do not use the PL_EVT[c:c] as an update source (UPDATE[c:c], PL_UPDATE[c:c]), as an interrupt source (TIO_IRQ[c:c]), or as a trigger source (TRIG_OUT[c:c], PL_TRIG_OUT[c:c]).	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0

GTM-IP-450	Title : DPLL: Stored time stamp values do not consider filter delays Scope : DPLL Severity : Medium Classification : Non-critical Effects : The missing correction of the stored time stamp values does lead to inaccuracies in DPLL PMT calculations. Description : For the case where the filter delay values should be considered (DPLL_CTRL_0.IDT/IDS=1) the data values of the time stamp fields in RAM1c (DPLL_TSF_S) and RAM2 (DPLL_TSF_T) actually do not take them into account for the input signals TRIGGER/STATE. Workaround : The entry of DPLL_TSF_T[p]/_S[p] can be read, corrected (by DPLL_FTV_T/_S), and written back. The correction needs to be done after the DPLL has received new input data. For this reason it is necessary to read and store the filter value of the last but one DPLL input signal, which then will be used for the correction.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0

Errata-ID	Errata	refer to
		v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0

GTM-IP-451	Title : DPLL: Wrong measured position stamps in RAM Scope : DPLL Severity : Medium Classification : Non-critical Effects : Wrong values for DPLL_PSSM and DPLL_PSSM_OLD stored in memory. Controlling of angle clock cannot rely on these values. Description : For the synchronous motor control (DPLL_CTRL_1.SMC=1) in normal mode (DPLL_CTRL_0.RMO=0) wrong values are stored in RAM1b for DPLL_PSSM and DPLL_PSSM_OLD. The entries are not derived from CCM[0]_TBU_TS2 at the point of time when the active input signal arrives but they are derived erroneously from CCM[0]_TBU_TS1 instead. Workaround : Configure relevant TIM channels which are used to define the STATE input signal, such that CCM[0]_TBU_TS2 is captured in each one of the TIM[0]_CH[x]_GPR1.GPR1 registers. After a STATE input signal has arrived wait until the point in time when the DPLL should have calculated the DPLL_PSSM or DPLL_PSSM_OLD value. This is fulfilled when the content of the bit field DPLL_STA.STA_S has passed the value 0x28. Then write DPLL_PSSM or DPLL_PSSM_OLD with the value of the TIM[0]_CH[x]_GPR1.GPR1 register of the corresponding TIM channel causing the captured input signal edge of STATE input. Which of the DPLL_PSSM or DPLL_PSSM_OLD values has to be written might be figured out by using the content of the bit field DPLL_OSW.SWON_S.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0

Errata-ID	Errata	refer to
		v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0

Errata-ID	Errata	refer to
GTM-IP-452	Title : TIO: Incorrect initialization of internal compare event enables on cancel trigger Scope : TIO Severity : Medium Classification : Non-critical Effects : Compare events might not be detected as configured and expected. This can result in an unexpected instruction end and in an unexpected behaviour of O_OUT[c:c] (driving TIO_G[g]_OUT[c:c]). Description : In the dual compare mode the initialization of internal compare event enable flags is not performed when a cancel trigger O_INSTR_PULL_NEXT occurs. Workaround : No workaround in hardware possible. The application should avoid canceling an instruction by using O_INSTR_PULL_NEXT.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0

Errata-ID	Errata	refer to
GTM-IP-453	Title : TIO: Cancel trigger in single compare mode does not suppress action on O_OUT Scope : TIO Severity : Medium Classification : Non-critical Effects : The output O_OUT[c:c] (driving TIO_G[g]_OUT[c:c]) of channel [x] might have a wrong value. Description : If in single compare mode an instruction terminates regularly and the cancel trigger O_INSTR_PULL_NEXT occurs at the same time the instruction is canceled, instruction end (signal INSTR_END=1) is correctly suppressed, but not the action on O_OUT[c:c] (driving TIO_G[g]_OUT[c:c]). Workaround : No workaround in hardware possible. The application should avoid canceling an instruction by using O_INSTR_PULL_NEXT.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0

Errata-ID	Errata	refer to
GTM-IP-454	Title : (A)TOM: No output if trigger generation feature is used Scope : TOM, ATOM Severity : Medium Classification : Non-critical Effects : No module output signals (A)TOM_OUT and (A)TOM_OUT_T are generated. Description : For trigger generation ((A)TOM[i]_CH[x]_CTRL.SR0_TRIG=1) in up-down counter mode ((A)TOM[i]_CH[x]_CTRL.UDMODE>0) neither a new PWM on (A)TOM_OUT nor an additional trigger output on (A)TOM_OUT_T is generated if (A)TOM[i]_CH[x]_SR0.SR0 register is configured to zero. Workaround : A second (A)TOM channel z can be used to generate a trigger signal on (A)TOM_OUT_T for (A)TOM[i]_CH[z]_SR0.SR0=0. The channel has to be configured in up counter mode ((A)TOM[i]_CH[z]_CTRL.UDMODE=0) with a period value calculated by (A)TOM[i]_CH[x]_CM0.CM0*2-2 related to the period value of the first channel x. Both channels have to be started synchronously via the TGC/AGC mechanisms.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0

GTM-IP-456	Title : DPLL: No action calculation Scope : DPLL Severity : Low Classification : Critical Effects : No action calculation of channels NOAC/2 to NOAC-1. Description : If DPLL_CTRL_1.SMC=1 and DPLL_CTRL_0.RMO=0 no action calculation is done in STATE processing unit for action channels NOAC/2 to NOAC-1 (NOAC: number of action channels). Note: Starting with V4.1.* NOAC=32, while in previous versions NOAC may be set to either 32 or 24. Workaround : No workaround available.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0

Errata-ID	Errata	refer to
		v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100

GTM-IP-458	Title : DPLL: Missing TOR or SOR interrupt and status flag Scope : DPLL Severity : Medium Classification : Non-critical Effects : The TOR interrupt (DPLL_IRQ_NOTIFY.TORI) is not triggered and the status flag (DPLL_STATUS.TOR) is not set with the described configuration. The SOR interrupt (DPLL_IRQ_NOTIFY.SORI) is not triggered and the status flag (DPLL_STATUS.SOR) is not set with the described configuration. Description : If DPLL_CTRL_0.RMO=1 and DPLL_CTRL_1.SMC=0, the TOR interrupt (DPLL_IRQ_NOTIFY.TORI) is not triggered and the status flag (DPLL_STATUS.TOR) is not set on encountering an out of range TRIGGER. If DPLL_CTRL_0.RMO=0 and DPLL_CTRL_1.SMC=0, the SOR interrupt (DPLL_IRQ_NOTIFY.SORI) is not triggered and the status flag (DPLL_STATUS.SOR) is not set on encountering an out of range STATE input signal. Workaround : No workaround available in hardware. Nevertheless the application can detect the trigger out of range interrupt by observing TBU_TS0: a) If the current TRIGGER time stamp (DPLL_TS_T.TRIGGER_TS / DPLL_TS_T_OLD.TRIGGER_TS_OLD) + DPLL_DT_T_ACT.DT_T_ACT * DPLL_TLR.TLR > TBU_TS0 and no active TRIGGER input was encountered, the CPU/MCS can force a TOR interrupt by writing a one to DPLL_IRQ_FORCINT.TRG_TORI. b) If the current STATE time stamp (DPLL_TS_S.STATE_TS / DPLL_TS_S_OLD.STATE_TS_OLD) + DPLL_DT_S_ACT.DT_S_ACT * DPLL_SLR.SLR > TBU_TS0 and no active STATE input was encountered, the CPU/MCS can force a SOR interrupt by writing a one to DPLL_IRQ_FORCINT.TRG_SORI.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0

Errata-ID	Errata	refer to
		v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100

Errata-ID	Errata	refer to
GTM-IP-459	Title : MCS: Missing data break point initiations Scope : MCS Severity : Low Classification : Non-critical Effects : Data break point is not triggered. Description : Assume that a break point is reconfigured as a data break point. If the preceding break point is resumed the next possible match for the reconfigured data break point is not initiated. Workaround : No workaround in hardware possible.	v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0

Errata-ID	Errata	refer to
GTM-IP-460	Title : MCS: Missing data break point for parallel memory access Scope : MCS Severity : Low Classification : Non-critical Effects : Data break point is not triggered. Description : If a hardware break point with index 0 is configured with type DPAT-R or DPAT-RW a match event resulting from a parallel memory read access does not trigger a break point. Workaround : No workaround in hardware possible.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0

Errata-ID	Errata	refer to
GTM-IP-461	Title : MCS: Unexpected behavior of instruction WUCE Scope : MCS Severity : Low Classification : Non-critical Effects : The behavior of the WUCE instruction for both boundary values does not follow the formal definition of Cyclic Event Compare functionality. Description : The GTM specification for the Cyclic Event Compare was not detailed enough to describe the complete range including the boundaries between future and past. With the revised specification of GTM 4.1 it was revealed that the implementation for the WUCE instruction is not correct for the boundaries. The implementation of the WUCE instruction has an inverted behavior for both boundaries between future and past. Note: Typical applications do not operate directly with these boundary values, which means that the erroneous behavior can usually be considered as an irrelevant corner case. Workaround : No workaround in hardware possible.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0

GTM-IP-462	Title : (A)TOM: Missing CCU0TC_IRQ interrupt signal Scope : TOM, ATOM Severity : Medium Classification : Non-critical Effects : Interrupt signal CCU0TC_IRQ is not triggered. Description : Configuration: The channel is configured in SOMP (ATOM) up-counter mode with updown counter mode disabled ((A)TOM[i]_CH[x]_CTRL.UDMODE=0) or not existing and triggering by a preceding channel with configuration of (A)TOM[i]_CH[x]_CTRL.RST_CCU0=1. Expected behaviour: When the counter (A)TOM[i]_CH[x]_CN0.CN0 reaches the value of (A)TOM[i]_CH[x]_CM0.CM0, the interrupt signal CCU0TC_IRQ must be triggered. Observed behaviour: In the first period after (A)TOM[i]_CH[x]_CM0.CM0 is changed to the value 0 or 1, no CCU0TC_IRQ interrupt signal is triggered. Note: When the second period starts after (A)TOM[i]_CH[x]_CM0.CM0 is changed to the value 0 or 1 and stays at that value, then the CCU0TC_IRQ interrupt signal generation works correctly. Workaround : No workaround available. It needs to be checked if the application can accept the interrupt occurring with the second period.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
		v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100

GTM-IP-463	Title : DPLL: DPLL_PVT not cleared after direction change Scope : DPLL Severity : Low Classification : Non-critical Effects : DPLL_PVT is not cleared and the PVT check is not suppressed under the described conditions. The PVT violation interrupt (DPLL_PWI_IRQ) could be unexpectedly triggered. Description : For settings of DPLL_CTRL_1.SMC=1 or alternatively DPLL_CTRL_1.SMC=0 and DPLL_CTRL_1.IDDS=1 the direction change on TRIGGER channel is done via DPLL input port "TDIR" (generated via the control path SPE or TIM to MAP to DPLL). If there is a direction change the RAM parameter DPLL_PVT is not cleared as specified. Workaround : Reset DPLL_PVT by CPU or MCS0 write operation, when direction change is detected via DPLL_IRQ_NOTIFY.DCGI interrupt.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0

Errata-ID	Errata	refer to
		v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100

Errata-ID	Errata	refer to
GTM-IP-464	Title : DPLL: Pulse correction executed twice when DPLL_CTRL_11.INCF1/2 is activated. Scope : DPLL Severity : Low Classification : Non-critical Effects : Pulse correction is executed twice. The angle clocks CCM[0]_TBU_TS1/2 are misaligned. DPLL_PSTM, DPLL_PSSM, DPLL_PSTM_OLD, and DPLL_PSSM_OLD will have wrong values. Description : DPLL_MPVAL1/2.MPVAL1/2 is incremented (or decremented) twice in subsequent input signal events (only in the current increment and the following) when DPLL_CTRL_11.INCF1/2 is switching to 1 and a pulse correction is triggered via DPLL_CTRL_1.PCM1/2=1. Workaround : Do not change DPLL_CTRL_11.INCF1/2 to 1 while pulse correction is ongoing. If this cannot be avoided, additional pulse correction might be needed to counteract the double correction of this erratum.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100

Errata-ID	Errata	refer to
GTM-IP-465	Title : (A)TOM: Missing CCU0TC_IRQ interrupt signal for UDMODE>0 Scope : TOM, ATOM Severity : Medium Classification : Critical Effects : Interrupt signal CCU0TC_IRQ is not triggered. Description : Configuration: The channel is configured in SOMP (ATOM) up-down counter mode with (A)TOM[i]_CH[x]_CTRL.UDMODE>0 and will be triggered by an preceding channel with configuration of (A)TOM[i]_CH[x]_CTRL.RST_CCU0=1. Expected behaviour: When the counter (A)TOM[i]_CH[x]_CN0.CN0 reaches in the up-counting phase the value of (A)TOM[i]_CH[x]_CM0.CM0, the interrupt signal CCU0TC_IRQ must be triggered. Observed behaviour: In the first period after (A)TOM[i]_CH[x]_CM0.CM0 is changed to the value 0, the CCU0TC_IRQ interrupt signal is triggered but not in the following periods with unchanged value of (A)TOM[i]_CH[x]_CM0.CM0=0. A second observation is that the CCU0TC_IRQ interrupt signal is not triggered in the first period after the value of (A)TOM[i]_CH[x]_CM0.CM0 is changed from 0 to 1. Note: in this case, the CCU0TC_IRQ interrupt is triggered in the following periods with unchanged value of 1 for (A)TOM[i]_CH[x]_CM0.CM0. Workaround : No workaround available. If applicable use the interrupt indication from the preceding channel, which is always generated half a period earlier.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110

Errata-ID	Errata	refer to
GTM-IP-466	Title : TOM: Unexpected behaviour of TOM_OUT_T for UDMODE>0 Scope : TOM Severity : Medium Classification : Critical Effects : Output signal TOM_OUT_T behaves not as expected. Description : Configuration: The channel is configured in up-down counter mode with TOM[i]_CH[x]_CTRL.UDMODE>0 and will be triggered by an preceding channel with configuration of TOM[i]_CH[x]_CTRL.RST_CCU0=1. Expected behaviour: The output signal TOM_OUT_T has to be set to TOM[i]_CH[x]_CTRL.SL value as long as the condition TOM[i]_CH[x]_CN0.CN0 >= TOM[i]_CH[x]_CM0.CM0 is true. Observed behaviour for TOM[i]_CH[x]_CM0.CM0=0: The output signal TOM_OUT_T is set to TOM[i]_CH[x]_CTRL.SL value only for one clock period of the selected CMU clock when TOM[i]_CH[x]_CN0.CN0 has reached 0. Afterwards TOM_OUT_T is set unexpectedly to the inverted value of TOM[i]_CH[x]_CTRL.SL. Observed behaviour for TOM[i]_CH[x]_CM0.CM0=1: An unexpected pulse on the output signal TOM_OUT_T with the length of one clock period of the selected CMU clock to the inverted value of TOM[i]_CH[x]_CTRL.SL can be observed when the trigger input signal TRIGIN occurs and the counter TOM[i]_CH[x]_CN0.CN0 starts to count down. Workaround : No workaround available.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110

Errata-ID	Errata	refer to
GTM-IP-467	Title : MCS: Some internal MCS registers are not controlled by GTM halt logic Scope : MCS Severity : Low Classification : Non-critical Effects : MCS processing is not reliable with respect to the mentioned effects after resuming from a GTM halt event. Description : Some internal MCS registers (not mentioned in the specification) are not controlled by the GTM halt logic. Therefore, the following side effects might occur: 1) If an MCS is getting resumed after a GTM halt event a previous error of type write protection (MCS[i]_CTRL_STAT.ERR_SRC_ID = 6), ECC error (MCS[i]_CTRL_STAT.ERR_SRC_ID = 1), or memory overflow (MCS[i]_CTRL_STAT.ERR_SRC_ID = 2) might not be signalized and the MCS will not halt due to that error. 2) If an MCS is getting resumed after a GTM halt event a halted parallel memory access might be corrupt. Workaround : No workaround in hardware possible. A resume after GTM halt is not recommended.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0

Errata-ID	Errata	refer to
GTM-IP-468	Title : MCS: Write access to protected bit field reports unexpected AEI status Scope : MCS Severity : Low Classification : Non-critical Effects : Unexpected AEI status during write access to a protected bit field. Description : If the protection enable condition of bit field MCS[i]_CTRL_STAT.RAM_RST is active any write access to the register MCS[i]_CTRL_STAT nevertheless must return an AEI status 0. However, if this protection enable condition is active and a write access with value 1 to bitfield MCS[i]_CTRL_STAT.RAM_RST is executed an AEI status 2 is returned. Workaround : No workaround in hardware possible. The application needs to consider the unexpected status.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100

Errata-ID	Errata	refer to
GTM-IP-469	Title : MCS: Missing trace information of WUCE instruction Scope : MCS Severity : Low Classification : Non-critical Effects : Missing signalization in instruction trace interface. Description : If the match event for a WUCE instruction arrives a few system clock cycles after the corresponding MCS channel has entered the suspended state, the WUCE instruction is executed correctly, but the instruction trace interface does not signalize this instruction. Workaround : No workaround in hardware possible.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

Errata-ID	Errata	refer to
GTM-IP-470	Title : SPEC-CMU: Superscript values not displayed correctly Scope : CMU Severity : Low Classification : Non-critical Effects : Customer might set wrong values which could then lead to a wrong behavior. Description : Due to a formatting error, the superscript formatting of values in CMU_528 is lost and the text-parts are displayed without the special formatting. Thus the customer cannot recognize the error and in the worst case uses the wrong values. Workaround : Hint: In CMU_528 numbers are to be interpreted as powers of two e.g. 2^0, 2^4, 2^8...2^q. The correct formatting is shown in figure of CMU_1314.	v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10

GTM-IP-471	Title : SPEC-ATOM: Wrong description of SOMI/SOMS modes Scope : ATOM Severity : Low Classification : Non-critical Effects : The customer erroneously assumes that in SOMS/SOMI mode the force update trigger is always synchronized to the cluster clock. Description : The implementation of the shadow registers is intended for all applicable modes in ATOM. The specification is not describing the corresponding aspects for the SOMI and SOMS modes. The following functions are to be considered: In SOMI mode, ATOM[i]_CH[x]_CTRL_SOMI.CLK_SRC must be configured as 0. As a result, the clock resolution CCM[i]_CLK_RES[0:0] from CCM module is selected to be used. The force update trigger from AGC unit is then always synchronized to the selected clock resolution CCM[i]_CLK_RES[0:0] to update ATOM[i]_CH[x]_CTRL_SOMI.SL from ATOM[i]_CH[x]_CTRL_SR.SL_SR. In SOMS mode, the force update trigger from AGC unit is also synchronized to the selected clock resolution configured in ATOM[i]_CH[x]_CTRL_SOMS.CLK_SRC. Based on the above description, the specification should contain the following updates. The RW coding of ATOM[i]_CH[x]_CTRL_SOMI.CLK_SRC should be changed as: "0b0000 :CCM[i]_CLK_RES[0:0] resolution in use 0b0001-0b1111: prohibited." The spec item ATOM_2710 should be changed as: "In SOMP, SOMI and SOMS mode, the force update request is synchronized to the selected CCM[i]_CLK_RES as shown in figure "ATOM_2544" and then executed. In other modes the force update request is executed immediately." The note at ATOM_2659 should be removed. Workaround : Hint: If the customer wants to have the force update trigger that is synchronized to the cluster clock in SOMS/SOMI mode, they should configure ATOM[i]_CH[x]_CTRL_SOMI.CLK_SRC=0 /	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10

Errata-ID	Errata	refer to
	ATOM[i]_CH[x]_CTRL_SOMS.CLK_SRC=0 and configure the CCM clock resolution CCM[i]_CLK_RES[0:0] to be equal to the cluster clock.	

GTM-IP-473	Title : SPEC-FIFO: Wrong description of FIFO Flush operation Scope : FIFO Severity : Low Classification : Non-critical Effects : Effect 1: The value of FIFO[i]_CH[x]_RD_PTR.ADDR and FIFO[i]_CH[x]_WR_PTR.ADDR are not set to the initial value as described in the specification. Effect 2: False value of FIFO[i]_CH[x]_STATUS.UP_WM after a flush request in case FIFO[i]_CH[x]_UPPER_WM.ADDR is programmed to 0. Description : FLUSH bit field description of register FIFO[i]_CH[x]_CTRL (GTM4.1 spec.: FIFO_585): The specification describes that the FIFO[i]_CH[x]_FILL_LEVEL.LEVEL, the FIFO[i]_CH[x]_RD_PTR.ADDR, and FIFO[i]_CH[x]_WR_PTR.ADDR will be reset to their initial values. This is valid for FIFO[i]_CH[x]_FILL_LEVEL.LEVEL but not for FIFO[i]_CH[x]_RD_PTR.ADDR and FIFO[i]_CH[x]_WR_PTR.ADDR, which are set to the value of FIFO[i]_CH[x]_START_ADDR.ADDR on a FIFO Flush operation. Also it should be mentioned in the specification that the status bits EMPTY, FULL, LOW_WM and UP_WM of register FIFO[i]_CH[x]_STATUS are set to EMPTY=1, FULL=0, LOW_WM and UP_WM depending on the values programmed into FIFO[i]_CH[x]_LOWER_WM.ADDR and FIFO[i]_CH[x]_UPPER_WM.ADDR. UP_WM bit field description of register FIFO[i]_CH[x]_STATUS (GTM4.1 spec.: FIFO_628): The condition for the UP_WM bitfield of the register FIFO[i]_CH[x]_STATUS is not correct in case the register for FIFO[i]_CH[x]_UPPER_WM.ADDR is programmed to 0 and afterwards a FIFO FLUSH is requested. In this case the bit UP_WM will signal 0 in RTL, but the evaluation due to the specification expects a 1. To overcome this inconsistency between RTL and the specification, the value 0 for FIFO[i]_CH[x]_UPPER_WM.ADDR has to be excluded in the specification (see Note in the ADDR bit field description of register FIFO[i]_CH[x]_UPPER_WM, GTM4.1 spec.: FIFO_609), as this value does not make sense from an application point of view. Prose text in the Overview chapter of FIFO (GTM4.1 spec.: FIFO_836):	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
	It is mentioned that the read and write pointer and also the fill level of the corresponding FIFO channel will be reset. Here the word reset is used in context with the Flush. Typically reset is combined with setting the initial values, but this is not true here. Instead of "reset" another term should be used, for example: "set to previously configured values". Following note is missing in the specification: A FIFO flush operation does not influence the state of the FIFO[i]_CH[x]_IRQ_NOTIFY register. Workaround : Workaround 1: Configure FIFO[i]_CH[x]_START_ADDR.ADDR to its initial value before executing the flush operation. Workaround 2: Do not configure value 0 for FIFO[i]_CH[x]_UPPER_WM.ADDR	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10

GTM-IP-474	Title : DPLL: DPLL_PSTC, DPLL_PSSC erroneously modified. Scope : DPLL Severity : Low Classification : Non-critical Effects : Update of DPLL_PSTC and/or DPLL_PSSC after direction change. These values are unreliable then. Description : If a direction change happens while the TRIGGER processing unit is not yet synchronized (DPLL_STATUS.SYT = 0) then DPLL_PSTC is erroneously overwritten. If a direction change happens while the STATE processing unit is not yet synchronized (DPLL_STATUS.SYS = 0) then DPLL_PSSC is erroneously overwritten. Workaround : Store the DPLL_PSTC, DPLL_PSSC values outside the DPLL, each time a TRIGGER/STATE input occurs. If a direction change is detected, overwrite the newly calculated value by the value stored earlier. This is necessary as long as the DPLL is not yet synchronized (DPLL_STATUS.SYT=0 for DPLL_PSTC and/or DPLL_STATUS.SYS=0 for DPLL_PSSC).	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0

Errata-ID	Errata	refer to
		v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120

GTM-IP-475	Title : DPLL: Incorrect values of DPLL_RCDT_TX, DPLL_RCDT_SX Scope : DPLL Severity : Low Classification : Non-critical Effects : Wrong value is stored in either DPLL_RCDT_TX (normal mode) or DPLL_RCDT_SX (emergency mode) after a detection of a reciprocal overflow condition. The derived parameters DPLL_RCDT_TX_NOM.RCDT_TX_NOM and DPLL_RCDT_SX_NOM.RCDT_SX_NOM are diverging accordingly. This is leading to a different calculation of the pulse generator frequencies (DPLL_ADD_IN_CAL1.ADD_IN_CAL1 or DPLL_ADD_IN_CAL2.ADD_IN_CAL2 in dependence of the configured DPLL mode), which might lead to a different settling behavior of the generated angle clocks in such cases. The diverging settling behavior is not necessarily malicious. Description : If during the reciprocal value calculation an overflow happens then the parameters DPLL_RCDT_TX.RCDT_TX and DPLL_RCDT_SX.RCDT_SX are set erroneously to 0x000000. The specified value is 0xFFFFFF. Workaround : If a different settling behaviour of the DPLL control loop is acceptable no specific countermeasure is necessary.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0

Errata-ID	Errata	refer to
		v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120

Errata-ID	Errata	refer to
GTM-IP-476	Title : MCS: Unexpected instruction execution while disabling of MCS channel Scope : MCS Severity : Medium Classification : Non-critical Effects : Unexpected write access to MCS memory or read/write access to the GTM sub module. Description : A disable request initiated by a write access MCS[i]_CH[x]_CTRL.EN = 0 might cause the following unexpected side effects if the MCS is not configured in Round Robin Scheduling mode and the following conditions are met: 1) Assume that an MCS channel x is disabled after the execution of an instruction instr1. If a potential successor instruction instr2 of instruction instr1 is a memory instruction executing a parallel memory write access and the delay between instr2 and instr1 is up to 3 cluster clock cycles, the write access of instruction instr2 might be executed unexpectedly after the MCS channel is already disabled. 2) Assume that an MCS channel x is disabled after the execution of an instruction instr1. If a potential successor instruction instr2 of instruction instr1 is a bus master instruction executing a bus access and the delay between instr2 and instr1 is up to 2 cluster clock cycles, the access of instruction instr2 might be executed unexpectedly after the MCS channel is already disabled. Workaround : Provide a disabling feature by MCS program, e.g.: 1) Reserve a memory cell in MCS RAM and define value 1 as a request for a MCS channel disable. 2) Instead of writing MCS[i]_CH[x]_CTRL.EN = 0 write value 1 to reserved memory cell. 3) Poll the reserved memory cell during idle time of MCS program and switch off the MCS channel with instruction MOVL STA 0x0 if the reserved memory cell contains value 1.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

GTM-IP-477	Title : DPLL: DPLL_DCGI interrupt not triggered Scope : DPLL Severity : Medium Classification : Non-critical Effects : The interrupt DPLL_DCGI does not occur. Description : When synchronous motor control mode is active (DPLL_CTRL_1.SMC=1): If a first direction change together with an input signal change (active edge) has happened, then for a consecutive direction change together with the next following input signal change the interrupt DPLL_DCGI does not occur. Workaround : When a direction change is detected by DPLL_IRQ_NOTIFY.DCGI the Register DPLL_STATUS.BWD1 can be checked after the next relevant input signal edge on TRIGGER. If a second direction change is detected with the very next relevant input signal, the DPLL_DCGI can be set by writing DPLL_IRQ_FORCINT.TRG_DCGI =1. The next relevant input signal edge is the next input signal edge for DPLL_CTRL_1.SMC=1 (In contrast to the next inactive input signal edge when DPLL_CTRL_1.SMC=0).	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0

Errata-ID	Errata	refer to
		v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120

GTM-IP-478	Title : DPLL: Incorrect calculation of DPLL_THVAL, DPLL_THVAL2 Scope : DPLL Severity : Low Classification : Non-critical Effects : Under the described conditions the values of DPLL_THVAL, DPLL_THVAL2 are incorrect. The divergence is small, but in theory this can still lead to a wrong direction decision as the THVAL is used for the evaluation of the direction change. As an example: In case of a 45/90us sensor input signal for this failure to happen means to have a difference of the filter values between active and inactive input signal edge on TRIGGER larger than 450 clock cycles in case of a 20MHz TBU_TS0 clock configuration. Description : In case of LOW_RES=1, DPLL_CTRL_1.SMC=0, DPLL_CTRL_0.IDT=1, and DPLL_CTRL_1.TS0_HRT=0 the values of DPLL_THVAL, DPLL_THVAL2 are calculated incorrectly because the filter values are not divided by 8 as specified. Workaround : If a negative effect on the direction decision is not expected no workaround is necessary. If a negative effect cannot be excluded the use of the filter values can be switched off by setting DPLL_CTRL_0.IDT=0.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0

Errata-ID	Errata	refer to
		v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120

GTM-IP-479	Title : SPEC-DPLL@GTM4_1: PSSC/PSTC behaviour description incorrect Scope : DPLL Severity : Low Classification : Non-critical Effects : The DPLL_PSSC.PSSC value is not updated at the following trigger slope but at the following STATE slope with the value DPLL_PSSC.PSSC=DPLL_PSSM.PSSM +/- correction value with correction value = DPLL_INC_CNT1.INC_CNT1 - DPLL_NMB_S.NMB_S. This might lead to an unexpected behaviour of the GTM IP. The DPLL_PSTC.PSTC value is not updated at the following STATE slope but at the following TRIGGER slope with the value DPLL_PSTC.PSTC=DPLL_PSTM.PSTM +/- correction value with correction value = DPLL_INC_CNT1.INC_CNT1 - DPLL_NMB_T.NMB_T. This might lead to an unexpected behaviour of the GTM IP. Description : When changing from normal to emergency mode (DPLL_CTRL_0.RMO = 0->1) the DPLL_PSSC.PSSC value is not calculated as specified. When changing from emergency to normal mode (DPLL_CTRL_0.RMO = 1->0) the DPLL_PSTC.PSTC value is not calculated as specified. The GTM4.1 specification error is a consequence of an incorrect specification update resulting from erratum GTM-IP-262. In the specification it is written: ... For changing from normal mode to emergency mode at the following STATE slope (according to the DPLL_CTRL_0.RMO value in the shadow register, the DPLL_PSSC.PSSC value is calculated by DPLL_PSSC.PSSC = DPLL_PSTC.PSTC. For changing from emergency mode to normal mode at the following TRIGGER slope (according to the DPLL_CTRL_0.RMO value in the shadow register, the DPLL_PSTC.PSTC value is calculated by DPLL_PSTC.PSTC = DPLL_PSSC.PSSC. In case of no further TRIGGER or STATE events the CPU has to perform the above corrections. Note: For DPLL_CTRL_1.SMC=0: TRIGGER and STATE are prepared to calculate SUB_INC1. The DPLL_CTRL_0.RMO bit gives a decision only, which of them is used. For changing from normal mode to emergency mode at the following STATE slope (according to the DPLL_CTRL_0.RMO value in the shadow register, stored in an independent shadow register for an active TRIGGER event and for DPLL_CTRL_1.DEN = 1.) the DPLL_PSSC.PSSC value is calculated by DPLL_PSSC.PSSC = DPLL_PSTC.PSTC. Note:	v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10

For changing from emergency mode to normal mode at the following TRIGGER slope (according to the DPLL_CTRL_0.RMO value in the shadow register, stored in an independent shadow register for an active STATE event and for DPLL_CTRL_1.DEN = 1.) the DPLL_PSTC.PSTC value is calculated by DPLL_PSTC.PSTC = DPLL_PSSC.PSSC. In case of no further TRIGGER or STATE events the CPU has to perform the above corrections.

Instead the following behaviour should be specified:
For changing from normal mode to emergency mode at the following STATE slope (according to DPLL_CTRL_0_SHADOW_STATE.RMO) the DPLL_PSSC.PSSC value is calculated by DPLL_PSSC.PSSC = DPLL_PSSM.PSSM + correction value (forward direction) or DPLL_PSSC.PSSC = DPLL_PSSM.PSSM - correction value (backward direction) with the correction value = DPLL_INC_CNT1.INC_CNT1 - DPLL_NMB_S.NMB_S.
For changing from emergency mode to normal mode at the following TRIGGER slope (according to DPLL_CTRL_0_SHADOW_TRIGGER.RMO) the DPLL_PSTC.PSTC value is calculated by DPLL_PSTC.PSTC = DPLL_PSTM.PSTM + correction value (forward direction) or DPLL_PSTC.PSTC = DPLL_PSTM.PSTM - correction value (backward direction) with the correction value = DPLL_INC_CNT1.INC_CNT1 - DPLL_NMB_T.NMB_T. In case no further TRIGGER or STATE events the CPU has to perform the above corrections.
DPLL_CTRL_0.RMO is stored to DPLL_CTRL_0_SHADOW_STATE.RMO on encountering an active STATE event if DPLL_CTRL_1.DEN = 1.
DPLL_CTRL_0.RMO is stored to DPLL_CTRL_0_SHADOW_TRIGGER.RMO on encountering an active TRIGGER event if DPLL_CTRL_1.DEN = 1.

Workaround :
1) If possible leave DPLL_PSSC.PSSC or DPLL_PSTC.PSTC as is.
If a different value for DPLL_PSSC.PSSC/DPLL_PSTC.PSTC is necessary the value could be written by CPU interface as already written in the specification. The modification could be done by MCS0 as well.

2) Alternatively, the application can disable the DPLL via DPLL_CTRL_1.DEN=0 and then re-start the DPLL in emergency or normal mode with the following sequence:
Setting up the DPLL modes as desired, for example (not mandatory values)
GTM_DPLL_CTRL_1.B.PIT = 1; -- only as an example
GTM_DPLL_CTRL_1.B.DMO = 0; -- only as an example
GTM_DPLL_CTRL_1.B.COA = 0; -- only as an example
GTM_DPLL_CTRL_1.B.SYSF = 1; -- only as an example
GTM_DPLL_CTRL_1.B.TSL = 1; -- only as an example
GTM_DPLL_CTRL_1.B.SSL = 3; -- only as an example
GTM_DPLL_CTRL_0.B.SEN/TEN = 1; -- only as an example
Then switch into emergency/normal mode and enable the DPLL again.
GTM_DPLL_CTRL_0.B.RMO = 1 or 0; -- only as an example
GTM_DPLL_CTRL_0.B.SEN/TEN = 1; -- only as an example
GTM_DPLL_CTRL_1.B.DEN = 1; -- only as an example
In this case the behaviour for DPLL_PSSC.PSSC/DPLL_PSTC.PSTC is different:
For DPLL_CTRL_0.RMO = 0->1:
DPLL_PSSC.PSSC=DPLL_PSSM.PSSM.
For DPLL_CTRL_0.RMO = 1->0: DPLL_PSTC.PSTC=DPLL_PSTM.PSTM.

Errata-ID	Errata	refer to
	If in this case nevertheless a different value for DPLL_PSSC.PSSC/DPLL_PSTC.PSTC is necessary the value could be written by CPU interface as already written in the specification. The modification could be done by MCS0 as well.	

Errata-ID	Errata	refer to
GTM-IP-480	Title : SPEC-TIM: Wrong action description for TPIM mode Scope : TIM Severity : Low Classification : Non-critical Effects : Contrary to the description, neither a capture nor an interrupt is triggered by a rising or falling edge of the input signal. Description : In TIM Pulse Integration Mode (TPIM) with External Capture (TIM[i]_CH[x]_CTRL.EXT_CAP_EN=1) the capture is done only with the external capture signal and not with the rising or falling edge of the TIM input signal. Therefore in the chapter describing the TPIM mode the action description in the table "Operation depending ..." (GTM4.1 spec.: TIM_2138) rows 2 and 4 are wrong. In both rows it is described that if inc_cnt == true, a capture as well as a TIM_NEWVAL_IRQ has to be executed. But this is not the case and has to be removed. Only the last line in both rows of the table ("inc_cnt=false") is correct. Workaround : Not applicable.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10

GTM-IP-481	Title : SPEC-TIM: Wrong description for TBCM mode Scope : TIM Severity : Low Classification : Non-critical Effects : The input signal level defined by TIM[i]_CH[x]_CTRL.DSL with TIM[i]_CH[x]_CTRL.ISL=0 is not taken into account. Description : In TIM Bit Compression Mode with External Capture (TIM[i]_CH[x]_CTRL.EXT_CAP_EN=1) the capture is done only with the external capture signal without dependency to the input signal level. Therefore the bit field TIM[i]_CH[x]_CTRL.ISL must be set to 1. The value 0 for TIM[i]_CH[x]_CTRL.ISL is prohibited. The bit field TIM[i]_CH[x]_CTRL.DSL is not relevant. The following specification sections in the TBCM chapter have to be adapted as follows: In the prose text: "If external capture is enabled, capturing is done for TIM[i]_CH[x]_CTRL.ISL=1 as defined in the next table. The value 0 for TIM[i]_CH[x]_CTRL.ISL is prohibited." In the Table: - In the action description of row 1 the part "TIM[i]_CH[x]_CNT++" has to be removed - All rows starting with row 3 have to be replaced with only one row where the content for the column of TIM[i]_CH[x]_CTRL.ISL has to be filled with "0 - prohibited". All other columns in row 3 have to be marked with "-" (Don't Care). Workaround : Hint: Do not configure TIM[i]_CH[x]_CTRL.ISL to 0 (which is actually prohibited).	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
		v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10

GTM-IP-482	Title : SPEC-TIM: Wrong description in TBCM mode regarding TIM[i]_CH[x]_CTRL.GPR1_SEL bit field Scope : TIM Severity : Low Classification : Non-critical Effects : The captured value depends on the bit field TIM[i]_CH[x]_CTRL.GPR1_SEL in contrast to the notion in the specification. Description : In TIM Bit Compression Mode it is described that the bit field TIM[i]_CH[x]_CTRL.GPR1_SEL is not applicable. That is not the case and therefore the sentence mentioning that the bit field TIM[i]_CH[x]_CTRL.GPR1_SEL " is not applicable in TBCM mode." in the section "TIM Bit Compression Mode" (GTM4.1 spec.: TIM_1055) has to be ignored. Workaround : Hint: The value of the bit field TIM[i]_CH[x]_CTRL.GPR1_SEL must be taken into account.	v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

Errata-ID	Errata	refer to
		@Specification v4.1.0-V1.10

Errata-ID	Errata	refer to
GTM-IP-483	Title : DPLL: Malfunction on changing DPLL_PVT.PVT Scope : DPLL Severity : Medium Classification : Non-critical Effects : Rejecting a TRIGGER only partially will ultimately lead to a wrong angle clock (CCM[0]_TBU_TS1) and wrong PMT calculations. Description : If the DPLL is operated in normal mode with DPLL_CTRL_11.INCF1 = 1, the calculation of the PVT check starts in the current increment (in the DPLL state DPLL_STA.STA_T = 0x58). The decision of whether to admit or to reject the upcoming active TRIGGER is then evaluated upon encountering it. If DPLL_PVT.PVT changes after DPLL_STA.STA_T = 0x58, the DPLL behaves as follows: 1. If the old DPLL_PVT.PVT (the one written before DPLL_STA.STA_T = 0x58) causes rejection and the new one causes admission: The upcoming TRIGGER will be (partially) rejected in the sense that DPLL_INC_CNT1.INC_CNT1 will not be updated as expected and therefore no micro ticks will be generated. However, erroneously the pointers (DPLL_APT.APT, DPLL_APT.APT_2B, DPLL_APT_2C.APT_2C) will be incremented and the respective memory structures (DPLL_RDT_T[p], DPLL_TSF_T[p], DPLL_ADT_T[p], DPLL_DT_T[p]) in RAM Region 2 will be updated. The DPLL_PWI interrupt will not be triggered although it should be. 2. If the old DPLL_PVT.PVT causes admission and the new one causes rejection: The old one is the decisive one. That is, the upcoming TRIGGER will be admitted as expected. 3. If both cause rejection: The upcoming TRIGGER is rejected (as expected). 4. If both cause admission: The upcoming TRIGGER is admitted (as expected). Workaround : Write DPLL_PVT.PVT only between DPLL_STA.STA_T = 0x8 and DPLL_STA.STA_T = 0x58. In order to do that timely, MCS[0] can be programmed as follows: 1. Suspend until DSTA.STA_T = 0x8 (by means of WURM instruction). 2. Write DPLL_PVT.PVT on resumption.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

Errata-ID	Errata	refer to
GTM-IP-486	Title : SPEC-DPLL: Incorrect ModifiedWriteValue attribute for bit fields in DPLL_STATUS Scope : DPLL Severity : Low Classification : Non-critical Effects : The current specified behavior falsely implies that there is no manipulation of the data written to the fields. The intended behavior is described as follows: a write-access to one of the bit fields with the data written as one results in clearing it. A write-access to one of the bit fields with the data written as zero results in nothing (the data stored is left unchanged). This makes the behavior of a write-access different from what the user expects which might, in turn, lead to misinterpretation and inconsistent diagnostics. Since these bit fields are only used for diagnostic purposes, their values do not (directly) impact the DPLL operation. Description : The bit fields DPLL_STATUS.FPCE, CSO, CTO, CRO, SOR, MS, TOR, MT, RAM2_ERR have their ModifiedWriteValue incorrectly set to 'nil'. It should rather be set to 'oneToClear'. These bit fields are used for diagnostic purposes only and their values do not impact DPLL operation. They are evaluated and updated by the DPLL in every active (STATE/TRIGGER) increment if specific conditions are met. The user can clear the bit fields to zero by writing ones to them. Workaround : Hint: In order to clear one of the bit fields, the user should perform a write-access with the data written as one. The bit fields are only set by hardware (DPLL). The user cannot set them to one. These bit fields are evaluated and updated by DPLL in every active (STATE/TRIGGER) increment. That is, a change driven by write-accesses in a particular increment does not persist and will be automatically rectified in the next increment.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10

GTM-IP-487	Title : GTM_AEI: Changing BRIDGE_MODE[2:0] in Pipeline mode can lead to violation of Pipeline protocol Scope : GTM_AEI Severity : Low Classification : Non-critical Effects : Transaction not terminated according to protocol, user might be stuck waiting for AEI_READY to be set. Description : The issue from erratum GTM-IP-421 ("GTM_AEI: Changing BRIDGE_MODE.MSK_WR_RSP in Pipeline mode can lead to violation of Pipeline protocol") not only appears when BRIDGE_MODE.MSK_WR_RSP changes, but also when it stays '1' while the other configuration bit fields in BRIDGE_MODE.BYPASS_SYNC and/or BRIDGE_MODE.BRG_MODE change. Please also check on erratum GTM-IP-488. Workaround : These workarounds match the workarounds from GTM-IP-421 1) Make sure the transaction preceding the write of the mentioned BRIDGE_MODE bit fields is a read transaction. OR 2) Integration dependent: Issue the write to the mentioned BRIDGE_MODE bit fields in standard mode instead of pipeline mode.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
		v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

GTM-IP-488	Title : GTM_AEI: Turning off BRIDGE_MODE.MSK_WR_RSP in asynchronous mode might lead to following transactions being corrupted Scope : GTM_AEI Severity : Low Classification : Non-critical Effects : Transaction not terminated according to protocol, user might be stuck waiting for AEI_READY to be set. Description : If the AEI bridge operates in asynchronous mode and in pipelined protocol, with Mask-Write-Response turned on (BRIDGE_MODE[2:0]=="011") and the BRIDGE_MODE.MSK_WR_RSP is turned off (by writing BRIDGE_MODE[2:0]="001"), the following transaction might be corrupted by the AEI_READY not being set. This is an issue like in GTM-IP-421 and GTM-IP-487 but another workaround is needed. Workaround : Change BRIDGE_MODE.MSK_WR_RSP together with setting the soft-Reset (pipeline writing BRIDGE_MODE[16:0]=h#10001)	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
		v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

Errata-ID	Errata	refer to
GTM-IP-490	Title : TOP: Interrupt from DPLL not detected in MCS0 Scope : MCS, DPLL, TOP Severity : Medium Classification : Non-critical Effects : Interrupt from DPLL cannot be detected in MCS0. Description : Some of the DPLL interrupts can be detected in the internal registers DSTA and DSTAX of MCS0. If the clock divider of cluster 0 is configured to 0b10 (2:1 clock ratio) inside GTM_CLS_CLK_CFG.CLS[0]_CLK_DIV and DPLL_IRQ_MODE.IRQ_MODE is configured to 0b01, 0b10, or 0b11, the interrupt pulse cannot be detected inside MCS0 due to an connectivity failure on GTM_IP top level and gets lost. Workaround : Workaround 1: Use interrupt level mode in DPLL by setting of DPLL_IRQ_MODE.IRQ_MODE=0b00. Workaround 2: Configure the cluster clock divider of cluster 0 to 1 by setting of GTM_CLS_CLK_CFG.CLS[0]_CLK_DIV=0b01.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

GTM-IP-492	Title : DPLL: Wrong value of DPLL_INC_CNT1.INC_CNT1 upon switching to normal mode Scope : DPLL Severity : Medium Classification : Non-critical Effects : (1) DPLL_CTRL_0.RMO: 1 -> 0 The generation of the extra micro ticks accumulated in DPLL_INC_CNT1.INC_CNT1 after encountering the first active TRIGGER input ultimately leads to wrong angle clock (manifests in wrong CCM[0]_TBU_TS1) and wrong PMT calculations (due to incorrect DPLL_PSTC.PSTC). Further effect, which is only applicable to GTM v4.1.0 devices: the value of DPLL_INC_CNT1.INC_CNT1 is not assigned to DPLL_MP_T.MP_T on the first active TRIGGER input (in contrast to what is specified in MP_T description in "DPLL_MP_T" (GTM4.1 specs: DPLL_16159)). Further observations without malicious effects: The value of the current position stamp is not assigned to DPLL_PSSM.PSSM at the active STATE input (in contrast to what is specified in "State description of the State Machine Table" step 21 (GTM4.1 spec.: DPLL_6908)). This is, however, insignificant because DPLL_PSSM.PSSM is deemed invalid in normal mode (see PSSM description in "Memory DPLL_PSSM" (GTM4.1 spec.: DPLL_6370)) and therefore should not be used/relied on. (2) DPLL_CTRL_0.RMO: 0 -> 1 Upon switching from normal to emergency mode (with DPLL_CTRL_1.SGE1 set to 1), the value of the current position stamp is not assigned to DPLL_PSTM.PSTM at the active TRIGGER input "State description of the State Machine Table" step 1 (GTM4.1 spec.: DPLL_6908)). This is, however, insignificant because DPLL_PSTM.PSTM is deemed invalid in emergency mode (see PSTM description in "Memory DPLL_PSTM" (GTM4.1 spec.: DPLL_6360)) and therefore should not be used/relied on. No effect is associated with not assigning the current position stamp to DPLL_PSSM.PSSM in normal mode and DPLL_PSTM.PSTM in emergency mode. Description : DPLL_CTRL_0.RMO 1 -> 0: Upon switching from emergency to normal mode (with DPLL_CTRL_1.SGE1 set to 1), DPLL_INC_CNT1.INC_CNT1 increments by DPLL_MLS1.MLS1 micro ticks every time an active STATE input is encountered till the first active TRIGGER input is encountered. The extra	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0

Errata-ID	Errata	refer to
	micro ticks accumulated in DPLL_INC_CNT1.INC_CNT1 will only be generated after encountering the first active TRIGGER. The described behavior is not intended because the STATE input is not supposed to contribute to the pulse generation in normal mode. Workaround : Two possible workarounds for DPLL_CTRL_0.RMO: 1 -> 0: (1) Defer setting DPLL_CTRL_1.SGE1 to 1 till the first DPLL_TASI interrupt is encountered (signaling the arrival of the first active TRIGGER). (2) Make sure that DPLL_MLS1.MLS1 is set to zero upon switching the mode. The user may then alter it on encountering the first DPLL_TASI interrupt.	v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

Errata-ID	Errata	refer to
GTM-IP-494	Title : MCS: Missing hazard detection for parallel memory write access Scope : MCS Severity : Medium Classification : Non-critical Effects : Corrupted memory content. Description : The MCS is configured in a scheduling mode unequal to round robin (MCS[i]_CTRL_STAT.SCD_MODE != 0b01) and is executing an instruction instr2 immediately after instruction instr1, which means that there is no delay in between both instructions. If instruction instr1 is a bus master read instruction that is executing a fast access (e.g. BRD R1, TIM_CH0_CTRL) and instruction instr2 is a memory write access that is executing a parallel memory access (e.g. MWRI R1, R2) via Harvard architecture: In this case the MCS does not resolve any hazard induced by a write after read data dependency between both instructions. As a consequence the data that is written by the parallel memory write access does not reflect the read data of instr1. Example for such a sequence: MOVL R1, 0xBAD7 ... BRD R1, TIM_CH0_CTRL #instr1 MWRI R1, R2, 0 #instr2 In the case of a fail in this example, the memory write access is writing the value 0xBAD7 instead of the content of configuration register TIM_CH0_CTRL. The following instructions are memory write access instructions that are affected by this erratum: MWR, MWRI, MWRIO, PUSH, CALL, and CALLI. Workaround : Add an additional NOP instruction between bus master read instruction and memory write instruction.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

Errata-ID	Errata	refer to
GTM-IP-495	Title : SPEC-CCM: Wrong initial values for bit fields in CCM[i]_CFG Scope : CCM Severity : Low Classification : Non-critical Effects : None. Description : The device-dependent bit fields EN_TIM, EN_TOM_SPE_TDTM, EN_ATOM_ADTM, EN_MCS, EN_DPLL_MAP, EN_BRC, EN_PSM, EN_CMP_MON of the register CCM[i]_CFG have their initial values set unconditionally to 1 (or to 'X' as in GTM specification v3.1.5.1). This is only correct for devices in which these bit fields are implemented. For devices in which these bit fields are not implemented they qualify as 'reserved' and hence an attempt to read them returns a 0 (GTM4.1 spec.: APP_16906). For that, the initial value must be 0 too in order to avoid any confusion/misinterpretation. In order to fix the specifications, the initial values must rather be a function of the device dependency: For EN_TIM (GTM4.1 spec.: CCM_542), the initial value must be NTIM > i. For EN_TOM_SPE_TDTM (GTM4.1 spec.: CCM_547), the initial value must be NTOM > i || NSPE > i. For EN_ATOM_ADTM (GTM4.1 spec.: CCM_550), the initial value must be NATOM > i. For EN_MCS (GTM4.1 spec.: CCM_553), the initial value must be NMCS > i. For EN_DPLL_MAP (GTM4.1 spec.: CCM_556), the initial value must be NDPLL > i. For EN_BRC (GTM4.1 spec.: CCM_559), the initial value must be NBRC > i. For EN_PSM (GTM4.1 spec.: CCM_562), the initial value must be NPSM > i. For EN_CMP_MON (GTM4.1 spec.: CCM_565), the initial value must be i == 1 && (NCMP > 0 || NMON > 0). Workaround : Not applicable.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10

GTM-IP-497	Title : SPEC-SPE wiring in figure is wrong Scope : SPE Severity : Low Classification : Non-critical Effects : The enabling of the affected TIM input signals of the SPE is not working as expected. Description : In the figure "SPE[i]_IN_PAT register representation" (GTM4.1 spec.: SPE_523 "SPE[i]_CTRL_STAT Register Representation"): The usage of the SIE inputs SIE0 and SIE2 need to be swapped. Workaround : Not applicable.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
		v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10

GTM-IP-499	Title : SPEC-CCM Wrong description of TIM auxiliary input signal selection Scope : CCM Severity : Low Classification : Non-critical Effects : The signals forwarded to the TIM auxiliary inputs (TIM[i]_AUX_IN[7:0]) are different from what the user expects. Description : The bit fields GTM_CFG.SRC_IN_MUX, CCM[i]_TIM_AUX_IN_SRC.SRC_CH0..7, CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[x] are used to define which/how signals (outputs from TOMs and ATOMs) are fed back to the TIMs via the auxiliary input (TIM[i]_AUX_IN[7:0]). The multiplexing circuitry is depicted in figure "TIM Auxiliary Input Multiplexing" (GTM4.1 spec: ARCH_2133). The problem is that the coding for the bit fields CCM[i]_TIM_AUX_IN_SRC.SRC_CH0..7, CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[x] is incorrect. Here is a summary of the changes required to fix that, with referencing the TAGs of the GTM4.1 specification: 1. Fix the coding for CCM[i]_TIM_AUX_IN_SRC.SRC_CH0..7: For the SRC_CH0 (CCM_1259): CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[0] == 1 0 : DTM0 of instance [i] Output DTM_OUT1[1:1] selected 1 : DTM4 of instance [i] Output DTM_OUT1[1:1] selected For the SRC_CH1 (CCM_1260): CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[1] == 1 0 : DTM0 of instance [i] Output DTM_OUT1[2:2] selected 1 : DTM4 of instance [i] Output DTM_OUT1[2:2] selected For the SRC_CH2 (CCM_1261): CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH2] == 1 0 : DTM0 of instance [i] Output DTM_OUT1[3:3] selected 1 : DTM4 of instance [i] Output DTM_OUT1[3:3] selected For the SRC_CH3 (CCM_1262): CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[3] == 1 0 : DTM1 of instance [i] Output DTM_OUT1[0:0] selected 1 : DTM5 of instance [i] Output DTM_OUT1[0:0] selected For the SRC_CH4 (CCM_1263): CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[4] == 1 0 : DTM1 of instance [i] Output DTM_OUT1[1:1] selected	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10

	1 : DTM5 of instance [i] Output DTM_OUT1[1:1] selected For the SRC_CH5 (CCM_1264): CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[5] == 1 0 : DTM1 of instance [i] Output DTM_OUT1[2:2] selected 1 : DTM5 of instance [i] Output DTM_OUT1[2:2] selected For the SRC_CH6 (CCM_1265): CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[6] == 1 0 : DTM1 of instance [i] Output DTM_OUT1[3:3] selected 1 : DTM5 of instance [i] Output DTM_OUT1[3:3] selected For the SRC_CH7 (CCM_1266): CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[7] == 1 0 : DTM0 of instance [i] Output DTM_OUT1[0:0] selected 1 : DTM4 of instance [i] Output DTM_OUT1[0:0] selected For SRC_CH0, replace CCM_1127 with two new codings: CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[0] == 0 AND GTM_CFG.SRC_IN_MUX == 0 0 : DTM[h/4] of instance [k] Output DTM_OUT0[0:0] selected where h = mod(i, 2)*8 and k = i/2 1 : DTM4 of instance [i] Output DTM_OUT0[0:0] selected CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[0] == 0 AND GTM_CFG.SRC_IN_MUX == 1 0 : DTM0 of instance [i] Output DTM_OUT0[0:0] selected 1 : DTM4 of instance [i] Output DTM_OUT0[0:0] selected For SRC_CH1, replace CCM_1129 with two new codings: CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[1] == 0 AND GTM_CFG.SRC_IN_MUX == 0 0 : DTM[h/4] of instance [k] Output DTM_OUT0[1:1] selected where h = mod(i, 2)*8 and k = i/2 1 : DTM4 of instance [i] Output DTM_OUT0[1:1] selected CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[1] == 0 AND GTM_CFG.SRC_IN_MUX == 1 0 : DTM0 of instance [i] Output DTM_OUT0[1:1] selected 1 : DTM4 of instance [i] Output DTM_OUT0[1:1] selected For SRC_CH2, replace CCM_1131 with two new codings: CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[2] == 0 AND GTM_CFG.SRC_IN_MUX == 0 0 : DTM[h/4] of instance [k] Output DTM_OUT0[2:2] selected where h = mod(i, 2)*8 and k = i/2 1 : DTM4 of instance [i] Output DTM_OUT0[2:2] selected CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[2] == 0 AND GTM_CFG.SRC_IN_MUX == 1 0 : DTM0 of instance [i] Output DTM_OUT0[2:2] selected 1 : DTM4 of instance [i] Output DTM_OUT0[2:2] selected For SRC_CH3, replace CCM_1133 with two new codings: CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[3] == 0 AND GTM_CFG.SRC_IN_MUX == 0 0 : DTM[h/4] of instance [k] Output DTM_OUT0[3:3] selected where h = mod(i, 2)*8 and k = i/2 1 : DTM4 of instance [i] Output DTM_OUT0[3:3] selected	

	CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[3] == 0 AND GTM_CFG.SRC_IN_MUX == 1 0 : DTM0 of instance [i] Output DTM_OUT0[3:3] selected 1 : DTM4 of instance [i] Output DTM_OUT0[3:3] selected For SRC_CH4, replace CCM_1135 with two new codings: CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[4] == 0 AND GTM_CFG.SRC_IN_MUX == 0 0 : DTM[h/4+1] of instance [k] Output DTM_OUT0[0:0] selected where h = mod(i, 2)*8 and k = i/2 1 : DTM5 of instance [i] Output DTM_OUT0[0:0] selected CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[4] == 0 AND GTM_CFG.SRC_IN_MUX == 1 0 : DTM1 of instance [i] Output DTM_OUT0[0:0] selected 1 : DTM5 of instance [i] Output DTM_OUT0[0:0] selected For SRC_CH5, replace CCM_1137 with two new codings: CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[5] == 0 AND GTM_CFG.SRC_IN_MUX == 0 0 : DTM[h/4+1] of instance [k] Output DTM_OUT0[1:1] selected where h = mod(i, 2)*8 and k = i/2 1 : DTM5 of instance [i] Output DTM_OUT0[1:1] selected CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[5] == 0 AND GTM_CFG.SRC_IN_MUX == 1 0 : DTM1 of instance [i] Output DTM_OUT0[1:1] selected 1 : DTM5 of instance [i] Output DTM_OUT0[1:1] selected For SRC_CH6, replace CCM_1139 with two new codings: CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[6] == 0 AND GTM_CFG.SRC_IN_MUX == 0 0 : DTM[h/4+1] of instance [k] Output DTM_OUT0[2:2] selected where h = mod(i, 2)*8 and k = i/2 1 : DTM5 of instance [i] Output DTM_OUT0[2:2] selected CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[6] == 0 AND GTM_CFG.SRC_IN_MUX == 1 0 : DTM1 of instance [i] Output DTM_OUT0[2:2] selected 1 : DTM5 of instance [i] Output DTM_OUT0[2:2] selected For SRC_CH7, replace CCM_1141 with two new codings: CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[7] == 0 AND GTM_CFG.SRC_IN_MUX == 0 0 : DTM[h/4+1] of instance [k] Output DTM_OUT0[3:3] selected where h = mod(i, 2)*8 and k = i/2 1 : DTM5 of instance [i] Output DTM_OUT0[3:3] selected CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[7] == 0 AND GTM_CFG.SRC_IN_MUX == 1 0 : DTM1 of instance [i] Output DTM_OUT0[3:3] selected 1 : DTM5 of instance [i] Output DTM_OUT0[3:3] selected 2. Fix the coding for CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[x]: i. Delete CCM_3112 as the note is incorrect. ii. Fix the coding in CCM_1145: 0 : Use DTM_OUT0[q:q] signal as CCM_AUX_IN source of TIM[i] channel x; q = mod(x, 4)	

Errata-ID	Errata	refer to
	1 : Use DTM_OUT1[q:q] signal as CCM_AUX_IN source of TIM[i] channel x; q = mod(x+1, 4) Workaround : Hint: Base the selection on what is depicted in figure "TIM Auxiliary Input Multiplexing" (GTM4.1 spec: ARCH_2133) instead of the bit field coding for CCM[i]_TIM_AUX_IN_SRC.SRC_CH0..7 and CCM[i]_TIM_AUX_IN_SRC.SEL_OUT_N_CH[x].	

Errata-ID	Errata	refer to
GTM-IP-500	Title : SPEC-CCM/CMU Wrong clock resolution name used Scope : CCM/CMU Severity : Low Classification : Non-critical Effects : The signal, routed from CCM to CMU, which can be selected as a source for clock resolution (CMU_CLK_RES[6:6]) is different from what the user expects. Description : The output clock resolution from the CCM (CCM[0]_CLK_RES[7:7]) is fed back to the CMU in which it can be used as a source for CMU_CLK_RES[6:6] by appropriately configuring CMU_CLK_6_CTRL.CLK_SEL. The problem is that in CCM_698, CCM_699, CMU_1314, CMU_1371, CMU_1415 another clock resolution is referenced instead - namely CCM[0]_CLK_RES[6:6] using index 6 instead of 7. Here are the changes required to fix the specifications: 1. Fix the labels in the figures CCM_699 (remove wrong label CCM[0]_CLK_RES[6:6] used within block "CMU") and CMU_1314 (replace index 6 with 7). 2. Change CCM_698 to: Figure "CCM_699" shows important details about the wiring of the cluster's local clock signals. It is worth mentioning that CCM[0]_CLK_RES[7:7] is routed to the CMU module in which it can be used for clock resolution generation. 3. Change the bit field coding for CMU_CLK_6_CTRL.CLK_SEL (CMU_1371) to actually reference CCM[0]_CLK_RES[7:7]: NDPLL == 1 0b00 : Use output of clock resolution generator 6 0b01 : Use signal SUB_INC2 of module DPLL 0b10 : Use signal SUB_INC1C of module DPLL 0b11 : Use signal CCM[0]_CLK_RES[7:7] of sub-module CCM0 4. Change the bit field coding for CMU_CLK_6_CTRL.CLK_SEL (CMU_1415) to actually reference CCM[0]_CLK_RES[7:7]: NDPLL == 0 0b00 : Use output of clock resolution generator 6 0b01 : input tied to low, no DPLL present in device 0b10 : input tied to low, no DPLL present in device 0b11 : Use signal CCM[0]_CLK_RES[7:7] of sub-module CCM0 Workaround : Not applicable.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10

GTM-IP-501	Title : SPEC-TIO Incomplete specification of init trigger Scope : TIO Severity : Low Classification : Non-critical Effects : A TIO channel might behave different from what the user expects reading the specification. Description : The following is applicable if a TIO channel is configured as a cyclic buffer (TIO[i]_G[g]_CH[c]_CTRL.PL_CYCLIC_BUFF = 1) and the init trigger is enabled (TIO[i]_G[g]_CH[c]_CTRL.PL_CYCLIC_INIT_TRIG_EN = 1). Under this configuration, only one of the two resources is allowed to have INSTR_PULL_EN = 0 (see TIO_1645). Intended behavior: If a pulse is encountered on init trigger (CYCLIC_INIT_TRIG[c:c]), the resource that has its INSTR_PULL_EN bit field set to 0 is loaded to the S resource. The other one is loaded to the O resource. Once the loading of the resources is performed, the TIO instruction is initialized appropriately regardless of whether there was an exchange or not. Specification deficiency: The behavior of an init trigger that does not result in an exchange is not sufficiently specified. Here are the changes required to fix the specifications: 1. Change TIO_15123 to: On every init trigger event CYCLIC_INIT_TRIG[c:c] = 1 and TIO[i]_G[g]_CH[c]_OINST.INSTR_PULL_EN = 0 the register exchange is initiated: 2. Change TIO_1648 to: - TIO[i]_G[g]_CH[c]_SINST at (t+1) = TIO[i]_G[g]_CH[c]_OINST at (t); - TIO[i]_G[g]_CH[c]_OINST at (t+1) = TIO[i]_G[g]_CH[c]_SINST at (t); 3. Add the following directly after TIO_1648: i. TIO_15259: On every init trigger event CYCLIC_INIT_TRIG[c:c] = 1: ii. TIO_15247: - In case the S resource operates a count instruction TIO[i]_G[g]_CH[c]_CTRL.PL_S_MODE = 0b1−, the instruction initializes by setting the internal register ITERA_CNT[c] at (t+1) to TIO[i]_G[g]_CH[c]_OINST.CMD[4:3] at (t) if TIO[i]_G[g]_CH[c]_OINST.INSTR_PULL_EN at (t) = 0. If TIO[i]_G[g]_CH[c]_OINST.INSTR_PULL_EN at (t) = 1, the instruction initializes by setting the internal register ITER_CNT[c] at (t+1) to TIO[i]_G[g]_Ch[c]_SINST.CMD[4:3] at (t).	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10

Errata-ID	Errata	refer to
	- In case the O resource operates a shift instruction TIO[i]_G[g]_CH[c]_CTRL.PL_O_MODE = 0b01−, the instruction initializes by setting the internal register TIO[i]_G[g]_CH[c]_SHIFTCNT to 0. - In case the O resource operates a compare instruction TIO[i]_G[g]_CH[c]_CTRL.PL_O_MODE = 0b10−|0b110, the instruction initializes by setting the internal register CMP_EVT_EN[c:c], CMP_EVT_PREV_EN[c:c] according to the active dual compare instruction. In addition, compare events which have occurred during a previous activation will be cleared. Workaround : Not applicable.	

GTM-IP-502	Title : SPEC-DPLL Input selection for SUB_INC1 is incomplete Scope : DPLL Severity : Low Classification : Non-critical Effects : DPLL behaves in an unspecified manner if DPLL_CTRL_0_SHADOW_TRIGGER.RMO ≠ DPLL_CTRL_0_SHADOW_STATE.RMO. Description : The bit field DPLL_CTRL_0_SHADOW_TRIGGER.RMO is updated on active TRIGGER input, whereas DPLL_CTRL_0_SHADOW_STATE.RMO is updated on active STATE input. The active TRIGGER input and active STATE input might arrive at different times. Therefore, on a switch from normal mode to emergency mode (or the other way around), the two bit fields might be updated at different points in time leading to them having different values. The SPEC deficiency: The coding for DPLL_CTRL_0_SHADOW_TRIGGER.RMO (GTM4.1 spec.: DPLL_16133) and for bit field DPLL_CTRL_0_SHADOW_STATE.RMO (GTM4.1 spec.: DPLL_16132) does not take into account that the two bit fields may have different values. As a consequence it is ambiguous which input contributes to the calculation of INC_CNT1. In order to fix the specification: Add a note to bit field DPLL_CTRL_0_SHADOW_TRIGGER.RMO and also to bit field DPLL_CTRL_0_SHADOW_STATE.RMO: The coding is applicable if DPLL_CTRL_0_SHADOW_TRIGGER.RMO = DPLL_CTRL_0_SHADOW_STATE.RMO. If not (they are unequal) the DPLL_CTRL_0.RMO defines which input is evaluated: STATE is selected if DPLL_CTRL_0.RMO=1 else TRIGGER is selected. Workaround : Not applicable.	v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1

Errata-ID	Errata	refer to
		v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10

GTM-IP-504	Title : SPEC-DPLL Wrong description of DPLL_CTRL_11.ACBU Scope : DPLL Severity : Low Classification : Non-critical Effects : The ambiguity in the specification might lead to a misunderstanding of the mechanism the DPLL uses to determine if a PMT Action is in the past. Description : The DPLL can be used to perform up to 32 PMT calculations. The DPLL_CTRL_11.ACBU bit field, in conjunction with DPLL_ACB_[n].ACB_[m] (0 <= n <= 7, 0 <= m <= 3), is used to tell the DPLL whether time, position, or both is/are used to evaluate if a PMT calculation (with index z = n*4 + m) is in the past. Intended behavior: If DPLL_CTRL_11.ACBU = 0: The DPLL uses time as a basis for determining if a PMT calculation (with index z) is in the past - regardless of DPLL_ACB_[n].ACB_[m]. If DPLL_CTRL_11.ACBU = 1: The DPLL uses time as a basis for determining if a PMT calculation (with index z) is in the past if DPLL_ACB_[n].ACB_[m][0:0] = 1. The DPLL uses position as a basis for determining if a PMT calculation (with index z) is in the past if DPLL_ACB_[n].ACB_[m][1:1] = 1. If DPLL_ACB_[n].ACB_[m][0:0] = 1 and DPLL_ACB_[n].ACB_[m][1:1] = 1, both time and position are used as a basis for the same. The specification deficiency: The description and coding of DPLL_CTRL_11.ACBU (DPLL_9014 and DPLL_9015) are misleading due to referring to the wrong registers. The same applies for the note (DPLL_9016). Here are the changes required to fix the specifications: 1. Change the description for DPLL_ACB_[n].ACB_[m] (DPLL_6844) to: Action Control Bits of Action [n*4+m] 2. Change the description for DPLL_CTRL_11.ACBU (DPLL_9014) to: Use DPLL_ACB_[n].ACB_[m]. The DPLL_ACB_[n].ACB_[m] values of PMTR are used to decide if an Action is in the past 3. Change the coding (DPLL_9015) for CTRL_11.ACBU to: 0 : The decision if an Action with index n*4+m is in the past is made considering the calculated time value regardless of the value of DPLL_ACB_[n].ACB_[m]. 1 : For an Action with index n*4+m, DPLL_ACB_[n].ACB_[m] values are considered as follows: if DPLL_ACB_[n].ACB_[m][1:1] = 1, the calculated position value is used to decide whether the Action is in the past. If DPLL_ACB_[n].ACB_[m][0:0] = 1, the calculated time value is used to	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10

Errata-ID	Errata	refer to
	decide whether the Action is in the past. DPLL_ACB_[n].ACB_[m][1:1] and DPLL_ACB_[n].ACB_[m][0:0] can be set also simultaneously to 1. 4. Change the note (DPLL_9016) under CTRL_11.ACBU to: Return DPLL_ACB_[n].ACB_[m] values together with Actions as zero, when the Actions are in future; set the ARU Control Bit (ACB) with index 1 to 1, when calculated position value is in the past and the DPLL_ACB_[n].ACB_[m][1:1] of the respective PMTR with index n*4+m was 1. Set the ARU Control Bit (ACB) with index 0 to 1, when calculated time value is in the past and the DPLL_ACB_[n].ACB_[m][0:0] of the respective PMTR with index n*4+m was 1. The value of DPLL_CTRL_11.ACBU can be only written when DPLL_CTRL_11.WACBU = 1. Workaround : Not applicable.	

Errata-ID	Errata	refer to
GTM-IP-506	Title : MCS: Unexpected parallel memory access on ECC error Scope : MCS Severity : Low Classification : Non-critical Effects : Unexpected memory access beside an active ECC error. Description : If the MCS from cluster i fetches a memory access instruction where an ECC error is reported on its input MCSi_RAMx_ECC_ERR, the initiating MCS channel is stopped reliably and the ECC error is reported as expected. However, if the corrupted memory access instruction code would be a parallel memory access, the MCS will initiate that memory access instead of suppressing it. Workaround : No workaround available.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

GTM-IP-507	Title : DPLL: Unregular pulse generation and wrong PMT results Scope : DPLL Severity : High Classification : Non-critical Effects : 1) Wrong pulse generation frequency because of incorrect prediction. This leads to unregular pulse distributions. 2) Wrong PMT results Description : With the configuration of DPLL_CTRL_NUTC.NUTE = 2*(DPLL_CTRL_0.TNU +1)-1 for TRIGGER or DPLL_CTRL_NUSC.NUSE = 2* (DPLL_CTRL_0.SNU +1) -1 for STATE the prediction of the pulse generation frequency is incorrect. This results in unregular pulse generation and wrong PMT results. This problem occurs on either CCM[0]_TBU_TS1 or CCM[0]_TBU_TS2 or both depending on the DPLL operation mode (normal or emergency mode, or synchronous motor control). Workaround : Avoid these configurations: DPLL_CTRL_NUTC.NUTE = 2*(DPLL_CTRL_0.TNU +1)-1 or DPLL_CTRL_NUSC.NUSE = 2* (DPLL_CTRL_0.SNU +1) -1. Instead, use for example full scale configurations as described in the specification.	v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1

Errata-ID	Errata	refer to
		v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

Errata-ID	Errata	refer to
GTM-IP-508	Title : MCS: Unexpected parallel memory access after MCS error Scope : MCS Severity : Low Classification : Non-critical Effects : Unexpected memory access after entering MCS error state. Description : If an MCS enters an error state (e.g. due to a division by zero) and its pipeline has already fetched a subsequent memory access instruction with a parallel memory access, the access is initiated although the instruction should be suppressed. The unexpected memory access occurs only, if the MCS is not configured in round robin mode and the delay between the occurrence of the error and the memory access instruction is either 1 or 2 cluster clock cycles. Workaround : Change scheduling of MCS program in a way that no parallel memory access can occur only after 2 cluster clock cycles of an instruction that can possibly enter the error state (e.g. adding 2 extra NOPs).	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

Errata-ID	Errata	refer to
GTM-IP-510	Title : SPEC-ATOM: Wrong update description of SL in SOMS mode Scope : ATOM Severity : Low Classification : Non-critical Effects : Described functionality of synchronous update of ATOM[i]_CH[x]_CTRL.SL does not exists and hence the hardware is behaving different as the user might expect. Description : In the ATOM Channel Architecture chapter of the ATOM specification, it is mentioned (ATOM_5145) that the synchronous shadow register update of ATOM[i]_CH[x]_CTRL_SOMS.SL exists in SOMP and SOMS mode. But the shadow register update of ATOM[i]_CH[x]_CTRL_SOMS.SL is not intended for SOMS mode and hence does not exist. Therefore, the following sentence ATOM_5145 in the specification must be changed accordingly: "In SOMP and SOMS mode, it is possible to synchronously update the clock resolution register ATOM[i]_CH[x]_CTRL.CLK_SRC, the signal level register ATOM[i]_CH[x]_CTRL.SL, the operation registers ATOM[i]_CH[x]_CM0.CM0 and ATOM[i]_CH[x]_CM1.CM1 from their shadow registers." The replacement is: "In SOMP and SOMS mode, it is possible to synchronously update the clock resolution register ATOM[i]_CH[x]_CTRL.CLK_SRC and the operation registers ATOM[i]_CH[x]_CM0.CM0 and ATOM[i]_CH[x]_CM1.CM1 from their shadow registers. In addition, synchronous updating of the signal level register ATOM[i]_CH[x]_CTRL.SL is possible in SOMP mode. Workaround : Not applicable.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10 v4.1.0-V1.20

Errata-ID	Errata	refer to
GTM-IP-511	Title : SPEC-TOM: Wrong figure for TOM channel architecture Scope : TOM Severity : Low Classification : Non-critical Effects : Erroneous figure may lead to wrong expectations among customers. Description : In TOM sub-chapter "TOM Channel 8..14 architecture" the figure is wrong. Firstly, in the top right corner of the figure the designation "x: 15" must be replaced by "x: 8,9,...,14". Secondly, there is a BITREV logic block between the sub-blocks CCU0 and CCU1, which must be removed from the existing connection. Workaround : Not applicable	v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD

GTM-IP-512	Title : SPEC-SPE: Wrong signal names Scope : SPE Severity : Low Classification : Non-critical Effects : The user may draw wrong conclusions how the masking of the SPE pattern works. Description : In SPE Submodule chapter figure "SPE Submodule Architecture" (GTM 4.1.0 spec.: SPE_858) contains wrong signal names. The following replacements need to be done in the SPE_PAT register table ("Pattern bits"): - TIM_CHx[48] to be replaced by NIP_MASK[0] - TIM_CHy[48] to be replaced by NIP_MASK[1] - TIM_CHz[48] to be replaced by NIP_MASK[2] Workaround : Not applicable.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
		v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10 v4.1.0-V1.20

Errata-ID	Errata	refer to
GTM-IP-513	Title : SPEC-ATOM: Wrong register referenced Scope : ATOM Severity : Low Classification : Non-critical Effects : Using the wrong register might lead to the ATOM operating different from what the user the expects. Description : In ATOM chapter "SOMC Mode under ARU control" the table ATOM_652 which defines the output behavior, refers to the wrong bit field ATOM[i]_CH[x]_CTRL_SOMC.ACB42. The correct bit field reference is ATOM[i]_CH[x]_STAT.ACBI[4:2], which should be used in the last column "Output behavior" of the table. Workaround : Not applicable.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10 v4.1.0-V1.20

Errata-ID	Errata	refer to
GTM-IP-514	Title : SPEC-ATOM: Wrong description in SOMB table Scope : ATOM Severity : Low Classification : Non-critical Effects : The output behaviour is described wrong and hence the hardware is behaving different as the user might expect. Description : The table ATOM_1871 in ATOM SOMB mode chapter, which describes the comparison strategies, line 7 for coding "110" states that the output signal level is defined by the CCU0 comparison match. This is incorrect and should be replaced with CCU1 comparison match instead. Further, the same line describes that the output level is toggled when there is a CCU1 comparison match. This is wrong and must be deleted. Workaround : Not applicable.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10 v4.1.0-V1.20

Errata-ID	Errata	refer to
GTM-IP-515	Title : SPEC-MCS: Incomplete usage of term CPU in MCS chapter Scope : MCS Severity : Low Classification : Non-critical Effects : The description in the specification erroneously limits the accessibility of registers and bit fields to CPU only. Description : The MCS Spec describes in several parts that a register or a bit field can only be accessed by CPU although it can be accessed by CPU and MCS AEI bus master interface. This erratum applies to the following sections in the specifications: GTM 4.1.0 spec.: MCS_2119, MCS_3085, MCS_6805 GTM 3.1.x spec.: section 15.11.6 GTM 3.5 spec.: section 17.10.6 Workaround : Not applicable.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10 v4.1.0-V1.20

GTM-IP-516	Title : SPE-RTL: IRQ raised on disabled inputs Scope : SPE Severity : Medium Classification : Non-critical Effects : An interrupt will be raised on masked input signals instead of ignoring these. Description : The inputs for the interrupt generation of the SPE[i]_IRQ_NOTIFY.SPE_PERR are not fed by the masked input signals. Hence an interrupt SPE[i]_IRQ_NOTIFY.SPE_PERR will occur when there is a pattern mismatch detected on the corresponding TIM channels beside active masking (SPE[i]_CTRL_STAT.SIE(k)=0). Workaround : Do not toggle (it is not use) the TIM channels that are disabled on the input side of the SPE.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
		v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

GTM-IP-517	Title : (A)TOM: Missing edge on output signal (A)TOM_OUT Scope : TOM, ATOM Severity : Medium Classification : Non-critical Effects : Missing edge on output signal (A)TOM_OUT. Description : If an (A)TOM channel is configured to be triggered by a previous channel by setting of (A)TOM[i]_CH[x]_CTRL.RST_CCU0=1 (SOMP mode in ATOM) and there is a pipeline/synchronization register within the trigger chain between the triggering channel and the triggered channel, the edge to the inverse SL at the output signal (A)TOM_OUT is not generated for (A)TOM[i]_CH[x]_CM1.CM1<2 and (A)TOM[i]_CH[x]_CM0.CM0>(A)TOM[i]_CH[x]_CM1.CM1. The problem only occurs if the selected clock resolution for the triggered channel has a divider factor of more than 1 related to the cluster clock CLS[i]_CLK. Since GTM Gen3, the problem does not occur if the pipeline/synchronization register is internally of (A)TOM module and the clock divider for the cluster clock CLS[i]_CLK is configured with a clock divider of 2 by setting of GTM_CLS_CLK_CFG.CLS[j]_CLK_DIV = 0b10. Hint: To find the relevant places in the specification versions v1.x and v2.x, search for "trigger chain" instead of "pipeline register" or "synchronization register". Workaround : Workaround 1: If available use channels without a pipeline/synchronization register within the trigger chain between the triggering channel and the triggered channel. Workaround 2a - Applicable for the error case with (A)TOM[i]_CH[x]_CM1.CM1=1: Switch the order of the edges, so that (A)TOM[i]_CH[x]_CM0.CM0 defines the first edge and (A)TOM[i]_CH[x]_CM1.CM1 the second edge. Additionally invert the SL value to get the same waveform on the output signal (A)TOM_OUT. Note: In this case, to generate 0% duty cycle, still use (A)TOM[i]_CH[x]_CM1.CM1=0 and (A)TOM[i]_CH[x]_CM0.CM0>MAX. Workaround 2b - Applicable for the error case with (A)TOM[i]_CH[x]_CM1.CM1=0: Set (A)TOM[i]_CH[x]_CM0.CM0=MAX and (A)TOM[i]_CH[x]_SR0.SR0=MAX by writing them before the target period. Set (A)TOM[i]_CH[x]_CM1.CM1 to the original application value of (A)TOM[i]_CH[x]_CM0.CM0. Additionally invert the SL value to get the same waveform on the output signal (A)TOM_OUT.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
	Workaround 3: Use a clock resolution for the triggered channel with a divider value of 1 related to the cluster clock.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

GTM-IP-518	Title : SPEC-DPLL: Incorrect bit field names Scope : DPLL Severity : Low Classification : Non-critical Effects : Using the wrong set of bit fields or a mix of both might lead to the DPLL operating different from what the user the expects. Description : The DPLL supports up to 64 STATE events in FULL_SCALE. By setting DPLL_CTRL_11.STATE_EXT to 1, the DPLL state extension is enabled (see MCS2DPLL_500) and the support is extended to up to 128 STATE events in FULL_SCALE. For that, the DPLL offers two sets of registers - one is considered when the state extension is not in use, and the other is considered when it is in use. The bit fields considered if the state extension is not in use: DPLL_NUSC.SYN_S DPLL_NUTC.SYN_S_OLD DPLL_NUTC.WSYN DPLL_NUTC.FSS DPLL_NUTC.VSN DPLL_NUTC.WNUS DPLL_NUTC.WVSN DPLL_APS.WAPS DPLL_APS.APS DPLL_APS.WAPS_1C2 DPLL_APS.APS_1C2 DPLL_APS_1C3.APS_1C3 DPLL_APS_SYNC.APS_1C2_EXT DPLL_APS_SYNC.APS_1C2_STATUS DPLL_APS_SYNC.APS_1C2_OLD DPLL_CTRL_0.SNU DPLL_CTRL_1.SYN_NS The corresponding bit fields considered if the state extension is in use: DPLL_NUSC_EXT1.SYN_S DPLL_NUSC_EXT1.SYN_S_OLD DPLL_NUSC_EXT1.WSYN DPLL_NUSC_EXT2.FSS DPLL_NUSC_EXT2.VSN DPLL_NUSC_EXT2.WNUS DPLL_NUSC_EXT2.WVSN DPLL_APS_EXT.WAPS DPLL_APS_EXT.APS DPLL_APS_EXT.WAPS_1C2 DPLL_APS_EXT.APS_1C2 DPLL_APS_1C3_EXT.APS_1C3 DPLL_APS_SYNC_EXT.APS_1C2_EXT	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10 v4.1.0-V1.20

DPLL_APS_SYNC_EXT.APS_1C2_STATUS
DPLL_APS_SYNC_EXT.APS_1C2_OLD
DPLL_CTRL_EXT.SNU
DPLL_CTRL_EXT.SYN_NS

Specification deficiency:
In several places throughout the DPLL chapter, the listed bit fields were not used correctly. Example: In DPLL_10067: DPLL_CTRL_0.SNU is used when it should be DPLL_CTRL_EXT.SNU.

In order to fix the specifications:
1. Add a subsection directly after DPLL_51740 in order to introduce a list of variables that will be used throughout the chapter:
State Extension:
By default, the DPLL supports up to 64 STATE events in FULL_SCALE. By setting DPLL_CTRL_11.STATE_EXT to 1, the DPLL state extension is enabled (see MCS2DPLL_500) and the support is extended to up to 128 STATE events in FULL_SCALE. When the state extension is used, the data structures (DPLL_RDT_S[p], DPLL_TSF_S[p], DPLL_ADT_S[p], DPLL_DT_S[p]) in RAM1c are not used. The data structures are instead emulated/managed by MCS[0].
The variables defined in this table are used throughout the chapter:
Variable	Refers to (if DPLL_CTRL_11.STATE_EXT == 0)	Refers to (if DPLL_CTRL_11.STATE_EXT == 1)
DPLL_NUSC_SYN_S	DPLL_NUSC.SYN_S	DPLL_NUSC_EXT1.SYN_S
DPLL_NUSC_SYN_S_OLD	DPLL_NUSC.SYN_S_OLD	DPLL_NUSC_EXT1.SYN_S_OLD
DPLL_NUSC_NUSE	DPLL_NUSC.NUSE	DPLL_NUSC_EXT2.NUSE
DPLL_NUSC_FSS	DPLL_NUSC.FSS	DPLL_NUSC_EXT2.FSS
DPLL_NUSC_VSN	DPLL_NUSC.VSN	DPLL_NUSC_EXT2.VSN
DPLL_APS_APS	DPLL_APS.APS	DPLL_APS_EXT.APS
DPLL_APS_1C2	DPLL_APS.APS_1C2	DPLL_APS_EXT.APS_1C2
DPLL_APS_1C3	DPLL_APS_1C3.APS_1C3	DPLL_APS_1C3_EXT.APS_1C3
DPLL_APS_SYNC_APS_1C2_EXT	DPLL_APS_SYNC.APS_1C2_EXT	DPLL_APS_SYNC_EXT.APS_1C2_EXT
DPLL_APS_SYNC_APS_1C2_STATUS	DPLL_APS_SYNC.APS_1C2_STATUS	DPLL_APS_SYNC_EXT.APS_1C2_STATUS
DPLL_APS_SYNC_APS_1C2_OLD	DPLL_APS_SYNC.APS_1C2_OLD	DPLL_APS_SYNC_EXT.APS_1C2_OLD
DPLL_SNU	DPLL_CTRL_0.SNU	DPLL_CTRL_EXT.SNU
DPLL_SYN_NS	DPLL_CTRL_1.SYN_NS	DPLL_CTRL_EXT.SYN_NS

2. Apply the following changes:
Index	Change	Tags
1	DPLL_APS_1C3.APS_1C3 --> DPLL_APS_1C3	DPLL_10953, DPLL_1547
2	DPLL_APS_1C3_EXT.APS_1C3 --> DPLL_APS_1C3	DPLL_10975, DPLL_11240, DPLL_1503, DPLL_1504, DPLL_1506, DPLL_1516, DPLL_1521, DPLL_1534, DPLL_1549, DPLL_1563, DPLL_5920, DPLL_6543, DPLL_6908, DPLL_7033, DPLL_7197, DPLL_7199, DPLL_9268
3	DPLL_APS_1C3_EXT.APS_1C3 --> DPLL_APS_1C3.APS_1C3	DPLL_5983, DPLL_7068

		4 | DPLL_APS_EXT.APS --> DPLL_APS_APS | DPLL_6311, DPLL_6908, DPLL_6916, DPLL_6942, DPLL_6948, DPLL_7033, DPLL_7199, DPLL_9268, DPLL_1500, DPLL_1502, DPLL_1505, DPLL_1506, DPLL_1547, DPLL_1548| | 5 | DPLL_APS_EXT.APS_1C2 --> DPLL_APS.APS_1C2 | DPLL_7063, DPLL_7064, DPLL_7068, DPLL_7069 | | 6 | DPLL_APS_EXT.APS_1C2 --> DPLL_APS_1C2 | DPLL_11160, DPLL_1503, DPLL_1505, DPLL_1506, DPLL_1517, DPLL_1547, DPLL_1548, DPLL_6908, DPLL_6942, DPLL_6948, DPLL_7033, DPLL_7111, DPLL_7198, DPLL_7199, DPLL_9268 | | 7 | DPLL_APS_SYNC_EXT.APS_1C2_EXT --> DPLL_APS_SYNC.APS_1C2_EXT | DPLL_5983 | | 8 | DPLL_APS_SYNC_EXT.APS_1C2_EXT --> DPLL_APS_SYNC_APS_1C2_EXT | DPLL_1503 | | 9 | DPLL_APS_SYNC_EXT.APS_1C2_OLD --> DPLL_APS_SYNC_APS_1C2_OLD | DPLL_1503 | | 10 | DPLL_APS_SYNC_EXT.APS_1C2_STATUS --> DPLL_APS_SYNC.APS_1C2_STATUS | DPLL_5983 | | 11 | DPLL_APS_SYNC_EXT.APS_1C2_STATUS --> DPLL_APS_SYNC_APS_1C2_STATUS | DPLL_1503 | | 12 | DPLL_CTRL_0.SNU --> DPLL_CTRL_EXT.SNU | DPLL_10067, DPLL_10081, DPLL_10096, DPLL_9865, DPLL_9866, DPLL_9972 | | 13 | DPLL_CTRL_0.SNU --> DPLL_SNU | DPLL_10975, DPLL_11115, DPLL_11127, DPLL_1404, DPLL_1413, DPLL_1478, DPLL_1502, DPLL_1503, DPLL_17484, DPLL_51842, DPLL_51843, DPLL_5740, DPLL_7189, DPLL_732 | | 14 | DPLL_CTRL_1.SYN_NS --> DPLL_CTRL_EXT.SYN_NS | DPLL_10067, DPLL_10096, DPLL_9937, DPLL_9972 | | 15 | DPLL_CTRL_1.SYN_NS --> DPLL_SYN_NS | DPLL_10975, DPLL_11115, DPLL_11127, DPLL_1502, DPLL_1503, DPLL_51842, DPLL_51843, DPLL_6980 | | 16 | DPLL_CTRL_EXT.SNU --> DPLL_SNU | DPLL_729 | | 17 | DPLL_CTRL_EXT.SYN_NS --> DPLL_SYN_NS | DPLL_1506, DPLL_1551, DPLL_5931, DPLL_5932, DPLL_6978, DPLL_7101 | | 18 | DPLL_CTRL_EXT.SYN_NS --> DPLL_CTRL_1.SYN_NS | DPLL_7065 | | 19 | DPLL_NUSC.NUSE --> DPLL_NUSC_NUSE | DPLL_11118, DPLL_11127, DPLL_11130, DPLL_1404, DPLL_1405, DPLL_1406, DPLL_1413, DPLL_1415, DPLL_1416, DPLL_51842, DPLL_51843, DPLL_6526, DPLL_6527, DPLL_6920, DPLL_6928, DPLL_6942, DPLL_6948, DPLL_9194, DPLL_9195 | | 20 | DPLL_NUSC.SYN_S --> DPLL_NUSC_SYN_S | DPLL_1478, DPLL_9466, DPLL_6908, DPLL_17660, DPLL_1465 | | 21 | DPLL_NUSC.VSN --> DPLL_NUSC_VSN | DPLL_11130, DPLL_1404, DPLL_1405, DPLL_1413, DPLL_1415, DPLL_51842, DPLL_51843, DPLL_6526, DPLL_6527, DPLL_6920, DPLL_6928, DPLL_6942, DPLL_6948, DPLL_9194, DPLL_9195 | | 22 | DPLL_NUSC.WSYN --> DPLL_NUSC_EXT1.WSYN | DPLL_9850 | | 23 | DPLL_NUSC_EXT1.SYN_S --> DPLL_NUSC_SYN_S | DPLL_10953, DPLL_11023, DPLL_11201, DPLL_11224, DPLL_11240, DPLL_1516, DPLL_1521, DPLL_1534, DPLL_1539, DPLL_1549, DPLL_1552, DPLL_5918, DPLL_5931, DPLL_5932, DPLL_6190, DPLL_6298, DPLL_6908, DPLL_7212, DPLL_8398, DPLL_9268, DPLL_9455, DPLL_7210 | | 24 | DPLL_NUSC_EXT1.SYN_S_OLD --> DPLL_NUSC.SYN_S_OLD | DPLL_5983, DPLL_7064 |	

Errata-ID	Errata	refer to
	| 25 | DPLL_NUSC_EXT1.SYN_S_OLD --> DPLL_NUSC_SYN_S_OLD | DPLL_10953, DPLL_11023, DPLL_11156, DPLL_11160, DPLL_11240, DPLL_1359, DPLL_1516, DPLL_1517, DPLL_1521, DPLL_1534, DPLL_1549, DPLL_6908, DPLL_6976, DPLL_6977, DPLL_9268, DPLL_7111 | | 26 | DPLL_NUSC_EXT2.FSS --> DPLL_NUSC_FSS | DPLL_11032, DPLL_11033, DPLL_11034, DPLL_11068, DPLL_11069, DPLL_11070 | | 27 | DPLL_NUSC_EXT2.NUSE -> DPLL_NUSC.NUSE | DPLL_7064, DPLL_7065 | | 28 | DPLL_NUSC_EXT2.NUSE --> DPLL_NUSC_NUSE | DPLL_10134, DPLL_10975, DPLL_11034, DPLL_11070, DPLL_11115, DPLL_1384, DPLL_1463, DPLL_1500, DPLL_1508, DPLL_1547, DPLL_1562, DPLL_1563, DPLL_7033, DPLL_7206 | | 29 | DPLL_NUSC_EXT2.VSN --> DPLL_NUSC.VSN | DPLL_7048 | | 30 | DPLL_NUSC_EXT2.VSN --> DPLL_NUSC_VSN | DPLL_11115, DPLL_11127, DPLL_7206 | 3. Fix the figure in DPLL_9425: 1. DPLL_APS_EXT.APS --> DPLL_APS_APS 2. DPLL_APS_EXT.APS_1C2 --> DPLL_APS_1C2 3. DPLL_APS_1C3_EXT.APS_1C3 --> DPLL_APS_1C3 Workaround : Not applicable.	

GTM-IP-519	Title : SPEC-(A)TOM: Misleading description of Continuous Counting Up Mode Scope : ATOM, TOM Severity : Low Classification : Non-critical Effects : Textual description can be erroneously interpreted as the configuration of (A)TOM[i]_CH[x]_CM0.CM0=(A)TOM[i]_CH[x]_CM1.CM1 is suitable to generate 100% duty cycle for the current PWM period. This is because the potential value change to SL will happen as soon as (A)TOM[i]_CH[x]_CN0.CN0 reaches the value of (A)TOM[i]_CH[x]_CM0.CM0 while (A)TOM[i]_CH[x]_CM1.CM1 is equal to (A)TOM[i]_CH[x]_CM0.CM0. Description : In the third list item of the paragraph, where some statements are given for Continuous Counting Up Mode with RST_CCU0=1 (GTM 4.1.0 spec.: TOM_4277; ATOM_2780), the following statement for the case (A)TOM[i]_CH[x]_CM0.CM0=(A)TOM[i]_CH[x]_CM1.CM1 is given: "- if (A)TOM[i]_CH[x]_CM0.CM0=(A)TOM[i]_CH[x]_CM1.CM1, the output switches to (A)TOM[i]_CH[x]_CTRL_SOMP.SL if (A)TOM[i]_CH[x]_CN0.CN0=(A)TOM[i]_CH[x]_CM0.CM0=(A)TOM[i]_CH[x]_CM1.CM1 ((A)TOM[i]_CH[x]_CM0.CM0 has higher priority)" or in the older specification versions (before GTM3 generations): "if (A)TOM[i]_CH[x]_CM0.CM0=(A)TOM[i]_CH[x]_CM1.CM1, the output is 100% (A)TOM[i]_CH[x]_CTRL.SL ((A)TOM[i]_CH[x]_CM0.CM0 has higher priority) " Both statements are misleading and have to be replaced by the following statement: "- as soon as (A)TOM[i]_CH[x]_CN0.CN0 reaches the value of (A)TOM[i]_CH[x]_CM0.CM0 while (A)TOM[i]_CH[x]_CM1.CM1 is equal to (A)TOM[i]_CH[x]_CM0.CM0, an edge to (A)TOM[i]_CH[x]_CTRL.SL is generated at the output or the output remains at (A)TOM[i]_CH[x]_CTRL.SL level, depending on the former level of the output ((A)TOM[i]_CH[x]_CM0.CM0 has higher priority). Please note that this configuration is not suitable for generating 100% duty cycle." Workaround : Hint: For a setup of 100% duty cycle for Continuous Counting Up Mode with RST_CCU0=1 the following setting has to be used: ATOM[i]_CH[x]_CM0.CM0 = 0 and ATOM[i]_CH[x]_CM1.CM1 > MAX.	v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120

Errata-ID	Errata	refer to
		v4.1.0-130 @Specification v4.1.0-V1.10 v4.1.0-V1.20

Errata-ID	Errata	refer to
GTM-IP-520	Title : SPEC-(A)TOM: Description for 100% duty cycle incorrect Scope : TOM, ATOM Severity : Low Classification : Non-critical Effects : Output behaviour for 100% duty cycle is not correct. Description : In the list of characteristics for Continuous Counting Up Mode with (A)TOM[i]_CH[x]_CTRL.RST_CCU0=0b1 (GTM 4.1.0 spec.: TOM_4277; ATOM_2780), it is stated that for 100% duty cycle (A)TOM[i]_CH[x]_CM1.CM1 has to be set to MAX value. This is incorrect. Instead, (A)TOM[i]_CH[x]_CM1.CM1 has to be set to a value greater than MAX. Therefore the statement has to be corrected as follows: "If ATOM[i]_CH[x]_CM0.CM0 = 0 and ATOM[i]_CH[x]_CM1.CM1 > MAX, the output is a pulse of ATOM[i]_CH[x]_CTRL_SOMP.SL for the period MAX (i.e. 100% duty cycle PWM signal)." Workaround : Not applicable.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10 v4.1.0-V1.20

GTM-IP-521	Title : SPEC-ATOM: Missing information for SOMB mode Scope : ATOM Severity : Low Classification : Non-critical Effects : In case only one of the bit fields (ATOM[i]_CH[x]_SR0.SR0 and ATOM[i]_CH[x]_SR1.SR1) is written, the behavior of the operation register bit fields ATOM[i]_CH[x]_CM0.CM0, ATOM[i]_CH[x]_CM1.CM1 and ATOM[i]_CH[x]_STAT.ACBI will be unexpected. Description : If the channel is configured in SOMB mode and controlled over configuration interface, it is mandatory to always write both bit fields ATOM[i]_CH[x]_SR0.SR0 and ATOM[i]_CH[x]_SR1.SR1 regardless of the compare strategy. Therefore the following note has to be added inside the chapter "SOMB controlled over configuration interface" (GTM 4.1.0 spec.: after ATOM_1879): "Note: It is mandatory to always write both bit fields ATOM[i]_CH[x]_SR0.SR0 and ATOM[i]_CH[x]_SR1.SR1 regardless of the compare strategy." Workaround : Not applicable.	v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

Errata-ID	Errata	refer to
		@Specification v4.1.0-V1.10 v4.1.0-V1.20

GTM-IP-522	Title : (A)TOM: Edge at output signal (A)TOM_OUT does not occur Scope : TOM, ATOM Severity : Medium Classification : Non-critical Effects : Output signal (A)TOM_OUT remains at (A)TOM[i]_CH[x]_CTRL.SL value. Description : If the channel is configured to be triggered by a preceding channel with (A)TOM[i]_CH[x]_CTRL.RST_CCU0=0b1 (SOMP mode for ATOM) and the duty cycle synchronously switches from 100% duty cycle with (A)TOM[i]_CH[x]_CM0.CM0=0x0 and (A)TOM[i]_CH[x]_CM1.CM1>MAX to 0% duty cycle with (A)TOM[i]_CH[x]_CM0.CM0>MAX for 0% duty cycle, the expected edge on the output signal (A)TOM_OUT to the inverted (A)TOM[i]_CH[x]_CTRL.SL value does not occur. If this switch is performed by setting the corresponding registers asynchronously, the edge on the output signal (A)TOM_OUT to the inverted (A)TOM[i]_CH[x]_CTRL.SL value does occur as expected. Hint: If the setting after synchronously switching to 0% duty cycle is not changed, the edge appears at the beginning of the next period. Workaround : Workaround 1: In the period before the synchronous change to 0% duty cycle, set the value of (A)TOM[i]_CH[x]_CM1.CM1 to MAX instead of greater than MAX. This can be done asynchronously by writing the bit field (A)TOM[i]_CH[x]_CM1.CM1 within the period. Alternatively it can be done via the synchronous update mechanism by writing the bit field (A)TOM[i]_CH[x]_SR1.SR1 two periods before switching to 0% duty cycle. Workaround 2: For the GTM Gen 4.1 releases, the following workaround can be used for 0% duty cycle: For 0% duty cycle on the output signal use the setting for 100% duty cycle with (A)TOM[i]_CH[x]_CM0.CM0 = 0 and (A)TOM[i]_CH[x]_CM1.CM1 > MAX and toggle (A)TOM[i]_CH[x]_CTRL.SL value synchronously by writing to (A)TOM[i]_CH[x]_CTRL_SR.SL_SR.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
		v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1

GTM-IP-523	Title : SPEC-(A)TOM: Missing priority information for register update Scope : TOM, ATOM Severity : Low Classification : Non-critical Effects : In (A)TOM the bus write access to the "OUTEN_STAT" and "ENDIS_STAT" registers is overridden by a trigger update and the desired values not written into the register. Description : The following information is missing in the specification and has to be placed inside the TGC Sub-unit/AGC Sub-unit chapter (GTM 4.1.0 spec.: after ATOM_2038/TOM_541): Inside ATOM chapter: The trigger condition has always priority over the bus write access to the ATOM[i]_AGC_OUTEN_STAT and ATOM[i]_AGC_ENDIS_STAT registers, even if ATOM[i]_AGC_OUTEN_CTRL.OUTEN_CTRL[k] / ATOM[i]_AGC_ENDIS_CTRL.ENDIS_CTRL[k] is set to 0b00. This means that the bus write access to ATOM[i]_AGC_OUTEN_STAT and ATOM[i]_AGC_ENDIS_STAT register is ignored in the clock cycle when the trigger condition is active. Inside TOM chapter: The trigger condition has always priority over the bus write access to the TOM[i]_TGC[g]_OUTEN_STAT and TOM[i]_TGC[g]_ENDIS_STAT registers, even if TOM[i]_TGC[g]_OUTEN_CTRL.OUTEN_CTRL[k] / TOM[i]_TGC[g]_ENDIS_CTRL.ENDIS_CTRL[k] is set to 0b00. This means that the bus write access to TOM[i]_TGC[g]_OUTEN_STAT and TOM[i]_TGC[g]_ENDIS_STAT register is ignored in the clock cycle when the trigger condition is active. Hint: The trigger override does not happen if the trigger is a HOST_TRIG, as this is initiated by a bus write itself and cannot happen at the same time as another bus write to the register. Workaround : To nevertheless ensure that the desired value is actually stored in the target register consider one of the following hints: Hint 1: Firstly, write the channel k within "ENDIS_CTRL" ("OUTEN_CTRL") and write the desired channel k in "ENDIS_STAT" ("OUTEN_STAT") afterwards. For the first write accesses to "ENDIS_CTRL" ("OUTEN_CTRL") it has to be ensured that all unused channels within "ENDIS_CTRL" ("OUTEN_CTRL") are set to "0b11". This way either the asynchronous write or the synchronous write becomes effective.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
	Hint 2: Read back the value of the "OUTEN_STAT" and "ENDIS_STAT" register to ensure the written value is actually present in the register.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10 v4.1.0-V1.20

Errata-ID	Errata	refer to
GTM-IP-524	Title : Unexpected AEI status on write access to GTM_RST Scope : GTM-ARCH Severity : Low Classification : Non-critical Effects : Unexpected AEI status value 0b10 although the write to the register and the reset were executed. Description : When the clock for cluster 0 is turned off by setting GTM_CLS_CLK_CFG.CLS[0]_CLK_DIV=0b00 and the write protection is turned off by GTM_CTRL.RF_PROT=0b0, a write of value 1 to the bit field GTM_RST.RST will execute the reset as expected, but AEI_STATUS is set to 0b10 (instead of 0b00) erroneously. Workaround : Before writing GTM_RST.RST = 1 enable cluster 0 by writing 0b01 to GTM_CLS_CLK_CFG.CLS[0]_CLK_DIV.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

Errata-ID	Errata	refer to
GTM-IP-525	Title : SPEC-(A)TOM: Description for 0% duty cycle incorrect Scope : TOM, ATOM Severity : Low Classification : Non-critical Effects : The configuration of a value for (A)TOM[i]_CH[x]_CM1.CM1 not equal to 0 does not lead to 0% duty cycle on the output signal. Description : In the list of characteristics for Continuous Counting Up Mode with (A)TOM[i]_CH[x]_CTRL.RST_CCU0=0b1, it is stated that configuration of 0% duty cycle is independent of (A)TOM[i]_CH[x]_CM1.CM1. This is incorrect and has to be modified. Instead, (A)TOM[i]_CH[x]_CM1.CM1 has to be set to 0. Therefore, the statement has to be corrected as follows: "if (A)TOM[i]_CH[x]_CM0.CM0 > MAX and (A)TOM[i]_CH[x]_CM1.CM1 =0, the output is !(A)TOM[i]_CH[x]_CTRL_SOMP.SL (i.e. 0% duty cycle PWM signal)." Workaround : Not applicable.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

GTM-IP-526	Title : SPEC-(A)TOM: Missing information for SOMP mode Scope : TOM, ATOM Severity : Low Classification : Non-critical Effects : The user may not be aware that the setting of (A)TOM[i]_CH[x]_CM0.CM0=MAX will definitely lead to a setting of the output to (A)TOM[i]_CH[x]_CTRL.SL at the very end of the period. Description : The following information about the priority between the CCU0 and CCU1 compare match (configured by (A)TOM[i]_CH[x]_CM0.CM0 and (A)TOM[i]_CH[x]_CM1.CM1) is missing in the specification and has to be added to the list of characteristics for Continuous Counting Up Mode with (A)TOM[i]_CH[x]_CTRL.RST_CCU0=0b1 (GTM 4.1.0 spec.: TOM_4277; ATOM_2780): For ATOM: "If ATOM[i]_CH[x]_CM0.CM0 is set to MAX, an edge to ATOM[i]_CH[x]_CTRL_SOMP.SL is generated at the output at the very end of the current period or the output remains at the ATOM[i]_CH[x]_CTRL_SOMP.SL level, depending on the previous level of the output. Be aware that this applies even if the value of ATOM[i]_CH[x]_CM1.CM1 is updated to 0 for the new period (ATOM[i]_CH[x]_CM0.CM0 has higher priority)." For TOM: "If TOM[i]_CH[x]_CM0.CM0 is set to MAX, an edge to TOM[i]_CH[x]_CTRL.SL is generated at the output at the very end of the current period or the output remains at the TOM[i]_CH[x]_CTRL. SL level, depending on the previous level of the output. Be aware that this applies even if the value of TOM[i]_CH[x]_CM1.CM1 is updated to 0 for the new period (TOM[i]_CH[x]_CM0.CM0 has higher priority)." Workaround : To reach a 0% duty cycle after a period where ATOM[i]_CH[x]_CM0.CM0 was set to MAX the following applies: Hint 1 (for Gen4.1): ATOM[i]_CH[x]_CTRL_SOMP.SL shall be switched in the cycle where the edge at the output happens because of the "CM0=MAX" settings. This can be realized by inverting the bit on ATOM[i]_CH[x]_CTRL_SR.SL_SR at the same time as the shadow registers ATOM[i]_CH[x]_SR0.SR0 and ATOM[i]_CH[x]_SR1.SR1 are updated. Additionally, ATOM[i]_CH[x]_CTRL_SR.SL_SR has to be switched back to the original	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10 v4.1.0-V1.20 v4.1.0-V1.30

Errata-ID	Errata	refer to
	value before the next update of the registers ATOM[i]_CH[x]_CM0.CM0 and ATOM[i]_CH[x]_CM1.CM1. Hint 2 (for Gen3 and following): At the same time as ATOM[i]_CH[x]_SR0.SR0 and ATOM[i]_CH[x]_SR1.SR1 are updated before the unwanted output edge, ATOM[i]_CH[x]_CM0.CM0 must be set to the same value as ATOM[i]_CH[x]_SR0.SR0. This will prevent the priority decision.	

Errata-ID	Errata	refer to
GTM-IP-527	Title : GTM-ARCH: CPU bus access is not acknowledged Scope : GTM-ARCH Severity : Low Classification : Non-critical Effects : CPU bus accesses to switched off clusters are not terminated. Description : If a cluster is switched off by writing GTM_CLS_CLK_CFG.CLS[j]_CLK_DIV = 0b00 while the MCS inside this cluster is executing a bus access, further CPU bus accesses to the switched off cluster are not acknowledged with an AEI_READY signal and the corresponding AEI_STATUS = 0b10. Workaround : Disable the MCS bus access by writing MCS_AEM_DIS.DIS_CLS[j] = 0b10 before switching off the cluster with GTM_CLS_CLK_CFG.CLS[j]_CLK_DIV = 0b00. Enable the MCS bus access by writing MCS_AEM_DIS.DIS_CLS[j] = 0b01 after switching on the cluster again.	v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

GTM-IP-528	Title : Spec-(A)TOM: Missing priority information Scope : TOM, ATOM Severity : Low Classification : Non-critical Effects : Unclear behaviour. Description : There is a missing priority information in the figures "ATOM channel architecture" (ATOM) and " TOM Channel ... architecture" (TOM). For the output driving storing element "SOUR" in the mentioned figures, CCU0 has priority over CCU1. It is when TRIG_CCU0=1 this is dominant over TRIG_CCU1. Workaround : Not applicable	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
GTM-IP-529	Title : SPEC-TIM: Wrong bit fields referenced Scope : TIM Severity : Low Classification : Non-critical Effects : The user may read back values from the wrong bit fields and draw wrong conclusions accordingly. Description : 1. In TSSM mode with TIM[i]_CH[x]_CTRL.ISL=0 the following statement is written in the first item of the list (GTM 4.1.0 spec.: TIM_7230): "TIM[i]_CH[x]_CNTS.CNTS [22:22]=0: Shifted in data stored in TIM[i]_CH[x]_CNT.CNT can be captured on a capture event in TIM[i]_CH[x]_GPR0.GPR0, all other TIM[i]_CH[x]_CTRL.GPR0_SEL/TIM[i]_CH[x]_CTRL.EGPR0_SEL settings can be used too." This is wrong and "GPR0" has to be replaced by "GPR1": "TIM[i]_CH[x]_CNTS.CNTS [22:22]=0: Shifted in data stored in TIM[i]_CH[x]_CNT.CNT can be captured on a capture event in TIM[i]_CH[x]_GPR1.GPR1, all other TIM[i]_CH[x]_CTRL.GPR1_SEL/TIM[i]_CH[x]_CTRL.EGPR1_SEL settings can be used too." 2. In TSSM mode with TIM[i]_CH[x]_CTRL.ISL=1 the following statement is written in the fourth item of the list (GTM 4.1.0 spec.: TIM_7232): "TIM[i]_CH[x]_CNTS.CNTS [22:22]=0: On a capture event, values can be captured in TIM[i]_CH[x]_GPR0.GPR0 , all TIM[i]_CH[x]_CTRL. GPR0_SEL / TIM[i]_CH[x]_CTRL.EGPR0_SEL settings can be used." This is wrong and should be replaced similarly and with same wording: "TIM[i]_CH[x]_CNTS.CNTS [22:22]=0: Shifted in data stored in TIM[i]_CH[x]_CNT.CNT can be captured on a capture event in TIM[i]_CH[x]_GPR1.GPR1, all other TIM[i]_CH[x]_CTRL.GPR1_SEL/TIM[i]_CH[x]_CTRL.EGPR1_SEL settings can be used too." Workaround : Not applicable.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10 v4.1.0-V1.20 v4.1.0-V1.30

Errata-ID	Errata	refer to
GTM-IP-530	Title : GTM_AEI: AEI_READY erroneously set Scope : GTM_AEI Severity : Medium Classification : Non-critical Effects : 1. Relevant for the GTM Integrator: The length of combinatorial path might lead to a timing violation. 2. In this case the combinatorial setting of AEI_READY might lead to a violation of the AEI protocol. Description : Only applies to GTM devices with an AEI Slave Interface (integration dependent): There is a combinatorial path from the AEI_WDATA[16] input port to the AEI_READY output port. Therefore the AEI_READY could be set in the same clock cycle as AEI_SEL. This is forbidden in Standard and Pipelined AEI protocol (protocol is GTM integration dependent) This possibility only exists when the AEI_ADDR =x"40" (BRIDGE_MODE) and AEI_W1R0 = '1' are set; i.e. only when writing '1' to the BRIDGE_MODE.BRG_RST bitfield (requesting a Bridge Reset). Whether the errata applies depends on the integration of the GTM-IP; this information can be obtained from the semiconductor vendor. Workaround : Step 1. Relevant for the GTM Integrator: If there is a timing problem, mark the path from aei_wdata[16] to aei_ready as a false path. e.g. Design Compiler: "set_false_path -through gtm_core_i/gtm_aei_i/a2a_i/aei_wdata[16] -through gtm_core_i/gtm_aei_i/a2a_i/aei_ready_out" Step 2. Relevant for applications: Do not use AEI-Bridge Soft-Reset	v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

Errata-ID	Errata	refer to
GTM-IP-532	Title : MCS: No resume action after clearing hardware breakpoints Scope : MCS Severity : Low Classification : Non-critical Effects : MCS stays in halted state instead of resuming after hardware breakpoints. Description : If both hardware breakpoints are configured to potentially trigger at the same point in time (e.g. instruction breakpoint at the same address), and the selected scope is a system halt (MCS[i]_HBP[h]_CTRL.SCOPE=2 with h=0 and h=1), the MCS enters the halted state as expected if both breakpoints are hit. However, after a corresponding write access to both of the HBP status registers (MCS[i]_HBP[h]_STATUS with h=0 and h=1) the MCS erroneously doesn't resume its execution. Workaround : Avoid breakpoint configurations for both HBPs that will activate the system halt at the same point in time.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0

GTM-IP-533	Title : SPEC-(A)TOM: Missing update conditions in SOMP mode Scope : TOM, ATOM Severity : Low Classification : Non-critical Effects : The user may not be aware of all update conditions for the operation registers. Description : The following information is missing in the ATOM[i]_CH[x]_CTRL_SOMP.UDMODE/TOM[i]_CH[x]_CTRL.UDMODE Register Description (GTM 4.1.0 spec.: ATOM_4907/TOM_1437) of the specification and has to be appended to the first coding item ("0b00"): For ATOM: "ATOM[i]_CH[x]_CM0.CM0, ATOM[i]_CH[x]_CM1.CM1, ATOM[i]_CH[x]_CTRL_SOMP.SL and ATOM[i]_CH[x]_CTRL_SOMP.CLK_SRC are updated if ATOM[i]_CH[x]_CN0.CN0 reaches the value of ATOM[i]_CH[x]_CM0.CM0 -1." For TOM: "TOM[i]_CH[x].CM0.CM0, TOM[i]_CH[x]_CM1.CM1, TOM[i]_CH[x]_CTRL.SL and TOM[i]_CH[x]_CTRL.CLK_SRC are updated if TOM[i]_CH[x]_CN0.CN0 reaches the value of TOM[i]_CH[x]_CM0.CM0 -1." Also, this following information is missing in the "ATOM SOMP Pulse Width, Period, Signal Level and Clock Frequency Update Mechanisms"/"TOM Pulse Width, Period, Signal Level and Clock Frequency Update Mechanisms" chapter (GTM 4.1.0 spec.: ATOM_5498/TOM_1358) of the specification: For ATOM: The first update case has to be updated with: "- In case ATOM[i]_CH[x]_CTRL_SOMP.RST_CCU0 =0b0 when the specified ATOM[i]_CH[x]_CTRL_SOMP.UDMODE compare condition is fulfilled the update will be performed. Additional information is given in the bit field description of ATOM[i]_CH[x]_CTRL_SOMP.UDMODE. The update mechanism must be enabled by configuring ATOM[i]_AGC_GLB_CTRL.UPEN_CTRL[k] =0b10." The following two additional update cases have to be added: - "In SOMP mode, if ATOM[i]_CH[x]_CTRL_SOMP.RST_CCU0 =0b0, the operating register is continuously updated as long as ATOM[i]_CH[x]_CM0.CM0 =0x0. This update condition must be enabled by configuring ATOM[i]_AGC_GLB_CTRL.UPEN_CTRL[k] =0b10 regardless of the source for the shadow registers. The source can be the configuration interface or the ARU.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10 v4.1.0-V1.20 v4.1.0-V1.30

Errata-ID	Errata	refer to
	- When the stop condition of the clock is configured (ATOM[i]_CH[x]_CTRL_SOMP.CLK_SRC =0b1100), new data is received via the ARU interface, until the clock stop condition is released. This update case does not depend on the state of ATOM[i]_AGC_GLB_CTRL.UPEN_CTRL[k]." For TOM: The first and second update cases have to be updated with: "- In case TOM[i]_CH[x]_CTRL.RST_CCU0 =0b0 when the specified TOM[i]_CH[x]_CTRL.UDMODE compare condition is fulfilled, the update will be performed. Additional information is given in the bit field description of TOM[i]_CH[x]_CTRL.UDMODE. The update mechanism must be enabled by configuring TOM[i]_TGC[g]_GLB_CTRL.UPEN_CTRL[c] =0b10. - In case TOM[i]_CH[x]_CTRL.RST_CCU0 =0b1 when the channel [x] is triggered by the signal TOM_CH_TRIGIN[x:x] from another TOM channel or by the external trigger signal TOM_EXT_TRIGIN of the assigned TIM channel, after it is synchronized to the selected CCM[i]_FXCLK_RES of channel [x], the update will also be performed. The update mechanism must be enabled by configuring TOM[i]_TGC[g]_GLB_CTRL.UPEN_CTRL[c] =0b10." The fourth update case has to be added: "- If TOM[i]_CH[x]_CTRL.RST_CCU0 =0b0, the operating registers are continuously updated as long as TOM[i]_CH[x]_CM0.CM0 =0x0. This update condition must be enabled by configuring TOM[i]_TGC[g]_GLB_CTRL.UPEN_CTRL[c] =0b10." Workaround : Not applicable	

GTM-IP-535	Title : DPLL: DPLL_PSTC.PSTC / DPLL_PSSC.PSSC is incorrect in continuous mode Scope : DPLL Severity : High Classification : Non-critical Effects : Miscalculation of DPLL_PSTC.PSTC / DPLL_PSSC.PSSC in continuous mode (DPLL_CTRL_1.DMO = 1) ultimately leads to wrong PMT calculations. Description : In continuous mode (DPLL_CTRL_1.DMO = 1), the pulse generation has to be a function of DPLL_CNT_NUM_1.CNT_NUM_1 / DPLL_CNT_NUM_2.CNT_NUM_2 instead of DPLL_INC_CNT1.INC_CNT1 / DPLL_INC_CNT2.INC_CNT2. Neither the GTM IP design nor the specification are correct regarding this fact. The behavior when DPLL_CTRL_1.DMO = 1 is not stated in the specification and the design is behaving incorrect regarding the missing definition. The design deficiency leads to a wrong calculation of DPLL_NMB_T_TAR.NMB_T_TAR / DPLL_NMB_S_TAR.NMB_S_TAR and DPLL_PSTC.PSTC / DPLL_PSSC.PSSC. The aforementioned behavior is not specified in "State description of the State Machine Table" (GTM 4.1.0 spec.: DPLL_6908 (step 5, 25)), "Description for DPLL_PSTC.PSTC" (GTM 4.1.0 spec.: DPLL_9465), and "Description for DPLL_PSSC.PSSC" (GTM 4.1.0 spec.: DPLL_9466.) In order to fix the specifications (here GTM4.1 tags are mentioned): 1. DPLL_6908: 1.1. Append the following to the description of step 5: If DPLL_CTRL_1_SHADOW_TRIGGER.DMO = 1, DPLL_NMB_T_TAR.NMB_T_TAR = DPLL_NUTC.SYN_T * DPLL_CNT_NUM_1.CNT_NUM_1. 1.2. Add the following to the description of step 25 (right after "(for DPLL_CTRL_1.SMC=0)"): DPLL_NMB_S_TAR.NMB_S_TAR = DPLL_NUSC_SYN_S * DPLL_CNT_NUM_1.CNT_NUM_1 (for DPLL_CTRL_1_SHADOW_STATE.DMO = 1 and DPLL_CTRL_0_SHADOW_STATE.SMC = 0) 1.3. Add the following to the description of step 25 (right after "(for DPLL_CTRL_1.SMC=1)"): DPLL_NMB_S_TAR.NMB_S_TAR = DPLL_NUSC_SYN_S * DPLL_CNT_NUM_2.CNT_NUM_2 (for DPLL_CTRL_1_SHADOW_STATE.DMO = 1 and DPLL_CTRL_0_SHADOW_STATE.SMC = 1)	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0

Errata-ID	Errata	refer to
	2. DPLL_9465: Append the following: DPLL_CTRL_1_SHADOW_TRIGGER.DMO = 1: DPLL_NUTC.SYN_T * DPLL_CNT_NUM_1.CNT_NUM_1 3. DPLL_9466: 3.1. Add the following right after "DPLL_CTRL_1.SMC=0: add (DPLL_MLS1.MLS1 + PD_S_store)*(DPLL_NUSC_SYN_S);": add DPLL_NUSC_SYN_S * DPLL_CNT_NUM_1.CNT_NUM_1 instead if DPLL_CTRL_1_SHADOW_STATE.DMO = 1 3.2 Add the following right after "DPLL_CTRL_1.SMC=1: add (DPLL_MLS2.MLS2 + PD_S_store)*(DPLL_NUSC_SYN_S);": add DPLL_NUSC_SYN_S * DPLL_CNT_NUM_2.CNT_NUM_2 instead if DPLL_CTRL_1_SHADOW_STATE.DMO = 1 <u>Workaround :</u> When setting DPLL_CNT_NUM1.CNT_NUM1 / DPLL_CNT_NUM2.CNT_NUM2 for the following modes, ensure the setting as described: In normal mode: While the DPLL is operating in continuous mode make sure that DPLL_CTRL_0.MLT = DPLL_CNT_NUM1.CNT_NUM1 - 1. In emergency mode: While the DPLL is operating in continuous mode, make sure DPLL_MLS1.MLS1 = DPLL_CNT_NUM1.CNT_NUM1. For synchronous motor control applications (DPLL_CTRL_1.SMC = 1): While the DPLL is operating in continuous mode, make sure that DPLL_MLS1.MLS1 = DPLL_CNT_NUM_1.CNT_NUM1 and DPLL_MLS2.MLS2 = DPLL_CNT_NUM_2.CNT_NUM2.	v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10 v4.1.0-V1.20 v4.1.0-V1.30 v4.1.0-V1.40

Errata-ID	Errata	refer to
GTM-IP-536	Title : GTM_AEI: Aborting an access might cause the GTM to become inaccessible Scope : GTM_AEI Severity : High Classification : Non-critical Effects : GTM becomes inaccessible from the AEI slave interface Description : Only applies to GTM devices with an AEI Slave Interface using the AEI Standard Mode and having a setting for Buffer Depth of 4 or 8 (all of these are integration dependent): When BRIDGE_MODE[2:0] = "011" (i.e. Asynchronous mode with Write Buffer active) and consecutive accesses on the AEI slave interface are happening without Idle Cycles (AEI_SEL becoming 0) in between, if a transfer is aborted exactly one AEI clock cycle after its initiation, the next access can lead to the AEI-bridge becoming unrecoverably unresponsive if this happens while AEI_FREE_BUFFER_CNT = 0. Workaround : Hint: No workaround needed since aborting after a single clock cycle is not a realistic scenario	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

Errata-ID	Errata	refer to
GTM-IP-537	Title : SPEC-ARCH: Wrong implementation conditions for bit fields in GTM_(E)IRQ_EN Scope : ARCH Severity : Low Classification : Non-critical Effects : The bit fields behave different to what is expected in devices with NMCS = 0. Description : The specification states that the bit fields (AEIM_USP_ADDR_IRQ_EN, AEIM_IM_ADDR_IRQ_EN, AEIM_USP_BE_IRQ_EN) in register GTM_IRQ_EN, as well as the bit fields (AEIM_USP_ADDR_EIRQ_EN, AEIM_IM_ADDR_EIRQ_EN, AEIM_USP_BE_EIRQ_EN) in register GTM_EIRQ_EN are only implemented in devices with NMCS > 1. This is incorrect - the aforementioned bit fields are implemented unconditionally. In order to fix the specification, the condition for the aforementioned bit fields (affected tags: ARCH_1832, ARCH_1834, ARCH_1836, ARCH_1861, ARCH_1862, ARCH_1863) must be set to nil ("-"). Workaround : None.	@Specification v4.1.0-V1.40

GTM-IP-538	Title : RTL-TIM: Wrong functionality of the overflow bit TIM[i]_CH[x]_IRQ_NOTIFY.CNTOFL Scope : TIM Severity : Medium Classification : Non-critical Effects : The interrupt TIM_CNTOFL_IRQ[x:x] is raised too early and cannot be cleared until the register TIM[i]_CH[x]_CNT reaches the value 0x0. The TIM IRQ output behaves the same (constant level output) in every interrupt mode except the single-pulse mode, where still only one pulse will be generated. Description : The specification states that if the register TIM[i]_CH[x]_CNT produces an overflow (wrap around 0xFFFFFF to 0x0 due to increment) during the measurement, the bit TIM[i]_CH[x]_IRQ_NOTIFY.CNTOFL is to be set. The bit TIM[i]_CH[x]_IRQ_NOTIFY.CNTOFL is set erroneously one (cluster) clock cycle after the register TIM[i]_CH[x]_CNT reaches the value 0xFFFFFF. It cannot be cleared as long as the counter stays at 0xFFFFFF. Workaround : For applications where the counter counts unconditionally: Use no clock divider in the CMU so that the register TIM[i]_CH[x]_CNT continuously increments with each (cluster) clock cycle.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
		v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

GTM-IP-539	Title : RTL-TIM: Unexpected overflow bit TIM[i]_CH[x]_IRQ_NOTIFY.CNTOFL Scope : TIM Severity : Low Classification : Non-critical Effects : The overflow bit TIM[i]_CH[x]_IRQ_NOTIFY.CNTOFL can be set in the TIPM, TGPS and TSSM mode, resulting in the false raising of the interrupt TIM_CNTOFL_IRQ[x:x] if the corresponding interrupt enable condition is met. Description : The specification states that in the TIM modes TIPM (gtm1.0 onwards), TGPS (gtm1.5 onwards) and TSSM (gtm3.1 onwards) the register TIM[i]_CH[x]_CNT never produces an overflow and the bit TIM[i]_CH[x]_IRQ_NOTIFY.CNTOFL is never set. This mode dependency is not implemented and the overflow bit TIM[i]_CH[x]_IRQ_NOTIFY.CNTOFL may be activated in all TIM modes. Workaround : Disable the interrupt by setting TIM[i]_CH[x]_IRQ_EN.CNTOFL_IRQ_EN and TIM[i]_CH[x]_EIRQ_EN.CNTOFL_EIRQ_EN to the value of 0.	v1.3 v1.4.0 v1.4.2 v1.4.4-11 v1.5.0-A0 v1.5.0-A1 v1.5.1-A1 v1.5.2-A1 v1.5.2-A2 v1.5.3-A1 v1.5.3-A2 v1.5.4-A1 v1.5.4-A2 v1.5.4-A3 v1.5.5-A1 v2.0.2-A1 v2.1.1-A1 v2.1.2-A1 v2.1.2-A2 v3.0.2-A1 v3.0.3-A1 v3.0.3-A2 v3.0.4-A1 v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Errata-ID	Errata	refer to
		v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

Errata-ID	Errata	refer to
GTM-IP-540	Title : SPEC-TIM: Wrong update condition in TSSM mode Scope : TIM Severity : Low Classification : Non-critical Effects : The user assumes an incorrect update condition. Description : In TIM TSSM mode ("Signal Generation with TIM Serial Shift Mode"; GTM 4.1.0 spec.: TIM_3167) it is stated that the update of TIM[i]_CH[x]_CNT will only take place once on a trigger "...if the TIM[i]_CH[x]_GPR0 was written by the CPU.". But the update of TIM[i]_CH[x]_CNT doesn't depend on whether a value has been written by CPU. Therefore, this update condition has to be removed from specification. Workaround : Not applicable	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10 v4.1.0-V1.20 v4.1.0-V1.30 v4.1.0-V1.40

Errata-ID	Errata	refer to
GTM-IP-541	Title : GTM-ARCH: Bit field GTM_RST.BRIDGE_MODE_WRDIS not writable Scope : GTM-ARCH Severity : Medium Classification : Non-critical Effects : A write access to GTM_RST.BRIDGE_MODE_WRDIS will not update the bit field value and no error will be reported. Description : The bit field GTM_RST.BRIDGE_MODE_WRDIS cannot be reliably written via the configuration interface if the clock divider for cluster 0 is configured to 1 (GTM_CLS_CLK_CFG.CLS0_CLK_DIV = 0b1) or if cluster 0 clock is switched off (GTM_CLS_CLK_CFG.CLS0_CLK_DIV = 0b0). The reason is that the register GTM_RST runs always with a 2:1 clock and hence the write will be missed with a 50% probability. No error will be reported. Note: MCS bus write accesses to GTM_RST.BRIDGE_MODE_WRDIS are also affected if the clock divider for cluster 0 is configured to 1 (GTM_CLS_CLK_CFG.CLS0_CLK_DIV = 0b1). Note: This is only true for GTM devices with existing cluster clock dividers (CFG_CLOCK_RATE = 1). Workaround : Configure the clock divider for cluster 0 to a 2:1 clock ratio (GTM_CLS_CLK_CFG.CLS0_CLK_DIV = 0b10) before writing to GTM_RST.BRIDGE_MODE_WRDIS.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2 v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130

Errata-ID	Errata	refer to
GTM-IP-542	Title : SPEC-ALL: Incorrect volatility Scope : GTM-ARCH, GTM-TBU, GTM-DPLL Severity : Low Classification : Non-critical Effects : The bit fields (GTM_RST.BRIDGE_MODE_WRDIS, DPLL_IRQ_MODE.IRQ_MODE, TBU_CH3_CTRL.CH_MODE, TBU_CH2_CTRL.CH_MODE, TBU_CH1_CTRL.CH_MODE) behave different from what is specified. Description : The volatility - as defined in the GTM4.1 specification - for the bit fields GTM_RST.BRIDGE_MODE_WRDIS, DPLL_IRQ_MODE.IRQ_MODE, TBU_CH3_CTRL.CH_MODE, TBU_CH2_CTRL.CH_MODE, and TBU_CH1_CTRL.CH_MODE is incorrectly set to true. These bit fields are involatile. In order to fix the specification, the volatility attribute for the aforementioned bit fields (GTM4.1 spec.: ARCH_3868, DPLL_6888, TBU_838, TBU_864, TBU_853) shall be set to false. Workaround : Not applicable.	v4.1.0-0A0 v4.1.0-0A1 v4.1.0-0A2 v4.1.0-0B0 v4.1.0-0B1 v4.1.0-0C0 v4.1.0-0C1 v4.1.0-0D0 v4.1.0-0D1 v4.1.0-0E0 v4.1.0-0F0 v4.1.0-100 v4.1.0-110 v4.1.0-120 v4.1.0-130 @Specification v4.1.0-V1.10 v4.1.0-V1.20 v4.1.0-V1.30 v4.1.0-V1.40 v4.1.0-V1.50

Errata-ID	Errata	refer to
GTM-IP-543	Title : SPEC-TIM: Wrong clock name referenced Scope : TIM Severity : Low Classification : Non-critical Effects : Assumption of an incorrect clock for input synchronisation, and also a differing latency. Description : In the "Timer Input Module (TIM)" specification chapter it is stated that the incoming input signals are synchronized with the clock SYS_CLK, resulting in a delay of two SYS_CLK periods for the incoming signals. The reference to the clock signal SYS_CLK is wrong. Instead it has to reference the internal cluster clock cls_clk. Workaround : Not applicable.	v3.1.4-A0 v3.1.5-A0 v3.1.5-A1 v3.1.5-A2 v3.1.5-A3 v3.1.5-A4 v3.1.5-A5 v3.1.5-A6 v3.1.5-A7 v3.1.5-A8 v3.1.5-A9 v3.1.5-AA v3.1.5-AB v3.1.5-AC v3.1.5-AD v3.1.5-AE v3.1.5-AF v3.1.5-B0 v3.1.5-B1 v3.1.5-B2 v3.1.5-B3 v3.1.5-B4 v3.1.5-B5 v3.1.5-B6 v3.1.5-B7 v3.1.5-B8 v3.1.5-B9 v3.1.5-BA v3.1.5-BB v3.1.5-BD v3.5.0-A0 v3.5.0-A1 v3.5.0-A2

Robert Bosch GmbH
ME-IC/PRM-IP
Postfach 13 42
72703 Reutlingen
Germany