SLG46108-EV Errata Note

Abstract

This document contains the known errata for SLG46108-EV and the recommended workarounds.

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1. Information

Package(s)	1.0 mm x 1.2 mm x 0.55 mm, 0.4 mm pitch

2. Errata Summary

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3	FILTER Cell Does Not Filter Out Glitches
4	Input Glitch Pattern Combination into DLYs Fails to Trigger Auto Power On of 25 kHz or 2 MHz OSC
5	OSC Long Start-Up Time

3. Errata Details

3.1 Incorrect Counter Operation after the Reset

3.1.1. Effect

Counter

3.1.2. Conditions

Counter Reset is asserted at the same time as a rising clock edge

3.1.3. Technical Description

If the Counter Reset is asserted at the same time as a rising clock edge, it is possible that the Counter Data will be reset incorrectly and the counter output may appear faster than expected, it doesn't depend on the edge select option. This phenomenon appears more often as the clock frequency increases.

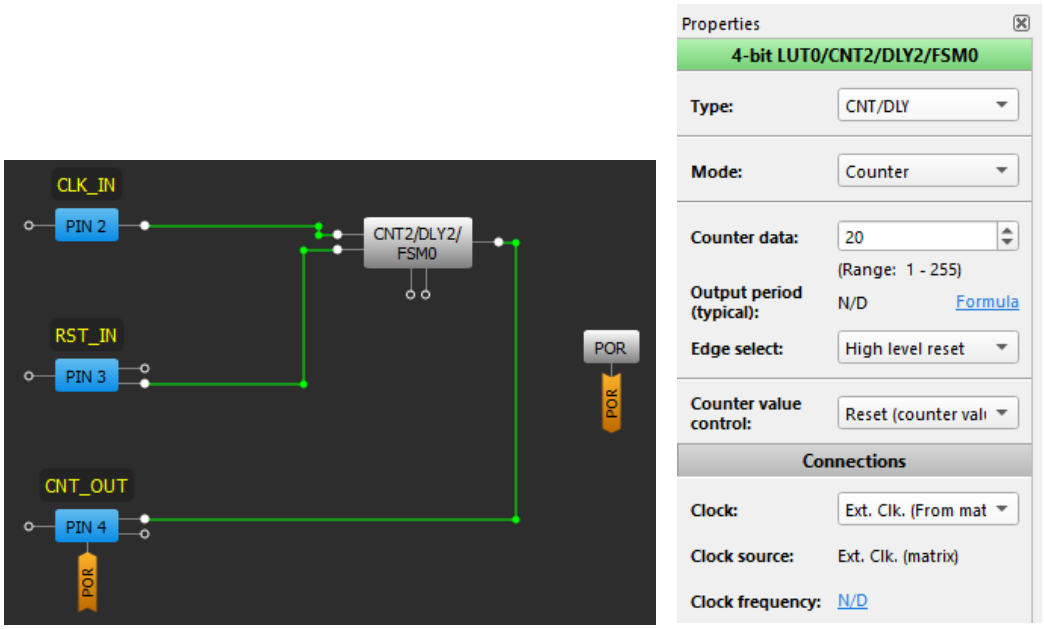

Figure 1. Testing Design and Settings

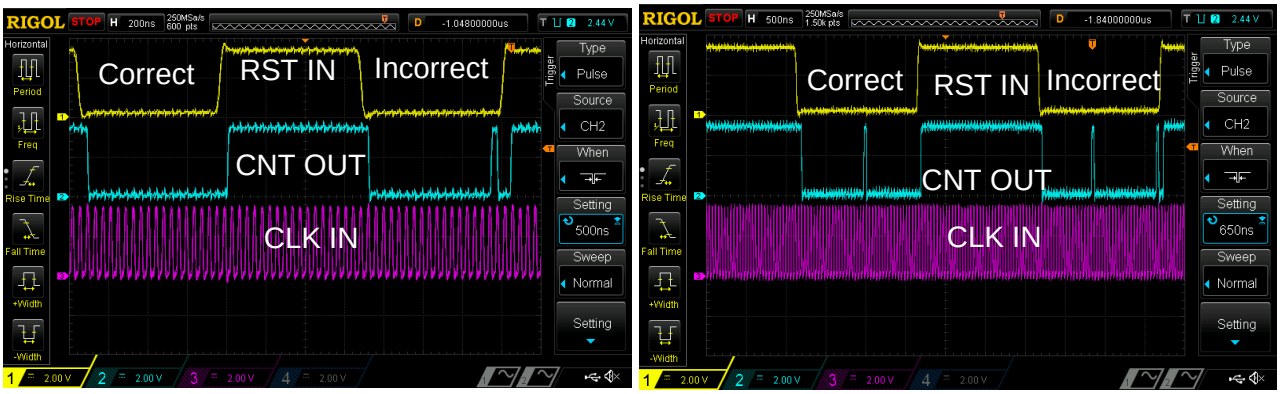

Figure 2. Testing Waveforms

3.1.4. Workaround

Synchronize the RESET input of the Counter with its CLK using 2 DFF cells as shown in Figure 3.

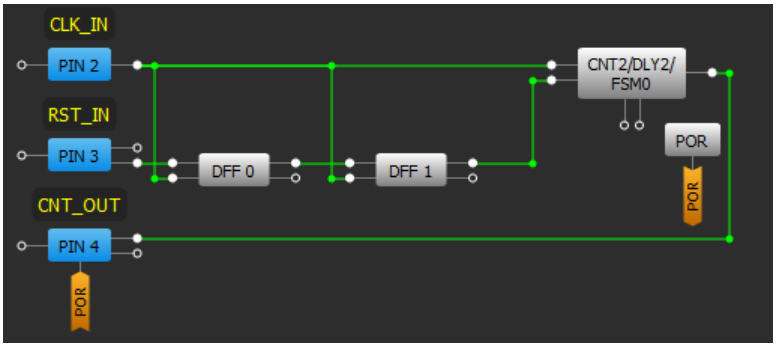

Figure 3. Improved Design

3.2 V_{DD} Noise Influences OSC Variation

3.2.1. Effect

OSC, Counter/Delay

3.2.2. Conditions

High-frequency noise at V_{DD}

3.2.3. Technical Description

While applying some high-frequency noise to the VDD, OSC inaccuracy may increase. The same behavior is also present in cases where high-frequency switches are outputted from the chip using the Push-Pull type driver. See, the test results in Table 1.

Table 1. Additional Frequency Shift by Different PINs

V_{DD} = 5 V Trim V_{DD} = 3.3 V	Push-Pull 1X	Push-Pull 2X	Push-Pull 1X	Push Pull 2X
OUT PIN #	f Shifted, %	f shifted, %	Average	Average
4	1.42 %	3.63 %	1.52 %	3.81 %
6	1.67 %	4.03 %		
7	1.62 %	3.98 %		
8	1.38 %	3.59 %		
4 … 8	6.73 %	11.98 %	--	--

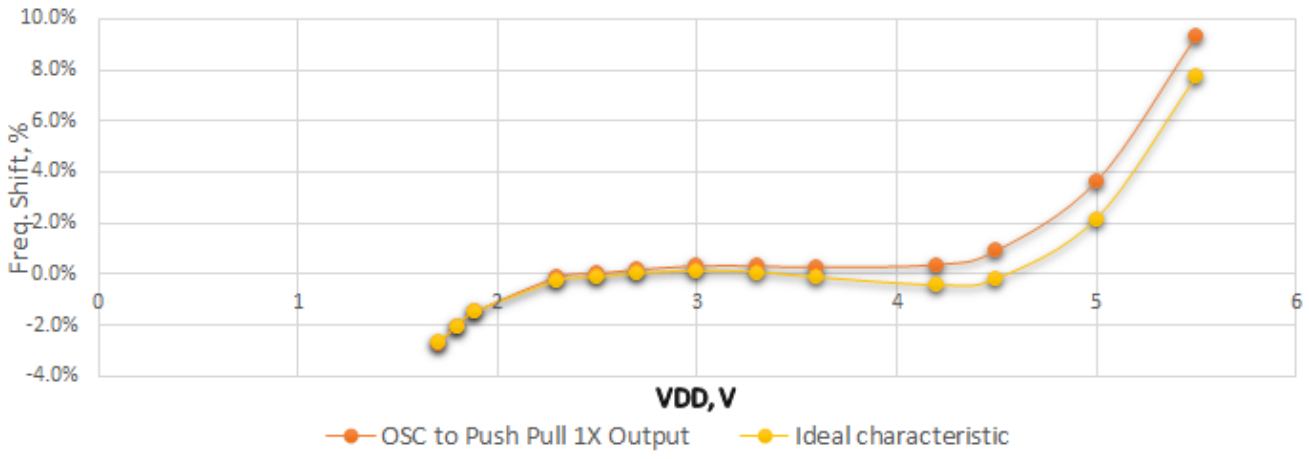

Figure 4. OSC Frequency vs. V_{DD}

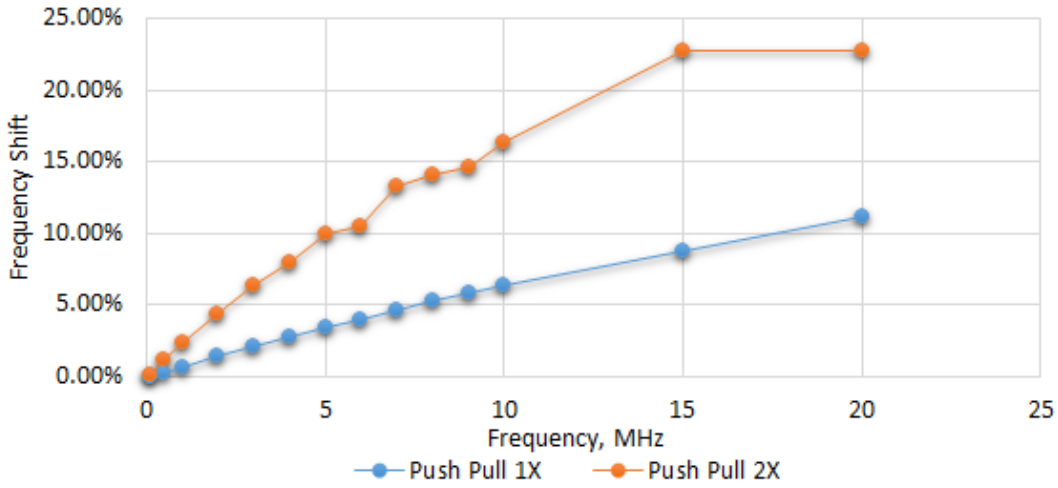

Figure 5. OSC Accuracy vs. Pass-Through Signal Frequency

3.2.4. Workaround

Currently, there are no viable workarounds for this issue.
However, the issue can be minimized by doing the following:

- Only use frequencies lower than 2 MHz when switching the output.
- Do not use parallel PIN connections to output high-speed switching signals.

3.3 FILTER Cell Does Not Filter Out Glitches

3.3.1. Effect

FILTER

3.3.2. Conditions

High-frequency clock

3.3.3. Technical Description

If high-frequency clock input comes in, the FILTER cell may not filter out it. There are several factors like input frequency, duty cycle, and LOW duration in such signal that may lead to its passing through the FILTER block.

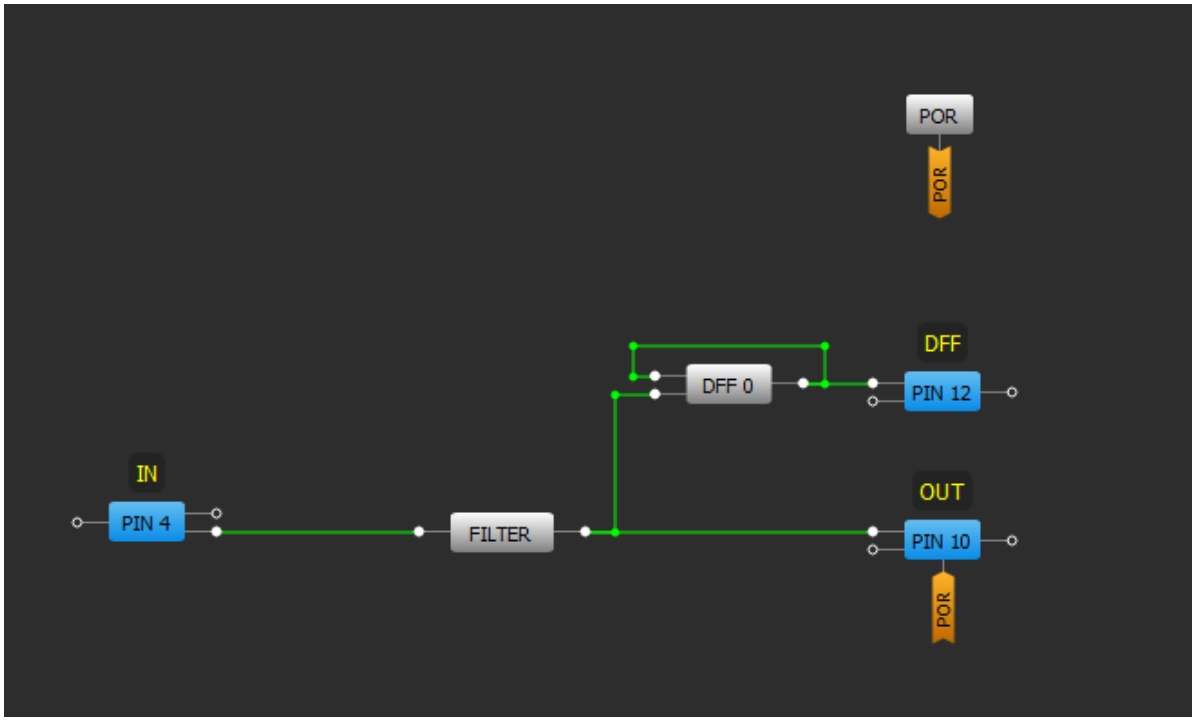

Figure 6. Testing Design

Channel 1 (yellow/top line) – PIN#4 (IN).

Channel 2 (light blue/2nd line) – PIN#10 (OUT).

Channel 3 (magenta /3rd line) – PIN#12 (DFF).

Figure 7. Output Waveforms at Period = 60 ns, Pulse Width = 10 ns, DC = 16.7 % (Correct Functionality)

Figure 8. Output Waveforms at Period = 60 ns, Pulse Width = 20 ns, DC = 33.3 % (Incorrect Functionality)

Figure 9. Output Waveforms at Period = 60 ns, Pulse Width = 30 ns, DC = 50 % (Incorrect Functionality)

Figure 10. Output Waveforms at Period = 60 ns, Pulse Width = 40 ns, DC = 66.67% (Correct Functionality)

3.3.4. Workaround

Currently, there is no workaround for this issue. Filter block is good at filtering short spontaneous glitches. It is intended to be used in a series connection before the delay cell to avoid its latching.

3.4 Input Glitch Pattern Combination into DLYs Fails to Trigger Auto Power On of 25 kHz or 2 MHz OSC

3.4.1. Effect

Specific combinations of DLY inputs can fail to trigger Auto Power On to enable 25 kHz or 2 MHz OSC. Other OSC generators (25 MHz) do not have an issue with the Auto Power On setting.

3.4.2. Conditions

Auto Power On can potentially fail to enable OSC when all the following conditions are present together:

1. 25 kHz or 2 MHz OSC is in Auto Power On mode.
2. DLYs are clocked by such OSC.
3. Input to one more such DLY have glitches < 200 ns.
4. OR of OSC trigger signals from all DLYs clocked by the same OSC together form a long+short glitch pattern with precise (ns) timings as shown in Figure 11. The trigger signal generation per DLY is detailed in the section Technical Description.
5. During the glitch period, no other DLY is active, meaning has already enabled OSC.

3.4.3. Technical Description

OSC generators have an Auto Power On mode which can be selected to automatically power on the OSC only when needed, such as when a DLY needs to count OSC cycles to time the delay output, thereby reducing quiescent power. Each individual DLY starts waiting in an inactive state, and when upon receiving an input edge (of polarity set by DLY configuration) then sets its individual trigger signal high. For example, in a rising-edge DLY, a rising edge input sets this trigger high. For a falling edge, the situation is inverted. In either case (or both edge DLY), the individual DLY trigger is reset if either an opposite edge is detected (therefore, canceling the

DLY function) or the DLY finishes timing its output upon reaching the desired count per its setting. Therefore, an input pulse shorter than the DLY time is filtered out. The global Auto Power On circuitry then takes the OR of all the individual DLY triggers and subsequently sends the master enable signal to activate the OSC.

For this chip, the Auto Power On circuitry of the 25 kHz/2 MHz generators contains a circuit errata, which can potentially fail to power on the OSC for a specific pattern and timing of the OR of all related DLY trigger signals. The pattern is shown in Figure 11 (boxed in red) and consists of a relatively longer pulse (~145 ns) followed by a shorter (~5 ns) glitch of opposite polarity.

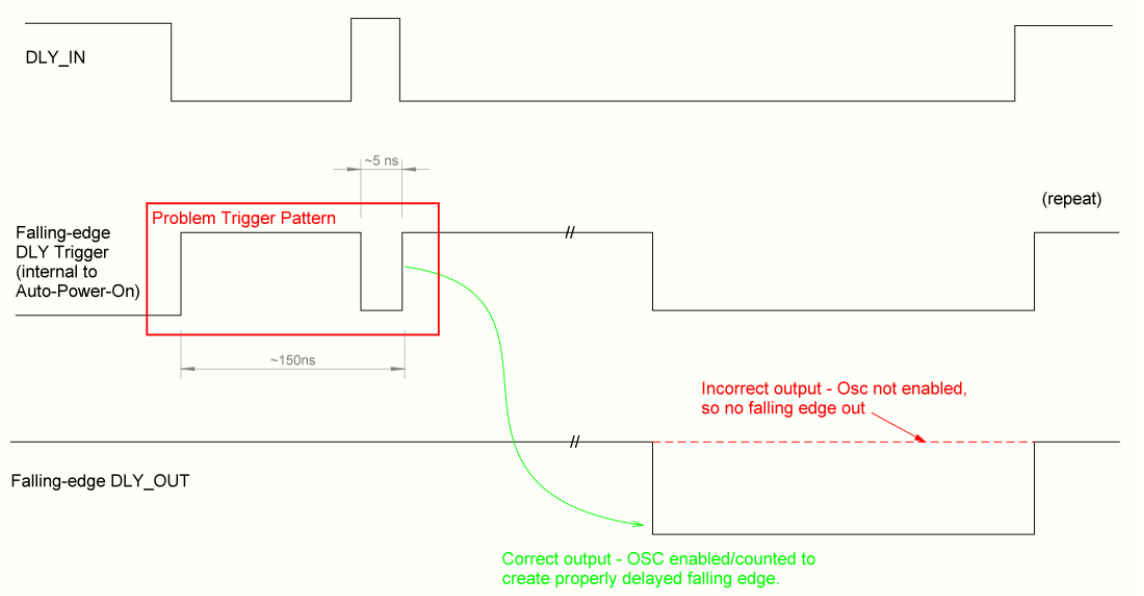

Figure 11. Problem Trigger Pattern

The error is difficult to capture as the timing must be exact within ns, and short (ns) pulses are difficult to generate glitches precise enough to induce the problem. GPIO naturally filters out ns pulses, so for purposes of errata capture, two simultaneous falling-edge DLY circuits (as shown in Figure 12) were used. By lining up two delays precisely at a particular timing relationship, we can use the internal Auto Power On (OR logic) to generate the glitch pattern necessary to cause the error.

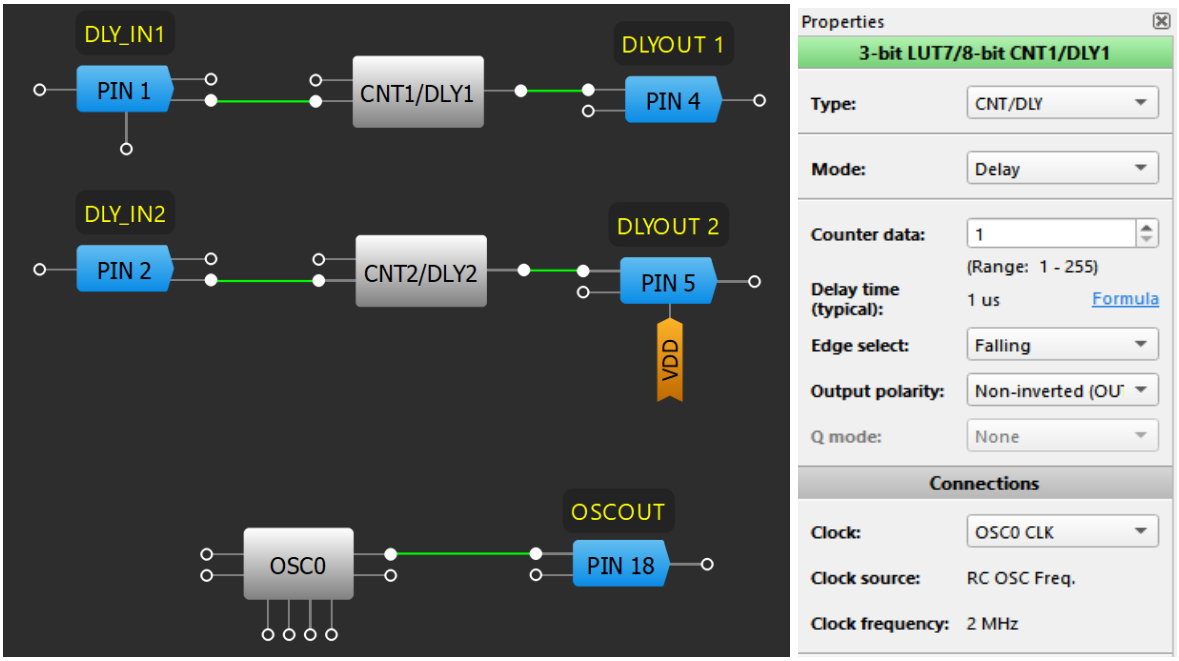

Figure 12. Test Circuit

Figure 13 shows a series of DLY output events are missing, where the OSC is correspondingly not triggering when it was supposed to. Figure 14 is a zoom-in of the boxed region from Figure 13. The total glitch/chatter time was measured in this case at 152 ns. By using the composite OR of the two delay channels, we can asynchronously strobe with tiny frequency variations, and so tune the timing to induce this errata. Note that the error is not persistent – the system is recovered when all DLYs are returned to inactive state, such as when input of falling edge DLY goes high, thus canceling delay, or after DLY out finishes.

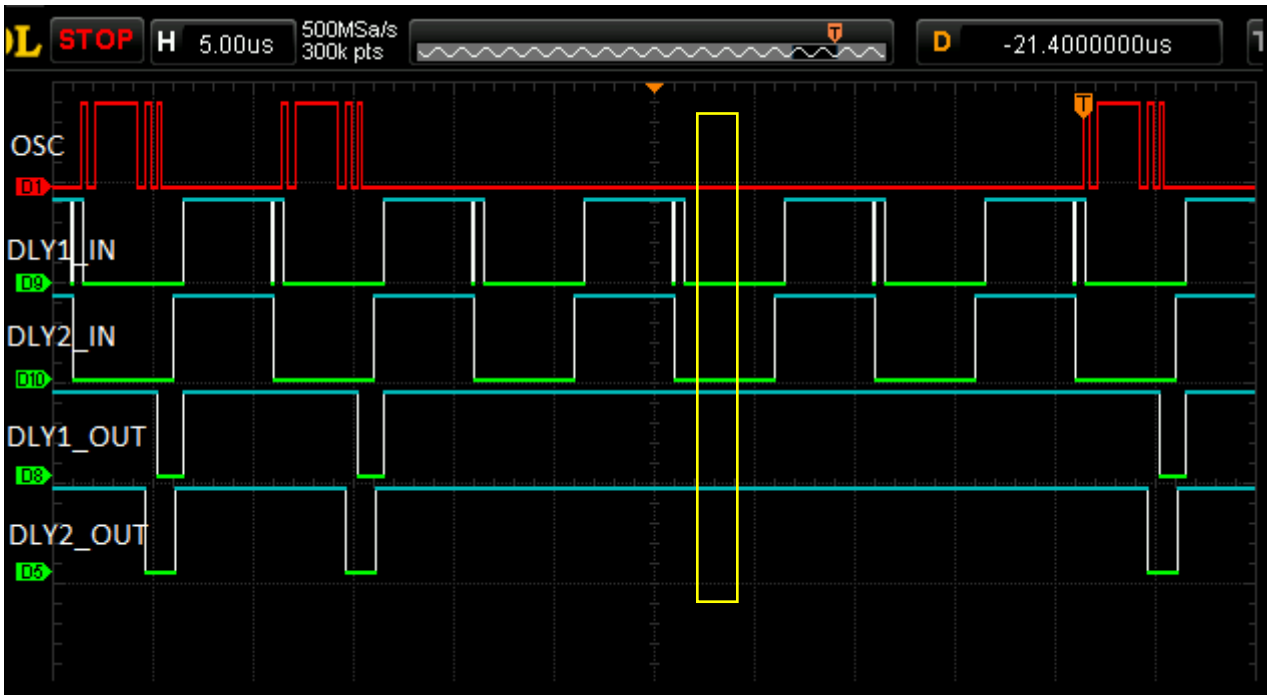

Figure 13. Errata Capture (Zoom Out)

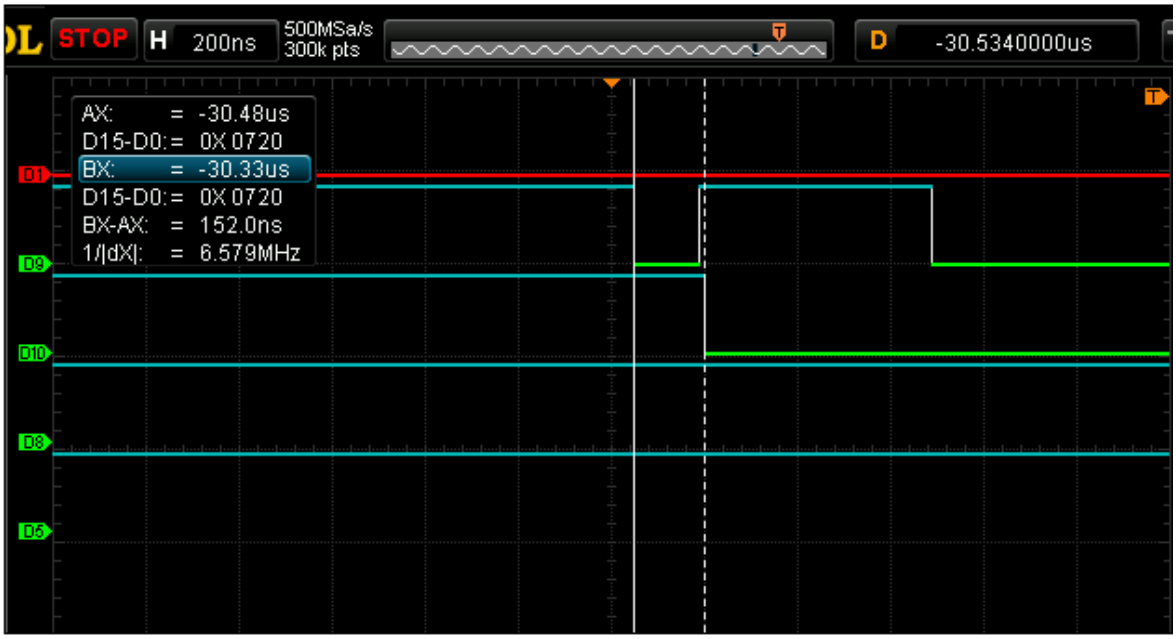

Figure 14. Errata Capture (Zoom In)

3.4.4. Workaround

Any one of the following prevents the issue:

- Use signal conditioning circuits to prevent glitches on DLY inputs < 200 ns. Examples:
  - ACMP with Hysteresis
  - External RC in front of Digital Input with Schmitt Trigger
  - Filter cell.
- Set OSC power mode to Force Power On mode instead of Auto Power On.
- Use a different oscillator, such as 25 MHz Ring OSC, which does not have Auto Power On issue.

3.5 OSC Long Start-Up Time

3.5.1. Effect

When a short pulse is applied to the PWR DOWN input, the oscillator exhibits a long start-up time.

3.5.2. Conditions

When a short pulse of less than ~40 ns is applied to the PWR DOWN input.

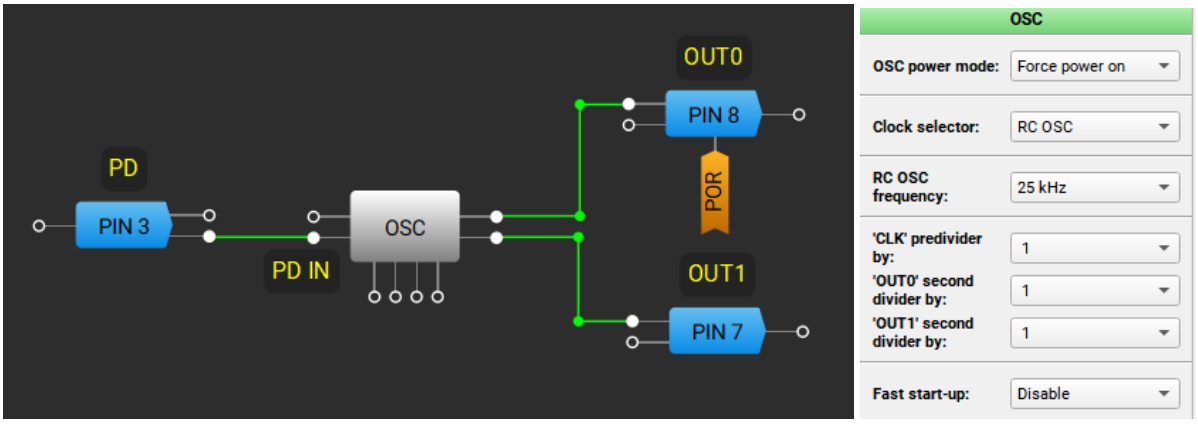

Figure 15. Test Design

3.5.3. Technical Description

If a pulse with a duration of less than ~40 ns is applied to the PWR DOWN input of the oscillator, the oscillator outputs remain stuck for milliseconds, as shown in Figure 16 and Figure 17. This issue is observed for both 25 kHz and 2 MHz oscillators.

Figure 16. 25 kHz OSC Long Start-Up

Figure 17. 2 MHz OSC Long Start-Up

3.5.4. Workaround

Change the Fast Start-up setting to "Enable" (see Figure 18) or avoid applying glitches to the PWR DOWN input of the oscillator.

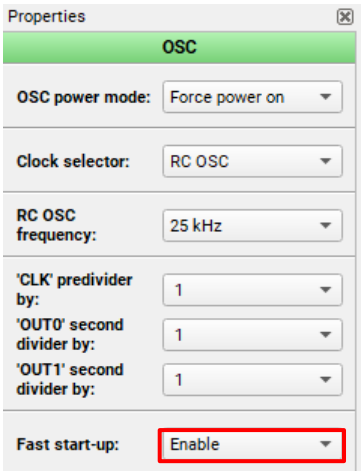

Figure 18. Enabling Fast Start-Up to Eliminate OSC Start-Up Delay

4. Revision History

Revision	Date	Description
1.01	Dec 19, 2024	Added issue #5
1.00	June 12, 2024	Initial release.