Supplemental Information

This Device Errata reflects revision 1.0 silicon and supplement information found in the documentation for this device.

Z step is revision 1.0. This is identified by material date code (top mark) of 0327 or later.

Document Revision History

April 9, 2007 : First version of the document.

Description and Workarounds

Item #1: FB Internal PLL Feedback Divider

Issue: Under certain process conditions FB in divide by four may be marginal which would cause excessive jitter.

Use of FB in divide by 4 configuration is not recommended for this device. The following configurations in Table 3, Clock Frequency Configuration, of the datasheet will not be supported:

Table 3. Clock Frequency Configuration

Name	FSEL0	FSEL1	FSEL2	FSEL3	f_{REF} range [MHz]	QAx		QBx		QFB	FB[1]
						Ratio	f_{QAX} [MHz]	Ratio	f_{QBX}[MHz]		
M2H	1	0	0	0	60–100	f_{REF} * 2	120–200	f_{REF} * 2	120–200	f_{REF}	4
M22H	1	0	0	1				f_{REF}	60–100		
M1H	1	1	1	0	60–100	f_{REF}	60–100.0	f_{REF}	60–100	f_{REF}	4
M12H	1	1	1	1				f_{REF} ÷ 2	30–50		

Workaround: If possible in application, use of FB in other configurations such as FB divide by 6, 8 or 16 is recommended to obtain desired frequency.

Fix: There are no plans to fix this device. Product ICS879893AYI is recommended as pin compatible replacement if FB divide by four configuration is required.