ZSSC4169D-14

Automotive Resistor Sensor Signal Conditioner with SENT Output

Description

The ZSSC4169D-14 is member of Renesas's family of CMOS integrated circuits for highly accurate amplification and sensor-specific correction of differential bridge sensor element signals. Featuring a maximum analog pre-amplification in the range of up to 200, the ZSSC4169D-14 is adjustable to nearly all resistive bridges.

Digital compensation of offset, gain, sensitivity, temperature drift, and nonlinearity is accomplished via a 16-bit RISC microcontroller. Calibration coefficients and configuration data are stored in the ZSSC4169D-14 nonvolatile memory (NVM), which is reliable in automotive applications.

The ZSSC4169D-14 supports using the internal PTAT or external diodes as temperature references.

Measured values are provided via a digital SENT interface. The SENT interface enables transmission of sensor data via its Fast Channel as well as transmission of supplementary data via its Serial Data Message (SDM) Channel (also referred to as the "slow" channel) using only one output pin. End-of-line calibration is also supported through this output pin via a One-Wire Interface (OWI). The ZSSC4169D-14 and the calibration equipment communicate digitally, so the noise sensitivity is greatly reduced. Digital calibration helps keep assembly cost low as no trimming by external devices or lasers is needed.

The ZSSC4169D-14 is optimized for automotive environments by overvoltage and reverse polarity protection circuitry, excellent electromagnetic compatibility, and multiple diagnostic features.

Typical Applications

- Fluid brake pressure sensing (PV)
- Hydraulic pressure sensing
  (e.g., steering systems with hydraulic steering support)
- Pneumatic pressure sensing
  (e.g., air brake systems; pneumatic shock absorbers)

Available Support

- Evaluation kit
- Application notes
- Calculation tools

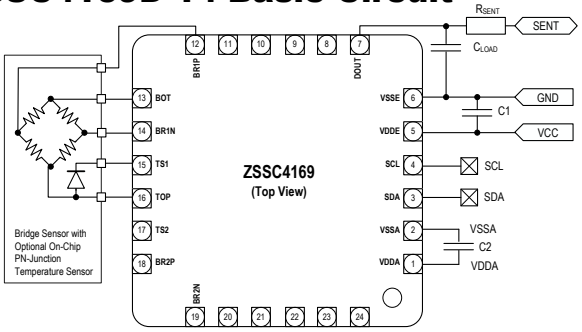
Features

- Differential bridge sensor input and on-chip or external temperature sensors, selectable for conditioning of the sensor input signal and/or temperature output
- Digital compensation for offset, gain, and higher order nonlinearity as well as temperature coefficients of measured bridge sensor input signal
- Operating temperature range: -40°C to 150°C
- Accuracy: ±0.5% FS at -40°C to 150°C
- NVM memory for configuration, calibration data, and configurable measurement and conditioning functionality
- SENT output compliant to SAE J2716 JAN2010 (SENT Rev. 3) and APR2016 (SENT Rev. 4) Specification
- Supports output of one or more sensor signals and product identification via a single SENT interface connection
- Configurable for nearly all resistive bridge sensors
- One-pass, end-of-line calibration algorithm minimizes production costs
- No external trimming or components required
- Qualified according to AEC-Q100 Grade 0
- Support up to ASIL-C safety applications

Physical Characteristics

- Supply voltage: 4.75V to 5.25V
- Over-voltage and reverse polarity protection up to ±18V
- Bridge sensor input span: 1 to 800 mV/V
- Bridge sensor signal ADC resolution: 14 bit
- Output resolution: 12-bit via SENT interface
- Package: 24-QFN (4 × 4 mm; wettable flanks);
  16-TSSOP (4.4 × 5mm, exposed pad)

ZSSC4169D-14 Basic Circuit



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1. Pin Assignments

The ZSSC4169D-14 is available in 24-QFN (4mm × 4mm; wettable flanks) and in 16-TSSOP RoHS-conformant packages (4.4mm × 5.0mm according to JEDEC MO-153 with exposed pad). Both allow 2 years of shelf life relative to the package date code (see section 15).

Note: The backside of both the 24-QFN and the 16-TSSOP packages (exposed pad; see section 14 regarding actual dimensions) are electrically connected to VSSA.

Recommendation: Solder the QFN exposed pad to the PCB, even if electrically redundant, to ensure adequate thermal performance and to reduce mechanical stress and solder joint failure risk.

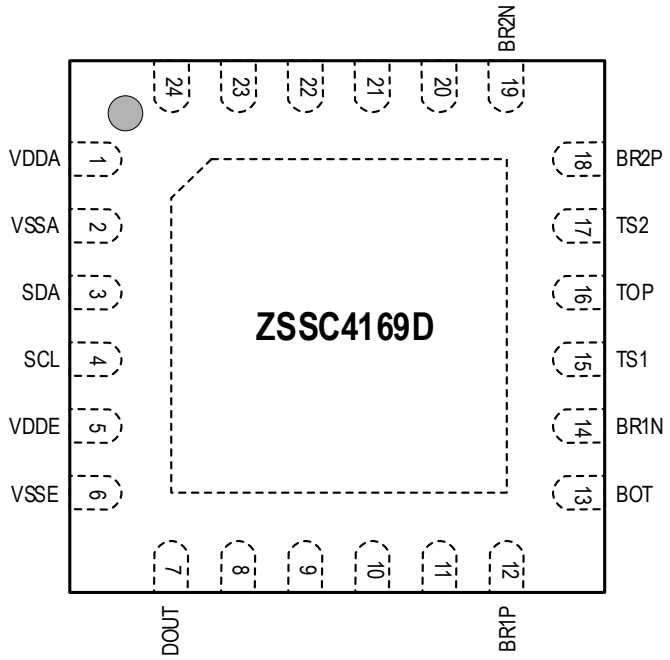


Figure 1. 24-QFN Pin Assignments – Top View

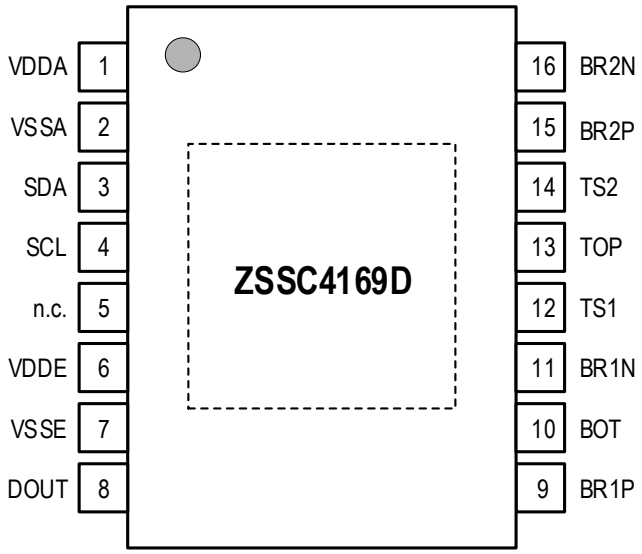


Figure 2. 16-TSSOP Pin Assignments – Top View

2. Pin Descriptions

Table 1. Pin Descriptions

Note: “n.c.” in the following table refers to “No connection.”

24-QFN Pin #	16-TSSOP Pin#	Pin Name	Type	Description
1	1	VDDA	Supply	Internal supply
2	2	VSSA	Ground	Internal ground
3	3	SDA	Analog I/O	I2C data input/output with internal pull-up (*optional production communication interface*)
4	4	SCL	Analog Input	I2C clock, with internal pull-up (*optional production communication interface*)
–	5	–	–	n.c.
5	6	VDDE	Supply	External supply
6	7	VSSE	Analog	External ground
7	8	DOUT	Analog	SENT output and One-Wire Interface (OWI) input/output
8 to 11	–	–	–	n.c.
12	9	BR1P	Analog	Positive bridge sensor input
13	10	BOT	Analog	Negative bridge supply voltage
14	11	BR1N	Analog	Negative bridge sensor input
15	12	TS1	Analog	External temperature sensor input 1
16	13	TOP	Analog	Positive bridge supply voltage
17	14	TS2	Analog	External temperature sensor input 2 (*optional alternative to TS1*)
18	15	BR2P	Analog	Positive bridge sensor input 2 (*not applicable*)
19	16	BR2N	Analog	Negative bridge sensor input 2 (*not applicable*)
20 to 24	–	–	–	n.c.
–	–	EPAD	Ground	Internal ground; connected to VSSA

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the ZSSC4169D-14 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability. In addition, extended exposure to stresses above the operating conditions given in section 4 might affect device reliability.

See section 7.8 for information about overvoltage protection, reverse polarity, and short-circuit protection.

Table 2. Absolute Maximum Ratings

No.	Symbol	Parameter	Conditions	Min	Max	Unit
DS_177	V_{VDDE_MAX}	Supply voltage		-18	18	V
DS_178	V_{DOUT_MAX}	Voltage at the DOUT pin		-18	18	V
DS_179	V_{DIFF_MAX}	Pin voltage difference	Voltage between any two of these pins: VDDE, OUT and VSSE	-18	18	V
DS_180	V_{VDDA_MAX}	Analog supply voltage	On-chip controlled voltage; do not supply externally	-0.3	6	V

No.	Symbol	Parameter	Conditions	Min	Max	Unit
DS_181	V_{PIN_MAX}	Voltage at all other pins	Maximum voltage is V_{VDDA} + 0.3V	-0.3	6	V
DS_182	T_{J_MAX}	Junction temperature	Note: See section 7.8 regarding overvoltage protection	-40	160[a]	°C
DS_183	T_{STOR_MAX}	Storage temperature		-55	155	°C

[a] Required for DS_016 and DS_012.

4. Operating Conditions

The operating conditions below specify the conditions that the application circuit must provide to the device during operation for proper function. Unless otherwise stated, the parameter limits in this section are applied as test conditions for the electrical parameters specified in section 5.

Table 3. Recommended Operating Conditions

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DS_009	V_{VDDE}	Supply voltage	VDDE to VSSE	4.75	5	5.25	V
DS_010	V_{VDDE_EXTD}	Extended supply voltage[a]	VDDE to VSSE; derated accuracy as specified with DS_059.	4.5	5	5.5	V
DS_011	V_{VDDE_OP}	Operating supply voltage[a]	VDDE to VSSE; derated accuracy and derated SENT pulse shaping outside of normal supply range V_{VDDE}. Note for a supply greater than 5.5V: Above the ZSSC4169D-14 overvoltage limitation threshold, the output potential is clipped at this threshold.	4		6	V
DS_012	T_{AMB}	Ambient temperature[b], [c]	Extended Temperature Range (TQE)	-40		150	°C
Informational [d]	$R_{th\_JA\_QFN24}$	Thermal resistance 24-QFN[a]	According to JESD 51		32		K/W
Informational [d]	$R_{th\_JA\_TSSOP16}$	Thermal resistance 16-TSSOP[a] with epad	According to JESD 51		38		K/W
DS_013	R_{BR}	Bridge sensor resistance[a], [e], [f]	One sensor bridge at pins BR1P/BR1N	1		10	kΩ

[a] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[b] Temperature stress over lifetime is restricted to the Temperature Profile described in section 13 or to similar stress caused by equivalent temperature profiles. Use the calculation sheet Temperature Profile Calculation Sheet for temperature stress calculation.

[c] Assuming application conditions according to Test Board Design as per JESD51-7 and natural convection Test Conditions as per JESD51-2.

[d] Package-related parameter.

[e] Symmetric behavior and identical electrical properties (especially the low-pass characteristic) of the differential bridge sensor inputs are required. Unsymmetrical conditions of the sensor and/or external components connected to the sensor input pins can generate a failure in signal operation.

[f] Higher bridge resistance will cause a higher input noise.

5. Electrical Characteristics

All parameter values are valid under the operating conditions specified in section 4 (unless otherwise stated). All parameters are valid for the ambient temperature range T_{AMB} and for the supply voltage range V_{VDDE} = 4.75 to 5.25 V. Unless otherwise defined, the parameters are related to the ZSSC4169D-14 itself. All voltages are referenced to VSSA pin.

The following parameters are specified based on a ZSSC4169D-14 main channel configuration setup using a PGA gain of 100 and assuming a resulting ADC input range usage of ≥ 50%FS. Further preconditions are an ADC resolution of 14 bits, a 2-step A/D conversion scheme using an MSB-to-LSB ratio of 8/6 bit, an oscillator frequency of 8MHz, and an ADC clock frequency of 1MHz (1st step) / 2MHz (2nd step).

Table 4. Electrical Parameters

Note: See important table notes at the end of this table.

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
5.1 Supply Current and System Operating Conditions							
DS_015	I_S	Supply current	Excluding sensor supply current and excluding output current at DOUT pin; oscillator adjusted to f_{OSC} = 8MHz.		8	10	mA
DS_016	P_{OV}	Overvoltage power consumption [a]	5.5V < V_{VDDE} < 18V; excluding sensor and output load.			300	mW
DS_017	$V_{OV\_LIM\_TH}$	Overvoltage limitation threshold [a]	V_{VDDA} is limited if V_{VDDE} exceeds the threshold $V_{OV\_LIM\_TH}$.	5.55		18	V
DS_018	$V_{OV\_OFF\_TH}$	Overvoltage switch-off threshold [a]	The ZSSC4169D-14 is set to the reset state with limited current consumption if V_{VDDE} exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$.	7		12	V
DS_019	$t_{OV\_OFF\_DLY}$	Overvoltage switch-off delay [a]	The ZSSC4169D-14 is set to the reset state with limited current consumption if V_{VDDE} exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$.		10	25	ms
DS_020	$I_{S\_OV\_OFF}$	Supply current limitation in the event of an overvoltage switch-off [a]	Overvoltage switch-off is activated if the supply voltage exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$. V_{VDDE} < 18V; excluding sensor and output load.			10	mA
DS_184	V_{VDDA}	Analog supply voltage	V_{VDDA} is limited if V_{VDDE} exceeds the threshold $V_{OV\_LIM\_TH}$.	0.9		1.0	V_{VDDE}
DS_021	V_{SENS}	Bridge sensor supply voltage	$V_{SENS} = V_{TOP} – V_{BOT}$ at $R_{BR} ≥ 1kΩ$ where V_{TOP} is the voltage at the TOP pin and V_{BOT} is the voltage at BOT pin.	0.9		1	V_{VDDA}
DS_022	V_{POR_OFF}	Power-on reset off-threshold	V_{VDDA} measured referenced to VSSA; POR is active until V_{VDDA} exceeds this threshold.	3.3		3.8	V
DS_023	V_{POR_ON}	Power-on reset on-threshold	V_{VDDA} measured referenced to VSSA; POR is activated if V_{VDDA} falls below this threshold.	3.0		3.6	V

No.	Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DS_024	V_{POR_HYST}	Power-on reset hysteresis [a]	$V_{POR\_ON} – V_{POR\_OFF}$			0.4		V
DS_025	f_{OSC}	Oscillator frequency	Calibrated oscillator frequency. Adjustment via NVM settings is required.		7.6	8	8.6	MHz
5.2 Analog Front-End Characteristics								
DS_027	V_{IN_SPAN}	Differential input span	Analog gain: 1 to 200.		1		800	mV/V
DS_028	$V_{IN\_RNG\_1}$	Input voltage range	Analog gain = 1 Corresponds to V_{ADC_IN}.		0.05		0.95	V_{SENS}
DS_029	$V_{IN\_RNG\_2}$		Analog gain = 2 to 200.		0.3		0.65	V_{SENS}
DS_030	C_{IN}	Capacitance at input [a]	Capacitance at pins BR1P and BR1N to VSSA; Exceeding this parameter increases measurement noise	$R_{BR} \leq 5k\Omega$	0		1.2	nF
				$R_{BR} > 5k\Omega$			0.6	
5.3 A/D Conversion Refer to section 7.5.5.								
DS_032	r_{ADC}	ADC resolution [a]	Fixed resolution selection for each measured signal according to Table 6.		11		14	Bit
DS_033	V_{ADC_IN}	ADC input range [a]	Differential input signal range depending on the analog gain a_{PGA} and on the ADC range shift rs_{ADC}: $V_{ADC\_IN} = V_{IN} * a_{PGA} + rs_{ADC} * V_{SENS}$.		0.05		0.95	V_{SENS}
			Restriction for analog gain > 100.		0.1		0.9	V_{SENS}
DS_034	DNL_{ADC}	DNL [a]					0.95	LSB
DS_035	INL_{ADC}	INL	Best fit.			3	8	LSB_{14}
5.4 Temperature Measurement Refer to section 7.3.3; external temperature sensor (TSE) connected to the TS1 or TS2 pin.								
Informational [b]	OPR_{TS}	Temperature sensor range [a]	Important: This range exceeds the ZSSC4169D-14 operating conditions for T_{AMB}.		-60		200	°C
DS_036	ST_{TSI}	Internal temperature PTAT sensitivity	Raw values, without conditioning calculation; analog gain = 12.6.		20			LSB_{14} /K
DS_037	A_{TSE_D}	External temperature diode channel gain			10			LSB_{14} /mV
DS_038	I_{TSE_D}	External temperature diode bias current			10	20	40	µA
DS_039	V_{TSE_D}	External temperature diode input range [a]	Related to V_{TOP}, absolute measurement.		-1		-0.2	V

No.	Symbol	Parameter	Conditions		Min	Typ	Max	Unit
5.5 V_{VDDE}/V_{VDDA} Measurement								
DS_041	err_{VDDE}	V_{VDDE} supply voltage measurement error					200	mV
Informational	$VDDE_{RNG}$	V_{VDDE} supply voltage measurement range [a]	Important: This range exceeds ZSSC4169D-14 operating conditions (see section 4).		3		8	V
DS_042	err_{VDDA}	V_{VDDA} supply voltage measurement error					200	mV
Informational	$VDDA_{RNG}$	V_{VDDA} supply voltage measurement range [a]	Important: This range exceeds ZSSC4169D-14 operating conditions (see section 4).		3		8	V
5.6 Sensor Diagnostic Tasks								
DS_043	R_{BRSC_TH}	Sensor connection loss detection threshold	Fault check BRSC: Sensor pin to ZSSC4169D-14 pin connection; without capacitive load at pins BR1P and BR1N in the event of a connection loss.		20		100	kΩ
DS_044	r_{BRSC_TH}	Sensor bridge resistor short and open check threshold [a]	Fault check BRSCMRNG: Ratio of sensor bridge branch resistances. Deviation can be caused by shorts or opens of single bridge resistors or by resistor aging.			2		
DS_045	I_{LEAK_TH}	Input leakage detection threshold	Fault check BRSCMRNG: Based on common mode voltage measurement. BRSCMRNG check must be calibrated in conjunction with the sensor bridge. Detectable leakage current depends on the bridge sensor resistance R_{BR} and on the applied analog gain a_{PGA} (refer to Table 9). Limits must be adapted to the required safety target.			10		µA
DS_046	DTI	Diagnostic testing interval [a]					10	ms
DS_047	FMT	Fault messaging time [a]	t_{TICK} = 3µs, SENT pause pulse enabled and set to minimum	Configuration version 2.0 or above			24	ms
				Configuration version below 2.0			22	
	FHTI	Fault handling time interval	Time from appearance of detectable fault until error flag is set (excluding SENT error code transmission)	Configuration version 2.0 or above			22.2	ms
				Configuration version below 2.0			20.2	

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
5.7 System Response							
DS_055	$t_{STARTUP}$	Startup time [a]	Time to first valid output after power-on; V_{VDDE} slew rate > 0.1V/µs; f_{OSC} = 8MHz.			20	ms
DS_056	OUR	Output update rate [a]	ZSSC4169D-14 internal output update, asynchronous to SENT transmission.			1.5	ms
DS_057	ORT	Output response time [a]	100% input step, t_{TICK} = 3µs, SENT pause = on, minimum.			5	ms
DS_058	RE	Ratiometricity error	Maximum error for V_{VDDE} from 5V to 4.75V or to 5.25V Ratiometricity error is already contained in overall failure (DS_059).			500	ppm
DS_059	F_{ALL_BR}	Overall failure Deviation from ideal line including INL, gain, offset, and temperature impacts; excluding sensor-caused effects	Differential sensor readout V_{VDDE} = 4.75V to 5.25V.			0.5	%FS
	$F_{ALL\_BR\_EXTD}$ [a]		Differential sensor readout V_{VDDE_EXTD} = 4.5V to 5.5V.			1.0	%FS
	F_{ALL_HBR} [a]		Single-ended sensor readout V_{VDDE} = 4.75V to 5.25V.			1.0	%FS
	$F_{ALL\_HBR\_EXTD}$ [a]		Single-ended sensor readout V_{VDDE_EXTD} = 4.5V to 5.5V.			1.5	%FS
	$F_{ALL\_DERATED}$ [a]		In the operating supply voltage range V_{VDDE_OP}.			5	%FS
5.8 Nonvolatile Memory							
DS_065	T_{AMB_NVM}	Ambient temperature for NVM programming [c]		-40		125	°C
DS_066	N_{NVM_PAGE}	NVM page count [a]	Pages available for writing	22			
DS_067	t_{NVM_RET}	Data retention [a]	Temperature profile. [d]	15			years
DS_068.1	$t_{NVM\_WRI\_DIFF}$	Programming time without soaking [a]	Per programmed data word in differential mode.			1.7	ms
DS_068.2	$t_{NVM\_WRI\_RED}$		Per programmed data word in redundant mode.			3.3	

[a] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[b] The temperature sensor range is the calibration target for the SENT output of the SDM temperature channels. This target can be adjusted.

[c] Take into consideration additional package and temperature range restrictions.

[d] Over lifetime and valid for the dice. Note that the package can cause additional restrictions. Use the calculation sheet *Renesas Temperature Profile Calculation Sheet* (available on request) for temperature stress calculation.

6. Interface Characteristics

Table 5. Interface Characteristics

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
6.1 SENT Output Refer to *SAE J2716 JAN2010 (Rev.3) and APR2016 (Rev. 4) Specification* for detailed specifications for SENT Physical and Software Layer.							
DS_048	t_{TICK}	Tick time [a]	Adjustment step = 1µs for tick times ≥ 3µs. Tick times less than 3µs are not compliant to *SAE J2716 (JAN2010 and APR2016)*.	2.4		90	µs
DS_049	t_{TICK_JITTER}	Tick time jitter [a], [b]	Valid for tick time ≤ 10µs, 6-sigma value			300	ns
DS_050	n_{SDM}	Number of SDMs	Absolute count of different messages	0		32	
DS_051	n_{SDM_CYC}	Number of SDM in SDM cycle	Message count in SDM cycle, including use of different priority levels.	0		64	
DS_052	n_{SDM_PRIO}	SDM transmission priority levels		1		3	
DS_053	t_{PAUSE}	Pause length	Fixed frame length.	12		768	t_{TICK}
DS_054	t_{FRAME}	Frame length	Pause pulse disabled, 6 data nibble, and variable frame length.	154		270	t_{TICK}
			Pause pulse enabled, 6 data nibble, and fixed frame length.	282		922	t_{TICK}
6.2 ZACwire™ One-Wire Interface One-wire communication at the DOUT pin.							
DS_060	t_{PWRUP}	Power-on time [a]	Time to ready for communication after power-on; V_{VDDE} slew rate > 0.1V/µs; f_{OSC} = 8MHz			3.0	ms
DS_061	$t_{OWI\_STARTWIN}$	Start window [a]	OWI enabled latest 5ms after power-on; V_{VDDE} slew rate > 0.1V/µs; f_{OSC} = 8MHz		250		ms
DS_062	$V_{OWI\_IN\_H}$	OWI voltage level HIGH [a]	Master to slave	0.80			V_{VDDE}
DS_063	$V_{OWI\_IN\_L}$	OWI voltage level LOW [a]	Master to slave			0.20	V_{VDDE}
DS_064	$V_{OWI\_OUT\_L}$	Slave output level LOW	Open drain, I_{OL} < 2mA			0.1	V_{VDDE}

[a] No measurement in volume production; parameter is guaranteed by design and/or quality observation.

[b] Compliant to SAE J2716 APR2016. – SAE J2716 JAN2010 specifies maximum jitter of 50ns at tick time = 3µs and maximum jitter of 250ns at tick time = 10µs.

7. Circuit Description

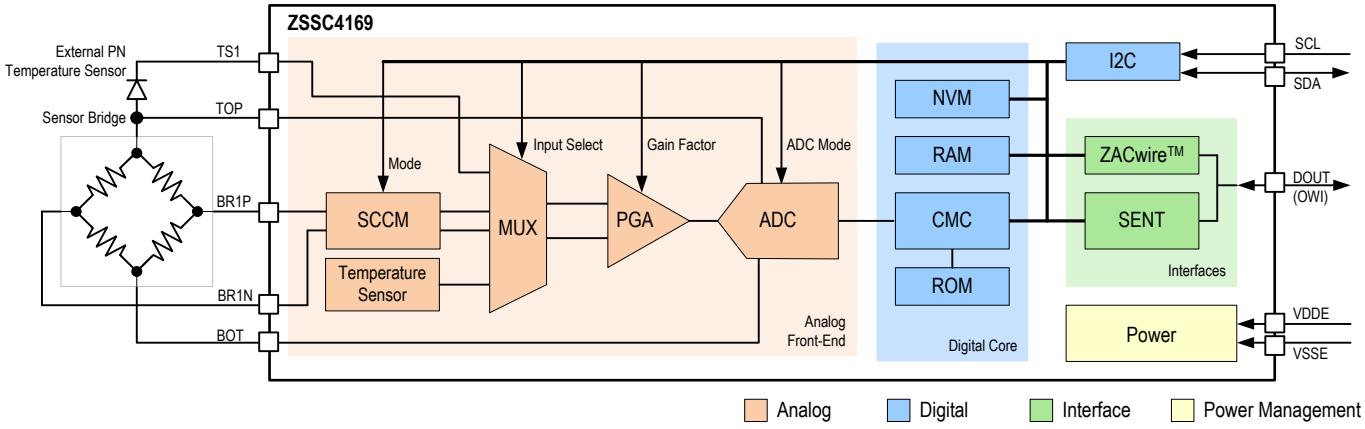
7.1 General Operation Description

The ZSSC4169D-14 is a sensor signal conditioner for readout of resistive bridge sensors. The sensor signal is pre-amplified and converted to a digital signal by the analog-to-digital-converter (ADC). Then the digital conversion result is offset compensated and gain adjusted. Temperature coefficients and nonlinearity of the sensing element are compensated, if necessary. Then the calculated conditioning result is output using the SENT protocol.

Signal conditioning processes the following tasks:

- Measurement of the voltage signal of the connected resistive sensing element
- Measurement of temperature
- Conditioning calculation for the sensor signal
- SENT output of the conditioning result

Figure 3. Block Diagram



SCCM	Sensor Check and Common Mode Adjustment Unit
MUX	Multiplexer
PGA	Programmable Gain Amplifier
ADC	Analog-to-Digital Converter
CMC	Calibration Microcontroller
ROM	Read-Only Memory for Correction Formula and Algorithm
NVM	Nonvolatile Memory for Configuration and Conditioning Coefficients
RAM	Volatile Memory for Configuration and Conditioning Coefficients
SENT	SENT Controller and SENT Physical Layer Output Stage
ZACwire™	Digital One-Wire Interface
I2C	I2C Digital Interface
PWR	Power Management and Protection Unit

7.2 Signal Path

The ZSSC4169D-14 signal path consists of the analog front-end (AFE), the digital signal processing unit, the SENT Controller, and the SENT physical interface (SENT PHY). In addition, this is supported by a serial digital one-wire interface (ZACwire™).

The resistive bridge sensor signal is input via the BR1P and BR1N pins and is handled as a fully differential signal. Both signal lines have a dynamic range symmetrical to the common mode potential (analog ground; equal to $V_{VDDA}/2$) so that it is possible to process positive and negative differential input signals. These differential signals are pre-amplified by the programmable gain amplifier (PGA) and are converted to digital values by the A/D converter (ADC). In addition, the measurement of a half-bridge sensor signal (half of the full bridge, not an independent channel) is available either via the BR1P pin or via the BR1N pin referenced to an on-chip reference half-bridge and using the same signal path.

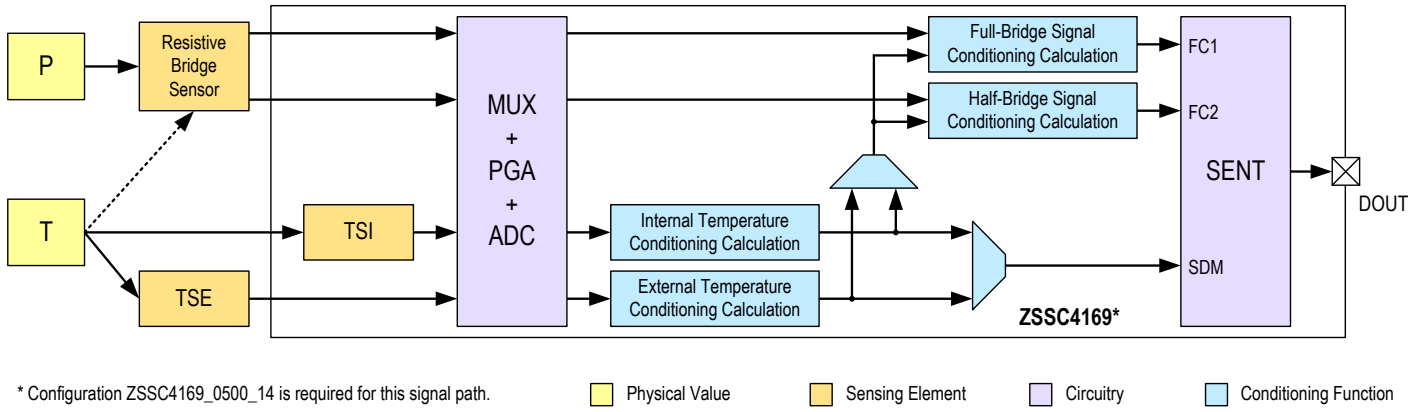
A multiplexer (MUX) selects and transmits the signals from either the bridge sensor or the selected temperature sensor to the analog-to-digital converter (ADC) in a defined sequence. The temperature sensors can be either an external diode or an internal proportional-to-absolute-temperature (PTAT) source selected by NVM configuration.

The digital signal correction is processed in the calibration microcontroller (CMC) using ROM-resident correction formulas and sensor-specific coefficients stored in the NVM. The configuration data and the conditioning coefficients are programmed into the NVM during the calibration process by digital one-wire communication via the DOUT pin.

During the calibration process, raw measurement values can be requested via the digital interfaces.

The ZSSC4169D-14 provides SENT output transmission according to the *SAE J2716 SENT Specification*. Depending on the programmed configuration, there are several SENT output modes. These modes include assignment of the various sensor signals to the SENT Fast and Serial Data Message (SDM) communication channels as well as the configuration of the SENT frame itself.

Figure 4. Configuration ZSSC4169D-14 Main Signal Path



7.3 Signal Measurement

7.3.1 Full Bridge Sensor Measurement

The ZSSC4169D-14 measures a differential sensor signal (BR1P to BR1N); i.e. a bridge or voltage source type signal. The signal path is ratiometric and fully differential. The ratiometric reference voltage V_{REF} is equal to ($V_{TOP} – V_{BOT}$).

7.3.2 Half-Bridge Sensor Measurement

The ZSSC4169D-14 supports the measurement of a half-bridge sensor signal referenced to an internal reference potential of nominal (V_{TOP} - V_{BOT})/2. The signal path is ratiometric and fully differential. The ratiometric reference voltage V_{REF} is equal to (V_{TOP} - V_{BOT}). The signal input pin is selectable between BR1P and BR1N. As both half-bridges are measured consecutively, a bridge common mode voltage can be derived by averaging both measurement results.

7.3.3 Temperature Measurement

The ZSSC4169D-14 supports different methods for acquiring temperature data needed for the conditioning of the sensor signal as well as for a separate temperature measurement:

- Internal PTAT sensor
- External PN-junction temperature sensor connected to the TS1 or TS2 pin and referenced to the sensor top potential (TOP pin).

7.3.4 Measurement Cycle

The measurement cycle is the sequence of measurements processed during the Normal Operation Mode (NOM). It delivers the raw measurement results from all connected sensors and from the supervision functions. The measurements are processed sequentially, all using the ADC to convert the analog input voltages to a digital value.

Table 6 shows the list of the ZSSC4169D-14 measurement tasks. The full-bridge differential input voltage (BR1P – BR1N) and the single-ended input voltage from one of the half-bridges (either BR1P or BR1N) are measured most frequently in the main measurement slots while all other measurements are inserted alternatively as auxiliary measurements.

The resulting measurement cycle configured in the ZSSC4169D-14 is shown in Figure 5. The sequence of measurements is retained even if any fault check connected to a measurement is disabled. The sensor signal conditioning is synchronized to the main measurement tasks to assure a regular internal output update rate.

In the configuration illustrated in Figure 5, the internal output update rate (OUR) of the full-bridge sensor signal as well as of the half-bridge signal is about 0.95ms (nominal); the update rate of all auxiliary measurement results and their connected fault checks is 8.7ms (nominal).

Table 6. Measurement Task List

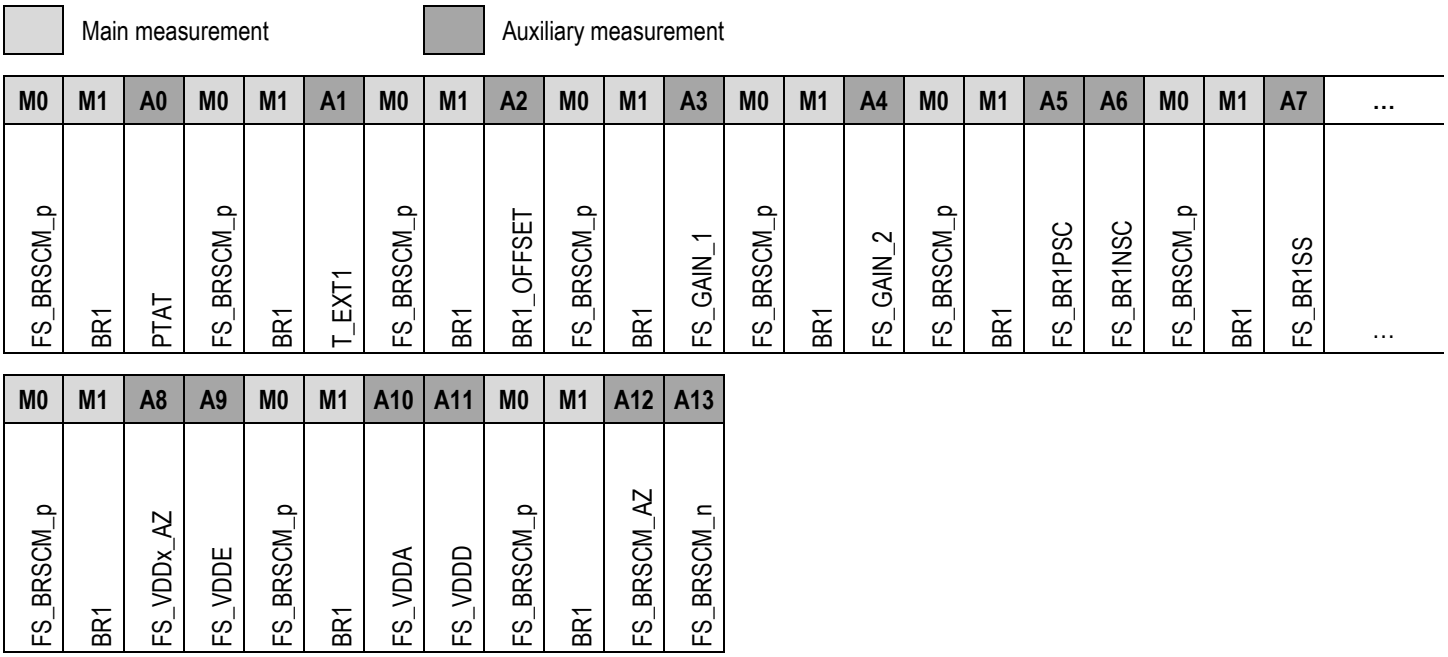
Note: See important notes at the end of this table.

Slot	Measurement Task	Name	Description	Resolution [bit]	Time [a] [µs]
Main 0	0 / M0	FS_BRSCM_p[/n]	Half-bridge input voltage at BR1P or BR1N pin (configurable) for half-bridge and bridge common mode measurement	13	203
Main 1	1 / M1	BR1	Full-bridge differential voltage; main sensor signal	14	332
Aux 0	2 / A0	PTAT	On-chip PTAT including auto-zero compensation	13	406
Aux 1	3 / A1	T_EXT1	External temperature sensor including auto-zero compensation	13	406
Aux 2	4 / A2	BR1_OFFSET	Full-bridge auto-zero compensation value	14	332
Aux 3	5 / A3	FS_GAIN_1	Main signal gain check value 1	14	332
Aux 4	6 / A4	FS_GAIN_2	Main signal gain check value 2	14	332
Aux 5	7 / A5	FS_BR1PSC	Bridge sensor connection check BR1P	11	244
	8 / A6	FS_BR1NSC	Bridge sensor connection check BR1N	11	
Aux 6	9 / A7	FS_BR1SS	Bridge sensor short check	11	212
Aux 7	10 / A8	FS_VDDx_AZ	Supply voltage measurement auto-zero compensation value	12	342
	11 / A9	FS_VDDE	Supply V_{VDDE} measurement	12	

Slot	Measurement Task	Name	Description	Resolution [bit]	Time [a] [µs]
Aux 8	12 / A10	FS_VDDA	Analog supply V_{VDDA} measurement	12	342
	13 / A11	FS_VDDD	Digital supply voltage measurement for fault check VDDDRNG	12	
Aux 9	14 / A12	FS_BRSCM_AZ	Bridge common mode and half-bridge auto-zero compensation value	13	406
	15 / A13	FS_BRSCM_n[/p]	Half-bridge input voltage at BR1N or BR1P pin for bridge common mode voltage; select the pin that is the opposite of the pin configured for task M0	13	

[a] Time values are given based on a system clock frequency of 8MHz.

Figure 5. Measurement Cycle



7.4 Signal Conditioning

Refer to the *Configuration Description for ZSSC4169D-14* for the details for the coefficients and weights referenced in this section.

7.4.1 Internal Temperature Sensor Signal Conditioning

The internal temperature sensor signal conditioning is processed every time that a new measurement result value *T_int* is available from the analog-to-digital conversion. The conditioning calculation provides compensation of offset, gain, and nonlinearity.

$$tsi\_comp = 2^{-40} * 2^{w_{tsi\_2}} * c_{tsi\_2} * T\_int^2 + 2^{-25} * 2^{w_{tsi\_1}} * c_{tsi\_1} * T\_int + 2^{-9} * 2^{w_{tsi\_0}} * c_{tsi\_0} \quad (1)$$

The conditioning coefficients c_{tsi_i} are stored as signed 16-bit values (sint16, two's complement) in the NVM during the calibration process. The weights w_{tsi_i} are unsigned 4-bit values (uint4).

The normalized conditioning result of the internal temperature sensor *tsi_comp* is stored as a signed 16-bit value (sint16, two's complement) in the RAM output memory. This value can be assigned to a SENT SDM output channel and can be selected as *ts_comp* for the conditioning calculation of the full-bridge or half-bridge sensor signal (see section 7.4.3).

7.4.2 External Temperature Sensor Signal Conditioning

The external temperature sensor signal conditioning is processed every time that a new measurement result value *T_ext* is available from the analog-to-digital conversion. The conditioning calculation provides compensation of offset, gain, and nonlinearity.

$$tse\_comp = 2^{-40} * 2^{w_{tse\_2}} * c_{tse\_2} * T\_ext^2 + 2^{-25} * 2^{w_{tse\_1}} * c_{tse\_1} * T\_ext + 2^{-9} * 2^{w_{tse\_0}} * c_{tse\_0} \quad (2)$$

The conditioning coefficients c_{tse_i} are stored as signed 16-bit values (sint16, two's complement) in the NVM during the calibration process. The weights w_{tse_i} are unsigned 4-bit values (uint4).

The normalized conditioning result of the external temperature sensor *tse_comp* is stored as a signed 16-bit value (sint16, two's complement) in the RAM output memory. This value can be assigned to a SENT SDM output channel and can be selected as *ts_comp* for conditioning calculation of the full- or half-bridge sensor signal (see section 7.4.3).

Table 7. On-Chip and External Temperature Signal Conditioning Coefficients

Coefficient	Configuration Field	
	On-Chip PTAT	External Temperature Sensor
w_{ts_2}	w_tsi_2	w_tse_2
w_{ts_1}	w_tsi_1	w_tse_1
w_{ts_0}	w_tsi_0	w_tse_0
c_{ts_2}	c_tsi_2	c_tse_2
c_{ts_1}	c_tsi_1	c_tse_1
c_{ts_0}	c_tsi_0	c_tse_0

7.4.3 Full Bridge and Half Bridge Sensor Signal Conditioning

The full-bridge and the half-bridge sensor signal conditioning is processed every time that a new measurement result value *br* is available from the analog-to-digital conversion. The conditioning calculation provides compensation of the non-linearity and the temperature-dependent offset and gain.

Temperature-dependent bridge offset calculation up to 2nd order using conditioned temperature value *ts_comp*:

$$br\_offset = 2^{-40} * 2^{w_{o2}} * c_{o2} * ts\_comp^2 + 2^{-25} * 2^{w_{o1}} * c_{o1} * ts\_comp + 2^{-9} * 2^{w_{o0}} * c_{o0} \quad (3)$$

Temperature-dependent gain calculation up to 2nd order using conditioned temperature value *ts_comp*:

$$br\_gain = 2^{-40} * 2^{w_{g2}} * c_{g2} * ts\_comp^2 + 2^{-25} * 2^{w_{g1}} * c_{g1} * ts\_comp + 2^{-9} * 2^{w_{g0}} * c_{g0} \quad (4)$$

Offset and gain compensation of the bridge sensor signal *br*:

$$Y = 2^{14} * (br + br\_offset) * br\_gain^{-1} \quad (5)$$

Nonlinearity compensation up to 3rd order:

$$br\_comp = 2^{-56} * 2^{w_{l3}} * c_{l3} * Y^3 + 2^{-41} * 2^{w_{l2}} * c_{l2} * Y^2 + 2^{-25} * 2^{w_{l1}} * c_{l1} * Y + 2^{w_{l0}} * c_{l0} * 2^{-9} \quad (6)$$

The conditioning coefficients c_{oi}, c_{gi} and c_{li} are stored as signed 16-bit values (sint16, two's complement) in the NVM during the calibration process. The weights w_{oi}, w_{gi} and w_{li} are unsigned 4-bit values (uint4). All intermediate results and the final conditioning results *br_comp* for the full-bridge or the half-bridge sensor are stored as signed 16-bit values (sint16, two's complement) in the RAM output memory (for addresses, refer to the *Configuration Description for ZSSC4169D-14*). These values can be low-pass filtered and can be assigned to SENT Fast output channels.

Table 8. Full-Bridge and Half-Bridge Signal Conditioning Coefficients

Coefficient	Configuration Field		Coefficient	Configuration Field		Coefficient	Configuration Field	
	Full-Bridge	Half-Bridge		Full-Bridge	Half-Bridge		Full-Bridge	Half-Bridge
w_{o2}	fb_wo2	hb_wo2	w_{g2}	fb_wg2	hb_wg2	w_{l3}	fb_wl3	hb_wl3
w_{o1}	fb_wo1	hb_wo1	w_{g1}	fb_wg1	hb_wg1	w_{l2}	fb_wl2	hb_wl2
w_{o0}	fb_wo0	hb_wo0	w_{g0}	fb_wg0	hb_wg0	w_{l1}	fb_wl1	hb_wl1
c_{o2}	fb_co2	hb_co2	c_{g2}	fb_cg2	hb_cg2	w_{l0}	fb_wl0	hb_wl0
c_{o1}	fb_co1	hb_co1	c_{g1}	fb_cg1	hb_cg1	c_{l3}	fb_cl3	hb_cl3
c_{o0}	fb_co0	hb_co0	c_{g0}	fb_cg0	hb_cg0	c_{l2}	fb_cl2	hb_cl2
						c_{l1}	fb_cl1	hb_cl1
						c_{l0}	fb_cl0	hb_cl0

7.4.4 Bridge Sensor Common Mode Signal Conditioning

The bridge sensor common mode voltage conditioning is processed every time that new measurement result values for both half-bridges are available from the analog-to-digital conversion. The conditioning calculation provides compensation of the bridge sensor signal dependent nonlinearity and of the temperature-dependent offset and gain.

Bridge sensor signal dependent offset calculation using conditioned bridge sensor value *br_comp*:

$$cm\_offset\_P = 2^{-15} * c_{brcm\_o} * br\_comp \quad (7)$$

Temperature dependent offset calculation up to 2nd order using conditioned temperature value *ts_comp*:

$$cm\_offset\_T = 2^{-40} * 2^{w_{brcm\_o2}} * c_{brcm\_o2} * ts\_comp^2 + 2^{-25} * 2^{w_{brcm\_o1}} * c_{brcm\_o1} * ts\_comp + 2^{-9} * 2^{w_{brcm\_o0}} * c_{brcm\_o0} \quad (8)$$

Temperature and bridge sensor signal dependent offset:

$$cm\_offset = (cm\_offset\_T + cm\_offset\_P)/2 \quad (9)$$

Bridge sensor signal dependent gain calculation using conditioned bridge sensor value *br_comp*:

$$cm\_gain\_P = 2^{-15} * c_{brcm\_g} * br\_comp \quad (10)$$

Temperature dependent gain calculation up to 2nd order using conditioned temperature value *ts_comp*:

$$cm\_gain\_T = 2^{-40} * 2^{w_{brcm\_g2}} * c_{brcm\_g2} * ts\_comp^2 + 2^{-25} * 2^{w_{brcm\_g1}} * c_{brcm\_g1} * ts\_comp + 2^{-9} * 2^{w_{brcm\_g0}} * c_{brcm\_g0} \quad (11)$$

Temperature and bridge sensor signal dependent gain:

$$cm\_gain = (cm\_gain\_T + cm\_gain\_P)/2 \quad (12)$$

Sensor common mode calculation using both half-bridge measurement values *br_p, br_n*.

$$brcm = (br\_n + br\_p)/2 \quad (13)$$

Offset and gain compensation of the sensor common mode signal *brcm*:

$$brcm\_comp = 2^{14} * (brcm + cm\_offset) * cm\_gain^{-1} \quad (14)$$

The conditioning coefficients c_{brcm_oi} and c_{brcm_gi} are stored as signed 16-bit values (sint16, two's complement) in the NVM during the calibration process. The weights w_{brcm_oi} and w_{brcm_gi} are unsigned 4-bit values (uint4).

The normalized conditioning result of the bridge sensor common mode voltage *brcm_comp* is stored as a signed 16-bit value (sint16, two's complement) in the RAM output memory (for address, refer to the *Configuration Description for ZSSC4169D-14*). This value can be used for the supervision of the sensor and of the input leakage at the pins BR1P and BR1N.

7.5 Analog Front-End

7.5.1 Overview

The analog front-end (AFE) consists of the multiplexer (MUX), the programmable gain amplifier (PGA), and the analog-to-digital converter (ADC). The internal offset of the analog front-end is eliminated by an auto-zero compensation.

7.5.2 SCCM

The sensor check and common mode block (SCCM) implements the self-diagnostic features for the analog front-end. The SCCM provides the sensor connection checks (short and open circuit) as well as several other diagnostic functions.

7.5.3 Input Multiplexer

The input multiplexer (MUX) selects one of the various inputs and connects it to the signal path utilizing a single ADC. It allows a very flexible signal routing between the sensors and the ZSSC4169D-14.

7.5.4 Programmable Gain Amplifier

The sensor signal can be amplified by the on-chip programmable amplifier (PGA) using a gain between 2 and 200. Alternatively the PGA can be bypassed and the sensor signal is applied directly to the ADC. The gain is individually adjustable for the bridge sensor signal measurement task in order to provide an ADC input signal span of greater than 50% FS.

Table 9 shows the adjustable gains of the PGA, the corresponding signal spans, and the common mode range limits.

Table 9. Adjustable PGA Gains and Resulting Sensor Signal Spans and Common Mode Ranges

Nominal PGA Gain a_{PGA}	Maximum Input Span V_{IN_SPAN} [mV/V]	Input Common Mode Range V_{IN_CM} [% V_{VDDA}]
PGA bypassed	800	5 to 95
2.08	385	30 to 65
3.15	254	30 to 65
4.31	186	30 to 65
6.25	128	30 to 65
8.31	96	30 to 65
12.6	63	30 to 65
17.3	46	30 to 65
25.0	32	30 to 65
33.2	24	30 to 65
50.4	16	30 to 65
69.0	12	30 to 65
100.0	8	30 to 65
138.0	6	30 to 65
200.0	4	30 to 65

Recommendation: To achieve the best stability and linearity performance of the AFE, operate the PGA in a differential output voltage range within 10% to 90% of the ratiometric reference voltage $V_{REF} = V_{SENS} = (V_{TOP} – V_{BOT})$. The gain must be selected to guarantee this constraint for the entire operating temperature range of the application and for the specified sensor bridge tolerances.

Table 10. Requirements – Programmable Gain Amplifier

No.	Parameter	Value	Unit
DS_069	Nominal minimum adjustable PGA gain	2.08	–
DS_070	Nominal maximum adjustable PGA gain	200	–
DS_071	PGA gain adjustment steps	14	–

7.5.5 Analog-to-Digital Converter

The analog-to-digital converter is implemented using the full-differential switched-capacitor technique. The conversion is largely insensitive to short-term and long-term instabilities of the clock frequency. The ADC provides adjustability for the A/D conversion input voltage range shift.

7.6 SENT Output

7.6.1 Overview

ZSSC4169D-14 provides two different digital interfaces for the output of data and status messages:

- The SENT controller and physical layer for SENT transmission complies with the *SAE J2716 JAN2010 (Rev. 3) and APR2016 (Rev. 4) Specification* and enables readout of conditioned sensor signal data.
- The ZACwire™ interface for one-wire communication supports the sensor configuration and calibration process.

The SENT interface is the main application output interface. The configuration of the SENT frame format and the assignment of sensor signals and fault messages to the SENT output channels are configurable.

In addition to other protocols, the SENT interface supports the application-specific SENT protocols Single Sensor (P, P/t), Single Pressure Secure Sensor (P/S, P/S/t) and Pressure-Pressure Sensor (P1/P2, P1/P2/t) [1].

Table 11. SENT Output Protocol Options

No.	Parameter	Value	Unit
DS_072	SENT protocol Single Pressure Sensor P and P/t	n.a.	–
DS_073	SENT protocol Single Pressure Secure Sensor P/S and P/S/t	n.a.	–
DS_074	SENT protocol Pressure-Pressure Sensor P1/P2 and P1/P2/t	n.a.	–

[1] According to SAE J2716 APR2016 (Rev. 4) SENT specification, the term “Pressure” refers to the bridge sensor element.

7.6.2 SENT Fast Channel Modes and Frame Format

The ZSSC4169D-14 SENT interface supports various frame configurations:

- SENT Fast Channel Mode: one or two Fast data channels.
- SENT Transmission Mode: fixed SENT frame length and adjustable pause pulse, or SENT transmission without pause pulse.

The ZSSC4169D-14 provides the following different Fast data channel modes that support fault-safe data transmission:

- 12-bit FC1, 8-bit counter and 4-bit zero (6 nibbles) (*SAE J2716 SENT* specification, appendix H.5 [1])
- 12-bit FC1, 8-bit counter and 4-bit MSN of FC1 inverted (6 nibbles) (H.4 [1])

The ZSSC4169D-14 also provides the following different Fast data channel modes that are compliant to SAE J2716:

- 12-bit FC1 (3 nibbles) (H.2 [1])
- 12-bit FC1 and 12-bit FC1 inverted (6 nibbles) (H.1 [1])
- 12-bit FC1 and 12-bit FC2 (6 nibbles) (H.1 [1])

The SENT frame transmission is not synchronized to the ZSSC4169D-14 internal output data update. The internal output data update is determined by the ADC resolution for the sensor signal measurements. The output data update time and the SENT frame length are generally different. Depending on the SENT frame length used, it is possible that individual data is either sent twice or it is skipped and not sent at all.

After power-on, the initial output values of the SENT Fast data channels are 0 until the first valid output data is available from the measurement and conditioning cycle.

Table 12. Requirements – SENT Fast Channel Modes and Frame Format

No.	Parameter	Value	Unit
DS_075	Fast channel modes	5	–
DS_076	Fast channel 1 data: conditioned differential full-bridge sensor signal	n.a.	–
DS_077	Fast channel 2 data: source assignment configurable: → half-bridge sensor signal from BR1P or from BR1N	n.a.	–
DS_078	SENT tick time adjustment; step: 0.125µs for t_{TICK} < 16µs; 1µs for t_{TICK} ≥ 16µs	Configurable	–

[1] According to SAE J2716 SENT specification APR2016 (Rev. 4)

7.6.3 SENT SDM Channel Modes

The ZSSC4169D-14 SENT interface supports up to 32 different serial data messages (SDM) transmitted in the SDM data channels. The SDM format, the number of SDMs, and the transmission priority are configurable. For details for the configuration fields, refer to the *Configuration Description for ZSSC4169D-14*).

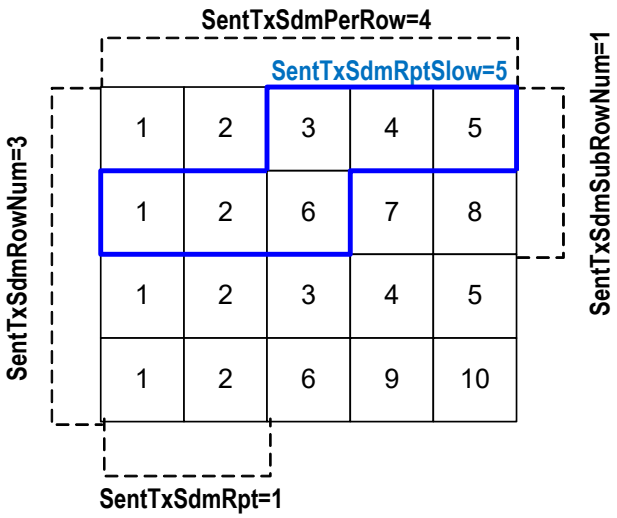
Options include

- Enhanced SDM format with up to 32 SDMs
- Mode with no SDM available (SDM bits in the status nibble are set to “0”)
- Configurable SDM IDs
- Three priority levels with a configurable number of SDMs per priority level

SDM Cycle Configuration Example:

Priority Level	SDM ID			
1	1	2		
2	3	4	5	6
3	7	8	9	10

Configuration via Field	Value
SentTxSdmRpt	1
SentTxSdmRowNum	3
SentTxSdmPerRow	4
SentTxSdmRptSlow	5
SentTxSdmSubRowNum	1



7.6.4 SENT Output Operation Modes

The ZSSC4169D-14 provides SENT output of the conditioned sensor measurement results at the DOUT pin. This pin is also connected to the ZACwire™ interface for “End of Line” communication using a one-wire communication protocol (OWI).

There are four different selectable modes for starting the OWI communication in combination with the SENT output:

SENT_TX_INIT:

- SENT transmission starts immediately after the initialization phase.
- During the initialization, the DOUT pin is set to the output idle state.
- SENT data channels are set to “0” until the first valid values are available.
- OWI Rx is enabled in parallel to the SENT output for a time window.
- OWI communication can be started by transmitting the command for starting Command Mode (CM) during this time window. The communication master must overwrite the output potential at the DOUT pin for transmitting the first command (DOUT pin drive capability is current limited).

SENT_TX_FIRST_CYC:

- SENT transmission starts after the first measurement and conditioning cycle.
- During the initialization and the first cycle, the DOUT pin is set to the output idle state.
- SENT data channels start transmission with valid values.
- OWI Rx is enabled in parallel with the SENT output for a time window.
- OWI communication can be started by transmitting the command for starting CM during this time window. The communication master must overwrite the output potential at the DOUT pin for transmitting the first command (DOUT pin drive capability is current limited).

SENT_TX_STRT_WINDOW:

- SENT transmission starts only after a time window; the DOUT pin is set to the output idle state.
- DOUT is weakly pulled to VDDA (pull-up current: ~2.5µA). OWI Rx is enabled for a specified time window.
- OWI communication can be started by transmitting the command for starting CM during this time window. The communication master must overwrite the output potential at the DOUT pin for transmitting the first command (DOUT pin drive capability is current limited).

OWI:

- SENT transmission is disabled. OWI Rx/Tx is enabled without time limitation. OWI communication can be started by transmitting the command for starting CM.

All fault checks are processed in the initialization phase before calculating the first conditioned sensor signal. In the event of a detected failure and when no fault filtering is activated, the transmission starts with transmitting a fault code instead of transmitting invalid sensor data (different from initialization value “0”) via the SENT interface in all SENT modes.

The output idle state of the ZSSC4169D-14 is defined as follows:

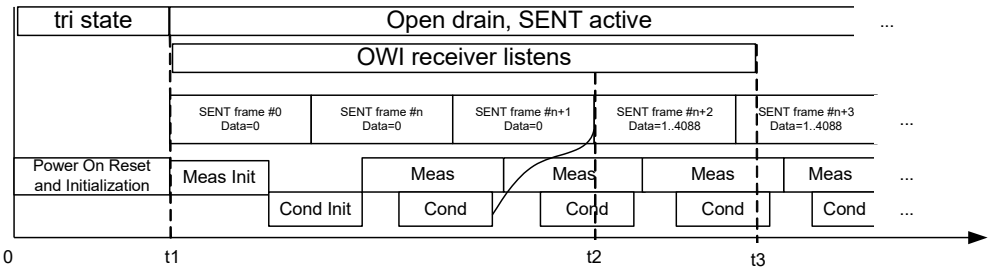
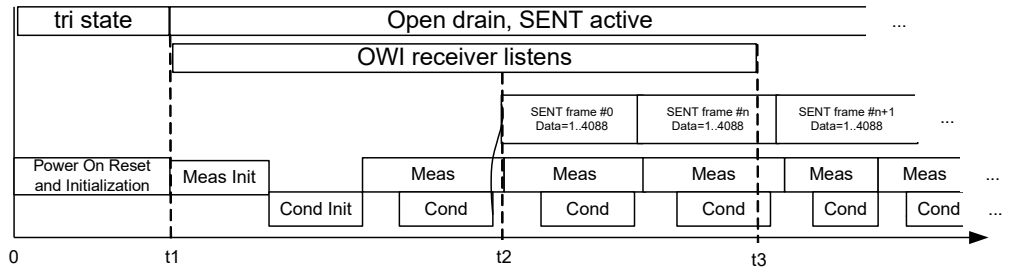
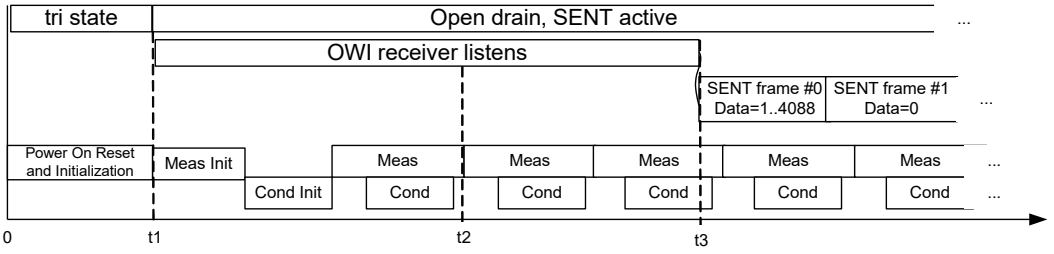
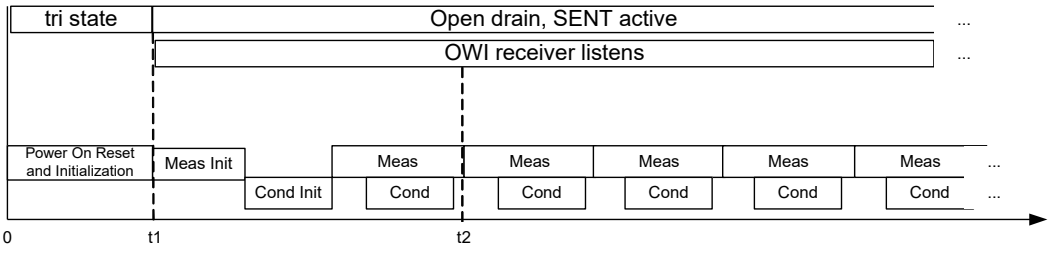
- The DOUT pin is switched to high impedance; DOUT is weakly pulled to VDDA (pull-up current: ~2.5µA).
- The final resulting potential at the output is defined by the (pull-up) load resistor at the SENT communication line.

After power-on reset and after initializing from NVM (t1), the measurement and conditioning cycle starts. The timing of the measurement and conditioning tasks is fixed. If output data is available, it is transmitted via the SENT Fast Channels. The first valid data is available at time t2. The OWI receiver is always enabled after power-on for a time window (t3) to make the start of OWI communication possible.

Table 13. SENT Output Operation Modes and Initialization Behavior

No.	Parameter	Value	Unit
DS_079	Number of SENT output operation modes (SENT_TX_INIT, SENT_TX_FIRST_CYC, SENT_TX_STRT_WINDOW, OWI)	4	–
DS_080	SENT transmission starts with initialization value 0. Valid sensor data is output only after processing all enabled fault checks.	n.a.	–

Table 14. SENT Output Modes

Configuration Field	Value (hex)	Description
DoutMd	0	SENT_TX_INIT 
	1	SENT_TX_FIRST_CYC 
	2	SENT_TX_STRT_WINDOW 
	3	OWI 

7.6.5 SENT Pulse Shaping

The ZSSC4169D-14 configuration provides several fixed adjustment options to optimize the rise and fall times depending on the configured SENT tick time. This helps to achieve the optimal EMC performance regarding electromagnetic emission.

7.7 NVM OEM Data Memory

The ZSSC4169D-14 provides a NVM memory area for the storage of OEM data, which is physically part of the NVM memory module and is one-time programmable (OTP), but it is delimited from the configuration and calibration data by dedicated commands for READ and WRITE access. The data is stored in redundant mode, which increases data reliability. Additional data protection and multiple-time programming data management must be implemented by the OEM.

Table 15. Requirements – NVM OEM Data Memory

No.	Parameter	Value	Unit
DS_081	NVM OEM data memory (OTP)	8	16-bit words
DS_083	Dedicated command for NVM OEM data memory write access; includes WRITE authorization for the limited memory area only	n.a.	–
DS_084	Dedicated command for NVM OEM data memory read access	n.a.	–

7.8 Overvoltage and Short Circuit Protection

The ZSSC4169D-14 is designed for a 5V supply provided by an electronic control unit (ECU).

The ZSSC4169D-14 and the connected sensors are protected from over-voltage and reverse polarity damage by an internal supply voltage limiter. The SENT output pin DOUT is protected regarding short circuit, over-voltage, and reverse polarity. These functions are described in Table 16 and are valid for operation of the ZSSC4169D-14 in the application circuit shown in section 11 within the specifications of absolute maximum ratings given in section 3.

Note: The specified junction temperature range T_J (see Table 2) is in force not only for operation but also applies for all protection cases listed in Table 16. In the event of an over-voltage, the device might have increased power dissipation. Depending on the sensor elements and the output load, this might lead to a violation of the maximum junction temperature.

Table 16. Overvoltage, Reverse Polarity, and Short Circuit Protection

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Overvoltage and Reverse Polarity Protection							
DS_085	Maximum voltage at VDDE to VSSE	V_{VDDE_OV1}	DOUT is connected to VSSE or VDDE (connection resistance value = 0 to ∞)	0		18	V
DS_086	Maximum voltage at VDDE to DOUT	V_{VDDE_OV2}	VSSE is connected to DOUT or VDDE (connection resistance value = 0 to ∞)	0		18	V
DS_087	Maximum voltage at DOUT to VSSE	V_{DOUT_OV1}	VDDE is connected to DOUT or VSSE (connection resistance value = 0 to ∞)	0		18	V
DS_088	Maximum voltage at DOUT to VDDE	V_{DOUT_OV2}	VSSE is connected to DOUT or VDDE (connection resistance value = 0 to ∞)	0		18	V
DS_089	Maximum voltage at VSSE to VDDE	V_{VSSE_OV1}	DOUT is connected to VSSE or VDDE (connection resistance value = 0 to ∞)	0		18	V
DS_090	Maximum voltage at VSSE to DOUT	V_{VSSE_OV2}	VDDE is connected to DOUT or VSSE (connection resistance value = 0 to ∞)	0		18	V

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Short Circuit Protection							
DS_091	Current limitation in the event of a VDDA to VSSA short circuit	$I_{VDDA\_SHRT\_VSSA}$				60	mA
DS_092	Current limitation in the event of a DOUT to VSSE short circuit	$I_{DOUT\_SHRT\_VSSE}$	Output is activated; output current limitation has been adjusted	-10		-2	mA
DS_093	Current limitation in the event of a DOUT to VDDE short circuit	$I_{DOUT\_SHRT\_VDDE}$	Output is activated; output current limitation has been adjusted	2		10	mA

8. Fault-Safe Operation

8.1 Fault-Safe Operation Modes

Fault checks verify the operation of the ZSSC4169D-14 and of the connected sensing element at power-on and during Normal Operation Mode (NOM). If a fault is detected, the Diagnostic Mode (DM) is activated and the fault status is provided via one of the two methods described below depending on the diagnostic mode.

ZSSC4169D-14 differentiates between two DMs with different behavior:

Static Diagnostic Mode

- Measurement and conditioning cycle are interrupted.
- SENT transmission is stopped, and the output pin DOUT is either driven to a HIGH output level or is switched to high impedance.
- The ZACwire™ interface for one-wire communication (OWI) is enabled; both RAM output pages are readable. The command *StrtCmdMd* must be sent to switch to Command Mode for further command processing.
- If enabled, the ZSSC4169D-14 is reset, i.e. the ZSSC4169D-14 is restarted including a reset of all status registers.
- The ZSSC4169D-14 can be restarted by a power-off/power-on sequence.

Temporary Diagnostic Mode

- Measurement and conditioning cycle are continuously processed.
- Fault checks are continuously processed including fault filtering (see below).
- SENT transmission is continued. At least one of following the fault messaging options is activated: the fault code is transmitted in the SENT Fast Channel; fault bit(s) are set in the SENT status nibble; the fault code is transmitted in the SDM Channel (SENT fault messaging and fault codes are configurable).
- The ZACwire™ interface for one-wire communication is enabled. The command *StrtCmdMd* must be sent to switch to Command Mode for further command processing (SENT output must be overwritten by the OWI master).
- The ZSSC4169D-14 returns to Normal Operation Mode including SENT transmission of valid sensor signal if fault checks do not detect continuation of fault conditions.

The **Fault Filtering** of the ZSSC4169D-14 is defined as follows:

- Fault filtering is only processed for fault checks assigned to the Temporary DM.
- Fault filtering is a low-pass filter that delays the activation and deactivation of the Temporary DM.
- In the event of a fault detection, faults are re-checked before entering Temporary DM.
- In the case of Temporary DM, detected fault conditions that no longer exist are re-checked before returning from Temporary DM to NOM.
- Fault filtering is an up-and-down event counter with programmable increment, threshold, and hysteresis; the decrement is always 1.

8.2 Fault Messaging

8.2.1 Overview

The SENT offers three different options for fault messaging:

- Fault codes in the data channels (the Fast channels as well as the SDM channels; e.g., the channel used for temperature)
- Two status bits in the SENT status nibble
- SDM Channel status word

8.2.2 SENT Fast Channel Fault Codes

For the 12-bit SENT Fast channel, the output value interval [4089, 4095] is reserved for fault codes. This is according to the SENT standard. In addition, the value 0 is used to signal initialization (no valid data available).

In the ZSSC4169D-14, the SENT Fast channel fault codes are selectable, and a dedicated fault code must be assigned to every supervised fault. A fault prioritization is available, and in the event of simultaneous detection of multiple faults, the fault code of the highest prioritized fault is transmitted.

8.2.3 SENT Status Bits

According to the SENT standard, the SENT status nibble contains two bits for status information. The assignment of the status bits to the individual detectable faults is configurable.

8.2.4 SENT SDM Channel Status Codes

The SENT standard defines a SMD channel status word assigned to the SDM identifier #01.

In the ZSSC4169D-14, the SENT SMD channel status codes are freely programmable, and a dedicated fault code must be assigned to every supervised fault. A fault prioritization is available, and in the event of simultaneous detection of multiple faults, the status code of the highest prioritized fault is transmitted.

8.2.5 Timing Definitions

The timing for the update of the SENT output and for the fault messaging is defined in Figure 6 and Figure 7. The relevant timing parameters are listed in Table 17.

Table 17. Timing Parameter

Symbol	Parameter	Description
OUR	Output update rate	Internal update rate of the main signal data
ORT	Output response time	Latency from the main signal event to the completion of the SENT transmission of this signal event
DTI	Diagnostic testing interval	Rate of fault check processing
FRT	Fault Reaction Time	Internal time of calculation and processing of fault detection
FTT	Fault Transmission Time	The time to transmit the fault indication over the SENT interface
FMT	Fault messaging time	Latency from the fault event to the completion of the SENT transmission of the fault message

Figure 6. Output-Update Timing Diagram

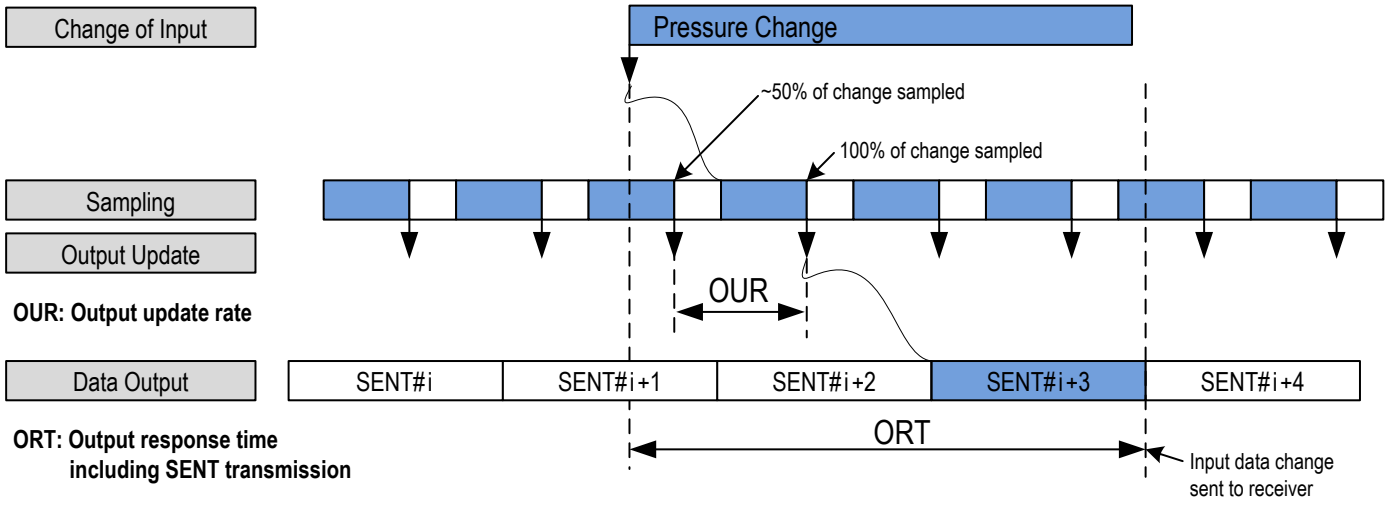
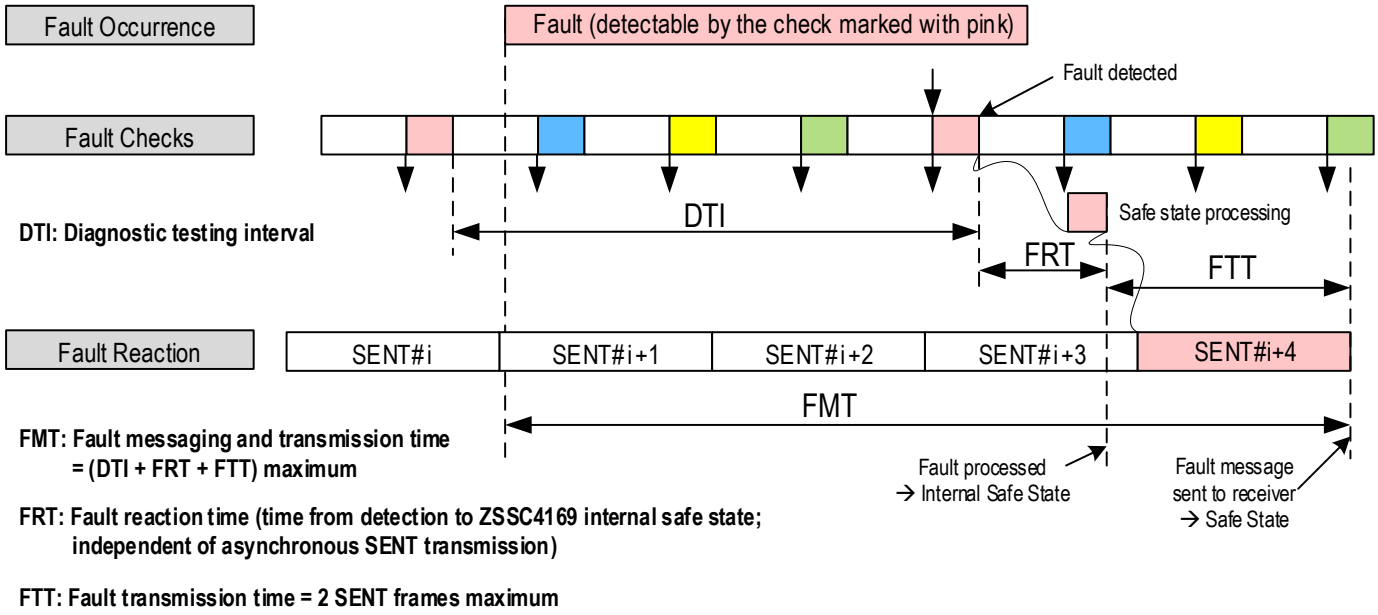


Figure 7. Fault-Messaging Timing Diagram

Note: In this figure, the different colors indicate the different fault checks processed in the cycle.



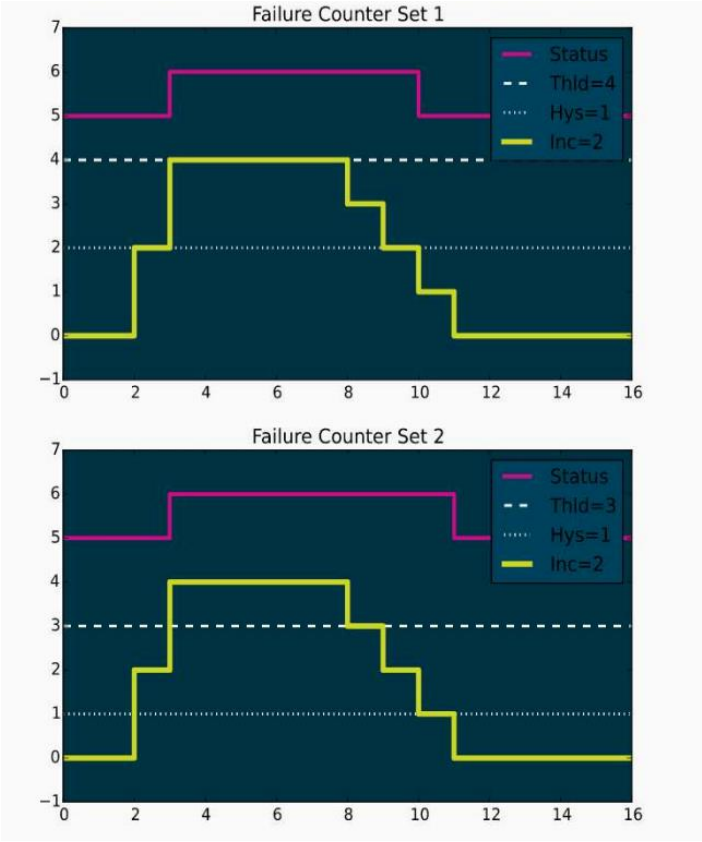
8.2.6 Fault Filtering

Fault filtering is implemented to confirm the fault detected by a fault check before sending a fault message. This function is realized by counting the fault events. The fault filtering is defined by a threshold, a step size for increment, a maximum value, and a hysteresis value. Two failure counter sets are used and assigned to the fault checks. Fault filtering directly influences the FMT.

For sensor connection check (BRSC) no fault filtering is available to enhance detection sensitivity of this fault.

Table 18. Failure Counter Configuration

Failure Counter Set	Hysteresis	Max Value	Increment	Threshold
1	1	2	2	4
2	1	2	2	3



9. Fault Checks

9.1 Overview

The ZSSC4169D-14 implements a diagnostic mechanism architecture that can support end-user applications up to ASIL C requirements in regard to random failure diagnostic capabilities. Table 19 lists the available fault checks.

Table 19. Fault Checks Overview

This table shows an overview of the available fault checks. For details, refer to Table 20, Table 21, Table 22, and Table 23.

Note: See important notes at the end of this table.

No.	Identifier	Fault Check
ZSSC4169D-14 Self-Supervision Fault Checks		
DS_094	VDDAPOR	Analog supply voltage V_{VDDA} under-voltage check; power-on reset (POR)
DS_095	VDDDBOD	Digital supply under-voltage check; brownout detection (BOD)
DS_096	OSCFAIL	Oscillator-fail check based on a second oscillator/timer; reset after oscillator restart
DS_097	ROMCRC	ROM content CRC check
DS_098	NVMCRC	NVM content CRC check
DS_099	RAMCRC	RAM content CRC check
DS_100	RAMPRTY	RAM content parity check
DS_101	WWDG	Windowed watchdog; microcontroller and measurement and conditioning cycle active check
DS_102	INITCRC	Measurement and conditioning initialization check; processing, order, and configuration
DS_103	MCYCCRC	Measurement cycle operation check; processing, order, and configuration
	AFEMUX	AFE input multiplexer operation check
	REGCRC	Configuration register content CRC check
DS_104	CCYCCRC	Conditioning cycle operation check; processing, order, and configuration
DS_105	SENTDATA	SENT data consistency check
DS_106	SENTPHY [a]	SENT transmission monitoring
DS_107	CHIPP	Chipping check
DS_108	COMP	Computational check; microcontroller conditioning calculation, code processing, and peripheral bus access check
DS_109	VDDDRNG	Digital supply voltage range check; digital core and memory supply
DS_110	ADCOFFSRNG	ADC offset range check; ADC operation check
DS_111	AFEGAIN	AFE gain check
DS_112	VDDARNG	Analog supply voltage V_{VDDA} range check; front-end and sensor supply
DS_171	H/BRSRAW	Half- and full-bridge sensor raw data check; ADC operation check
Sensing Element Fault Checks		
DS_113	BRSC	Bridge sensor connection check
DS_114	BRSS	Bridge sensor short check

No.	Identifier	Fault Check
DS_115	BRSCMRNG	Bridge sensor common mode range check and sensor input leakage check
DS_116	TSI	Internal temperature sensor operation check
DS_117	TSEC	External temperature sensor connection check
Environment and Operating Condition Fault Checks		
DS_118	BRSRNGH	Bridge sensor conditioning result range check: upper limit
DS_119	BRSRNGL	Bridge sensor conditioning result range check: lower limit
Informational [b]	HBRSRNG	Half-bridge sensor range check
DS_120	TSIRNG	Internal temperature sensor range check (over-temperature/under-temperature)
DS_121	TSERNG	External temperature sensor range check (over-temperature/under-temperature)
DS_122	VDDEUV	Supply voltage V_{VDDE} under-voltage check
DS_123	VDDEOV	Supply voltage V_{VDDE} over-voltage check
DS_124	CSAT	Conditioning calculation saturation check

[a] SENTPHY is not applicable for SENT tick times less than 3µs.

[b] HBRSRNG is available for SENT Fast channel P2 transmission of the half-bridge sensor signal.

9.2 Fault Checks for ZSSC4169D-14 Self-Supervision

The ZSSC4169D-14 provides several fault checks that supervise the ZSSC4169D-14 hardware itself.

Table 20. ZSSC4169D-14 Hardware Fault Checks

Note: See important notes at the end of this table.

No.	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [b]
DS_094	V_{VDDA} under-voltage check (VDDAPOR); power-on reset	< 200µs	–	Always on	Static	1
DS_095	Digital supply under-voltage check (VDDDBOD); brownout detection	< 200µs	–	Always on	Static	1
DS_096	Oscillator fail check (OSCFAIL)	< 200µs	–	Always on	Static	1
DS_097	ROM CRC check (ROMCRC)	< FMT	–	Always on	Static	1
DS_098	NVM CRC check (NVMCRC)	$t_{STARTUP}$	Page-wise 16-bit CRC	Always on	Static	1
DS_099	RAM CRC check (RAMCRC)	< FMT	Page-wise 16-bit CRC	Always on	Static	1
DS_100	RAM parity check (RAMPRTY)	< FMT	–	Always on	Static	1
DS_101	Windowed watchdog (WWDG)	< 2 × OUR	–	Always on	Static	1
DS_102	Initialization phase check (INITCRC)	$t_{STARTUP}$	16-bit CRC	Enable/ Disable	Static	1

No.	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [b]
DS_103	Measurement cycle check (MCYCCRC) including ▪ AFE input multiplexer check (AFEMUX) ▪ Register data check (REGCRC)	< FMT	16-bit CRC	Enable/ Disable	Static	1
DS_104	Conditioning cycle check (CCYCCRC)	< FMT	16-bit CRC	Enable/ Disable	Static	1
DS_105	SENT data consistency check (SENTDATA)	t_{FRAME}	–	Enable/ Disable	Static	1

[a] "Enable/Disable" indicates that the user can enable or disable the check.

[b] Prioritization describes the default fault messaging order ("1" means highest priority).

Table 21. ZSSC4169D-14 Operation and Cycle Fault Checks

No.	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [b]
DS_106	SENT transmission monitoring (SENTPHY) [c]	< FMT	–	Enable/ Disable	Temporary	2
DS_107	Chipping check (CHIPP)	< FMT	–	Enable/ Disable	Temporary	2
DS_108	Computational check (COMP) including microcontroller arithmetic, code processing, and bus access	< FMT	–	Enable/ Disable	Temporary	2
DS_109	Digital supply voltage check (VDDDRNG)	< FMT	Lower limit	Enable/ Disable	Temporary	3
DS_110	ADC offset check (ADCOFFSRNG)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	3
DS_172	Half-bridge sensor raw data check (HBRSRAW)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	3
DS_111	AFE gain check (AFEGAIN)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	4
DS_173	Full-bridge sensor raw data check (BRSRAW)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	4
DS_112	Analog supply voltage check (VDDARNG)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	15

[a] "Enable/Disable" indicates that the user can enable or disable the check.

[b] Prioritization describes the default fault messaging order ("1" means highest priority).

[c] SENTPHY is not applicable for SENT tick times less than 3µs.

9.3 Fault Checks for Sensing Element Supervision

The ZSSC4169D-14 provides several fault checks that supervise the sensing elements.

Table 22. Sensing Element Fault Checks

No.	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [b]
DS_113	Bridge sensor connection check (BRSC)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	6
DS_114	Bridge sensor short check (BRSS)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	7
DS_115	Bridge sensor common mode range check (BRSCMRNG) including sensor input leakage check	< FMT	Lower/upper limit	Enable/ Disable	Temporary	8
DS_116	Internal temperature sensor operation check (TSI)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	9
DS_117	External temperature sensor connection check (TSEC)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	10

[a] "Enable/Disable" indicates that the user can enable or disable the check.

[b] Prioritization describes the default fault messaging order ("1" means highest priority).

9.4 Fault Checks for Environment and Operating Condition Supervision

The ZSSC4169D-14 provides several fault checks that supervise the environment and operating conditions.

Table 23. Environment and Operating Condition Fault Checks

No.	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [b]
DS_118	Bridge sensor range check upper limit (BRSRNGH)	< FMT	Upper limit	Enable/ Disable	Temporary	13
DS_119	Bridge sensor range check lower limit (BRSRNGL)	< FMT	Lower limit	Enable/ Disable	Temporary	13
Informational [c]	Half-bridge sensor range check (HBRSRNG)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	12
DS_120	Internal temperature sensor range check (TSIRNG)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	9
DS_121	External temperature sensor range check (TSERNG)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	11
DS_122	Supply V_{VDDE} under-voltage check (VDDEUV)	< FMT	Lower limit	Enable/ Disable	Temporary	15

No.	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [b]
DS_123	Supply V_{VDDE} overvoltage check (VDDEOV)	< FMT	Upper limit	Enable/ Disable	Temporary	14
DS_124	Conditioning calculation saturation (CSAT)	< FMT	-	Enable/ Disable	Temporary	16

[a] "Enable/Disable" indicates that the user can enable or disable the check.

[b] Prioritization describes the default fault messaging order ("1" means highest priority).

[c] HBRSRNG is available for SENT Fast channel P2 transmission of the half-bridge sensor signal.

Table 24. SENT Transmission Fault Checks

Note: SENT transmission fault checks must be implemented on the SENT receiver.

Fault Check	Messaging Time	Adjustable	Notes	Priority [a]
SENT CRC (SENTCRC)	t_{FRAME}	n.a.	SENT receiver	n.a.
SENT tick time (SENTTICK)	t_{FRAME}	n.a.	SENT receiver	n.a.
SENT timeout (SENTIMEOUT)	t_{FRAME}	n.a.	SENT receiver	n.a.
SENT sync time (SENTSYNC)	t_{FRAME}	n.a.	SENT receiver	n.a.
SENT idle state (SENTIDLE)	t_{FRAME}	n.a.	SENT receiver	n.a.

[a] Prioritization describes the default fault messaging order ("1" means highest priority).

10. Configuration and Adjustment

The ZSSC4169D-14 is based on a dedicated configuration, which must be adjusted for the application. This includes the adjustment of some ZSSC4169D-14 parameters, the configuration of the sensor signal measurements, the calibration of the sensor conditioning calculation, and the setup of the SENT protocol.

Table 25. ZSSC4169D-14 Parameter Adjustment

No.	Parameter	Conditions	Value	Unit
DS_125	Oscillator frequency	Adjustable (adjustment steps)	32	–

Table 26. Sensor Signal Measurement Configuration

No.	Parameter	Conditions	Value	Unit
DS_126	Source select for P2	Half-bridge selection for SENT Fast Channel FC2	BR1P / BR1N	–
DS_127	Gain P1	Full-bridge sensor signal gain (adjustment steps)	14	–
DS_128	Gain P2	Half-bridge sensor signal gain (adjustment steps)	14	–
DS_129	Gain TSE	External temperature sensor signal gain (adjustment steps)	14	–
DS_130	Source select for BR temperature compensation	Selection of the temperature signal used for temperature compensation of the main sensor signal	TSI / TSE	–

No.	Parameter	Conditions	Value	Unit
DS_131	Source select for SENT temperature output	Selection of the temperature signal used for the SENT temperature measurement output	TSI / TSE	–
DS_132	TSE type	External temperature sensor type	Diode	–

Table 27. Calibration of Sensor Signal Conditioning Calculation

No.	Parameter	Conditions	Value	Unit
DS_133	Full-bridge signal offset compensation	Coefficients for 2nd order temperature compensation (number of coefficients)	4	16-bit words
DS_134	Full-bridge signal gain compensation	Coefficients for 2nd order temperature compensation (number of coefficients)	4	16-bit words
DS_135	Full-bridge signal nonlinearity compensation	Coefficients for 3rd order nonlinearity compensation (number of coefficients)	5	16-bit words
DS_136	Full-bridge signal filter	Conditioned full-bridge signal filter: average and differential coefficients	1	16-bit words
DS_137	Half-bridge signal offset compensation	Coefficients for 2nd order temperature compensation	4	16-bit words
DS_138	Half-bridge signal gain compensation	Coefficients for 2nd order temperature compensation	4	16-bit words
DS_139	Half-bridge signal nonlinearity compensation	Coefficients for 3rd order nonlinearity compensation	5	16-bit words
DS_140	Half-bridge signal filter	Conditioned half-bridge signal filter: average and differential coefficients	1	16-bit words
DS_141	Temperature TSI conditioning	Temperature from internal temperature sensor; coefficients for gain, offset, and 2nd order nonlinearity compensation	4	16-bit words
DS_142	Temperature TSI filter	Conditioned internal temperature signal filter: average and differential coefficients	2	–
DS_143	Temperature TSE conditioning	Temperature from external temperature sensor; coefficients for gain, offset, and 2nd order nonlinearity compensation	4	16-bit words
DS_144	Temperature TSE filter	Conditioned external temperature signal filter: average and differential coefficients	2	–
DS_145	Common mode voltage offset compensation	Coefficients for 2nd order temperature compensation and 1st order bridge sensor signal compensation	5	16-bit words
DS_146	Common mode voltage gain compensation	Coefficients for 2nd order temperature compensation and 1st order bridge sensor signal compensation	5	16-bit words

Table 28. SENT Protocol Configuration

No.	Parameter	Conditions	Value	Unit
DS_147	Tick time	Clock tick times	[2.4 to 128]	µs
DS_148	Frame length	Enables constant frame length	[282 to 1024]	Clock ticks
DS_149	Sensor type	Single Sensor (P/t), Single Secure Sensor (P/S/t), Pressure-Pressure Sensor (P1/P2/t)	Selectable	–
DS_151	SDM priority	Up to 3 priority levels	Configurable	–
DS_152	SDM ID	SDM Identifier	Programmable	–
DS_153	SDM data	Static SDM data	Programmable	–
DS_154	SDM initial data	Initial data for SDM signal channels	Programmable	–
DS_155	Temperature SDM	Priority level for SENT SDM channel of conditioned temperature output	Configurable	–
DS_156	Status SDM	Diagnostic codes	Programmable	–

Table 29. Fault Handling Configuration

No.	Parameter	Conditions	Value	Unit
DS_157	Watchdog reset	The Static Diagnostic Mode results in a functional halt or in a reset after watchdog timeout.	Selectable	–
DS_158	BRSRNGH limits	Full-bridge sensor conditioning result check upper limit	Upper limit	16-bit words
DS_159	BRSRNGL limits	Full-bridge sensor conditioning result check lower limit	Lower limit	16-bit words
Informational [a]	HBRSRNG limits	Half-bridge sensor conditioning result check limits	Upper limit, lower limit	16-bit words
DS_161	TSIRNG limits	Internal temperature sensor range check limits	Upper limit, lower limit	16-bit words
DS_162	TSE limits	External temperature sensor connection check limits	Upper limit, lower limit	16-bit words
DS_163	TSERNG limits	External temperature sensor range check limits	Upper limit, lower limit	16-bit words
DS_164	BRSCMRNG limits	Full-bridge sensor signal conditioned common mode voltage check limits	Upper limit, lower limit	16-bit words
DS_165	AFEGAIN input	AFE gain check input voltages	2 AFEDAC configurations	16-bit words
DS_166	AFEGAIN limits	AFE gain check limits	2 upper limits, 2 lower limits	16-bit words
DS_167	COMP input	Computation check input value	Input value	16-bit word
DS_168	COMP limits	Computation check limits	Upper limit, lower limit	16-bit words
Informational [b]	MCYCCRC value	Measurement cycle check expected CRC	Initial CRC, cycle CRC	16-bit words

No.	Parameter	Conditions	Value	Unit
Informational [b]	CCYCCRC value	Conditioning cycle check expected CRC	Initial CRC, cycle CRC	16-bit words

[a] HBRSRNG is available for SENT Fast channel P2 transmission of the half-bridge sensor signal.

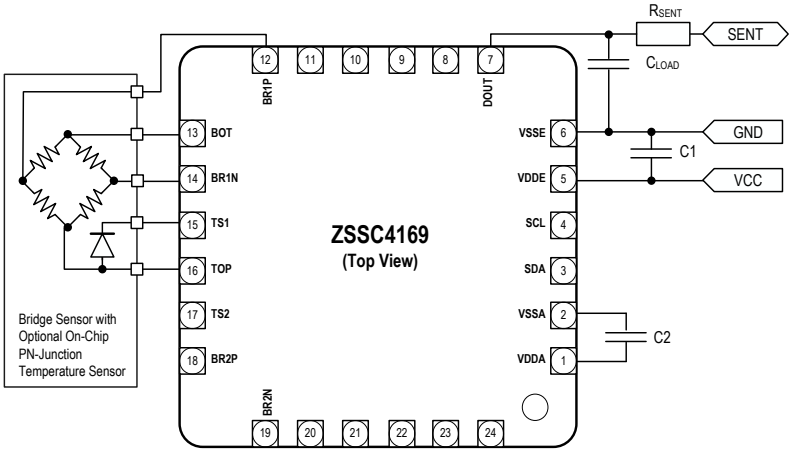
[b] Generation of the expected CRCs for MCYCCRC and CCYCCRC fault checks is supported by a dedicated command.

11. Application Circuit and External Components

Figure 8. Application Circuit Example of a Pressure and Temperature Sensor with SENT Output

Application features:

- 5V module is powered by the application's electronic control unit (ECU)
- Sensor module with 3-pin connector provides pressure and media or ambient temperature measurement data via SENT output
- Temperature signal for pressure signal correction can be derived either from the on-chip PTAT or from an external diode (connected to TS1 or TS2)
- End-of-line calibration uses one-wire communication via the DOUT pin



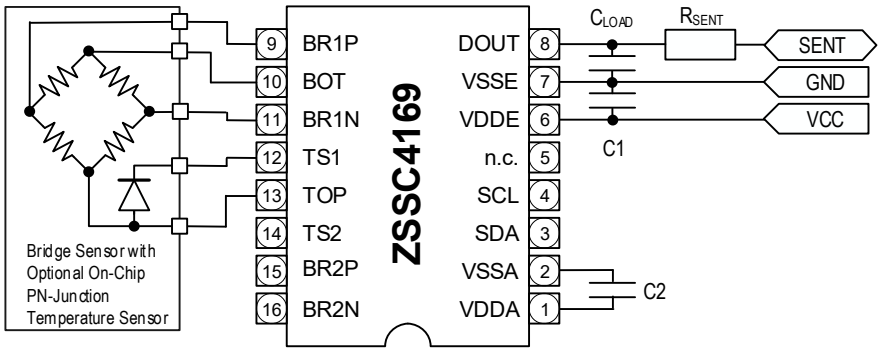


Table 30. Dimensioning of External Components for the Application Example

Component	Symbol	Conditions	Min	Typical	Max	Unit
Capacitor	C1	V_{MAX} ≥ 32V		100 ± 20%		nF
Capacitor	C2	V_{MAX} ≥ 10V		100 ± 20%	470 + 20%	nF
Capacitor	C_{LOAD}	V_{MAX} ≥ 32V		2.2 ± 20%		nF
Resistor	R_{SENT}				50	Ω

Note: The component values are examples and must be adapted to the requirements of the application, in particular to the EMC requirements.

12. ESD Protection and EMC Specification

12.1 ESD Protection

All pins have an ESD protection of ≥2000V according to the Human Body Model (HBM with 1.5kΩ/100pF, based on MIL883, Method 3015.7). The VDDE, VSSE, and DOUT pins have an additional ESD protection of ≥ 4000V (HBM with 1.5kΩ/100pF, based on MIL883, Method 3015.7).

The levels of ESD protection are tested with devices in a 4 × 4 mm 24-QFN package during the product qualification.

12.2 Electromagnetic Emission

The wired emission of the externally connected pins of the ZSSC4169D-14 is measured according to the following standard: *IEC 61967_4:2002 + A1:2006.*

Measurements must be performed with the application circuit described in Figure 8; SENT transmission uses a tick time of 9µs.

For the off-board pins, the spectral power measured with the 150Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code H10kN*. For the VSSE pin, the spectral power measured with the 1Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code H10kN.*

12.3 Conducted Susceptibility (DPI)

The conducted susceptibility of externally connected pins of the device is measured according to the IEC 62132-4 standard.

Measurements must be performed with the application circuit described in Figure 8; the sensor bridge is replaced by a 3-resistor string connected to TOP, BR1P, BR1N, and BOT; SENT transmission uses a tick time of 9µs.

Table 31 gives the specifications for the DPI tests. RES refers to the coupling impedance. CAP refers to the injection capacitance.

Table 31. Conducted Susceptibility (DPI) Tests

No.	Test	Frequency Range	Power [dBm]	Load Pins	Protocol	Error Band[a]	Comment
DS_169	DPI, direct coupled	1MHz to 10MHz	20dBm	VDDE, DOUT	SENT	±1%	RES = 50Ω CAP= 4.7nF
DS_170	DPI, direct coupled	> 10MHz	30dBm	VDDE, DOUT	SENT	±1%	RES = 50Ω CAP = 4.7nF

[a] Error band regarding main signal (SENT FC1).

13. Reliability and RoHS Conformity

The ZSSC4169D-14 is qualified according to the AEC-Q100 standard, operating temperature grade 0. A fit rate < 5 FIT (junction temperature = 55°C, confidence level = 60%, activation energy = 0.7eV) is estimated.

A typical fit rate for TSMC's CV018BCD technology, which is used for the ZSSC4169D-14, is < 1 FIT (temperature = 55°C, confidence level = 60%, activation energy = 0.7eV).

The reliability calculation is based on an average operating junction temperature of 90.5°C over an operating lifetime of 15000 hours, in normal operating conditions, and according to the ambient temperature profile listed in Table 32.

Table 32. Ambient Temperature Profile (Example)

Operating Ambient Temperature [°C]	Relative Time [%] Based on a 15000h Operating Lifetime	Absolute Time [h]
-40	2	300
-20	8	1200
0	15	2250
25	25	3750
55	25	3750
85	17	2550
125	6	900
150	2	300

The calculation examples in this chapter are based on the following assumptions:

- Normal Operation mode:
  - Maximum supply current is 10mA at maximum supply voltage of 5.5V
  - Minimum SENT load resistance of 10kΩ
  - This causes a maximum power dissipation of P_{max} = 5.5V × 10mA + 5.5V × 5.5V / 10kΩ ≈ 58mW
- Over-voltage condition:
  - maximum power dissipation is $P_{max,OV}$ = 300mW; (output is switched off)

Calculation examples for self-heating (maximum thermal resistor in 24-QFN package is $R_{th\_JA\_QFN24}$ = 32K/W):

- Temperature difference in Normal Operation: $T_J – T_{AMB}$ = 32K/W × P_{max} < 1.9K
  → With the conditions above, the maximum junction temperature T_J is approx. 2K greater than the ambient temperature T_{AMB}.
- Temperature difference in Overvoltage Conditions (18V): $T_J - T_{AMB}$ = 32K/W × $P_{max,OV}$ = 9.6K
  → With these conditions, the maximum junction temperature T_J is approx. 10K greater than the ambient temperature T_{AMB}.

Calculation examples for self-heating (maximum thermal resistor in 16-TSSOP package is $R_{th\_JA\_TSSOP16}$ = 38K/W):

- Temperature difference in Normal Operation: $T_J – T_{AMB}$ = 38K/W × P_{max} < 2.3K
  → With the conditions above, the maximum junction temperature T_J is approx. 2.3K greater than the ambient temperature T_{AMB}.
- Temperature difference in Overvoltage Conditions (18V): $T_J - T_{AMB}$ = 38K/W × $P_{max,OV}$ = 11.4K
  → With these conditions, the maximum junction temperature T_J is approx. 12K greater than the ambient temperature T_{AMB}.

The ZSSC4169D-14 complies with the RoHS directive and does not contain hazardous substances. The complete RoHS declaration update can be downloaded at http://www.idt.com/ehs.

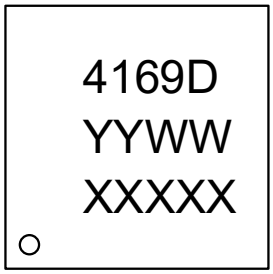
14. Package Drawings

The package outline drawings and land pattern are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

- For the 24-QFN package
- For the 16-TSSOP package

15. Marking Diagram

15.1 QFN24 Marking

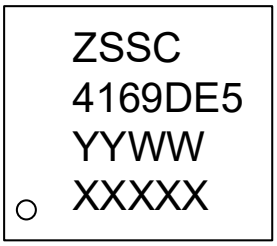


Line 1: “4169D” is the truncated part number.

Line 2: “YYWW” is the last digits of the year and week that the part was assembled.

Line 3: “XXXXX” is the last digits of the lot number.

15.2 TSSOP16 Marking



Line 1: “ZSSC” is the first part of the product family.

Line 2: “4169DE5” is the truncated part number, with special remark on DE5 for TSSOP package.

Line 3: “YYWW” is the last digits of the year and week that the part was assembled.

Line 4: “XXXXX” is the last digits of the lot number.

16. Glossary

Term	Description
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AFE	Analog Front-End
ASIL	Automotive Safety Integrity Level
BOD	Brownout Detection
BR	Bridge Sensor
CIC Filter	Cascaded-Integrator-Comb Filter
CM	Command Mode
CMC	Calibration Microcontroller; optimized microcontroller architecture for Renesas signal conditioners
CMV	Common Mode Voltage
DM	Diagnostic Mode
DNL	Differential Nonlinearity
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FC	Fast Channel; transmitted in SENT frame
FMT	Fault Messaging Time
FS	Full Scale
HBM	Human Body Model
I/O	Input/Output
I2C	Inter-Integrated Circuit; serial two-wire data bus
INL	Integral Nonlinearity
LSB	Least Significant Bit
LSN	Least Significant Nibble
MSB	Most Significant Bit
MSN	Most Significant Nibble
MUX	Multiplexer
MTP	Multiple-Time Programmable
n.a.	Not Applicable
NOM	Normal Operation Mode
NVM	Nonvolatile memory
OTP	One-Time Programmable
OWI	One-Wire Interface
PCB	Printed Circuit Board

Term	Description
PGA	Programmable Gain Amplifier
POR	Power-On Reset
PTAT	Proportional to Absolute Temperature
PWR	Power Management and Protection Unit
QFN	Quad-Flat No-Leads – ZSSC4169 package
RAM	Volatile Memory for Configuration and Conditioning Coefficients
RISC	Reduced Instruction Set Computing
ROM	Read-Only Memory
SCCM	Sensor Check and Common Mode Adjustment Unit
SDM	Serial Data Message; transmitted in the slow channel of SENT protocol
SENT	Single Edge Nibble Transmission; communication protocol for automotive applications defined by SAE International.
SSC	Sensor Short Check—diagnostic task or Sensor Signal Conditioner
TSE	External Temperature Sensor
TSI	Internal Temperature Sensor
TSSOP	Thin Shrink Small Outline – ZSSC4169 package
TQE	Extended Temperature Range Identifier
ZACwire™	Renesas specific one-wire interface

17. Ordering Information

Part Number	Description and Package	MSL Rating	Carrier type	Temperature
ZSSC4169DE1B	Single bridge input, SENT output, internal and/or external temperature measurement, tested wafer	N/A	Wafer Boxes	-40°C to 150°C
ZSSC4169DE1C	Single bridge input, SENT output, internal and/or external temperature measurement, tested die sawn on frame	N/A	Frame Boxes	-40°C to 150°C
ZSSC4169DE1D-ES	Single bridge input, SENT output, internal and/or external temperature measurement, tested die in waffle pack	N/A	Waffle Pack	-40°C to 150°C
ZSSC4169DE4R	Single bridge input, SENT output, internal and/or external temperature measurement, 4 × 4 mm 24-QFN, wettable flanks (NLG24S2)	MSL1	13” Reel	-40°C to 150°C
ZSSC4169DE5R	Single bridge input, SENT output, internal and/or external temperature measurement, 4.4mm x 5.0mm 16-TSSOP with exposed pad (ENG16)	MSL1	13” Reel	-40°C to 150°C
ZSSC4169DE5T	Single bridge input, SENT output, internal and/or external temperature measurement, 4.4mm x 5.0mm 16-TSSOP with exposed pad (ENG16)	MSL1	Tube	-40°C to 150°C
ZSSC4160EVKV1P5	ZSSC4160 SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, 10 Samples.			

Contact Renesas for additional options.

18. Revision History

Revision Date	Description of Change
Apr 28, 2026	▪ Updated QFN-20L package recommendation (see “Pin Assignments”) ▪ Split programming time into 2x parameters (see “Nonvolatile Memory”: DS_068) ▪ Completed other minor changes
June 5, 2025	▪ Parameter FMT corrected and FHTI added ▪ Parameter C_{IN} updated with dependency to R_{BR} ▪ Replace DS_082 with DS_066 (N_{NVM_PAGE})
March 19, 2025	▪ Preliminary removed
January 21, 2025	▪ DS_065: decreased the max limit to 125 ▪ DS_066: Parameter changed
February 3, 2022	▪ Order information updated
December 8, 2020	▪ Description of failure confirmation enhanced ▪ Adding ES to ZSSC4169DE1D order code ▪ Adding references to SAE J2716 APR2016 (Rev. 4) Specification
December 10, 2019	▪ Adding DS_171, DS_172 and DS_173 ▪ Adding 16-TSSOP package specification ▪ Package 24-QFN outline drawing updated from NLG24P5 to NLG24S2 (see revision history of the drawing) ▪ Adding wafer, bare die and waffle pack ordering options ▪ Product name changed from ZSSC4169 to ZSSC4169D-14, according to company standard(order codes not affected) ▪ DS_064, DS_092 and DS_093 corrected ▪ Chapter 6 renamed from “Interface Characteristics and Nonvolatile Memory” to “Interface Characteristics” ▪ Chapter 14 renamed from “Package Outline Drawings” to “Package Drawings” ▪ Adding missing DS_106 number to Table 21
January 19, 2018	▪ Initial release.

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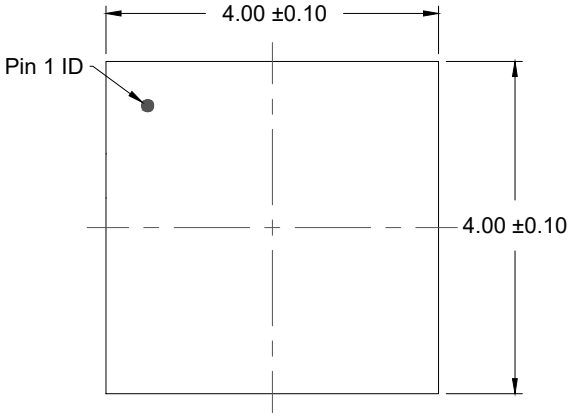
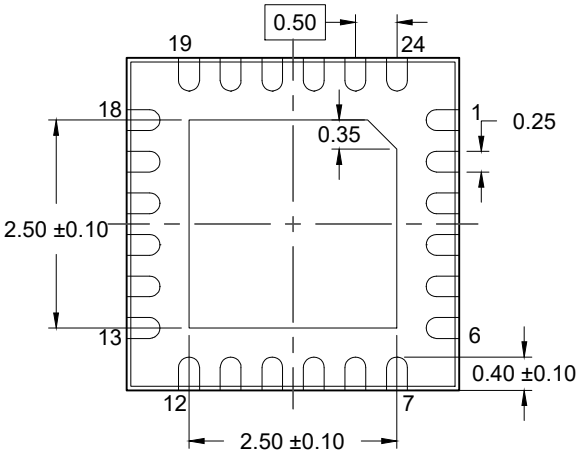
Package Outline Drawing

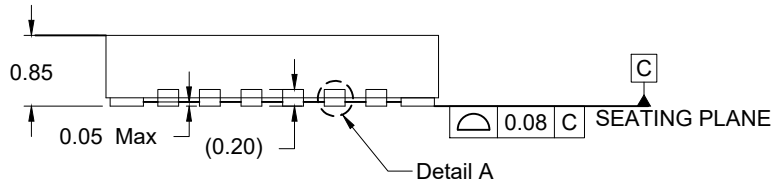
PSC-4192-05
NLG24S2
24-VFQFPN 4.0 x 4.0 x 0.85 mm Body, 0.5mm Pitch
Rev.08, Jun 20, 2025



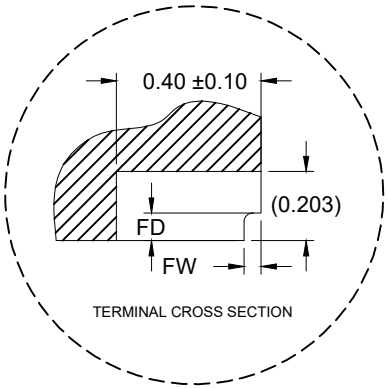
TOP VIEW



BOTTOM VIEW



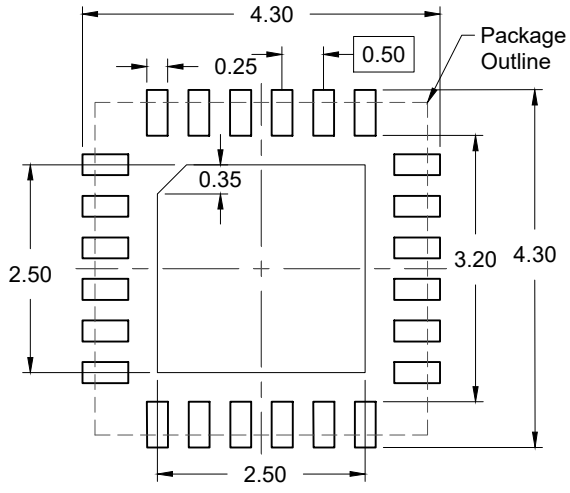
SIDE VIEW



DETAIL A

Table 1: Dimensions of wettable flank (DETAIL A)

Symbol	Unit (mm)	
	MIN	MAX
FD	0.100	-
FW	0.010	0.075



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

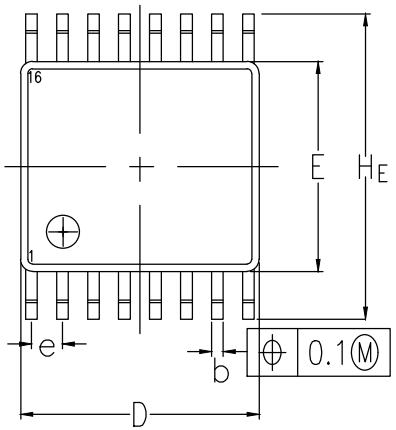
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Wettable flank (step cut).

BASED ON JEDEC JEP95: MO-153

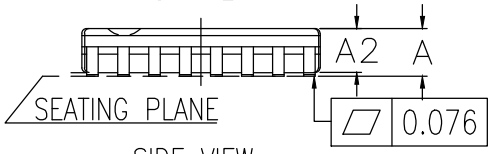
DIMENSIONS IN MILLIMETERS

1. DIMENSIONS

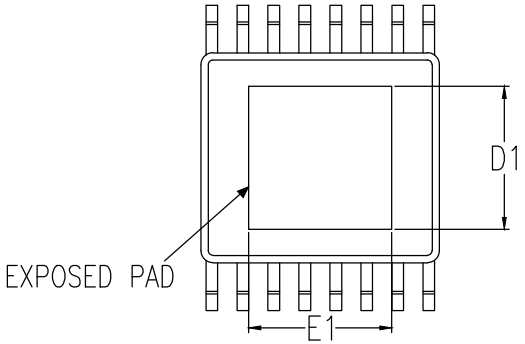
DATE CREATED	REV	REVISIONS DESCRIPTION	AUTHOR
9/20/18	00	Revised from PSC-4749 PGG16	Eddie Lee/CM
6/14/19	01	Correct Title Description	RC/CM
8/29/19	02	EPAD OPTION ADDED	CM
12/10/19	03	EPAD OPTION ADDED	CM
08/13/21	04	EPAD OPTION ON P3 UPDATED	JHTAN
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE			



TOP VIEW

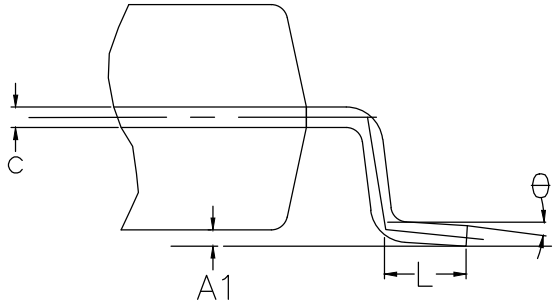


SIDE VIEW



BOTTOM VIEW

VIEW X



DIMENSIONS	min	max
A	0.90	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.20	0.30
c	0.10	0.20
D	4.90	5.10
E	4.30	4.50
D1	REFER TO EPAD OPTION	
E1	REFER TO EPAD OPTION	
e	0.65nom	
H_E	6.20	6.60
L	0.45	0.75
θ	0°	8°

* WITHOUT MOLD FLASH

2. WEIGHT ≤ 0.05 g
3. BODY MATERIAL LOW STRESS EPOXY
4. LEAD MATERIAL Cu-ALLOY
5. LEAD FINISH SOLDER PLATING
6. LEAD FORM Z-BENDS

EPAD OPTIONS:

SYMBOL	P1			P2			P3		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
D1	–	3.00	–	2.50	2.70	2.90	2.55	2.75	2.95
E1	–	3.00	–	2.50	2.70	2.90	3.10	3.30	3.50

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

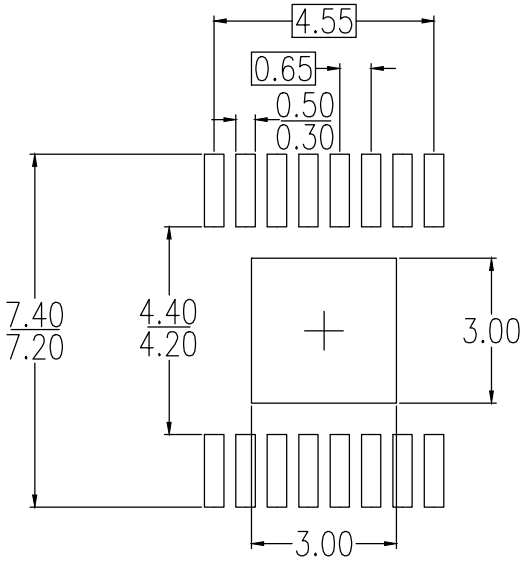
RENESAS
6024 Silver Creek Valley Rd
San Jose, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-3572

TITLE ENG16 Package Outline Drawing
5.0 x 4.4 mm Body,
0.65mm Pitch TSSOP with EPAD

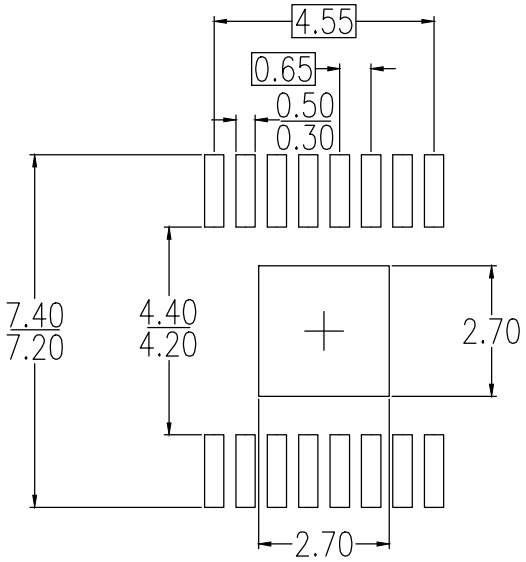
SIZE	DRAWING No.	REV
C	PSC-4761	04

DO NOT SCALE DRAWING

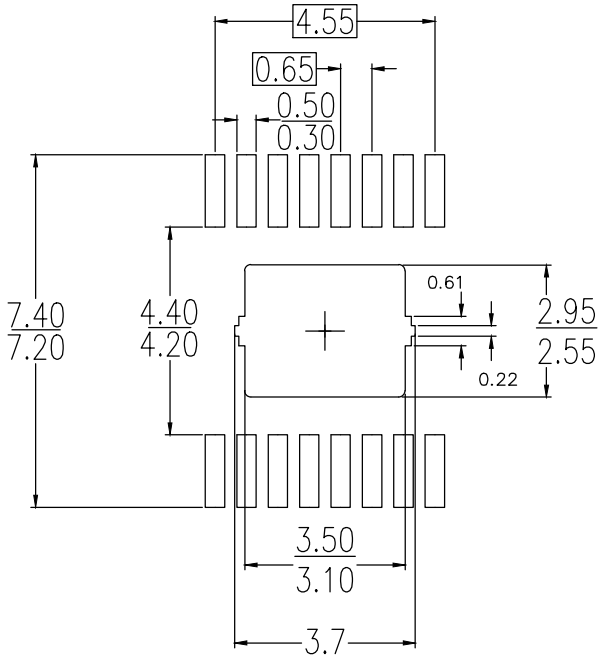
DATE CREATED	REV	REVISIONS DESCRIPTION	AUTHOR
9/20/18	00	Revised from PSC-4749 PGG16	Eddie Lee/CM
6/14/19	01	Correct Title Description	RC/CM
8/29/19	02	EPAD OPTION ADDED	CM
12/10/19	03	EPAD OPTION ADDED	CM
08/13/21	04	EPAD OPTION ON P3 UPDATED	JHTAN
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE			



P1



P2



P3

LAND PATTERN DIMENSIONS

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	RENESAS 6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572
	TITLE ENG16 Package Outline Drawing 5.0 x 4.4 mm Body, 0.65mm Pitch TSSOP with EPAD
	SIZE C | DRAWING No. PSC-4761 | REV 04
	DO NOT SCALE DRAWING | SHEET 2 OF 2