ZSSC4162D-04

Automotive Resistive Sensor Signal Conditioner with SENT Output

Description

The ZSSC4162D-04 is a member of Renesas' family of CMOS integrated circuits for highly accurate amplification and sensor-specific correction of differential bridge sensor element signals. Featuring a maximum analog pre-amplification up to 200, the ZSSC4162D-04 is configurable to nearly all resistive bridges.

Digital compensation of offset, sensitivity, temperature drift, and nonlinearity are accomplished via a 16-bit RISC microcontroller. Calibration coefficients and configuration data are stored in the ZSSC4162D-04 nonvolatile memory (NVM), which is reliable in automotive applications.

The ZSSC4162D-04 supports use of an external PN diode, RTD (PTC) or internal PTAT as a temperature reference. Additionally, NTC sensor can be used as direct temperature output.

Measured values are provided via a digital SENT interface. The SENT interface enables transmission of sensor data via its Fast Channel as well as transmission of supplementary data via its Serial Data Message (SDM) channel (also referred to as the "slow" channel) using only one output pin. End-of-line calibration is also supported through this output pin via the One-Wire Interface (OWI). The ZSSC4162D-04 and the calibration equipment communicate digitally, so the noise sensitivity is greatly reduced. Digital calibration helps keep assembly cost low as no trimming by external devices or lasers is needed.

The ZSSC4162D-04 is optimized for automotive environments by overvoltage and reverse polarity protection circuitry, excellent electromagnetic compatibility, and multiple diagnostic features.

Typical Applications

- Fluid brake pressure sensing (PV)
- Hydraulic pressure sensing
  (for example, steering systems with hydraulic steering support)
- Pneumatic pressure sensing
  (for example, air brake systems, pneumatic shock absorbers)

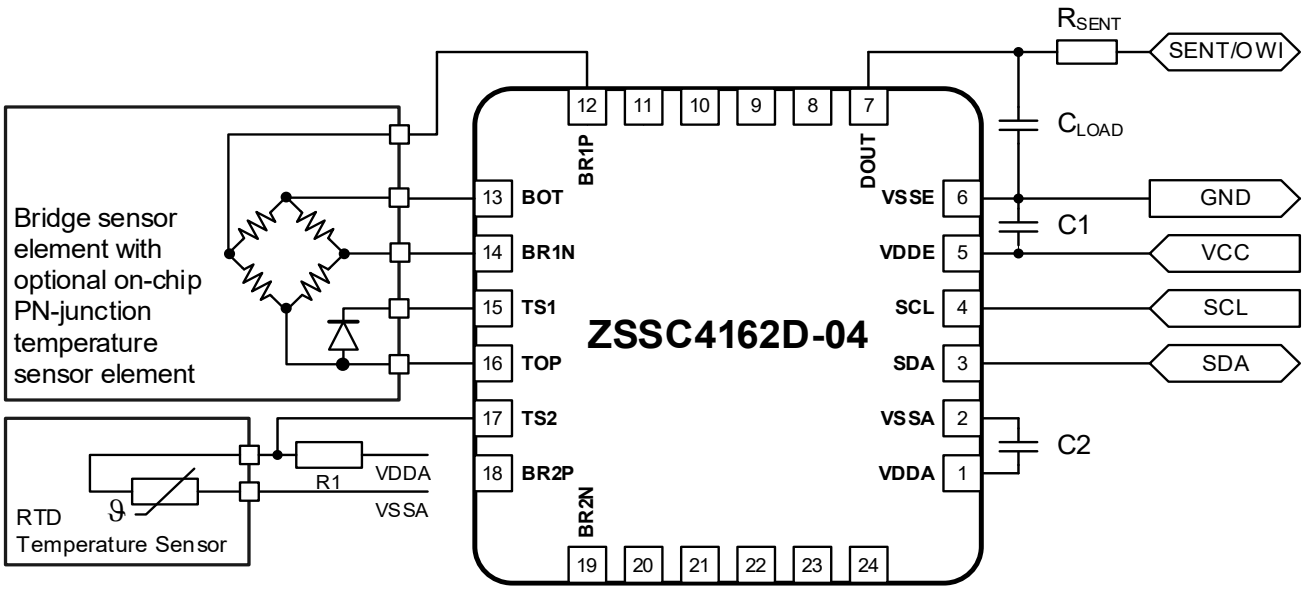
Available Support

- Evaluation kit
- Application notes
- Calculation tools

Features

- Single differential full-bridge sensor element measurement
- Internal chip and/or external temperature measurement (PTC, PN diode) which could be used for bridge temperature compensation.
- NTC measurement for direct SENT output
- Developed in compliance with ISO 26262:2018 ASIL B
- Accuracy as high as ±0.50% full scale in supply voltage range 4.75V to 5.25V and ±1% in range 4.5V to 5.5V
- Outstanding accuracy for NTC: within ±1°C
- AEC-Q100 Grade 0 qualified with operating ambient temperature range from -40°C to 150°C
- Digital compensation for offset, gain, and higher order nonlinearity as well as temperature coefficients of the differential and half-bridge sensor element input signal
- NVM memory for configuration, calibration data, and configurable measurement and conditioning functionality
- Compliant to SENT standard SAE J2716 JAN2010 (SENT Rev. 3) and APR2016 (SENT Rev. 4)
- Supports output of one or more sensor signals and product identification via a single SENT interface connection
- Configurable for nearly all resistive bridge sensors
- One-pass, end-of-line calibration algorithm minimizes production costs
- Over-voltage and reverse polarity protection up to ±18V
- Bridge sensor input span: 1mV/V to 800mV/V
- Bridge sensor signal ADC resolution: 14 to 18 bit
- QFN24 4 × 4 mm package with wettable flanks or bare die

ZSSC4162D-04 Basic Circuit



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1. ZSSC4162D-04 Functional Safety (FuSa) Product Version

The ZSSC4162D-04 product is released for usage in safety related applications supporting ASIL-B.

ASIL-B application use of the ZSSC4162D-04 requires usage of configuration file version v1.0 and a configuration check as described in the *ZSSC4162D-04 Functional Description* document. Note the different order codes for the FuSa version of ZSSC4162D-04 as documented in section 17.

2. Pin Assignments

The ZSSC4162D-04 is available in a 24-QFN (4mm x 4mm; wettable flanks) RoHS-conformant package.

Note: The backside of the 24-QFN package (exposed pad; see section 15) is electrically connected to VSSA.

Recommendation: Solder the QFN exposed pad to the PCB, even if electrically redundant, to ensure adequate thermal performance and to reduce mechanical stress and solder joint failure risk.

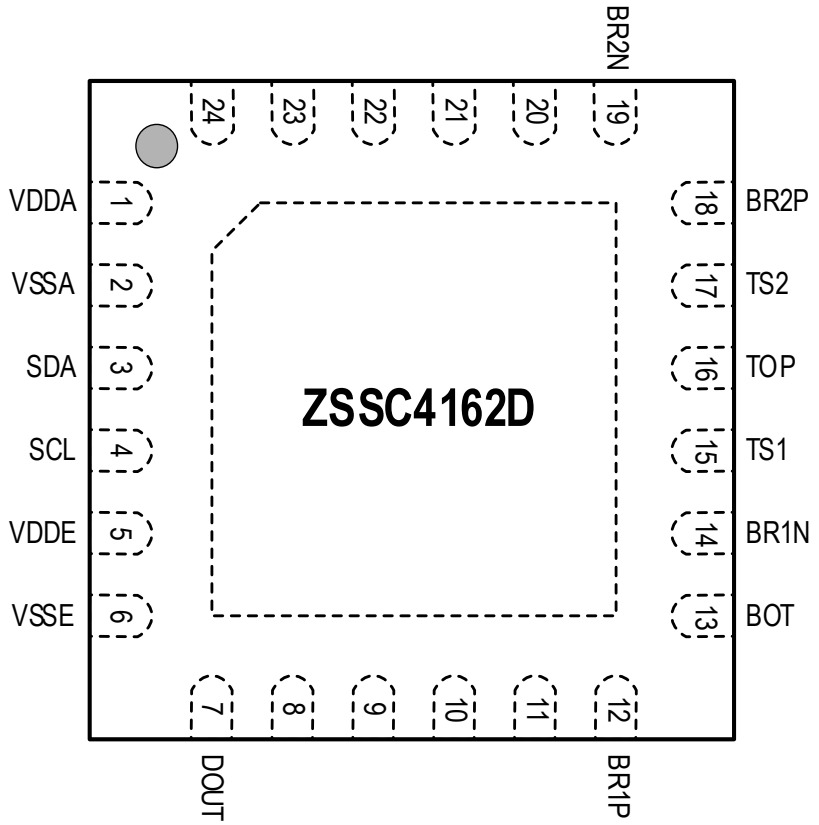


Figure 1. Pin Assignments for QFN24 4x4mm Package – Top View

3. Pin Descriptions

Table 1. Pin Descriptions

24-QFN Pin #	Pin Name	Type	Description
1	VDDA	Supply	Internal supply [1]
2	VSSA	Supply	Internal ground
3	SDA	I/O	I2C data input/output (optional communication interface) [2]
4	SCL	Input	I2C clock (optional communication interface) [2]
5	VDDE	Supply	External supply
6	VSSE	Supply	External ground
7	DOUT	I/O	SENT output and One-Wire Interface (OWI) input/output
8 to 11, 20 to 24	–	–	n.c.
12	BR1P	Input	Positive bridge sensor input
13	BOT	Supply	Negative bridge supply voltage
14	BR1N	Input	Negative bridge sensor input
15	TS1	Input	External temperature sensor input [1]
16	TOP	Supply	Positive bridge supply voltage
17	TS2	Input	External temperature sensor input 2 (optional alternative to TS1)
18, 19	BR2P, BR2N	Input	n.c.
	EPAD	Supply	Internal ground, connected to VSSA [4]

1. Do not supply VDDA externally.
2. Internal pull-up, no connection required.
3. Only one of the two sensor input options can be used: sensor input 1 (BR1P and BR1N).
4. VSSA and EPAD are connected internally; can be shorted externally to VSSA (pin 2) additional.

4. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability. In addition, extended exposure to stresses above the operating conditions given in section 5 might affect device reliability.

See section ■ for information about over-voltage protection, reverse polarity, and short-circuit protection.

Table 2. Absolute Maximum Ratings

Specification	Symbol	Parameter	Conditions	Min	Max	Unit
DS_001	V_{VDDE_ABS}	Supply voltage		-18	18	V
DS_002	V_{DOUT_ABS}	Voltage at the DOUT pin		-18	18	V
DS_003	V_{DIFF_ABS}	Pin voltage difference	Voltage between any two of these pins: VDDE, DOUT, and VSSE	-18	18	V
DS_004	V_{VDDA_ABS}	Analog supply voltage	On-chip controlled voltage; do not supply VDDA externally	-0.3	6	V
DS_005	V_{PIN_ABS}	Voltage at all other pins	Maximum voltage is V_{VDDA} + 0.3V	-0.3	6	V
DS_006	T_{J_ABS}	Junction temperature	Note: See section 8.2.4 regarding over-voltage protection	-40	160	°C
DS_007	T_{STOR_ABS}	Storage temperature		-55	155	°C

5. Operating Conditions

The operating conditions below specify the conditions that the application circuit must provide to the device during operation for proper function. Unless otherwise stated, the parameter limits in this section are applied as test conditions for the electrical parameters specified in section 6.

Table 3. Operating Conditions

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DS_009	V_{VDDE}	Supply voltage	VDDE to VSSE	4.75	5	5.25	V
DS_010	V_{VDDE_EXTD}	Extended supply voltage[1]	VDDE to VSSE; derated accuracy as specified with DS_059	4.5	5	5.5	V
DS_011	V_{VDDE_OP}	Operating supply voltage[1]	VDDE to VSSE; derated accuracy Note for a supply greater than 5.5V: above the ZSSC4162D-04 over-voltage limitation threshold, the output potential is clipped at this threshold.	4		6	V
DS_012	T_{AMB}	Ambient temperature [2, 3]	Temperature range	-40		150	°C
Informational 4	$R_{th\_JA\_QFN24}$	Thermal resistance QFN24[1]	According to JESD 51		32		K/W
DS_185	R_{BR}	Bridge sensor resistance[1, 5]	One sensor bridge at pins BR1P and BR1N	1		15	kΩ

1. No measurement in mass production; parameter is guaranteed by design and/or quality observation.
2. Temperature stress over lifetime is restricted to the Temperature Profile described in section 14 or to similar stress caused by equivalent temperature profiles. Contact Renesas for temperature stress calculation support.
3. Assuming application conditions according to test board design as per JESD51-7 and natural convection test conditions as per JESD51-2.
4. Package-related parameter.
5. Symmetric behavior and identical electrical properties (especially the low-pass characteristic) of the differential bridge sensor inputs are required. Unsymmetrical conditions of the sensor and/or external components connected to the sensor input pins can generate a failure in signal operation.

6. Electrical Characteristics

All parameter values are valid under the operating conditions specified in section 5 (unless otherwise stated). All parameters are valid for the ambient temperature range T_{AMB} and for the supply voltage range as specified (4.5-5.5V or 4.75-5.25V) as provided at the VDDE to VSSE pin. Unless otherwise defined, the parameters are related to the ZSSC4162D-04 itself. All voltages are referenced to VSSA pin.

The following parameters are specified based on a ZSSC4162D-04 main channel configuration setup using a PGA gain of 100 and assuming a resulting ADC input range usage of ≥25%FS. Further preconditions are an ADC resolution of 14 bits, an oscillator frequency of 8MHz (calibrated by Renesas in production), and an ADC clock frequency of 1MHz (1st step) / 2MHz (2nd step).

Table 4. Electrical Parameters

Note: See important table notes at the end of this table.

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Current and System Operating Conditions							
DS_015	I_S	Supply current	Excluding sensor supply current and excluding output current at DOUT pin; oscillator factory-adjusted to f_{OSC} = 8MHz.		8	10	mA
DS_016	P_{OV}	Over-voltage power consumption [1]	5.5V < V_{VDDE} < 18V; excluding sensor and output load.			300	mW
DS_017	$V_{OV\_LIM\_TH}$	Over-voltage limitation threshold [1]	V_{VDDA} is limited if V_{VDDE} exceeds the threshold of $V_{OV\_LIM\_TH}$.	5.4		6	V
DS_018	$V_{OV\_OFF\_TH}$	Over-voltage switch-off threshold [1]	The ZSSC4162D-04 is set to the reset state with limited current consumption if V_{VDDE} exceeds the threshold of $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$.	7		12	V
DS_019	$t_{OV\_OFF\_DLY}$	Over-voltage switch-off delay [1]	The ZSSC4162D-04 is set to the reset state with limited current consumption if V_{VDDE} exceeds the threshold of $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$.		10	25	ms
DS_020	$I_{S\_OV\_OFF}$	Supply current limitation in the event of over-voltage switch-off [1]	Over-voltage switch-off is activated if the supply voltage exceeds $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$. V_{VDDE} < 18V; excluding sensor and output load.			10	mA
DS_021	V_{SENS}	Bridge sensor supply voltage	$V_{SENS} = V_{TOP} - V_{BOT}$ at $R_{BR} \geq 1k\Omega$ where V_{TOP} is the voltage at the TOP pin and V_{BOT} is the voltage at BOT pin.	0.9		1	V_{VDDA}
DS_022	V_{POR_OFF}	Power-on reset off-threshold	V_{VDDA} measured referenced to VSSA; POR is active until V_{VDDA} exceeds this threshold.	3.3		3.8	V
DS_023	V_{POR_ON}	Power-on reset on-threshold	V_{VDDA} measured referenced to VSSA; POR is activated if V_{VDDA} falls below V_{POR_ON}	3.0		3.6	V
DS_024	V_{POR_HYST}	Power-on reset hysteresis [1]	$V_{POR\_ON} - V_{POR\_OFF}$		0.4		V
DS_025	f_{OSC}	Oscillator frequency	Factory-calibrated oscillator frequency.	7.6	8	8.6	MHz
DS_026	TC_{OSC}	Oscillator frequency temperature coefficient [1]		-200		200	ppm/K
Analog Front-End Characteristics							
DS_027	V_{IN_SPAN}	Differential input span	Analog gain: 1, 138 and 200 are not released for ASIL application	1		800	mV/V
			Analog gain: 2 to 100, released for ASIL application	2.5		400	mV/V
DS_028	$V_{IN\_RNG\_1}$	Input voltage range	Analog gain = 1; corresponds to V_{ADC_IN}, not released for ASIL application	0.05		0.95	V_{SENS}
DS_029	$V_{IN\_RNG\_2}$		Analog gain = 2 to 200	0.3		0.65	V_{SENS}
DS_030	C_{IN}	Capacitance at input [1]	BR1P/BR1N or BR2P/BR2N to VSSA; requirement for timing parameters.	0		12	nF

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
A/D Conversion Refer to section 8.2.4.							
DS_032	r_{ADC}	ADC resolution [1]		14		18	Bit
DS_033	V_{ADC_IN}	ADC input range [1]	Differential input signal range depending on analog gain a_{PGA} and ADC range shift rs_{ADC}: $V_{ADC\_IN} = V_{IN} \times a_{PGA} + rs_{ADC} \times V_{SENS}$	0.05		0.95	V_{SENS}
			Restriction for analog gain ≥100.	0.1		0.9	V_{SENS}
DS_034	DNL_{ADC}	DNL [1]				0.95	LSB
DS_035	INL_{ADC}	INL	Best fit.		3	8	LSB_{14}
Temperature Measurement Refer to section 8.3.2; external temperature sensor (TSE) connected to the TS1 or TS2 pin.							
Informational 2	OPR_{TS}	Temperature sensor range[1]	Important: This range exceeds the operating conditions for T_{AMB}.	-60		200	°C
DS_036	ST_{TSI}	Internal temperature PTAT sensitivity	Raw values, without conditioning calculation; analog gain = 12.6	20			LSB_{14} /K
DS_037	A_{TSE_D}	External temperature diode channel gain		10			LSB_{14}/mV
DS_038	I_{TSE_D}	External temperature diode bias current		10	20	55	µA
DS_039	V_{TSE_D}	External temperature diode input range [1]	Related to V_{TOP}, absolute value	-1		-0.2	V
DS_069	V_{TSE_RTD}	External temperature RTD input range	TS1/2 input voltage range (relative to VREF=VDDA-VSSA, or VREF=VTOP-VBOT)	0.3		0.65	V_{REF}
DS_070	RTD_{ADC_OUT}	RTD ADC Output Range	The allowed operational ADC input range	5.0		95	%
DS_071	F_{TSE_RTD}	External temperature RTD accuracy	The remaining measurement error, relative to the adjusted PgaGainSel when using Mode=RTD	-1		1	%FS
DS_072	V_{RTD_IN}	RTD Input Voltage Range	Allowed input voltage at TS1/TS2 pin	0.02		0.98	VDDA
DS_073	F_{NTC_MEAS}	NTC Measurement Error	Remaining measurement error	-0.15		0.15	%FS
VDDE/VDDA Measurement							
DS_041	err_{VDDE}	Un-calibrated V_{VDDE} measurement error	V_{VDDE_OP}	-125		125	mV
DS_042	err_{VDDA}	Un-calibrated V_{VDDA} measurement error	Valid for VDDAUV, V_{VDDE_OP} up to 5V	-180		180	mV
Sensor Diagnostic Tasks							
DS_043.1	R_{BRSC_TH25}	Sensor connection loss detection threshold for 25µA sense current I_{probe}	Fault check BRSC: Sensor to SSC pin connection; without capacitive load at input pins in the event of a connection loss	8.8		277	kΩ
DS_043.2	R_{BRSC_TH100}	Sensor connection loss detection threshold for 100µA sense current I_{probe}		1.5		63	kΩ
DS_044	R_{BRSS_TH}	Sensor short detection threshold[1]	Fault check BRSS - BR1N to BR1P	100		1750	Ω

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DS_046	DTI	Diagnostic testing interval[1]			8	10	ms
DS_047	FMT	Fault messaging time [1]	t_{TICK} = 3µs, fault confirmation is enabled; SENT frame length 846µs (pause enabled); Remark: contains SENT transmission			26	ms
			With disabled fault confirmation			22	ms
DS_047.1	FHTI	Fault handling tolerance interval	Fault confirmation is enabled			29	ms
			Fault confirmation is disabled			21	ms
SENT Output Refer to SAE J2716 Specification JAN2010 (Rev.3) and APR2016 (Rev. 4) for detailed specifications for SENT Physical and Software Layer.							
DS_048	t_{TICK}	Tick time [1]	Adjustment step =1µs.	3		90	µs
DS_049	t_{TICK_JITTER}	Tick time jitter [1, 3]	Valid for tick time ≤10µs, 6-sigma value.			300	ns
DS_050	n_{SDM}	Number of SDMs	Absolute count of different messages.	2		32	
DS_051	n_{SDM_CYC}	Number of SDM in SDM cycle	Message count in SDM cycle, including use of different priority levels.	0		64	
DS_052	n_{SDM_PRIO}	SDM transmission priority levels		1		3	
DS_053	t_{PAUSE}	Pause length	Fixed frame length.	12		768	t_{TICK}
DS_054	t_{FRAME}	Frame length	Pause pulse disabled, 6 data nibbles, and variable frame length.	154		270	t_{TICK}
			Pause pulse enabled, 6 data nibbles, and fixed frame length.	282		922	t_{TICK}
System Response							
DS_055	$t_{STARTUP}$	Startup time [1]	Time to first valid output after power-on; $V_{VDDE} > V_{POR\_OFF}$; f_{OSC} = 8MHz. [4]			10	ms
DS_056	OUR	Output update rate [1]	ZSSC4162D-04 internal output update, asynchronous to SENT transmission.			1	ms
DS_057	ORT	Output response time [1]	100% input step. [4]			3.5	ms
DS_058	RE	Ratiometricity error	Maximum error for V_{VDDE} from 5V to 4.75V or to 5.25V. Ratiometricity error is already contained in overall failure (DS_059).			500	ppm
DS_059	F_{ALL_BR}	Overall failure Deviation from ideal line including INL, gain, offset, and temperature impacts; excluding sensor-caused effects	Differential sensor readout V_{VDDE} = 4.75V to 5.25V.			0.5	%FS
	$F_{ALL\_BR\_EXTD}$[1]		Differential sensor readout V_{VDDE_EXTD} = 4.5V to 5.5V.			1.0	%FS
	$F_{ALL\_DERATED}$[1]		In the operating supply voltage range V_{VDDE_OP}.			5	%FS

1. No measurement in mass production; parameter is guaranteed by design and/or quality observation.
2. The temperature sensor range is the calibration target for the SENT output of the SDM temperature channels. This target can be adjusted.
3. Compliant to SAE J2716 JAN2010 (SENT Rev. 3) and APR2016 (SENT Rev. 4) specifies maximum jitter of 50ns at tick time = 3µs and maximum jitter of 250ns at tick time = 10µs.
4. t_{TICK} = 3µs, SENT pause pulse enabled, and the SENT frame length is set to the minimum.

7. Interface Characteristics and Nonvolatile Memory

Table 5. Interface Characteristics and Nonvolatile Memory

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ZACwire™ One-Wire Interface							
One-wire communication at the DOUT pin.							
DS_060	t_{PWRUP}	Power-on time [1]	$V_{VDDE} > V_{POR\_OFF}$; f_{OSC} = 8MHz.			3.0	ms
DS_061	$t_{OWI\_STARTWIN}$	Start window [1]	$V_{VDDE} > V_{POR\_OFF}$; f_{OSC} = 8MHz.		250		ms
DS_062	$V_{OWI\_IN\_H}$	OWI voltage level HIGH [1]	Master to slave.	0.80			V_{VDDE}
DS_063	$V_{OWI\_IN\_L}$	OWI voltage level LOW [1]	Master to slave.			0.20	V_{VDDE}
DS_064	$V_{OWI\_OUT\_L}$	Slave output level LOW	Open drain; I_{OL} < 2mA.			0.1	V_{VDDE}
Selected I2C Interface Parameters							
The I2C interface complies with the I2C Bus Specification, Version 6.0, April 4, 2014.							
Informational	f_{SCL}	SCL clock frequency		0		400	kHz
Informational	$V_{I2C\_IN\_IL}$	Input low level voltage		-0.5	-	0.15 V_{DDA} [3]	V
Informational	$V_{I2C\_IN\_IH}$	Input high level voltage		0.7 V_{DDA}	-	V_{DDA}+0.5V	V
Informational	V_{OL}	Output low level voltage	(Open-drain or open-collector) at 3mA sink current; V_{DDE} = 5V.	0	-	0.4	V
Informational	R_{I2C}	Internal pull-up resistor		25		100	kΩ
Nonvolatile Memory (NVM)							
DS_065	T_{AMB_NVM}	Ambient temperature for NVM programming [2]		-40		125	°C
DS_066	N_{NVM_PAGE}	NVM page count[1]	Pages available for writing	22			
DS_067	t_{NVM_RET}	Data retention [1]	Temperature profile. [4]	15			years
DS_068.1	$t_{NVM\_WRI\_DIFF}$	Programming time without soaking [1]	Per programmed data word in differential mode.			1.7	ms
DS_068.2	$t_{NVM\_WRI\_RED}$		Per programmed data word in redundant mode.			3.3	

1. No measurement in volume production; parameter is guaranteed by design and/or quality observation.
2. Take into consideration additional package and temperature range restrictions.
3. Different from the referenced I2C bus specification.
4. Over lifetime and valid for the dice. Note that the package can cause additional restrictions.

8. Circuit Description

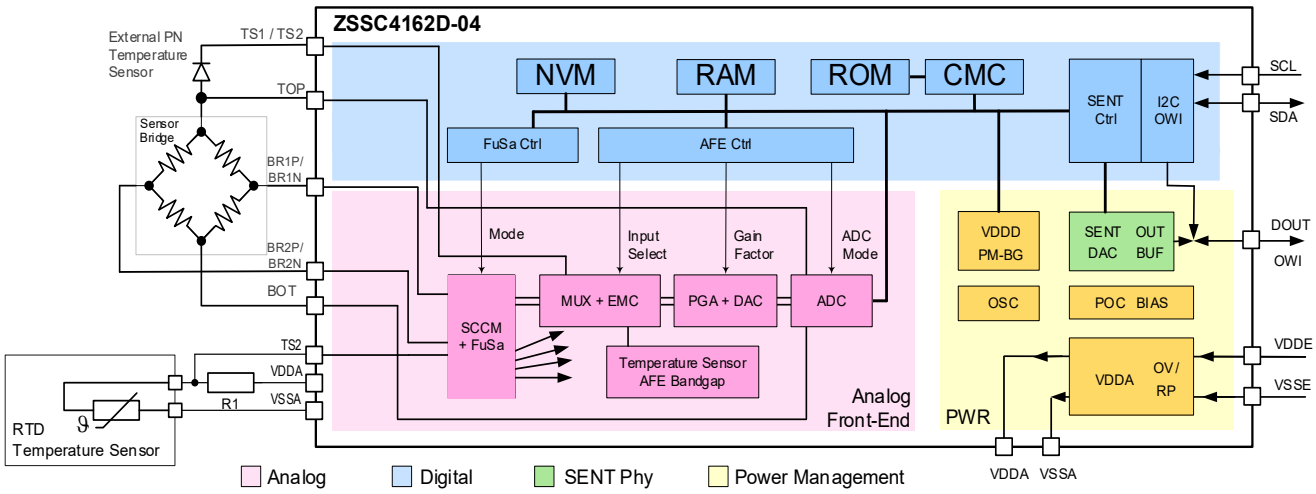
8.1 General Operation Description

The ZSSC4162D-04 is a sensor signal conditioner for readout of resistive bridge sensors by the following steps:

1. The sensor signal is pre-amplified and converted to a digital signal by the analog-to-digital-converter (ADC).
2. The digital conversion result is offset compensated, and gain adjusted.
   Temperature coefficients and nonlinearity of the sensing element are compensated, if necessary.
3. The calculated conditioning result is output using the SENT protocol.

Signal conditioning processes the following tasks:

- Measurement of the voltage signal of the connected resistive bridge sensor sensing element
- Auxiliary measurements of internal and/or external temperature sensors as connected
- Auxiliary measurements for application, environmental and self-supervision
- Conditioning calculation for the sensor signal
- SENT output of the conditioning result



SCCM+FuSa	Sensor Check and Common Mode Adjustment Unit, FuSa Supervision Hardware	NVM	Nonvolatile Memory for Configuration and Conditioning Coefficients
MUX+EMC	Multiplexer and EMC input filter	RAM	Volatile Memory for Configuration and Conditioning Coefficients
PGA+DAC	Programmable Gain Amplifier and AFE BIST DAC	SENT* OUTBUF	SENT Controller and SENT Physical Layer Pulse Shaping Unit and Output Stage
Temperature Sensor, AFE Bandgap	Internal PTAT Temperature Sensor and Analog Front End Bandgap Reference	FuSa- & AFE Ctrl	Functional Safety Hardware & Analog Front End Configuration and Control Logic
ADC	Analog-to-Digital Converter	I2C/OWI	Serial I2C and One-Wire Interface
CMC	Calibration Microcontroller	OSC, POC BIAS	Clock frequency oscillator, Power-On-Clear circuit, BIAS Current Generator
ROM	Read-Only Memory for Correction Formula and Algorithm	VDDA OV/RP	Power Management and Over Voltage / Reverse Polarity Protection Unit as well as VDDA Regulator

Figure 2. Block Diagram

8.2 Analog Front-End

The analog front-end (AFE) consists of the sensor connection check module (SCCM+FuSa), the multiplexer (MUX+EMC), the programmable gain amplifier including the BIST DAC (PGA+DAC), and the analog-to-digital converter (ADC). The internal offset of the analog front-end is eliminated by an auto-zero compensation. An internal PTAT is used to measure the junction temperature and a bandgap reference provides necessary reference voltage (Temperature Sensor, AFE Bandgap).

8.2.1. SCCM and Functional Safety

The sensor check and common mode block (SCCM) implements the bridge sensor related supervision: connection and short check. Further functional safety hardware is used to supervise the operation of the whole IC as well as the analog front-end itself.

8.2.2. Input Multiplexer

The input multiplexer (MUX) selects one of the various inputs and connects it to the signal path allowing the use of a single ADC. It allows a very flexible signal routing between the sensors and the ZSSC4162D-04.

8.2.3. Programmable Gain Amplifier

The sensor signal can be amplified by the on-chip programmable amplifier (PGA) using a gain between 2 and 200. Alternatively, the PGA can be bypassed and the sensor signal can be input directly to the ADC. The gain is adjustable for the bridge measurement task in order to provide an ADC input signal span of greater than 50% FS. An additional DAC is used as sensor replacement for PGA+ADC build in self test.

Table 6 shows the adjustable gains of the PGA, the corresponding signal spans, and the common mode range limits.

Table 6. Adjustable PGA Gains and Resulting Sensor Signal Spans and Common Mode Ranges

Nominal PGA Gain aPGA	Maximum Input Span V_{IN_SPAN} [mV/V]	Input Common Mode Range V_{IN_CM} [% V_{VDDA}]
1 (PGA bypassed): applicable, but not released for FuSa application!	800	5 to 95
2.08	385	30 to 65
3.15	254	30 to 65
4.31	186	30 to 65
6.25	128	30 to 65
8.31	96	30 to 65
12.6	63	30 to 65
17.3	46	30 to 65
25.0	32	30 to 65
33.2	24	30 to 65
50.4	16	30 to 65
69.0	12	30 to 65
100.0	8	30 to 65
138.0	6	30 to 65
200.0	4	30 to 65

Recommendation: To achieve the best stability and linearity performance of the AFE, operate the PGA in a differential output voltage range within 10% to 90% of the ratiometric reference voltage $V_{REF} = V_{SENS} = (V_{TOP} – V_{BOT})$. The gain must be selected to guarantee this constraint for the entire operating temperature range of the application and for the specified sensor bridge tolerances.

8.2.4. Analog-to-Digital Converter

The analog-to-digital converter (ADC) is implemented using the full differential switched capacitor technique. The conversion is largely insensitive to short-term and long-term instabilities of the clock frequency. The ADC allows adjusting the A/D conversion input voltage range shift.

8.3 Signal Conditioning

8.3.1. Internal Temperature Sensor Signal Conditioning

The internal temperature sensor signal conditioning is processed every time that a new measurement result value is available from the analog-to-digital conversion. The conditioning calculation described in the *ZSSC4162D-04 Functional Description* document provides compensation of offset and gain and of the nonlinearity.

The conditioning coefficients are stored as signed 16-bit values (sint16, two's complement) in the NVM during the calibration process. The weights are unsigned 4-bit values (uint4).

The normalized conditioning result of the internal temperature sensor is stored as a signed 16-bit value (sint16, two's complement) in the RAM Output Memory. This value can be assigned to a SENT SDM output channel and can be selected for the conditioning calculation of the full-bridge sensor signal.

8.3.2. External Temperature Sensor Signal Conditioning

The external temperature sensor signal conditioning is processed every time that a new measurement result value is available from the analog-to-digital conversion. The conditioning calculation described in section the *ZSSC4162D-04 Functional Description* document provides compensation of offset and gain and of the nonlinearity.

The conditioning coefficients are stored as signed 16-bit values (sint16, two's complement) in the NVM during the calibration process. The weights are unsigned 4-bit values (uint4).

The normalized conditioning result of the external temperature sensor is stored as a signed 16-bit value (sint16, two's complement) in the RAM Output Memory. This value can be assigned to a SENT SDM output channel and can be selected for the conditioning calculation of the full bridge sensor signal.

The first path provides a polynomial conditioning which is intended for PTC sensors. The transfer function of the conditioning output with input from the measurement is as follows:

$$Output = 2^{w_2-40}c_2 * Input^2 + 2^{w_1-25}c_1 * Input^1 + 2^{w_0-9}c_0 \quad (1)$$

The second path is a spline function that is optimized for NTC sensors. The calibrated default NTC characteristic is given in Table 7. The coefficients must be calculated for every NTC – RTD once. It can be selected which conditioning result of both paths is stored as a signed 16-bit value (sint16, two's complement) in the RAM Output Memory. This value can be assigned to a SENT FC or SDM output.

$$Input = Z \qquad Z \in \left[0; 2^{15}\right) \quad (2)$$

$$x = (ld(Input) - ld\left(2^{15} - \text{Input}\right)) * 2^{11} \qquad Input \in \left[1; 2^{15}\right] \quad (3)$$

3rd order spline:

$$s_{j(x)} = \underbrace{2^{-56} * 2^{w_{j3}} * c_{j3} * x^3 + 2^{-41} * 2^{w_{j2}} * c_{j2} * x^2 + 2^{-25} * 2^{w_{j1}} * c_{j1} * x + 2^{-9} * 2^{w_{j0}} * c_{j0}}_{\text{SPLINEWGTN Spline}} \qquad s_{j(x)} \in \left[-2^{15}; 2^{15}\right) \quad (4)$$

$$Output = \frac{s_{j(x)} + offset}{2} * \frac{2^{15}}{gain} \qquad Output \in \left[-2^{15}; 2^{15}\right) \quad (5)$$

j (Spline Segment)	*x* (Polynomial Input Range)	Spline Segment Boarder Recommendation
0	$x < x_0$	$x_0 = Z(80°C)$ $x_1 = Z(0°C)$
1	$x_0 \leq x < x_1$	
2	$x \geq x_1$	

Table 7. NTC Mathematic Coefficients

Calibration Coefficient Name	Range	Formulaic Character	Description
CoeffCal4Offset	$[-2^{15}; 2^{15})$	*offset*	Supports 1 or 2 point calibration in production.
CoeffCal4Gain	$[-2^{15}; 2^{15})$	*gain*	
CoeffCal4Spline1	[0; 15]	W_{03}; W_{02}; W_{01}; W_{00}	Spline coefficients and weights. Calculated for an external resistor network and NTC characteristic.
CoeffCal4Spline2	$[-2^{15}; 2^{15})$	C_{03}	
CoeffCal4Spline3	$[-2^{15}; 2^{15})$	C_{02}	
CoeffCal4Spline4	$[-2^{15}; 2^{15})$	C_{01}	
CoeffCal4Spline5	$[-2^{15}; 2^{15})$	C_{00}	
CoeffCal4Spline6	$[0; 2^{15})$	x_0	
CoeffCal4Spline7	[0; 15]	W_{13}; W_{12}; W_{11}; W_{10}	
CoeffCal4Spline8	$[-2^{15}; 2^{15})$	C_{13}	
CoeffCal4Spline9	$[-2^{15}; 2^{15})$	C_{12}	
CoeffCal4Spline10	$[-2^{15}; 2^{15})$	C_{11}	
CoeffCal4Spline11	$[-2^{15}; 2^{15})$	C_{10}	
CoeffCal4Spline12	$[0; 2^{15})$	x_1	
CoeffCal4Spline13	[0; 15]	W_{23}; W_{22}; W_{21}; W_{20}	
CoeffCal4Spline14	$[-2^{15}; 2^{15})$	C_{23}	
CoeffCal4Spline15	$[-2^{15}; 2^{15})$	C_{22}	
CoeffCal4Spline16	$[-2^{15}; 2^{15})$	C_{21}	
CoeffCal4Spline17	$[-2^{15}; 2^{15})$	C_{20}	

8.3.3. Full Bridge Sensor Signal Conditioning

The full-bridge sensor signal conditioning is processed every time that a new measurement result value is available from the analog-to-digital conversion. The conditioning calculation described in the *ZSSC4162D-04 Functional Description* document provides compensation of the temperature dependent offset and gain and of the nonlinearity.

The conditioning coefficients are stored as signed 16-bit values (sint16, two's complement) in the NVM during the calibration process. The weights are unsigned 4-bit values (uint4).

All intermediate results and the final conditioning results for the full-bridge sensor are stored as signed 16-bit values (sint16, two's complement) in the RAM Output Memory. These values can be low-pass filtered and can be assigned to SENT Fast output channels.

8.3.4. Conditioning Cycle

The conditioning cycle is the sequence of equations and supervision functions processed during the Normal Operation Mode (NOM). It uses raw measurement results from the measurement cycle and delivers conditioned data for output.

8.3.5. Digital Interface

The ZSSC4162D-04 provides a digital interface for the calibration. The I2C controller and physical layer for I2C transmission complies with the *I2C Bus Specification, Rev.6 – April 4, 2014* document.

The ZSSC4162D-04 supports the following bus selection.

Bidirectional bus options:

- Standard-mode (Sm), supporting a bit rate up to 100kbit/s
- Fast-mode (Fm), supporting a bit rate up to 400kbit/s

8.3.6. Timing Definitions

The timing for the update of the SENT output and for the fault messaging is defined in Figure 3. The relevant timing parameters are listed in Table 8.

Table 8. Timing Parameter

Symbol	Parameter	Description
OUR	Output update rate	Internal update rate of the main signal data
ORT	Output response time	Latency from the main signal event to the completion of the SENT transmission of this signal event

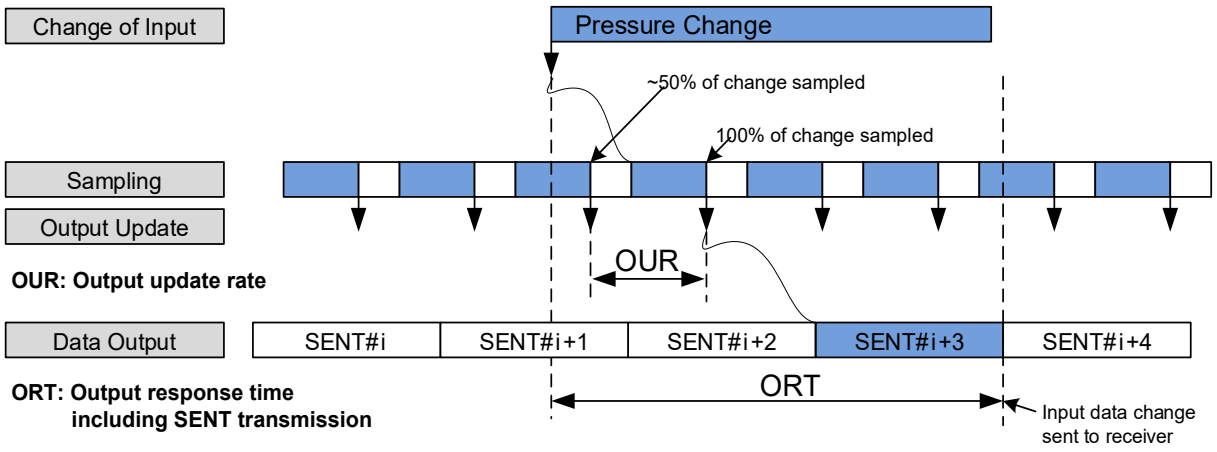


Figure 3. Output Update Timing Diagram

8.3.7. NVM OEM Data Memory

The ZSSC4162D-04 provides an NVM memory area for the storage of OEM data, which is physically part of the one-time programmable (OTP) NVM memory module, but it is delimited from the configuration and calibration data by dedicated commands for READ and WRITE access. The OEM must implement data protection and multiple-time programming data management.

Table 9. Requirements – NVM OEM Data Memory

Requirement	Parameter	Value	Unit
DS_081	NVM OEM data memory (OTP)	8	16-bit words
DS_082	Multi-time programming (MTP) provided by additional memory area	16	16-bit words

8.4 Signal Path

The ZSSC4162D-04ZSSC4162D-04 signal path consists of the analog front-end (AFE), the digital signal processing unit, the SENT controller, and the SENT interface (SENT PHY). In addition, this is supported by a serial digital one-wire interface (ZACwire™).

Table 10. Requirements – Main Signal Path Polarity

Specification	Parameter	Description
DP_040	Main Signal Path Polarity	The resistive bridge sensor element signal is input via the BR1P and BR1N or BR2P and BR2N pins and is handled as a fully differential signal. Both signal lines have a dynamic range symmetrical to the common mode potential (analog ground; equal to $V_{VDDA}/2$) so that it is possible to process positive and negative differential input signals. These differential signals are pre-amplified by the programmable gain amplifier (PGA) and are converted to digital values by the A/D converter (ADC).

A multiplexer (MUX) selects and transmits the signals from either the bridge sensor or the selected temperature sensor to the analog-to-digital converter (ADC) in a defined sequence. The temperature sensors can either be an external PN diode, RTD (PTC/NTC) or an internal proportional-to-absolute-temperature (PTAT) source selected by NVM configuration. Note that the NTC sensor can only be used for direct SENT output and not for bridge temperature compensation.

The digital signal correction is processed in the calibration microcontroller (CMC) using ROM-resident correction formulas and sensor-specific coefficients stored in the NVM. The configuration data and the conditioning coefficients are programmed into the NVM during the calibration process by digital one-wire communication via the DOUT pin.

During the calibration process, raw measurement values can be requested via the digital interfaces.

The ZSSC4162D-04 provides SENT transmission according to the SAE J2716 SENT Specification. Depending on the selected settings, there are several SENT output modes. These modes include assignment of the various sensor signals to the SENT Fast and Serial Data Message (SDM) communication channels as well as the configuration of the SENT frame itself.

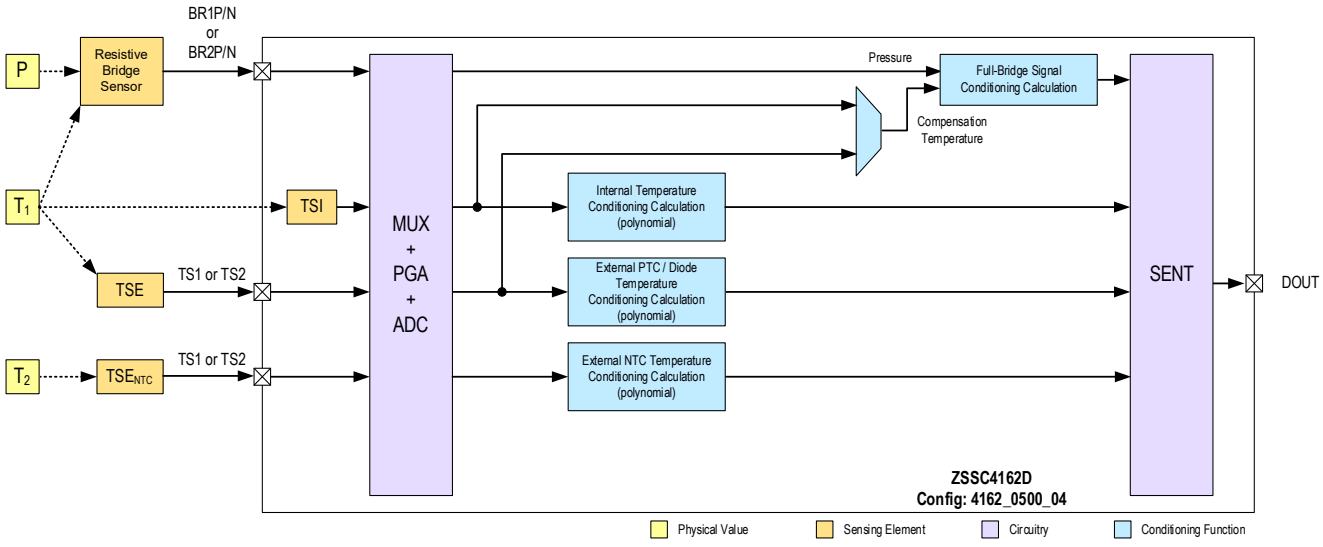


Figure 4. Main Signal Path (Example P/t Sensor)

8.4.1. Full-Bridge Sensor Measurement

The ZSSC4162D-04 measures a differential sensor signal (BR1P to BR1N or BR2P to BR2N); i.e., a bridge or voltage source type signal. The signal path is ratiometric and fully differential. The ratiometric reference voltage V_{REF} is equal to (V_{TOP} – V_{BOT}).

The user can select the following parameter settings:

- Gain: 2.1 to 200
- Range Shift: 1/16, 1/8, 1/4, or 1/2
- Input Multiplexer: BR1P/BR1N, BR1N/BR1P, BR2P/BR2N, or BR2N/BR2P
- Measurement resolution: 14 bits, 15 bits, 16 bits, 17 bits, or 18 bits

8.4.2. Internal Temperature Measurement

The ZSSC4162D-04 supports temperature measurement by a chip-internal PTAT sensor.

8.4.3. External Temperature Measurement

A ratiometric measurement is implemented using VDDA and VSSA as the internal reference voltage. For every measurement result, an automatic offset compensation is performed.

In the case of an NTC sensor, it is recommended to use the value of R25 as the pull-up resistor. The temperature measurement error must be calculated from the sum of the failures F_{NTC_MATH}, F_{RTD_MEAS}, and F_{NTC_Sensor}. As the sensor sensitivity might change over the temperature measurement range, F_{NTC_Sensor} might also change and typically increases on the temperature corners.

Following parameters are adjustable:

- Range Shift: 1/16 and 1/4
- Input Multiplexer: TS1 or TS2

8.5 Over-Voltage and Short-Circuit Protection

The ZSSC4162D-04 is designed for a 5V supply provided by an electronic control unit (ECU). The ZSSC4162D-04 and the connected sensor elements are protected from over-voltage and reverse-polarity damage by an internal supply voltage limiter. The DOUT pin is protected from short circuits, over-voltage, and reverse polarity. These functions are described in Table 11 and are valid for operation of the ZSSC4162D-04 in the application circuit shown in section 12 within the specifications of absolute maximum ratings given in section 4.

Note: The specified junction temperature range T_J (Table 2) is in force not only for operation but also for all protection cases listed in Table 11. In the event of an over-voltage, the device might have increased power dissipation. Depending on the sensor elements and the output load, this may lead to a violation of the maximum junction temperature.

Table 11. Over-Voltage, Reverse-Polarity, and Short Circuit Protection

Specification	Symbol	Parameter	Description	Min	Typ	Max	Unit
Over-Voltage and Reverse-Polarity Protection							
DS_085	V_{VDDE_OV1}	Maximum voltage at VDDE to VSSE	Independent of resistance between DOUT and VSSE or VDDE	0		18	V
DS_086	V_{VDDE_OV2}	Maximum voltage at VDDE to DOUT [1]	Independent of resistance between VSSE and DOUT or VDDE	0		18	V
DS_087	V_{DOUT_OV1}	Maximum voltage at DOUT to VSSE	Independent of resistance between VDDE and DOUT or VSSE	0		18	V
DS_088	V_{DOUT_OV2}	Maximum voltage at DOUT to VDDE[1]	Independent of resistance between VSSE and DOUT or VDDE	0		18	V
DS_089	V_{VSSE_OV1}	Maximum voltage at VSSE to VDDE[1]	Independent of resistance between DOUT and VSSE or VDDE	0		18	V
DS_090	V_{VSSE_OV2}	Maximum voltage at VSSE to DOUT[1]	Independent of resistance between VDDE and DOUT or VSSE	0		18	V

Specification	Symbol	Parameter	Description	Min	Typ	Max	Unit
Short Circuit Protection							
DS_091	$I_{VDDA\_SHRT\_VSSA}$	Current limitation in the event of a VDDA to VSSA short circuit	The output is deactivated (high Z). The supply current is limited to 60mA.			60	mA
DS_092	$I_{DOUT\_SHRT\_VSSE}$	Current limitation in the event of a DOUT to VSSE short circuit	Output is activated, output current limitation has been adjusted	-10		-2	mA
DS_093	$I_{DOUT\_SHRT\_VDDE}$	Current limitation in the event of a DOUT to VDDE short circuit	Output is activated, output current limitation has been adjusted	2		10	mA

1. Reverse polarity condition.

9. Fault-Safe Operation

9.1 Fault-Safe Operation Modes

Fault checks verify the operation of the ZSSC4162D-04 and of the connected sensing elements at power-on and during Normal Operation Mode (NOM). If a fault is detected, the Diagnostic Mode (DM) is activated and the fault status is provided via one of the two methods described below depending on the diagnostic mode.

The ZSSC4162D-04 differentiates between two DMs with different behavior: Static Diagnostic Mode and Temporary Diagnostic Mode.

9.1.1. Static Diagnostic Mode

- Measurement and conditioning cycle are interrupted.
- SENT transmission is stopped; the output pin DOUT is driven to high level.
  Except if the static DM is caused by supply under-voltage (VDDAPOR, VDDDBOD), which switches the DOUT pin to high-impedance.
- The ZACwire™ interface for one-wire communication (OWI) is enabled; both RAM output pages are readable. The command StrtCmdMd must be sent to switch to Command Mode for further command processing.
- The watchdog can trigger the Static Diagnostic Mode (or a full chip reset, depending on customizable settings)
- The ZSSC4162D-04 can be restarted by a power-off/power-on sequence.

9.1.2. Temporary Diagnostic Mode

- Measurement and conditioning cycle are continuously processed.
- Fault checks are continuously processed including fault filtering.
- The ZSSC4162D-04 returns to Normal Operation Mode (NOM) including SENT transmission of valid sensor signal if fault checks do not detect continuation of fault conditions.

9.1.3. Fault Confirmation

The fault confirmation of the ZSSC4162D-04 is defined as follows:

- Fault confirmation is only processed for fault checks assigned to the Temporary DM.
- Fault confirmation is a low-pass filter that delays the activation and deactivation of the Temporary DM.
- In the event of a fault detection, faults are re-checked before entering Temporary DM.
- In the case of Temporary DM, detected fault conditions that no longer exist are re-checked before returning from Temporary DM to NOM.
- Fault confirmation (debouncing) can be enabled/disabled in configuration.

9.2 Fault Messaging

9.2.1. Overview

The SENT interface offers three different options for fault messaging:

- Fault codes in the data channels (the Fast Channels as well as the SDM Channels; for example, the channel used for temperature)
- Two status bits in the SENT status nibble
- SDM Channel status word

9.2.2. SENT Fast Channel Fault Codes

For the 12-bit SENT Fast Channel, the output value interval [4089, 4095] is reserved for fault codes. This is according to the SENT standard. In addition, the value 0 is used to signal initialization (no valid data available).

In the ZSSC4162D-04, the SENT Fast Channel fault codes are selectable, and a dedicated fault code must be assigned to every supervised fault. A fault prioritization is available, and in the event of simultaneous detection of multiple faults, the fault code of the highest prioritized fault is transmitted.

9.2.3. SENT Status Bits

According to the SENT standard, the SENT status nibble contains two bits for status information. The assignment of the status bits to the individual detectable faults is configurable.

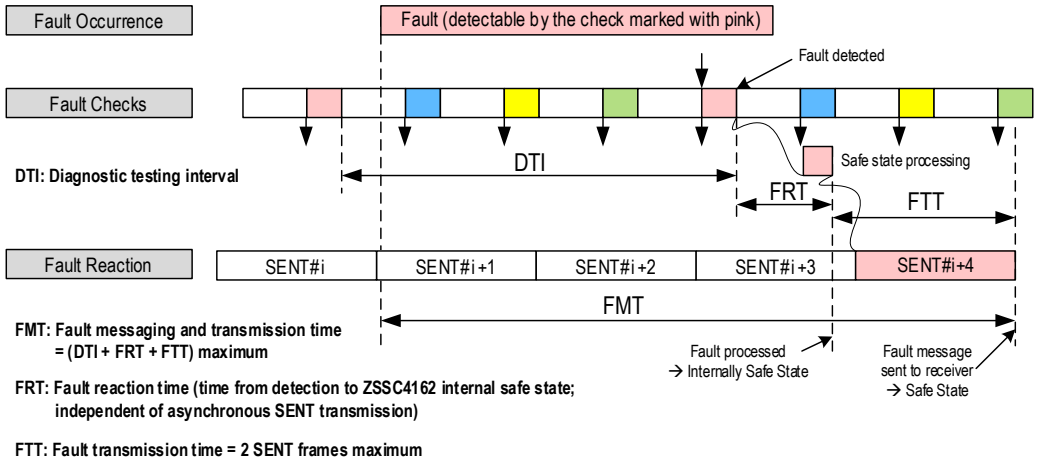
9.2.4. SENT SDM Channel Status Codes

The SENT standard defines an SMD channel status word assigned to the SDM identifier #01.

In the ZSSC4162D-04, the SENT SMD channel status codes are freely programmable, and a dedicated fault code must be assigned to every supervised fault. A fault prioritization is available, and in the event of simultaneous detection of multiple faults, the status code of the highest prioritized fault is transmitted.

9.2.5. Timing Definitions

The timing for the fault messaging is defined in Figure 5. See Table 4 for the fault messaging time (FMT) specifications. Refer to the *ZSSC4162D-04 Functional Description* document regarding the timing for the diagnostic testing interval (DTI). This document is available on request from Renesas.



Note: colors indicate the fault checks processed in the cycle.

Figure 5. Fault Messaging Timing Diagram

10. Fault Checks

10.1 Overview

The ZSSC4162D-04 implements a diagnostic mechanism architecture that can support end-user applications up to ASIL B requirements in regard to random failure diagnostic capabilities. Table 12 lists the available fault checks.

Table 12. Fault Checks Overview

Specification	Identifier	Fault Check
ZSSC4162D-04 Self-Supervision Fault Checks		
DS_094	VDDAPOR	Analog supply voltage V_{VDDA} under-voltage check; power-on reset (POR)
DS_095	VDDDBOD	Digital supply under-voltage check; brownout detection (BOD)
DS_096	OSCFAIL	Oscillator-fail check based on a second oscillator/timer; reset after oscillator restart
DS_097	ROMCRC	ROM content CRC check
DS_098	NVMCRC	NVM content CRC check
DS_099	RAMCRC	RAM content CRC check
DS_100	RAMPRTY	RAM content parity check
DS_101	WWDG	Windowed watchdog; microcontroller and measurement and conditioning cycle active check
DS_102	INITCRC	Measurement and conditioning initialization check; processing, order, and configuration
DS_103	MCYCCRC	Measurement cycle operation check; processing, order, and configuration
	AFEMUX	AFE input multiplexer operation check
	REGCRC	Configuration register content CRC check
DS_104	CCYCCRC	Conditioning cycle operation check; processing, order, and configuration
DS_105	SENTDATA	SENT data consistency check
DS_106	SENTPHY	SENT transmission monitoring
DS_107	CHIPP	Chipping check
DS_108	COMP	Computational check; microcontroller conditioning calculation, code processing, and peripheral bus access check
DS_109	VDDDRNG	Digital supply voltage range check; digital core and memory supply
DS_110	ADCOFFSRNG	ADC offset range check; ADC operation check
DS_111	AFEGAIN	AFE gain check
DS_112	VDDARNG	Analog supply voltage V_{VDDA} range check; front-end and sensor supply
DS_200	AFEBGRNG	AFE bandgap check
Sensing Element Fault Checks		
DS_113	BRSC	Bridge sensor connection check
DS_114	BRSS	Bridge sensor short check
DS_115	BRSCMRNG	Common mode range check
DS_116	TSI	Internal temperature sensor operation check
DS_117	TSEC	External temperature sensor connection check
Environment and Operating Condition Fault Checks		
DS_118	BRSRNGH	Bridge sensor conditioning result range check: upper limit
DS_119	BRSRNGL	Bridge sensor conditioning result range check: lower limit
DS_120	TSIRNG	Internal temperature sensor range check (over-temperature/under-temperature)
DS_121	TSERNG	External temperature sensor range check (over-temperature/under-temperature)
DS_210	TSEPBSN	Internal/external temperature sensor plausibilization
DS_122	VDDEUV	Supply voltage V_{VDDE} under-voltage check
DS_123	VDDEOV	Supply voltage V_{VDDE} over-voltage check
DS_124	CSAT	Conditioning calculation saturation check

10.2 Fault Checks for ZSSC4162D-04 Self-Supervision

The ZSSC4162D-04 provides several fault checks which supervise the ZSSC4162D-04 hardware itself.

Table 13. ZSSC4162D-04 Hardware Fault Checks

Requirement	Fault Check	Messaging Time	Adjustable	Active [1]	DM Type	Priority [2]
DS_094	V_{VDDA} under-voltage check (VDDAPOR); power-on reset	< 200µs	–	Always on	Static	0
DS_095	Digital supply under-voltage check (VDDDBOD); brownout detection	< 200µs	–	Always on	Static	0
DS_096	Oscillator fail check (OSCFAIL)	< 200µs	–	Always on	Static	0
DS_097	ROM CRC check (ROMCRC)	< FMT	–	Always on	Static	0
DS_098	NVM CRC check (NVMCRC)	$t_{STARTUP}$	Page-wise 16-bit CRC	Always on	Static	0
DS_099	RAM CRC check (RAMCRC)	< FMT	Page-wise 16-bit CRC	Always on	Static	0
DS_100	RAM parity check (RAMPRTY)	< FMT	–	Always on	Static	0
DS_101	Windowed watchdog (WWDG)	< 2 × OUR	–	Always on	Static	0
DS_102	Initialization phase check (INITCRC, INITCOND)	$t_{STARTUP}$	16-bit CRC	Enabled [3]	Static	0
DS_103	Measurement cycle check (MCYCCRC) including AFE input multiplexer check (AFEMUX) Register data check (REGCRC)	< FMT	16-bit CRC	Enabled [3]	Static	0
DS_104	Conditioning cycle check (CCYCCRC)	< FMT	16-bit CRC	Enabled [3]	Static	0
DS_105	SENT data consistency check (SENTDATA) 4	t_{FRAME}	–	Enabled [3]	Static	0

1. “Enable/Disable” indicates that the user can enable or disable the check.
2. Prioritization describes the default fault messaging order (“0” means highest priority) as configured in default configuration.
3. Must be enabled for FuSa application.
4. SENTDATA is applicable with some restrictions, see the *ZSSC4162D-04 Errata Sheet* document for details.

Table 14. ZSSC4162D-04 Operation and Cycle Fault Checks

Requirement	Fault Check	Messaging Time	Adjustable / Calibration	Active [1]	DM Type	Priority [2]
DS_106	SENT transmission monitoring (SENTPHY)	< FMT	Default source selection to “OUTBUF”	Enabled [3]	Temporary	1
DS_107	Chipping check (CHIPP)	< FMT	–	Enabled [3]	Temporary	1
DS_108	Computational check (COMP) including microcontroller arithmetic, code processing, and bus access	< FMT	–	Enabled [3]	Temporary	1
DS_109	Digital supply voltage check (VDDDRNG)	< FMT	Lower limit	Enabled [3]	Temporary	2
DS_110	ADC offset check (ADCOFFSRNG)	< FMT	Lower/upper limit	Enabled [3]	Temporary	2
DS_111	AFE gain check (AFEGAIN)	< FMT	Lower/upper limit	Enabled [3]	Temporary	3
DS_173	Full-bridge sensor raw data check (BRSRAW)	< FMT	Lower/upper limit	Enabled [3]	Temporary	3

Requirement	Fault Check	Messaging Time	Adjustable / Calibration	Active [1]	DM Type	Priority [2]
DS_112	Analog supply voltage check (VDDARNG)	< FMT	Lower/upper limit	Enabled [3]	Temporary	14

1. "Enabled/Disabled" indicates that the user can enable or disable the check/safety mechanism depending on application constraints.
2. Prioritization describes the default fault messaging order ("0" means highest priority) as configured in default configuration.
3. Must be enabled for FuSa application.

10.3 Fault Checks for Sensing Element and ZSSC4162D-04 Supervision

The ZSSC4162D-04 provides several fault checks that supervise the sensing elements.

Table 15. Sensing Element and ZSSC4162D-04 Operation related Fault Checks

Requirement	Fault Check	Messaging Time	Adjustable / Calibration	Active [1]	DM Type	Priority [2]
DS_113	Bridge sensor connection check (BRSC)	< FMT	Lower/upper limit	Enabled [3]	Temporary	5
DS_114	Bridge sensor short check (BRSS)	< FMT	Lower/upper limit	Enabled [3]	Temporary	6
DS_115	Common mode range check (CMR) including sensor input leakage check	< FMT	Lower/upper limit	Enabled [3]	Temporary	7
DS_116	Internal temperature sensor operation check (TSI)	< FMT	Lower/upper limit	Enabled [3]	Temporary	8
DS_117	External temperature sensor connection check (TSEC)	< FMT	Lower/upper limit	Enabled [3]	Temporary	9

1. "Enabled/Disabled" indicates that the user can enable or disable the check/safety mechanism depending on application constraints.
2. Prioritization describes the default fault messaging order ("0" means highest priority) as configured in default configuration.
3. Must be enabled for FuSa application.

10.4 Fault Checks for Environment and Operating Condition Supervision

The ZSSC4162D-04 provides several fault checks that supervise the environment and operating conditions.

Table 16. Environment and Operating Condition Fault Checks

Requirement	Fault Check	Messaging Time	Adjustable / Calibration	Active [1]	DM Type	Priority [2]
DS_118	Bridge sensor range check upper limit (BRSRNGH)	< FMT	Upper limit	Enabled [3]	Temporary	12
DS_119	Bridge sensor range check lower limit (BRSRNGL)	< FMT	Lower limit	Enabled [3]	Temporary	12
DS_120	Internal temperature sensor range check (TSIRNG)	< FMT	Lower/upper limit	Enabled [3]	Temporary	8
DS_121	External temperature sensor range check (TSERNG)	< FMT	Lower/upper limit	Enabled [3]	Temporary	10
DS_122	Supply V_{VDDE} under-voltage check (VDDEUV)	< FMT	Lower limit	Enabled [3]	Temporary	14

Requirement	Fault Check	Messaging Time	Adjustable / Calibration	Active [1]	DM Type	Priority [2]
DS_123	Supply V_{VDDE} overvoltage check (VDDEOV)	< FMT	Upper limit	Enabled [3]	Temporary	13
DS_124	Conditioning calculation saturation (CSAT)	< FMT	–	Enabled [3]	Temporary	15
DS_210	Internal/external temperature sensor plausibilization (TSEPBSN)	< FMT + LPF_tc [4]	Limits and LPF adjust	Enabled [4]	Temporary	12

1. "Enabled/Disabled" indicates that the user can enable or disable the check/safety mechanism depending on application constraints.
2. Prioritization describes the default fault messaging order ("0" means highest priority) as configured in default configuration..
3. Must be enabled for FuSa application.
4. Must be enabled for FuSa application, if an external temperature sensor is used for main channel conditioning. LPF_tc – the low pass filter time constant – must be added, if the LPF is activated

Table 17. External SENT Transmission Fault Checks [1]

Fault Check	Messaging Time	DM Type, Notes
SENT CRC (SENTCRC)	t_{FRAME}	External, SENT receiver
SENT tick time (SENTTICK)	t_{FRAME}	External, SENT receiver
SENT timeout (SENTIMEOUT)	t_{FRAME}	External, SENT receiver
SENT sync time (SENTSYNC)	t_{FRAME}	External, SENT receiver

1. SENT transmission fault checks must be implemented at the SENT receiver.

10.5 Fault Check Limit Settings

10.5.1. Limits Types and Measurement Uncertainties

ZSSC4162D-04 provides several fault checks based on the monitoring of a physical value, see the *ZSSC4162D-04 v1.0 Functional Safety Manual* document for details.

10.5.2. Technical Details

BRSRAW

The limits of the ADC raw data check must be adjusted depending on the selected ADC resolution for the full-bridge measurement. The ADC raw data measurement register range is [0, 2^15). If the resolution is higher than 14 bit, the digital zooming is activated and the range of the ADC results is different.

TSEC

TSEC must be adapt to the transfer characteristic of the connected external pn-junction temperature sensor:

- LOW_{MAX}: Smaller than minimum flow voltage V_F of the diode in application temperature range, excitation current tolerance and full process range (production spread). Additional 50mV measurement uncertainty has to be subtracted from this value for limit calculation (see the *ZSSC4162D-04 Functional Description* document).
- UPP_{MIN}: Greater than maximum flow voltage V_F of the diode in application temperature range, excitation current tolerance and full process range (production spread). Additional 50mV measurement uncertainty has to be added to this value for limit calculation (see the *ZSSC4162D-04 Functional Description* document).

BRSS/BRSC (+BRSCMRNG for BRSC)

Detection thresholds have to be rated in relation to sensor fault model by customer/sensor module assembler, refer to the *ZSSC4162D-04 Functional Description* document.

TSIRNG/TSERNG

Must be adjusted based on application requirements refer to the *ZSSC4162D-04 Functional Description* document for a calibration instruction.

TSEPBSN

Must be adjusted based on application requirements if an external temperature sensor is used for main channel conditioning, refer to the *ZSSC4162D-04 Functional Description* document for a configuration and calibration instructions.

BRSRNGL/BRSRNGH

Must be assigned related to selected main channel resolution.

VDDE/VDDA limit calibration – VDDEUV/VDDEOV/VDDARNG

Must be adjusted based on application supply voltage range or calibrated, refer to the *ZSSC4162D-04 Functional Description* document for a calibration instruction.

AFEBGRNG

Must be calibrated, refer to the *ZSSC4162D-04 Functional Description* document for a calibration instruction.

BRSCMRNG/AFEGAIN Calibration

Refer to the *ZSSC4162D-04 Functional Description* document for a calibration instruction.

SENTDATA Check

SENTDATA check processing can be influenced from RAM data update: an access conflict can occur, which leads to unintended activation of the Static Diagnostic mode. Solve the conflict by either of the following workarounds:

- Disabling of SENTDATA check: ASIL B metrics are fulfilled further on under this condition
- Enabled SENTDATA check and SENT tick time adjust ≥4us
- Enabled SENTDATA check and application set up based on the constraints in Table 18.

Table 18. SENTDATA Check Workaround

Configuration Block	Parameter	Required Parameter Value
Bridge1 Output	DataDivision	1/8
Block SENT Output, Bridge1 Cm SENT Output, Chip-Temp SENT Output, Diode1 Output	Channel	Must NOT be set to either FcReg1 or FcReg2
Config Sent	FC Data Format	SAE H.4
Bridge1 Measurement	SettleTime / AdcRsl	1 / 14 Bit
Bridge1 Low-Pass	Diff / Avrg	0 / 0

1. The correct function of the IC is verified for these parameter adjusts/values. All these parameters values are the default setting of the configuration.

Traceability

A ZSSC4162D-04 device can be identified by the product code 0xF1D1, which can be read out by the “RdProductVerCode” command.

11. Configuration and Adjustment

The ZSSC4162D-04 is based on a dedicated configuration that must be adjusted for the application. This includes the adjustment of the parameters for the configuration of the sensor signal measurements (see Table 19), the calibration of the sensor conditioning calculation (see Table 20 and Table 22), and the setup of the SENT protocol (see Table 21).

Table 19. Sensor Signal Measurement Configuration

Specification	Parameter	Conditions	Value
DS_127	Gain P1	Full-bridge sensor signal gain	2…200 (as adjusted in config)
DS_129	Gain TSE	External temperature sensor signal gain	2…50 (as adjusted in config)
DS_130	Source select for BR temperature compensation	Selection of the temperature signal used for temperature compensation of the main sensor signal	TSI / TSE
DS_131	Source select for SENT temperature output	Selection of the temperature signal used for the SENT temperature measurement output	TSI / TSE
DS_132	TSE type	External temperature sensor type	Diode

Table 20. Calibration of Sensor Signal Conditioning Calculation

Requirement	Parameter	Conditions	Value	Unit
DS_133	Full-bridge signal offset compensation	Coefficients for 2nd order temperature compensation (number of coefficients)	4	16-bit words
DS_134	Full-bridge signal gain compensation	Coefficients for 2nd order temperature compensation (number of coefficients)	4	16-bit words
DS_135	Full-bridge signal nonlinearity compensation	Coefficients for 3rd order nonlinearity compensation (number of coefficients)	5	16-bit words
DS_136	Full-bridge signal filter	Conditioned full-bridge signal filter: average and differential coefficients	1	16-bit words
DS_141	Temperature TSI conditioning	Temperature from internal temperature sensor; coefficients for gain, offset, and 2nd order nonlinearity compensation	4	16-bit words
DS_142	Temperature TSI filter	Conditioned internal temperature signal filter: average and differential coefficients	2	–
DS_143	Temperature TSE conditioning	Temperature from external temperature sensor; coefficients for gain, offset, and 2nd order nonlinearity compensation	4	16-bit words
DS_144	Temperature TSE filter	Conditioned external temperature signal filter: average and differential coefficients	2	–
DS_145	Common mode voltage offset compensation	Coefficients for 2nd order temperature compensation and 1st order bridge sensor signal compensation	5	16-bit words
DS_146	Common mode voltage gain compensation	Coefficients for 2nd order temperature compensation and 1st order bridge sensor signal compensation	5	16-bit words

Table 21. SENT Protocol Configuration

Requirement	Parameter	Conditions	Value	Unit
DS_147	Tick time	Clock tick time: adjustable minimum/maximum value	3 to 90	µs
		Clock tick time: worst case minimum/maximum range in PVT	2.4 to 108	
DS_148	Frame length	Enables constant frame length	282 to 1024	Clock ticks
DS_149	Sensor type	Single Sensor (P/t), Single Secure Sensor (P/S/t), Pressure Temperature Sensor (P/T/t)	Selectable	–
DS_151	SDM priority	Up to 3 priority levels	Configurable	–
DS_152	SDM ID	SDM identifier	Programmable	–
DS_153	SDM data	Static SDM data	Programmable	–
DS_154	SDM initial data	Initial data for SDM signal channels	Programmable	–
DS_155	Temperature SDM	Priority level for SENT SDM channel of conditioned temperature output	Configurable	–
DS_156	Status SDM	Diagnostic codes	Programmable	–

Table 22. Fault Handling Configuration

Requirement	Parameter	Conditions	Value	Unit
DS_157	Watchdog reset	The Static Diagnostic Mode results in a functional halt or in a reset after watchdog timeout	Selectable	–
DS_158	BRSRNGH limits	Full-bridge sensor conditioning result check upper limit	Upper limit	16-bit words
DS_159	BRSRNGL limits	Full-bridge sensor conditioning result check lower limit	Lower limit	16-bit words
DS_161	TSIRNG limits	Internal temperature sensor range check limits	Upper limit, lower limit	16-bit words
DS_162	TSE limits	External temperature sensor connection check limits	Upper limit, lower limit	16-bit words
DS_163	TSERNG limits	External temperature sensor range check limits	Upper limit, lower limit	16-bit words
DS_164	CMR limits	Common mode voltage check limits	Upper limit, lower limit	16-bit words
DS_165	AFEGAIN input	AFE gain check input voltages	2 AFEDAC configurations	16-bit words
DS_166	AFEGAIN limits	AFE gain check limits	2 upper limits, 2 lower limits	16-bit words
DS_167	COMP input	Computation check input value	Input value	16-bit word
DS_168	COMP limits	Computation check limits	Upper limit, lower limit	16-bit words
DS_200 1	MCYCCRC value	Measurement cycle check expected CRC	Initial CRC, cycle CRC	16-bit words
DS_201 1	CCYCCRC value	Conditioning cycle check expected CRC	Initial CRC, cycle CRC	16-bit words

1. Generation of the expected CRCs for MCYCCRC and CCYCCRC fault checks is supported by a dedicated command. This CRC generation must be processed/done in final calibration of the DUT.

12. Application Circuit and External Components

Table 23. Application Circuit Example with Full-Bridge Input BR1

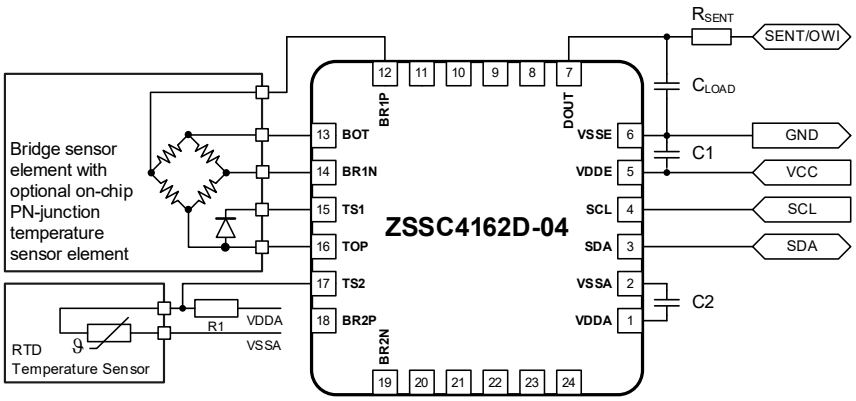
Specification	Circuit Diagram
DP_043	 Application features: ▪ 5V module is powered by the application's electronic control unit (ECU) ▪ Sensor module with 3-pin connector provides pressure and media or ambient temperature measurement data via SENT output ▪ Temperature signal for pressure signal correction can be derived either from the on-chip PTAT or from an external diode (connected to TS1 or TS2) ▪ End-of-line calibration uses one-wire communication via the DOUT pin

Table 24. Dimensioning of External Components for the Application Example

Specification	Component	Symbol	Conditions	Min	Typical	Max	Unit
DP_044	Capacitor	C1	$V_{MAX} \geq 32V$		100 ± 20%		nF
	Capacitor	C2	$V_{MAX} \geq 10V$		100 ± 20%	470 + 20%	nF
	Capacitor	C_{LOAD}	$V_{MAX} \geq 32V$		2.2 ± 20%		nF
	Resistor	R_{SENT}				50	Ω

1. The component values are examples and must be adapted to the requirements of the application, in particular to the EMC requirements.

13. ESD Protection and EMC Specification

13.1 ESD Protection

All pins have an ESD protection of up to 2kV according to the Human Body Model (HBM with 1.5kΩ/100pF, based on MIL883, Method 3015.7). The VDDE, VSSE, and DOUT pins have an additional ESD protection of up to 4kV (HBM with 1.5kΩ/100pF, based on MIL883, Method 3015.7).

The levels of ESD protection are tested with devices in a 4mm × 4mm 24-QFN package during the product qualification.

13.2 Electromagnetic Emission

The conducted emission of the externally connected pins of the ZSSC4162D-04 is measured according to the following standard: IEC 61967_4:2002 + A1:2006.

Measurements must be performed with the application circuit described in Table 23; SENT transmission uses a tick time of 9µs.

For the off-board pins, the spectral power measured with the 150Ω method must not exceed the limits according to IEC 61967_4k, Annex B.4 Code H10kN. For the VSSE pin, the spectral power measured with the 1Ω method must not exceed the limits according to IEC 61967_4k, Annex B.4 code H10kN.

13.3 Conducted Susceptibility (DPI)

The conducted susceptibility of externally connected pins of the device is measured according to the IEC 62132-4 standard:

Measurements must be performed with the application circuit described in Table 23; the sensor bridge is replaced by a 3-resistor string connected to TOP, BR1P, BR1N, and BOT; SENT transmission uses a tick time of 9µs.

Table 25 gives the specifications for the DPI tests. RES refers to the coupling impedance. CAP refers to the injection capacitance.

Table 25. Conducted Susceptibility (DPI) Tests

Requirement	Test	Frequency Range	Power [dBm]	Load Pins	Protocol	Error Band[1]	Comment
DS_169	DPI, direct coupled	1MHz to 10MHz	20	VDDE, DOUT	SENT	±1%	RES = 50Ω CAP = 4.7nF
DS_170	DPI, direct coupled	>10MHz	30	VDDE, DOUT	SENT	±1%	RES = 50Ω CAP = 4.7nF

1. Error band regarding main signal (SENT FC1).

14. Reliability and RoHS Conformity

The ZSSC4162D-04 is qualified according to the AEC-Q100 standard, operating temperature grade 0. The ZSSC4162D-04 complies with the RoHS directive and does not contain hazardous substances. The complete RoHS declaration update can be downloaded at https://www.renesas.com/eu/en/document/cer/green-products-rohs-material-declaration-certificate.

14.1 Calculation of Power Dissipation and Junction Temperature

Calculation examples for self-heating (maximum thermal resistor in 24-QFN package is Rth_JA_QFN24 = 32K/W):

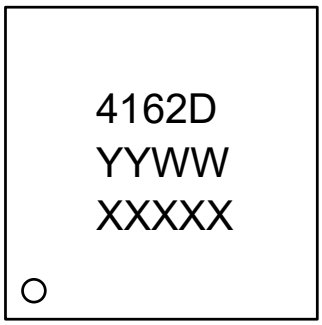
- Normal Operation:
  Maximum supply current at 5.5V is 10mA. Minimum SENT load resistance of 10kΩ.
  Maximum power dissipation is P_{max} = 5.5V × 10mA + 5.5V × 5.5V / 10kΩ = 58mW.
  Temperature difference: T_J – T_{AMB} = 32K/W × 58mW = 1.9K.
  → With the conditions above, the maximum junction temperature T_J is ~2K greater than the ambient temperature T_{AMB}.
- Over-voltage conditions (18V):
  Maximum power dissipation is $P_{max,OV}$ = 300mW, output is switched off.
  Temperature difference: T_J - T_{AMB} = 32K/W × 300mW = 9.6K
  → With these conditions, the maximum junction temperature T_J is ~10K greater than the ambient temperature T_{AMB}.

15. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

Package Outline Drawing Package Code: NLG24S2 24-VFQFPN 4.0 x 4.0 x 0.85 mm Body, 0.5mm Pitch

16. Marking Diagram



“4162D” is the truncated part number.

“YYWW” is the last digits of the year and week that the part was assembled.

“XXXXX” is the last digits of the lot number.

17. Ordering Information

Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
ZSSC4162DE4R-APB	Single bridge input, SENT output, internal and/or external temperature measurement, QFN24 (4x4), wettable flanks, Config v1.0	MSL1	13” Reel	-40°C to 150°C
ZSSC4160EVKV1P5	ZSSC416x SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, 10 Samples.			

Contact Renesas for additional options.

18. Glossary

Term	Description	Term	Description
ADC	Analog-to-Digital Converter	LSN	Least Significant Nibble
AEC	Automotive Electronics Council	MSB	Most Significant Bit
AFE	Analog Front-End	MSN	Most Significant Nibble
(A) SIL	(Automotive) Safety Integrity Level	MUX	Multiplexer
BIST	Build in Self Test	MTP	Multiple-Time Programmable
BOD	Brownout Detection	n.a.	Not Applicable
BR	Bridge Sensor	n.c.	Not Connected
CM	Command Mode	NOM	Normal Operation Mode
CMC	Calibration Microcontroller	NVM	Nonvolatile Memory
CMV	Common Mode Voltage	OTP	One-Time Programmable
DAC	Digital Analog Converter	OUR	Output Update Rate
DM	Diagnostic Mode	(O) RT	(Output) Response Time
DNL	Differential Nonlinearity	OWI	One-Wire Interface (called ZACwire™ also)
DS	Data Sheet	PCB	Printed Circuit Board
DTI	Diagnostic Testing Interval	PGA	Programmable Gain Amplifier
ECU	Electronic Control Unit	POR	Power-On Reset
EMC	Electromagnetic Compatibility	PTAT	Proportional-to-Absolute Temperature
ESD	Electrostatic Discharge	PWR	Power Management and Protection Unit
FD	Function Description	QFN	Quad-Flat No-Leads
FIT	Failure In Time	RAM	Volatile Memory for Configuration and Conditioning Coefficients
FHTI	Fault Handling Time Interval	RISC	Reduced Instruction Set Computing
FMT	Fault Messaging Time; latency from the fault event to the completion of the transmission of the fault message	ROM	Read-Only Memory
FS	Full Scale	SCCM	Sensor Check and Common Mode Adjustment Unit
FSM	Functional Safety Manual	SEooC	Safety Element out of Context

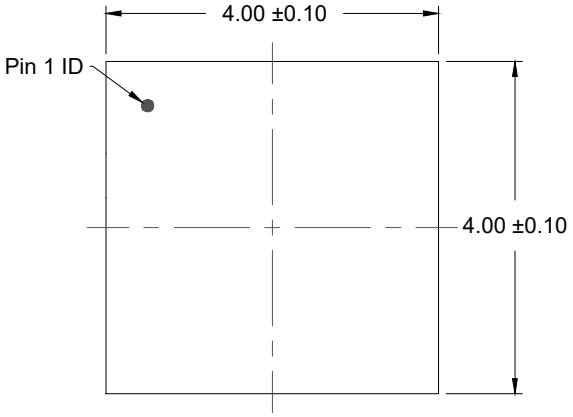
Term	Description	Term	Description
FTT(I)	Fault Transmission Time (Interval)	SG	Safety Goal
FuSa	Functional Safety	SM	Safety Mechanism
HBM	Human Body Model	SPF(M)	Single Point Fault (Metrics)
I/O	Input/Output	SSC	Sensor Short Check (diagnostic task) or Sensor Signal Conditioner
I2C	Inter-Integrated Circuit (serial two-wire data bus)	TS(I)	(Internal) Temperature Sensor
LF(M)	Latent Fault (Metrics)	TQE	Extended Temperature Range Identifier
INL	Integral Nonlinearity	ZACwire™	Renesas-specific one-wire interface (OWI)
LSB	Least Significant Bit		

19. Revision History

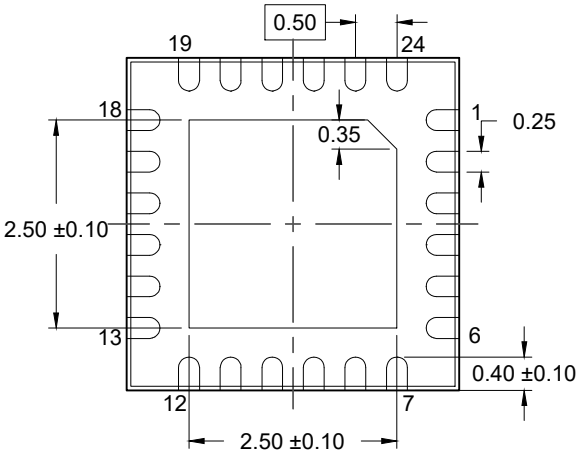
Revision	Date	Description
2.30	Apr 23, 2026	▪ Updated QFN-20L package recommendation (see “Pin Assignments”) ▪ Split programming time into 2x parameters (see “Interface Characteristics and Nonvolatile Memory”: DS_068) ▪ Completed other minor changes
2.20	Mar 19, 2025	▪ Removed preliminary status
2.10	Jan 21, 2025	▪ DS_065: decreased the max limit to 125 ▪ DS_066: Parameter changed
2.00	Jan 14, 2025	▪ Updated according to v1.0 configuration release
1.00	Jul 30, 2024	▪ Initial draft

Package Outline Drawing

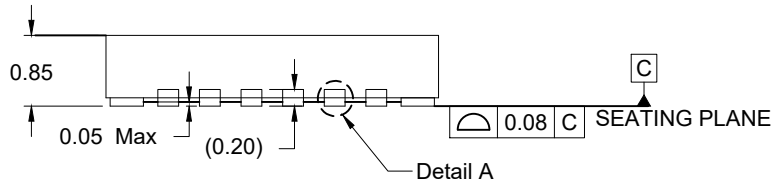
PSC-4192-05
NLG24S2
24-VFQFPN 4.0 x 4.0 x 0.85 mm Body, 0.5mm Pitch
Rev.08, Jun 20, 2025



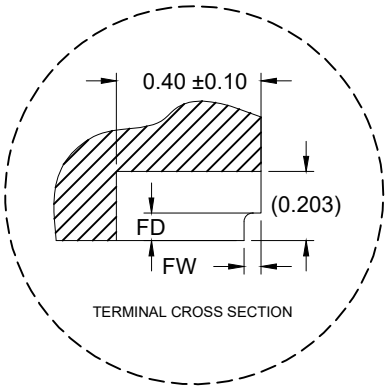
TOP VIEW



BOTTOM VIEW



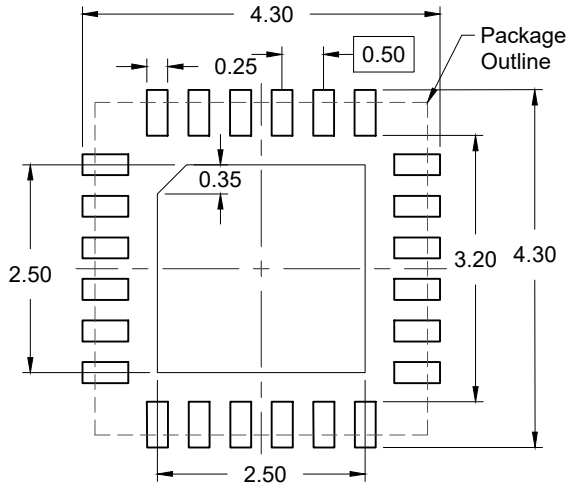
SIDE VIEW



DETAIL A

Table 1: Dimensions of wettable flank (DETAIL A)

Symbol	Unit (mm)	
	MIN	MAX
FD	0.100	-
FW	0.010	0.075



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Wettable flank (step cut).

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